REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 02 and 03. Add vendor CAGE 61772 for device types 02 and 03. Delete vendor CAGE 61772 for device type 01. Add vendor CAGE 75569 for device types 02 and 03. Technical and editorial changes throughout.	92-03-06	Michael A. Frye
B	Updated to reflect current MIL-PRF-38535 requirements.- jak	12-12-04	Thomas M. Hess

REV																				
SHEET																				
REV	B																			
SHEET	15																			

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
Jeffery Tunstall

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Ray Monnin

APPROVED BY
Donald R. Cool

DRAWING APPROVAL DATE
88-09-30

MICROCIRCUIT, DIGITAL, FAST CMOS SYNCHRONOUS PRESETTABLE BINARY, COUNTER, TTL COMPATIBLE, MONOLITHIC SILICON

REVISION LEVEL
B

SIZE	CAGE CODE	
A	**67268**	**5962-88640**

SHEET 1 OF 15

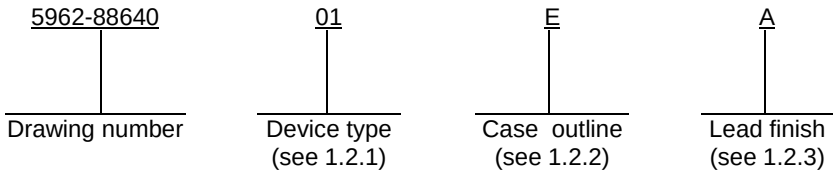
DSCC FORM 2233
APR 97

5962-E035-13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01 1/	54FCT161	Presettable binary counter, synchronous, TTL compatible
02	54FCT161	Presettable binary counter, synchronous, TTL compatible
03	54FCT161A	Presettable binary counter, synchronous, TTL compatible

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-F16	16	dual-in-line
F	GDIP1-F16 or CDFP2-F16	16	flat package
2	CQCC1-N20	20	square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1/ Due to internal noise problems, device type 01 does not meet the minimum V_{IH} threshold limits characteristic of the FCT family or the limits specified on this drawing. The device type is no longer available for acquisition.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN}) ..... -0.5 V dc to V_{CC} + 0.5 V dc 2/
DC output voltage range (V_{OUT}) ..... -0.5 V dc to V_{CC} + 0.5 V dc 2/
DC input diode current (I_{IK}) ..... -20 mA
DC output diode current (I_{OK}) ..... -50 mA
DC output current (I_{OUT}) ..... ±100 mA
Maximum power dissipation (P_D) ..... 500 mW 3/
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Junction temperature (T_J) ..... +175°C
Lead temperature (soldering, 10 seconds) ..... +300°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +4.5 V dc to +5.5 V dc
Maximum low level input voltage (V_{IL}) ..... 0.8 V dc
Minimum high level input voltage (V_{IH}) ..... 2.0 V dc 4/
Case operating temperature range (T_C) ..... -55°C to +125°C
Minimum setup time, high or low (Pn to CP) (t_{s1}):
  Device types 01 and 02 ..... 5.5 ns
  Device type 03 ..... 4.5 ns
Minimum setup time, high or low ($\overline{PE}$ to CP) (t_{s2}):
  Device types 01 and 02 ..... 13.5 ns
  Device type 03 ..... 11.5 ns
Minimum setup time, high or low (CEP, CET to CP) (t_{s3}):
  Device types 01 and 02 ..... 13.0 ns
  Device type 03 ..... 11.0 ns
Minimum hold time, high or low (Pn to CP) (t_{h1}) ..... 2.0 ns
Minimum hold time, high or low ($\overline{PE}$ to CP) (t_{h2}) ..... 1.5 ns
Minimum hold time, high or low (CEP, CET to CP) (t_{h3}) ..... 0.0 ns
Minimum CP pulse width, high, low (load) (t_{w1}):
  Device types 01 and 02 ..... 5.0 ns
  Device type 03 ..... 4.0 ns
Minimum CP pulse width, high, low (count) (t_{w2}):
  Device types 01 and 02 ..... 8.0 ns
  Device type 03 ..... 7.0 ns
Minimum MR pulse width, low (t_{w3}):
  Device types 01 and 02 ..... 5.0 ns
  Device type 03 ..... 4.0 ns
Maximum recovery time MR to CP (t_{REC}):
  Device type 01 ..... 6.0 ns
  Device type 02 ..... 5.0 ns

1/ All voltages are referenced to ground.
2/ For V_{CC} > 6.5 V dc, the upper bound is limited to V_{CC}.
3/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.
4/ For dynamic operation of device type 01, a V_{IH} level between 2.0 V and 3.0 V may be recognized by this device as a high logic level input. For static operation of device type 01, a VIH ≥ 2.0 V will be recognized by these devices as a high logic level input. Users are cautioned to verify that this change will not affect their system.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.4 Logic diagram(s). The logic diagram(s) shall be as specified on figure 3.

3.2.5 Counting sequence. The counting sequence shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full (case or ambient) operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V dc ±10% unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits		Unit
						Min	Max	
High level output voltage	V_{OH} 1/	V_{IL} = 0.8 V V_{IH} = 2.0 V I_{OH} = -300 µA	All	4.5 V	1, 2, 3	4.3		V
		V_{IL} = 0.8 V V_{IH} = 2.0 V I_{OH} = -12 mA	All	4.5 V		2.4		
Low level output voltage	V_{OL} 1/	V_{IL} = 0.8 V V_{IH} = 2.0 V I_{OL} = 300 µA 2/	All	4.5 V	1, 2, 3		0.2	V
		V_{IL} = 0.8 V V_{IH} = 2.0 V I_{OL} = 32 mA	All	4.5 V			0.5	
Input clamp voltage	V_{IK}	I_{IN} = -18 mA	All	4.5 V	1		-1.2	V
High level input current	I_{IH}	V_{IN} = 5.5 V	All	5.5 V	1, 2, 3		5.0	µA
Low level input current	I_{IL}	V_{IN} = GND	All	5.5 V	1, 2, 3		-5.0	µA
Short circuit output current	I_{OS} 3/		All	5.5 V	1, 2, 3	-60		mA
Quiescent power supply current (CMOS inputs)	I_{CCQ}	$V_{IN} \le 0.2$ V or $V_{IN} \ge 5.3$ V f_i = 0 MHz	All	5.5 V	1, 2, 3		1.5	mA
Quiescent power supply current (TTL inputs)	ΔI_{CC} 4/	V_{IN} = 3.4 V	All	5.5 V	1, 2, 3		2.0	mA
Dynamic power supply current	I_{CCD} 5/	$V_{IN} \le 0.2$ V or $V_{IN} \ge 5.3$ V MR = V_{CC} Outputs open, one bit toggling 50% duty cycle	All	5.5 V	3/		0.4	mA/ MHz
Total power supply current	I_{CC} 6/	f_{CP}= 10 MHz Outputs open, $V_{IN} \ge 5.3$ V or $V_{IN} \le 0.2$ V One bit toggling at f_i = 5 MHz, 50% duty cycle	All	5.5 V	1, 2, 3		4.0	mA
		f_{CP}= 10 MHz Outputs open $V_{IN} \ge 3.4$ V or V_{IN} = GND One bit toggling at f_i = 5 MHz, 50% duty cycle	All	5.5 V	1, 2, 3		6.0	mA
Input capacitance	C_{IN}	See 4.3.1c	All		4		10	pF
Output capacitance	C_{OUT}	See 4.3.1c	All		4		12	pF
Functional tests	7/	See 4.3.1d	All		7, 8			

See footnotes at end of table.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V dc ±10% unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits		Unit
						Min	Max	
Propagation delay time, CP to Q (PE input high)	t_{PLH1}, t_{PHL1} 8/	C_L = 50 pF minimum R_L = 500Ω See figure 5	01, 02	4.5 V	9, 10, 11	2.0	11.5	ns
			03	4.5 V		2.0	7.5	
Propagation delay time, CP to Q (PE input low)	t_{PLH2}, t_{PHL2} 8/		01, 02	4.5 V	9, 10, 11	2.0	10.0	ns
			03	4.5 V		2.0	6.5	
Propagation delay time, CP to TC	t_{PLH3}, t_{PHL3} 8/		01, 02	4.5 V	9, 10, 11	1.5	16.5	ns
			03	4.5 V		1.5	10.8	
Propagation delay time, CET to TC	t_{PLH4}, t_{PHL4} 8/		01, 02	4.5 V	9, 10, 11	2.0	9.0	ns
			03	4.5 V		2.0	5.9	
Propagation delay time, MR to TC	t_{PHL5} 8/		01, 02	4.5 V	9, 10, 11	2.0	12.5	ns
			03	4.5 V		2.0	8.2	
Propagation delay time, CET to TC	t_{PHL6} 8/		01, 02	4.5 V	9, 10, 11	2.0	14.0	ns
			03	4.5 V		2.0	9.1	

1/ For dynamic operation of device type 01, a VIH level between 2.0 V and 3.0 V may be recognized by this device as a high logic level input. For static operation of device type 01, a V_{IH} - 2.0 V will be recognized by this device as a high logic level input. Users are cautioned to verify that this change will not affect their system.

2/ Guaranteed by testing at worst case condition of V_{CC} = 3 volts. 3/ Not more than one output should be shorted at one time Duration of the short circuit test should not exceed 1 second.

4/ In accordance with TTL driven input (VIN = 3.4 V dc); all other outputs at V_{CC} or GND. 5/ This parameter is not directly testable, but is derived for use in total power supply calculations.

6/ $I_{CC} = I_{CCQ} + (\_I_{CC} \times DH \times NT) + I_{CCD} (fcp/2 + fI \times N_I)$. Where D_H = Duty cycle for TTL inputs high. N_T = Number of TTL inputs at D_H. fI = Input frequency in MHz. N_I = Number of inputs at fI.

7/ Due to internal noise problems, device type 01 cannot meet the threshold limits required in accordance with MIL-STD-883, test method 5004, for the V_{IH} minimum limit (2.0 V) of this technology family. For device types 02 and 03, use a V_{IH} limit of 3.0 V. The VIL limit (0.8 V) remains unchanged. Users are cautioned to verify that this change will not affect their system.

8/ Minimum limits are guaranteed, if not tested on propagation delays

Device types	01, 02 and 03	
Case outlines	E and F	2
Terminal number	Terminal symbol	Terminal symbol
1	$\overline{MR}$	NC
2	CP	$\overline{MR}$
3	P_0	CP
4	P_1	P_0
5	P_2	P_1
6	P_3	NC
7	CEP	P_2
8	GND	P_3
9	$\overline{PE}$	CEP
10	CET	GND
11	Q_3	NC
12	Q_2	$\overline{PE}$
13	Q_1	CET
14	Q_0	Q_3
15	TC	Q_2
16	V_{CC}	NC
17		Q_1
18		Q_0
19		TC
20		V_{CC}

Terminal symbol	Description
CEP	Count enable parallel input
CET	Count enable trickle input
CP	Clock pulse input (active rising edge)
$\overline{MR}$	Asynchronous master reset input (active low)
P_{0-3}	Parallel data inputs
PE	Parallel enable input (active low)
Q_{0-3}	Flip- flop outputs
TC	Terminal count output

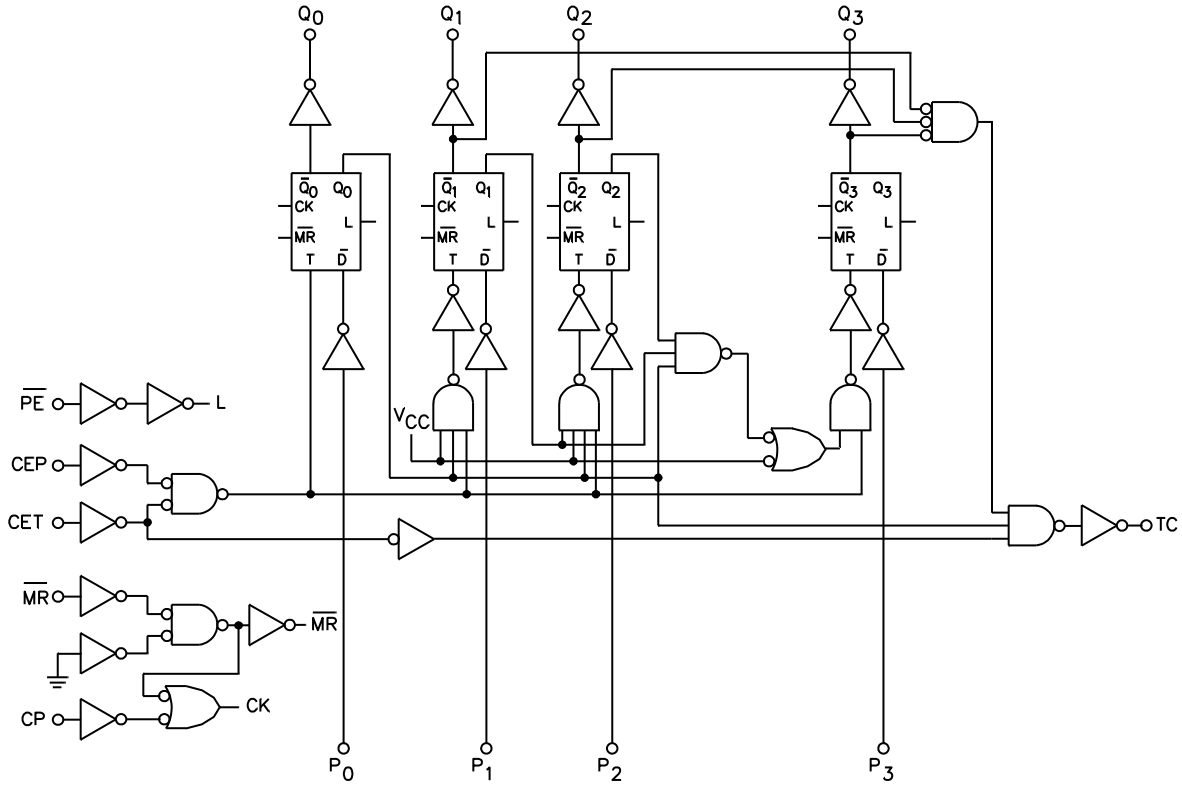
FIGURE 1. Terminal connections.

MR	PE	CET	CEP	Function
L	X	X	X	Reset (clear)
H	L	X	X	Load (P_n to Q_n) (see note)
H	H	H	H	Count (increment) (see note)
H	H	L	X	No change (hold) (see note)
H	H	X	L	No change (hold) (see note)

H = High voltage level steady state
L = Low voltage level steady state
X = Irrelevant

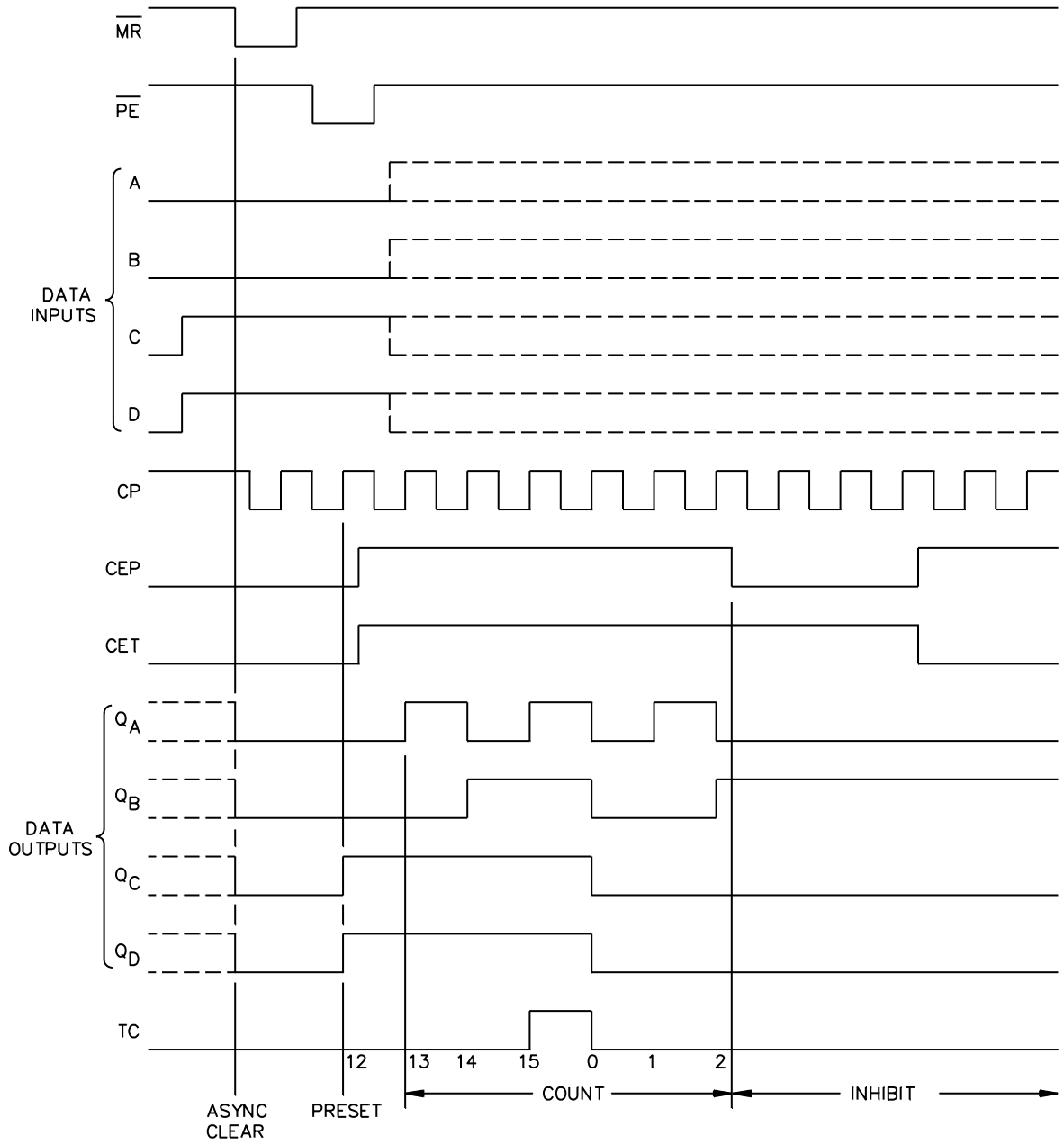
Note: Action is on the rising clock edge.

FIGURE 2. Truth table.



CK = Internal clock.

FIGURE 3. Logic diagram.



Sequence is as follows
1. Clear outputs to zero
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit

Figure 4 Counting sequence.

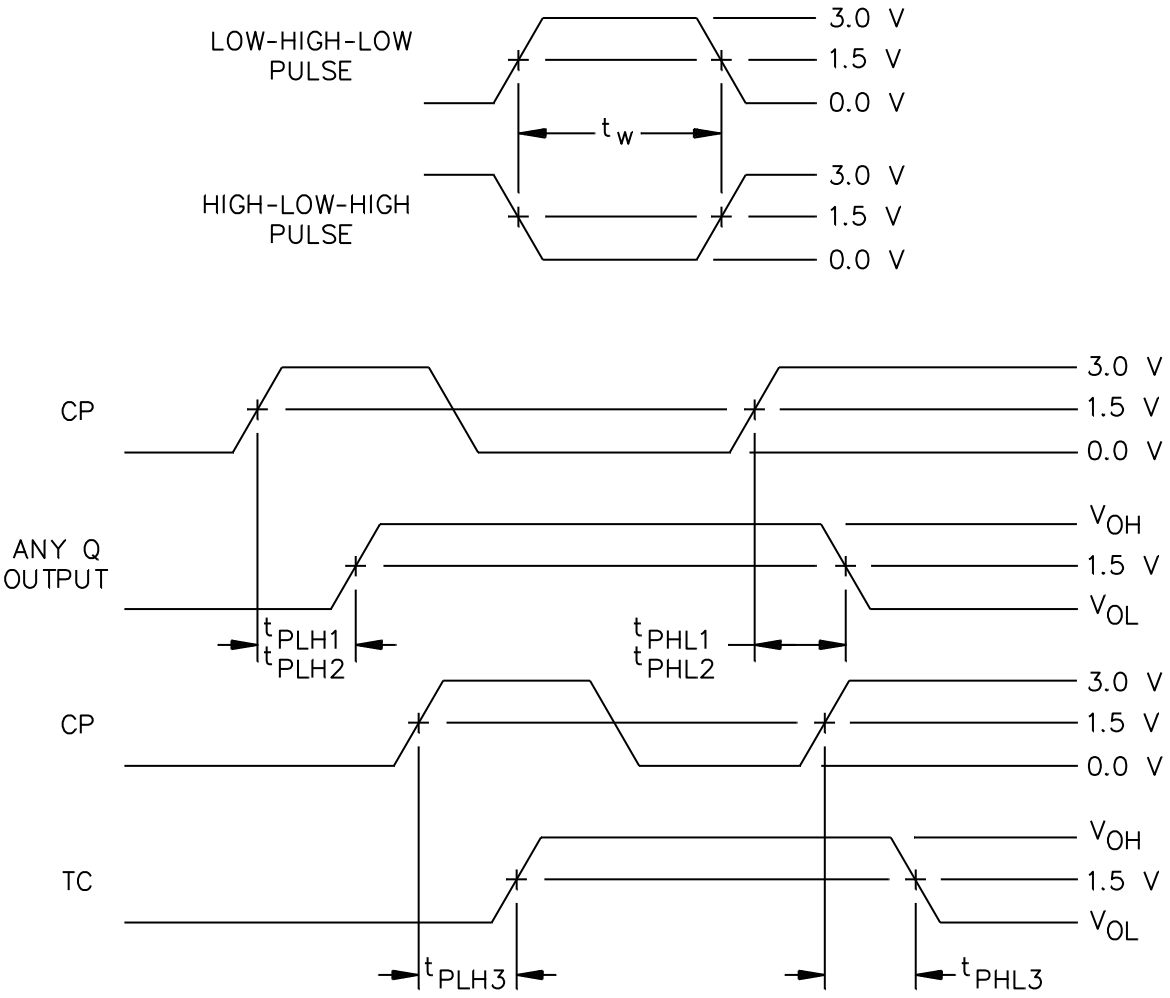
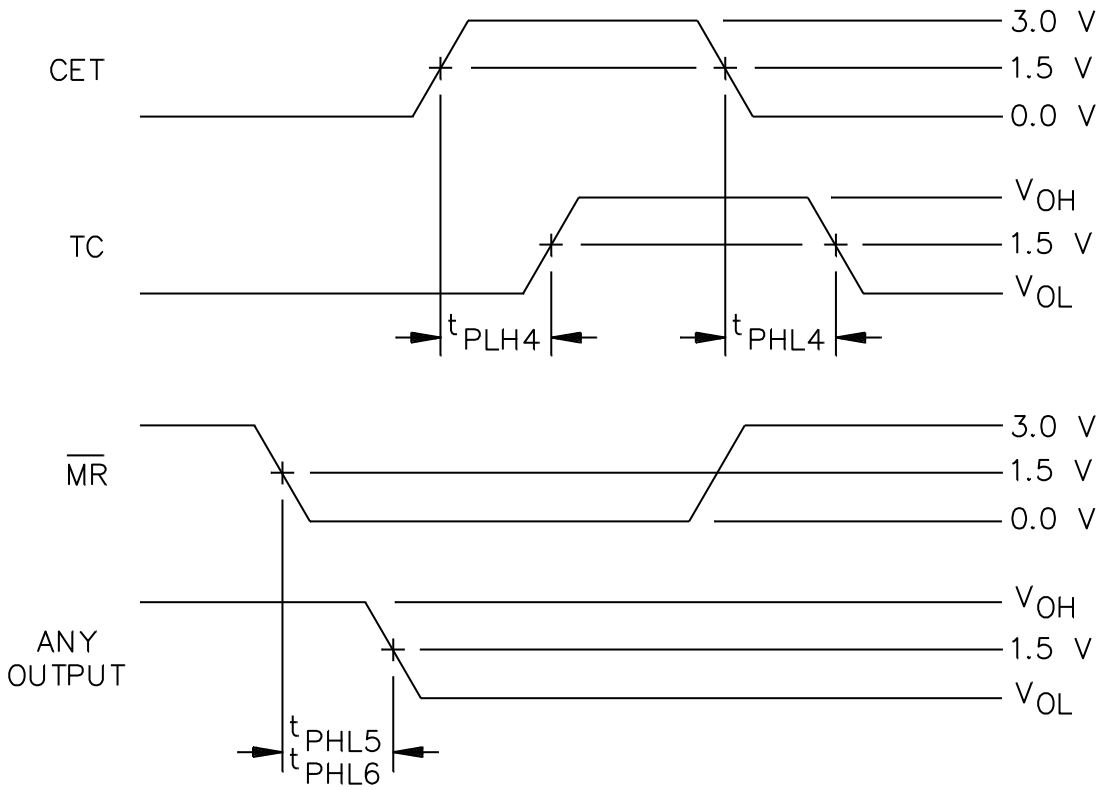
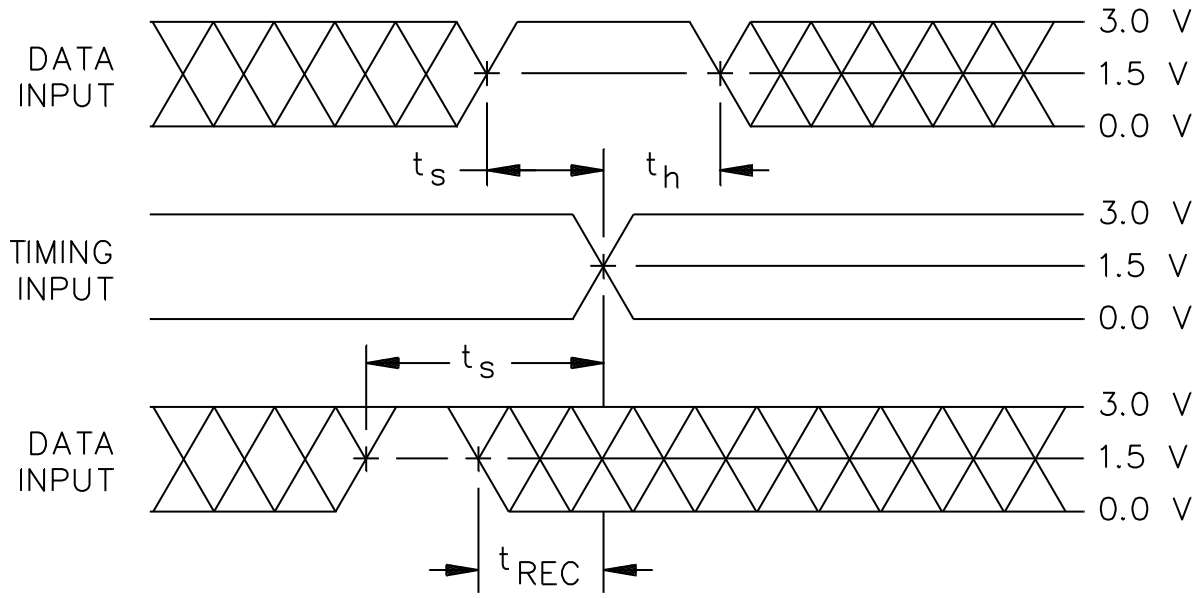
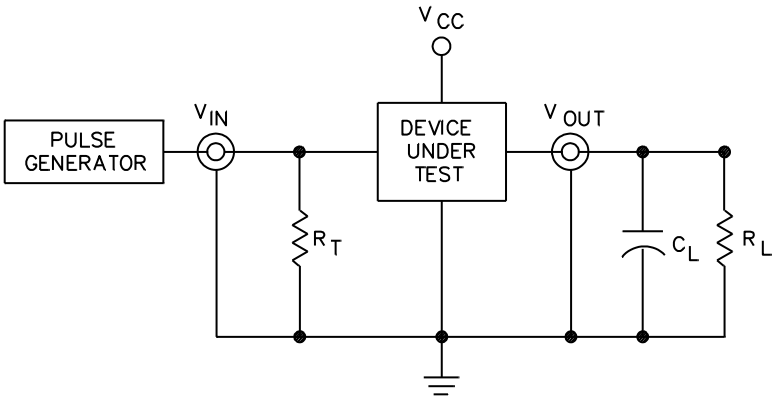


FIGURE 5. Switching waveforms and test circuit.







NOTES:

1. R_L = 500Ω or equivalent.
2. C_L = 50 pF or equivalent (includes test jig and probe capacitance).
3. R_T = 50Ω or equivalent, terminal resistance which should be equal to Z_{OUT} of the pulse generator.

.

FIGURE 5. Switching waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall verify the truth table as specified on figure 2.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0547.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 12-12-04

Approved sources of supply for SMD 5962-88640 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-88640012A	3/	54FCT161LMQB
5962-8864001EA	3/	54FCT161DMQB
5962-8864001FA	3/	54FCT161FMQB
5962-88640022A	0C7V7	QP54FCT161LMQB
5962-8864002EA	0C7V7	QP54FCT161DMQB
5962-8864002FA	0C7V7	QP54FCT161FMQB
5962-88640032A	0C7V7	QP54FCT161ALMQB
5962-8864003EA	0C7V7	QP54FCT161ADMQB
5962-8864003FA	0C7V7	QP54FCT161AFMQB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	e2v aerospace and defense, inc dba QP Semiconductor, Inc. 765 Sycamore Drive Milpitas, CA 95035

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.