# NCV8405A, NCV8405B

# Self-Protected Low Side Driver with Temperature and Current Limit

NCV8405A/B is a three terminal protected Low−Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain−to−Gate clamping for overvoltage protection. This device is suitable for harsh automotive environments.

### Features

- Short−Circuit Protection
- Thermal Shutdown with Automatic Restart
- Overvoltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

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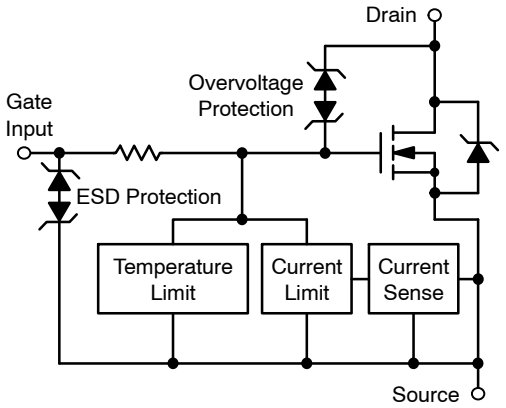
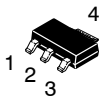
| $V_{(BR)DSS}$ (Clamped) | $R_{DS(ON)}$ TYP | $I_D$ MAX |
|---|---|---|
| 42 V | 90 mΩ @ 10 V | 6.0 A* |

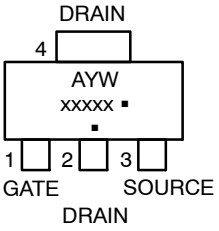
*Max current limit value is dependent on input condition.

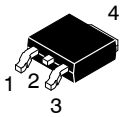



**MARKING DIAGRAM**

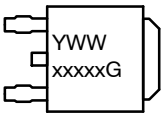



**SOT−223**
**CASE 318E**
**STYLE 3**




**DPAK**
**CASE 369C**




A = Assembly Location
Y = Year
W, WW = Work Week
xxxxx = 8405A or 8405B
G or ▪ = Pb−Free Package
(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain−to−Source Voltage Internally Clamped | $V_{DSS}$ | 42 | V |
| Drain−to−Gate Voltage Internally Clamped ($R_G$ = 1.0 MΩ) | $V_{DGR}$ | 42 | V |
| Gate−to−Source Voltage | $V_{GS}$ | ±14 | V |
| Continuous Drain Current | $I_D$ | Internally Limited | |
| Power Dissipation − SOT−223 Version | $P_D$ | | W |
| @ $T_A$ = 25°C (Note 1) | | 1.0 | |
| @ $T_A$ = 25°C (Note 2) | | 1.7 | |
| @ $T_S$ = 25°C | | 11.4 | |
| Power Dissipation − DPAK Version | | | |
| @ $T_A$ = 25°C (Note 1) | | 2.0 | |
| @ $T_A$ = 25°C (Note 2) | | 2.5 | |
| @ $T_S$ = 25°C | | 40 | |
| Thermal Resistance − SOT−223 Version | | | °C/W |
| Junction−to−Ambient Steady State (Note 1) | $R_{\theta JA}$ | 130 | |
| Junction−to−Ambient Steady State (Note 2) | $R_{\theta JA}$ | 72 | |
| Junction−to−Soldering Point Steady State | $R_{\theta JS}$ | 11 | |
| Thermal Resistance − DPAK Version | | | |
| Junction−to−Ambient Steady State (Note 1) | $R_{\theta JA}$ | 60 | |
| Junction−to−Ambient Steady State (Note 2) | $R_{\theta JA}$ | 50 | |
| Junction−to−Soldering Point Steady State | $R_{\theta JS}$ | 3.0 | |
| Single Pulse Drain−to−Source Avalanche Energy ($V_{DD}$ = 40 V, $V_G$ = 5.0 V, $I_{PK}$ = 2.8 A, L = 80 mH, $R_{G(ext)}$ = 25 Ω, TJ = 25°C) | $E_{AS}$ | 275 | mJ |
| Load Dump Voltage $V_{LD} = V_A + V_S$ ($V_{GS}$ = 0 and 10 V, $R_I$ = 2.0 Ω, $R_L$ = 6.0 Ω, $t_d$ = 400 ms) | $V_{LD}$ | 53 | V |
| Operating Junction Temperature | $T_J$ | −40 to 150 | °C |
| Storage Temperature | $T_{stg}$ | −55 to 150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted onto min pad FR4 PCB, (2 oz. Cu, 0.06″ thick).
2. Surface−mounted onto 2″ sq. FR4 board (1″ sq., 1 oz. Cu, 0.06″ thick).

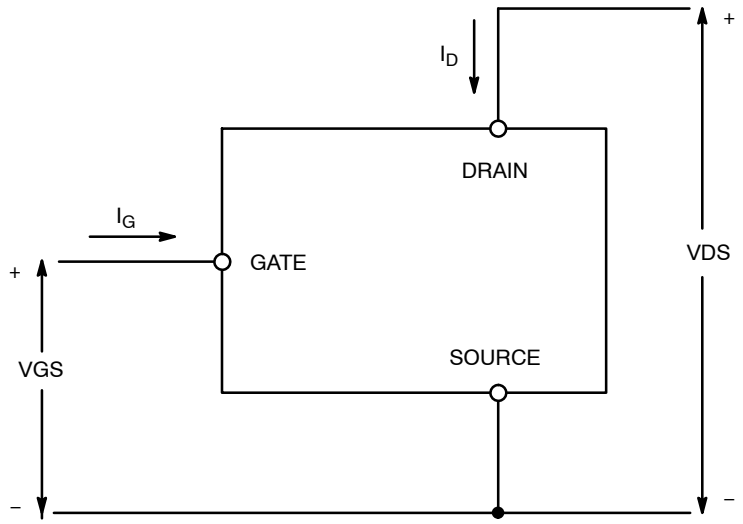



**Figure 1. Voltage and Current Convention**

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | Test Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain−to−Source Breakdown Voltage (Note 3) | $V_{GS}$ = 0 V, $I_D$ = 10 mA, $T_J$ = 25°C | $V_{(BR)DSS}$ | 42 | 46 | 51 | V |
| | $V_{GS}$ = 0 V, $I_D$ = 10 mA, $T_J$ = 150°C (Note 5) | | 42 | 45 | 51 | |
| Zero Gate Voltage Drain Current | $V_{GS}$ = 0 V, $V_{DS}$ = 32 V, $T_J$ = 25°C | $I_{DSS}$ | | 0.5 | 2.0 | μA |
| | $V_{GS}$ = 0 V, $V_{DS}$ = 32 V, $T_J$ = 150°C (Note 5) | | | 2.0 | 10 | |
| Gate Input Current | $V_{DS}$ = 0 V, $V_{GS}$ = 5.0 V | $I_{GSSF}$ | | 50 | 100 | μA |
| **ON CHARACTERISTICS** (Note 3) | | | | | | |
| Gate Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 150 μA | $V_{GS(th)}$ | 1.0 | 1.6 | 2.0 | V |
| Gate Threshold Temperature Coefficient | | $V_{GS(th)}/T_J$ | | 4.0 | | −mV/°C |
| Static Drain−to−Source On−Resistance | $V_{GS}$ = 10 V, $I_D$ = 1.4 A, $T_J$ = 25°C | $R_{DS(on)}$ | | 90 | 100 | mΩ |
| | $V_{GS}$ = 10 V, $I_D$ = 1.4 A, $T_J$ = 150°C (Note 5) | | | 165 | 190 | |
| | $V_{GS}$ = 5.0 V, $I_D$ = 1.4 A, $T_J$ = 25°C | | | 105 | 120 | |
| | $V_{GS}$ = 5.0 V, $I_D$ = 1.4 A, $T_J$ = 150°C (Note 5) | | | 185 | 210 | |
| | $V_{GS}$ = 5.0 V, $I_D$ = 0.5 A, $T_J$ = 25°C | | | 105 | 120 | |
| | $V_{GS}$ = 5.0 V, $I_D$ = 0.5 A, $T_J$ = 150°C (Note 5) | | | 185 | 210 | |
| Source−Drain Forward On Voltage | $V_{GS}$ = 0 V, $I_S$ = 7.0 A | $V_{SD}$ | | 1.05 | | V |
| **SWITCHING CHARACTERISTICS** (Note 5) | | | | | | |
| Turn−ON Time (10% $V_{IN}$ to 90% $I_D$) | $V_{GS}$ = 10 V, $V_{DD}$ = 12 V $I_D$ = 2.5 A, $R_L$ = 4.7 Ω | $t_{ON}$ | | 20 | | μs |
| Turn−OFF Time (90% $V_{IN}$ to 10% $I_D$) | | $t_{OFF}$ | | 110 | | |
| Slew−Rate ON (70% $V_{DS}$ to 50% $V_{DS}$) | $V_{GS}$ = 10 V, $V_{DD}$ = 12 V, $R_L$ = 4.7 Ω | $-dV_{DS}/dt_{ON}$ | | 1.0 | | V/μs |
| Slew−Rate OFF (50% $V_{DS}$ to 70% $V_{DS}$) | | $dV_{DS}/dt_{OFF}$ | | 0.4 | | |
| **SELF PROTECTION CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 4) | | | | | | |
| Current Limit | $V_{DS}$ = 10 V, $V_{GS}$ = 5.0 V, $T_J$ = 25°C | $I_{LIM}$ | 6.0 | 9.0 | 11 | A |
| | $V_{DS}$ = 10 V, $V_{GS}$ = 5.0 V, $T_J$ = 150°C (Note 5) | | 3.0 | 5.0 | 8.0 | |
| | $V_{DS}$ = 10 V, $V_{GS}$ = 10 V, $T_J$ = 25°C | | 7.0 | 10.5 | 13 | |
| | $V_{DS}$ = 10 V, $V_{GS}$ = 10 V, $T_J$ = 150°C (Note 5) | | 4.0 | 7.5 | 10 | |
| Temperature Limit (Turn−off) | $V_{GS}$ = 5.0 V (Note 5) | $T_{LIM(off)}$ | 150 | 180 | 200 | °C |
| Thermal Hysteresis | $V_{GS}$ = 5.0 V | $\Delta T_{LIM(on)}$ | | 15 | | |
| Temperature Limit (Turn−off) | $V_{GS}$ = 10 V (Note 5) | $T_{LIM(off)}$ | 150 | 165 | 185 | |
| Thermal Hysteresis | $V_{GS}$ = 10 V | $\Delta T_{LIM(on)}$ | | 15 | | |
| **GATE INPUT CHARACTERISTICS** (Note 5) | | | | | | |
| Device ON Gate Input Current | $V_{GS}$ = 5 V $I_D$ = 1.0 A | $I_{GON}$ | | 50 | | μA |
| | $V_{GS}$ = 10 V $I_D$ = 1.0 A | | | 400 | | |
| Current Limit Gate Input Current | $V_{GS}$ = 5 V, $V_{DS}$ = 10 V | $I_{GCL}$ | | 0.05 | | mA |
| | $V_{GS}$ = 10 V, $V_{DS}$ = 10 V | | | 0.4 | | |
| Thermal Limit Fault Gate Input Current | $V_{GS}$ = 5 V, $V_{DS}$ = 10 V | $I_{GTL}$ | | 0.22 | | mA |
| | $V_{GS}$ = 10 V, $V_{DS}$ = 10 V | | | 1.0 | | |
| **ESD ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 5) | | | | | | |
| Electro−Static Discharge Capability | Human Body Model (HBM) | ESD | 4000 | | | V |
| | Machine Model (MM) | | 400 | | | |

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Fault conditions are viewed as beyond the normal operating range of the part.
5. Not subject to production testing.

## TYPICAL PERFORMANCE CURVES

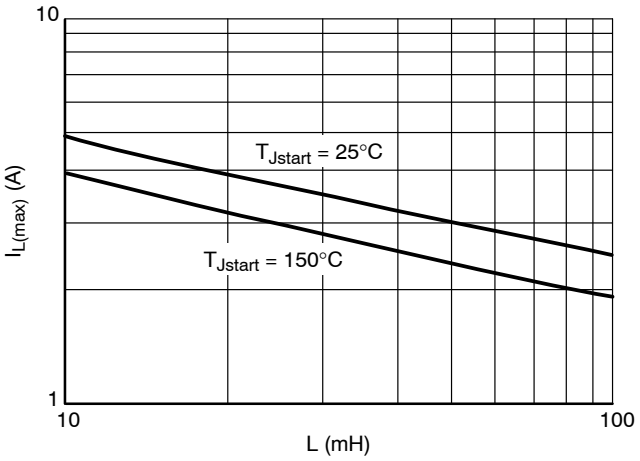



**Figure 2. Single Pulse Maximum Switch−off Current vs. Load Inductance**

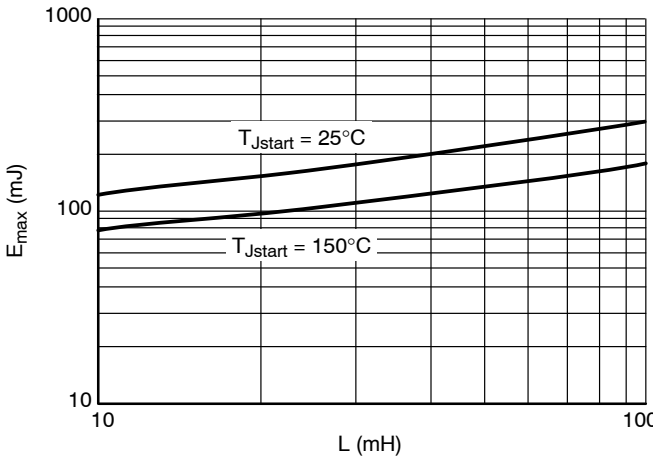



**Figure 3. Single Pulse Maximum Switching Energy vs. Load Inductance**

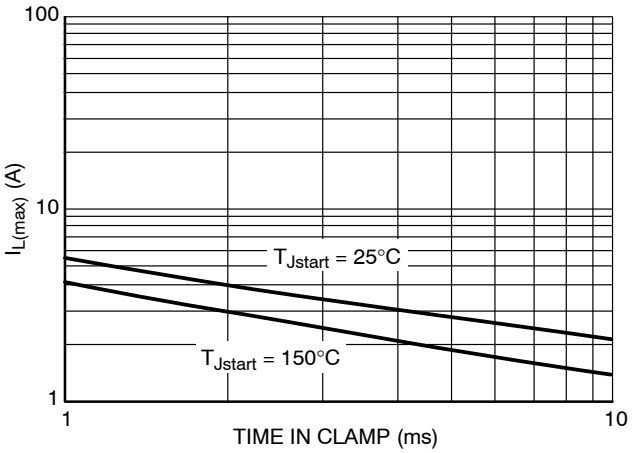



**Figure 4. Single Pulse Maximum Inductive Switch−off Current vs. Time in Clamp**

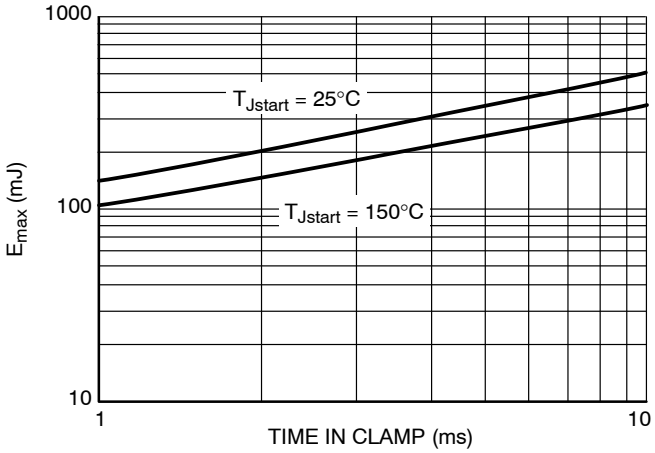



**Figure 5. Single Pulse Maximum Inductive Switching Energy vs. Time in Clamp**

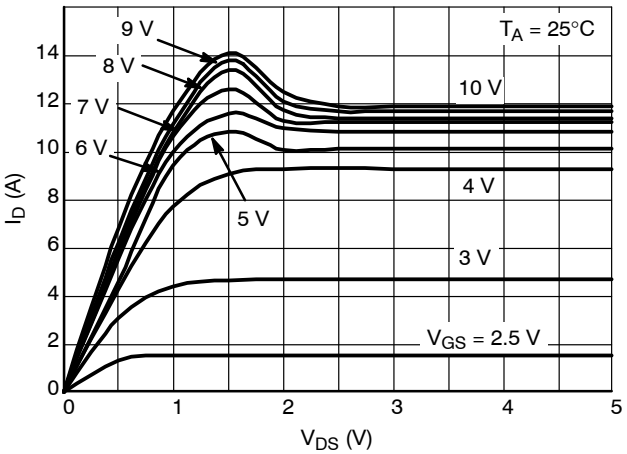



**Figure 6. Output Characteristics**

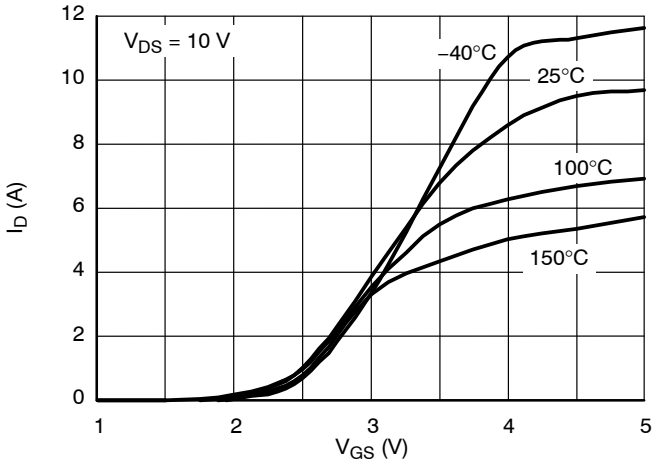



**Figure 7. Transfer Characteristics**

## TYPICAL PERFORMANCE CURVES

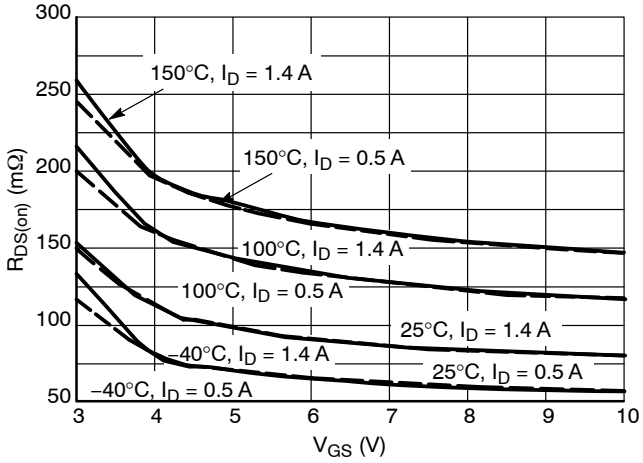



**Figure 8. $R_{DS(on)}$ vs. Gate−Source Voltage**

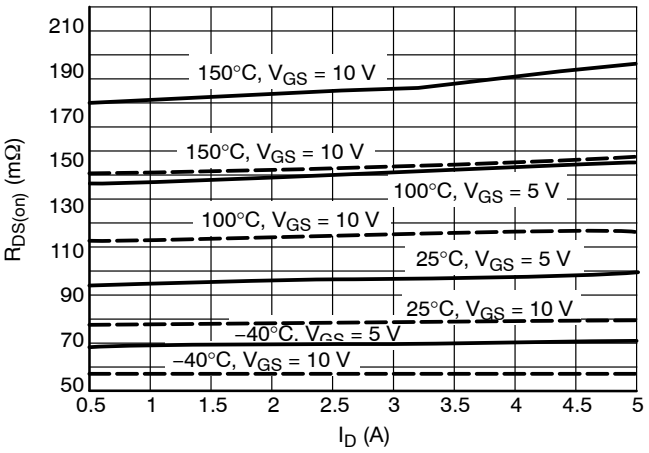



**Figure 9. $R_{DS(on)}$ vs. Drain Current**

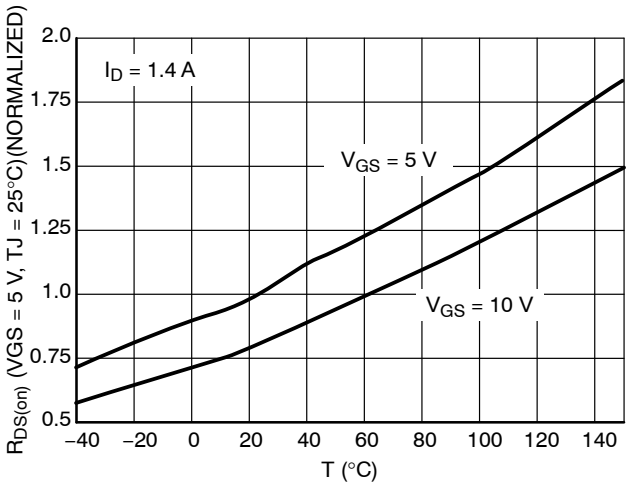



**Figure 10. Normalized $R_{DS(on)}$ vs. Temperature**

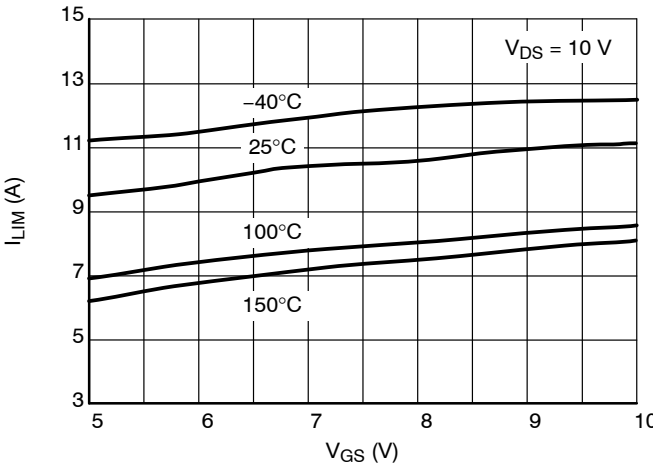



**Figure 11. Current Limit vs. Gate−Source Voltage**

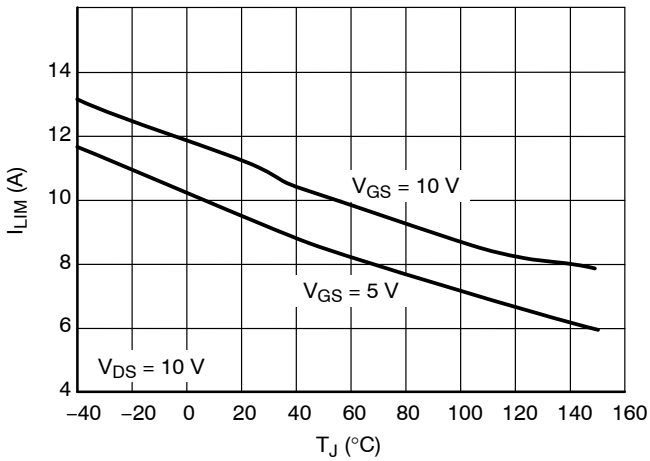



**Figure 12. Current Limit vs. Junction Temperature**

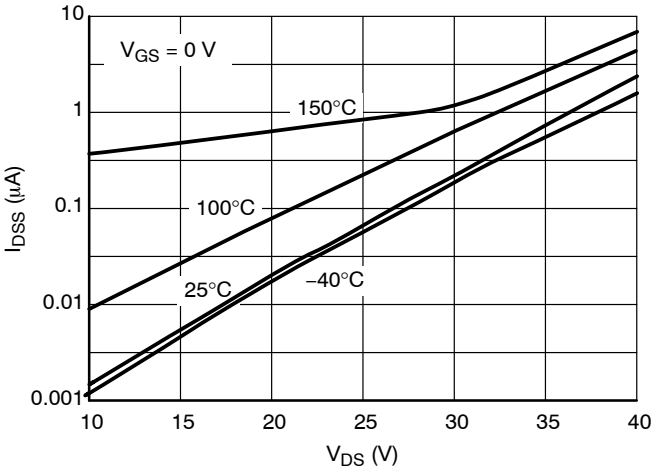



**Figure 13. Drain−to−Source Leakage Current**

## TYPICAL PERFORMANCE CURVES

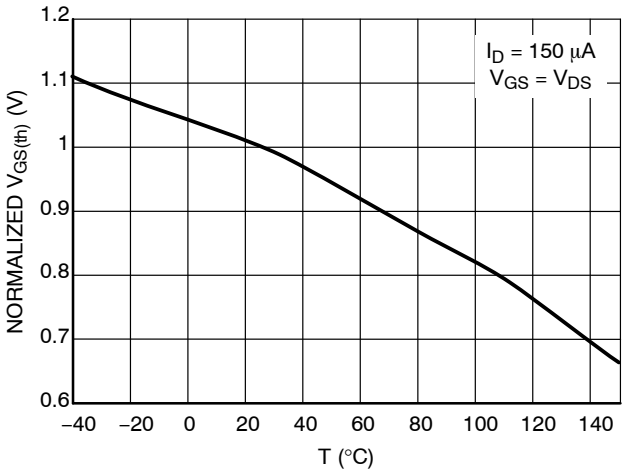



**Figure 14. Normalized Threshold Voltage vs. Temperature**

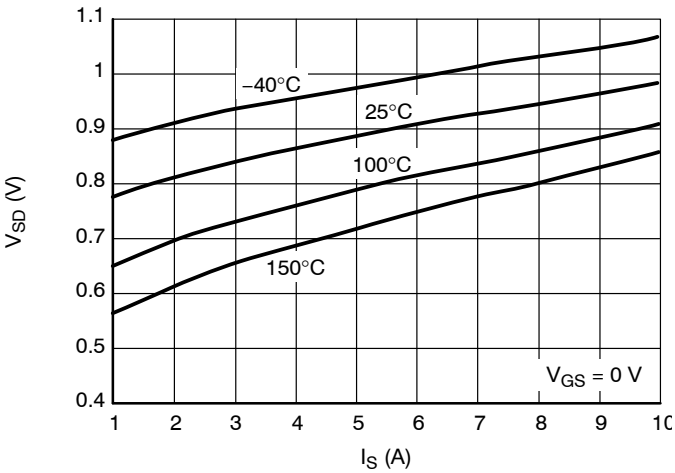



**Figure 15. Body−Diode Forward Characteristics**

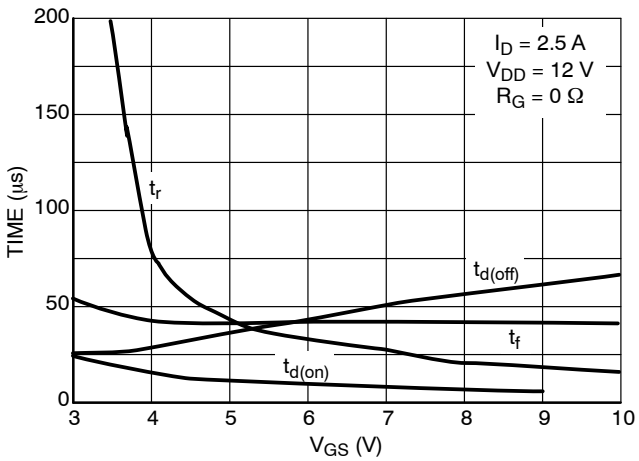



**Figure 16. Resistive Load Switching Time vs. Gate−Source Voltage**

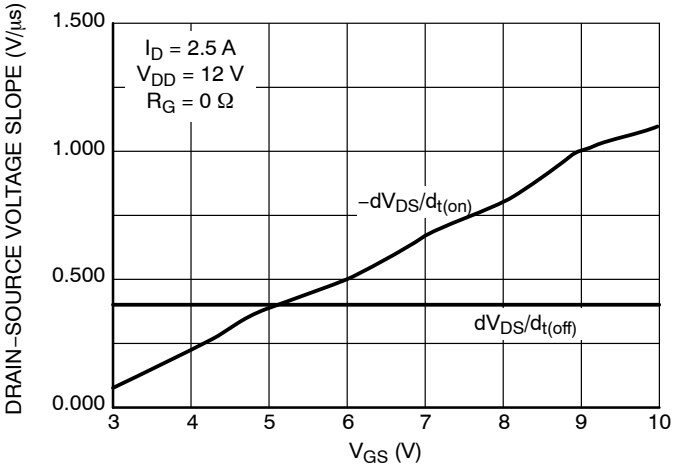



**Figure 17. Resistive Load Switching Drain−Source Voltage Slope vs. Gate−Source Voltage**

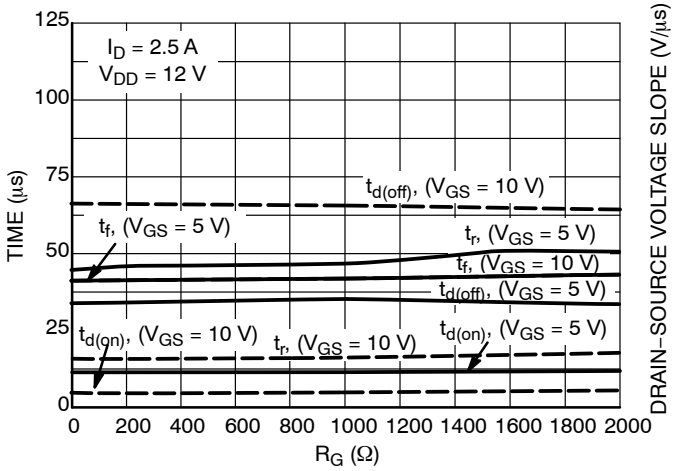



**Figure 18. Resistive Load Switching Time vs. Gate Resistance**

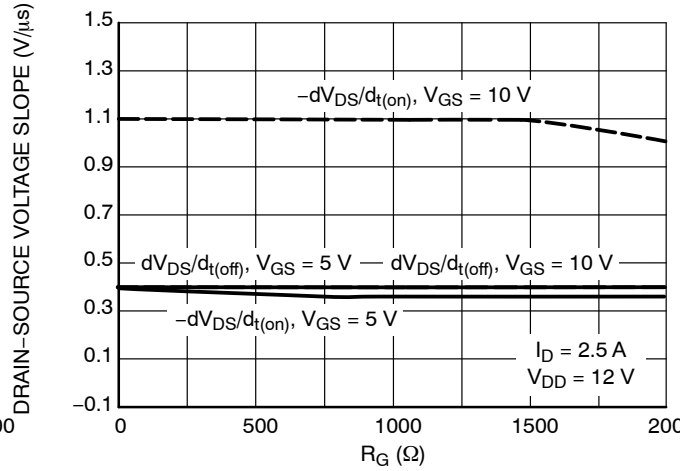



**Figure 19. Drain−Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance**

## TYPICAL PERFORMANCE CURVES

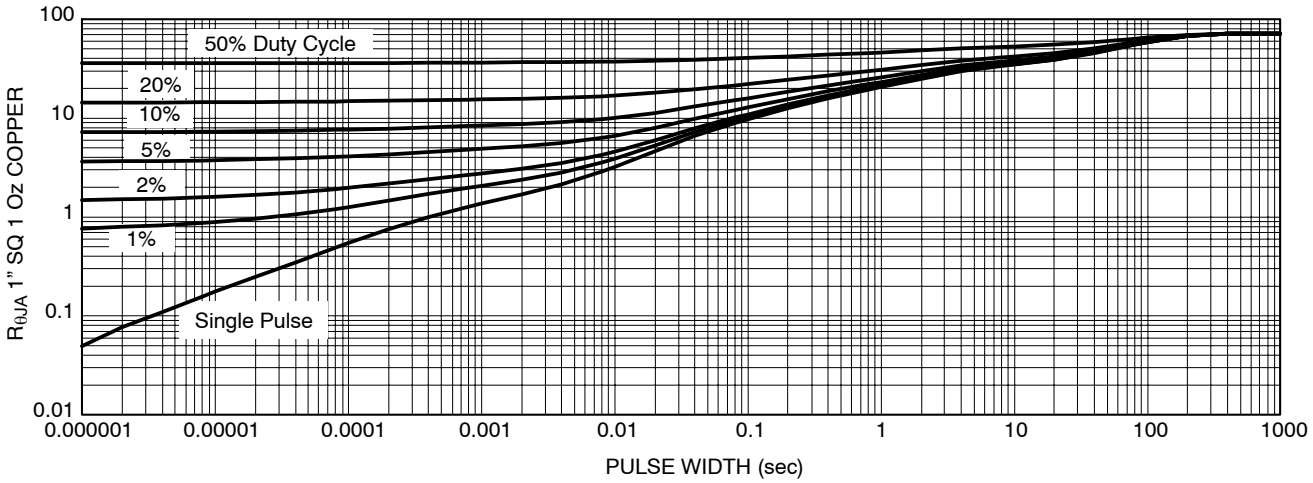



**Figure 20. Transient Thermal Resistance**

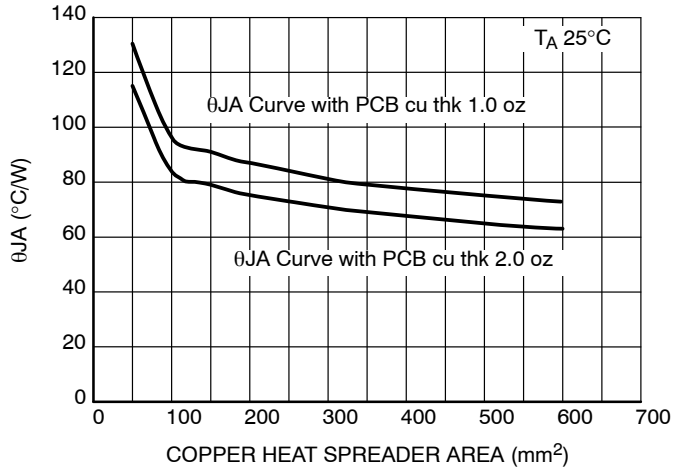



**Figure 21. θJA vs. Copper**

## TEST CIRCUITS AND WAVEFORMS

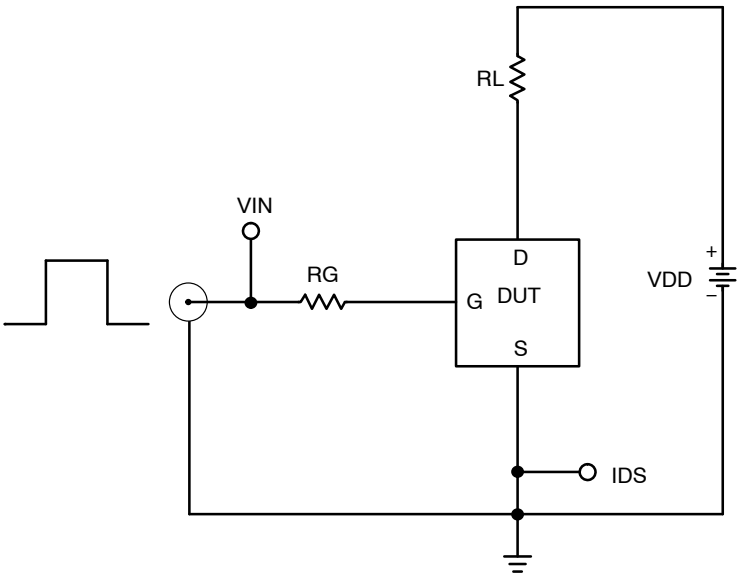



**Figure 22. Resistive Load Switching Test Circuit**

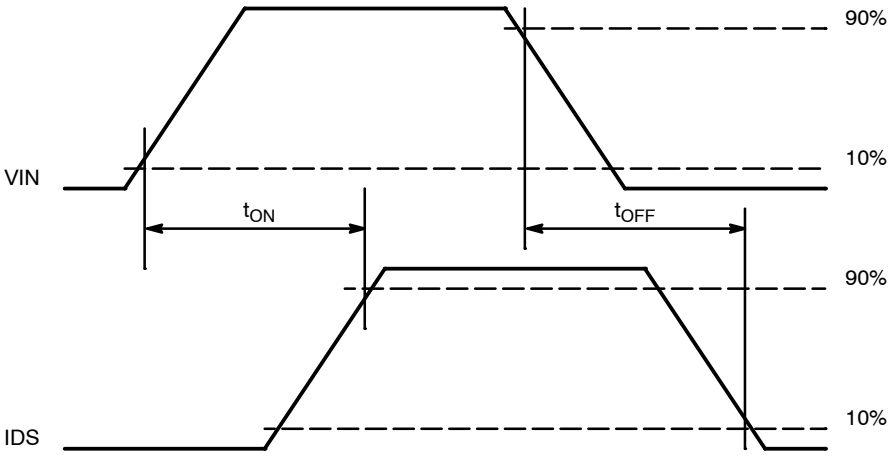



**Figure 23. Resistive Load Switching Waveforms**

## TEST CIRCUITS AND WAVEFORMS

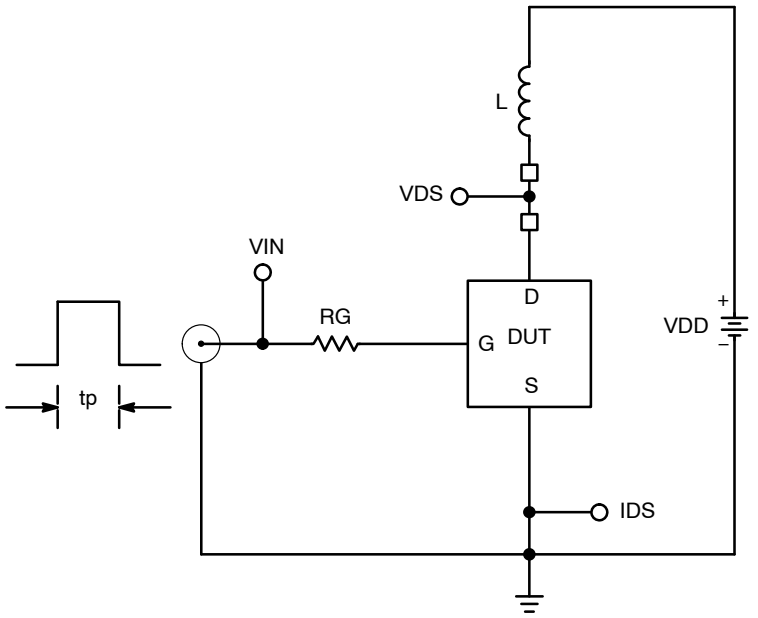



**Figure 24. Inductive Load Switching Test Circuit**

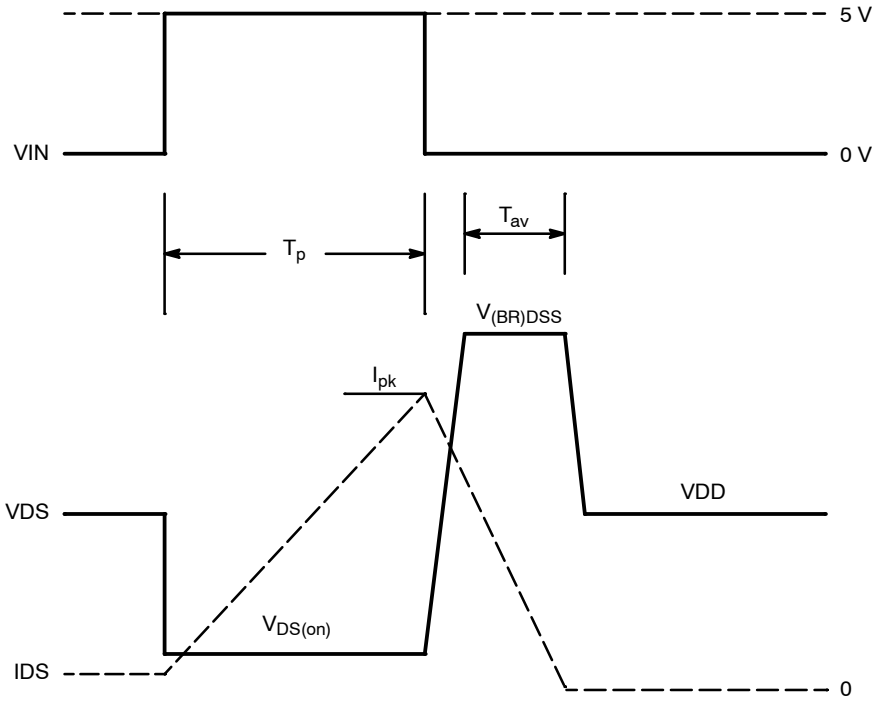



**Figure 25. Inductive Load Switching Waveforms**

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NCV8405ASTT1G | SOT−223 (Pb−Free) | 1000 / Tape & Reel |
| NCV8405ASTT3G | SOT−223 (Pb−Free) | 4000 / Tape & Reel |
| NCV8405ADTRKG | DPAK (Pb−Free) | 2500 / Tape & Reel |
| NCV8405BDTRKG | DPAK (Pb−Free) | 2500 / Tape & Reel |

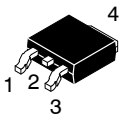
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

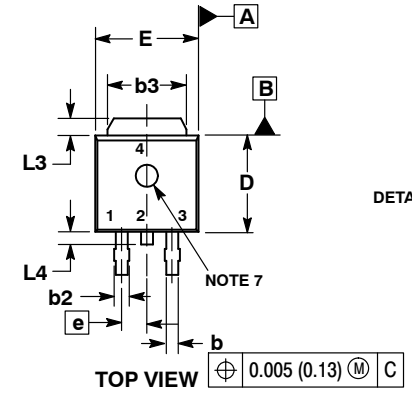
ON Semiconductor®

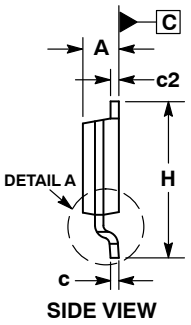
**DPAK (SINGLE GAUGE)**
CASE 369C
ISSUE F

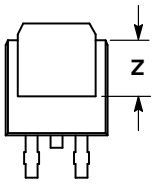
DATE 21 JUL 2015

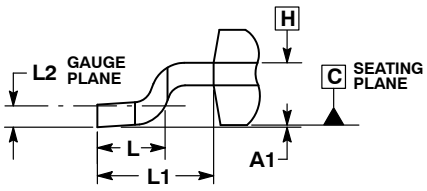


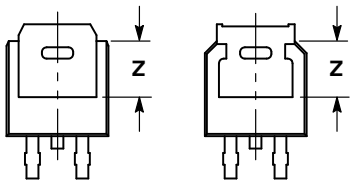

SCALE 1:1




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.028 | 0.045 | 0.72 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | | 2.29 BSC | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.114 REF | | 2.90 REF | |
| L2 | 0.020 BSC | | 0.51 BSC | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | --- | 0.040 | --- | 1.01 |
| Z | 0.155 | --- | 3.93 | --- |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

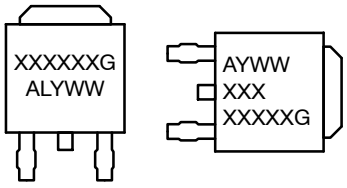
STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

## GENERIC MARKING DIAGRAM*

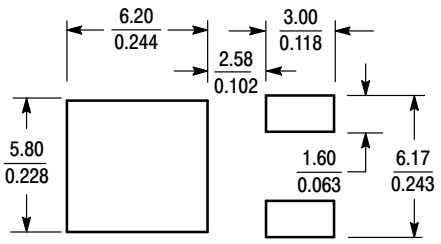



IC Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

## SOLDERING FOOTPRINT*




SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|---|---|---|
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