



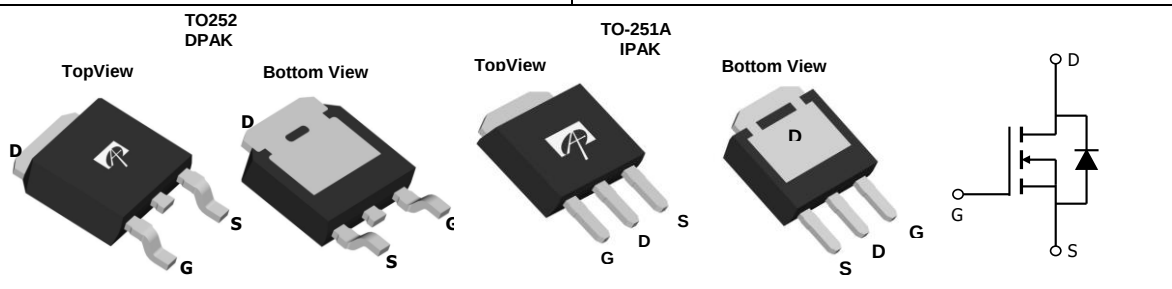
General Description

The AOD444/AOI444 combine advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. Those devices are suitable for use in PWM, load switching and general purpose applications.

Product Summary

V_{DS}	60V
I_D (at $V_{GS}=10V$)	12A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 60m Ω
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$)	< 85m Ω

100% UIS Tested
100% Rg Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	12	A
$T_C=25^\circ\text{C}$			
$T_C=100^\circ\text{C}$		9	
Pulsed Drain Current ^C	I_{DM}	30	
Continuous Drain Current	I_{DSM}	4	A
$T_A=25^\circ\text{C}$			
$T_A=70^\circ\text{C}$		3	
Avalanche Current ^C	I_{AS}, I_{AR}	19	A
Avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}, E_{AR}	18	mJ
Power Dissipation ^B	P_D	20	W
$T_C=25^\circ\text{C}$			
$T_C=100^\circ\text{C}$		10	
Power Dissipation ^A	P_{DSM}	2.1	W
$T_A=25^\circ\text{C}$			
$T_A=70^\circ\text{C}$		1.3	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	17.4	30	$^\circ\text{C/W}$
$t \leq 10\text{s}$				
Maximum Junction-to-Ambient ^{A D}	$R_{\theta JC}$	50	60	$^\circ\text{C/W}$
Steady-State				
Maximum Junction-to-Case	$R_{\theta JC}$	4	7.5	$^\circ\text{C/W}$
Steady-State				

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =48V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1	2.4	3	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	30			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =12A T _J =125°C		47 85	60 100	mΩ
		V _{GS} =4.5V, I _D =6A		67	85	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		14		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.74	1	V
I _S	Maximum Body-Diode Continuous Current				12	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =30V, f=1MHz	360	450	540	pF
C _{oss}	Output Capacitance		40	61	80	pF
C _{rss}	Reverse Transfer Capacitance		16	27	40	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.6	1.4	2.0	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =30V, I _D =12A		7.5	10	nC
Q _{g(4.5V)}	Total Gate Charge			3.8	5	nC
Q _{gs}	Gate Source Charge			1.2		nC
Q _{gd}	Gate Drain Charge			1.9		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =30V, R _L =2.5Ω, R _{GEN} =3Ω		4.2		ns
t _r	Turn-On Rise Time			3.4		ns
t _{D(off)}	Turn-Off DelayTime			16		ns
t _f	Turn-Off Fall Time			2		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =12A, dI/dt=100A/μs		27	35	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =12A, dI/dt=100A/μs		30		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO MAKE CHANGES TO PRODUCT SPECIFICATIONS WITHOUT NOTICE. IT IS THE RESPONSIBILITY OF THE CUSTOMER TO EVALUATE SUITABILITY OF THE PRODUCT FOR THEIR INTENDED APPLICATION. CUSTOMER SHALL COMPLY WITH APPLICABLE LEGAL REQUIREMENTS, INCLUDING ALL APPLICABLE EXPORT CONTROL RULES, REGULATIONS AND LIMITATIONS.

AOS' products are provided subject to AOS' terms and conditions of sale which are set forth at:

http://www.aosmd.com/terms_and_conditions_of_sale

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

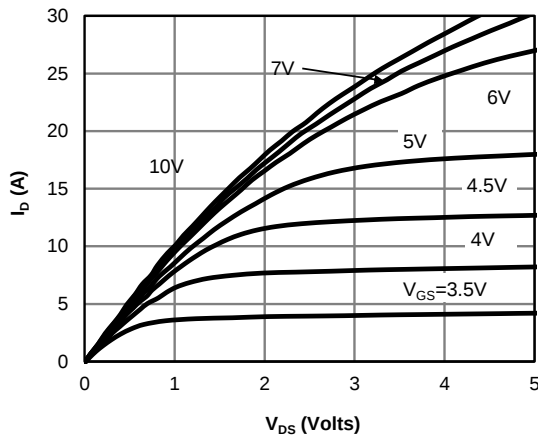


Fig 1: On-Region Characteristics (Note E)

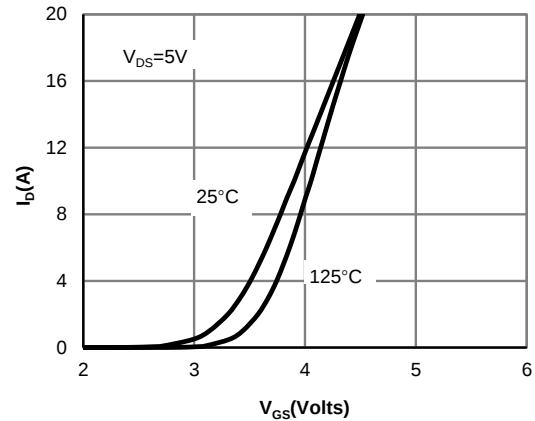


Figure 2: Transfer Characteristics (Note E)

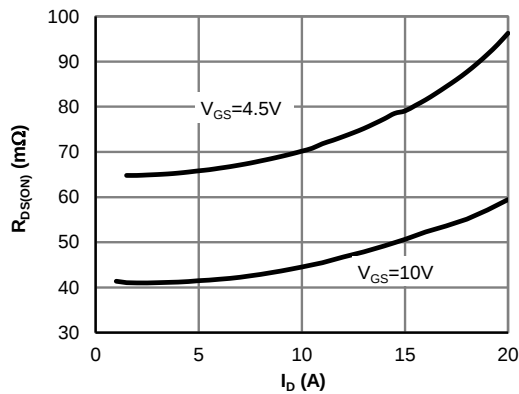


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

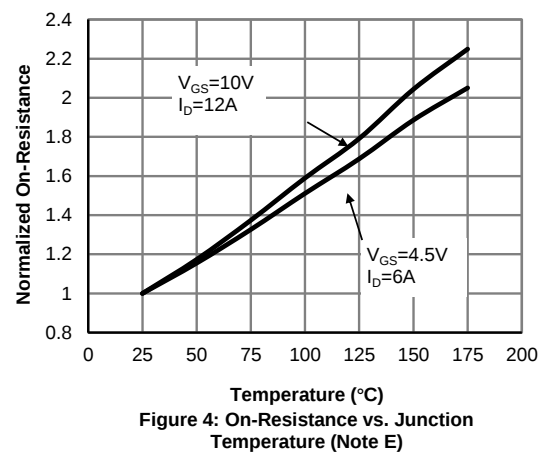


Figure 4: On-Resistance vs. Junction Temperature (Note E)

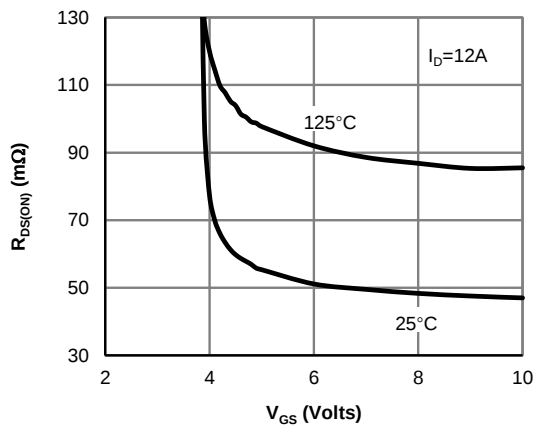


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

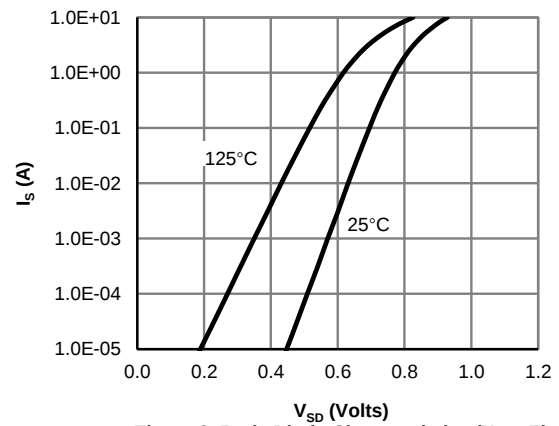
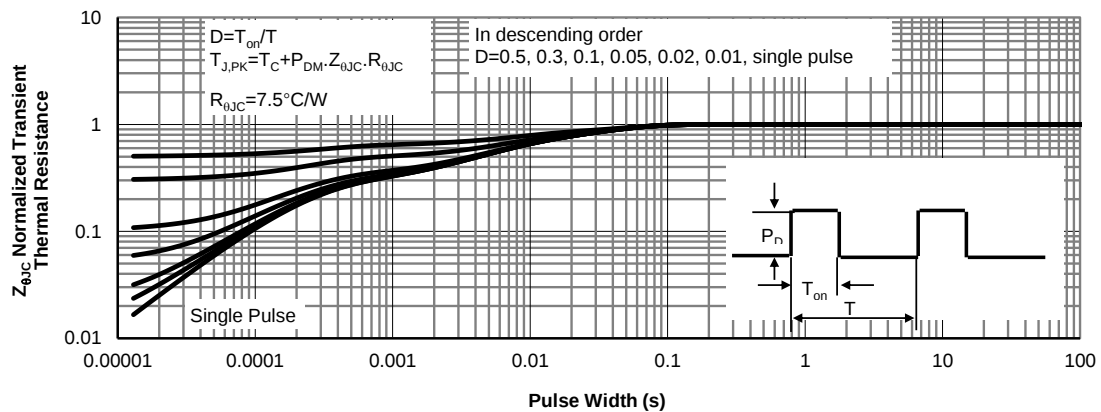
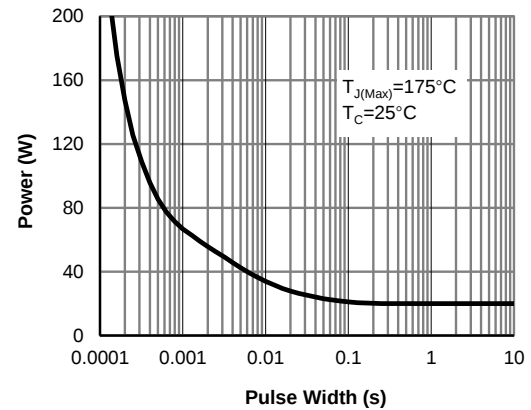
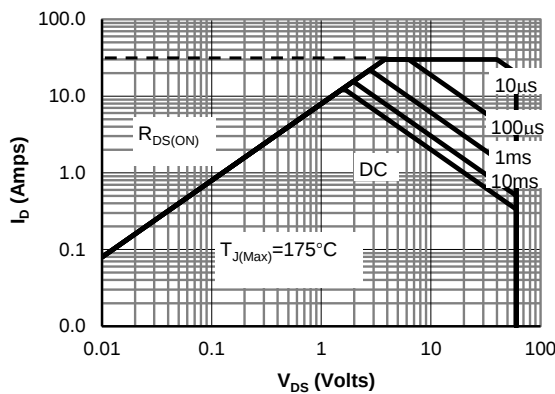
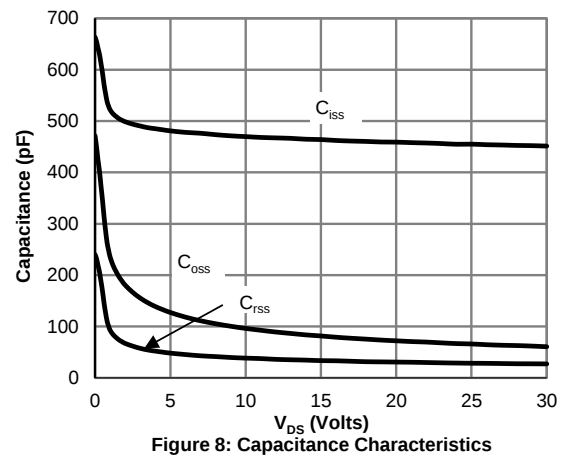
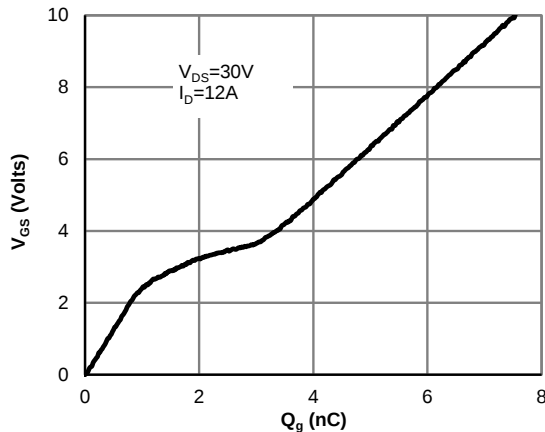


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

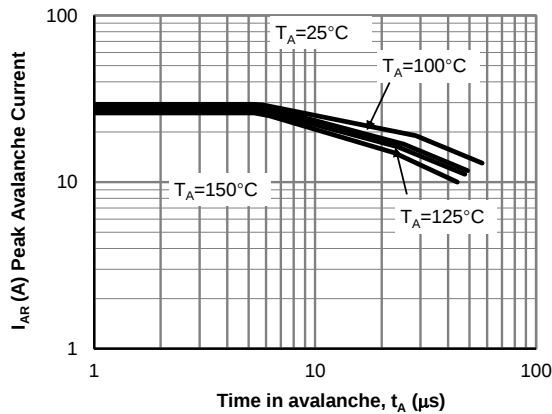


Figure 12: Single Pulse Avalanche capability (Note C)

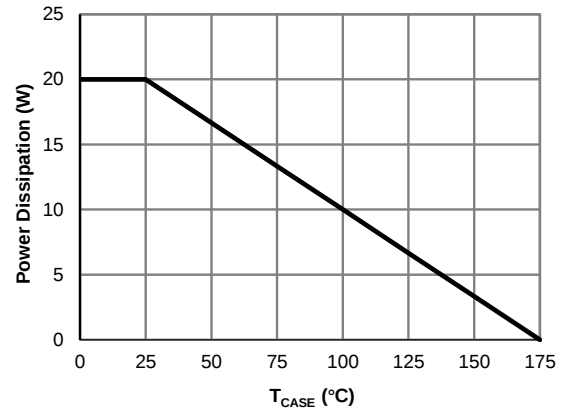


Figure 13: Power De-rating (Note F)

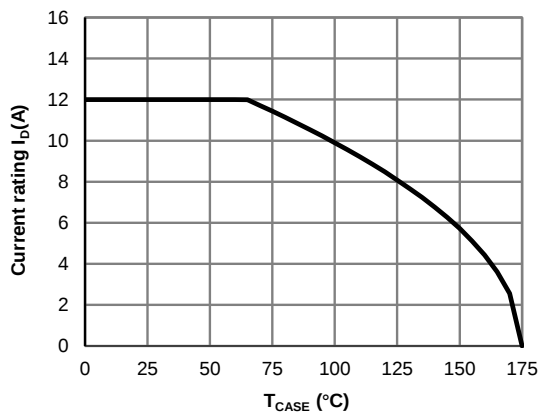


Figure 14: Current De-rating (Note F)

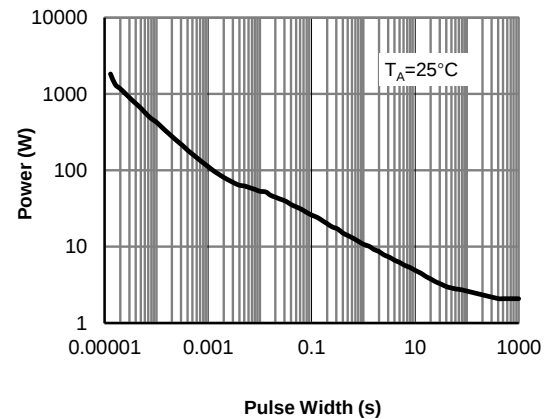


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

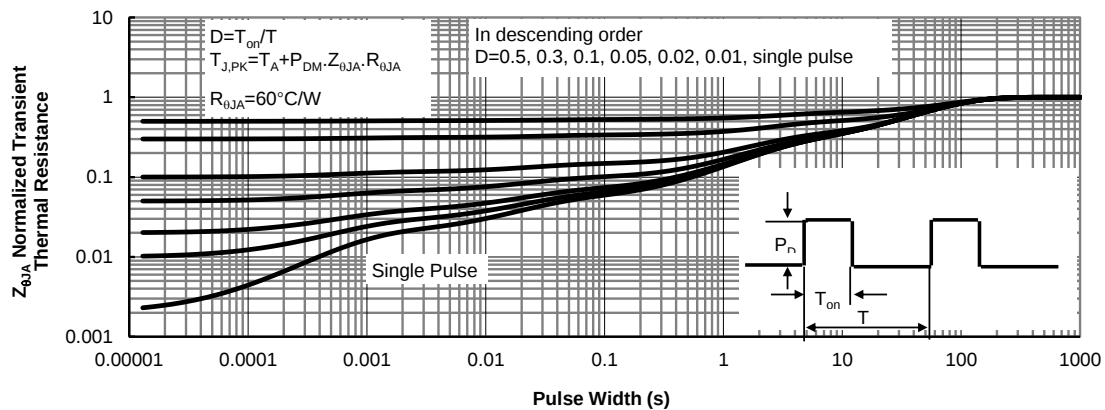
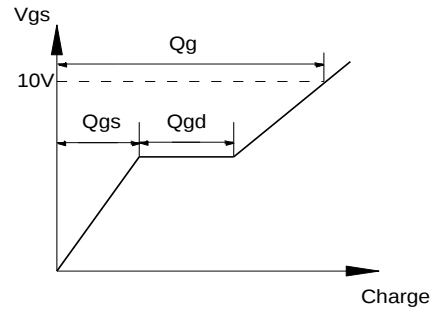
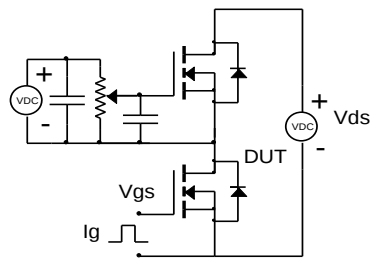
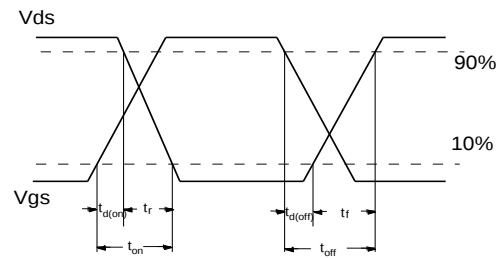
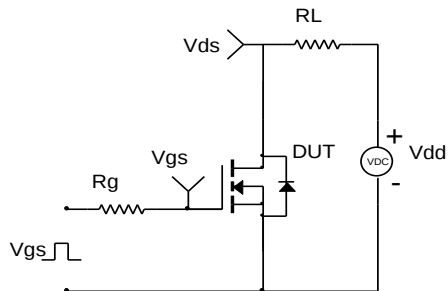


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

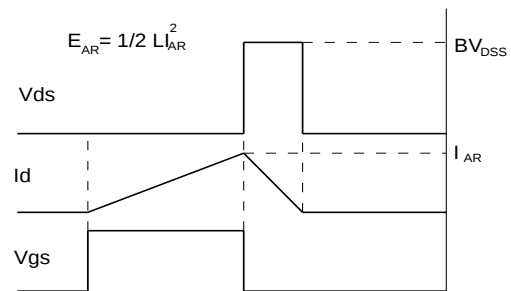
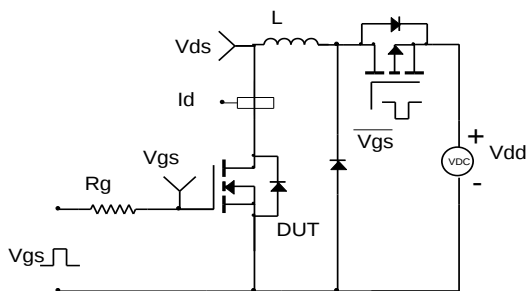
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

