MAX25169

Automotive, I²C-Controlled, 6-Channel, 150mA Backlight Driver and 4-Output TFT-LCD Bias with ASIL B Features

General Description

The MAX25169 is a highly integrated TFT power supply and LED backlight driver IC for automotive TFT-LCD applications. This IC integrates one boost converter, one inverting buck-boost converter, two gate-driver supplies, and a boost/SEPIC controller that can power 1 to 6 strings of LEDs in the display backlight.

The source-driver power supplies consist of a boost converter which can provide up to +18V in unipolar mode and an inverting buck-boost converter that can generate a voltage down to -10.5V. The AVDD output can deliver up to 300mA at 13.5V, while NAVDD can provide up to 200mA. The positive source-driver supply-regulation voltage (V_{AVDD}) is set using internal NV memory or through I²C. The negative source-driver supply voltage (V_{NAVDD}) is always tightly regulated to $-V_{AVDD}$. The source-driver supplies operate from an input voltage between 2.65V and 5.5V.

The gate-driver power supplies consist of regulated charge pumps that generate up to +31.5V and down to -18V and can deliver up to 15mA each.

The IC features a 6-string LED driver with input switch control (NGATE) that can power up to 6 strings of LEDs with 150mA (max) of current per string.

Logic-controlled and I²C-controlled pulse-width modulation (PWM) dimming are included, with minimum pulse widths as low as 300ns and the option of phase shifting the LED strings with respect to one another. When phase shifting is enabled, each string is turned on at a different time, reducing the input and output ripple, as well as audible noise. With phase shifting disabled, the current sinks turn on simultaneously and parallel connection of current sinks is possible.

The startup and shutdown sequences for all power domains are controlled using one of the eight preset modes, which are selectable using internal nonvolatile memory or through the I²C interface.

The MAX25169 is available in a 7mm x 7mm, 48-pin TQFN package with an exposed pad, and operates over the -40°C to +125°C ambient temperature range.

Applications

- Automotive Dashboards
- Automotive Central Information Displays
- Automotive Head-Up Displays
- Automotive Navigation Systems

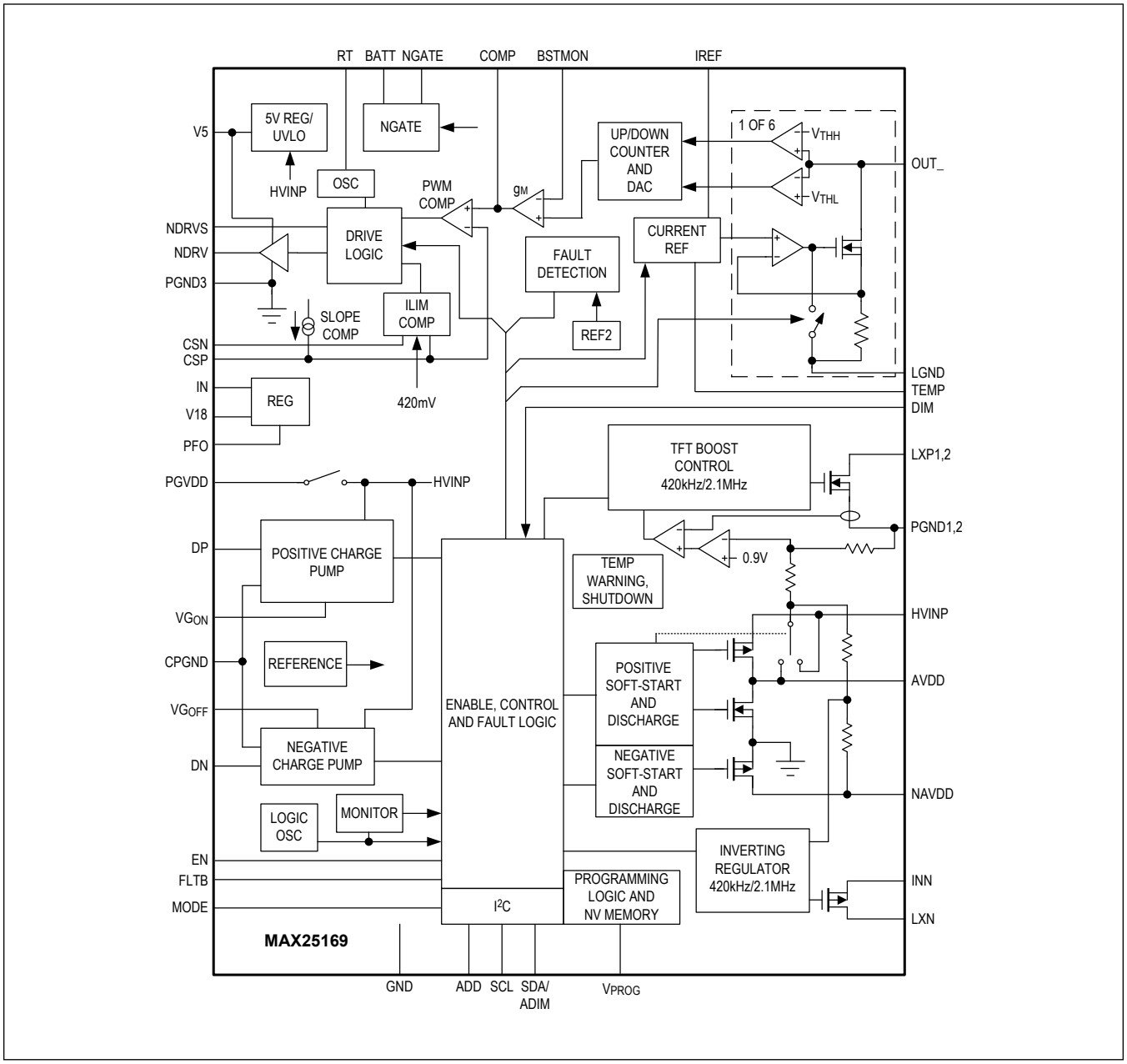
Benefits and Features

- 4-Output TFT-LCD Bias Power
  - 2.65V to 5.5V Input for the TFT-LCD Section
  - Integrated 420kHz or 2.1MHz Boost and Buck-Boost Converters
  - Positive and Negative 15mA Gate Voltage Regulators with Adjustable Output Voltage (Tripler/Inverting Doubler)
  - Flexible Sequencing
  - Undervoltage Detection on All Outputs
  - Low-Quiescent-Current Standby Mode
- 6-Channel, 36V LED Backlight Driver
  - NGATE Control for External NMOSFET Series Switch
  - Programmable nMOSFET Current Limit
  - Up to 150mA Current per Channel
  - 4.5V to 36V Input Voltage Range, 3V Operation after Startup
  - Integrated Boost/SEPIC Controller (400kHz to 2.2MHz with Synchronization)
  - Dimming Ratio 16,667:1 at 200Hz
  - Adaptive Voltage Optimization to Reduce Power Dissipation in LED Current Sinks
  - Open-String, Shorted-LED, and Short-to-GND Diagnostics
- Low EMI
  - Phase-Shift Dimming of LED Strings
  - Spread Spectrum on LED Driver and TFT Outputs
  - Selectable Switching Frequency
- I²C Interface for Control and Diagnostics
  - Fault Indication through the FLTB Pin and I²C
  - Nonvolatile Configuration Memory
- Overload and Thermal Protection
- ASIL B Compliant
- -40°C to +125°C Ambient Temperature Operation
- 7mm x 7mm, 48-Pin TQFN Package with Exposed Pad
- AEC-Q100 Grade 1

Ordering Information appears at end of data sheet.

19-101585; Rev 1; 6/23

Simplified Block Diagram



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Absolute Maximum Ratings

BATT, OUT1-6, BSTMON to GND ..... -0.3V to +42V
NGATE to BATT ..... +6V
NGATE to GND ..... -0.3V to +42V
IN, INN, FLTB, PFO, DIM, EN, SDA, SCL to GND... -0.3V to +6V
NDRV, NDRVS to GND ..... -0.3V to V5 + 0.3V
TEMP, MODE, CSP, COMP, IREF, RT, ADD to GND ..... -0.3V to V18 + 0.3V
HVINP to GND ..... -0.3V to +22V
LXP to GND ..... -0.3V to +30V
LXP1/2, PGND1/2 RMS Total Current Rating 2.4A
V5 to GND ..... -0.3V to MIN (6, HVINP + 0.3)V
V18 to GND ..... -0.3V to MIN (2.2, IN + 0.3)V
PGVDD, AVDD, DP, DN to GND ..... -0.3V to HVINP + 0.3V
LXN to INN ..... -22V to +0.3V
LXN, INN RMS Current Rating 1.6A
VG_{ON} to GND ..... -0.3V to +40V
V_{PROG} to GND ..... -0.3V to +12V
NAVDD to GND ..... V_{V18} - 16V to V_{V18} + 0.3V
VG_{OFF} to GND ..... V_{V18} - 22V to V_{V18} + 0.3V
GND to PGND1, PGND2, PGND3 ..... -0.3V to +0.3V
GND to LGND ..... -0.3V to +0.3V
GND to CPGND ..... -0.3V to +0.3V
GND to CSN ..... -0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFN-EP (derate 43mW/°C above +70°C), (multilayer board) 3433mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

48 TQFN

Package Code	T4877+9C
Outline Number	21-0144
Land Pattern Number	90-0464
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	23.3°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(V_{IN} = 3.3V, V_{BATT} = 12V, typical operating circuit, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
IN, INN Voltage Range	V_{IN_RNG}		2.65		5.5	V
IN UVLO Threshold, Rising	V_{IN_UVLOR}	IN voltage rising	2.4	2.5	2.57	V
IN UVLO Threshold, Falling	V_{IN_UVLOF}		2.3		2.5	V
PFO Threshold	V_{PFO}	IN falling, pfo_th = 0, PFO output goes low	2.4	2.5	2.6	V
Total Input Shutdown Current (IN + INN + HVINP + LXP)	I_{IN_SHDN}	EN = GND, T_A = +25°C		3.5	15	µA

Electrical Characteristics (continued)

(V_{IN} = 3.3V, V_{BATT} = 12V, typical operating circuit, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IN + INN Quiescent Current	I_{IN_Q}	V_{EN} = 3.3V, no switching			2	4	mA
V18 REGULATOR							
V18 Output Voltage	V_{V18_ACC}	No load on V18		1.72	1.8	1.88	V
V18 Current Limit	I_{LIM_V18}	V_{V18} = 1V		50			mA
V18 Undervoltage Lockout	V_{V18_UVLO}	V18 voltage rising		1.6	1.65	1.7	V
V18 Undervoltage Hysteresis	$V_{V18\_UVLO\_HYS}$				150		mV
V18OOR Diagnostic Levels					±8		%
TFT POWER SECTION / OSCILLATOR							
Operating Frequency	f_{BOOSTH}	f_{SW} bit = 0, dither disabled		1950	2100	2250	kHz
	f_{BOOSTL}	f_{SW} bit = 1, dither disabled		380	420	460	
Frequency Dither	f_{BOOSTD}				±6		%
TFT POWER SECTION / BOOST REGULATOR							
HVINP Output Voltage Range	V_{HVINP}	dis_navdd = 0		4.9		10.5	V
		dis_navdd = 1		11.7		18	
AVDD Adjustment Step Size	V_{STEP}				0.1		V
AVDD Output Regulation	V_{AVDD_ACC}	avdd[5:0] = 0x1A, dis_navdd = 0		6.66	6.8	6.94	V
LXP Maximum Duty Cycle	D_{LXP_MAX}	420kHz switching frequency		91.75	95		%
		2.1MHz switching frequency		91.75	95		
Low-Side Switch On-Resistance	$R_{ON\_LS\_LXP}$	I_{LXP} = 0.1A			0.1	0.2	Ω
LXP Leakage Current	I_{LEAK_LXP}	V_{EN} = 0V, V_{LXP} = 15V				6	µA
LXP Current Limit	I_{LIMPHB}	dis_navdd = 0	Duty cycle = 80%, Lxp_Lim_Low = 0	1.5	1.8	2.1	A
	I_{LIMPLB}		Duty cycle = 80%, Lxp_Lim_Low = 1		1		
	I_{LIMPHU}	dis_navdd = 1	Duty cycle = 80%, Lxp_Lim_Low = 0	2.3	2.7	3.2	
	I_{LIMPLU}		Duty cycle = 80%, Lxp_Lim_Low = 1		1.35		
Soft-Start Period	t_{BOOST_SS}	Current-limit ramp			5		ms
TFT POWER SECTION / INVERTING REGULATOR							
LXN Maximum Duty Cycle	D_{LXN_MAX}	f_{SW} = 420kHz or 2.1MHz		91.75	95		%
V_{AVDD} + V_{NAVDD} Regulation Voltage	$V_{NAVDD\_AVDD\_REG}$	V_{INN} = 2.65V to 5.5V, V_{AVDD} = 6.8V, 1mA < I_{NAVDD} < 200mA, I_{AVDD} = same load as NAVDD		-34	0	34	mV
LXN On-Resistance	R_{ON_LXN}	I_{LXN} = 0.1A			0.25	0.5	Ω

Electrical Characteristics (continued)

(V_{IN} = 3.3V, V_{BATT} = 12V, typical operating circuit, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LXN Leakage Current	I_{LXN_LEAK}	V_{LXN} = V_{NAVDD} = -6.8V, T_A = +25°C			20	µA
LXN Current Limit	I_{LIMNL}	Duty cycle = 80%, Lxp_Lim_low = 1	0.6	0.8		A
	I_{LIMNH}	Duty cycle = 80%, Lxp_Lim_low = 0	1.55	1.9	2.25	
Soft-Start Period	t_{INV_SS}	Current-limit ramp		5		ms
TFT POWER SECTION / CHARGE-PUMP REGULATORS						
PGVDD Operating Voltage Range	V_{PGVDD}		4.9		V_{HVINP}	V
HVINP-PGVDD Threshold for VG_{ON} Startup	$V_{HVINP-PGVDD}$	V_{HVINP} = 5V	360	520	680	mV
High-Side DP/DN Current Limit	I_{DR_HS}	V_{HVINP} = 6.8V, V_{DP} = V_{DN} = 3V	95			mA
Low-Side DP/DN Current Limit	I_{DR_LS}	V_{DP} = V_{DN} = 3V	95			mA
High-Side DP/DN On-Resistance	R_{DR_HS}	I_{DP} = I_{DN} = -20mA, V_{PGVDD} = V_{HVINP} = 6.8V		5	8	Ω
Low-Side DP/DN On-Resistance	R_{DR_LS}	I_{DP} = I_{DN} = 20mA		3	6	Ω
VG_{ON} Unipolar Voltage Range	VG_{ON_RNG}	dis_navdd = 1	12.6		31.5	V
VG_{ON} Bipolar Voltage Range	$VGON_{RNGB}$	dis_navdd = 0	8.4		21	V
VG_{ON} Unipolar Adjustment Step Size	LSB_{VGON}	dis_navdd = 1		0.3		V
VG_{ON} Bipolar Adjustment Step Size	LSB_{VGONB}	dis_navdd = 0		0.2		V
VG_{ON} Internal Feedback Resistor Value	R_{VGON}		700		1250	kΩ
VG_{ON} Output Voltage Accuracy	ACC_{VGON}	0x16h setting	-2		2	%
VG_{OFF} Voltage Range	VG_{OFF_RNG}		-18		-4	V
VG_{OFF} Adjustment Step Size	LSB_{VGOFF}			0.25		V
VG_{OFF} Output-Voltage Accuracy	ACC_{VGOFF}	0x16h setting	-3		+3	%
TFT POWER SECTION / SEQUENCE SWITCHES						
AVDD Switch On-Resistance	R_{ON_AVDD}	V_{HVINP} = 6.8V, I_{AVDD} = -100mA		0.9	1.6	Ω
AVDD Switch Current Limit	I_{LIM_AVDD}		400	500	650	mA
AVDD Discharge Resistance	R_{AVDD_DIS}	AVDD disabled, V_{V18} > V_{V18_UVLO}		1.2		kΩ
PGVDD On-Resistance	R_{ON_PGVDD}	(HVINP - PGVDD), I_{PGVDD} = 10mA		2.5	5	Ω

Electrical Characteristics (continued)

(V_{IN} = 3.3V, V_{BATT} = 12V, typical operating circuit, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PGVDD Current Limit	I_{LIM_PGVDD}	V_{PGVDD} = 3V, V_{HVINP} = 6.8V	70	100		mA
VG_{ON} Discharge Resistance	R_{DIS_VGON}		2	3	4	kΩ
VG_{OFF} Discharge Current	I_{DIS_VGOFF}			1.5		mA
NAVDD Discharge Resistance	R_{NAVDD_DIS}	NAVDD disabled, $V_{V18} > V_{V18\_UVLO}$		1		kΩ
TFT POWER SECTION / TFT FAULT PROTECTION						
Fault Timeout	t_{FAULT}	tfault[1:0] = 10		60		ms
Fault Retry Time	t_{AUTO}	tretry[1:0] = 10 or 11		1.9		s
FLTB Output Frequency		Stand-alone mode only	0.88	1	1.12	kHz
HVINP/AVDD Undervoltage Fault Threshold	THR_{UV}	Relative measurement between HVINP and AVDD	81	85	89	%
HVINP/AVDD Overvoltage Fault Threshold	THR_{OV}	Percentage of set value, voltage rising	111	115	119	%
HVINP/AVDD Short-Circuit Fault Threshold	THR_{SHRT}		36	40	44	%
NAVDD Undervoltage Fault Threshold	THR_{UV}	Of AVDD regulation voltage, NAVDD rising	81	85	89	%
NAVDD Overvoltage Fault Threshold	THR_{OV}	Of AVDD regulation voltage, NAVDD voltage falling	111	115	119	%
NAVDD Short-Circuit Fault Threshold	THR_{SHRT}	Of AVDD regulation voltage, NAVDD voltage rising	36	40	44	%
VG_{ON} Undervoltage Fault Threshold	THR_{UV}	Of set value, VG_{ON} voltage falling	81	85	89	%
VG_{ON} Overvoltage Fault Threshold	THR_{OV}	Of set value, VG_{ON} voltage rising	111	115	119	%
VG_{OFF} Undervoltage Fault Threshold	THR_{UV}	Of set value, VG_{OFF} voltage rising	78		88	%
VG_{OFF} Overvoltage Fault Threshold	THR_{OV}	Of set value, VG_{OFF} voltage falling	105		120	%
Short-Circuit Fault Delay		After completion of soft-start		10		µs
Bandgap Out-of-Range Diagnostic Threshold				±11		%
LED BACKLIGHT DRIVER						
BATT Operating Voltage Range	V_{BATT}		4.5		36	V
BATT Operating Voltage Range after Startup	V_{BATT}	Maximum duration 100ms	3		36	V
BATT Quiescent Supply Current	I_{Q_BATT}			5	10	µA

Electrical Characteristics (continued)

(V_{IN} = 3.3V, V_{BATT} = 12V, typical operating circuit, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BATT Shutdown Supply Current	I_{BATT_SHDN}	V_{EN} = 0V, T_A = +25°C, typical application circuit		1	3	µA
BATT Undervoltage Lockout, Rising	V_{BATT_UVR}	BATT voltage rising	4.15	4.29	4.4	V
BATT Undervoltage Lockout, Falling	V_{BATT_UVF}	BATT voltage falling	2.77	2.9	2.95	V
BATT Threshold for Low-Voltage Operation Mode	V_{BATT_LVF}	BATT voltage falling	5.35	5.5	5.65	V
	V_{BATT_LVR}	BATT voltage rising	5.55	5.72	5.85	
LED BACKLIGHT DRIVER / V5 REGULATOR						
V5 Output Voltage	V_{V5}	5.75V < V_{HVINP} < 18V, I_{V5} = 1mA to 10mA	4.8	5	5.2	V
V5 Dropout Voltage	V_{V5_DRP}	V_{HVINP} = 4.9V, I_{V5} = 5mA		0.05	0.12	V
V5 Undervoltage Lockout	V_{V5_UVLOR}	V5 voltage rising	3.8	3.9	4.1	V
	V_{V5_UVLOF}	V5 voltage falling	3.6	3.7	3.8	
V5 Short-Circuit Current Limit	I_{V5_SC}	V5 shorted to GND	50			mA
V5 Overvoltage Threshold			5.6	5.75	5.9	V
LED BACKLIGHT DRIVER / NGATE OUTPUT						
NGATE Output Voltage	V_{NGATE}	Above V_{BATT}, 3.3V < V_{BATT} < 33V, I_{NGATE} = 1µA	4.3	5.25	6	V
NGATE Source Current	I_{NG_SO}	V_{NGATE} = V_{BATT}	30	50		µA
NGATE Sink Current	I_{NG_SINK}		0.4	0.7		mA
NGATE Output Voltage at High Input Voltage	V_{NGATE_HV}	Above V_{BATT}, V_{BATT} > 35.5V, I_{NGATE} = 1µA	-0.3		0	V
BATT HV Comparator Threshold	V_{LD_THR}	BATT voltage rising	33		35.5	V
BATT HV Comparator Hysteresis	V_{LD_HYS}			0.7		V
NGATE Start Delay	t_{NG_DEL}	Delay between NGATE charge-pump turning on and BSTMON rising		2	2.2	ms
LED BACKLIGHT DRIVER / RT OSCILLATOR						
Switching Frequency Range	f_{SW_RT}	Frequency dithering disabled	400		2200	kHz
Oscillator Frequency Accuracy		I_{RT} = 13.85µA (f_{SW} = 400kHz), I_{RT} = 75µA (f_{SW} = 2200kHz)	-10		10	%
Boost Converter Maximum Duty Cycle, High Frequency		1.3MHz to 2.2MHz	89	91	94	%
Boost Converter Maximum Duty Cycle, Low Frequency		f_{SW} = 400kHz to 1.3MHz	94		98	%

Electrical Characteristics (continued)

(V_{IN} = 3.3V, V_{BATT} = 12V, typical operating circuit, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Boost Minimum On-Time				60		ns
Frequency Dither, High Setting	SSHI	bl_ssl = 0		±6		%
Frequency Dither, Low Setting	SSLO	bl_ssl = 1		±4		%
RT Output Voltage	V_{RT}	R_{RT} = 65kΩ or R_{RT} = 10kΩ	0.875	0.9	0.925	V
Sync Threshold	V_{RT_SYNC}	V_{RT} rising	0.77		0.84	V
Sync Frequency Duty-Cycle	D_{SYNC}			50		%
Sync Frequency Range			400		2200	kHz
LED BACKLIGHT DRIVER / SLOPE COMPENSATION						
Peak Slope-Compensation Current Ramp per Cycle	I_{SLOPE}	Current ramp added to CS	42	50	60	µA
LED BACKLIGHT DRIVER / CURRENT-LIMIT COMPARATOR						
CSP Threshold Voltage	$V_{CSP-CSNL}$	bl_ilim = 1	275	300	325	mV
	$V_{CSP-CSN}$	bl_ilim = 0	380	410	440	
CSP Threshold Voltage During Low Voltage	V_{CSP_LV}	V_{BATT} < V_{BATT_LVF}, V_{BATT} falling	560	600	640	mV
CSP Input Current	I_{CSP}	V_{EN} = 0V, V_{CSP} = 0.4V			+1	µA
LED BACKLIGHT DRIVER / ERROR AMPLIFIER						
OUT_ Regulation High Threshold	V_{THH}	$V_{OUT\_}$ rising	0.825	0.85	0.875	V
OUT_ Regulation Low Threshold	V_{THL}	$V_{OUT\_}$ falling	0.55	0.58	0.61	V
Transconductance	g_M		410	630	890	µS
COMP Sink Current	I_{COMP_SINK}	V_{COMP} = 1V	270	380	500	µA
COMP Source Current	I_{COMP_SRC}	V_{COMP} = 1V	270	380	500	µA
LED BACKLIGHT DRIVER / MOSFET DRIVER						
NDRV On-Resistance	R_{NDRV_LS}	V_{V5} = 5V, I_{NDRV} = 100mA		1.2	2	Ω
	R_{NDRV_HS}	V_{V5} = 5V, I_{NDRV} = -100mA		1.5	3	
NDRV Rise Time	t_{NDRV_R}	C_{NDRV} = 1nF, (*Note 2*)		8		ns
NDRV Fall Time	t_{NDRV_F}	C_{NDRV} = 1nF, (*Note 2*)		8		ns
NDRVS Input Logic-Low	V_{IL_NDRVS}	V_{NDRVS} falling		2	2.4	V
NDRVS Input Logic-High	V_{IH_NDRVS}	V_{NDRVS} rising	2.55	3.3		V
NDRVS Input Current	I_{NDRVS}	V_{NDRVS} = 5V		60		µA
LED BACKLIGHT DRIVER / LED CURRENT SINKS						
IREF Output Voltage	V_{IREF}	I_{IREF} = 40µA	0.86	0.88	0.9	V

Electrical Characteristics (continued)

(V_{IN} = 3.3V, V_{BATT} = 12V, typical operating circuit, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Full-Scale OUT_ Output Current	$I_{OUT\_}$	iset[6:0] = 0x7F, 150mA setting	145	150	154	mA
	I_{OUT100}	iset[6:0] = 0x4D, 100mA setting	97	100	103	
	I_{OUT50}	iset[6:0] = 0x1B, 50mA setting	48	50	52	
	I_{OUT23}	iset[6:0] = 0x00, 23mA setting	21.5	23	25.2	
Current Regulation Between Strings	$I_{OUT\_MATCH150}$	$I_{OUT\_}$ = 150mA, design target	-2		+2	%
Current-Setting Resolution	I_{OUT_LSB}			1		mA
OUT_ Leakage Current	I_{OUT_LEAK}	$V_{OUT\_}$ = 36V, DIM = 0, all OUT_ pins shorted together, T_A = +25°C		0.1	5	µA
		$V_{OUT\_}$ = 36V, DIM = 0, all OUT_ pins shorted together		0.1	15	µA
OUT_ Minimum Pulse Width				300		ns
OUT_ Minimum Negative Pulse Width				90		ns
$I_{OUT\_}$ Rise Time	I_{OUT_TR}	$I_{OUT\_}$ = 150mA, 10% to 90% $I_{OUT\_}$		150		ns
$I_{OUT\_}$ Fall Time	I_{OUT_TF}	$I_{OUT\_}$ = 150mA, 90% to 10% $I_{OUT\_}$		20		ns
LED BACKLIGHT DRIVER / DIM, ADIM INPUTS						
DIM Frequency Range			90		50000	Hz
DIM Sampling Frequency				20		MHz
ADIM Input Frequency Range			10		100	kHz
LED BACKLIGHT DRIVER / LED FAULT DETECTION						
LED Short-Detection Threshold	V_{THSHRT}	I²C mode, bit configuration = 11 (00: short detection disabled), default value in stand-alone mode	7.7	8	8.3	V
		I²C mode, led_short_th[1:0] = 10	5.75	6	6.25	
		I²C mode, led_short_th[1:0] = 01	2.8	3	3.2	
OUT_ Check-LED-Source Current	I_{OUT_CKLED}	$V_{OUT\_}$ = 0.5V	50	60	70	µA
OUT_ Short-to-GND Detection Threshold	V_{OUT_GND}	$V_{OUT\_}$ falling	230	250	270	mV
OUT_ Unused-Detection High Threshold	V_{OUT_UN}		0.8	0.85	0.9	V
OUT_ Open-LED-Detection Threshold	V_{OUT_OPEN}		230	250	270	mV
Shorted-LED-Detection Flag Delay	t_{SHRT}			6.8		µs
LED BACKLIGHT DRIVER / OVERVOLTAGE AND UNDERVOLTAGE PROTECTION						
BSTMON Overvoltage Threshold	V_{BSTMON_OV}	V_{BSTMON} rising	0.92	0.95	0.98	V

Electrical Characteristics (continued)

(V_{IN} = 3.3V, V_{BATT} = 12V, typical operating circuit, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BSTMON Overvoltage Hysteresis	V_{BSTMON_OVHYS}			50		mV
BSTMON Input Bias Current	I_{BSTMON}	0 < V_{BSTMON} < 1V	-1		+1	µA
BSTMON Undervoltage-Trip Threshold	$V_{OVPUVLO}$	V_{BSTMON} rising	0.384	0.4	0.416	V
Boost Undervoltage-Detection Delay	OVPUVLO_BLK			10		µs
Boost Undervoltage-Blanking Time		After soft-start, fast_ss = 1	26.28	28.46	30.74	ms
		After soft-startup, fast_ss = 0	49	53.25	57.5	
TEMP PIN						
TEMP Pin Voltage	V_{TEMP}	I_{TEMP} = -10µA	380	400	420	mV
TEMP to IOUT_ Gain				0.667		%/µA
TEMP Pin Disable Threshold				0.5		V
TEMP Pin Leakage Current		+25°C		0.05	1	µA
TEMP Current for LED Current Disable	I_{TEMPD}		80	120	160	µA
PROGRAMMING VOLTAGE						
V_{PROG} Voltage			8.2	8.5	8.8	V
V_{PROG} Voltage Undervoltage Threshold		V_{PROG} rising		8	8.2	V
V_{PROG} Voltage Overvoltage Threshold		V_{PROG} falling	8.8	9		V
V_{PROG} Input Current		During NV programming, T_A = +25°C		9	25	mA
NV Programming Time				16	20	ms
LOGIC INPUTS AND OUTPUTS (EN, SCL, SDA, DIM, ADD, MODE, PFO)						
Digital Inputs Logic-High	V_{IH}		1.25			V
Digital Inputs Logic-Low	V_{IL}				0.5	V
Digital Inputs Hysteresis	V_{HYS}			300		mV
EN Input Pull-down Resistor			100	165		kΩ
EN Blanking Time	t_{EN_BLK}			10		µs
DIM Pull-up Current	I_{DIM}	V_{DIM} = 0V		5		µA
ADD and MODE Pull-up Current	I_{ADD_MODE}	V_{ADD} = V_{MODE} = 0V		2		µA
SCL Input Current	I_{SCL}	V_{SCL} = +5V			+1	µA
PFO, FLTB, SDA Output Low Voltage	V_{OL_OUT}	I_{FLTB} = I_{SDA} = I_{PFO} = 5mA			0.4	V
PFO, FLTB, SDA Output Leakage Current	I_{OUT_LEAK}	V_{EN} = 0V, V_{FLTB} = V_{SDA} = V_{PFO} = 5.5V			+1	µA

Electrical Characteristics (continued)

(V_{IN} = 3.3V, V_{BATT} = 12V, typical operating circuit, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL WARNING/SHUTDOWN						
Thermal-Warning Threshold, TFT Section	T_{WARN_TFT}	Temperature rising		125		°C
Thermal-Warning Threshold, Backlight Section	T_{WARN_BL}			125		°C
Thermal-Shutdown Threshold, TFT Section	T_{SHDN_TFT}	Temperature rising		165		°C
Thermal-Shutdown Threshold, Backlight Section	T_{SHDN_BL}	Temperature rising		160		°C
Thermal-Shutdown Hysteresis	T_{SHDN_HYS}			17		°C
ANALOG-TO-DIGITAL CONVERTER						
ADC Measurement Resolution	ADC_{BIT}	(*Note 2*)		8		bits
Total Measurement Error, Current	E_ADC_{OUT}	150mA setting	-8		+8	mA
Total Measurement Error, BSTMON	E_ADC_{BSTMON}	V_{BSTMON} = 0.9V	-70		70	mV
ADC Gain Error	ADC_{GAIN}	150mA setting	-4		+4	%
ADC Offset Error	ADC_{OFF}	150mA setting	-4		+4	LSB
Measurement Resolution, Current	LSB_{OUT}			0.64		mA
Measurement Resolution, BSTMON	LSB_{BSTMON}			3.9216		mV
I²C INTERFACE						
Clock Frequency	f_{SCL}				0.4	MHz
Hold Time (Repeated) START	$t_{HD:STA}$		600			ns
SCL Low Time	t_{LOW}		1300			ns
SCL High Time	t_{HIGH}		600			ns
Setup Time (Repeated) START	$t_{SU:STA}$		600			ns
Data Hold Time	$t_{HD:DAT}$		0			ns
Data Setup Time	$t_{SU:DAT}$		100			ns
Setup Time for STOP Condition	$t_{SU:STO}$		600			ns
Spike Suppression				50		ns

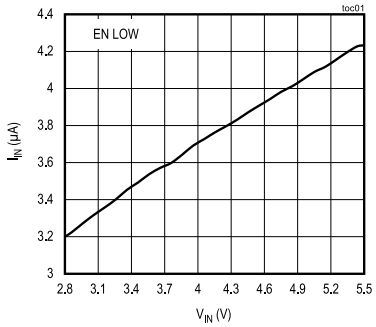
Note 1: Limits are 100% tested at T_A = +25°C, T_A = +125°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Guaranteed by design. Not production tested.

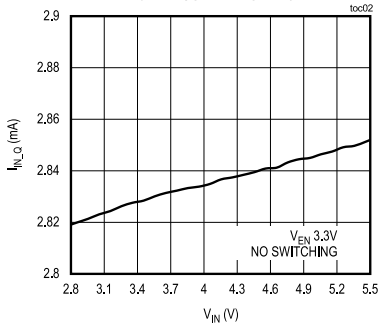
Typical Operating Characteristics

(T_A = +25°C, V_{IN} = V_{INN} = 3.3V, V_{BATT} = 12V, f_{DIM} = 200Hz, unless otherwise noted.)

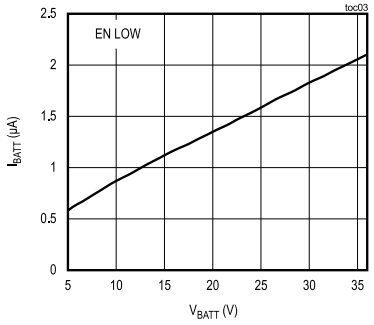
TOTAL INPUT SHUTDOWN CURRENT vs. TFT SUPPLY VOLTAGE



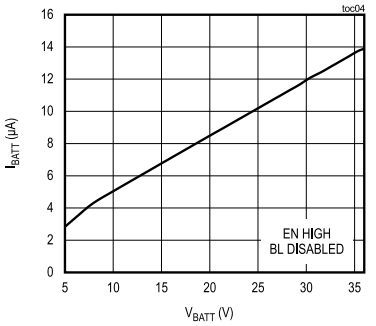
TOTAL IN QUIESCENT CURRENT vs. TFT SUPPLY VOLTAGE



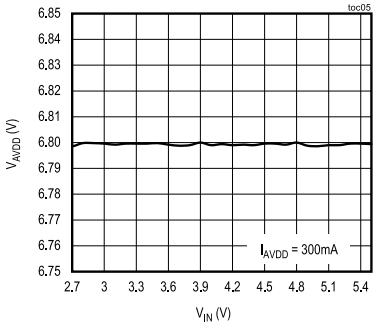
TOTAL BATT SHUTDOWN CURRENT vs. BATT SUPPLY VOLTAGE



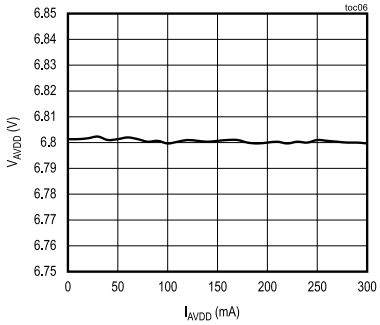
TOTAL BATT QUIESCENT CURRENT vs. BATT SUPPLY VOLTAGE



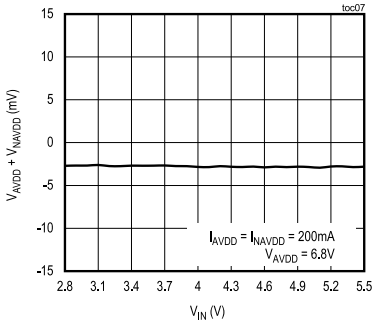
AVDD LINE REGULATION AT 6.8V



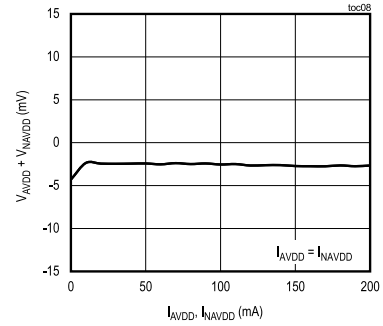
AVDD LOAD REGULATION AT 6.8V



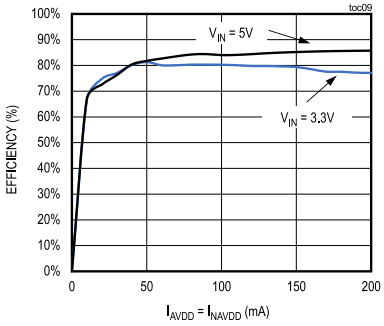
AVDD + NAVDD LINE REGULATION



AVDD + NAVDD LOAD REGULATION



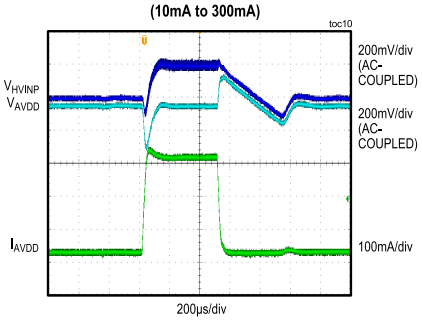
EFFICIENCY WITH DIFFERENTIAL LOAD FROM AVDD TO NAVDD



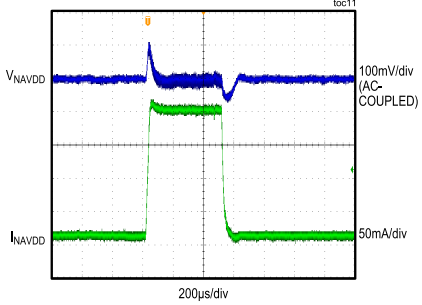
Typical Operating Characteristics (continued)

(T_A = +25°C, V_{IN} = V_{INN} = 3.3V, V_{BATT} = 12V, f_{DIM} = 200Hz, unless otherwise noted.)

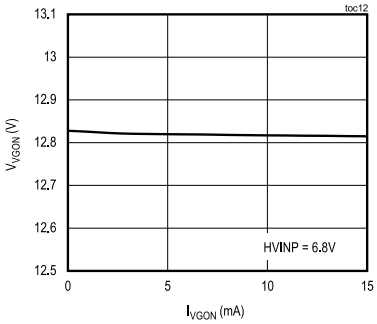
AVDD LOAD-TRANSIENT RESPONSE AT 6.8V (10mA to 300mA)



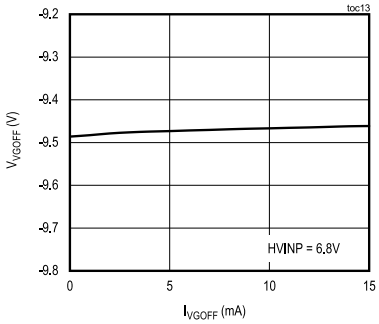
NAVDD LOAD-TRANSIENT RESPONSE AT -6.8V (10mA TO 200mA)



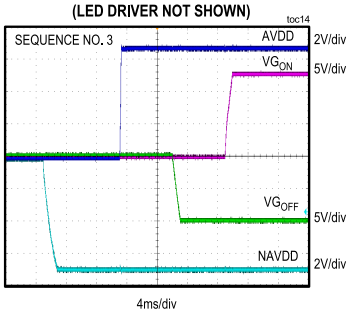
VGON LOAD REGULATION



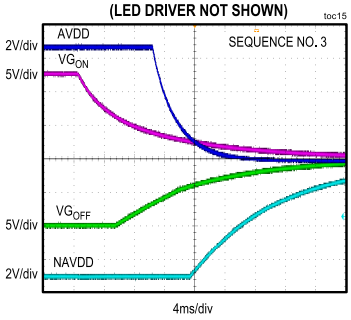
VGOFF LOAD REGULATION



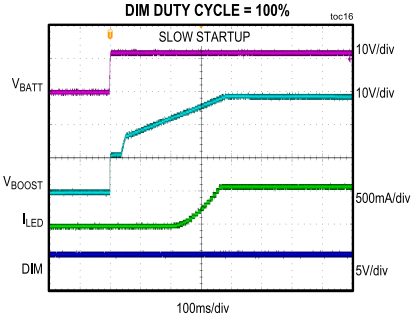
POWER-UP SEQUENCE OF ALL SUPPLY OUTPUTS (LED DRIVER NOT SHOWN)



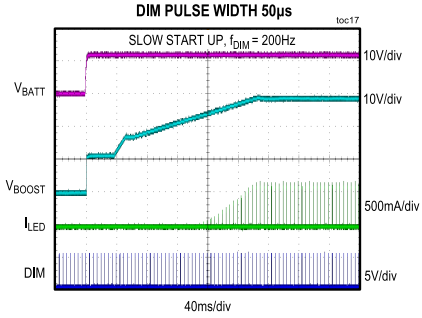
POWER-OFF SEQUENCE OF ALL SUPPLY OUTPUTS (LED DRIVER NOT SHOWN)



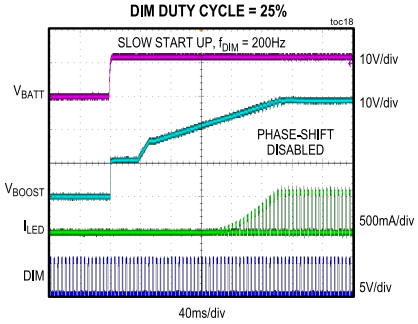
STARTUP WAVEFORM OF LED DRIVER AT DIM DUTY CYCLE = 100%



STARTUP WAVEFORM OF LED DRIVER WITH DIM PULSE WIDTH 50µs



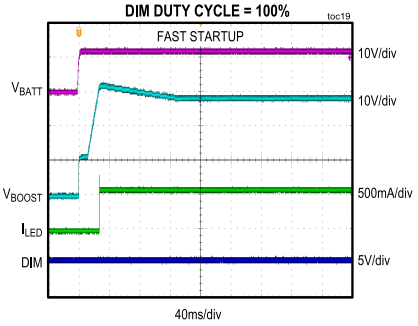
STARTUP WAVEFORM OF LED DRIVER WITH DIM DUTY CYCLE = 25%



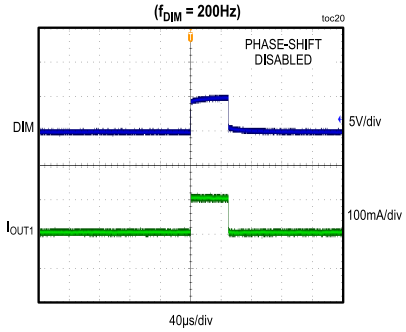
Typical Operating Characteristics (continued)

(T_A = +25°C, V_{IN} = V_{INN} = 3.3V, V_{BATT} = 12V, f_{DIM} = 200Hz, unless otherwise noted.)

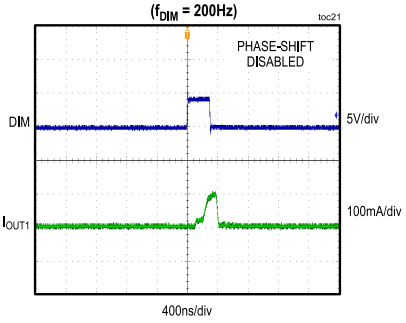
STARTUP WAVEFORM OF LED DRIVER WITH DIM DUTY CYCLE = 100%



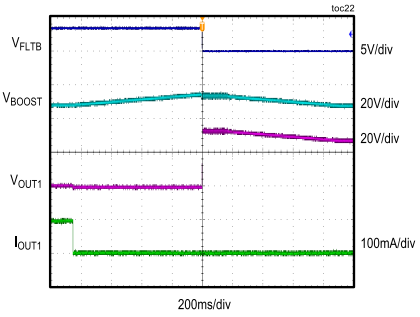
LED SWITCHING WITH DIMMING PULSE WIDTH OF 50µs (f_{DIM} = 200Hz)



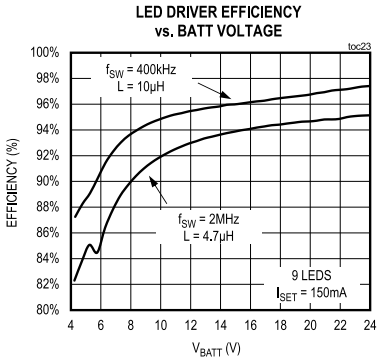
LED SWITCHING WITH DIMMING PULSE WIDTH OF 300ns (f_{DIM} = 200Hz)



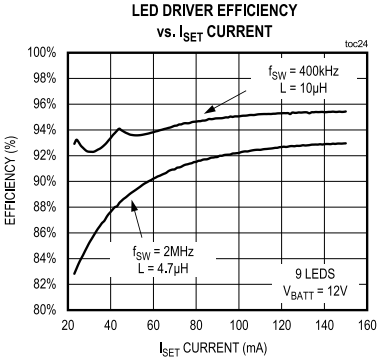
LED OPEN FAULT ON OUT1



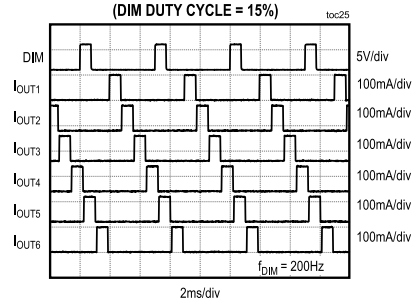
LED DRIVER EFFICIENCY vs. BATT VOLTAGE



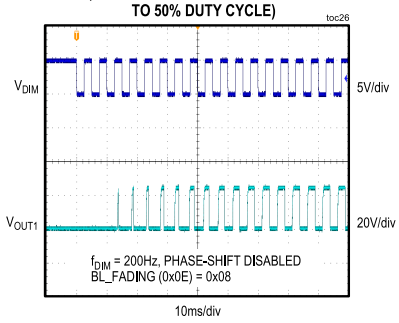
LED DRIVER EFFICIENCY vs. I_{SET} CURRENT



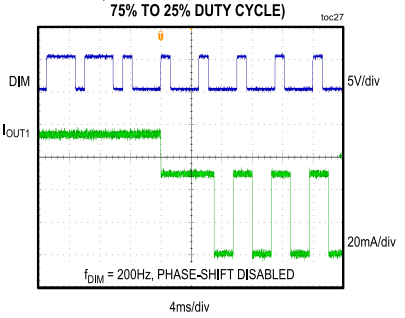
PHASE-SHIFTED LED OUTPUT CURRENTS (DIM DUTY CYCLE = 15%)



FADING WAVEFORM (DIMMING TRANSITION FROM 100% TO 50% DUTY CYCLE)



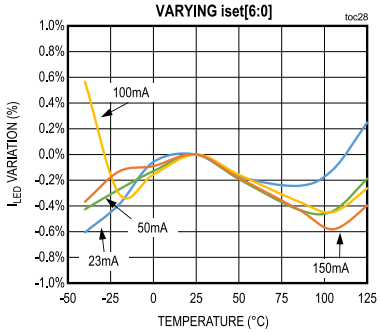
HYBRID DIMMING WAVEFORM (DIMMING TRANSITION FROM 75% TO 25% DUTY CYCLE)



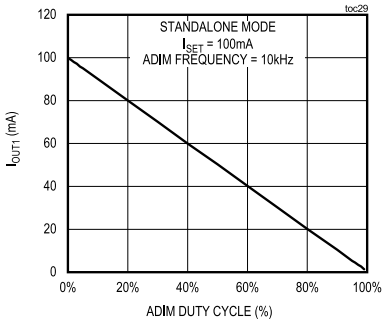
Typical Operating Characteristics (continued)

(T_A = +25°C, V_{IN} = V_{INN} = 3.3V, V_{BATT} = 12V, f_{DIM} = 200Hz, unless otherwise noted.)

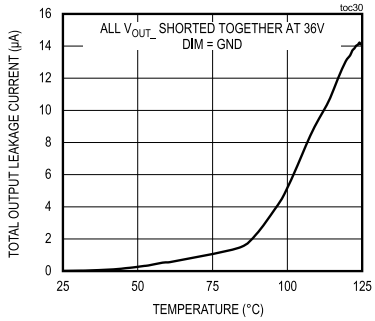
LED CURRENT VARIATION vs. TEMPERATURE VARYING iset[6:0]



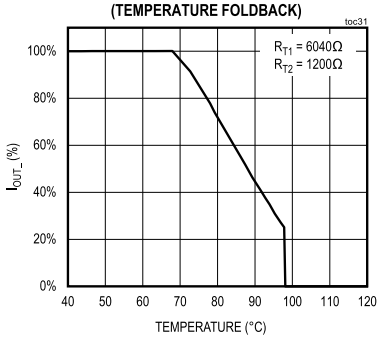
LED CURRENT vs. ADIM DUTY CYCLE



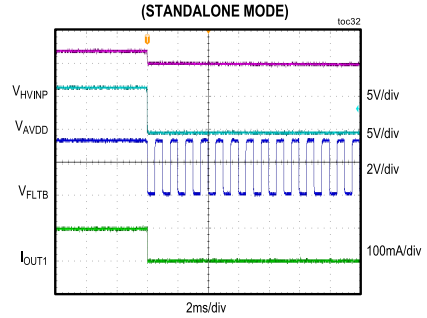
OUTPUT LEAKAGE CURRENT vs. TEMPERATURE



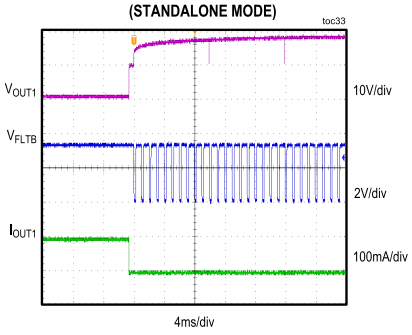
LED CURRENT vs. TEMPERATURE (TEMPERATURE FOLDBACK)



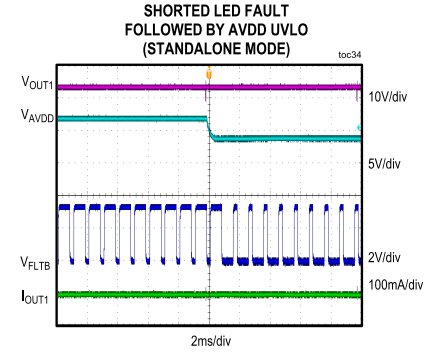
AVDD SHORTED TO GROUND (STANDALONE MODE)



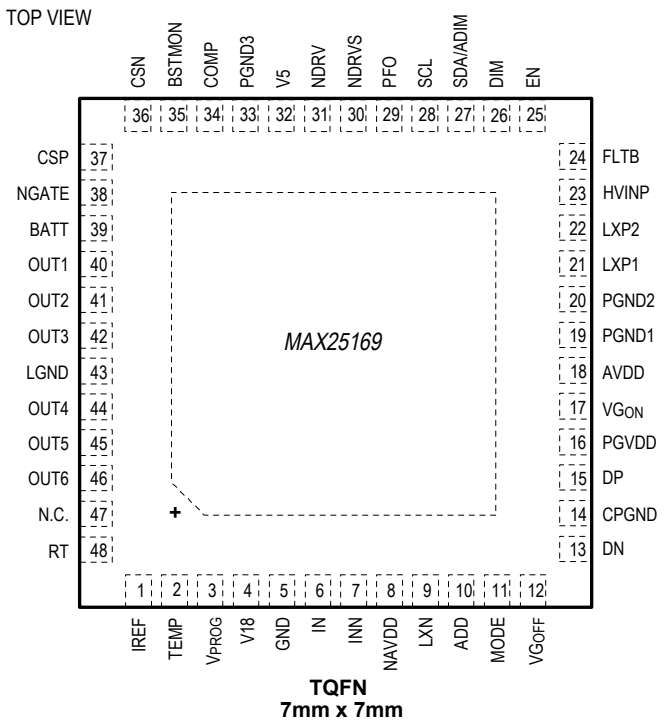
LED FAULT CREATED BY SHORTING 3 LEDS IN STRING 1 (STANDALONE MODE)



SHORTED LED FAULT FOLLOWED BY AVDD UVLO (STANDALONE MODE)



Pin Configuration



TQFN
7mm x 7mm

Pin Description

PIN	NAME	FUNCTION
1	IREF	Reference Current Set Pin. Connect a 1% resistor of value 22kΩ from IREF to GND.
2	TEMP	Temperature Sensor Input. To implement LED current reduction at high temperatures, connect an NTC temperature sensor (e.g., the NTCLE100E3103G) to GND with resistors from the NTC to TEMP and to V18. If unused, connect TEMP to V18.
3	V_{PROG}	Programming Voltage. Apply a voltage of 8.5V to this pin during the programming of nonvolatile registers. Connect to GND through a resistor during normal operation.
4	V18	Output of Internal 1.8V Regulator. Connect 1µF and 22nF capacitors in parallel from V18 to GND with an additional 100nF capacitor close to the V18 and GND pins.
5	GND	Ground Connection
6	IN	Supply Input. Connect at least one 10µF ceramic capacitor from IN to GND for proper operation.
7	INN	Buck-Boost Converter Input. Connect a 10µF ceramic capacitor from INN to GND for proper operation.
8	NAVDD	Negative Source-Driver Output Voltage
9	LXN	DC-DC Inverting Converter Inductor/Diode Connection
10	ADD	Device Address Select Pin. Connect to GND or V18 to select the device I²C address. See Table 5. ADD has an internal pull-up to V18.
11	MODE	Mode Selector Pin. Together with ADD, this pin determines the mode of operation of the I²C interface and whether it is used. See Table 3. MODE has an internal pull-up to V18.

Pin Description (continued)

PIN	NAME	FUNCTION
12	VG_{OFF}	Output of Negative Charge-Pump Block. Connects directly to the negative charge-pump output to facilitate VG_{OFF} discharge through an internal switch connected between VG_{OFF} and GND. VG_{OFF} is also the regulator feedback pin.
13	DN	Regulated Charge-Pump Driver for the Negative Charge Pump. Connect to an external flying capacitor.
14	CPGND	Charge Pump Ground
15	DP	Regulated Charge-Pump Driver for Positive Charge Pump. Connect to an external flying capacitor.
16	PGVDD	Switched Version of HVINP Voltage for the Positive Charge Pump. Provides soft-start control of the VG_{ON} output. Bypass PGVDD with a 1µF ceramic capacitor to GND.
17	VG_{ON}	Output of Positive Charge-Pump Block. VG_{ON} connects directly to the positive charge-pump output to facilitate VG_{ON} discharge through an internal switch connected between VG_{ON} and GND. VG_{ON} is also the regulator feedback pin.
18	AVDD	Positive Source-Driver Output Voltage. Bypass AVDD with a capacitor to GND.
19	PGND1	Power-Ground Connection
20	PGND2	Power-Ground Connection
21	LXP1	Boost HVINP Converter Switching-Node Connection. Connect LXP1 to the external inductor and rectifier diode.
22	LXP2	Boost HVINP Converter Switching-Node Connection. Connect LXP2 to the external inductor and rectifier diode.
23	HVINP	Boost Output and Input for the AVDD, PGVDD, and Charge Pumps
24	FLTB	Active-Low, Open-Drain Fault Indication Output. Connect an external pull-up resistor from FLTB to an external supply lower than 5V.
25	EN	Enable Input. When EN is high, the device is enabled. With EN low, the device is in shutdown with low quiescent current. EN has an internal pull-down resistor.
26	DIM	PWM Dimming Input. DIM has an internal pull-up to V18.
27	SDA/ADIM	I²C Data I/O. Connect a pull-up resistor from SDA to the system logic supply. In standalone mode, this pin is the analog dimming input (if unused, connect to GND).
28	SCL	I²C Clock Input. Connect a pull-up resistor from SCL to the system logic supply.
29	PFO	Open-Drain Power-Fail Indicator Pin. When the IN voltage is below a threshold, the PFO output goes low. Add an external pull-up resistor between PFO and IN.
30	NDRVS	Sense Connection for Gate of External MOSFET. Connect NDRVS directly to the gate after the gate resistor.
31	NDRV	Switching nMOSFET Gate-Driver Output. Connect NDRV to the gate of the external switching-power MOSFET. Typically, a small resistor (1Ω to 22Ω) is inserted between the NDRV output and nMOSFET gate to decrease the slew rate of the gate driver and reduce the switching noise.
32	V5	5V Regulator Output, Voltage Supply for NDRV Gate Driver. Place a 2.2µF ceramic capacitor as close as possible to V5 and PGND3.
33	PGND3	Power-Ground Connection
34	COMP	LED Driver Switching-Converter Compensation Input. Connect an RC network from COMP to GND to compensate the backlight boost converter (see the *Feedback Compensation* section).
35	BSTMON	LED Driver Output-Voltage-Sensing Input. This voltage is used for overvoltage and undervoltage protection.
36	CSN	LED Driver MOSFET Negative Current-Sense Connection. Connect this pin directly to the GND side of the compensation network connected to the COMP pin.

Pin Description (continued)

PIN	NAME	FUNCTION
37	CSP	LED Driver MOSFET Positive Current-Sense Connection. Connect a sense resistor from the MOSFET source to PGND and a further resistor from the MOSFET source to the CSP pin to set the slope compensation (see the *Current-Sense Resistor and Slope Compensation* section).
38	NGATE	Gate Connection for External Series nMOSFET Driven by the Internal Charge Pump
39	BATT	LED Driver Supply Input. Connect BATT to a 4.5V to 36V supply. Bypass BATT to ground with a ceramic capacitor.
40	OUT1	LED String 1 Cathode Connection
41	OUT2	LED String 2 Cathode Connection. Connect OUT2 to ground using a 9.1kΩ resistor, if not used.
42	OUT3	LED String 3 Cathode Connection. Connect OUT3 to ground using a 9.1kΩ resistor, if not used.
43	LGND	LED Ground Connection
44	OUT4	LED String 4 Cathode Connection. Connect OUT4 to ground using a 9.1kΩ resistor, if not used.
45	OUT5	LED String 5 Cathode Connection. Connect OUT4 to ground using a 9.1kΩ resistor, if not used.
46	OUT6	LED String 6 Cathode Connection. Connect OUT4 to ground using a 9.1kΩ resistor, if not used.
47	N.C.	Not internally connected.
48	RT	Frequency Setting Resistor for Backlight Boost Converter
—	EP	Exposed Pad. Connect to a large contiguous copper-ground plane for optimal heat dissipation. Do not use EP as the only electrical ground connection.

Detailed Description

The MAX25169 is a highly integrated TFT power supply and LED backlight driver IC for automotive TFT-LCD applications. The IC integrates one boost converter, one inverting buck-boost converter, two gate-driver supplies, and a boost/SEPIC controller that can power 1 to 6 strings of LEDs in the display backlight. The complete device configuration can be stored in on-board nonvolatile memory.

The source-driver power supplies consist of a boost converter and an inverting buck-boost converter that can generate voltages up to +18V and down to -10.5V. The positive source-driver can deliver up to 300mA at 13.5V, while the negative source driver is capable of 200mA. The positive source-driver-supply regulation voltage (V_{AVDD}) is set through I2C. The negative source-driver-supply voltage (V_{NAVDD}) is always tightly regulated to -V_{AVDD}. The source-driver supplies operate from an input voltage between 2.65V and 5.5V.

The gate-driver-power supplies consist of regulated charge pumps that generate up to +31.5V and down to -18V and can deliver up to 15mA each.

The IC features a 6-string LED driver with input switch control (NGATE) that can power up to 6 strings of LEDs with 150mA (max) of current per string. Logic-controlled and I2C-controlled pulse-width modulation (PWM) dimming are included, with minimum pulse widths as low as 300ns and the option of phase shifting the LED strings with respect to one another. When phase shifting is enabled, each string is turned on at a different time, reducing the input and output ripple, as well as audible noise. With phase shifting disabled, each current sink turns on at the same time and allows parallel connection of current sinks.

The startup and shutdown sequences for all power domains are controlled using one of the eight preset modes that are selectable using a nonvolatile setting. When a regulator other than HVINP is enabled, the HVINP boost is automatically enabled (if not previously active). In this case, the second regulator is enabled when the soft-start of HVINP has completed.

Supply Voltages

The voltage on IN is the main supply voltage for the device. An on-chip regulator derives a 1.8V supply from the voltage on IN, and this 1.8V supply provides power to most of the on-chip circuitry. The IN voltage must be greater than V_{IN_UVLO} to allow device operation. In addition, V18 must be greater than V_{V18_UVLO} for the device to function. If the voltage on IN drops below V_{PFO}, the PFO output asserts low until the V18 supply reaches its undervoltage lockout level. When IN is connected directly to EN, a vin_uvlo fault may be detected at power-up. To avoid this, place a filter with a time constant of at least 10ms composed of a resistor from IN to EN and a capacitor from EN to GND.

The voltage on the BATT pin is the reference for the NGATE drive output. The voltage on BATT must exceed V_{BATT_UVR} in order for the backlight section to work. (V5 must also exceed V_{VCC_UVLOR}.) Once the backlight block is operating, the BATT voltage can drop as low as V_{BATT_UVF} while maintaining operation (and V5 must remain above V_{VCC_UVLOF} at all times). The drive output for the external boost MOSFET (NDRV) is powered from the V5 voltage, which is nominally 5V. V5 is derived from the HVINP voltage. In the case of HVINP voltages less than 5V, the V5 regulator will be in dropout and the NDRV output will not reach 5V.

PFO Output

PFO is an open-drain output which indicates that the voltage on the IN pin is below a threshold of V_{PFO_F}. The PFO output asserts low in this situation.

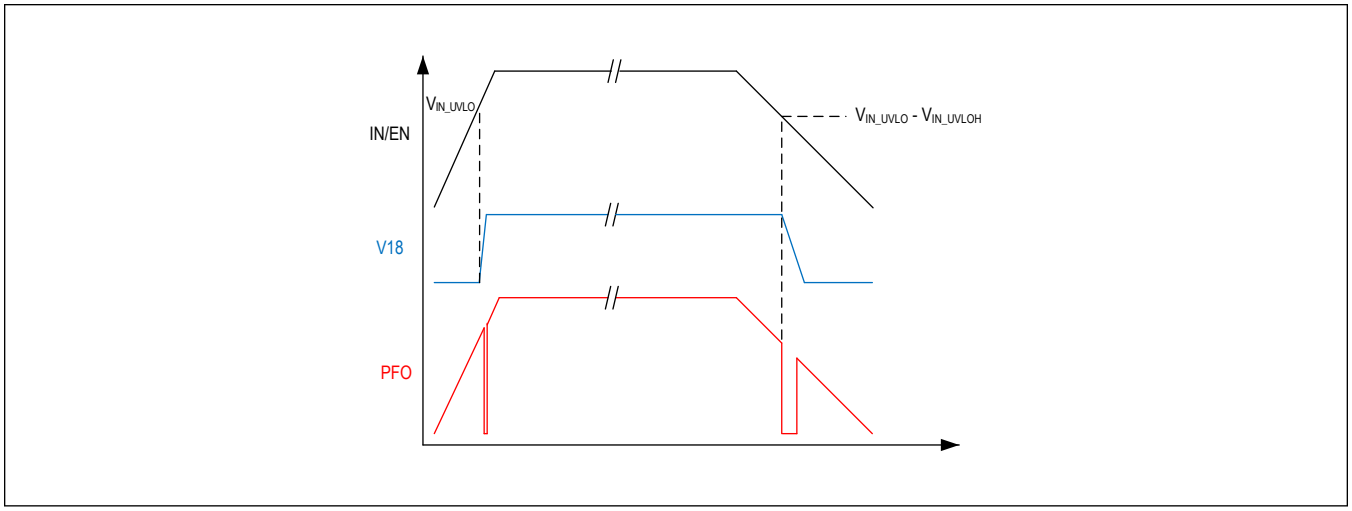


Figure 1. PFO Waveform

The threshold for the PFO output can be selected using the pfo_th bit in the SEQ register (address 0x09). This bit can also be stored in nonvolatile memory. The nominal thresholds are shown in Table 1:

Table 1. PFO Thresholds

SETTING OF pfo_th BIT	PFO FALLING THRESHOLD (V)
0 (default)	2.5
1	2.4

TFT Power Section

Source-Driver Power Supplies

The source-driver power supplies consist of a boost converter (with output at HVINP) with output switch and an inverting buck-boost converter that can be used in one of two ways:

- Boost converter only or unipolar mode: In this case, the boost converter output voltage range is from 11.7V to 18V, the VG_{ON} range is from 12.6V to 31.5V, and the inverting converter is not used. To invoke this mode, set the dis_navdd bit in register TFT_CONFIG to 1. In this mode, the external components on LXN and NAVDD can be omitted and INN should be connected to IN.
- Bipolar mode: In this mode, both converters operate and the inverting converter output voltage tracks the output voltage of the boost converter. V_{NAVDD} cannot be adjusted independently of V_{AVDD}. In this mode, the boost converter output voltage range is 4.9V to 10.5V, and the VG_{ON} range is 8.4V to 21V. This is the default mode of operation (dis_navdd = 0).

AVDD Switch

To facilitate sequencing, the AVDD current-limited switch connects the output of the HVINP boost converter to the capacitor at AVDD. When the AVDD output is turned on, the current limit of the switch is increased in eight steps to its final value. The total time to reach the maximum current limit setting is half of the soft-start time as set by the tstart[1:0] field in the SEQ register. This avoids a sudden drop in HVINP voltage or a surge in input current from IN during AVDD start-up.

Gate-Driver Power Supplies

The positive gate-driver power supply (VG_{ON}) generates up to +31.5V (max) and the negative gate-driver power supply (VG_{OFF}) generates as low as -18V (min). Both can supply up to 15mA output current in tripler/doubling inverter configurations. The VG_{ON} and VG_{OFF} regulation voltages are set independently by writing to the vgon[5:0] and vgoff[5:0] fields in the VG_{ON} and VG_{OFF} registers. Note that the VG_{ON} voltage also depends on the setting of the dis_navdd bit in

the TFT_CONFIG register (address 0x07).

Sequencing

When the start bit in the START register is set to 1, the outputs are enabled in the sequence programmed in the seq_set bits. The start bit can be set to 1 and stored in the nv_start nonvolatile bit so that the device powers up automatically when the EN pin is taken high. The setting should be written before the sequence is executed and should not be changed during the turn-on or turn-off sequences. The sequence options are shown in Table 2:

Table 2. Sequencing

	SEQUENCE SET BITS			POWER-ON				POWER-OFF (REVERSE-ORDER OF POWER-ON)			
SEQUENCE NO.	**seq_set2**	**seq_set1**	**seq_set0**	**1st**	**2nd after t1 ms**	**3rd after t2 ms**	**4th after t3 ms**	**1st**	**2nd after t3 ms**	**3rd after t2 ms**	**4th after t1 ms**
1	0	0	0	AVDD	NAVDD	VG_{OFF}	VG_{ON}	VG_{ON}	VG_{OFF}	NAVDD	AVDD
2	0	0	1	AVDD	NAVDD	VG_{ON}	VG_{OFF}	VG_{OFF}	VG_{ON}	NAVDD	AVDD
3 (default)	0	1	0	NAVDD	AVDD	VG_{OFF}	VG_{ON}	VG_{ON}	VG_{OFF}	AVDD	NAVDD
4	0	1	1	NAVDD	AVDD	VG_{ON}	VG_{OFF}	VG_{OFF}	VG_{ON}	AVDD	NAVDD
5	1	0	0	NAVDD	VG_{OFF}	AVDD	VG_{ON}	VG_{ON}	AVDD	VG_{OFF}	NAVDD
6	1	0	1	VG_{OFF}	VG_{ON}	NAVDD	AVDD	AVDD	NAVDD	VG_{ON}	VG_{OFF}
7	1	1	0	AVDD/ NAVDD	VG_{OFF}	VG_{ON}	—	VG_{ON}	VG_{OFF}	AVDD/ NAVDD	—
8	1	1	1	AVDD/ NAVDD	VG_{ON}	VG_{OFF}	—	VG_{OFF}	VG_{ON}	AVDD/ NAVDD	—

When dis_navdd is set to 1 and the NAVDD output is disabled, the NAVDD slot in Table 2 remains without the output being turned on.

The times in Table 2 are determined by the delayt1, delayt2, and delayt3 settings in the DELAY register (address 0x08). The fastest power-up is obtained by setting the delays to 0. After all of the TFT outputs have exceeded their power-good levels, the backlight block is turned on.

The output voltages are not monitored during off sequencing; each output is turned off in turn using the programmed delays, as seen in Figure 2. When the delays are set to 0, outputs are turned off in sequence with 1ms delays. A sequence can be stored in nonvolatile memory by writing to the burn_otp_reg register.

The V18 linear regulator is powered down 200ms after the power-down sequence is complete if power-down is performed using the EN pin. After this time, the device is in shutdown mode and can be restarted by setting the EN input high. If the outputs are turned off by taking the START bit low, the V18 regulator remains on.

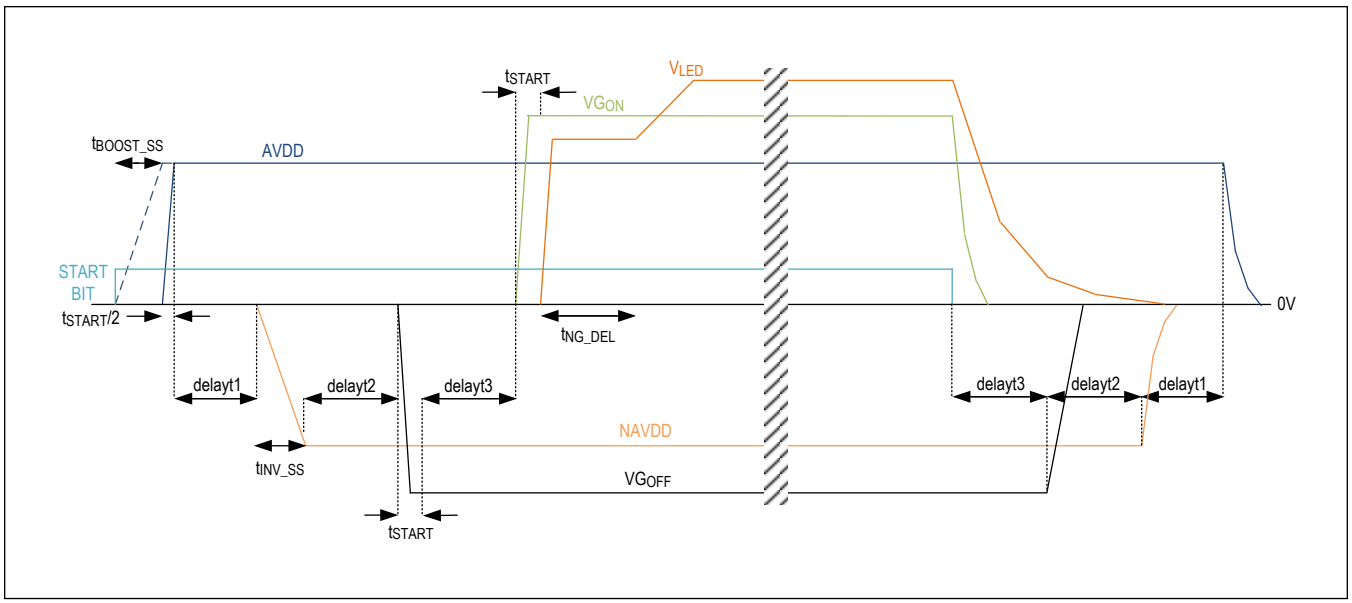


Figure 2. Output Sequencing

Description of the LED Driver

The IC also includes a high-efficiency, high-brightness LED driver that integrates all of the necessary features to implement a high-performance backlight driver to power LEDs in medium-to-large-sized displays for automotive and general applications. The IC provides load-dump voltage protection up to 40V in automotive applications and incorporates two major blocks: a DC-DC controller with peak current-mode control to implement a boost, or a SEPIC-type switched-mode power supply and a 6-channel LED driver with 23mA to 150mA constant-current-sink capability per channel.

The IC features constant-frequency, peak current-mode control with programmable slope compensation to control the duty cycle of the PWM controller. The DC-DC converter implemented using the controller generates the required supply voltage for the LED strings from a wide input-supply range. Connect LED strings from the DC-DC converter output to the 6-channel constant-current-sink drivers (OUT1–OUT6) to control the current through the LED strings. The LED current in all 6 LED strings is set by writing to the iset[6:0] field in the ISET register (address 0x0A).

The IC features adaptive voltage control that adjusts the converter output voltage depending on the forward voltage of the LED strings. This feature minimizes the voltage drop across the constant-current-sink drivers and reduces power dissipation in the device. The backlight boost and current sinks are enabled when the complete sequence of the TFT bias section is completed.

The IC provides a very wide (16,666:1) PWM dimming range at 200Hz dimming frequency (with a dimming pulse as narrow as 300ns). The internal dimming signal is derived from the DIM signal or from the phase-shift dimming logic. Phase shifting of the LED strings can be disabled by writing to the psen bit in the BL_CONFIG1 register (address 0x0B).

Other advanced features include detection and string disconnect for open-LED strings, partially or fully shorted strings, and unused strings. Overvoltage protection clamps the BSTMON voltage and thus the converter output voltage in the event of an open-LED condition.

The shorted-LED string threshold is programmable using the sldet[1:0] field in the BL_CONFIG2 register (address 0x0C).

The FLTB signal asserts low to indicate open-LED, shorted-LED, and overtemperature conditions if they are not masked.

Disable individual current-sink channels by connecting the corresponding OUT_ to LGND_ through a 9.1kΩ resistor (starting with OUT6). In this case, FLTB will not indicate an open-LED condition for the disabled channel.

Undervoltage Lockout

The WLED section features two UVLOs that monitor the input voltage at BATT and the output of the internal LDO

regulator at V5. The backlight boost is active only when both BATT and V5 exceed their respective UVLO thresholds.

Low-Voltage Operation

After the boost soft-start is completed, the MAX25169 can continue to operate with BATT voltages as low as 3V.

At very low input voltages, the efficiency of the boost converter reduces and the input current can reach very high levels as a consequence. When the BATT voltage falls below V_{BATT_LVF}, the boost converter current limit is automatically increased to V_{CSP_LV}, and the switching frequency is reduced if it is greater than 1.35MHz. In this mode, if the standard current limit is exceeded on four consecutive cycles, a 100ms timer is started which returns the current limit to its original value when it expires. When the input voltage returns above V_{BATT_LVR}, operation at the normal switching frequency is resumed.

The external boost converter components must be selected for worst-case operation. An alternative is to reduce the output power at low input voltages.

If the voltage at BATT drops below the undervoltage lockout level (V_{BATT_UVF}) at any time, the boost converter is disabled.

Oscillator Frequency/External Synchronization

The internal oscillator frequency is programmable between 400kHz and 2.2MHz using a timing resistor (R_{RT}) connected from the RT pin to GND. Use the following equation to calculate the value of R_{RT} for the desired switching frequency (f_{SW}):

$$R_{RT} = \frac{26400000}{f_{SW}} - 0.32$$

where R_{RT} is in kΩ and f_{SW} is in Hz. If the value of the RT resistor is too low or if the pin is shorted to GND, the boost converter does not start, the FLTB pin goes low, and the rtoor bit in the BL_DIAG register is set.

To synchronize the oscillator with an external clock, AC-couple the external clock to the RT input. The value of the capacitor used for AC-coupling is C_{SYNC} = 10pF, and the duty cycle of the external clock should be 50%. When synchronizing the converter, do not apply the synchronizing signal to the RT pin at startup, as this may cause the RT resistor value check to fail.

At low input voltages and when the switching frequency is above 1.35MHz, the switching frequency is automatically reduced to 1.35MHz to enable high-duty-cycle operation and maintain output voltage regulation. This does not apply when the device is synchronized to an external frequency.

Spread-Spectrum Modulation

The IC includes a spread-spectrum mode that reduces peak electromagnetic interference (EMI) at the switching frequency and its harmonics. Spread spectrum can be enabled and disabled using the bl_ss_off bit in the BL_CONFIG2 register (address 0x0C).

Spread spectrum uses a pseudorandom dithering technique where the switching frequency is varied in the 94% to 106% or 97% to 103% range (set by the bl_ssl bit in BL_CONFIG2) of the programmed switching frequency set through the external resistor from RT to GND. When spread spectrum is used, the total energy at the fundamental and each harmonic is spread over a wider bandwidth, thus reducing the peak energy at the relevant frequency.

Spread spectrum is disabled if external synchronization is used.

LED Forward Voltage

The forward voltage of the LEDs driven by the MAX25169 varies with current and temperature. While the LED forward voltage increases with current, it decreases with temperature. The highest voltage across a string of LEDs is thus encountered at the minimum operating temperature. When using the MAX25169, the worst-case total string voltage (at the minimum operating temperature) including the voltage across the device OUT_ pins should be kept below the absolute maximum rating of 42V. Under normal operating conditions and over temperature, it is recommended that the boost output voltage be less than or equal to 36V. Select the BSTMON resistor-divider in order to guarantee a maximum voltage of 42V using the procedure described in the *Open-LED Management and Overvoltage Protection (OVP)* section.

LED Current Control

The IC features 6 identical constant-current sources used to drive multiple high-brightness LED strings. The current through each of the channels is adjustable between 23mA and 150mA by setting the 7-bit value iset in the ISET register.

Multiple channels can be paralleled together for string currents exceeding 150mA.

Current-Mode DC-DC Controller

The IC backlight boost is a constant-frequency, current-mode controller designed to drive the LEDs in a boost or SEPIC configuration. The IC features multiloop control to regulate the peak current in the inductor, as well as the voltage across the LED current sinks to minimize power dissipation.

Programmable slope compensation is used to avoid subharmonic oscillation that can occur at > 50% duty cycles in continuous-conduction mode.

The external nMOSFET is turned on at the beginning of every switching cycle. The inductor current ramps up linearly until it is turned off at the peak current level set by the feedback loop. The peak inductor current is sensed from the voltage across the current-sense resistor (R_{CS}) that is connected from the source of the external nMOSFET to PGND.

The IC features leading-edge blanking to suppress the external nMOSFET switching noise. A PWM comparator compares the current-sense voltage plus the slope-compensation signal with the output of the transconductance error amplifier. The controller turns off the external nMOSFET when the voltage at CS exceeds the error amplifier's output voltage (at the COMP pin). This process repeats every switching cycle to achieve peak current-mode control.

In addition to the peak current-mode-control loop, the IC has two other feedback loops for control. The converter output voltage is sensed through the BSTMON input, which goes to the inverting input of the error amplifier.

The BSTMON gain (A_{OVP}) is defined as V_{OUT}/V_{BSTMON}, or (R17 + R16)/R16 (see the *Typical Application Circuit*). The other feedback comes from the OUT_ current sinks. This loop controls the headroom of the current sinks to minimize total power dissipation, while still ensuring accurate LED current matching. Each current sink has a window comparator with a low threshold of 0.58V and a high threshold of 0.85V. These comparators drive logic that controls an up/down counter. The up/down counter is updated on every falling edge of the DIM input and drives an 8-bit digital-to-analog converter (DAC), which sets the reference to the error amplifier. When the system is in steady state, all of the active OUT_ pin voltages should be over the minimum window threshold, and at least one should be lower than the upper threshold.

9-Bit Digital-to-Analog Converter (DAC)

The error amplifier's reference input is controlled with an 9-bit DAC. The DAC output is ramped up during startup to implement a soft-start function (see the *Startup Sequence* section). During normal operation, the DAC output range is limited to between 0.482V and 0.996V. Because the DAC output is limited to no less than 0.482V during normal operation, the overvoltage threshold for the output should be set to a value less than twice the minimum LED forward voltage. The DAC LSB determines the minimum output-voltage step according to the following equation:

$$V_{STEP\_MIN} = V_{DAC\_LSB} \times A_{OVP}$$

where V_{STEP_MIN} is the minimum output-voltage step, V_{DAC_LSB} is 1.95mV (typ), and A_{OVP} is the BSTMON resistor-divider gain.

Startup Sequence

The WLED section startup sequence occurs in three stages, which are described in the following sections and illustrated in Figure 3. The overall startup time can be selected using the fast_ss bit in the BL_CONFIG1 register. The boost output voltage at the end of soft-start (the end of Stage 2) differs between the slow- and fast-startup modes.

Stage 1

After the TFT sequence has been completed, the controller turns on the charge-pump for the external nMOSFET if the V5 and BATT voltages are above their respective undervoltage thresholds. The output current of the charge-pump charges the gate of the external nMOSFET, thus turning it on. After a 2ms timeout, stage 2 of the startup begins. If NGATE is unused, set the cp_dis bit in the BL_DIS register (address 0x0D) to disable the NGATE charge pump.

Stage 2

After the external MOSFET on NGATE has been enabled, the IC goes through its power-up checks, including unused

string detection, OUT_ short-to-ground detection, RT pin open/short detection, and IREF short detection. To avoid possible damage, the converter does not start if any OUT_ is detected as shorted to ground.

Any current sinks detected as unused are disabled to prevent a false fault-flag assertion during normal operation. After these checks have been performed, the converter begins to operate and the output voltage begins to ramp up. The DAC reference to the error amplifier is stepped upwards until the BSTMON pin reaches 0.48V (or 0.88V in fast-startup mode).

This stage duration is fixed at approximately 50ms (22ms in fast-startup mode).

Stage 3

The third stage begins once the second stage is complete and the DIM input goes high. During Stage 3, the output of the converter is adjusted until the minimum OUT_ voltage falls within the window comparator limits of 0.58V (typ) and 0.85V (typ). The output ramp is again controlled by the DAC, which provides the reference for the error amplifier. The DAC output is updated on each rising edge of the DIM input. If the DIM input is a 100% duty cycle (DIM = high), then the DAC output is updated once every 10ms.

The total soft-start time can be calculated using the following equation in slow-startup mode:

$$t_{SS} = 50ms + \frac{V_{LED} + 0.875 - \left(0.48 \times A_{OVP}\right)}{f_{DIM} \times 0.01 \times A_{OVP}}$$

where t_{SS} is the total soft-start time, 50ms is the fixed Stage 1 duration, V_{LED} is the total forward voltage of the LED strings, 0.715V is midpoint of the window comparator, A_{OVP} is the gain of the OVP resistor-divider, f_{DIM} is the dimming frequency (use 100Hz if the DIM input duty cycle is 100%), and 0.01V is the maximum voltage step per clock cycle of the DAC.

In fast-startup mode (with the fast_ss bit in the BL_CONFIG1 (0x0B) register set to 1), the following equation should be used:

$$t_{SS} = 22ms + \frac{0.88 \times A_{OVP} - (V_{LED} + 0.875)}{f_{DIM} \times 0.01 \times A_{OVP}}$$

Backlight Boost Startup

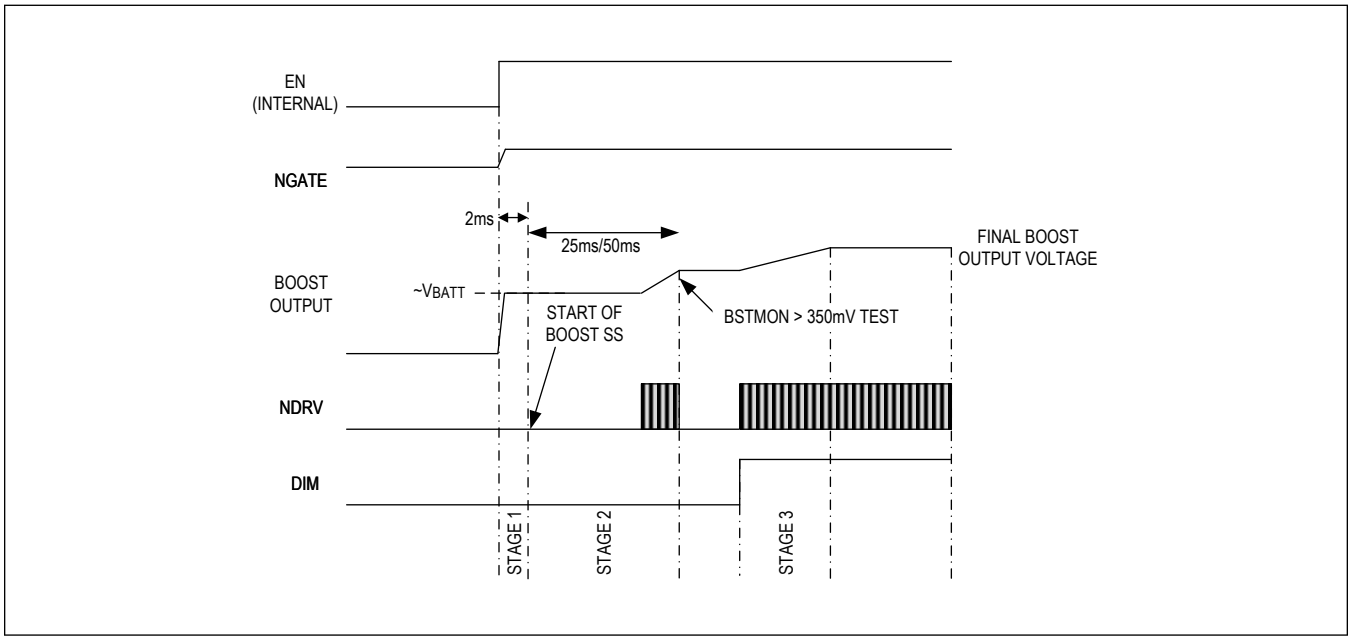


Figure 3. Backlight Boost Startup

Open-LED Management and Overvoltage Protection (OVP)

On power-up, the IC detects and disconnects any unused current-sink channels before entering the DC-DC converter soft-start. This avoids asserting the FLTB output for the unused channels. After soft-start, the IC detects open strings and disconnects them from the internal minimum OUT_ voltage detector. This keeps the DC-DC converter output voltage within safe limits and maintains high efficiency.

If any LED string is open, the voltage at the open OUT_ goes to GND. The DC-DC converter output voltage then increases to the overvoltage-protection threshold set by the voltage-divider network connected between the converter output, BSTMON input, and GND (the threshold at which the PWM controller is switched off, holding NDRV low). At that point, any current-sink output with $V_{OUT\_}$ < 250mV (typ) is disconnected from the minimum-voltage detector. Select V_{OUT_OVP} (which is the maximum voltage that the boost converter can produce) according to the following equation:

$$V_{OUT\_OVP} > 1.1 \times (V_{LED\_MAX} + 1)$$

where V_{LED_MAX} is the maximum expected LED string voltage. V_{OUT_OVP} should also be chosen such that the voltage at the OUT_ pins does not exceed the absolute maximum rating.

The upper resistor in the BSTMON resistor-divider (R17) can be selected using the following equation:

$$R17 = R16 \times (\frac{V_{OUT\_OVP}}{0.95} - 1)$$

where 0.95V is the typical BSTMON threshold. Ensure that the minimum voltage on the BSTMON pin is always greater than 0.4V to avoid the boost converter latching off due to undervoltage by checking the following:

$$(V_{LED\_MIN} + 0.55) \times \frac{R16}{R16 + R17} > 0.4V$$

where V_{LED_MIN} is the worst-case minimum LED string voltage.

When an open-LED condition occurs, FLTB is asserted low, and the bit corresponding to the channel with the fault is set to 1.

If the boost voltage reaches the BSTMON overvoltage threshold without any open channels, the converter is immediately disabled until the BSTMON voltage drops by 50mV, upon which switching resumes. In this condition, the boost converter output voltage is triangular due to the hysteretic mode of operation, and the bstov bit in the BL_DIAG register is set.

Short-LED Detection

The IC checks for shorted LEDs at the falling edge of OUT_. An LED short is detected at OUT_ if the OUT_ voltage is greater than the value programmed using the sldet[1:0] field in the BL_CONFIG2 register. Once a short is detected on any of the strings, the LED strings with the short are disconnected and the FLTB output flag asserts (unless the fault is masked) until the device detects that the shorts are removed on any of the following rising edges of DIM. Short-LED detection is disabled in low-dimming mode. If the DIM input is connected high, short-LED detection is performed continuously.

Short-LED detection is also disabled in cases where all active OUT_ channels rise above the threshold set by the sldet[1:0] bits in register BL_CONFIG2 (address 0x0C). This can occur in a boost-converter application when the input voltage becomes higher than the total LED string voltage drop, such as during a battery load dump. If a short-LED fault occurs during a load dump, the fault flag does not assert until the load dump is over and the minimum OUT_ voltage has fallen below 2.028V. If a load dump occurs after a short LED is detected, the fault flag deasserts until the load dump is over and the minimum OUT_ voltage has fallen below 2.028V, at which point the fault flag reasserts.

Dimming

Dimming can be performed using an external PWM signal applied to the DIM pin or by writing to the TON_ registers. The signal on the DIM pin is sampled with a 20MHz internal clock except when phase-shifting is disabled, in which case the DIM signal controls the OUT_ outputs directly.

Low-Dimming Mode

The IC's operation changes at very narrow dimming pulses to ensure a consistent dimming response of the LEDs. If the dimming on-time is lower than 50µs (typ), the device enters low-dimming mode. In this state, the converter switches continuously and LED short detection is disabled. When the DIM input is greater than 51µs (typ), the device goes back

into normal operation, enabling the short-LED detection and switching the power FET only when the effective dimming signal is high.

Phase-Shift Dimming

When the psen bit in register BL_CONFIG1 (address 0x0B) is set, phase shifting of the LED strings is enabled. To achieve this, the DIM signal is sampled internally by a 20MHz clock. The device automatically sets the phase shift between strings to a value depending on the number of strings enabled.

When phase shifting is enabled, the sampled DIM input is used to generate separate dimming signals for each LED string that is shifted in phase. The resolution with which the DIM signal is captured degrades at higher DIM input frequencies; therefore, dimming frequencies between 100Hz and 3kHz are recommended, although higher dimming frequencies are technically possible. The phase shift between strings is determined by the following equation:

$\Theta = 360\ n$

where n is the total number of strings being used and θ is the phase shift in degrees. See Figure 4 for a timing diagram example with phase shifting enabled.

When phase shifting is disabled, all strings turn on/off at the same time. If multiple current sinks are being connected in parallel, phase shifting should be disabled.

If a fault is detected, resulting in a string being disabled during normal operation, the phase shifting adjusts to the new situation.

When disabling unused strings, disable the higher-numbered OUT_ current sinks first.

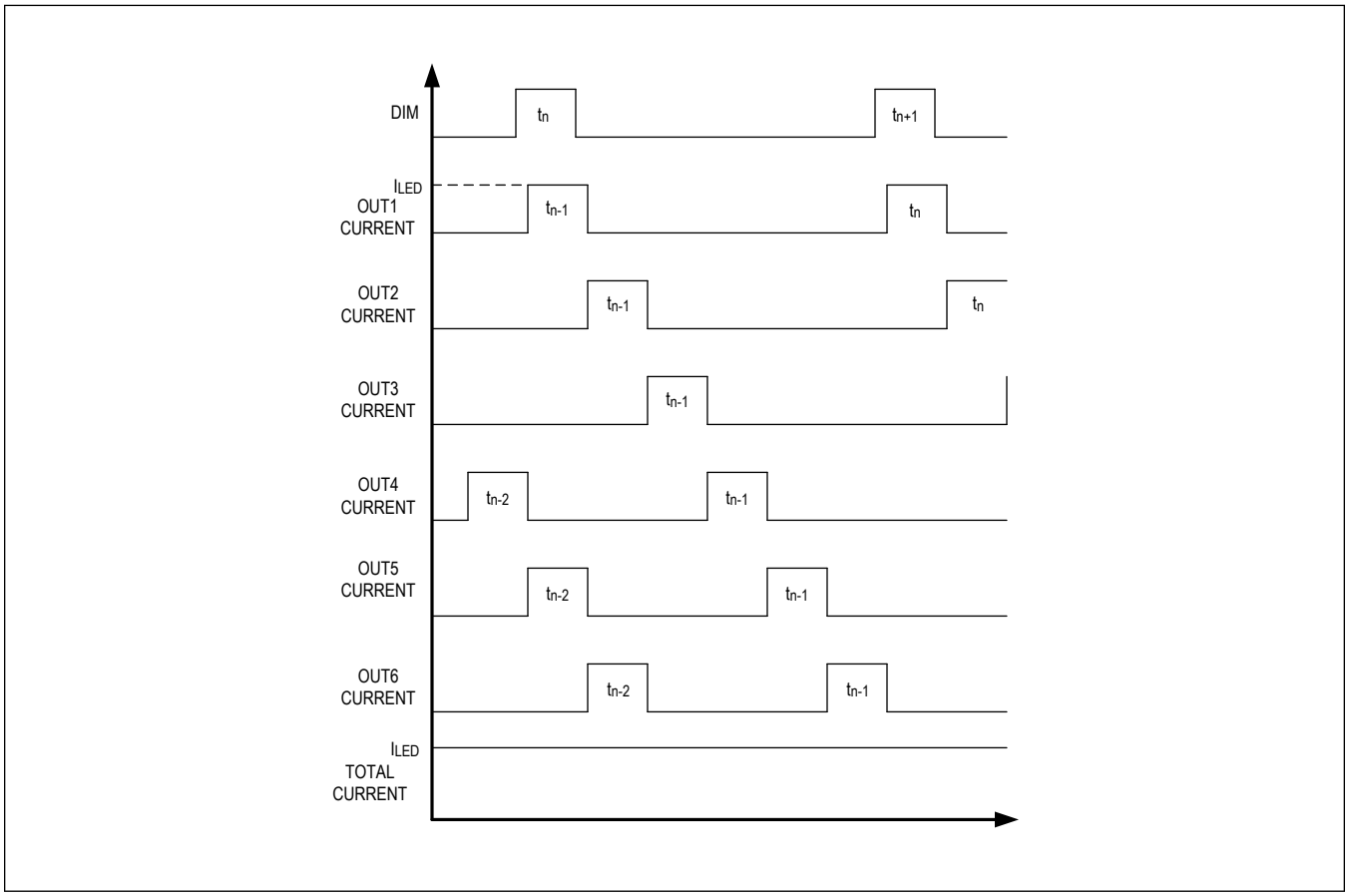


Figure 4. Phase-Shifted Outputs

Automatic Fade-In/Fade-Out During Dimming

The device can be configured to perform a smooth change in brightness, even when the DIM input duty cycle or TON_ setting is suddenly changed by setting the FADE_IN_OUT bit in the BL_FADING register to 1.

When using the fade function, it is important to maintain the DIM frequency constant while entering and leaving 100% duty cycle. This is necessary in order to avoid erroneous frequency measurement that can change the speed of the fade-in/out.

The step size in the dimming transition is either 6.25% or 12.5%, depending on the setting of the FADE_GAIN bit. The total transition time can be set by writing the TDIM field to a value between 0 to 5, where the value sets the update speed to once every 2^{TDIM}. The transition time depends on the initial and final dimming values according to:

$$t = \frac{1}{f_{DIM}} \times 2^{TDIM} \times \frac{\ln\left(DIM_F\right) - \ln\left(DIM_i\right)}{FADE\_GAIN}$$

where f_{DIM} is the dimming frequency, TDIM is the TDIM register setting, DIM_F is the final dimming setting, DIM_i is the initial dimming setting, and FADE_GAIN is either 0.0625 or 0.125. For this equation, DIM_F should be larger than DIM_i but, since the fading function is symmetrical, the values can be swapped if the final dimming ratio is lower than the initial one.

When transitioning to 100% dimming with fading enabled, do not change the input dimming from 100% until the complete fading transition to 100% is complete.

If fade-in is enabled at startup, the device will transition smoothly to the desired dimming level from 0. When the start bit is taken low or the EN pin set to ground, fade-out is not performed.

Disabling Individual Strings

To disable an unused LED string, connect the unused OUT_ to ground through a 9.1kΩ resistor, or set the corresponding DIS_ bit to 1 in the BL_DIS register (address 0x0D) before the start bit is set. During backlight boost startup, the device sources 60µA (typ) current through the OUT_ pins and measures the corresponding voltage. For the string to be properly disabled, the OUT_ voltage should measure between 270mV and 775mV during this check. The maximum threshold for the OUT_ short-to-ground check is 270mV, and the minimum unused string-detection threshold is 775mV.

Note: When disabling unused strings, start by disabling the highest numbered current sinks first (e.g., if two strings need to be disabled, disable OUT6 and the next channel down. Do not disable any two strings at random). During normal operation, strings can be selectively turned off by changing the corresponding TON_ setting to 0. This is only possible when internal dimming is used (not when using the DIM input pin).

Hybrid Dimming

To enable hybrid dimming, set the hdim bit in register BL_CONFIG1 (address 0x0B). With hybrid dimming enabled, the ADIM pin has no effect on device operation. In hybrid dimming mode, the external LEDs are dimmed by first reducing their current as the dimming duty-cycle decreases from 100% (see Figure 5). At the crossover level set by the hdim_thr[1:0] bits, dimming transitions to PWM dimming where the LED current is chopped. Depending on the dim_ext bit, the device functions in one of two ways:

- (dim_ext = 1) measures the duty cycle on the DIM pin and translates it into a combined LED current value and PWM setting.
- (dim_ext = 0) takes the 18-bit value from the TON1 register and translates it into a combined LED current value and PWM setting.

Figure 6 illustrates the difference between standard and hybrid dimming with phase-shifting enabled.

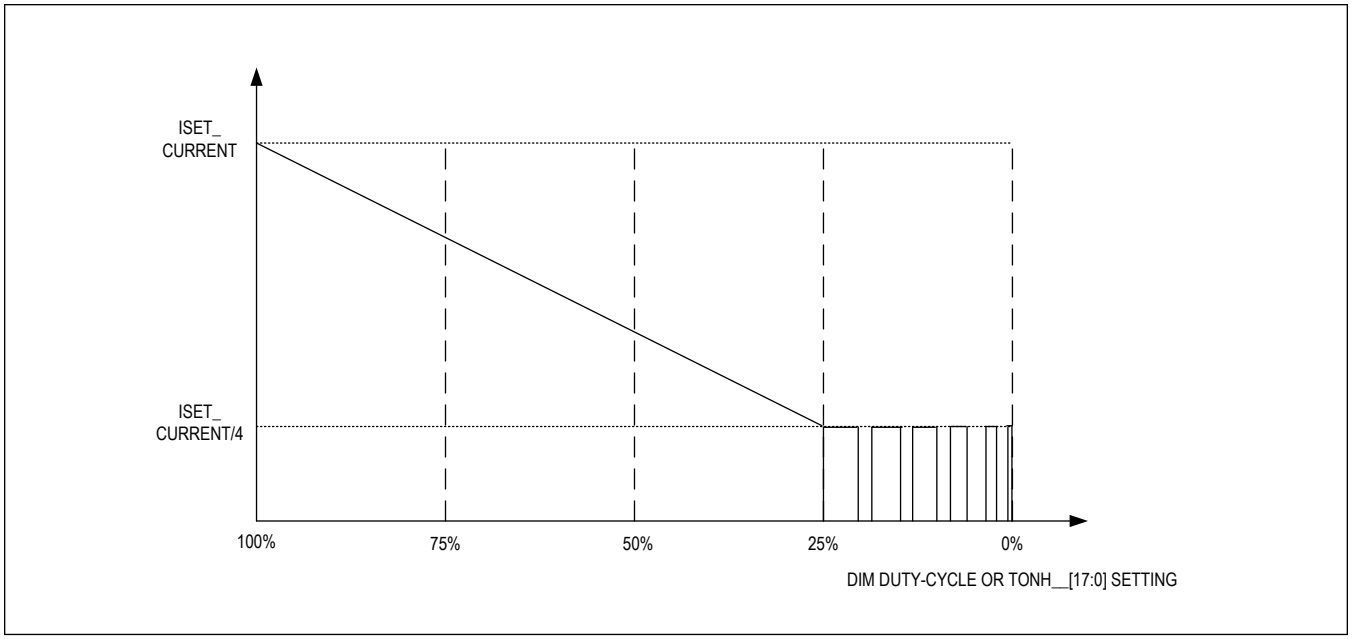


Figure 5. Hybrid Dimming Operation with hdim_thr[1:0] = 10 (25%)

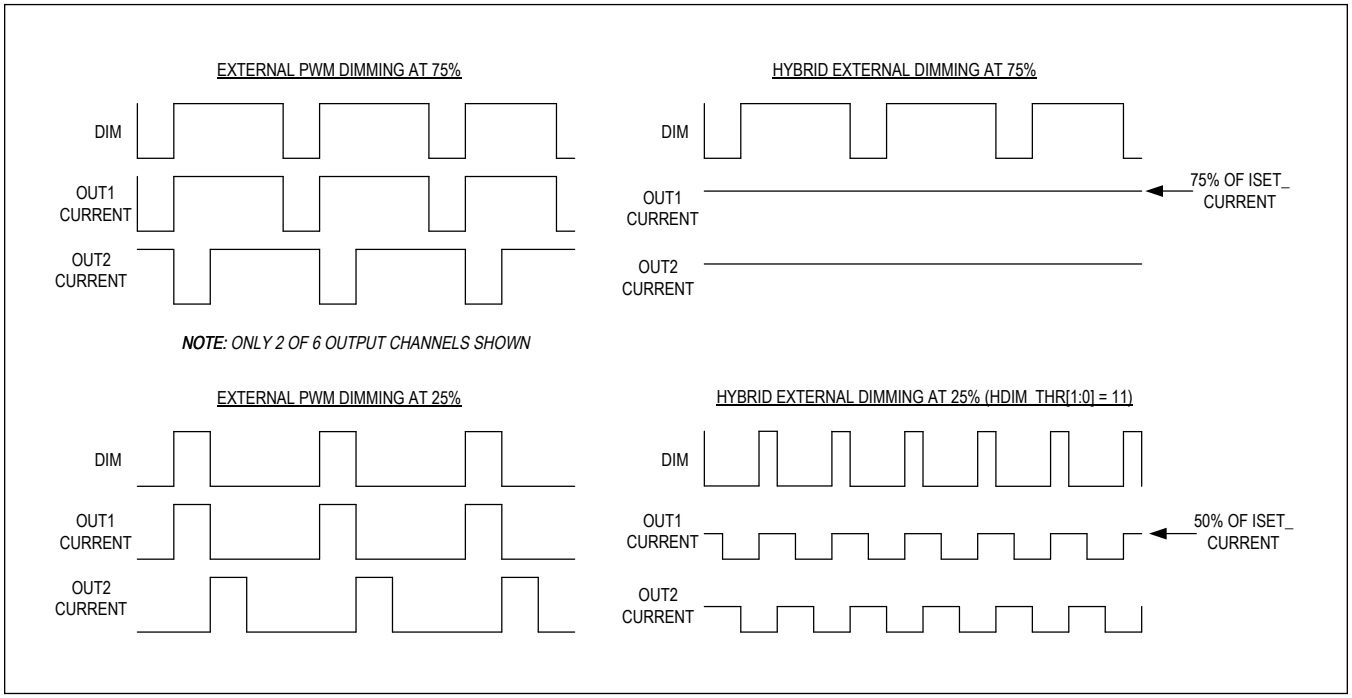


Figure 6. Hybrid Dimming Operation Modes

Temperature Foldback

When an NTC temperature sensor is connected between GND and a resistor (RT1) connected to the V18 supply, with a further resistor (RT2) connected from the junction of the NTC and RT1 to the TEMP pin, temperature foldback is implemented. When the temperature reaches the temperature T1 (set by RT1), the current in the LEDs is reduced according to the linear scheme shown in Figure 7. The slope of the current reduction is set by RT2. The MAX25169 is

specifically designed to be used with the NTCLE100E3103G or a similar NTC device. Table 3 illustrates some examples of RT1 and RT2 values to obtain certain values of T1 and T_{DELTA}.

Table 3. Temperature Foldback Examples

RT1 (kΩ)	RT2 (kΩ)	T1 (°C)	T_{DELTA} (°C)
6.04	1.2	70	30
6.04	2	70	50

When the temperature reaches T1, the OTW bit in register DIAG_REG is asserted. When the temperature reaches T_{OFF}, the LED current is turned off, the bl_ot bit is set high, and the FLTB pin asserts low.

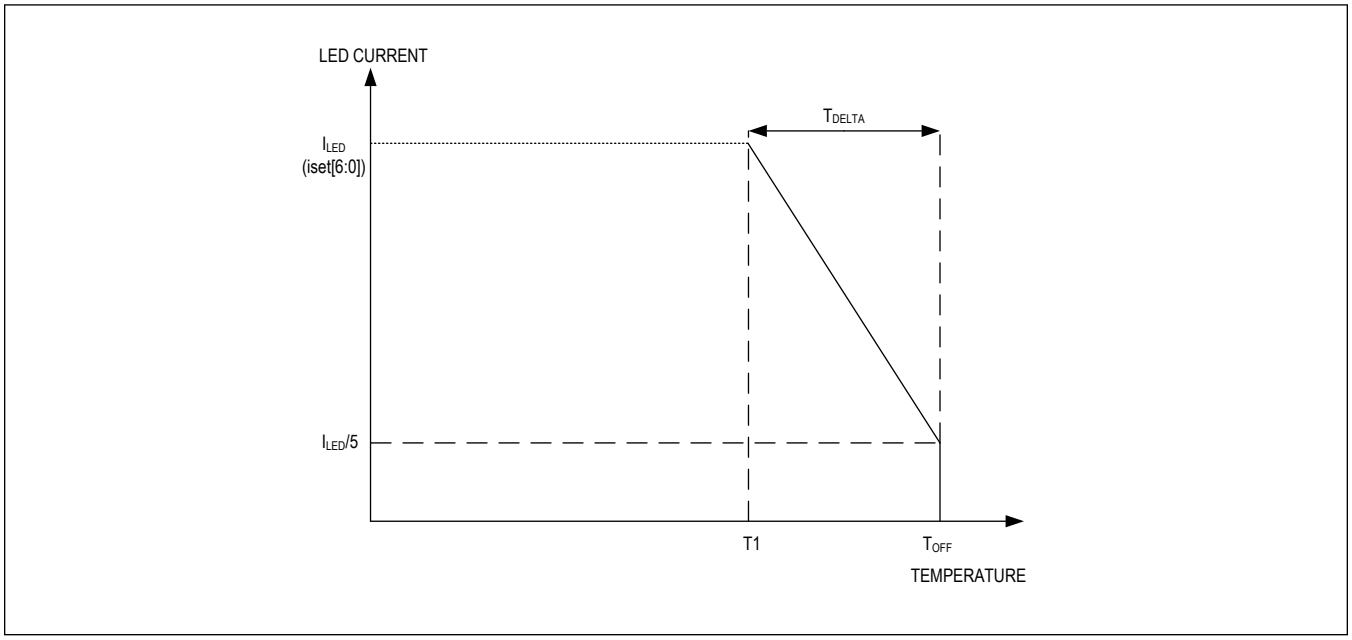


Figure 7. Temperature Foldback Curve

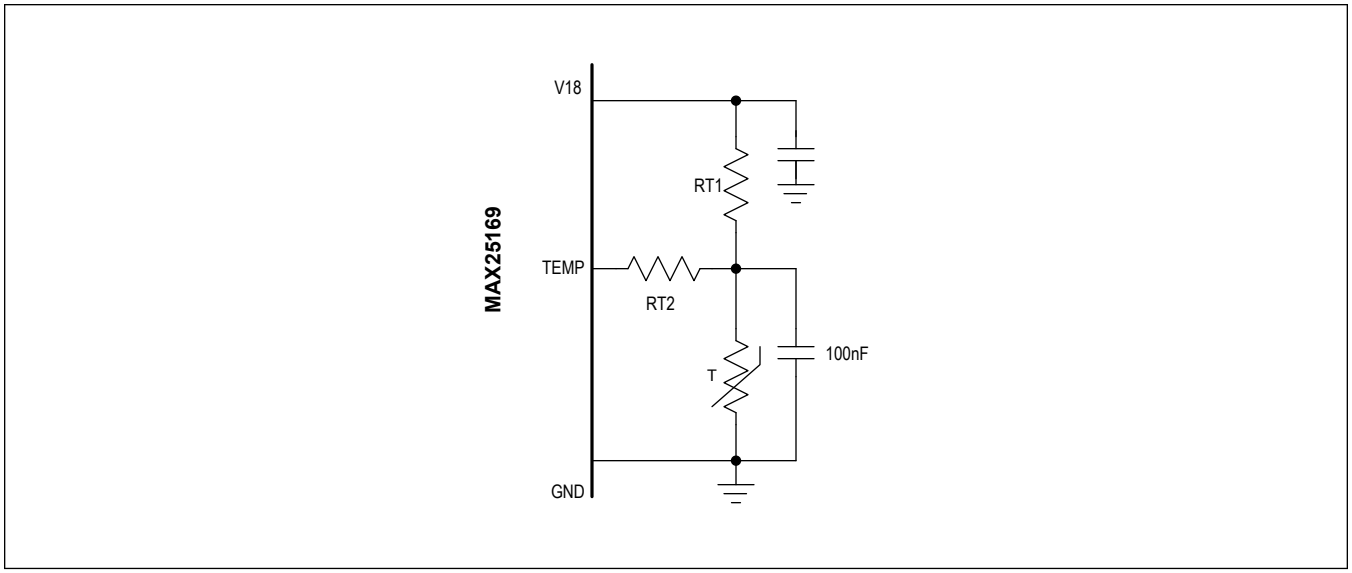


Figure 8. TEMP External Circuitry

Fault Protection

The MAX25169 has robust fault and overload protection. If any of the VG_{OFF}, NAVDD, AVDD, or VG_{ON} outputs fall to less than 85% (typ) of their intended regulation voltage for more than 15ms (typ), or if a short-circuit condition occurs on any output for any duration, then all outputs latch off and a fault condition is set. The backlight section also includes comprehensive diagnostics and fault signaling.

Both device sections (TFT and backlight) have thermal-fault detection and thermal warnings; if there is a TFT overtemperature, the complete device is disabled, while an overtemperature on the backlight section causes only that section to be disabled.

Thermal faults are cleared when the die temperature drops by 17°C.

When a fault is detected, the open-drain FLTB output goes low unless the fault is masked. The FLTB output pin is an active-low, open-drain output that is used to signal various device faults The FLTB output can flag any or all of the conditions listed as follows.

In the TFT section:

- Undervoltage fault on HVINP, AVDD, NAVDD, VGON or VGOFF
- Overvoltage fault on HVINP, AVDD, NAVDD, VGON or VGOFF
- Thermal warning in the TFT bias section
- Thermal shutdown in the TFT bias section

In the backlight section:

- Open fault on any of the OUT_ pins
- Shorted-LED fault on any of the OUT_ pins
- Any OUT_ shorted to GND
- LED boost converter undervoltage
- IREF resistor short to GND
- RT resistor out of range
- NTC fault
- V5 supply out of range
- Undervoltage on BATT
- Thermal warning in the backlight section
- Thermal shutdown in the backlight section

In addition, the following general faults are signaled:

- I2C parity error
- Undervoltage on the IN pin
- Nonvolatile memory fault
- Bandgap out of range fault based on comparison with redundant reference
- Internal oscillator failure
- V18 out-of-range

Some of the above conditions can be masked from causing FLTB to go low by using the corresponding mask bit in the TFTMASK1, TFTMASK2, and BL_MASK registers.

In standalone mode, if the fltb_mode bit is 0, the duty-cycle on the FLTB pin indicates the type of fault according to the following scheme:

- FLTB continuously low: Thermal-shutdown fault on either block, undervoltage on IN, nonvolatile memory fault, clock error, or V18 out-of-range
- 25% duty cycle on FLTB: Faults in both LED and TFT sections
- 50% duty cycle on FLTB: Fault in TFT section
- 75% duty cycle on FLTB: Fault in LED section

This list is in order of priority where FLTB continuously low takes highest precedence.

ASIL B Features

The following diagnostics are implemented in the TFT section of the device:

- OV/UV on all outputs
- Redundant reference for OV/UV comparators. If the two bandgaps are too different, undervoltage and overvoltage faults are signaled simultaneously on HVINP.

The backlight section includes these diagnostic features:

- An analog-to-digital converter (ADC) which measures the current in each of the OUT_ pins and the BSTMON voltage
- Overvoltage detection on V5 supply

The following features are common to both functional blocks:

- FLTB diagnostic to detect PCB open or stuck faults
- Monitor for internal oscillator
- I2C transactions: Optional parity check

Analog-to-Digital Converter (ADC)

The ADC is used to measure the current in each of the strings and the voltage on the BSTMON pin.

A conversion cycle is started by setting the convert bit in the CONVERT (0x01) register to 1. At the end of the cycle, the convert bit is reset to 0 to indicate a complete cycle, and the IOUT1–IOUT6 and VBSTMON registers contain the updated values. The full-scale value of the current measurement is 160mA (resolution 0.64mA) with an IREF resistor of 22kΩ. Values higher than this read as full scale or 0xFF. Current measurements are not performed on channels that are in low-dim mode; before performing a conversion, this can be checked by reading the lo_dim_ bits. If a conversion is attempted on a channel that is in low-dim mode, the current value returned will be 0x00. In the same way, any channels that are disabled, open circuit, or in the shorted-LED condition will read zero current.

The full-scale value of the BSTMON pin voltage conversion is 1V with a resolution of 3.92mV.

The duration of a complete conversion depends on whether or not phase shifting is enabled. With phase shifting enabled, a complete conversion can take up to two dimming cycles. With phase shifting disabled, one dimming cycle is the worst-case latency (the conversion is initiated at the beginning of a DIM cycle and concluded < 50µs later).

Serial Interface

The MAX25169 IC features an I2C, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the IC and the controller at clock rates up to 400kHz. The controller, typically a microcontroller, generates SCL and initiates data transfer on the bus. The operation mode of the device is controlled by the ADD and MODE pins as shown in Table 4.

Table 4. Add/Mode Pins

MODE	ADD	OPERATION MODE	FLTB
GND	GND	Full I2C read/write access	Low with fault
GND	V18	Full I2C read/write access	Low with fault
V18	GND	Standalone mode, no I2C access	PWM output with fault
V18	V18	I2C read-only access	Low with fault

If the device powers up in standalone mode, it is latched in that mode, and the mode of operation can only be changed by powering off the device.

The read and write addresses are shown in Table 5.

Table 5. I2C Address

ADD PIN CONNECTION	DEVICE ADDRESS							WRITE ADDRESS	READ ADDRESS
	A6	A5	A4	A3	A2	A1	A0		
GND	1	0	0	0	1	1	0	0x8C	0x8D
V18	1	0	0	0	1	1	1	0x8E	0x8F

A controller device communicates with the MAX25169 by transmitting the correct peripheral ID followed by the register address and data word. Each transmit sequence is framed by a START (S) or Repeated START (Sr) condition, and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The IC's SDA line operates as both an input and an open-drain output. A pull-up resistor greater than 500Ω is required on the SDA bus. In general, the resistor has to be selected as a function of bus capacitance such that the rise time on the bus is not greater than 120ns. The IC's SCL line operates as an input only. A pull-up resistor greater than 500Ω is required on SCL if there are multiple controllers on the bus, or if the controller in a single-controller system has an open-drain SCL output. In general, for the SCL-line resistor selection, the same SDA recommendations apply. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs suppress noise spikes to assure proper device operation, even on a noisy bus.

Parity Checking

Even parity checking for write transactions can be enabled by setting the par_en bit in the DELAY register to 1. The parity bit is the most significant bit (MSB) of the register address byte and should be set to attain even parity. The parity check is performed over all 3 bytes received by the device: the slave address, the register address, and the data payload. Burst-mode write is not supported when parity checking is enabled; a complete I2C transaction is needed to write to each single register. When a parity bit error is detected, the par_err bit is set, the I2C interface issues a NACK, and no write is performed.

When writing any of the BURN, REBOOT, and RESTART commands, parity must be adjusted by changing the third or payload byte; the command byte must not be changed.

Nonvolatile (NV) Memory

The MAX25169 includes six blocks of one-time-programmable memory (the number of writes performed so far can be read from nv_count[2:0] in the REG_CTRL register). The user can store the block of volatile registers from 0x07 to 0x15 in nonvolatile memory, which is in turn mapped to register locations 0x17 to 0x25. Note that before the nonvolatile memory has been written to the first time, a read from the locations 0x17 to 0x25 yields the result 0xFF.

The contents of the nonvolatile memory are protected by a single-error correction/double-error detection (SECDED) redundant code, while data transfer from nonvolatile memory to registers 0x07 to 0x15 is protected by a parity check. If the parity check fails, a retry is performed two times. If all three attempts are unsuccessful, the device does not start up, the nv_flt bit is set, and the FLTB pin is asserted low. If the SECDED check fails, the device does not start up, the nv_flt bit is set, and the FLTB pin is asserted low.

If there are no errors, the outputs are turned on with the stored values and in the stored sequence.

To store the contents of registers 0x07 to 0x15 to nonvolatile memory a voltage source of 8.5V ±2% capable of supplying

more than 25mA should be connected to the V_{PROG} pin. When the V_{PROG} voltage is stable, an I2C NV write command can be performed by writing to the burn_otp_reg register. If the NV write is unsuccessful (because the V_{PROG} voltage was out of range or because of a general memory error), the nv_flt bit is set and the FLTB pin goes low. After an NV write command is executed, the nv_flt bit should be checked. If nv_flt is high, another NV write can be attempted.

Connect V_{PROG} to GND if there is no need to program the nonvolatile memory.

Autorefresh Function

When the refresh bit in register CONFIG is set, the device reads from the nonvolatile registers at intervals of 1s and writes the data into the corresponding volatile registers. This avoids the effect of possible corruption of the volatile registers. Autorefresh reads are subject to error correction in the same way as the initial read after device power-up.

See the *Using the NV Memory* section when programming the nonvolatile memory.

BURN, REBOOT, and RESTART Commands

The BURN and REBOOT commands are used to store the contents of registers 0x07 to 0x15 in nonvolatile memory or to fetch the contents of nonvolatile memory and load them into registers 0x07 to 0x15, respectively. The RESTART command is used to restart the device from a latched-fault mode. When a RESTART command is performed, all fault bits are cleared.

A BURN command is performed by writing 0xA5 to register address 0x78 (burn_otp_reg).

A REBOOT command is performed by writing 0x5A to register address 0x79 (reboot_otp_reg).

A RESTART command is performed by writing 0xC3 to register address 0x7A (soft_restart).

When parity checking is enabled and one of these user commands is sent to the device, the third byte should be such as to have even parity over the 3 bytes sent.

Register Map

MAX25169

ADDRESS	NAME	MSB							LSB
USER REGISTERS									
0x00	DEVICE[7:0]	–	–	dev_id[5:0]					
0x01	CONVERT[7:0]	convert	–	–	–	–	–	–	–
0x02	REG_CTRL[7:0]	–	dis_refr	nv_count[2:0]			rev_id[2:0]		
0x03	TFTMASK1[7:0]	hvinp_ov_mask	avdd_uv_mask	navdd_ov_mask	navdd_uv_mask	vgon_ov_mask	vgon_uv_mask	vgoff_ov_mask	vgoff_uv_mask
0x04	TFTMASK2[7:0]	flt_flt	par_err_mask	vin_uvlo_mask	hvinp_uv_mask	–	–	clk_err_mask	th_warn_mask
0x05	TFT_FAULT1[7:0]	hvinp_ov	avdd_uv	navdd_ov	navdd_uv	vgon_ov	vgon_uv	vgoff_ov	vgoff_uv
0x06	TFT_FAULT2[7:0]	v18oor	par_err	vin_uvlo	hvinp_uv	th_shdn	nv_flt	clk_err	th_warn
0x07	TFT_CONFIG[7:0]	dis_navdd	refresh	en_ss	fSW	tretry[1:0]		tfault[1:0]	
0x08	DELAY[7:0]	delayt1[1:0]		delayt2[1:0]		delayt3[1:0]		–	par_en
0x09	SEQ[7:0]	seq_set[2:0]			pfo_th	tstart[1:0]		lxp_lim_low	start
0x0A	ISET[7:0]	–	iset[6:0]						
0x0B	BL_CONFIG1[7:0]	dim_ext	hdim	hdim_thr[1:0]		bstforce	fast_ss	psen	fltb_mode
0x0C	BL_CONFIG2[7:0]	bl_ilim	fpwm[2:0]			bl_ss_off	bl_ssl	sldet[1:0]	
0x0D	BL_DIS[7:0]	cp_dis	–	dis_bl	dis6	dis5	dis4	dis3	dis2
0x0E	BL_FADING[7:0]	–	–	–	fade_gain	fade_in_out	tfade[2:0]		
0x0F	CUSTOMER_USE1[7:0]	customer_use1[7:0]							
0x10	CUSTOMER_USE2[7:0]	customer_use2[7:0]							
0x11	CUSTOMER_USE3[7:0]	customer_use3[7:0]							
0x12	CUSTOMER_USE4[7:0]	customer_use4[7:0]							
0x13	AVDD_SET[7:0]	–	–	avdd[5:0]					
0x14	VGON[7:0]	–	–	vgon[5:0]					
0x15	VGOFF[7:0]	–	–	vgoff[5:0]					
0x17	NV_CONFIG[7:0]	nv_dis_navdd	nv_refresh	nv_en_ss	nv_fSW	nv_tretry[1:0]		nv_tfault[1:0]	
0x18	NV_DELAY[7:0]	nv_delayt1[1:0]		nv_delayt2[1:0]		nv_delayt3[1:0]		unused	nv_par_en
0x19	NV_SEQ[7:0]	nv_seq_set[2:0]			nv_pfo_th	nv_tstart[1:0]		nv_lxp_lim_low	nv_start
0x1A	NV_ISET[7:0]	unused	nv_iset[6:0]						
0x1B	NV_BL_CONFIG1[7:0]	nv_dim_ext	nv_hdim	nv_hdim_thr[1:0]		nv_bstforce	nv_fast_ss	nv_psen	nv_fltb_mode
0x1C	NV_BL_CONFIG2[7:0]	nv_bl_ilim	nv_fpwm[2:0]			nv_bl_ss_off	nv_bl_ssl	nv_sldet[1:0]	

ADDRESS	NAME	MSB							LSB
0x1D	NV_BL_DIS[7:0]	nv_cp_dis	unused	nv_dis_bl	nv_dis6	nv_dis5	nv_dis4	nv_dis3	nv_dis2
0x1E	NV_BL_FADING[7:0]	unused[2:0]			nv_fade_gain	nv_fade_in_out	nv_tfade[2:0]		
0x1F	NV_CUSTOMER_USE1[7:0]	nv_customer_use1[7:0]							
0x20	NV_CUSTOMER_USE2[7:0]	nv_customer_use2[7:0]							
0x21	NV_CUSTOMER_USE3[7:0]	nv_customer_use3[7:0]							
0x22	NV_CUSTOMER_USE4[7:0]	nv_customer_use4[7:0]							
0x23	NV_AVDD_SET[7:0]	unused[1:0]		nv_avdd[5:0]					
0x24	NV_VGON[7:0]	unused[1:0]		nv_vgon[5:0]					
0x25	NV_VGOFF[7:0]	unused[1:0]		nv_vgoff[5:0]					
0x26	AVDD_LIM[7:0]	–	–	avdd_lim[5:0]					
0x27	LO_DIM[7:0]	ton_master	–	lo_dim6	lo_dim5	lo_dim4	lo_dim3	lo_dim2	lo_dim1
0x28	TON1H[7:0]	ton1h[7:0]							
0x29	TON1L[7:0]	ton1l[7:0]							
0x2A	TON2H[7:0]	ton2h[7:0]							
0x2B	TON2L[7:0]	ton2l[7:0]							
0x2C	TON3H[7:0]	ton3h[7:0]							
0x2D	TON3L[7:0]	ton3l[7:0]							
0x2E	TON1_3LSB[7:0]	–	–	ton3lsb[1:0]		ton2lsb[1:0]		ton1lsb[1:0]	
0x2F	TON4H[7:0]	ton4h[7:0]							
0x30	TON4L[7:0]	ton4l[7:0]							
0x31	TON5H[7:0]	ton5h[7:0]							
0x32	TON5L[7:0]	ton5l[7:0]							
0x33	TON6H[7:0]	ton6h[7:0]							
0x34	TON6L[7:0]	ton6l[7:0]							
0x35	TON4_6LSB[7:0]	–	–	ton6lsb[1:0]		ton5lsb[1:0]		ton4lsb[1:0]	
0x36	OPEN_REG[7:0]	–	–	out6o	out5o	out4o	out3o	out2o	out1o
0x37	SHORTGND_REG[7:0]	–	–	out6sg	out5sg	out4sg	out3sg	out2sg	out1sg
0x38	SHORTED_LED_REG[7:0]	–	–	out6sl	out5sl	out4sl	out3sl	out2sl	out1sl
0x39	BL_MASK[7:0]	–	battuv	battuvmask	bstuvmask	omask	sgmask	bl_otwmask	slmask
0x3A	BL_DIAG[7:0]	v5oor	rtoor	irefoor	bstuv	bstov	hw_rst	bl_otw	bl_ot
0x3B	VBSTMON[7:0]	vbstmon[7:0]							
0x3C	IOUT1[7:0]	iout1[7:0]							
0x3D	IOUT2[7:0]	iout2[7:0]							
0x3E	IOUT3[7:0]	iout3[7:0]							
0x3F	IOUT4[7:0]	iout4[7:0]							
0x40	IOUT5[7:0]	iout5[7:0]							

ADDRESS	NAME	MSB							LSB
0x41	IOUT6[7:0]	iout6[7:0]							
USER COMMANDS									
0x78	burn_otp_reg[7:0]	burn_otp[7:0]							
0x79	reboot_otp_reg[7:0]	reboot_otp[7:0]							
0x7A	soft_restart[7:0]	soft_restart[7:0]							

Register Details

DEVICE (0x00)

BIT	7	6	5	4	3	2	1	0
Field	–	–	dev_id[5:0]					
Reset	–	–						
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
dev_id	5:0	Device ID, reads 0x39.

CONVERT (0x01)

BIT	7	6	5	4	3	2	1	0
Field	convert	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
convert	7	Write a 1 to this bit to start a conversion cycle of the ADC. When the cycle is finished, this bit is automatically reset to indicate that data is ready.

REG_CTRL (0x02)

BIT	7	6	5	4	3	2	1	0
Field	–	dis_refr	nv_count[2:0]			rev_id[2:0]		
Reset	–	0b0				0x0		
Access Type	–	Write, Read	Read Only			Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
dis_refr	6	Refresh disable bit. Use this bit to temporarily disable refresh before a burn_otp command.	0x0: Refresh bit determines whether refresh is on or off 0x1: Refresh disabled
nv_count	5:3	This field indicates the total number of writes to nonvolatile memory. The maximum value is 6.	
rev_id	2:0	Revision ID. Reads 0x0.	

TFTMASK1 (0x03)

BIT	7	6	5	4	3	2	1	0
Field	hvinp_ov_mask	avdd_uv_mask	navdd_ov_mask	navdd_uv_mask	vgon_ov_mask	vgon_uv_mask	vgoff_ov_mask	vgoff_uv_mask
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
hvinp_ov_mask	7	When 1, this bit prevents an overvoltage on AVDD from asserting FLTB low.
avdd_uv_mask	6	When 1, this bit prevents an undervoltage on AVDD from asserting FLTB low.
navdd_ov_mask	5	When 1, this bit prevents an overvoltage on NAVDD from asserting FLTB low.
navdd_uv_mask	4	When 1, this bit prevents an undervoltage on NAVDD from asserting FLTB low.
vgon_ov_mask	3	When 1, this bit prevents an overvoltage on VG_{ON} from asserting FLTB low.
vgon_uv_mask	2	When 1, this bit prevents an undervoltage on VG_{ON} from asserting FLTB low.
vgoff_ov_mask	1	When 1, this bit prevents an overvoltage on VG_{OFF} from asserting FLTB low.
vgoff_uv_mask	0	When 1, this bit prevents an undervoltage on VG_{OFF} from asserting FLTB low.

TFTMASK2 (0x04)

BIT	7	6	5	4	3	2	1	0
Field	flt_flt	par_err_mask	vin_uvlo_mask	hvinp_uv_mask	–	–	clk_err_mask	th_warn_mask
Reset	0x0	0x0	0x0	0x0	–	–	0x0	0x1
Access Type	Read Only	Write, Read	Write, Read	Write, Read	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
flt_flt	7	When 1, this bit indicates that the FLTB pin is stuck high or low.
par_err_mask	6	When 1, prevents parity errors from asserting the FLTB pin.
vin_uvlo_mask	5	When 1, this bit prevents an undervoltage on IN from asserting the FLTB pin.
hvinp_uv_mask	4	Mask bit for hvinp_uv diagnostic. When 1, an undervoltage on HVINP does not cause FLTB to assert.
clk_err_mask	1	When 1, this bit prevents a clk_err fault from asserting FLTB low.
th_warn_mask	0	When 1, this bit prevents an overtemperature warning from asserting FLTB low.

TFT_FAULT1 (0x05)

BIT	7	6	5	4	3	2	1	0
Field	hvinp_ov	avdd_uv	navdd_ov	navdd_uv	vgon_ov	vgon_uv	vgoff_ov	vgoff_uv
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
hvinp_ov	7	When 1, this bit indicates an overvoltage on AVDD.

BITFIELD	BITS	DESCRIPTION
avdd_uv	6	When 1, this bit indicates an undervoltage on AVDD.
navdd_ov	5	When 1, this bit indicates an overvoltage on NAVDD.
navdd_uv	4	When 1, this bit indicates an undervoltage on NAVDD.
vgon_ov	3	When 1, this bit indicates an overvoltage on VG_{ON}.
vgon_uv	2	When 1, this bit indicates an undervoltage on VG_{ON}.
vgoff_ov	1	When 1, this bit indicates an overvoltage on VG_{OFF}.
vgoff_uv	0	When 1, this bit indicates an undervoltage on VG_{OFF}.

TFT_FAULT2 (0x06)

BIT	7	6	5	4	3	2	1	0
Field	v18oor	par_err	vin_uvlo	hvinp_uv	th_shdn	nv_flt	clk_err	th_warn
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Only	Read Clears All

BITFIELD	BITS	DESCRIPTION
v18oor	7	Indicates that the 1.8V output is out of range, either above its overvoltage level or below its undervoltage level.
par_err	6	Indicates that a parity error was detected on an I2C transaction.
vin_uvlo	5	Indicates an undervoltage condition on the IN pin. When this happens, the device turns off all outputs and waits for IN to return above the IN UVLO level, after which the outputs are reenabled in the programmed sequence.
hvinp_uv	4	When 1, this bit indicates an undervoltage on the boost output, HVINP.
th_shdn	3	When 1, this bit indicates an overtemperature shutdown on the TFT section and that the complete device has been turned off.
nv_flt	2	Nonvolatile memory failure – unsuccessful transfer of the contents of NV memory to working memory or more than one error detected.
clk_err	1	When this bit is 1, the clock for either the TFT or the backlight section has been inactive for 5µs or is out of range. Unless this fault is masked, the FLTB pin asserts low and the local microcontroller should disable the device using the EN pin. This fault can only be cleared by power-on reset (POR).
th_warn	0	When 1, this bit indicates a thermal warning.

TFT_CONFIG (0x07)

BIT	7	6	5	4	3	2	1	0
Field	dis_navdd	refresh	en_ss	fSW	tretry[1:0]		tfault[1:0]	
Reset	0x0	0x0	0x0	0x0	0x1		0x0	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
dis_navdd	7	When set to 1, this bit disables the NAVDD converter. Set this bit before enabling the device using the start bit. The dis_navdd bit should not be changed during device operation.	

BITFIELD	BITS	DESCRIPTION	DECODE
refresh	6	When this bit is 1, the contents of the NV registers are automatically copied to the volatile registers every second.	0x0: Refresh disabled 0x1: Refresh enabled
en_ss	5	Enable spread-spectrum by setting this bit to 1.	
fSW	4	Sets switching frequency of TFT section.	0x0: 2.1MHz 0x1: 420kHz
tretry	3:2	Sets retry time after a fault.	0x0: Retry disabled 0x1: Retry after 0.95s, total 3 retries 0x2: Retry after 1.9s, total 3 retries 0x3: Retry after 1.9s
tfault	1:0	Sets fault delay time.	0x0: 15ms 0x1: 30ms 0x2: 60ms 0x3: 90ms

DELAY (0x08)

BIT	7	6	5	4	3	2	1	0
Field	delayt1[1:0]		delayt2[1:0]		delayt3[1:0]		–	par_en
Reset	0x2		0x2		0x2		–	0x0
Access Type	Write, Read		Write, Read		Write, Read		–	Write, Read

BITFIELD	BITS	DESCRIPTION
delayt1	7:6	Set delay t1 in the start-up sequence. Choose between 0, 5ms, 10ms, and 15ms.
delayt2	5:4	Set delay t2 in the start-up sequence. Choose between 0, 5ms, 10ms, and 15ms.
delayt3	3:2	Set delay t3 in the start-up sequence. Choose between 0, 5ms, 10ms, and 15ms.
par_en	0	Parity enable bit. When 1, this bit enables parity checking on write transactions to the device.

SEQ (0x09)

BIT	7	6	5	4	3	2	1	0
Field	seq_set[2:0]			pfo_th	tstart[1:0]		lxp_lim_low	start
Reset	0x2			0x0	0x1		0b0	0x0
Access Type	Write, Read			Write, Read	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
seq_set	7:5	Sequence selection bits.	0x0: Sequence 1 0x1: Sequence 2 0x2: Sequence 3 0x3: Sequence 4 0x4: Sequence 5 0x5: Sequence 6 0x6: Sequence 7 0x7: Sequence 8

BITFIELD	BITS	DESCRIPTION	DECODE
pfo_th	4	This bit sets the nominal falling threhsold for the PFO output.	0x0: 2.5V 0x1: 2.4V
tstart	3:2	This field sets the start-up time for VG_{ON} and VG_{OFF} between 1ms and 8ms. The AVDD startup is accordingly set to 0.5ms, 1ms, 2ms, or 4ms.	0x0: 1ms 0x1: 2ms 0x2: 4ms 0x3: 8ms
lxp_lim_low	1	When 1, the HVINP boost converter current limit is reduced.	
start	0	When this bit is set to 1, the device outputs are turned on in the sequence programmed by the seq_set bits in the SEQ register.	

ISET (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	–	iset[6:0]						
Reset	–							
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
iset	6:0	The value in this register sets the OUT_ LED current in the 23mA to 150mA range.	0x0: 23mA 0x1: 24mA ...: ... 0xB: 34mA 0xC: 35mA ...: ... 0x7D: 148mA 0x7E: 149mA 0x7F: 150mA

BL_CONFIG1 (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	dim_ext	hdim	hdim_thr[1:0]		bstforce	fast_ss	psen	fltb_mode
Reset	0x1	0x0	0x00		0x0	0x0	0x1	0x0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
dim_ext	7	When 1, dimming through the DIM pin is enabled. When 0, dimming is controlled using the TON__ registers.	
hdim	6	When 1, hybrid dimming is enabled.	
hdim_thr	5:4	Set hybrid-dimming threshold. Default value is 6.25% (00).	0x00: 6.25% 0x01: 12.5% 0x10: 25% 0x11: 50%
bstforce	3	When 1, this bit forces the boost converter to run continuously, independently of the dimming signal.	

BITFIELD	BITS	DESCRIPTION	DECODE
fast_ss	2	Selects slow or fast boost soft-start. Set to 1 for fast soft-start.	
psen	1	When 0, phase shifting is disabled. When 1, phase shifting is enabled.	
fltb_mode	0	This bit sets the mode of operation of the FLTB pin in standalone mode. When 0, the FLTB outputs a PWM signal to indicate the type of fault. When 1, FLTB is low when a fault is detected.	

BL_CONFIG2 (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	bl_ilim	fpwm[2:0]			bl_ss_off	bl_ssl	sldet[1:0]	
Reset	0x1	0x001			0x0	0x0	0x00	
Access Type	Write, Read	Write, Read			Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
bl_ilim	7	Sets boost current limit to one of two levels. When 1, the lower current limit is selected.	
fpwm	6:4	These bits set the PWM frequency in internal PWM mode.	0x0: 153Hz 0x1: 203Hz 0x2: 305Hz 0x3: 610Hz 0x4: 980Hz 0x5: 1220Hz 0x6: 1401Hz 0x7: 1634Hz
bl_ss_off	3	When 1, spread-spectrum switching is disabled.	
bl_ssl	2	When spread spectrum is enabled, the bl_ssl bit chooses the amount of spread: When 0, the spread is nominally ±6%; when 1, the spread is ±3%. When changing the percentage, first disable spread spectrum using the SS_OFF bit, then change the value of SSL, and finally reenable spread spectrum using SS_OFF.	
sldet	1:0	Shorted-LED threshold settings.	0x0: Disabled 0x1: 3V 0x2: 6V 0x3: 8V

BL_DIS (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	cp_dis	–	dis_bl	dis6	dis5	dis4	dis3	dis2
Reset	0x0	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
cp_dis	7	When 1, this bit disables the internal charge pump which drives the NGATE pin. Set to 1 when an external series switch is not used. Setting CP_DIS to 0 during operation will cause complete shutdown of the device and is not recommended.
dis_bl	5	Disable bit for backlight section.
dis6	4	Set this bit to 1 to disable OUT6. This must be done before ENA is written to 1.
dis5	3	Set this bit to 1 to disable OUT5. This must be done before ENA is written to 1.
dis4	2	Set this bit to 1 to disable OUT4. This must be done before ENA is written to 1.
dis3	1	Set this bit to 1 to disable OUT3. This must be done before ENA is written to 1.
dis2	0	Set this bit to 1 to disable OUT2. This must be done before ENA is written to 1.

BL_FADING (0x0E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	fade_gain	fade_in_out	tfade[2:0]		
Reset	–	–	–	0b0	0b0	0x0		
Access Type	–	–	–	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
fade_gain	4	When this bit is set to 1, the fade-in-out function has a gain of 12.5%, otherwise 6.25%.	
fade_in_out	3	When this bit is set to 1, the fade-in-out function for the LED dimming is enabled.	
tfade	2:0	Sets the fading update time interval according to 2^{TDIM}. TDIM can be between 0 and 5. When set to 0, fading is updated on every dimming cycle.	0x1: 2 0x2: 4 0x3: 8 0x4: 16 0x5: 32 0x6: N/A 0x7: N/A

CUSTOMER_USE1 (0x0F)

Register which can be used to store user data that can also be stored in nonvolatile memory.

BIT	7	6	5	4	3	2	1	0
Field	customer_use1[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
customer_use1	7:0	

CUSTOMER_USE2 (0x10)

Register which can be used to store user data that can also be stored in nonvolatile memory.

BIT	7	6	5	4	3	2	1	0
Field	customer_use2[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
customer_use2	7:0	

CUSTOMER_USE3 (0x11)

Register which can be used to store user data that can also be stored in nonvolatile memory.

BIT	7	6	5	4	3	2	1	0
Field	customer_use3[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
customer_use3	7:0	

CUSTOMER_USE4 (0x12)

Register which can be used to store user data that can also be stored in nonvolatile memory.

BIT	7	6	5	4	3	2	1	0
Field	customer_use4[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
customer_use4	7:0	

AVDD_SET (0x13)

BIT	7	6	5	4	3	2	1	0
Field	–	–	avdd[5:0]					
Reset	–	–	0x1A					
Access Type	–	–	Write, Read					

<table>
<tr><th>BITFIELD</th><th>BITS</th><th>DESCRIPTION</th></tr>
<tr><td>avdd</td><td>5:0</td><td>Sets AVDD and NAVDD voltages. When NAVDD is disabled using the dis_navdd bit, the voltage values represented by the avdd bits change.
<table>
<tr><th>Value</th><th>dis_navdd = 1</th><th>dis_navdd = 0</th></tr>
<tr><td>0x0</td><td>11.7</td><td>N/A</td></tr>
<tr><td>0x1</td><td>11.8</td><td>N/A</td></tr>
<tr><td>0x2</td><td>11.9</td><td>N/A</td></tr>
<tr><td>0x3</td><td>12</td><td>N/A</td></tr>
<tr><td>0x4</td><td>12.1</td><td>N/A</td></tr>
<tr><td>0x5</td><td>12.2</td><td>N/A</td></tr>
<tr><td>0x6</td><td>12.3</td><td>N/A</td></tr>
<tr><td>0x7</td><td>12.4</td><td>4.9</td></tr>
<tr><td>0x8</td><td>12.5</td><td>5</td></tr>
<tr><td>0x9</td><td>12.6</td><td>5.1</td></tr>
<tr><td>0xA</td><td>12.7</td><td>5.2</td></tr>
<tr><td>0xB</td><td>12.8</td><td>5.3</td></tr>
<tr><td>0xC</td><td>12.9</td><td>5.4</td></tr>
<tr><td>0xD</td><td>13</td><td>5.5</td></tr>
<tr><td>0xE</td><td>13.1</td><td>5.6</td></tr>
<tr><td>0xF</td><td>13.2</td><td>5.7</td></tr>
<tr><td>0x10</td><td>13.3</td><td>5.8</td></tr>
<tr><td>0x11</td><td>13.4</td><td>5.9</td></tr>
<tr><td>0x12</td><td>13.5</td><td>6</td></tr>
<tr><td>0x13</td><td>13.6</td><td>6.1</td></tr>
<tr><td>0x14</td><td>13.7</td><td>6.2</td></tr>
<tr><td>0x15</td><td>13.8</td><td>6.3</td></tr>
<tr><td>0x16</td><td>13.9</td><td>6.4</td></tr>
<tr><td>0x17</td><td>14</td><td>6.5</td></tr>
<tr><td>0x18</td><td>14.1</td><td>6.6</td></tr>
<tr><td>0x19</td><td>14.2</td><td>6.7</td></tr>
<tr><td>0x1A</td><td>14.3</td><td>6.8</td></tr>
<tr><td>0x1B</td><td>14.4</td><td>6.9</td></tr>
<tr><td>0x1C</td><td>14.5</td><td>7V</td></tr>
<tr><td>0x1D</td><td>14.6</td><td>7.1</td></tr>
<tr><td>0x1E</td><td>14.7</td><td>7.2</td></tr>
<tr><td>0x1F</td><td>14.8</td><td>7.3</td></tr>
<tr><td>0x20</td><td>14.9</td><td>7.4</td></tr>
<tr><td>0x21</td><td>15</td><td>7.5</td></tr>
<tr><td>0x22</td><td>15.1</td><td>7.6</td></tr>
<tr><td>0x23</td><td>15.2</td><td>7.7</td></tr>
<tr><td>0x24</td><td>15.3</td><td>7.8</td></tr>
<tr><td>0x25</td><td>15.4</td><td>7.9</td></tr>
<tr><td>0x26</td><td>15.5</td><td>8</td></tr>
</table>
</td></tr>
</table>

BITFIELD	BITS	DESCRIPTION		
		0x27	15.6	8.1
		0x28	15.7	8.2
		0x29	15.8	8.3
		0x2A	15.9	8.4
		0x2B	16	8.5
		0x2C	16.1	8.6
		0x2D	16.2	8.7
		0x2E	16.3	8.8
		0x2F	16.4	8.9
		0x30	16.5	9
		0x31	16.6	9.1
		0x32	16.7	9.2
		0x33	16.8	9.3
		0x34	16.9	9.4
		0x35	17	9.5
		0x36	17.1	9.6
		0x37	17.2	9.7
		0x38	17.3	9.8
		0x39	17.4	9.9
		0x3A	17.5	10
		0x3B	17.6	10.1
		0x3C	17.7	10.2
		0x3D	17.8	10.3
		0x3E	17.9	10.4
		0x3F	18	10.5

VGON (0x14)

BIT	7	6	5	4	3	2	1	0
Field	–	–	vgon[5:0]					
Reset	–	–	0x16					
Access Type	–	–	Write, Read					

<table>
<tr><th>BITFIELD</th><th>BITS</th><th>DESCRIPTION</th></tr>
<tr><td>vgon</td><td>5:0</td><td>Sets VG_{ON} voltage.
<table>
<tr><th>Value</th><th>dis_navdd = 0</th><th>dis_navdd = 1</th></tr>
<tr><td>0x0</td><td>8.4</td><td>12.6</td></tr>
<tr><td>0x1</td><td>8.6</td><td>12.9</td></tr>
<tr><td>0x2</td><td>8.8</td><td>13.2</td></tr>
<tr><td>0x3</td><td>9</td><td>13.5</td></tr>
<tr><td>0x4</td><td>9.2</td><td>13.8</td></tr>
<tr><td>0x5</td><td>9.4</td><td>14.1</td></tr>
<tr><td>0x6</td><td>9.6</td><td>14.4</td></tr>
<tr><td>0x7</td><td>9.8</td><td>14.7</td></tr>
<tr><td>0x8</td><td>10</td><td>15</td></tr>
<tr><td>0x9</td><td>10.2</td><td>15.3</td></tr>
<tr><td>0xA</td><td>10.4</td><td>15.6</td></tr>
<tr><td>0xB</td><td>10.6</td><td>15.9</td></tr>
<tr><td>0xC</td><td>10.8</td><td>16.2</td></tr>
<tr><td>0xD</td><td>11</td><td>16.5</td></tr>
<tr><td>0xE</td><td>11.2</td><td>16.8</td></tr>
<tr><td>0xF</td><td>11.4</td><td>17.1</td></tr>
<tr><td>0x10</td><td>11.6</td><td>17.4</td></tr>
<tr><td>0x11</td><td>11.8</td><td>17.7</td></tr>
<tr><td>0x12</td><td>12</td><td>18</td></tr>
<tr><td>0x13</td><td>12.2</td><td>18.3</td></tr>
<tr><td>0x14</td><td>12.4</td><td>18.6</td></tr>
<tr><td>0x15</td><td>12.6</td><td>18.9</td></tr>
<tr><td>0x16</td><td>12.8</td><td>19.2</td></tr>
<tr><td>0x17</td><td>13</td><td>19.5</td></tr>
<tr><td>0x18</td><td>13.2</td><td>19.8</td></tr>
<tr><td>0x19</td><td>13.4</td><td>20.1</td></tr>
<tr><td>0x1A</td><td>13.6</td><td>20.4</td></tr>
<tr><td>0x1B</td><td>13.8</td><td>20.7</td></tr>
<tr><td>0x1C</td><td>14</td><td>21</td></tr>
<tr><td>0x1D</td><td>14.2</td><td>21.3</td></tr>
<tr><td>0x1E</td><td>14.4</td><td>21.6</td></tr>
<tr><td>0x1F</td><td>14.6</td><td>21.9</td></tr>
<tr><td>0x20</td><td>14.8</td><td>22.2</td></tr>
<tr><td>0x21</td><td>15</td><td>22.5</td></tr>
<tr><td>0x22</td><td>15.2</td><td>22.8</td></tr>
<tr><td>0x23</td><td>15.4</td><td>23.1</td></tr>
<tr><td>0x24</td><td>15.6</td><td>23.4</td></tr>
<tr><td>0x25</td><td>15.8</td><td>23.7</td></tr>
<tr><td>0x26</td><td>16</td><td>24</td></tr>
<tr><td>0x27</td><td>16.2</td><td>24.3</td></tr>
</table></td></tr>
</table>

BITFIELD	BITS	DESCRIPTION		
		0x28	16.4	24.6
		0x29	16.6	24.9
		0x2A	16.8	25.2
		0x2B	17	25.5
		0x2C	17.2	25.8
		0x2D	17.4	26.1
		0x2E	17.6	26.4
		0x2F	17.8	26.7
		0x30	18	27
		0x31	18.2	27.3
		0x32	18.4	27.6
		0x33	18.6	27.9
		0x34	18.8	28.2
		0x35	19	28.5
		0x36	19.2	28.8
		0x37	19.4	29.1
		0x38	19.6	29.4
		0x39	19.8	29.7
		0x3A	20	30
		0x3B	20.2	30.3
		0x3C	20.4	30.6
		0x3D	20.6	30.9
		0x3E	20.8	31.2
		0x3F	21	31.5

VGOFF (0x15)

BIT	7	6	5	4	3	2	1	0
Field	–	–	vgoff[5:0]					
Reset	–	–	0x16					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
vgoff	5:0	Sets VG_{OFF} voltage.	0x0: -4 0x1: -4.25 0x2: -4.5 0x3: -4.75 0x4: -5 0x5: -5.25 0x6: -5.5 0x7: -5.75 0x8: -6 0x9: -6.25 0xA: -6.5 0xB: -6.75 0xC: -7 0xD: -7.25 0xE: -7.5 0xF: -7.75 0x10: -8 0x11: -8.25 0x12: -8.5 0x13: -8.75 0x14: -9 0x15: -9.25 0x16: -9.5 0x17: -9.75 0x18: -10 0x19: -10.25 0x1A: -10.5 0x1B: -10.75 0x1C: -11 0x1D: -11.25 0x1E: -11.5 0x1F: -11.75 0x20: -12 0x21: -12.25 0x22: -12.5 0x23: -12.75 0x24: -13 0x25: -13.25 0x26: -13.5 0x27: -13.75 0x28: -14 0x29: -14.25 0x2A: -14.5 0x2B: -14.75 0x2C: -15 0x2D: -15.25 0x2E: -15.5 0x2F: -15.75 0x30: -16 0x31: -16.25 0x32: -16.5 0x33: -16.75 0x34: -17 0x35: -17.25 0x36: -17.5 0x37: -17.75 0x38: -18 0x39: Do not use 0x3A: Do not use

BITFIELD	BITS	DESCRIPTION	DECODE
			0x3B: Do not use 0x3C: Do not use 0x3D: Do not use 0x3E: Do not use 0x3F: Do not use

NV_CONFIG (0x17)

Nonvolatile configuration register

BIT	7	6	5	4	3	2	1	0
Field	nv_dis_navdd	nv_refresh	nv_en_ss	nv_fSW	nv_tretry[1:0]		nv_tfault[1:0]	
Reset	0x1	0x1	0x1	0x1	0x3		0x3	
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only		Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
nv_dis_navdd	7	NV setting for dis_navdd	
nv_refresh	6	NV setting for refresh bit	
nv_en_ss	5	NV setting for en_ss bit	
nv_fSW	4	NV setting for fSW bit	0x0: 2.2MHz 0x1: 440kHz
nv_tretry	3:2	NV setting for tretry bits	
nv_tfault	1:0	NV setting for tfault bits	

NV_DELAY (0x18)

BIT	7	6	5	4	3	2	1	0
Field	nv_delayt1[1:0]		nv_delayt2[1:0]		nv_delayt3[1:0]		unused	nv_par_en
Reset	0x3		0x3		0x3		0x1	0x1
Access Type	Read Only		Read Only		Read Only		Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
nv_delayt1	7:6	NV setting for delayt1
nv_delayt2	5:4	NV setting for delayt2
nv_delayt3	3:2	NV setting for delayt3
unused	1	
nv_par_en	0	NV setting for par_en bit

NV_SEQ (0x19)

BIT	7	6	5	4	3	2	1	0
Field	nv_seq_set[2:0]			nv_pfo_th	nv_tstart[1:0]		nv_lxp_lim_low	nv_start
Reset	0x7			0x1	0x3		0x1	0x1
Access Type	Read Only			Read Only	Read Only		Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
nv_seq_set	7:5	NV setting for seq_set bits
nv_pfo_th	4	NV setting for pfo_th bit
nv_tstart	3:2	NV setting for tstart bits
nv_lxp_lim_low	1	NV setting for lxp_lim_low bit
nv_start	0	NV setting for start bit

NV_ISET (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	unused	nv_iset[6:0]						
Reset	0x1	0x7F						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION
unused	7	
nv_iset	6:0	NV LED current setting

NV_BL_CONFIG1 (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	nv_dim_ext	nv_hdim	nv_hdim_thr[1:0]		nv_bstforce	nv_fast_ss	nv_psen	nv_fltb_mode
Reset	0x1	0x1	0x3		0x1	0x1	0x1	0x1
Access Type	Read Only	Read Only	Read Only		Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
nv_dim_ext	7	NV setting for dim_ext bit
nv_hdim	6	NV setting for hdim bit
nv_hdim_thr	5:4	NV setting for hdim_thr bits
nv_bstforce	3	NV setting for bstforce bit
nv_fast_ss	2	NV setting for fast_ss bit
nv_psen	1	NV setting for psen bit
nv_fltb_mode	0	NV setting for fltb_mode bit

NV_BL_CONFIG2 (0x1C)

BIT	7	6	5	4	3	2	1	0
Field	nv_bl_ilim	nv_fpwm[2:0]			nv_bl_ss_off	nv_bl_ssl	nv_sldet[1:0]	
Reset	0x1	0x7			0x1	0x1	0x3	
Access Type	Read Only	Read Only			Read Only	Read Only	Read Only	

BITFIELD	BITS	DESCRIPTION
nv_bl_ilim	7	NV setting for bl_ilim bit
nv_fpwm	6:4	NV setting for fpwm bits

BITFIELD	BITS	DESCRIPTION
nv_bl_ss_off	3	NV setting for bl_ss_off bit
nv_bl_ssl	2	NV setting for bl_ssl bit
nv_sldet	1:0	NV setting for shorted-LED threshold

NV_BL_DIS (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	nv_cp_dis	unused	nv_dis_bl	nv_dis6	nv_dis5	nv_dis4	nv_dis3	nv_dis2
Reset	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
nv_cp_dis	7	NV setting for cp_dis bit
unused	6	
nv_dis_bl	5	NV setting for dis_bl bit
nv_dis6	4	NV setting for dis6 bit
nv_dis5	3	NV setting for dis5 bit
nv_dis4	2	NV setting for dis4 bit
nv_dis3	1	NV setting for dis3 bit
nv_dis2	0	NV setting for dis2 bit

NV_BL_FADING (0x1E)

BIT	7	6	5	4	3	2	1	0
Field	unused[2:0]			nv_fade_gain	nv_fade_in_out	nv_tfade[2:0]		
Reset	0x7			0x1	0x1	0x7		
Access Type	Read Only			Read Only	Read Only	Read Only		

BITFIELD	BITS	DESCRIPTION
unused	7:5	
nv_fade_gain	4	NV setting for fade_gain bit
nv_fade_in_out	3	NV setting for fade_in_out
nv_tfade	2:0	NV setting for tfade bits

NV_CUSTOMER_USE1 (0x1F)

Register which can be used to store user data.

BIT	7	6	5	4	3	2	1	0
Field	nv_customer_use1[7:0]							
Reset	0xff							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
nv_customer_use1	7:0	

NV_CUSTOMER_USE2 (0x20)

Register which can be used to store user data.

BIT	7	6	5	4	3	2	1	0
Field	nv_customer_use2[7:0]							
Reset	0xff							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
nv_customer_use2	7:0	

NV_CUSTOMER_USE3 (0x21)

Register which can be used to store user data.

BIT	7	6	5	4	3	2	1	0
Field	nv_customer_use3[7:0]							
Reset	0xff							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
nv_customer_use3	7:0	

NV_CUSTOMER_USE4 (0x22)

Register which can be used to store user data.

BIT	7	6	5	4	3	2	1	0
Field	nv_customer_use4[7:0]							
Reset	0xff							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
nv_customer_use4	7:0	

NV_AVDD_SET (0x23)

BIT	7	6	5	4	3	2	1	0
Field	unused[1:0]		nv_avdd[5:0]					
Reset	0x3		0x3f					
Access Type	Read Only		Read Only					

BITFIELD	BITS	DESCRIPTION
unused	7:6	
nv_avdd	5:0	NV setting for avdd bits

NV_VGON (0x24)

BIT	7	6	5	4	3	2	1	0
Field	unused[1:0]		nv_vgon[5:0]					
Reset	0x3		0x3f					
Access Type	Read Only		Read Only					

BITFIELD	BITS	DESCRIPTION
unused	7:6	
nv_vgon	5:0	NV setting for vgon bits

NV_VGOFF (0x25)

BIT	7	6	5	4	3	2	1	0
Field	unused[1:0]		nv_vgoff[5:0]					
Reset	0x3		0x3f					
Access Type	Read Only		Read Only					

BITFIELD	BITS	DESCRIPTION
unused	7:6	
nv_vgoff	5:0	NV setting for vgoff bits

AVDD_LIM (0x26)

BIT	7	6	5	4	3	2	1	0
Field	–	–	avdd_lim[5:0]					
Reset	–	–	0x3F					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
avdd_lim	5:0	Maximum limit setting for avdd. To use this function, write to this register before setting avdd. An avdd setting above avdd_lim will not be accepted.

LO_DIM (0x27)

BIT	7	6	5	4	3	2	1	0
Field	ton_master	–	lo_dim6	lo_dim5	lo_dim4	lo_dim3	lo_dim2	lo_dim1
Reset	0x0	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
ton_master	7	When this bit is set, the 18-bit PWM setting for channel 1 (TON1H:TON1L:TON1LSB) applies to all 6 channels.
lo_dim6	5	When 1, indicates that channel 6 is in low-dim mode.
lo_dim5	4	When 1, indicates that channel 5 is in low-dim mode.
lo_dim4	3	When 1, indicates that channel 4 is in low-dim mode.

BITFIELD	BITS	DESCRIPTION
lo_dim3	2	When 1, indicates that channel 3 is in low-dim mode.
lo_dim2	1	When 1, indicates that channel 2 is in low-dim mode.
lo_dim1	0	When 1, indicates that channel 1 is in low-dim mode.

TON1H (0x28)

BIT	7	6	5	4	3	2	1	0
Field	ton1h[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ton1h	7:0	Most significant byte of 18-bit on-time setting for channel 1. This value is set in 50ns units.

TON1L (0x29)

BIT	7	6	5	4	3	2	1	0
Field	ton1l[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ton1l	7:0	Least significant byte of 18-bit on-time setting for channel 1. This value is set in 50ns units.

TON2H (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	ton2h[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ton2h	7:0	Most significant byte of 18-bit on-time setting for channel 2. This value is set in 50ns units.

TON2L (0x2B)

BIT	7	6	5	4	3	2	1	0
Field	ton2l[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ton2l	7:0	Least significant byte of 18-bit on-time setting for channel 2. This value is set in 50ns units.

TON3H (0x2C)

BIT	7	6	5	4	3	2	1	0
Field	ton3h[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ton3h	7:0	Most significant byte of 18-bit on-time setting for channel 3. This value is set in 50ns units.

TON3L (0x2D)

BIT	7	6	5	4	3	2	1	0
Field	ton3l[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ton3l	7:0	Least significant byte of 18-bit on-time setting for channel 3. This value is set in 50ns units.

TON1_3LSB (0x2E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ton3lsb[1:0]		ton2lsb[1:0]		ton1lsb[1:0]	
Reset	–	–	0x3		0x3		0x3	
Access Type	–	–	Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
ton3lsb	5:4	Least significant bits of 18-bit on-time setting for channel 3. This value is set in 50ns units.
ton2lsb	3:2	Least significant bits of 18-bit on-time setting for channel 2. This value is set in 50ns units.
ton1lsb	1:0	Least significant bits of 18-bit on-time setting for channel 1. This value is set in 50ns units.

TON4H (0x2F)

BIT	7	6	5	4	3	2	1	0
Field	ton4h[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ton4h	7:0	Most significant byte of 18-bit on-time setting for channel 4. This value is set in 50ns units.

TON4L (0x30)

BIT	7	6	5	4	3	2	1	0
Field	ton4l[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ton4l	7:0	Least significant byte of 18-bit on-time setting for channel 4. This value is set in 50ns units.

TON5H (0x31)

BIT	7	6	5	4	3	2	1	0
Field	ton5h[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ton5h	7:0	Most significant byte of 18-bit on-time setting for channel 5. This value is set in 50ns units.

TON5L (0x32)

BIT	7	6	5	4	3	2	1	0
Field	ton5l[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ton5l	7:0	Least significant byte of 18-bit on-time setting for channel 5. This value is set in 50ns units.

TON6H (0x33)

BIT	7	6	5	4	3	2	1	0
Field	ton6h[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ton6h	7:0	Most significant byte of 18-bit on-time setting for channel 6. This value is set in 50ns units.

TON6L (0x34)

BIT	7	6	5	4	3	2	1	0
Field	ton6l[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ton6l	7:0	Least significant byte of 18-bit on-time setting for channel 6. This value is set in 50ns units.

TON4_6LSB (0x35)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ton6lsb[1:0]		ton5lsb[1:0]		ton4lsb[1:0]	
Reset	–	–	0x3		0x3		0x3	
Access Type	–	–	Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
ton6lsb	5:4	Least significant bits of 18-bit on-time setting for channel 6. This value is set in 50ns units.
ton5lsb	3:2	Least significant bits of 18-bit on-time setting for channel 5. This value is set in 50ns units.
ton4lsb	1:0	Least significant bits of 18-bit on-time setting for channel 4. This value is set in 50ns units.

OPEN_REG (0x36)

BIT	7	6	5	4	3	2	1	0
Field	–	–	out6o	out5o	out4o	out3o	out2o	out1o
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
out6o	5	When 1, this bit indicates an open-circuit condition on OUT6.
out5o	4	When 1, this bit indicates an open-circuit condition on OUT5.
out4o	3	When 1, this bit indicates an open-circuit condition on OUT4.
out3o	2	When 1, this bit indicates an open-circuit condition on OUT3.
out2o	1	When 1, this bit indicates an open-circuit condition on OUT2.
out1o	0	When 1, this bit indicates an open-circuit condition on OUT1.

SHORTGND_REG (0x37)

BIT	7	6	5	4	3	2	1	0
Field	–	–	out6sg	out5sg	out4sg	out3sg	out2sg	out1sg
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
out6sg	5	When 1, this bit indicates a short-to-ground condition on OUT6.
out5sg	4	When 1, this bit indicates a short-to-ground condition on OUT5.
out4sg	3	When 1, this bit indicates a short-to-ground condition on OUT4.
out3sg	2	When 1, this bit indicates a short-to-ground condition on OUT3.
out2sg	1	When 1, this bit indicates a short-to-ground condition on OUT2.
out1sg	0	When 1, this bit indicates a short-to-ground condition on OUT1.

SHORTED_LED_REG (0x38)

BIT	7	6	5	4	3	2	1	0
Field	–	–	out6sl	out5sl	out4sl	out3sl	out2sl	out1sl
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Read Clears All	Read Sets All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
out6sl	5	When 1, this bit indicates a shorted-LED condition on OUT6.
out5sl	4	When 1, this bit indicates a shorted-LED condition on OUT5.
out4sl	3	When 1, this bit indicates a shorted-LED condition on OUT4.
out3sl	2	When 1, this bit indicates a shorted-LED condition on OUT3.
out2sl	1	When 1, this bit indicates a shorted-LED condition on OUT2.
out1sl	0	When 1, this bit indicates a shorted-LED condition on OUT1.

BL_MASK (0x39)

BIT	7	6	5	4	3	2	1	0
Field	–	battuv	battuvmask	bstuvmask	omask	sgmask	bl_otwmask	slmask
Reset	–		0x1	0x0	0x0	0x0	0x1	0x0
Access Type	–	Read Clears All	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
battuv	6	This bit indicates an undervoltage on the BATT pin, which causes the backlight boost to be disabled.
battuvmask	5	Mask bit for BATT undervoltage indication. When 1, an undervoltage on BATT does not cause FLTB to assert low.
bstuvmask	4	Mask bit for boost undervoltage indication. When 1, an undervoltage on the boost output does not cause FLTB to assert low.
omask	3	Mask bit for open-LED indication.
sgmask	2	Mask bit for short-to-GND indication.

BITFIELD	BITS	DESCRIPTION
bl_otwmask	1	When 1, this bit prevents a backlight overtemperature warning from asserting the FLTB pin low.
slmask	0	Mask bit for shorted-LED indication.

BL_DIAG (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	v5oor	rtoor	irefoor	bstuv	bstov	hw_rst	bl_otw	bl_ot
Reset		0x0	0x0	0x0	0x0	0x1	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
v5oor	7	When 1, this bit indicates that the V5 supply for the NDRV output is out of range. When V5 out of range is detected, the backlight block is disabled.
rtoor	6	When set to 1, this bit indicates that the resistor on RT is out of the prescribed range.
irefoor	5	When 1, this bit indicates that the IREF current is too high. This is probably due to an incorrect resistor value on IREF. In this condition, the IC stops operation.
bstuv	4	If 1, an undervoltage has been detected on the boost output and the boost was disabled.
bstov	3	If 1, the boost converter is at its overvoltage limit.
hw_rst	2	If 1, the device has just emerged from a hardware reset (power-up). This bit is reset after the first read from this register.
bl_otw	1	If 1, the temperature of the backlight section is over +125°C or the temperature foldback circuit has reached the temperature T1.
bl_ot	0	If 1, the temperature of the backlight section exceeded +165°C and the backlight block was shut down or the TEMP input reached the level that shuts off the LED currents.

VBSTMON (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	vbstmon[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
vbstmon	7:0	ADC measurement result on BSTMON pin

IOUT1 (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	iout1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
iout1	7:0	ADC current measurement result for OUT1

IOUT2 (0x3D)

BIT	7	6	5	4	3	2	1	0
Field	iout2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
iout2	7:0	ADC current measurement result for OUT2

IOUT3 (0x3E)

BIT	7	6	5	4	3	2	1	0
Field	iout3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
iout3	7:0	ADC current measurement result for OUT3

IOUT4 (0x3F)

BIT	7	6	5	4	3	2	1	0
Field	iout4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
iout4	7:0	ADC current measurement result for OUT4

IOUT5 (0x40)

BIT	7	6	5	4	3	2	1	0
Field	iout5[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
iout5	7:0	ADC current measurement result for OUT5

IOUT6 (0x41)

BIT	7	6	5	4	3	2	1	0
Field	iout6[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
iout6	7:0	ADC current measurement result for OUT6

burn_otp_reg (0x78)

BIT	7	6	5	4	3	2	1	0
Field	burn_otp[7:0]							
Reset	0x0							
Access Type	Write Only							

BITFIELD	BITS	DESCRIPTION
burn_otp	7:0	Command to copy the contents of registers 0x07–0x15 to the nonvolatile registers 0x17–0x25. Send the data 8'hA5 after the address 8'h78 to enable the command.

reboot_otp_reg (0x79)

BIT	7	6	5	4	3	2	1	0
Field	reboot_otp[7:0]							
Reset								
Access Type	Write Only							

BITFIELD	BITS	DESCRIPTION
reboot_otp	7:0	Command to copy the contents of the nonvolatile registers 0x17–0x15 to the working registers 0x17–0x25. Send the data 8'h5A after the address 8'h79 to enable the command.

soft_restart (0x7A)

BIT	7	6	5	4	3	2	1	0
Field	soft_restart[7:0]							
Reset	0x00							
Access Type	Write Only							

BITFIELD	BITS	DESCRIPTION
soft_restart	7:0	Command used to restart the device from a latched fault mode. All faults are cleared when this command is executed. Send the data 8'hC3 after the address 8'h7A to enable the command.

Applications Information

TFT Power Section

AVDD Boost Converter

Boost Converter Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DC}). Use a 2.2µH inductor when the boost converter operates at 2.1MHz and 10µH at 420kHz. In unipolar mode, use a 3.3µH inductor at 2.1MHz.

The inductor's saturation rating must exceed the maximum LXP current limit.

Boost Output-Filter Capacitor Selection

The primary criterion for selecting the output-filter capacitor is low effective series resistance (ESR). The product of the peak inductor current and the output filter capacitor's ESR determine the amplitude of the high-frequency ripple seen on the output voltage. For stability, the boost output-filter capacitor should have a value of 10µF or greater at 2.1MHz and 20µF at 420kHz.

To avoid a large drop on HVINP when NAVDD is enabled, the capacitance on the HVINP node should be larger than that on NAVDD.

Boost Converter External Diode Selection

Select a diode with a peak current rating of at least the LXP current limit for use with the HVINP output. The diode breakdown-voltage rating should exceed the absolute value of the HVINP voltage. A Schottky diode improves the overall efficiency of the converter, but should be selected to have low leakage at the maximum operating temperature.

Setting the AVDD Voltage

The AVDD output is set by writing a 6-bit value to the avdd[5:0] field in the AVDD_SET register (address 0x13). The output voltage also depends on the setting of the dis_navdd bit in the TFT_CONFIG register (address 0x07).

NAVDD Inverting Regulator

The NAVDD converter outputs a negative voltage whose absolute value is the same as AVDD. The most negative voltage NAVDD can output is -10.5V. NAVDD can be disabled using the dis_navdd bit in the TFT_CONFIG register.

NAVDD Regulator Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DC}). Use a 2.2µH inductor when the converter operates at 2.1MHz and 10µH at 420kHz.

The inductor's saturation current rating must exceed the maximum LXN current limit.

NAVDD External Diode Selection

Select a diode with a peak current rating of at least the LXN current limit for use with the NAVDD output. The diode breakdown-voltage rating should exceed the sum of the maximum INN voltage and the absolute value of the NAVDD voltage. A Schottky diode improves the overall efficiency of the converter.

NAVDD Output Capacitor Selection

The primary criteria for selecting the output filter capacitor are low ESR and capacitance values, as the NAVDD capacitor provides the load current when the internal switch is on. The voltage ripple on the NAVDD output has two components:

- Ripple due to ESR, which is the product of the peak inductor current and the output filter capacitor's ESR
- Ripple due to bulk capacitance, which can be determined as follows:

$$\Delta V_{BULK} = \frac{I_{NAVDDG} \times \frac{D}{f_{SW}}}{C_{NAVDD}}$$

For stability, the NAVDD output capacitor should have a value of 10µF or greater when the switching frequency is 2.1MHz and greater than 15µF at 420kHz.

Setting the VG_{ON} and VG_{OFF} Output Voltages

Choose the external charge pump circuitry based on the ratios VG_{ON}/HVINP and VG_{OFF}/HVINP. In all cases, the VG_{ON} and VG_{OFF} voltages should be maintained within their permitted operating ranges.

The VG_{ON} and VG_{OFF} voltages are set by writing 6-bit values to the VG_{ON} (0x14) and VG_{OFF} (0x15) registers. Note that the VG_{ON} voltage range depends on the setting of dis_navdd bit.

LED Driver Section

DC-DC Converter for LED Driver

Two different converter topologies are possible with the DC-DC controller in the device, which has the ground-referenced outputs necessary to use the constant-current sink drivers. If the LED string forward voltage is always higher than the input supply voltage range, use the boost-converter topology. If the LED string forward voltage falls within the supply-voltage range, use the SEPIC topology.

Note that the boost converter topology provides the highest efficiency.

Power-Circuit Design

First select a converter topology based on the above factors. Determine the required input supply-voltage range, the maximum voltage needed to drive the LED strings, including the worst-case 0.875V across the constant LED current sink (V_{LED}), and the total output current needed to drive the LED strings (I_{LED}) as follows:

$$I_{LED} = I_{STRING} \times N_{STRING}$$

where I_{STRING} is the LED current per string in amperes and N_{STRING} is the number of strings used. Calculate the maximum duty cycle (D_{MAX}) using the following equations:

Boost Configuration:

$$D_{MAX} = \frac{\left(V_{LED} + V_{D1} - V_{IN\_MIN}\right)}{\left(V_{LED} + V_{D1} - V_{DS} - 0.42\right)}$$

SEPIC Configuration:

$$D_{MAX} = \frac{\left(V_{LED} + V_{D1}\right)}{\left(V_{IN\_MIN} - V_{DS} - 0.42 + V_{LED} + V_{D1}\right)}$$

where V_{D1} is the forward drop of the rectifier diode in volts (approximately 0.6V), V_{IN_MIN} is the minimum input supply voltage in volts, V_{DS} is the drain-to-source voltage of the external MOSFET in volts when it is on, and 0.42V is the peak current-sense voltage. Initially, use an approximate value of 0.2V for V_{DS} to calculate D_{MAX}. Calculate a more accurate value of D_{MAX} after the power MOSFET is selected based on the maximum inductor current.

Boost Configuration

The average inductor current varies with the line voltage, and the maximum average current occurs at the lowest line voltage. For the boost converter, the average inductor current is equal to the input current. Select the maximum peak-to-peak ripple on the inductor current (ΔI_L). The recommended peak-to-peak ripple is 60% of the average inductor current.

Use the following equations to calculate the maximum average inductor current (IL_{AVG}) and peak inductor current (IL_P) in amperes.

$$IL_{AVG} = \frac{I_{LED}}{1 - D_{MAX}}$$

Allowing the peak-to-peak inductor ripple (ΔI_L) to be ±30% of the average inductor current:

$$\Delta I_L = IL_{AVG} \times 0.3 \times 2$$

and

$$IL_P = IL_{AVG} + \frac{\Delta I_L}{2}$$

Calculate the minimum inductance value (L_{MIN}) in henries with the inductor-current ripple set to the maximum value.

$$L_{MIN} = \frac{\left(V_{IN\_MIN} - V_{DS} - 0.41\right) \times D_{MAX}}{f_{SW} \times \Delta I_L}$$

where 0.41V is the peak current-sense voltage (with bl_ilim set to 0, if bl_ilim is set to 1 use 0.3V in this equation). Choose an inductor that has a minimum inductance greater than the calculated L_{MIN} and current rating greater than IL_P. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current for boost configuration.

SEPIC Configuration

Power-circuit design for the SEPIC configuration is very similar to a conventional design, with the output voltage referenced to the input supply voltage. For SEPIC, the output is referenced to ground and the inductor is split into two parts (see the *SEPIC Application Circuit*). One of the inductors (L2) has the LED current as the average current, and the other inductor (L1) has the input current as its average current. Use the following equations to calculate the average inductor currents ($IL1_{AVG}$, $IL2_{AVG}$) and peak inductor currents ($IL1_P$, $IL2_P$) in amperes:

$$IL1_{AVG} = \frac{I_{LED} \times D_{MAX} \times 1.1}{1 - D_{MAX}}$$

The factor 1.1 provides a 10% margin to account for the converter losses:

$$IL2_{AVG} = I_{LED}$$

Assuming the peak-to-peak inductor ripple (ΔI_L) is ±30% of the average inductor current:

$$\Delta I_{L1} = IL1_{AVG} \times 0.3 \times 2$$

and

$$IL1_P = IL1_{AVG} + \frac{\Delta I_{L1}}{2}$$

$$\Delta I_{L2} = IL2_{AVG} \times 0.3 \times 2$$

and

$$IL2_P = IL2_{AVG} + \frac{\Delta I_{L2}}{2}$$

Calculate the minimum inductance values $L1_{MIN}$ and $L2_{MIN}$ in henries with the inductor current ripples set to the maximum value as follows:

$$L1_{MIN} = \frac{\left(V_{IN\_MIN} - V_{DS} - 0.42\right) \times D_{MAX}}{f_{SW} \times \Delta I_{L1}}$$

$$L2_{MIN} = \frac{\left(V_{IN\_MIN} - V_{DS} - 0.42\right) \times D_{MAX}}{f_{SW} \times \Delta I_{L2}}$$

where 0.42V is the peak current-sense voltage. Choose inductors that have a minimum inductance greater than the calculated $L1_{MIN}$ and $L2_{MIN}$, and current ratings greater than $IL1_P$ and $IL2_P$, respectively. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current.

For simplifying further calculations, consider L1 and L2 as a single inductor with L1/L2 connected in parallel. The combined inductance value and current is calculated as follows:

$$L_{MIN} = \frac{L1_{MIN} \times L2_{MIN}}{L1_{MIN} + L2_{MIN}}$$

and

$$IL_{AVG} = IL1_{AVG} + IL2_{AVG}$$

where IL_{AVG} represents the total average current through both the inductors, connected together for SEPIC configuration. Use these values in the calculations for the SEPIC configuration in the following sections.

Select coupling capacitor CS so that the peak-to-peak ripple on it is less than 2% of the minimum input supply voltage. This ensures that the second-order effects created by the series resonant circuit comprising L1, CS, and L2 do not affect the normal operation of the converter. Use the following equation to calculate the minimum value of CS:

$$CS \geq \frac{I_{LED} \times D_{MAX}}{V_{IN\_MIN} \times 0.02 \times f_{SW}}$$

where CS is the minimum value of the coupling capacitor in farads, I_{LED} is the LED current in amperes, and the factor 0.02 accounts for 2% ripple.

Current-Sense Resistor and Slope Compensation

The MAX25169 backlight boost generates a current ramp for slope compensation. This ramp current is synchronized to the switching frequency, starting from zero at the beginning of every clock cycle and rising linearly to reach 50µA at the end of the clock cycle. The slope-compensating resistor (R_{SC}) is connected between the CSP input and the source of the external MOSFET. This adds a programmable ramp voltage to the CSP input voltage to provide slope compensation.

Use the following equations to calculate the value of slope-compensation resistance (R_{SC}):

Boost Configuration:

$$R_{SC} = \frac{(V_{LED} - 2 \times V_{IN\_MIN}) \times R_{CS} \times 3}{L_{MIN} \times 50\mu A \times f_{SW} \times 4}$$

SEPIC and Coupled-Inductor Configurations:

$$R_{SC} = \frac{(V_{LED} - V_{IN\_MIN}) \times R_{CS} \times 3}{L_{MIN} \times 50\mu A \times f_{SW} \times 4}$$

where V_{LED} and V_{IN_MIN} are in volts, R_{SC} and R_{CS} are in ohms, L_{MIN} is in henries, and f_{SW} is in hertz. The value of the switch current-sense resistor (R_{CS}) can be calculated as follows:

Boost Configuration:

$$R_{CS} = \frac{4 \times L_{MIN} \times f_{SW} \times V_{CS\_MAX} \times 0.9}{I_{LP} \times 4 \times L_{MIN} \times f_{SW} + D_{MAX} \times \left(V_{LED} - 2 \times V_{IN\_MIN}\right) \times 3}$$

SEPIC and Coupled-Inductor Configurations:

$$R_{CS} = \frac{4 \times L_{MIN} \times f_{SW} \times V_{CS\_MAX} \times 0.9}{I_{LP} \times 4 \times L_{MIN} \times f_{SW} + D_{MAX} \times \left(V_{LED} - V_{IN\_MIN}\right) \times 3}$$

where V_{CS_MAX} is the minimum value of the peak current-sense threshold or 0.38 with bl_ilim = 0 and 0.275 when bl_ilim is set to 1. The current-sense threshold also includes the slope-compensation component. The minimum current-sense threshold is multiplied by 0.9 to take tolerances into account.

Output Capacitor Selection

For all converter topologies, the output capacitor supplies the load current when the main switch is on. The function of the output capacitor is to reduce the converter output ripple to acceptable levels. The entire output-voltage ripple appears across the constant-current sink outputs because the LED string voltages are stable due to the constant current. For the MAX25169, limit the peak-to-peak output-voltage ripple to 250mV to get stable output current.

The ESR, ESL, and bulk capacitance of the output capacitor contribute to the output ripple. In most applications, using low-ESR ceramic capacitors can dramatically reduce the output ESR and ESL effects, connecting multiple ceramic

capacitors in parallel to achieve the required bulk capacitance. To minimize audible noise during PWM dimming however, it may be desirable to limit the use of ceramic capacitors on the boost output. In such cases, an additional electrolytic or tantalum capacitor can provide the majority of the bulk capacitance.

External Switching-MOSFET Selection

The external switching MOSFET should have a voltage rating sufficient to withstand the maximum boost output voltage, together with the rectifier diode drop and any possible overshoot due to ringing caused by parasitic inductance and capacitance. The recommended MOSFET V_{DS} voltage rating is 30% higher than the sum of the maximum output voltage and the rectifier diode drop.

The continuous drain-current rating of the MOSFET (ID), when the case temperature is at the maximum operating ambient temperature, should be greater than that calculated as follows:

$$ID_{RMS} = \left(\sqrt{IL_{AVG}^2 \times D_{MAX}}\right) \times 1.3$$

The MOSFET dissipates power due to both switching losses and conduction losses. Use the following equation to calculate the conduction losses in the MOSFET:

$$P_{COND} = IL^2_{AVG} \times D_{MAX} \times R_{DS(ON)}$$

where $R_{DS(ON)}$ is the on-state drain-to-source resistance of the MOSFET. Use the following equation to calculate the switching losses in the MOSFET:

$$P_{SW} = \frac{IL_{AVG} \times V_{LED}^2 \times C_{GD} \times f_{SW}}{2} \times \left(\frac{1}{I_{GON}} + \frac{1}{I_{GOFF}}\right)$$

where I_{GON} and I_{GOFF} are the gate currents of the MOSFET in amperes when it is turned on and turned off, respectively. C_{GD} is the gate-to-drain MOSFET capacitance in farads.

Rectifier Diode Selection

Using a Schottky rectifier diode produces less forward drop and puts the least burden on the MOSFET during reverse recovery. A diode with considerable reverse-recovery time increases the MOSFET switching loss. Select a Schottky diode with a voltage rating 20% higher than the maximum boost-converter output voltage and current rating greater than the following:

$$I_D = IL_{AVG} \times \left(1 - D_{MAX}\right) \times 1.2$$

Feedback Compensation

During normal operation, the feedback control loop regulates the minimum OUT_ voltage to fall within the window comparator limits of 0.58V and 0.85V when LED string currents are enabled during PWM dimming. When LED currents are off during PWM dimming, the control loop turns off the converter. When the PWM dimming pulses are narrower than 50µs, the converter operates continuously.

The worst-case condition for the feedback loop is when the LED driver is in normal mode regulating the minimum OUT_ voltage. The switching converter small-signal transfer function has a right-half plane (RHP) zero for boost configuration if the inductor current is in continuous-conduction mode. The RHP zero adds a 20dB/decade gain and a 90° phase lag, which is difficult to compensate.

The worst-case RHP zero frequency (f_{ZRHP}) is calculated as follows:

Boost Configuration:

$$f_{ZRHP} = \frac{V_{LED} \times \left(1 - D_{MAX}\right)^2}{2\pi \times L \times I_{LED}}$$

SEPIC Configuration:

$$f_{ZRHP} = \frac{V_{LED} \times \left(1 - D_{MAX}\right)^2}{2\pi \times L \times I_{LED} \times D_{MAX}}$$

where f_{ZRHP} is in hertz, V_{LED} is in volts, L is the inductance value of L1 in henries, and I_{LED} is in amperes. A simple way to avoid this zero is to roll off the loop gain to 0dB at a frequency less than 1/5 of the RHP zero frequency with a -20dB/decade slope.

The switching converter small-signal transfer function also has an output pole. The effective output impedance, together with the output filter capacitance, determines the output pole frequency (f_{P1}), calculated as follows:

Boost Configuration:

$$f_{P1} = \frac{I_{LED}}{2\pi \times V_{LED} \times C_{OUT}}$$

SEPIC Configuration:

$$f_{P1} = \frac{I_{LED} \times D_{MAX}}{2\pi \times V_{LED} \times C_{OUT}}$$

where f_{P1} is in hertz, V_{LED} is in volts, I_{LED} is in amperes, and C_{OUT} is in farads. Compensation components (R_{COMP} and C_{COMP}) perform two functions: C_{COMP} introduces a low-frequency pole that presents a -20dB/ decade slope to the loop gain, and R_{COMP} flattens the gain of the error amplifier for frequencies above the zero formed by R_{COMP} and C_{COMP}. For compensation, this zero is placed at the output pole frequency (f_{P1}), so it provides a -20dB/decade slope for frequencies above f_{P1} to the combined modulator and compensator response.

The value of R_{COMP} needed to fix the total loop gain at f_{P1}, so the total loop gain crosses 0dB with -20dB/decade slope at 1/5 the RHP zero frequency, is calculated as follows:

Boost Configuration:

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED}}{5 \times f_{P1} \times GM_{COMP} \times V_{LED} \times \left(1 - D_{MAX}\right)}$$

SEPIC Configuration:

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED} \times D_{MAX}}{5 \times f_{P1} \times GM_{COMP} \times V_{LED} \times \left(1 - D_{MAX}\right)}$$

where R_{COMP} is the compensation resistor in ohms, f_{ZRHP} and f_{P2} are in hertz, R_{CS} is the switch current-sense resistor in ohms, and GM_{COMP} is the transconductance of the error amplifier (700µS).

The value of C_{COMP} is calculated as follows:

$$C_{COMP} = \frac{1}{2\pi \times R_{COMP} \times f_{Z1}}$$

where f_{Z1} is the compensation zero placed at 1/5 of the crossover frequency that is, in turn, set at 1/5 of the f_{ZRHP}. If the output capacitors do not have low ESR, the ESR zero frequency may fall within the 0dB crossover frequency. An additional pole may be required to cancel out this pole placed at the same frequency. This can be implemented by connecting a capacitor from COMP directly to GND.

Using NV Memory

Follow the sequence below to perform nonvolatile programming of the device when the autorefresh function is not used:

1. Apply a voltage between 3.3V and 5V to the IN and INN pins with the device in full I2C mode.
2. Write the desired values to be stored in OTP to the registers from 0x07 to 0x15.
3. Apply 8.5V to V_{PROG}.
4. Optionally wait to ensure the 8.5V at V_{PROG} is stable.
5. Send burn_otp_reg (write 0xA5 to register address 0x78) command. If parity is enabled, ensure the overall parity is even by altering the final byte if necessary.
6. Wait 20ms.
7. If the nv_flt bit is 0, the write was successful; go to the next step. If nv_flt = 1, perform retry (steps 5 and 6).
8. Send reboot_otp (write 0x5A to register address 0x79) command or power-cycle the part.

Special care is required when performing nonvolatile programming with the autorefresh feature enabled. In such cases,

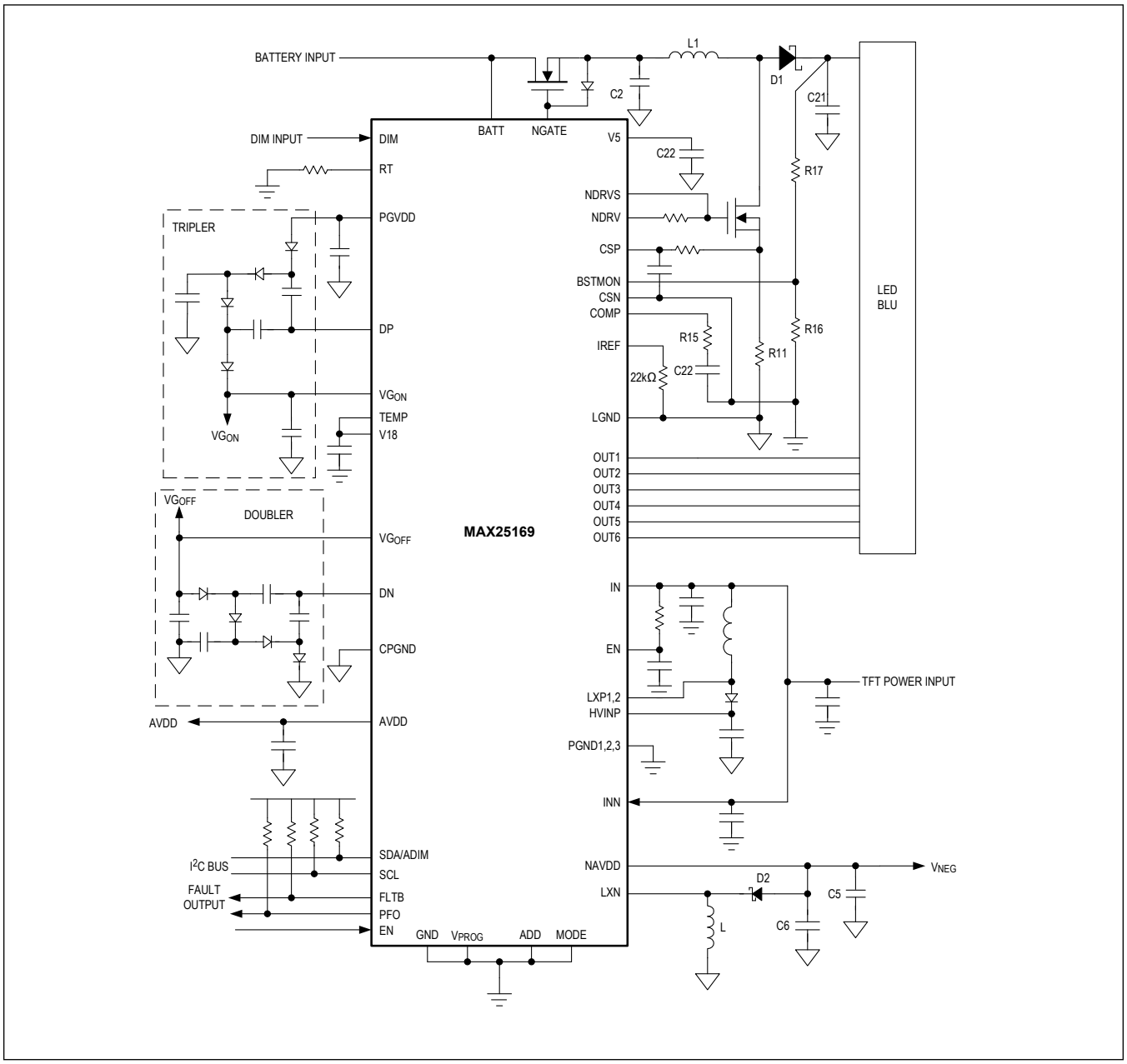
follow the sequence below when at least one calibration has already been performed:

1. Apply a voltage between 3.3V and 5V to the IN and INN pins with the device in full I2C mode.
2. Set REG_CTRL[6] = 1. This dis_refresh bit inhibits refresh during programming operations.
3. Write the desired data to volatile registers.
4. Apply 8.5V to V_{PROG}.
5. Send the burn_otp_reg (write 0xA5 to 0x78) command.
6. Wait 20ms.
7. If the nv_flt bit is 0, the write was successful; go to the next step. If nv_flt = 1, perform retry (steps 5 and 6).
8. Send reboot_otp (write 0x5A to register address 0x79) command or power-cycle the part.
9. Check/set REG_CTRL[6] = 0.

The nonvolatile memory can be written to a total of six times.

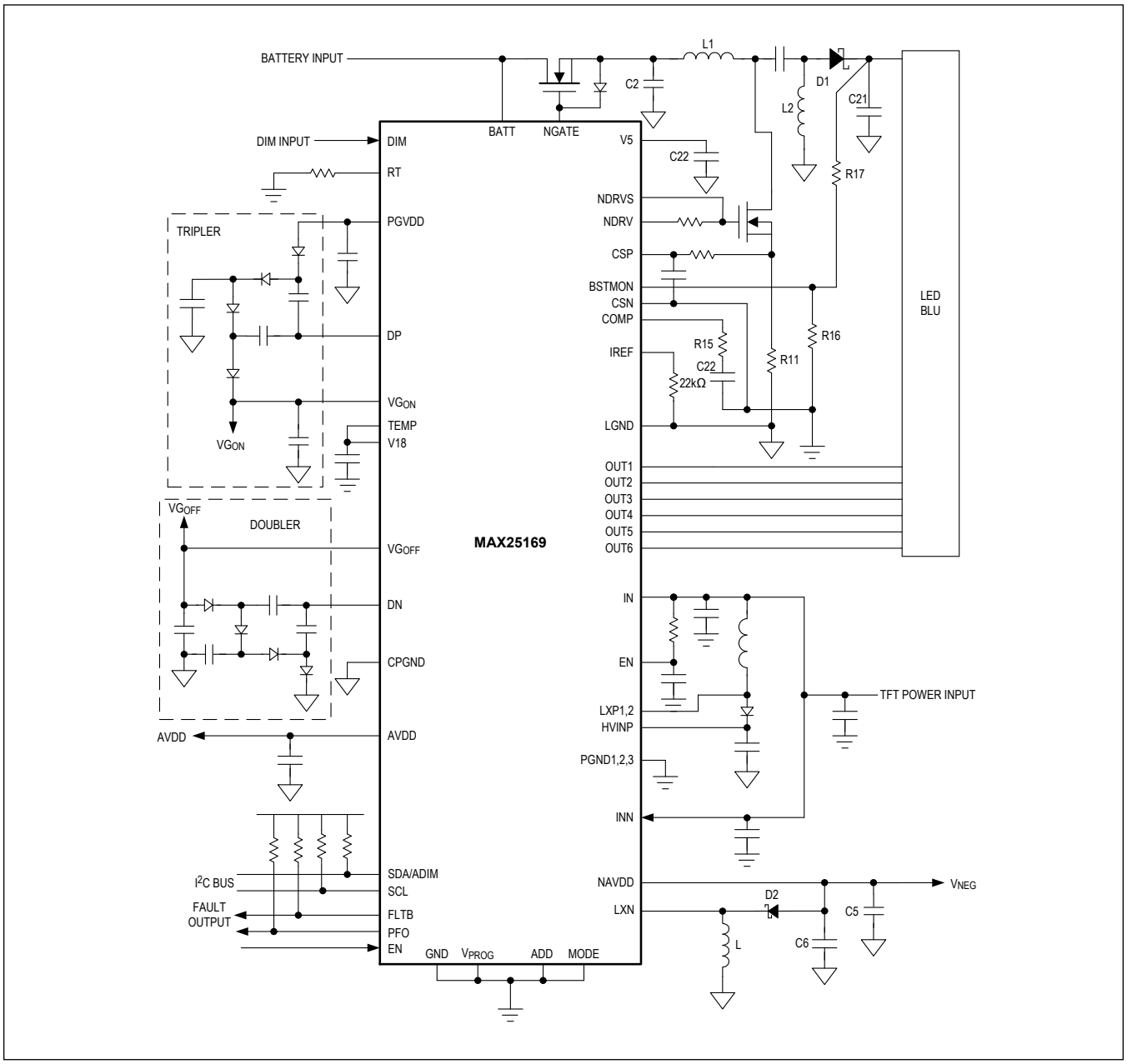
Typical Application Circuit

Basic Application Circuit



Typical Application Circuit (continued)

SEPIC Application Circuit



Ordering Information

PART	TEMP RANGE	PACKAGE CODE	PIN-PACKAGE	FEATURES	7-BIT I2C ADDRESSES
MAX25169ATM/V+	-40°C to +125°C	T4877+9C	48 TQFN-EP*	—	0x46/0x47
MAX25169ATM/VY+	-40°C to +125°C	T4877Y+9C	48 TQFN-EP*	—	0x46/0x47
MAX25169ATMB/V+**	-40°C to +125°C	T4877+9C	48 TQFN-EP*	VG_{ON}/VG_{OFF} disabled	0x46/0x47

/V Denotes an automotive-qualified part.

+ Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Y = Side-wettable (SW) package.

***Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/22	Initial release	—
1	6/23	Removed future product designation from side-wettable package, added parity checking paragraph.	38, 77