TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74HC373AP,TC74HC373AF,TC74HC373AFW

#### Octal D-Type Latch with 3-State Output

The TC74HC373A is a high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input ( $\overline{OE}$  ).

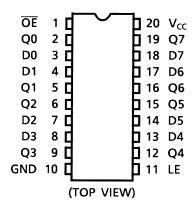
When the  $\overline{\rm OE}$  input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

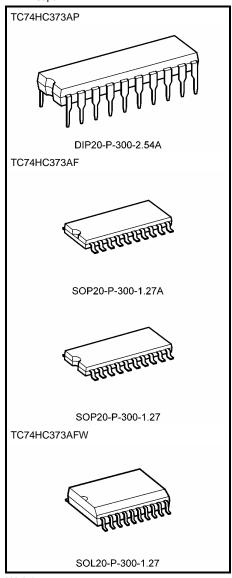
#### **Features**

- High speed:  $t_{pd} = 11 \text{ ns (typ.)}$  at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $ICC = 4 \mu A \text{ (max)}$  at  $Ta = 25^{\circ}C$
- High noise immunity: VNIH = VNIL = 28% VCC (min)
- Output drive capability: 15 LSTTL loads
- Symmetrical output impedance: |IOH| = IOL = 6 mA (min)
- Balanced propagation delays:  $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: VCC (opr) = 2 to 6 V
- Pin and function compatible with 74LS373

#### **Pin Assignment**



Note: xxxFW (JEDEC SOP) is not available in Japan.



Weight

DIP20-P-300-2.54A : 1.30 g (typ.) SOP20-P-300-1.27A : 0.22 g (typ.) SOP20-P-300-1.27 : 0.22 g (typ.) SOL20-P-300-1.27 : 0.46 g (typ.)



# **IEC Logic Symbol**

OE (1) LE (11)	EN C1		
D0 (3) D1 (4) D2 (7) D3 (8) D4 (13) D5 (14) D6 (17) D7 (18)	1D	▷ ♡	(2) Q0 (5) Q1 (6) Q2 (9) Q3 (12) Q4 (15) Q5 (16) Q6 (19) Q7

#### **Truth Table**

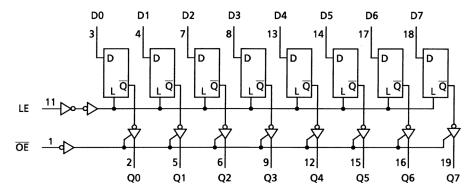
	Inputs					
ŌE	LE	D	Q			
Н	Х	Х	Z			
L	L	Х	Q <sub>n</sub>			
L	Н	L	L			
L	Н	Н	Н			

X: Don't care

Z: High impedance

Q<sub>n</sub>: Q outputs are latched at the time when the LE input is taken to a low logic level.

### **System Diagram**





### **Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	V <sub>CC</sub>	-0.5 to 7	V
DC input voltage	V <sub>IN</sub>	-0.5 to V <sub>CC</sub> + 0.5	V
DC output voltage	V <sub>OUT</sub>	−0.5 to V <sub>CC</sub> + 0.5	V
Input diode current	I <sub>IK</sub>	±20	mA
Output diode current	I <sub>OK</sub>	±20	mA
DC output current	lout	±35	mA
DC V <sub>CC</sub> /ground current	Icc	±75	mA
Power dissipation	P <sub>D</sub>	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T <sub>stg</sub>	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Note 2: 500 mW in the range of Ta = -40 to 65°C. From Ta = 65 to 85°C a derating factor of -10 mW/°C shall be applied until 300 mW.

### **Recommended Operating Conditions (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	Vcc	2 to 6	V
Input voltage	V <sub>IN</sub>	0 to V <sub>CC</sub>	V
Output voltage	V <sub>OUT</sub>	0 to V <sub>CC</sub>	V
Operating temperature	T <sub>opr</sub>	-40 to 85	°C
		0 to 1000 (V <sub>CC</sub> = 2.0 V)	
Input rise and fall time	t <sub>r</sub> , t <sub>f</sub>	0 to 500 (V <sub>CC</sub> = 4.5 V)	ns
		0 to 400 (V <sub>CC</sub> = 6.0 V)	

Note: The recommended operating conditions are required to ensure the normal operation of the device.

Unused inputs must be tied to either VCC or GND.



# **Electrical Characteristics**

#### **DC Characteristics**

Characteristics	Test Condition			Ta = 25°C		Ta = -40 to 85°C		Unit		
	,			V <sub>CC</sub> (V)	Min	Тур.	Max	Min	Max	
				2.0	1.50	_	_	1.50	_	
High-level input voltage	V <sub>IH</sub>		_	4.5	3.15	_	_	3.15	_	V
ű				6.0	4.20	_	_	4.20	_	
				2.0	_	_	0.50	_	0.50	
Low-level input voltage	$V_{IL}$		_	4.5	_	_	1.35	_	1.35	V
_				6.0		_	1.80	_	1.80	
				2.0	1.9	2.0	_	1.9	_	
			$I_{OH} = -20 \mu A$	4.5	4.4	4.5	_	4.4	_	
High-level output voltage	Voн	VIN = VIH or VIL		6.0	5.9	6.0		5.9	_	V
			$I_{OH} = -6 \text{ mA}$	4.5	4.18	4.31	_	4.13	_	
			$I_{OH} = -7.8 \text{ mA}$	6.0	5.68	5.80	_	5.63	_	
		V <sub>OL</sub> V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> .		2.0	_	0.0	0.1	_	0.1	V
			$I_{OL}=20~\mu A$	4.5	_	0.0	0.1	_	0.1	
Low-level output voltage	V <sub>OL</sub>			6.0		0.0	0.1	_	0.1	
			$I_{OL} = 6 \text{ mA}$	4.5		0.17	0.26	_	0.33	
			$I_{OL} = 7.8 \text{ mA}$	6.0		0.18	0.26	_	0.33	
3-state output	lo-	$V_{IN} = V_{IH}$ or	V <sub>IL</sub>	6.0		_	±0.5		±5.0	μА
off-state current		$V_{OUT} = V_{CC}$ or GND		0.0	_		±0.5		±3.0	μΑ
Input leakage current	I <sub>IN</sub>	$V_{IN} = V_{CC}$ or GND		6.0		_	±0.1	l	±1.0	μА
Quiescent supply current	Icc	VIN = VCC of	r GND	6.0	_	_	4.0	_	40.0	μА

#### Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40 to 85°C	Unit
			V <sub>CC</sub> (V)	Тур.	Limit	Limit	
Minimum pulse width			2.0	_	75	95	
(LE)	t <sub>W (H)</sub>	_	4.5	_	15	19	ns
			6.0	_	13	16	
Minimum set-up time			2.0	_	50	65	
•	ts	_	4.5	_	10	13	ns
(Dn)			6.0		9	11	
Minimum hold time			2.0	_	5	5	
(Dn)	t <sub>h</sub>	_	4.5	_	5	5	ns
(DII)			6.0	_	5	5	



#### AC Characteristics (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition Ta = 25°C					Ta = -40 to 85°C				
	,		CL (pF)	V <sub>CC</sub> (V)	Min	Тур.	Max	Min	Max		
Output transition time	t <sub>TLH</sub>	_	50	2.0 4.5	_ _	20 6	60 12	_	75 15	ns	
				6.0	_	5	10	_			
				2.0	_	42	125	_	155		
Propagation delay			50	4.5	_	14	25	_	31		
time	t <sub>pLH</sub>	_		6.0	_	12	21	_	26	ns	
(LE-Q)	$t_{pHL}$			2.0	_	57	175	_	220		
			150	4.5	_	19	35	_	44		
				6.0	_	16	30	_	37		
				2.0	_	42	125	_	155	200	
			50	4.5	_	14	25	_	31		
Propagation delay time	t <sub>pLH</sub>			6.0	_	12	21	_	26		
(D-Q)	tpHL	_		2.0	_	57	175	_	220	113	
,			150	4.5	_	19	35	_	44		
				6.0	_	16	30	_	Min         Max           —         75           —         15           —         13           —         155           —         31           —         26           —         220           —         44           —         37           —         26           —         220           —         44           —         37           —         26           —         220           —         44           —         37           —         155           —         31           —         26           —         31           —         26           —         10           —         -           —         -           —         10           —         -		
					2.0		39	125	_	155	
			50	4.5	_	13	25	_	31		
	t <sub>pZL</sub>			6.0	_	11	21	_	26		
Output enable time	t <sub>p</sub> ZH	$R_L = 1 \text{ k}\Omega$		2.0	_	54	175	_	220	ns	
			150	4.5	_	18	35	_	44		
				6.0	_	15	30	_	37		
				2.0		30	125	_	155		
Output disable time	t <sub>pLZ</sub>	$R_L = 1 \text{ k}\Omega$	50	4.5	_	14	25	_	31	ns	
	<sup>t</sup> pHZ			6.0	_	13	21	_	26		
Input capacitance	C <sub>IN</sub>	_	_	ı	_	5	10	_	10	pF	
Output capacitance	C <sub>OUT</sub>	_	_		_	10	_	_	_	pF	
Power dissipation capacitance	C <sub>PD</sub> (Note)	_	_		_	38	_	_	_	pF	

Note: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

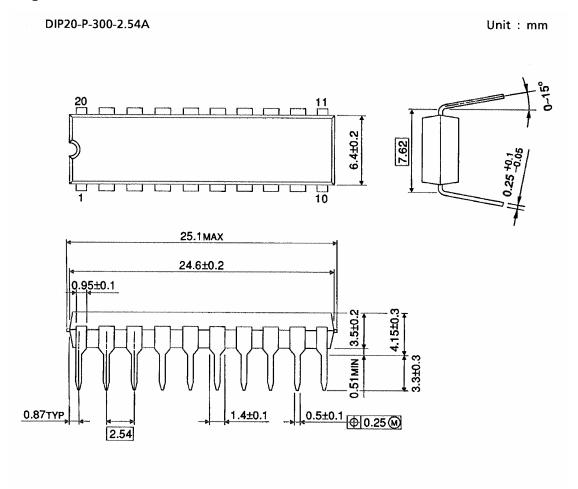
$$I_{CC}$$
 (opr) =  $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$  (per latch)

And the total  $C_{\mbox{\scriptsize PD}}$  when n pcs. of latch operate can be gained by the following equation:

$$C_{PD}$$
 (total) = 22 + 16 · n



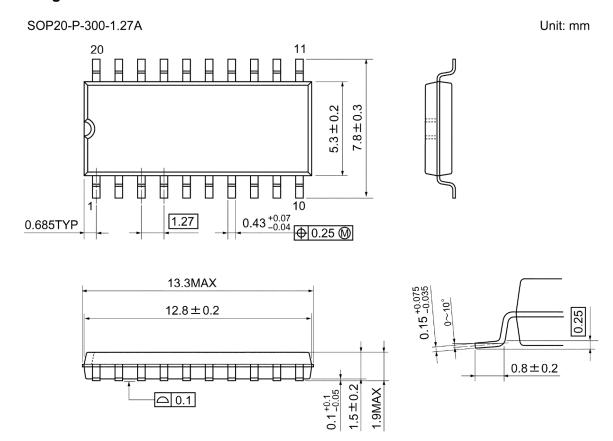
# **Package Dimensions**



Weight: 1.30 g (typ.)



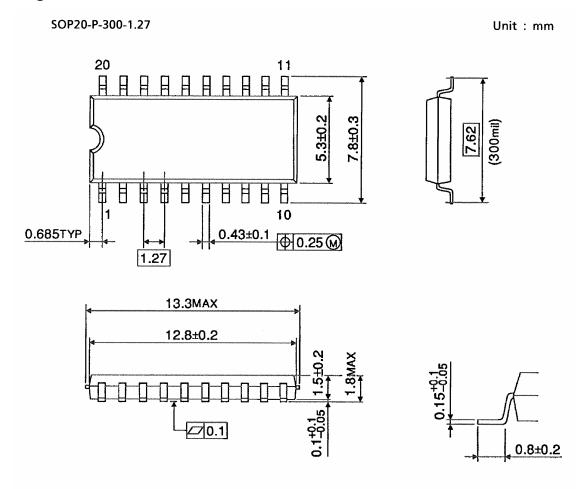
# **Package Dimensions**



Weight: 0.22 g (typ.)



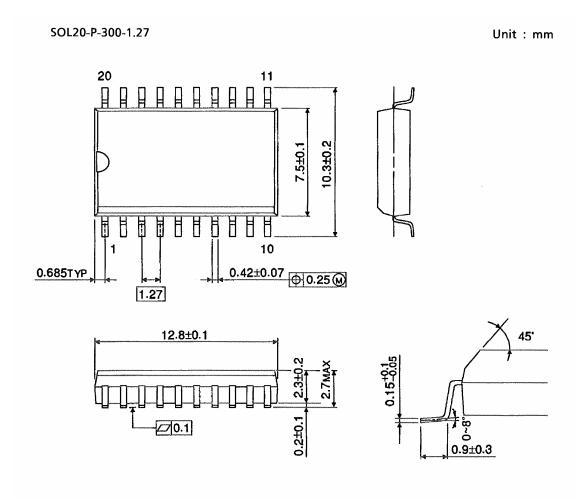
# **Package Dimensions**



Weight: 0.22 g (typ.)



# **Package Dimensions (Note)**



Note: This package is not available in Japan.

Weight: 0.46 g (typ.)

Note: Lead (Pb)-Free Packages

DIP20-P-300-2.54A SOP20-P-300-1.27A

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