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# 1. Overview

These MCUs are fabricated using a high-performance silicon gate CMOS process, embedding the R8C/Tiny Series CPU core, and is packaged in a 20-pin molded-plastic LSSOP, SDIP or a 28-pin plastic molded-HWQFN. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.
Furthermore, the R8C/19 Group has on-chip data flash ROM (1 KB × 2 blocks).
The difference between the R8C/18 Group and R8C/19 Group is only the presence or absence of data flash ROM. Their peripheral functions are the same.

## 1.1 Applications

Electric household appliances, office equipment, housing equipment (sensors, security systems), general industrial equipment, audio equipment, etc.



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## 1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/18 Group and Table 1.2 outlines the Functions and Specifications for R8C/19 Group.

**Table 1.1 Functions and Specifications for R8C/18 Group**

| Item | | Specification |
|---|---|---|
| CPU | Number of fundamental instructions | 89 instructions |
| | Minimum instruction execution time | 50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V)<br>100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) |
| | Operation mode | Single-chip |
| | Address space | 1 Mbyte |
| | Memory capacity | Refer to **Table 1.3 Product Information for R8C/18 Group** |
| Peripheral Functions | Ports | I/O ports: 13 pins (including LED drive port)<br>Input port: 3 pins |
| | LED drive ports | I/O ports: 4 pins |
| | Timers | Timer X: 8 bits × 1 channel, timer Z: 8 bits × 1 channel<br>(Each timer equipped with 8-bit prescaler)<br>Timer C: 16 bits × 1 channel<br>(Input capture and output compare circuits) |
| | Serial interfaces | 1 channel<br>Clock synchronous serial I/O, UART<br>1 channel<br>UART |
| | Comparator | 1-bit comparator: 1 circuit, 4 channels |
| | Watchdog timer | 15 bits × 1 channel (with prescaler)<br>Reset start selectable, count source protection mode |
| | Interrupts | Internal: 10 sources, External: 4 sources, Software: 4 sources,<br>Priority levels: 7 levels |
| | Clock generation circuits | 2 circuits<br>• Main clock oscillation circuit (with on-chip feedback resistor)<br>• On-chip oscillator (high speed, low speed)<br>High-speed on-chip oscillator has frequency adjustment function |
| | Oscillation stop detection function | Main clock oscillation stop detection function |
| | Voltage detection circuit | On-chip |
| | Power-on reset circuit | On-chip |
| Electric Characteristics | Supply voltage | VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz)<br>VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) |
| | Current consumption | Typ. 9 mA (VCC = 5.0 V, f(XIN) = 20 MHz, comparator stopped)<br>Typ. 5 mA (VCC = 3.0V, f(XIN) = 10 MHz, comparator stopped)<br>Typ. 35 μA (VCC = 3.0 V, wait mode, peripheral clock off)<br>Typ. 0.7 μA (VCC = 3.0 V, stop mode) |
| Flash Memory | Programming and erasure voltage | VCC = 2.7 to 5.5 V |
| | Programming and erasure endurance | 100 times |
| Operating Ambient Temperature | | -20 to 85°C<br>-40 to 85°C (D version) |
| Package | | 20-pin molded-plastic LSSOP |
| | | 20-pin molded-plastic SDIP |
| | | 28-pin molded-plastic HWQFN |



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**Table 1.2 Functions and Specifications for R8C/19 Group**

| Item | | Specification |
|---|---|---|
| CPU | Number of fundamental instructions | 89 instructions |
| | Minimum instruction execution time | 50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V)<br>100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) |
| | Operation mode | Single-chip |
| | Address space | 1 Mbyte |
| | Memory capacity | Refer to **Table 1.4 Product Information for R8C/19 Group** |
| Peripheral Functions | Ports | I/O ports: 13 pins (including LED drive port)<br>Input port: 3 pins |
| | LED drive ports | I/O ports: 4 pins |
| | Timers | Timer X: 8 bits × 1 channel, timer Z: 8 bits × 1 channel<br>(Each timer equipped with 8-bit prescaler)<br>Timer C: 16 bits × 1 channel<br>(Input capture and output compare circuits) |
| | Serial interfaces | 1 channel<br>Clock synchronous serial I/O, UART<br>1 channel<br>UART |
| | Comparator | 1-bit comparator: 1 circuit, 4 channels |
| | Watchdog timer | 15 bits × 1 channel (with prescaler)<br>Reset start selectable, count source protection mode |
| | Interrupts | Internal: 10 sources, External: 4 sources, Software: 4 sources,<br>Priority levels: 7 levels |
| | Clock generation circuits | 2 circuits<br>• Main clock generation circuit (with on-chip feedback resistor)<br>• On-chip oscillator (high speed, low speed)<br>High-speed on-chip oscillator has frequency adjustment function |
| | Oscillation stop detection function | Main clock oscillation stop detection function |
| | Voltage detection circuit | On-chip |
| | Power-on reset circuit | On-chip |
| Electric Characteristics | Supply voltage | VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz)<br>VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) |
| | Current consumption | Typ. 9 mA (VCC = 5.0 V, f(XIN) = 20 MHz, comparator stopped)<br>Typ. 5 mA (VCC = 3.0 V, f(XIN) = 10MHz, comparator stopped)<br>Typ. 35 μA (VCC = 3.0 V, wait mode, peripheral clock off)<br>Typ. 0.7 μA (VCC = 3.0 V, stop mode) |
| Flash Memory | Programming and erasure voltage | VCC = 2.7 to 5.5 V |
| | Programming and erasure endurance | 10,000 times (data flash)<br>1,000 times (program ROM) |
| Operating Ambient Temperature | | -20 to 85°C<br>-40 to 85°C (D version) |
| Package | | 20-pin molded-plastic LSSOP<br>20-pin molded-plastic SDIP<br>28-pin molded-plastic HWQFN |



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## 1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

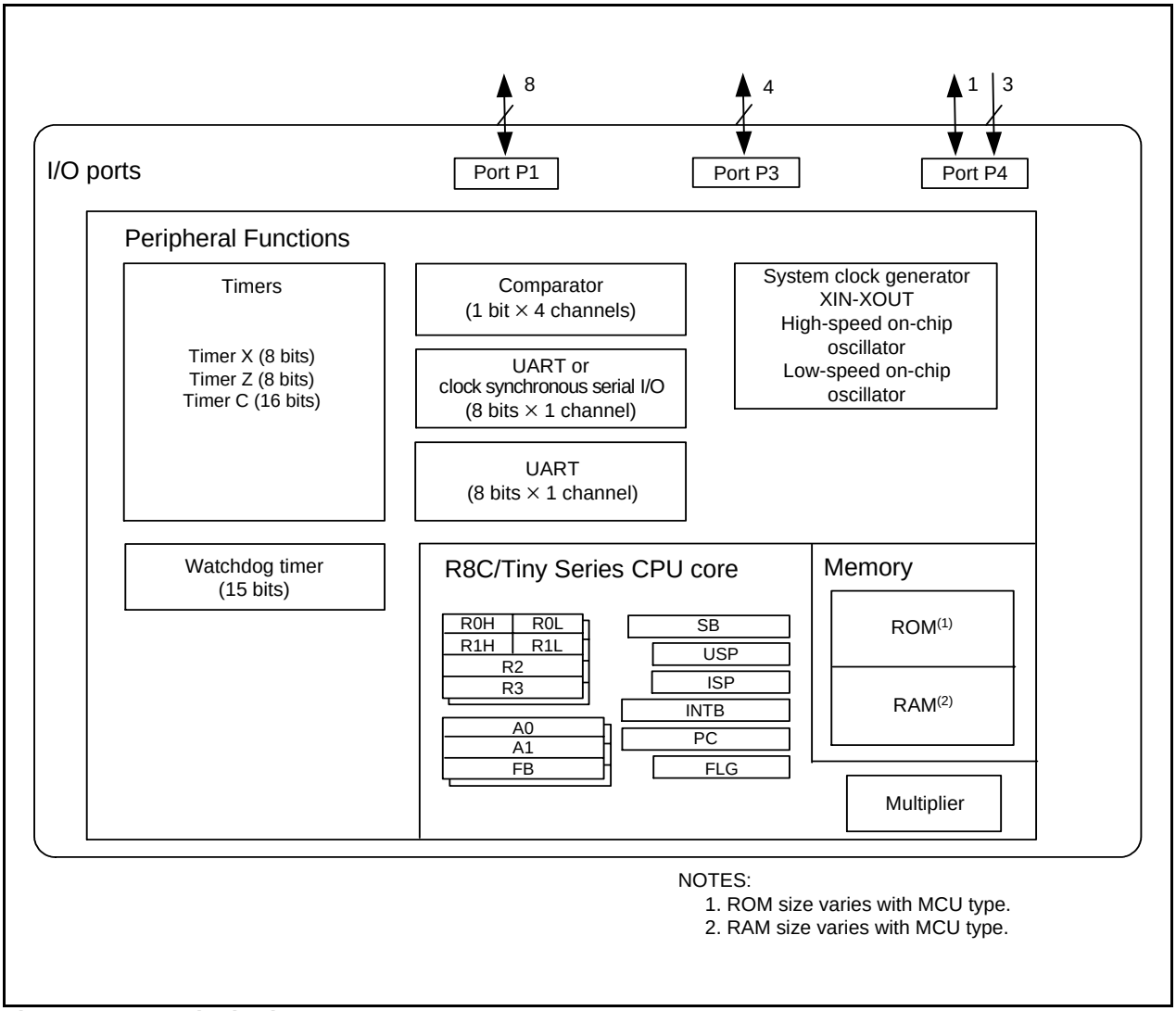



**Figure 1.1 Block Diagram**



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## 1.4 Product Information

Table 1.3 lists Product Information for R8C/18 Group and Table 1.4 lists Product Information for R8C/19 Group.

**Table 1.3 Product Information for R8C/18 Group** **Current of Apr. 2006**

| Type No. | ROM Capacity | RAM Capacity | Package Type | Remarks |
|---|---|---|---|---|
| R5F21181SP | 4 Kbytes | 384 bytes | PLSP0020JB-A | Flash memory version |
| R5F21182SP | 8 Kbytes | 512 bytes | PLSP0020JB-A | |
| R5F21183SP | 12 Kbytes | 768 bytes | PLSP0020JB-A | |
| R5F21184SP | 16 Kbytes | 1 Kbyte | PLSP0020JB-A | |
| R5F21181DSP (D) | 4 Kbytes | 384 bytes | PLSP0020JB-A | D version |
| R5F21182DSP (D) | 8 Kbytes | 512 bytes | PLSP0020JB-A | |
| R5F21183DSP (D) | 12 Kbytes | 768 bytes | PLSP0020JB-A | |
| R5F21184DSP (D) | 16 Kbytes | 1 Kbyte | PLSP0020JB-A | |
| R5F21181DD | 4 Kbytes | 384 bytes | PRDP0020BA-A | Flash memory version |
| R5F21182DD | 8 Kbytes | 512 bytes | PRDP0020BA-A | |
| R5F21183DD | 12 Kbytes | 768 bytes | PRDP0020BA-A | |
| R5F21184DD | 16 Kbytes | 1 Kbyte | PRDP0020BA-A | |
| R5F21182NP | 8 Kbytes | 512 bytes | PWQN0028KA-B | Flash memory version |
| R5F21183NP | 12 Kbytes | 768 bytes | PWQN0028KA-B | |
| R5F21184NP | 16 Kbytes | 1 Kbyte | PWQN0028KA-B | |

(D): Under Development

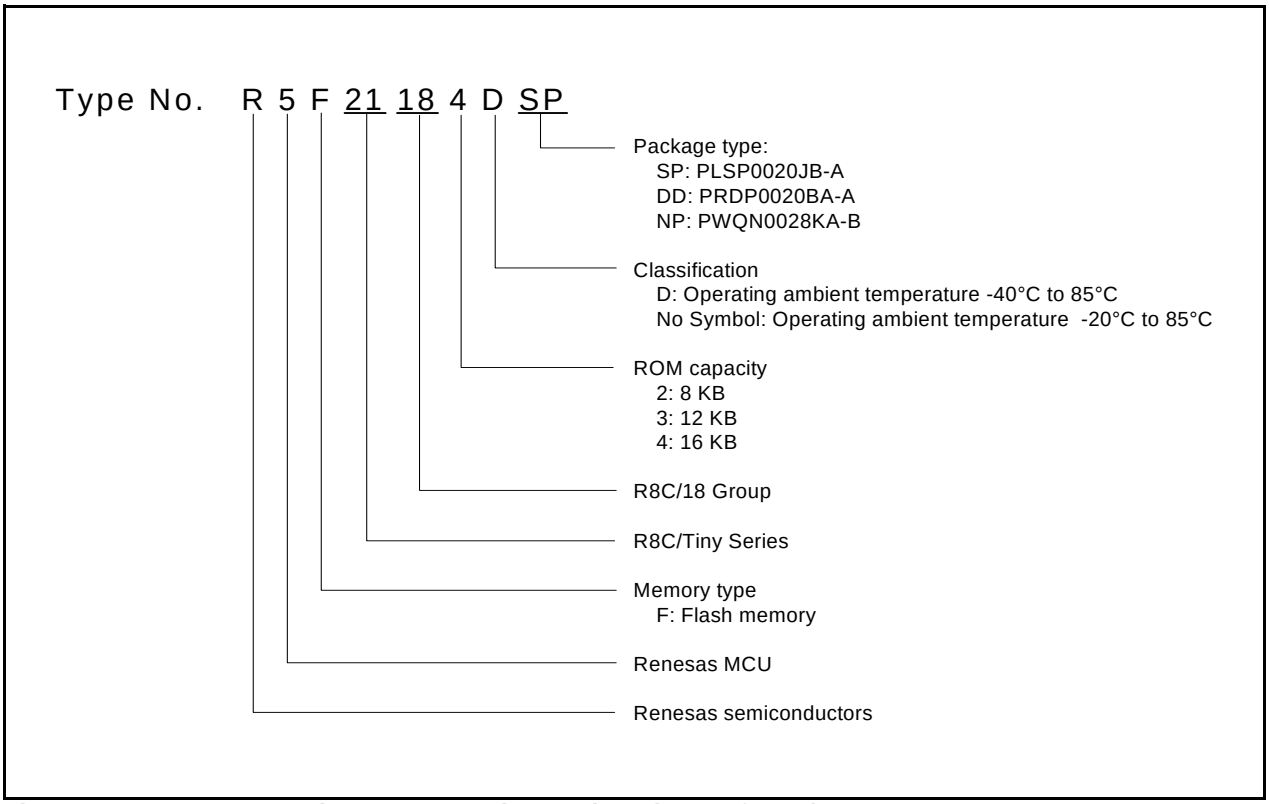



**Figure 1.2 Type Number, Memory Size, and Package of R8C/18 Group**



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**Table 1.4 Product Information for R8C/19 Group Current of Apr. 2006**

| Type No. | ROM Capacity | | RAM Capacity | Package Type | Remarks |
|---|---|---|---|---|---|
| | Program ROM | Data flash | | | |
| R5F21191SP | 4 Kbytes | 1 Kbyte × 2 | 384 bytes | PLSP0020JB-A | Flash memory version |
| R5F21192SP | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | PLSP0020JB-A | |
| R5F21193SP | 12 Kbytes | 1 Kbyte × 2 | 768 bytes | PLSP0020JB-A | |
| R5F21194SP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLSP0020JB-A | |
| R5F21191DSP (D) | 4 Kbytes | 1 Kbyte × 2 | 384 bytes | PLSP0020JB-A | D version |
| R5F21192DSP (D) | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | PLSP0020JB-A | |
| R5F21193DSP (D) | 12 Kbytes | 1 Kbyte × 2 | 768 bytes | PLSP0020JB-A | |
| R5F21194DSP (D) | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PLSP0020JB-A | |
| R5F21191DD | 4 Kbytes | 1 Kbyte × 2 | 384 bytes | PRDP0020BA-A | Flash memory version |
| R5F21192DD | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | PRDP0020BA-A | |
| R5F21193DD | 12 Kbytes | 1 Kbyte × 2 | 768 bytes | PRDP0020BA-A | |
| R5F21194DD | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PRDP0020BA-A | |
| R5F21192NP | 8 Kbytes | 1 Kbyte × 2 | 512 bytes | PWQN0028KA-B | Flash memory version |
| R5F21193NP | 12 Kbytes | 1 Kbyte × 2 | 768 bytes | PWQN0028KA-B | |
| R5F21194NP | 16 Kbytes | 1 Kbyte × 2 | 1 Kbyte | PWQN0028KA-B | |

(D): Under Development

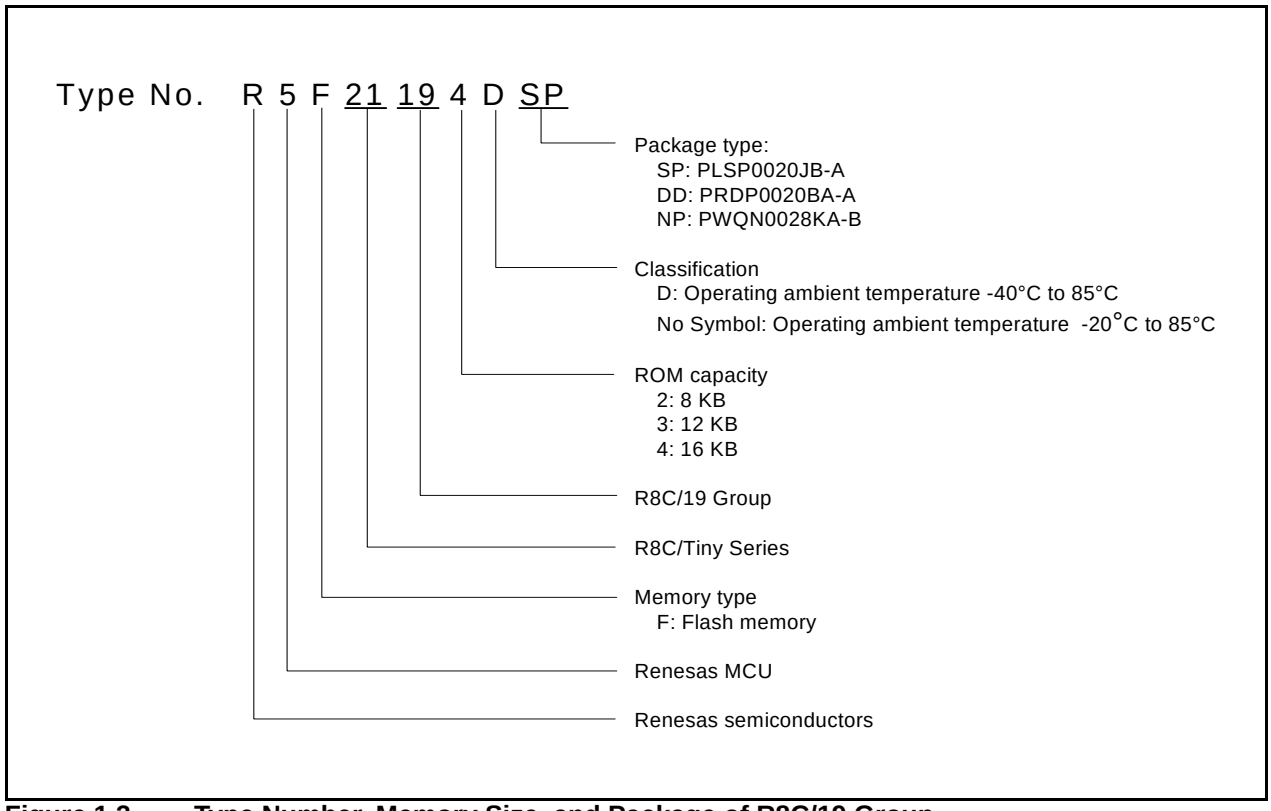



**Figure 1.3 Type Number, Memory Size, and Package of R8C/19 Group**



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## 1.5 Pin Assignments

Figure 1.4 shows Pin Assignments for PLSP0020JB-A Package (Top View), Figure 1.5 shows Pin Assignments for PRDP0020BA-A Package (Top View) and Figure 1.6 shows Pin Assignments for PWQN0028KA-B Package (Top View).

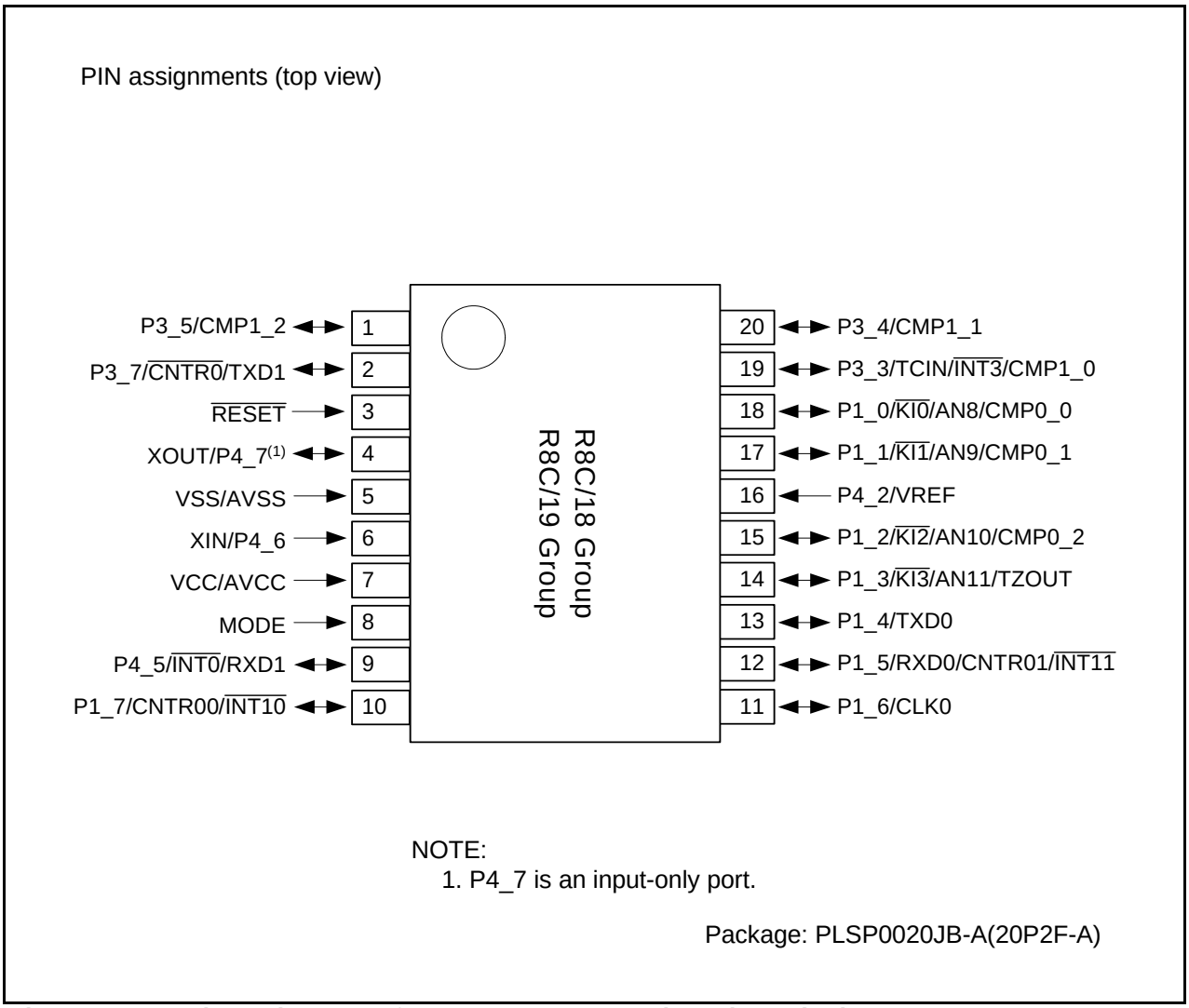



**Figure 1.4 Pin Assignments for PLSP0020JB-A Package (Top View)**



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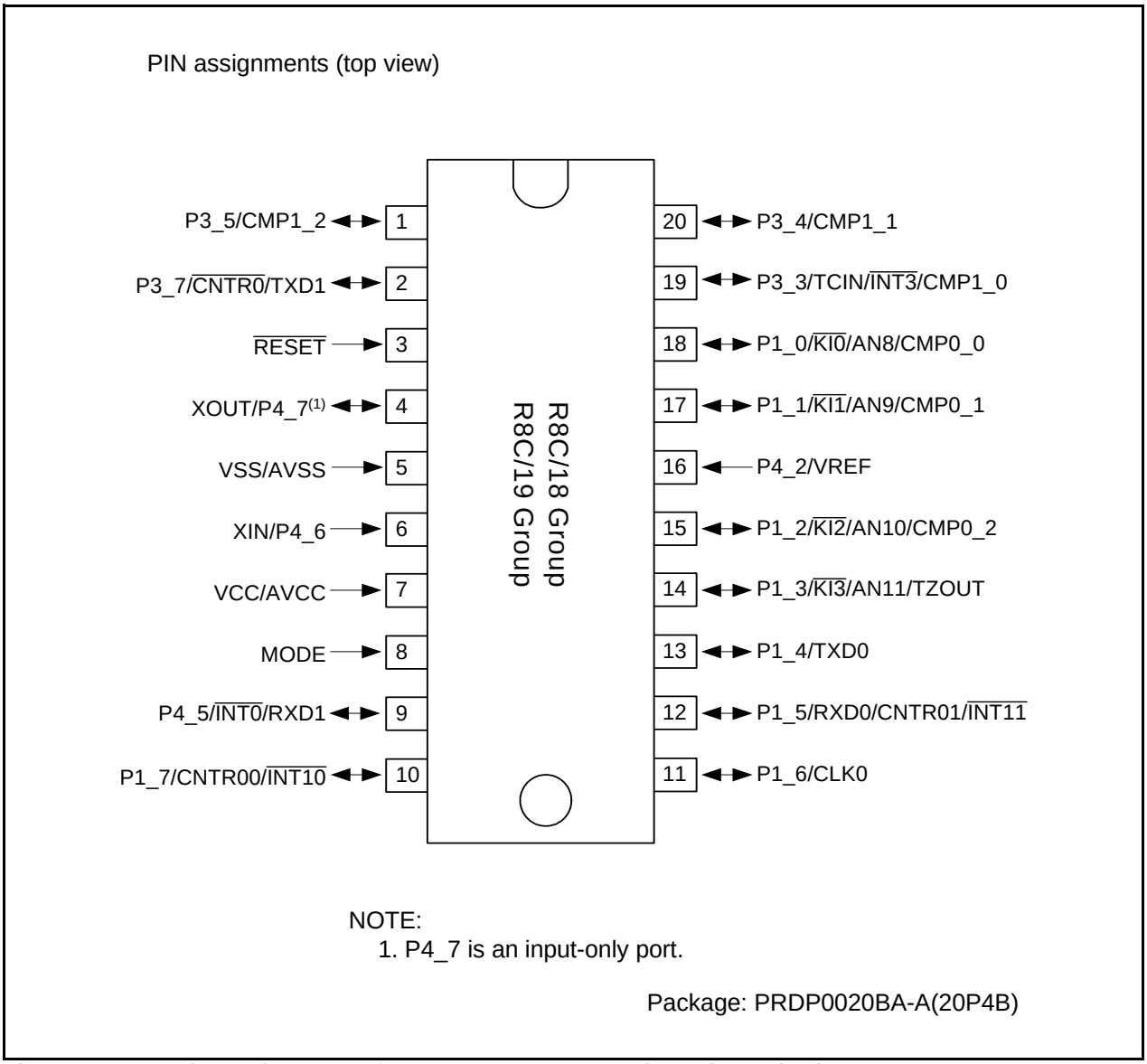
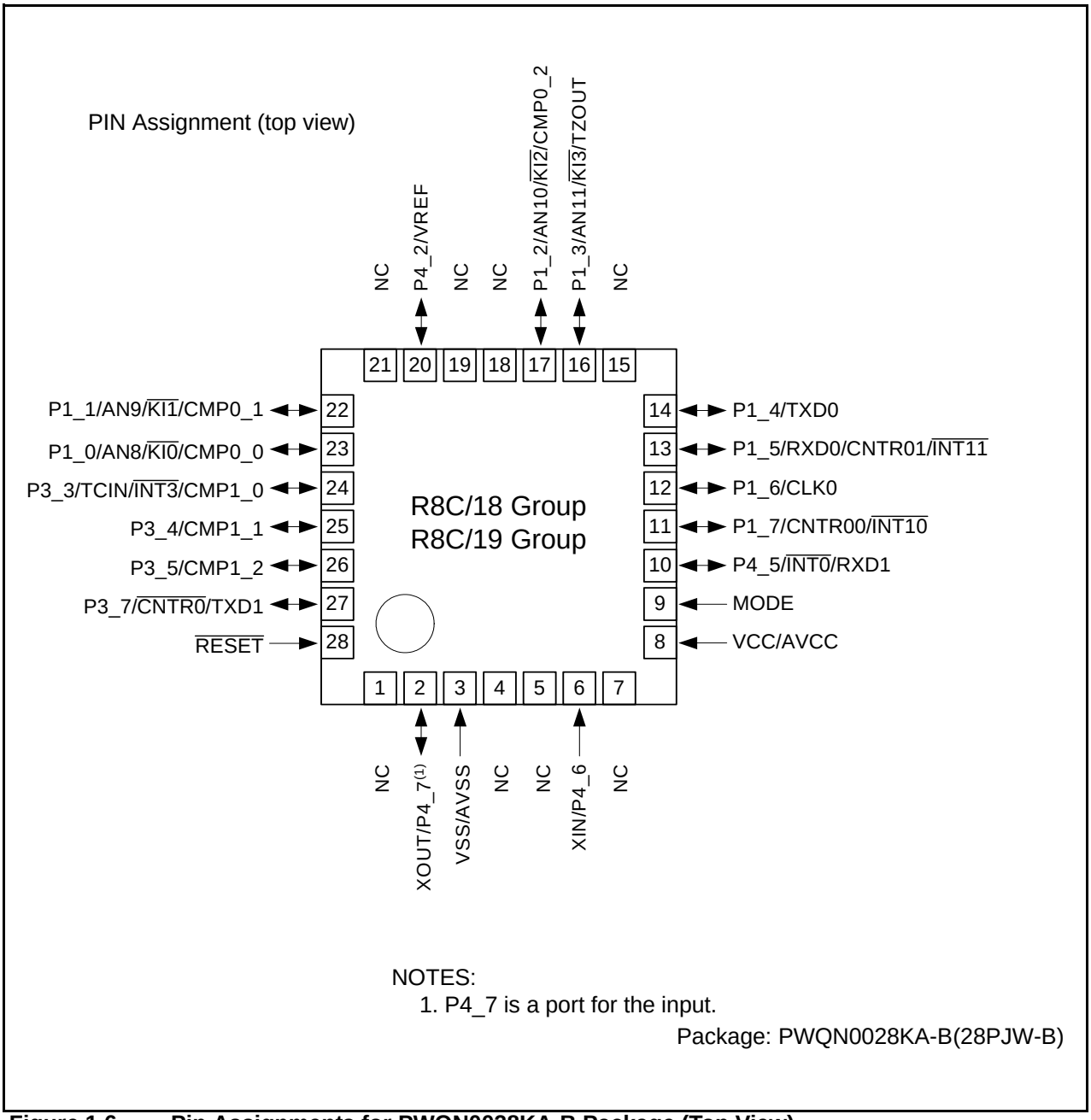



**Figure 1.5 Pin Assignments for PRDP0020BA-A Package (Top View)**



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NOTES:
1. P4_7 is a port for the input.

Package: PWQN0028KA-B(28PJW-B)

**Figure 1.6 Pin Assignments for PWQN0028KA-B Package (Top View)**



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## 1.6 Pin Functions

Table 1.5 lists Pin Functions, Table 1.6 lists Pin Name Information by Pin Number of PLSP0020JB-A, PRDP0020BA-A packages, and Table 1.7 lists Pin Name Information by Pin Number of PWQN0028KA-B package.

**Table 1.5 Pin Functions**

| Type | Symbol | I/O Type | Description |
|---|---|---|---|
| Power supply input | VCC<br>VSS | I | Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin. |
| Analog power supply input | AVCC, AVSS | I | Power supply for the comparator<br>Connect a capacitor between AVCC and AVSS. |
| Reset input | $\overline{\text{RESET}}$ | I | Input “L” on this pin resets the MCU. |
| MODE | MODE | I | Connect this pin to VCC via a resistor. |
| Main clock input | XIN | I | These pins are provided for main clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an external clock, input it to the XIN pin and leave the XOUT pin open. |
| Main clock output | XOUT | O | |
| $\overline{\text{INT}}$ interrupt | $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$ | I | $\overline{\text{INT}}$ interrupt input pins |
| Key input interrupt | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | Key input interrupt input pins |
| Timer X | CNTR0 | I/O | Timer X I/O pin |
| | $\overline{\text{CNTR0}}$ | O | Timer X output pin |
| Timer Z | TZOUT | O | Timer Z output pin |
| Timer C | TCIN | I | Timer C input pin |
| | CMP0_0 to CMP0_2, CMP1_0 to CMP1_2 | O | Timer C output pins |
| Serial interface | CLK0 | I/O | Transfer clock I/O pin |
| | RXD0, RXD1 | I | Serial data input pins |
| | TXD0, TXD1 | O | Serial data output pins |
| Reference voltage input | VREF | I | Reference voltage input pin to comparator |
| Comparator | AN8 to AN11 | I | Analog input pins to comparator |
| I/O port | P1_0 to P1_7, P3_3 to P3_5, P3_7, P4_5 | I/O | CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually.<br>Any port set to input can be set to use a pull-up resistor or not by a program.<br>P1_0 to P1_3 also function as LED drive ports. |
| Input port | P4_2, P4_6, P4_7 | I | Input-only ports |

I: Input O: Output I/O: Input and output



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**Table 1.6 Pin Name Information by Pin Number of PLSP0020JB-A, PRDP0020BA-A packages**

| Pin Number | Control Pin | Port | I/O Pin Functions for Peripheral Modules | | | |
|---|---|---|---|---|---|---|
| | | | Interrupt | Timer | Serial Interface | Comparator |
| 1 | | P3_5 | | CMP1_2 | | |
| 2 | | P3_7 | | $\overline{\text{CNTR0}}$ | TXD1 | |
| 3 | $\overline{\text{RESET}}$ | | | | | |
| 4 | XOUT | P4_7 | | | | |
| 5 | VSS/AVSS | | | | | |
| 6 | XIN | P4_6 | | | | |
| 7 | VCC/AVCC | | | | | |
| 8 | MODE | | | | | |
| 9 | | P4_5 | $\overline{\text{INT0}}$ | | RXD1 | |
| 10 | | P1_7 | $\overline{\text{INT10}}$ | CNTR00 | | |
| 11 | | P1_6 | | | CLK0 | |
| 12 | | P1_5 | $\overline{\text{INT11}}$ | CNTR01 | RXD0 | |
| 13 | | P1_4 | | | TXD0 | |
| 14 | | P1_3 | $\overline{\text{KI3}}$ | TZOUT | | AN11 |
| 15 | | P1_2 | $\overline{\text{KI2}}$ | CMP0_2 | | AN10 |
| 16 | VREF | P4_2 | | | | |
| 17 | | P1_1 | $\overline{\text{KI1}}$ | CMP0_1 | | AN9 |
| 18 | | P1_0 | $\overline{\text{KI0}}$ | CMP0_0 | | AN8 |
| 19 | | P3_3 | $\overline{\text{INT3}}$ | TCIN/CMP1_0 | | |
| 20 | | P3_4 | | CMP1_1 | | |



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**Table 1.7 Pin Name Information by Pin Number of PWQN0028KA-B package**

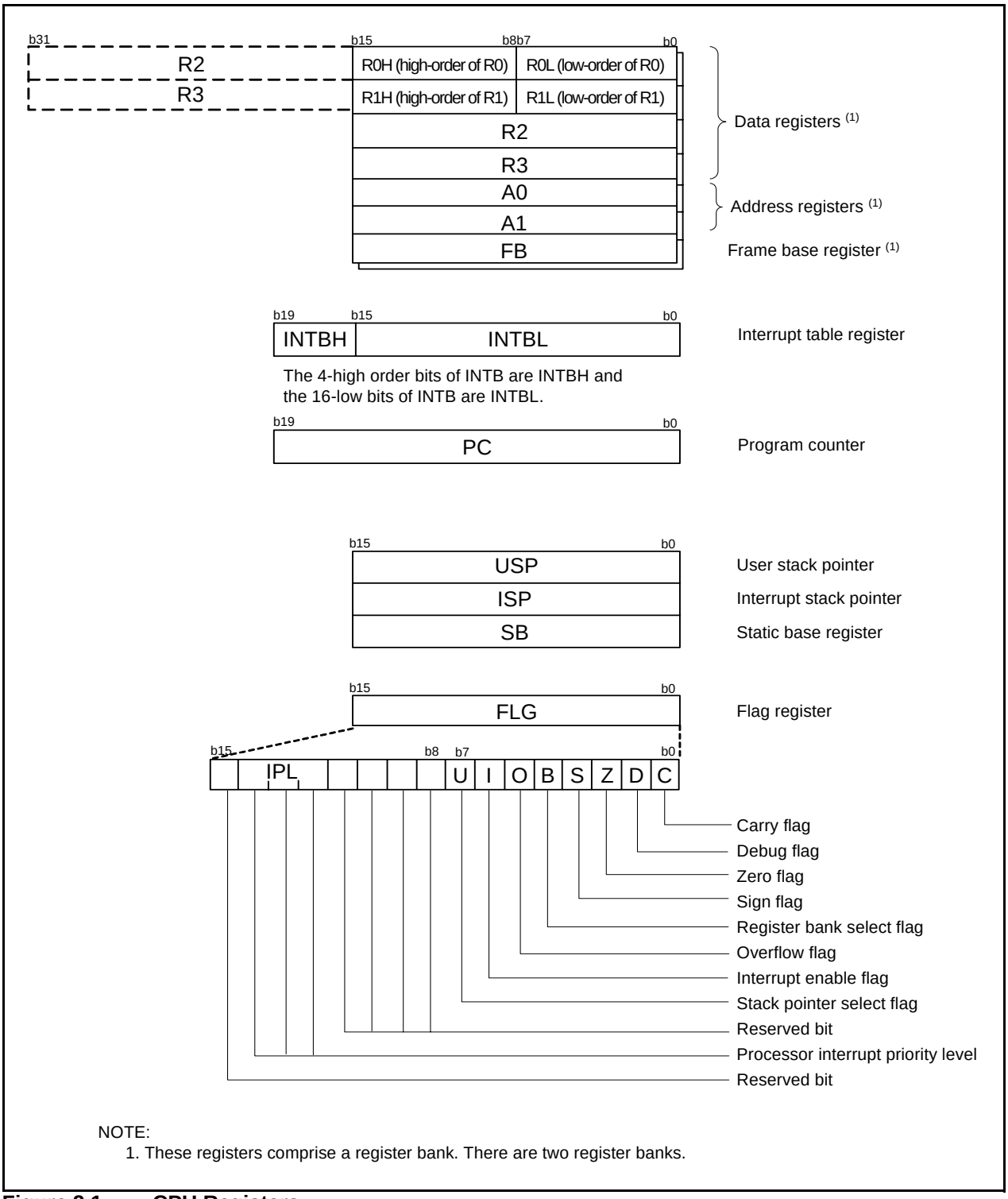
| Pin Number | Control Pin | Port | I/O Pin of Peripheral Function | | | |
|---|---|---|---|---|---|---|
| | | | Interrupt | Timer | Serial Interface | Comparator |
| 1 | NC | | | | | |
| 2 | XOUT | P4_7 | | | | |
| 3 | VSS/AVSS | | | | | |
| 4 | NC | | | | | |
| 5 | NC | | | | | |
| 6 | XIN | P4_6 | | | | |
| 7 | NC | | | | | |
| 8 | VCC/AVCC | | | | | |
| 9 | MODE | | | | | |
| 10 | | P4_5 | $\overline{\text{INT0}}$ | | RXD1 | |
| 11 | | P1_7 | $\overline{\text{INT10}}$ | CNTR00 | | |
| 12 | | P1_6 | | | CLK0 | |
| 13 | | P1_5 | $\overline{\text{INT11}}$ | CNTR01 | RXD0 | |
| 14 | | P1_4 | | | TXD0 | |
| 15 | NC | | | | | |
| 16 | | P1_3 | $\overline{\text{KI3}}$ | TZOUT | | AN11 |
| 17 | | P1_2 | $\overline{\text{KI2}}$ | CMP0_2 | | AN10 |
| 18 | NC | | | | | |
| 19 | NC | | | | | |
| 20 | VREF | P4_2 | | | | |
| 21 | NC | | | | | |
| 22 | | P1_1 | $\overline{\text{KI1}}$ | CMP0_1 | | AN9 |
| 23 | | P1_0 | $\overline{\text{KI0}}$ | CMP0_0 | | AN8 |
| 24 | | P3_3 | $\overline{\text{INT3}}$ | TCIN/CMP1_0 | | |
| 25 | | P3_4 | | CMP1_1 | | |
| 26 | | P3_5 | | CMP1_2 | | |
| 27 | | P3_7 | | $\overline{\text{CNTR0}}$ | TXD1 | |
| 28 | $\overline{\text{RESET}}$ | | | | | |



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# 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.




NOTE:
1. These registers comprise a register bank. There are two register banks.

**Figure 2.1 CPU Registers**



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## 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic and logic operations. A1 is analogous to A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is 20 bits wide, indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when the operation results in an overflow; otherwise to 0.



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### 2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

### 2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

### 2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

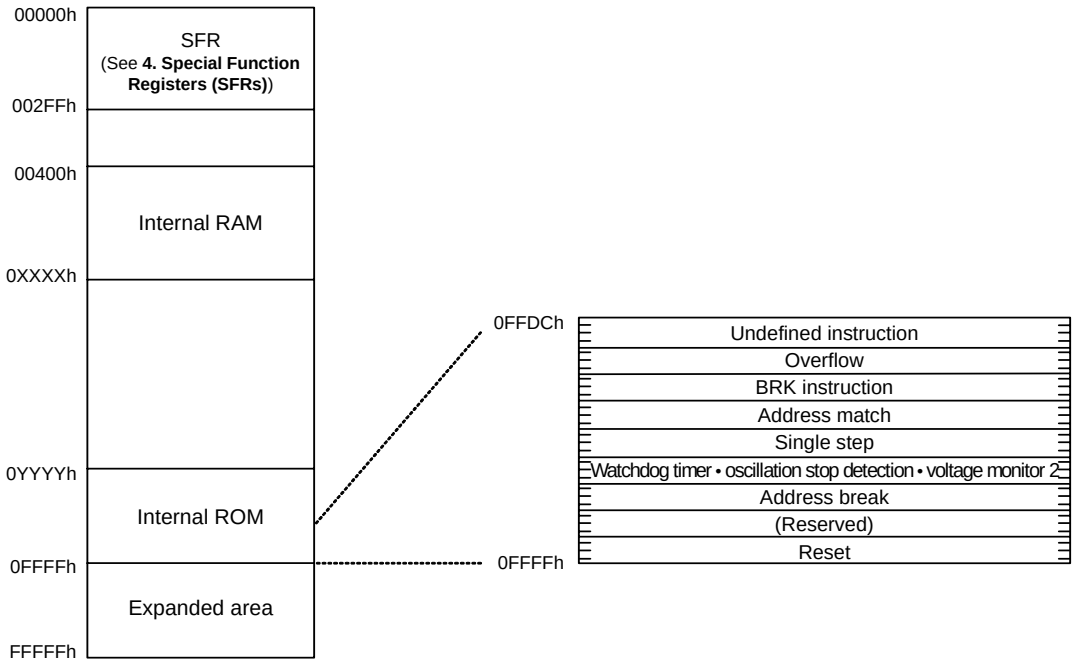


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# 3. Memory

## 3.1 R8C/18 Group

Figure 3.1 is a Memory Map of R8C/18 Group. The R8C/18 Group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM area is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.




NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

| Part Number | Internal ROM | | Internal RAM | |
|---|---|---|---|---|
| | Size | Address 0YYYYh | Size | Address 0XXXXh |
| R5F21184SP, R5F21184DSP, R5F21184DD, R5F21184NP | 16 Kbytes | 0C000h | 1 Kbyte | 007FFh |
| R5F21183SP, R5F21183DSP, R5F21183DD, R5F21183NP | 12 Kbytes | 0D000h | 768 bytes | 006FFh |
| R5F21182SP, R5F21182DSP, R5F21182DD, R5F21182NP | 8 Kbytes | 0E000h | 512 bytes | 005FFh |
| R5F21181SP, R5F21181DSP, R5F21181DD | 4 Kbytes | 0F000h | 384 bytes | 0057Fh |

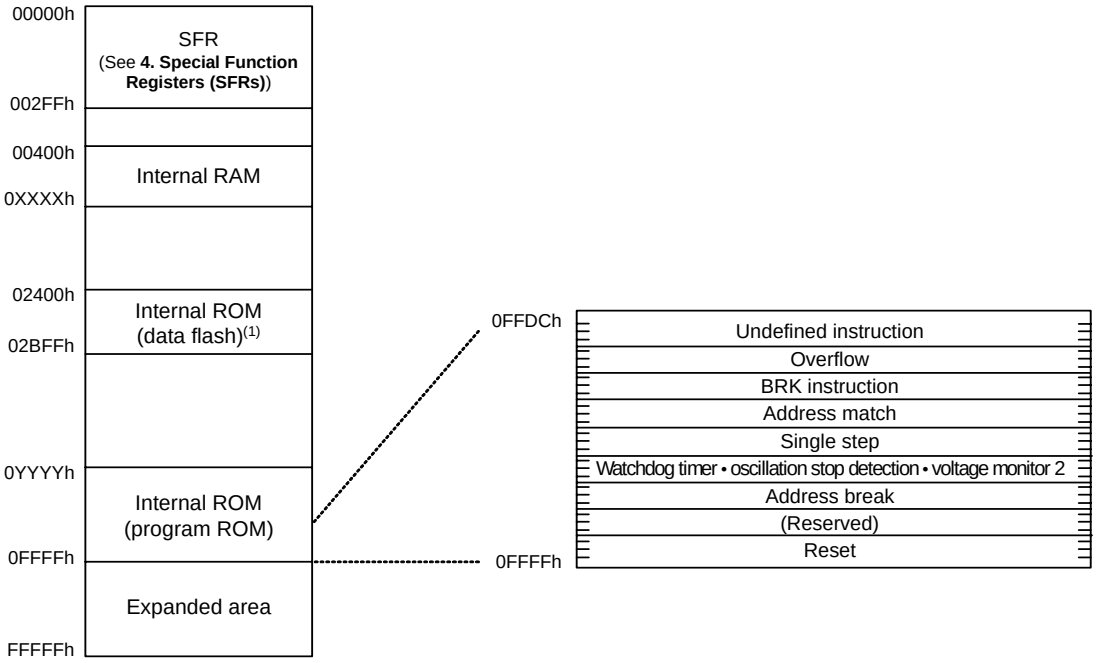
**Figure 3.1 Memory Map of R8C/18 Group**



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## 3.2 R8C/19 Group

Figure 3.2 is a Memory Map of R8C/19 Group. The R8C/19 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.




NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. The blank regions are reserved. Do not access locations in these regions.

| Part Number | Internal ROM | | Internal RAM | |
|---|---|---|---|---|
| | Size | Address 0YYYYh | Size | Address 0XXXXh |
| R5F21194SP, R5F21194DSP, R5F21194DD, R5F21194NP | 16 Kbytes | 0C000h | 1 Kbyte | 007FFh |
| R5F21193SP, R5F21193DSP, R5F21193DD, R5F21193NP | 12 Kbytes | 0D000h | 768 bytes | 006FFh |
| R5F21192SP, R5F21192DSP, R5F21192DD, R5F21192NP | 8 Kbytes | 0E000h | 512 bytes | 005FFh |
| R5F21191SP, R5F21191DSP, R5F21191DD | 4 Kbytes | 0F000h | 384 bytes | 0057Fh |

**Figure 3.2 Memory Map of R8C/19 Group**



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# 4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.4 list the special function registers.

**Table 4.1 SFR Information (1)[1]**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0000h | | | |
| 0001h | | | |
| 0002h | | | |
| 0003h | | | |
| 0004h | Processor Mode Register 0 | PM0 | 00h |
| 0005h | Processor Mode Register 1 | PM1 | 00h |
| 0006h | System Clock Control Register 0 | CM0 | 01101000b |
| 0007h | System Clock Control Register 1 | CM1 | 00100000b |
| 0008h | | | |
| 0009h | Address Match Interrupt Enable Register | AIER | 00h |
| 000Ah | Protect Register | PRCR | 00h |
| 000Bh | | | |
| 000Ch | Oscillation Stop Detection Register | OCD | 00000100b |
| 000Dh | Watchdog Timer Reset Register | WDTR | XXh |
| 000Eh | Watchdog Timer Start Register | WDTS | XXh |
| 000Fh | Watchdog Timer Control Register | WDC | 00011111b |
| 0010h | Address Match Interrupt Register 0 | RMAD0 | 00h |
| 0011h | | | 00h |
| 0012h | | | X0h |
| 0013h | | | |
| 0014h | Address Match Interrupt Register 1 | RMAD1 | 00h |
| 0015h | | | 00h |
| 0016h | | | X0h |
| 0017h | | | |
| 0018h | | | |
| 0019h | | | |
| 001Ah | | | |
| 001Bh | | | |
| 001Ch | Count Source Protection Mode Register | CSPR | 00h |
| 001Dh | | | |
| 001Eh | $\overline{\text{INT0}}$ Input Filter Select Register | INT0F | 00h |
| 001Fh | | | |
| 0020h | High-Speed On-Chip Oscillator Control Register 0 | HRA0 | 00h |
| 0021h | High-Speed On-Chip Oscillator Control Register 1 | HRA1 | When shipping |
| 0022h | High-Speed On-Chip Oscillator Control Register 2 | HRA2 | 00h |
| 0023h | | | |
| | | | |
| 002Ah | | | |
| 002Bh | | | |
| 002Ch | | | |
| 002Dh | | | |
| 002Eh | | | |
| 002Fh | | | |
| 0030h | | | |
| 0031h | Voltage Detection Register 1[2] | VCA1 | 00001000b |
| 0032h | Voltage Detection Register 2[2] | VCA2 | 00h[3]<br>01000000b[4] |
| 0033h | | | |
| 0034h | | | |
| 0035h | | | |
| 0036h | Voltage Monitor 1 Circuit Control Register [2] | VW1C | 0000X000b[3]<br>0100X001b[4] |
| 0037h | Voltage Monitor 2 Circuit Control Register [5] | VW2C | 00h |
| 0038h | | | |
| 0039h | | | |
| 003Ah | | | |
| 003Bh | | | |
| 003Ch | | | |
| 003Dh | | | |
| 003Eh | | | |
| 003Fh | | | |

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect this register.
3. After hardware reset.
4. After power-on reset or voltage monitor 1 reset.
5. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect b2 and b3.



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**Table 4.2 SFR Information (2)(1)**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0040h | | | |
| 0041h | | | |
| 0042h | | | |
| 0043h | | | |
| 0044h | | | |
| 0045h | | | |
| 0046h | | | |
| 0047h | | | |
| 0048h | | | |
| 0049h | | | |
| 004Ah | | | |
| 004Bh | | | |
| 004Ch | | | |
| 004Dh | Key Input Interrupt Control Register | KUPIC | XXXXX000b |
| 004Eh | Comparator Conversion Interrupt Control Register | ADIC | XXXXX000b |
| 004Fh | | | |
| 0050h | Compare 1 Interrupt Control Register | CMP1IC | XXXXX000b |
| 0051h | UART0 Transmit Interrupt Control Register | S0TIC | XXXXX000b |
| 0052h | UART0 Receive Interrupt Control Register | S0RIC | XXXXX000b |
| 0053h | UART1 Transmit Interrupt Control Register | S1TIC | XXXXX000b |
| 0054h | UART1 Receive Interrupt Control Register | S1RIC | XXXXX000b |
| 0055h | | | |
| 0056h | Timer X Interrupt Control Register | TXIC | XXXXX000b |
| 0057h | | | |
| 0058h | Timer Z Interrupt Control Register | TZIC | XXXXX000b |
| 0059h | $\overline{\text{INT1}}$ Interrupt Control Register | INT1IC | XXXXX000b |
| 005Ah | $\overline{\text{INT3}}$ Interrupt Control Register | INT3IC | XXXXX000b |
| 005Bh | Timer C Interrupt Control Register | TCIC | XXXXX000b |
| 005Ch | Compare 0 Interrupt Control Register | CMP0IC | XXXXX000b |
| 005Dh | $\overline{\text{INT0}}$ Interrupt Control Register | INT0IC | XX00X000b |
| 005Eh | | | |
| 005Fh | | | |
| 0060h | | | |
| 0061h | | | |
| 0062h | | | |
| 0063h | | | |
| 0064h | | | |
| 0065h | | | |
| 0066h | | | |
| 0067h | | | |
| 0068h | | | |
| 0069h | | | |
| 006Ah | | | |
| 006Bh | | | |
| 006Ch | | | |
| 006Dh | | | |
| 006Eh | | | |
| 006Fh | | | |
| 0070h | | | |
| 0071h | | | |
| 0072h | | | |
| 0073h | | | |
| 0074h | | | |
| 0075h | | | |
| 0076h | | | |
| 0077h | | | |
| 0078h | | | |
| 0079h | | | |
| 007Ah | | | |
| 007Bh | | | |
| 007Ch | | | |
| 007Dh | | | |
| 007Eh | | | |
| 007Fh | | | |

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.



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**Table 4.3 SFR Information (3)(1)**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0080h | Timer Z Mode Register | TZMR | 00h |
| 0081h | | | |
| 0082h | | | |
| 0083h | | | |
| 0084h | Timer Z Waveform Output Control Register | PUM | 00h |
| 0085h | Prescaler Z Register | PREZ | FFh |
| 0086h | Timer Z Secondary Register | TZSC | FFh |
| 0087h | Timer Z Primary Register | TZPR | FFh |
| 0088h | | | |
| 0089h | | | |
| 008Ah | Timer Z Output Control Register | TZOC | 00h |
| 008Bh | Timer X Mode Register | TXMR | 00h |
| 008Ch | Prescaler X Register | PREX | FFh |
| 008Dh | Timer X Register | TX | FFh |
| 008Eh | Timer Count Source Setting Register | TCSS | 00h |
| 008Fh | | | |
| 0090h | Timer C Register | TC | 00h |
| 0091h | | | 00h |
| 0092h | | | |
| 0093h | | | |
| 0094h | | | |
| 0095h | | | |
| 0096h | External Input Enable Register | INTEN | 00h |
| 0097h | | | |
| 0098h | Key Input Enable Register | KIEN | 00h |
| 0099h | | | |
| 009Ah | Timer C Control Register 0 | TCC0 | 00h |
| 009Bh | Timer C Control Register 1 | TCC1 | 00h |
| 009Ch | Capture, Compare 0 Register | TM0 | 00h |
| 009Dh | | | 00h(2) |
| 009Eh | Compare 1 Register | TM1 | FFh |
| 009Fh | | | FFh |
| 00A0h | UART0 Transmit/Receive Mode Register | U0MR | 00h |
| 00A1h | UART0 Bit Rate Register | U0BRG | XXh |
| 00A2h | UART0 Transmit Buffer Register | U0TB | XXh |
| 00A3h | | | XXh |
| 00A4h | UART0 Transmit/Receive Control Register 0 | U0C0 | 00001000b |
| 00A5h | UART0 Transmit/Receive Control Register 1 | U0C1 | 00000010b |
| 00A6h | UART0 Receive Buffer Register | U0RB | XXh |
| 00A7h | | | XXh |
| 00A8h | UART1 Transmit/Receive Mode Register | U1MR | 00h |
| 00A9h | UART1 Bit Rate Register | U1BRG | XXh |
| 00AAh | UART1 Transmit Buffer Register | U1TB | XXh |
| 00ABh | | | XXh |
| 00ACh | UART1 Transmit/Receive Control Register 0 | U1C0 | 00001000b |
| 00ADh | UART1 Transmit/Receive Control Register 1 | U1C1 | 00000010b |
| 00AEh | UART1 Receive Buffer Register | U1RB | XXh |
| 00AFh | | | XXh |
| 00B0h | UART Transmit/Receive Control Register 2 | UCON | 00h |
| 00B1h | | | |
| 00B2h | | | |
| 00B3h | | | |
| 00B4h | | | |
| 00B5h | | | |
| 00B6h | | | |
| 00B7h | | | |
| 00B8h | | | |
| 00B9h | | | |
| 00BAh | | | |
| 00BBh | | | |
| 00BCh | | | |
| 00BDh | | | |
| 00BEh | | | |
| 00BFh | | | |

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. When the output compare mode is selected (the TCC13 bit in the TCC1 register = 1), the value is set to FFFF16.



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**Table 4.4 SFR Information (4)(1)**

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 00C0h | A/D Register | AD | XXh |
| 00C1h | | | |
| 00C2h | | | |
| 00C3h | | | |
| 00C4h | | | |
| 00C5h | | | |
| 00C6h | | | |
| 00C7h | | | |
| 00C8h | | | |
| 00C9h | | | |
| 00CAh | | | |
| 00CBh | | | |
| 00CCh | | | |
| 00CDh | | | |
| 00CEh | | | |
| 00CFh | | | |
| 00D0h | | | |
| 00D1h | | | |
| 00D2h | | | |
| 00D3h | | | |
| 00D4h | A/D Control Register 2 | ADCON2 | 00h |
| 00D5h | | | |
| 00D6h | A/D Control Register 0 | ADCON0 | 00000XXXb |
| 00D7h | A/D Control Register 1 | ADCON1 | 00h |
| 00D8h | | | |
| 00D9h | | | |
| 00DAh | | | |
| 00DBh | | | |
| 00DCh | | | |
| 00DDh | | | |
| 00DEh | | | |
| 00DFh | | | |
| 00E0h | | | |
| 00E1h | Port P1 Register | P1 | XXh |
| 00E2h | | | |
| 00E3h | Port P1 Direction Register | PD1 | 00h |
| 00E4h | | | |
| 00E5h | Port P3 Register | P3 | XXh |
| 00E6h | | | |
| 00E7h | Port P3 Direction Register | PD3 | 00h |
| 00E8h | Port P4 Register | P4 | XXh |
| 00E9h | | | |
| 00EAh | Port P4 Direction Register | PD4 | 00h |
| 00EBh | | | |
| 00ECh | | | |
| 00EDh | | | |
| 00EEh | | | |
| 00EFh | | | |
| 00F0h | | | |
| 00F1h | | | |
| 00F2h | | | |
| 00F3h | | | |
| 00F4h | | | |
| 00F5h | | | |
| 00F6h | | | |
| 00F7h | | | |
| 00F8h | | | |
| 00F9h | | | |
| 00FAh | | | |
| 00FBh | | | |
| 00FCh | Pull-Up Control Register 0 | PUR0 | 00XX0000b |
| 00FDh | Pull-Up Control Register 1 | PUR1 | XXXXXX0Xb |
| 00FEh | Port P1 Drive Capacity Control Register | DRR | 00h |
| 00FFh | Timer C Output Control Register | TCOUT | 00h |
| 01B3h | Flash Memory Control Register 4 | FMR4 | 01000000b |
| 01B4h | | | |
| 01B5h | Flash Memory Control Register 1 | FMR1 | 1000000Xb |
| 01B6h | | | |
| 01B7h | Flash Memory Control Register 0 | FMR0 | 00000001b |
| 0FFFFh | Optional Function Select Register | OFS | (Note 2) |

X: Undefined

NOTES:

1. The blank regions, 0100h to 01B2h and 01B8h to 02FFh are all reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.



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# 5. Electrical Characteristics

### Table 5.1 Absolute Maximum Ratings

| Symbol | Parameter | Condition | Rated Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | $V_{CC}$ = $AV_{CC}$ | -0.3 to 6.5 | V |
| $AV_{CC}$ | Analog supply voltage | $V_{CC}$ = $AV_{CC}$ | -0.3 to 6.5 | V |
| $V_I$ | Input voltage | | -0.3 to $V_{CC}$+0.3 | V |
| $V_O$ | Output voltage | | -0.3 to $V_{CC}$+0.3 | V |
| $P_d$ | Power dissipation | $T_{opr}$ = 25°C | 300 | mW |
| $T_{opr}$ | Operating ambient temperature | | -20 to 85 / -40 to 85 (D version) | °C |
| $T_{stg}$ | Storage temperature | | -65 to 150 | °C |

### Table 5.2 Recommended Operating Conditions

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{CC}$ | Supply voltage | | | 2.7 | – | 5.5 | V |
| $AV_{CC}$ | Analog supply voltage | | | – | $V_{CC}$ | – | V |
| $V_{SS}$ | Supply voltage | | | – | 0 | – | V |
| $AV_{SS}$ | Analog supply voltage | | | – | 0 | – | V |
| $V_{IH}$ | Input “H” voltage | | | 0.8$V_{CC}$ | – | $V_{CC}$ | V |
| $V_{IL}$ | Input “L” voltage | | | 0 | – | 0.2$V_{CC}$ | V |
| $I_{OH(sum)}$ | Peak sum output “H” current | Sum of all pins $I_{OH\ (peak)}$ | | – | – | -60 | mA |
| $I_{OH(peak)}$ | Peak output “H” current | | | – | – | -10 | mA |
| $I_{OH(avg)}$ | Average output “H” current | | | – | – | -5 | mA |
| $I_{OL(sum)}$ | Peak sum output “L” currents | Sum of all pins $I_{OL\ (peak)}$ | | – | – | 60 | mA |
| $I_{OL(peak)}$ | Peak output “L” currents | Except P1_0 to P1_3 | | – | – | 10 | mA |
| | | P1_0 to P1_3 | Drive capacity HIGH | – | – | 30 | mA |
| | | | Drive capacity LOW | – | – | 10 | mA |
| $I_{OL(avg)}$ | Average output “L” current | Except P1_0 to P1_3 | | – | – | 5 | mA |
| | | P1_0 to P1_3 | Drive capacity HIGH | – | – | 15 | mA |
| | | | Drive capacity LOW | – | – | 5 | mA |
| $f_{(XIN)}$ | Main clock input oscillation frequency | | 3.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | – | 20 | MHz |
| | | | 2.7 V ≤ $V_{CC}$ < 3.0 V | 0 | – | 10 | MHz |

NOTES:
1. $V_{CC}$ = 2.7 to 5.5 V at $T_{opr}$ = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. Typical values when average output current is 100 ms.



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**Table 5.3 Comparator Characteristics**

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Resolution | | – | – | 1 | Bit |
| – | Absolute accuracy | $\phi_{AD}$ = 10 MHz(3) | – | – | ±20 | mV |
| $t_{conv}$ | Conversion time | $\phi_{AD}$ = 10 MHz(3) | 1 | – | – | µs |
| $V_{ref}$ | Reference voltage | | 0 | – | $AV_{CC}$ | V |
| $V_{IA}$ | Analog input voltage | | 0 | – | $AV_{CC}$ | V |
| – | Comparator conversion operating clock frequency(2) | | 1 | – | 10 | MHz |

NOTES:
1. $V_{CC}$ = 2.7 to 5.5 V at $T_{opr}$ = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. If f1 exceeds 10 MHz, divided f1 and ensure the comparator conversion operating clock frequency ($\phi_{AD}$) is 10 MHz or below.
3. If AVcc is less than 4.2 V, divided f1 and ensure the comparator conversion operating clock frequency ($\phi_{AD}$) is f1/2 or below.

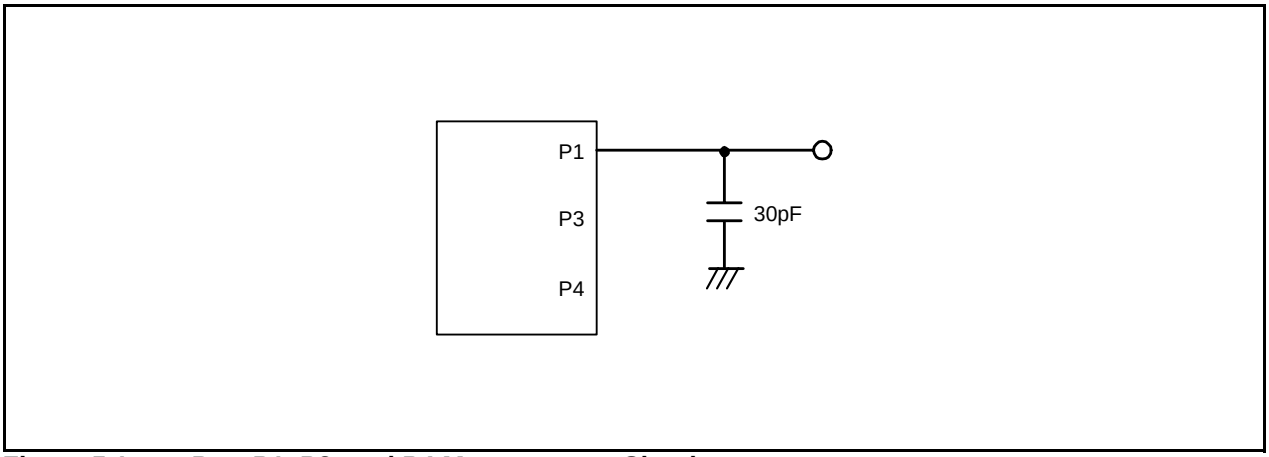



**Figure 5.1 Port P1, P3, and P4 Measurement Circuit**



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**Table 5.4 Flash Memory (Program ROM) Electrical Characteristics**

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance(2) | R8C/18 Group | 100(3) | – | – | times |
| | | R8C/19 Group | 1,000(3) | – | – | times |
| – | Byte program time | | – | 50 | 400 | µs |
| – | Block erase time | | – | 0.4 | 9 | s |
| $t_{d(SR-SUS)}$ | Time delay from suspend request until suspend | | – | – | 97+CPU clock × 6 cycles | µs |
| – | Interval from erase start/restart until following suspend request | | 650 | – | – | µs |
| – | Interval from program start/restart until following suspend request | | 0 | – | – | ns |
| – | Time from suspend until program/erase restart | | – | – | 3+CPU clock × 4 cycles | µs |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.7 | – | 5.5 | V |
| – | Program, erase temperature | | 0 | – | 60 | °C |
| – | Data hold time(8) | Ambient temperature = 55 °C | 20 | – | – | year |

NOTES:
1. $V_{CC}$ = 2.7 to 5.5 V at $T_{opr}$ = 0 to 60 °C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. If emergency processing is required, a suspend request can be generated independent of this characteristic. In that case the normal time delay to Suspend can be applied to the request.However, we recommend that a suspend request with an interval of less than 650 µs is only used once because, if the suspend state continues, erasure cannot operate and the incidence of erasure error rises.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the number of erase operations between block A and block B can further reduce the effective number of rewrites. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring programming/erasure failure rate information should contact their Renesas technical support representative.
8. The data hold time includes time that the power supply is off or the clock is not supplied.



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**Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics**

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance(2) | | 10,000(3) | – | – | times |
| – | Byte program time (Program/erase endurance ≤ 1,000 times) | | – | 50 | 400 | µs |
| – | Byte program time (Program/erase endurance > 1,000 times) | | – | 65 | – | µs |
| – | Block erase time (Program/erase endurance ≤ 1,000 times) | | – | 0.2 | 9 | s |
| – | Block erase time (Program/erase endurance > 1,000 times) | | – | 0.3 | – | s |
| $t_{d(SR-SUS)}$ | Time delay from suspend request until suspend | | – | – | 97+CPU clock × 6 cycles | µs |
| – | Interval from erase start/restart until following suspend request | | 650 | – | – | µs |
| – | Interval from program start/restart until following suspend request | | 0 | – | – | ns |
| – | Time from suspend until program/erase restart | | – | – | 3+CPU clock × 4 cycles | µs |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.7 | – | 5.5 | V |
| – | Program, erase temperature | | -20(8) | – | 85 | °C |
| – | Data hold time(9) | Ambient temperature = 55 °C | 20 | – | – | year |

NOTES:
1. $V_{CC}$ = 2.7 to 5.5 V at $T_{opr}$ = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. If emergency processing is required, a suspend request can be generated independent of this characteristic. In that case the normal time delay to suspend can be applied to the request. However, we recommend that a suspend request with an interval of less than 650 µs is only used once because, if the suspend state continues, erasure cannot operate and the incidence of erasure error rises.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring programming/erasure failure rate information should contact their Renesas technical support representative.
8. -40 °C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

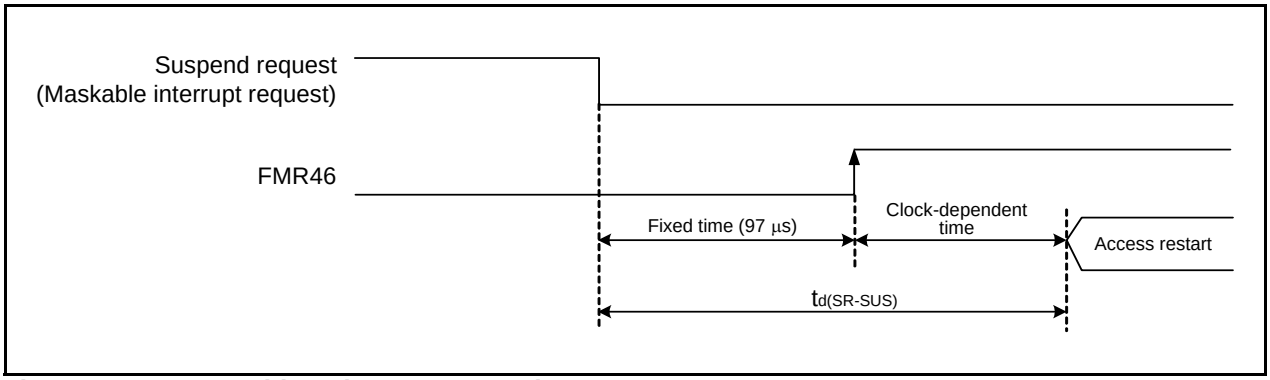



**Figure 5.2 Transition Time to Suspend**



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### Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det1}$ | Voltage detection level(3) | | 2.70 | 2.85 | 3.00 | V |
| – | Voltage detection circuit self power consumption | VCA26 = 1, $V_{CC}$ = 5.0 V | – | 600 | – | nA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts(2) | | – | – | 100 | µs |
| Vccmin | MCU operating voltage minimum value | | 2.7 | – | – | V |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.7 V to 5.5 V and $T_{opr}$ = -40°C to 85 °C.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
3. Ensure that $V_{det2} > V_{det1}$.

### Table 5.7 Voltage Detection 2 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det2}$ | Voltage detection level(4) | | 3.00 | 3.30 | 3.60 | V |
| – | Voltage monitor 2 interrupt request generation time(2) | | – | 40 | – | µs |
| – | Voltage detection circuit self power consumption | VCA27 = 1, $V_{CC}$ = 5.0 V | – | 600 | – | nA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts(3) | | – | – | 100 | µs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.7 V to 5.5 V and $T_{opr}$ = -40°C to 85 °C.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes $V_{det1}$.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
4. Ensure that $V_{det2} > V_{det1}$.



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**Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset)**

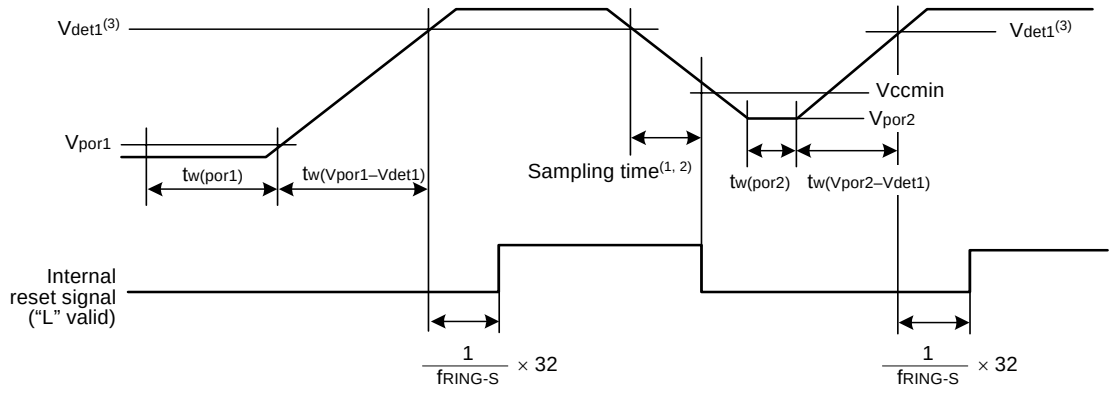
| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{por2}$ | Power-on reset valid voltage | -20°C ≤ Topr ≤ 85°C | – | – | $V_{det1}$ | V |
| $t_{w(Vpor2-Vdet1)}$ | Supply voltage rising time when power-on reset is deasserted(1) | -20°C ≤ Topr ≤ 85°C, $t_{w(por2)}$ ≥ 0s(3) | – | – | 100 | ms |

NOTES:
1. This condition is not applicable when using with Vcc ≥ 1.0 V.
2. When turning power on after the time to hold the external power below effective voltage ($V_{por1}$) exceeds10 s, refer to **Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)**.
3. $t_{w(por2)}$ is the time to hold the external power below effective voltage ($V_{por2}$).

**Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{por1}$ | Power-on reset valid voltage | -20°C ≤ Topr ≤ 85°C | – | – | 0.1 | V |
| $t_{w(Vpor1-Vdet1)}$ | Supply voltage rising time when power-on reset is deasserted | 0°C ≤ Topr ≤ 85°C, $t_{w(por1)}$ ≥ 10 s(2) | – | – | 100 | ms |
| $t_{w(Vpor1-Vdet1)}$ | Supply voltage rising time when power-on reset is deasserted | -20°C ≤ Topr < 0°C, $t_{w(por1)}$ ≥ 30 s(2) | – | – | 100 | ms |
| $t_{w(Vpor1-Vdet1)}$ | Supply voltage rising time when power-on reset is deasserted | -20°C ≤ Topr < 0°C, $t_{w(por1)}$ ≥ 10 s(2) | – | – | 1 | ms |
| $t_{w(Vpor1-Vdet1)}$ | Supply voltage rising time when power-on reset is deasserted | 0°C ≤ Topr ≤ 85°C, $t_{w(por1)}$ ≥ 1 s(2) | – | – | 0.5 | ms |

NOTES:
1. When not using voltage monitor 1, use with Vcc ≥ 2.7 V.
2. $t_{w(por1)}$ is the time to hold the external power below effective voltage ($V_{por1}$).




NOTES:
1. Hold the voltage inside the MCU operation voltage range (Vccmin or above) within the sampling time.
2. The sampling clock can be selected. Refer to **7. Voltage Detection Circuit** for details.
3. $V_{det1}$ indicates the voltage detection level of the voltage detection 1 circuit. Refer to **7. Voltage Detection Circuit** for details.

**Figure 5.3 Reset Circuit Electrical Characteristics**



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### Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | High-speed on-chip oscillator frequency when the reset is deasserted | $V_{CC}$ = 5.0 V, $T_{opr}$ = 25 °C | – | 8 | – | MHz |
| – | High-speed on-chip oscillator frequency temperature supply voltage dependence(2) | 0 to +60 °C/5 V ± 5 %(3) | 7.76 | – | 8.24 | MHz |
| | | -20 to +85 °C/2.7 to 5.5 V(3) | 7.68 | – | 8.32 | MHz |
| | | -40 to +85 °C/2.7 to 5.5 V(3) | 7.44 | – | 8.32 | MHz |

NOTES:
1. The measurement condition is $V_{CC}$ = 5.0 V and $T_{opr}$ = 25 °C.
2. Refer to **10.6.4 High-Speed On-Chip Oscillator Clock** for notes on high-speed on-chip oscillator clock.
3. The standard value shows when the HRA1 register is assumed as the value in shipping and the HRA2 register value is set to 00h.

### Table 5.11 Power Supply Circuit Timing Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{d(P-R)}$ | Time for internal power supply stabilization during power-on(2) | | 1 | – | 2000 | µs |
| $t_{d(R-S)}$ | STOP exit time(3) | | – | – | 150 | µs |

NOTES:
1. The measurement condition is $V_{CC}$ = 2.7 to 5.5 V and $T_{opr}$ = 25 °C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until CPU clock supply starts after the interrupt is acknowledged to exit stop mode.



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**Table 5.12 Electrical Characteristics (1) [Vcc = 5 V]**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| VOH | Output “H” voltage | Except XOUT | IOH = -5 mA | | Vcc – 2.0 | – | Vcc | V |
| | | | IOH = -200 µA | | Vcc – 0.3 | – | Vcc | V |
| | | XOUT | Drive capacity HIGH | IOH = -1 mA | Vcc – 2.0 | – | Vcc | V |
| | | | Drive capacity LOW | IOH = -500 µA | Vcc – 2.0 | – | Vcc | V |
| VOL | Output “L” voltage | Except P1_0 to P1_3, XOUT | IOL = 5 mA | | – | – | 2.0 | V |
| | | | IOL = 200 µA | | – | – | 0.45 | V |
| | | P1_0 to P1_3 | Drive capacity HIGH | IOL = 15 mA | – | – | 2.0 | V |
| | | | Drive capacity LOW | IOL = 5 mA | – | – | 2.0 | V |
| | | | Drive capacity LOW | IOL = 200 µA | – | – | 0.45 | V |
| | | XOUT | Drive capacity HIGH | IOL = 1 mA | – | – | 2.0 | V |
| | | | Drive capacity LOW | IOL = 500 µA | – | – | 2.0 | V |
| VT+-VT- | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, CNTR0, CNTR1, TCIN, RXD0 | | | 0.2 | – | 1.0 | V |
| | | $\overline{RESET}$ | | | 0.2 | – | 2.2 | V |
| IIH | Input “H” current | | VI = 5 V | | – | – | 5.0 | µA |
| IIL | Input “L” current | | VI = 0 V | | – | – | -5.0 | µA |
| RPULLUP | Pull-up resistance | | VI = 0 V | | 30 | 50 | 167 | kΩ |
| RfXIN | Feedback resistance | XIN | | | – | 1.0 | – | MΩ |
| fRING-S | Low-speed on-chip oscillator frequency | | | | 40 | 125 | 250 | kHz |
| VRAM | RAM hold voltage | | During stop mode | | 2.0 | – | – | V |

NOTE:
1. Vcc = 4.2 to 5.5 V at Topr = -20 to 85 °C / -40 to 85 °C, f(XIN) = 20 MHz, unless otherwise specified.



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**Table 5.13 Electrical Characteristics (2) [Vcc = 5 V] (Topr = -40 to 85 °C, unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Icc | Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss, comparator is stopped | High-speed mode | XIN = 20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 9 | 15 | mA |
| | | | XIN = 16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 8 | 14 | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 5 | – | mA |
| | | Medium-speed mode | XIN = 20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 4 | – | mA |
| | | | XIN = 16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 3 | – | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2 | – | mA |
| | | High-speed on-chip oscillator mode | Main clock off<br>High-speed on-chip oscillator on = 8 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 4 | 8 | mA |
| | | | Main clock off<br>High-speed on-chip oscillator on = 8 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 1.5 | – | mA |
| | | Low-speed on-chip oscillator mode | Main clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8<br>FMR47 = 1 | – | 110 | 300 | µA |
| | | Wait mode | Main clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = 0 | – | 40 | 80 | µA |
| | | Wait mode | Main clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = 0 | – | 38 | 76 | µA |
| | | Stop mode | Main clock off, Topr = 25 °C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = 0 | – | 0.8 | 3.0 | µA |



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**Timing Requirements**
**(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Ta = 25 °C) [Vcc = 5 V]**

**Table 5.14 XIN Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 50 | – | ns |
| $t_{WH(XIN)}$ | XIN input “H” width | 25 | – | ns |
| $t_{WL(XIN)}$ | XIN input “L” width | 25 | – | ns |

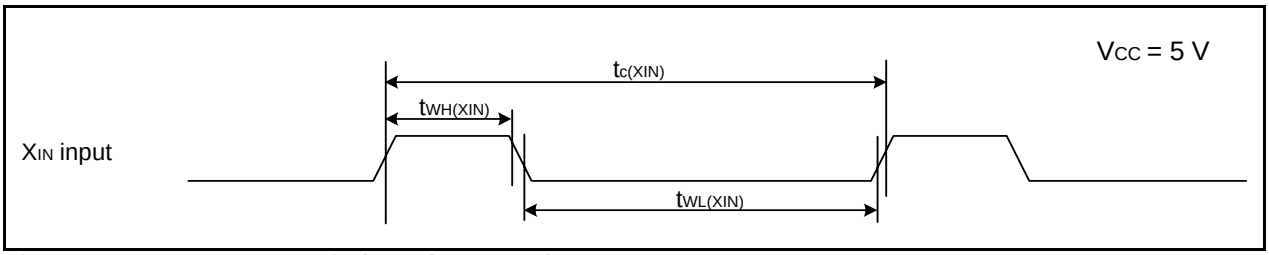



**Figure 5.4 XIN Input Timing Diagram when Vcc = 5 V**

**Table 5.15 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CNTR0)}$ | CNTR0 input cycle time | 100 | – | ns |
| $t_{WH(CNTR0)}$ | CNTR0 input “H” width | 40 | – | ns |
| $t_{WL(CNTR0)}$ | CNTR0 input “L” width | 40 | – | ns |

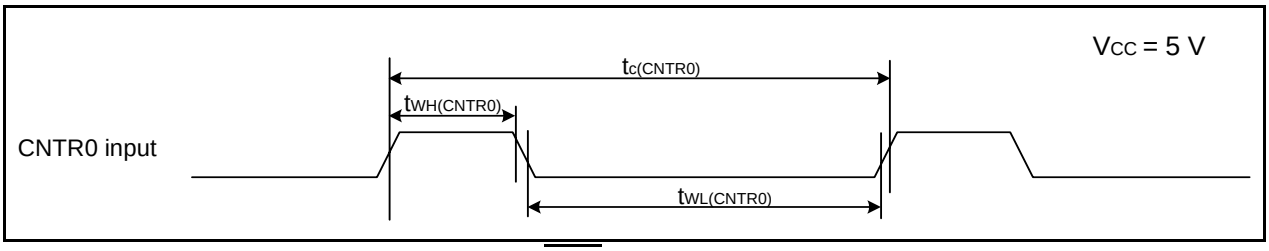



**Figure 5.5 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input Timing Diagram when Vcc = 5 V**

**Table 5.16 TCIN Input, $\overline{\text{INT3}}$ Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TCIN)}$ | TCIN input cycle time | 400(1) | – | ns |
| $t_{WH(TCIN)}$ | TCIN input “H” width | 200(2) | – | ns |
| $t_{WL(TCIN)}$ | TCIN input “L” width | 200(2) | – | ns |

NOTES:
1. When using timer C input capture mode, adjust the cycle time to (1/timer C count source frequency x 3) or above.
2. When using timer C input capture mode, adjust the pulse width to (1/timer C count source frequency x 1.5) or above.

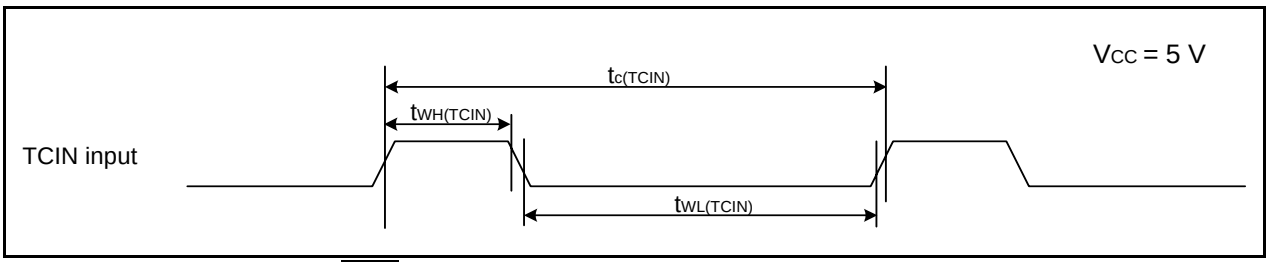



**Figure 5.6 TCIN Input, $\overline{\text{INT3}}$ Input Timing Diagram when Vcc = 5 V**



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**Table 5.17 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 200 | – | ns |
| $t_{W(CKH)}$ | CLKi input “H” width | 100 | – | ns |
| $t_{W(CKL)}$ | CLKi input “L” width | 100 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 50 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 50 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0 or 1

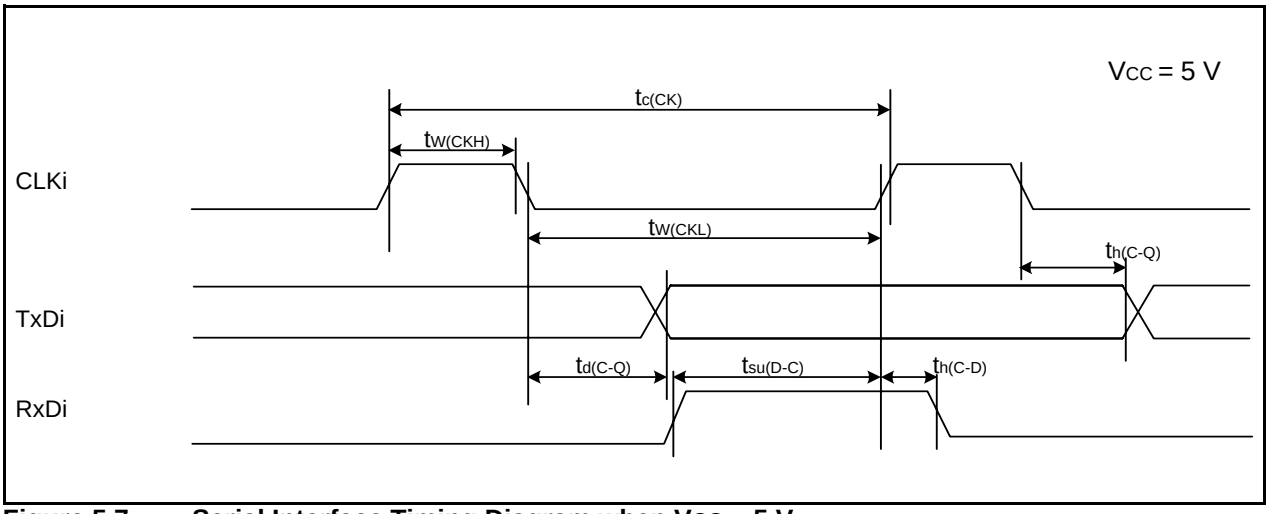



**Figure 5.7 Serial Interface Timing Diagram when Vcc = 5 V**

**Table 5.18 External Interrupt $\overline{INT0}$ Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{W(INH)}$ | $\overline{INT0}$ input “H” width | 250(1) | – | ns |
| $t_{W(INL)}$ | $\overline{INT0}$ input “L” width | 250(2) | – | ns |

NOTES:
1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

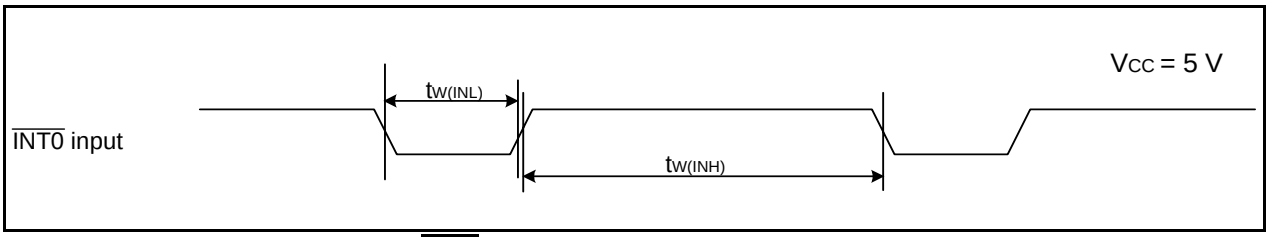



**Figure 5.8 External Interrupt $\overline{INT0}$ Input Timing Diagram when Vcc = 5 V**



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**Table 5.19 Electrical Characteristics (3) [Vcc = 3V]**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | Except $X_{OUT}$ | $I_{OH}$ = -1 mA | | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | $X_{OUT}$ | Drive capacity HIGH | $I_{OH}$ = -0.1 mA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| | | | Drive capacity LOW | $I_{OH}$ = -50 µA | $V_{CC}$ – 0.5 | – | $V_{CC}$ | V |
| $V_{OL}$ | Output “L” voltage | Except P1_0 to P1_3, $X_{OUT}$ | $I_{OL}$ = 1mA | | – | – | 0.5 | V |
| | | P1_0 to P1_3 | Drive capacity HIGH | $I_{OL}$ = 2 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 1 mA | – | – | 0.5 | V |
| | | $X_{OUT}$ | Drive capacity HIGH | $I_{OL}$ = 0.1 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | $I_{OL}$ = 50 µA | – | – | 0.5 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, CNTR0, CNTR1, TCIN, RXD0 | | | 0.2 | – | 0.8 | V |
| | | $\overline{RESET}$ | | | 0.2 | – | 1.8 | V |
| $I_{IH}$ | Input “H” current | | VI = 3 V | | – | – | 4.0 | µA |
| $I_{IL}$ | Input “L” current | | VI = 0 V | | – | – | -4.0 | µA |
| $R_{PULLUP}$ | Pull-up resistance | | VI = 0 V | | 66 | 160 | 500 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | – | 3.0 | – | MΩ |
| $f_{RING-S}$ | Low-speed on-chip oscillator frequency | | | | 40 | 125 | 250 | kHz |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 2.0 | – | – | V |

NOTE:
1. $V_{CC}$ = 2.7 to 3.3 V at $T_{opr}$ = -20 to 85 °C / -40 to 85 °C, f(XIN) = 10 MHz, unless otherwise specified.



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**Table 5.20 Electrical Characteristics (4) [Vcc = 3V] (Topr = -40 to 85 °C, unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Icc | Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss, comparator is stopped | High-speed mode | XIN = 20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 8 | 13 | mA |
| | | | XIN = 16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 7 | 12 | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 5 | – | mA |
| | | Medium-speed mode | XIN = 20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 3 | – | mA |
| | | | XIN = 16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 2.5 | – | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 1.6 | – | mA |
| | | High-speed on-chip oscillator mode | Main clock off<br>High-speed on-chip oscillator on = 8 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | – | 3.5 | 7.5 | mA |
| | | | Main clock off<br>High-speed on-chip oscillator on = 8 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | – | 1.5 | – | mA |
| | | Low-speed on-chip oscillator mode | Main clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8<br>FMR47 = 1 | – | 100 | 280 | µA |
| | | Wait mode | Main clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = 0 | – | 37 | 74 | µA |
| | | Wait mode | Main clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = 0 | – | 35 | 70 | µA |
| | | Stop mode | Main clock off, Topr = 25 °C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = 0 | – | 0.7 | 3.0 | µA |



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**Timing requirements**
**(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Ta = 25 °C) [Vcc = 3 V]**

**Table 5.21 XIN Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 100 | – | ns |
| $t_{WH(XIN)}$ | XIN input “H” width | 40 | – | ns |
| $t_{WL(XIN)}$ | XIN input “L” width | 40 | – | ns |

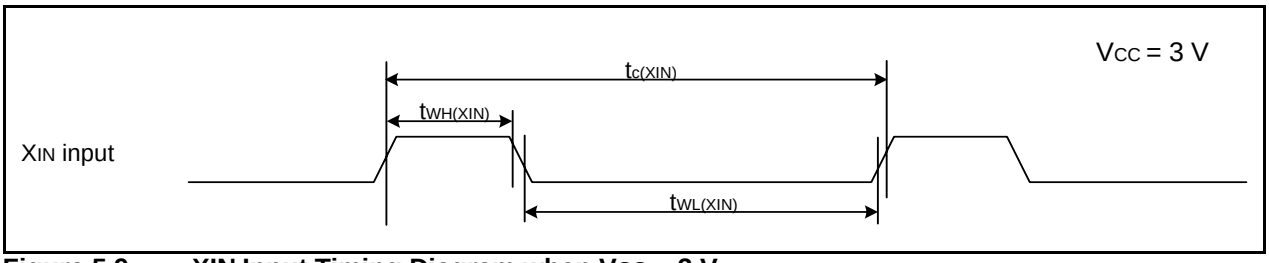



**Figure 5.9 XIN Input Timing Diagram when Vcc = 3 V**

**Table 5.22 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CNTR0)}$ | CNTR0 input cycle time | 300 | – | ns |
| $t_{WH(CNTR0)}$ | CNTR0 input “H” width | 120 | – | ns |
| $t_{WL(CNTR0)}$ | CNTR0 input “L” width | 120 | – | ns |

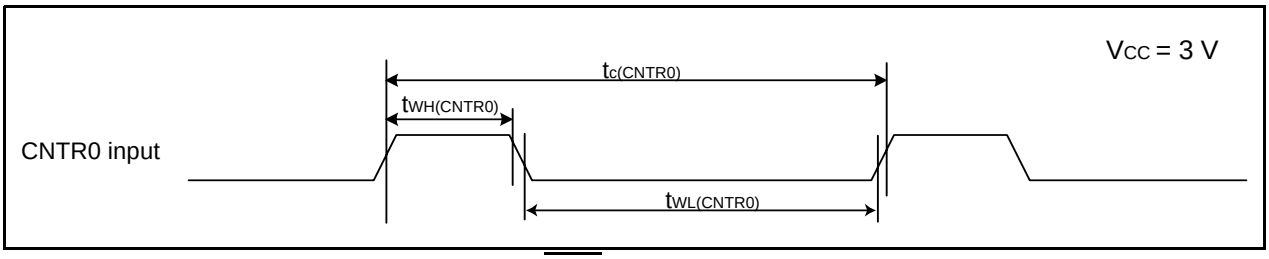



**Figure 5.10 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input Timing Diagram when Vcc = 3 V**

**Table 5.23 TCIN Input, $\overline{\text{INT3}}$ Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TCIN)}$ | TCIN input cycle time | 1,200(1) | – | ns |
| $t_{WH(TCIN)}$ | TCIN input “H” width | 600(2) | – | ns |
| $t_{WL(TCIN)}$ | TCIN input “L” width | 600(2) | – | ns |

NOTES:
1. When using the timer C input capture mode, adjust the cycle time to (1/timer C count source frequency × 3) or above.
2. When using the timer C input capture mode, adjust the width to (1/timer C count source frequency × 1.5) or above.

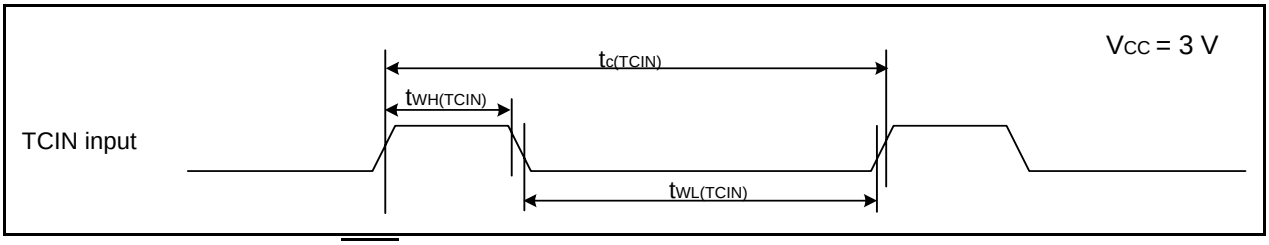



**Figure 5.11 TCIN Input, $\overline{\text{INT3}}$ Input Timing Diagram when Vcc = 3 V**



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**Table 5.24 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 300 | – | ns |
| $t_{W(CKH)}$ | CLKi input “H” width | 150 | – | ns |
| $t_{W(CKL)}$ | CLKi input “L” width | 150 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 80 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 70 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

i = 0 or 1

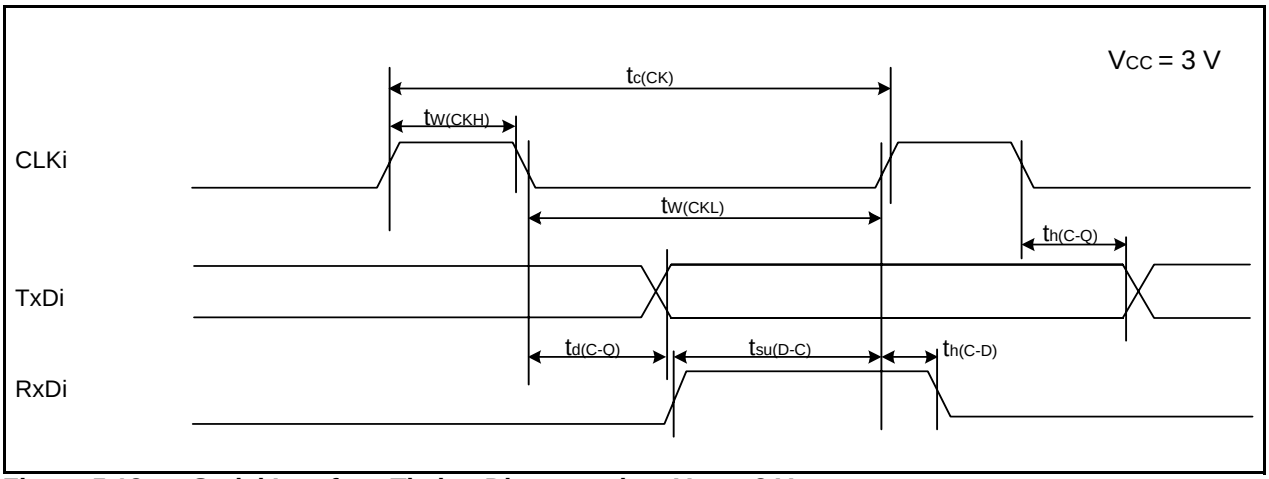



**Figure 5.12 Serial Interface Timing Diagram when VCC = 3 V**

**Table 5.25 External Interrupt $\overline{INT0}$ Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{W(INH)}$ | $\overline{INT0}$ input “H” width | 380(1) | – | ns |
| $t_{W(INL)}$ | $\overline{INT0}$ input “L” width | 380(2) | – | ns |

NOTES:
1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

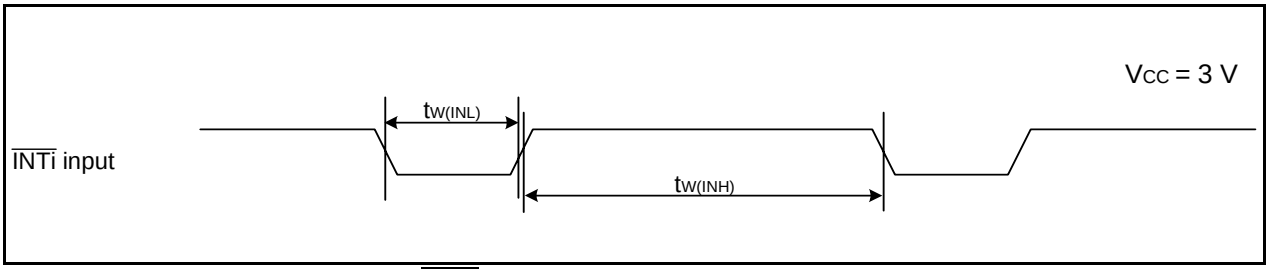


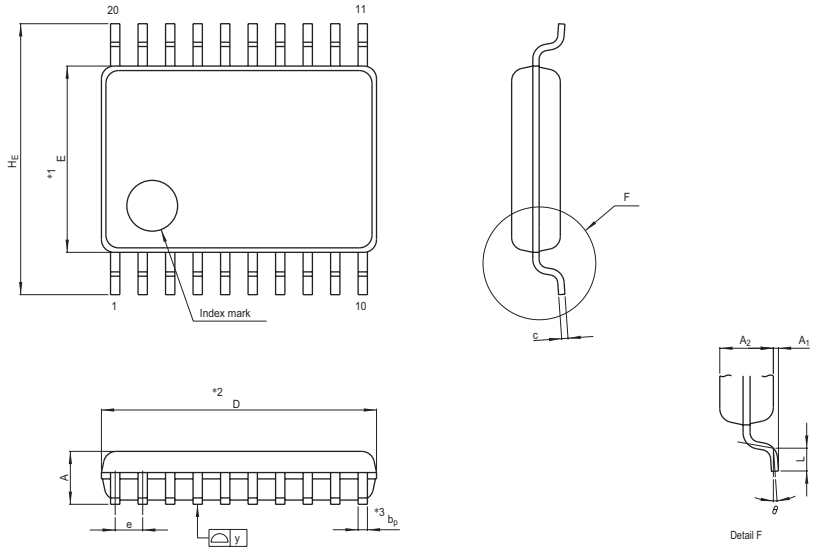

**Figure 5.13 External Interrupt $\overline{INT0}$ Input Timing Diagram when VCC = 3 V**



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# Package Dimensions

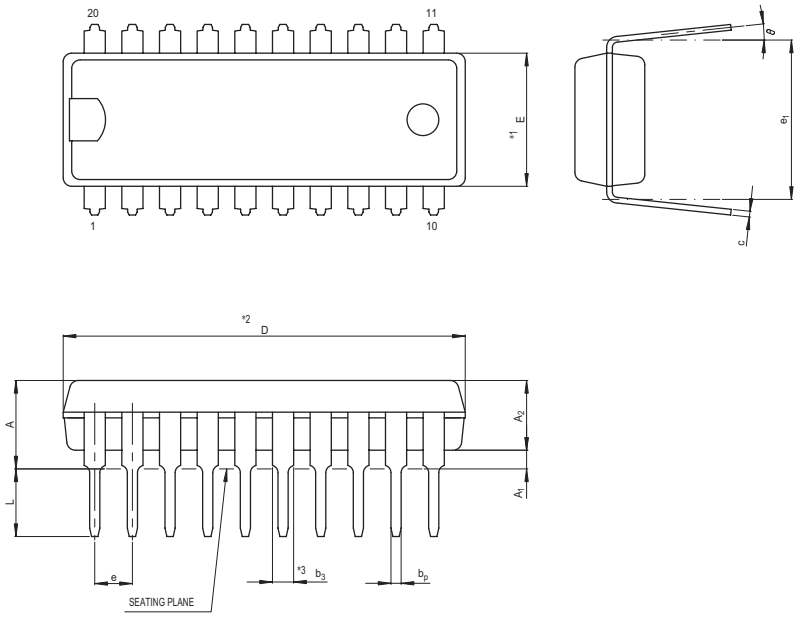
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LSSOP20-4.4x6.5-0.65 | PLSP0020JB-A | 20P2F-A | 0.1g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 6.4 | 6.5 | 6.6 |
| E | 4.3 | 4.4 | 4.5 |
| $A_2$ | — | 1.15 | — |
| A | — | — | 1.45 |
| $A_1$ | 0 | 0.1 | 0.2 |
| $b_p$ | 0.17 | 0.22 | 0.32 |
| c | 0.13 | 0.15 | 0.2 |
| θ | 0° | — | 10° |
| $H_E$ | 6.2 | 6.4 | 6.6 |
| e | 0.53 | 0.65 | 0.77 |
| y | — | — | 0.10 |
| L | 0.3 | 0.5 | 0.7 |

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-SDIP20-6.3x19-1.78 | PRDP0020BA-A | 20P4B | 1.0g |



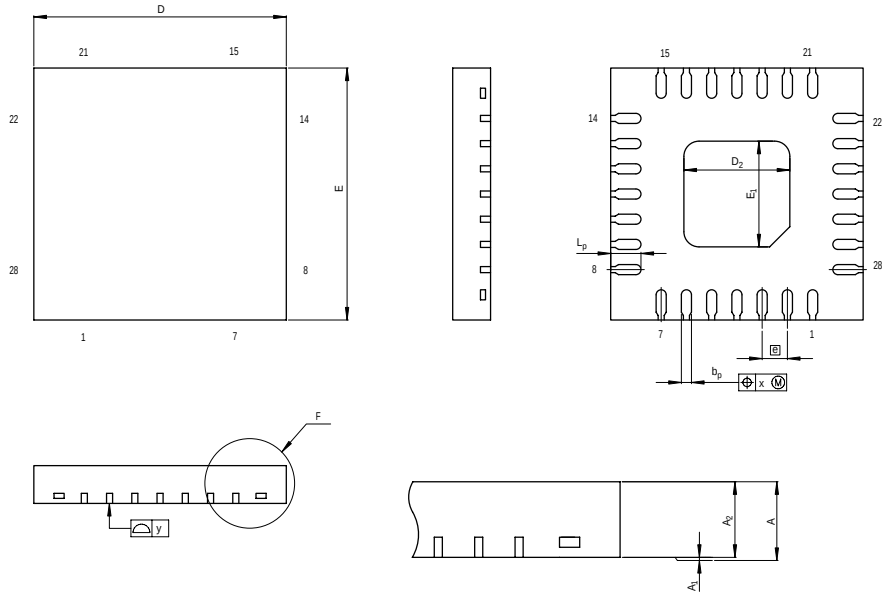

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| $e_1$ | 7.32 | 7.62 | 7.92 |
| D | 18.8 | 19.0 | 19.2 |
| E | 6.15 | 6.3 | 6.45 |
| A | — | — | 4.5 |
| $A_1$ | 0.51 | — | — |
| $A_2$ | — | 3.3 | — |
| $b_p$ | 0.38 | 0.48 | 0.58 |
| $b_3$ | 0.9 | 1.0 | 1.3 |
| c | 0.22 | 0.27 | 0.34 |
| θ | 0° | — | 15° |
| e | 1.528 | 1.778 | 2.028 |
| L | 3.0 | — | — |



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| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-HWQFN28-5x5-0.50 | PWQN0028KA-B | 28PJW-B | 0.05g |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 4.9 | 5.0 | 5.1 |
| E | 4.9 | 5.0 | 5.1 |
| $A_2$ | — | 0.75 | — |
| A | — | — | 0.8 |
| $A_1$ | 0 | 0 | 0.05 |
| $b_p$ | 0.15 | 0.2 | 0.25 |
| e | — | 0.5 | — |
| $L_p$ | 0.5 | 0.6 | 0.7 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| $D_2$ | — | — | 2.0 |
| $E_1$ | — | — | 2.0 |



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| REVISION HISTORY | R8C/18 Group, R8C/19 Group Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 0.10 | Nov 15, 2004 | – | First Edition issued |
| 0.20 | Jan 11, 2005 | 5, 6 | Tables 1.3 and 1.4: The date updated |
| 0.21 | Apr 04, 2005 | 2, 3 | Tables 1.1 and 1.2: Partly revised |
| | | 4 | Figure 1.1: Partly revised |
| | | 5, 6 | Tables 1.3 and 1.4: Partly revised |
| | | 5, 6 | Figure 1.2 and 1.3: Partly revised |
| | | 7, 8 | Figure 1.4 and 1.5: Partly revised |
| | | 10 | Table 1.6: Partly revised |
| | | 16 | Table 4.1: Partly revised |
| | | 17 | Table 4.2: Partly revised |
| | | 18 | Table 4.3: Partly revised |
| | | 20 | Package Dimensions are revised |
| 1.00 | May 27, 2005 | 5, 6 | Tables 1.3 and 1.4: Partly revised |
| | | 9 | Table 1.5: Partly revised |
| | | 25 | Table 5.9: Revised |
| | | 26 | Table 5.10: Partly revised |
| | | 28 | Table 5.13: Partly revised |
| | | 32 | Table 5.20: Partly revised |
| 1.10 | Jun 09, 2005 | 26 | Table 5.10: Partly revised |
| 1.20 | Nov 01, 2005 | 3 | Table 1.2 Performance Outline of the R8C/19 Group;<br>Flash Memory: (Data area) → (Data flash)<br>(Program area) → (Program ROM) revised |
| | | 4 | Figure 1.1 Block Diagram;<br>“Peripheral Function” added,<br>“System Clock Generation” → “System Clock Generator” revised |
| | | 6 | Table 1.4 Product Information of R8C/19 Group;<br>ROM capacity: “Program area” → “Program ROM”,<br>“Data area” → “Data flash” revised |
| | | 9 | Table 1.5 Pin Description;<br>Power Supply Input: “VCC/AVCC” → “VCC”,<br>“VSS/AVSS” → “VSS” revised<br>Analog Power Supply Input: added |
| | | 11 | Figure 2.1 CPU Register;<br>“Reserved Area” → “Reserved Bit” revised |
| | | 13 | 2.8.10 Reserved Area;<br>“Reserved Area” → “Reserved Bit” revised |
| | | 15 | 3.2 R8C/19 Group, Figure 3.2 Memory Map of R8C/19 Group;<br>“Data area” → “Data flash”,<br>“Program area” → “Program ROM” revised |



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| REVISION HISTORY | R8C/18 Group, R8C/19 Group Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.20 | Nov 01, 2005 | 16 | Table 4.1 SFR Information(1);<br>0009h: "XXXXXX00b" → "00h"<br>000Ah: "00XXX000b" → "00h"<br>001Eh: "XXXXX000b" → "00h" revised |
| | | 18 | Table 4.3 SFR Information(3);<br>0085h: "Prescaler Z" → "Prescaler Z Register"<br>0086h: "Timer Z Secondary" → "Timer Z Secondary Register"<br>0087h: "Timer Z Primary" → "Timer Z Primary Register"<br>008Ch: "Prescaler X" → "Prescaler X Register"<br>008Dh: "Timer X" → "Timer X Register"<br>0090h, 0091h: "Timer C" → "Timer C Register" revised |
| | | 22 | Table 5.4 Flash Memory (Program ROM) Electrical Characteristics;<br>NOTES 3 and 5 revised, NOTE8 deleted |
| | | 23 | Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics; NOTES 1 and 3 revised |
| | | 25 | Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset); NOTE 2 revised |
| | | 26 | Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics;<br>"High-Speed On-Chip Oscillator ..." →<br>"High-Speed On-Chip Oscillator Frequency ..." revised<br>NOTE 2, 3 added |
| | | 28 | Table 5.13 Electrical Characteristics (2) [Vcc = 5V];<br>NOTE 1 deleted |
| | | 32 | Table 5.20 Electrical Characteristics (4) [Vcc = 3V];<br>NOTE 1 deleted |
| 1.30 | Dec 16, 2005 | – | Products of PWQN0028KA-B package included |
| | | 5, 6 | Table 1.3, Table 1.4 revised |
| | | 24 | Table 5.4 Flash Memory (Program ROM) Electrical Characteristics;<br>Ta → Ambient temperature |
| | | 25 | Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics; Ta → Ambient temperature |
| | | 30, 34 | Table 5.13, Table 5.20; The title revised, Condition of Stop Mode added |
| | | 32, 36 | Table 5.17, Table 5.24; td(C-Q) and tsu(D-C) revised |
| | | 37, 38 | Package Dimensions revised |
| 1.40 | Apr 14, 2006 | 2, 3 | Table 1.1, Table 1.2;<br>Interrupts: Internal 8 → 10 sources, |
| | | 5, 6 | Table 1.3, Table 1.4; Type No. added, deleted |
| | | 16, 17 | Figure 3.1, Figure 3.2; Part Number added, deleted |
| | | 24, 25 | Table 5.4, Table 5.5;<br>Conditions: VCC = 5.0 V at Topr = 25 °C deleted |



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