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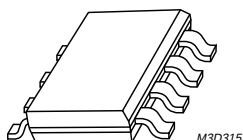
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Kind regards,

Team Nexperia



PHK12NQ03LT

N-channel TrenchMOS™ logic level FET

Rev. 02 — 02 March 2004

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Low on-state resistance
- Fast switching.

1.3 Applications

- DC-to-DC converters
- Portable equipment applications.

1.4 Quick reference data

- $V_{DS} \leq 30 \text{ V}$
- $I_D \leq 11.8 \text{ A}$
- $P_{tot} \leq 2.5 \text{ W}$
- $R_{DS(on)} \leq 14 \text{ m}\Omega$

2. Pinning information

Table 1: Pinning - SOT96-1 (SO8), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	Top view MBK187	MBB076
4	gate (g)		
5,6,7,8	drain (d)		

SOT96-1 (SO8)

3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
PHK12NQ03LT	SO8	Plastic small outline package; 8 leads	SOT96

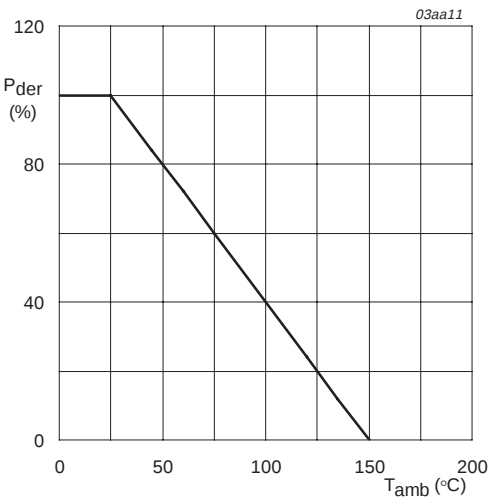


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4. Limiting values

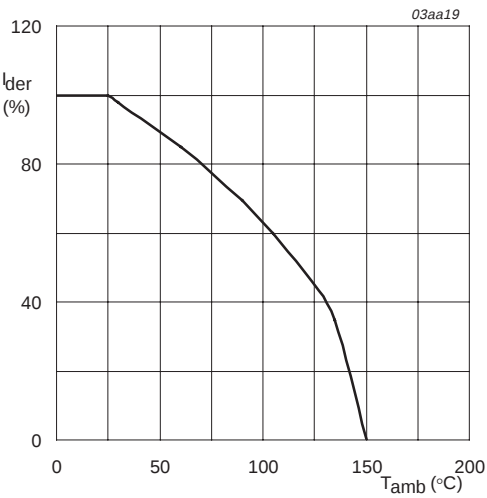
Table 3: Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage (DC)	25 °C ≤ T _j ≤ 150 °C	-	30	V
V _{GS}	gate-source voltage		-	±20	V
I _D	drain current	T _{amb} = 25 °C; pulsed; t _p ≤ 10 s; Figure 2 and 3	-	11.8	A
I _{DM}	peak drain current	T _{amb} = 25 °C; pulsed; t _p ≤ 10 μs; Figure 3	-	35.3	A
P _{tot}	total power dissipation	T _{amb} = 25 °C; pulsed; t _p ≤ 10 s; Figure 1	-	2.5	W
T _{stg}	storage temperature		-55	+150	°C
T _j	junction temperature		-55	+150	°C
Source-drain diode					
I _S	source (diode forward) current	T _{amb} = 25 °C; pulsed; t _p ≤ 10 s	-	11.8	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	unclamped inductive load; I _D = 7.7 A; t _p = 2.35 ms; V _{DD} ≤ 30 V; V _{GS} = 10 V; starting T _j = 25 °C	-	440	mJ



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

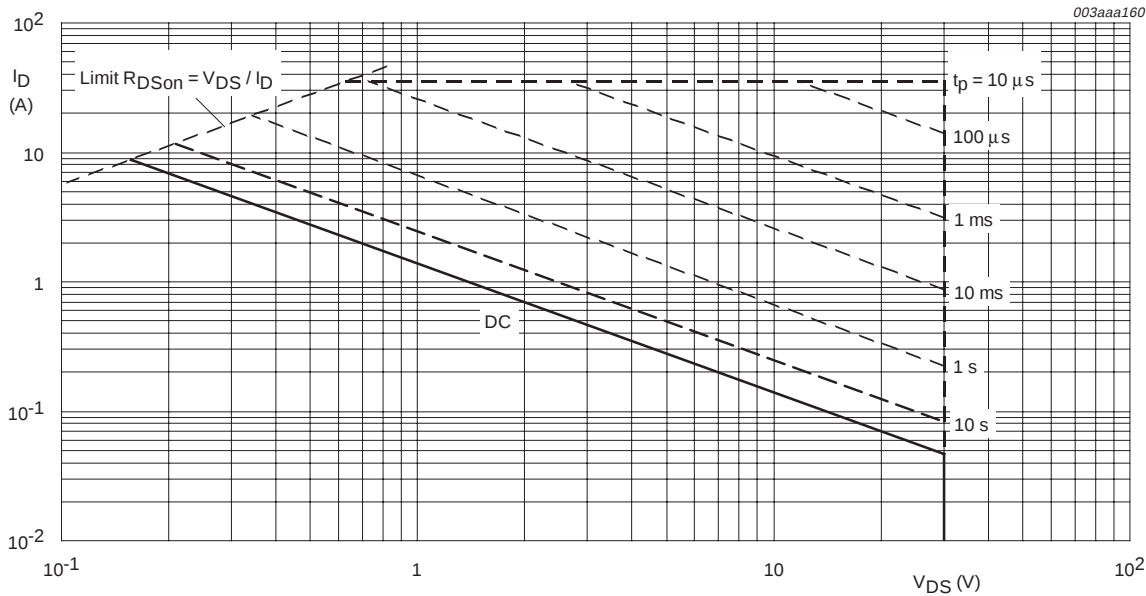
Fig 1. Normalized total power dissipation as a function of ambient temperature.



$V_{GS} \geq 5\text{ V}$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of ambient temperature.



$T_{amb} = 25^{\circ}C$; I_{DM} is single pulse

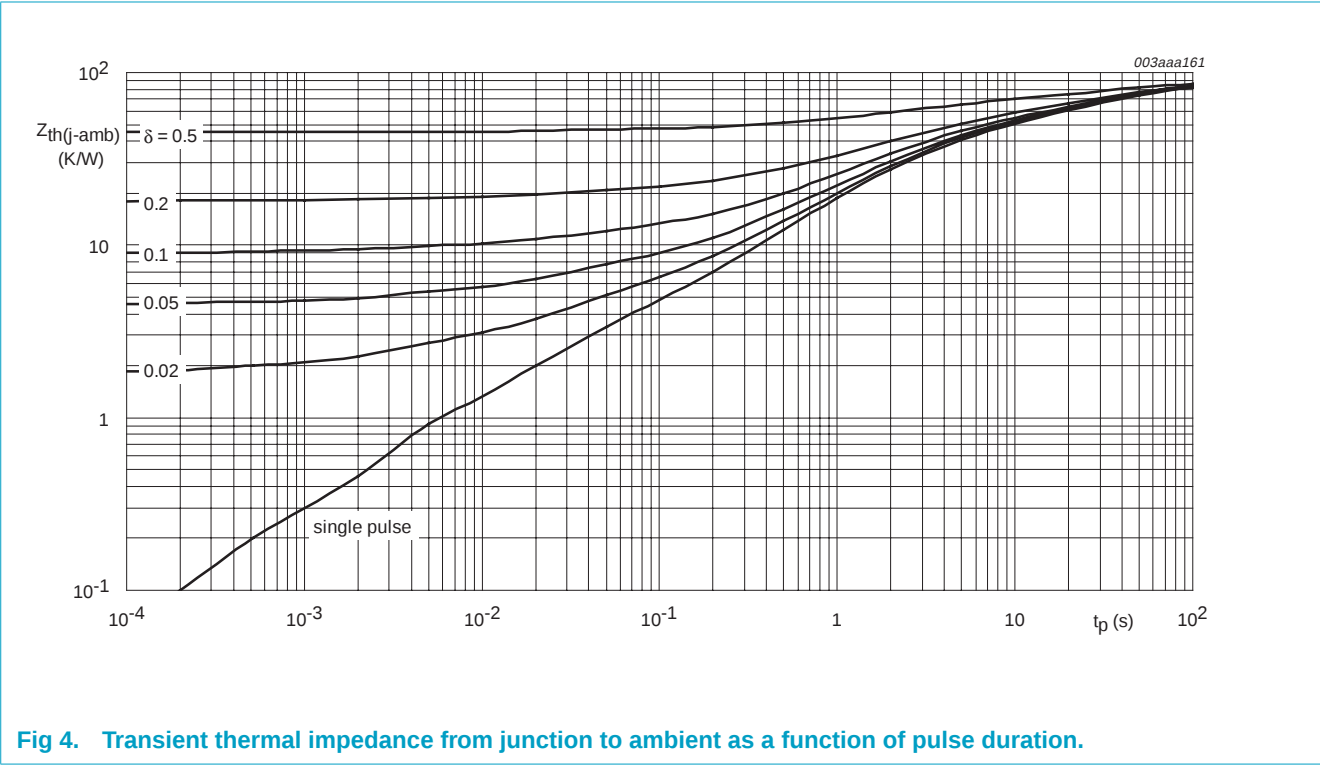
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint; $t_p \leq 10$ s; Figure 4	-	-	50	K/W

5.1 Transient thermal impedance

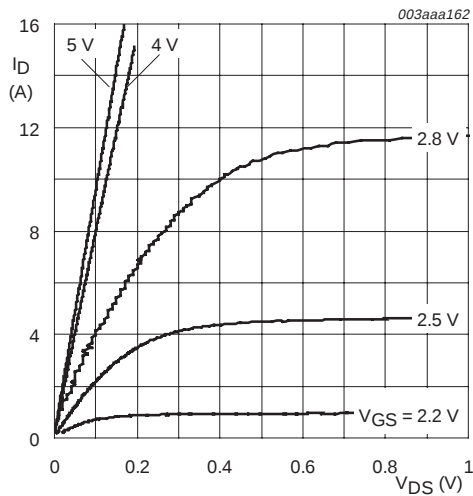


6. Characteristics

Table 5: Characteristics

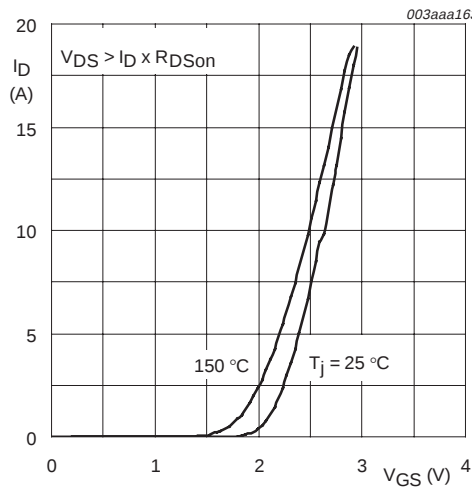
$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V	30	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 250 μA; V _{DS} = V _{GS} ; T _j = 25 °C; Figure 9	1	-	2	V
I _{DSS}	drain-source leakage current	V _{DS} = 24 V; V _{GS} = 0 V				
		T _j = 25 °C	-	-	1	μA
		T _j = 100 °C	-	-	5	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±20 V; V _{DS} = 0 V	-		100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 10 A; Figure 8	-	11	14	mΩ
		V _{GS} = 10 V; I _D = 12 A; Figure 8	-	8.9	10.5	mΩ
Dynamic characteristics						
g _{fs}	forward transconductance	V _{DS} = 15 V; I _D = 10 A;	-	34	-	S
Q _{g(tot)}	total gate charge	I _D = 15 A; V _{DD} = 16 V; V _{GS} = 5 V; Figure 13	-	17.6	-	nC
Q _{gs}	gate-source charge		-	4	-	nC
Q _{gd}	gate-drain (Miller) charge		-	4.4	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 16 V; f = 1 MHz; Figure 11	-	1335	-	pF
C _{oss}	output capacitance		-	391	-	pF
C _{rss}	reverse transfer capacitance		-	190	-	pF
t _{d(on)}	turn-on delay time	V _{DD} = 16 V; R _D = 10 Ω; V _{GS} = 10 V	-	10.6	-	ns
t _r	rise time		-	11.7	-	ns
t _{d(off)}	turn-off delay time		-	37	-	ns
t _f	fall time		-	19	-	ns
Source-drain (reverse) diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 1 A; V _{GS} = 0 V; Figure 12	-	0.7	1.0	V
t _{rr}	reverse recovery time	I _S = 2.3 A; dI _S /dt = −100 A/μs; V _{GS} = 0 V	-	70	-	ns



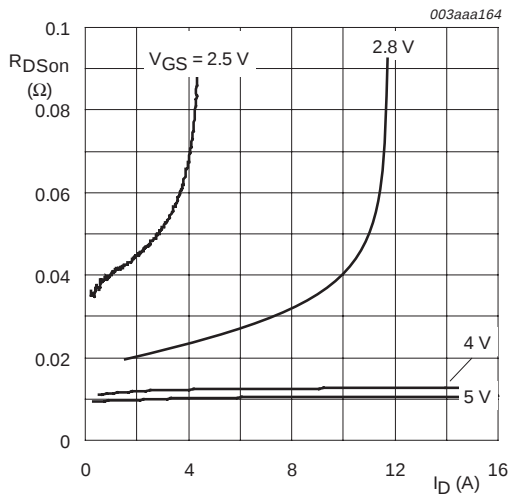
T_J = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



T_J = 25 °C and 150 °C; V_{DS} > I_D × R_{DSon}

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



T_J = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.

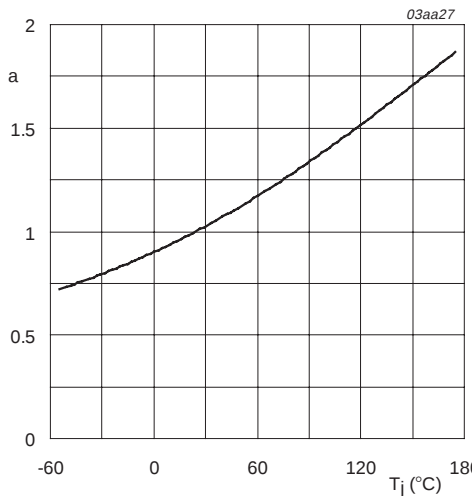
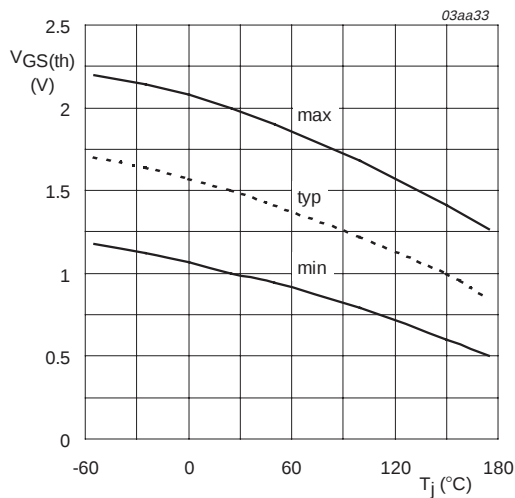
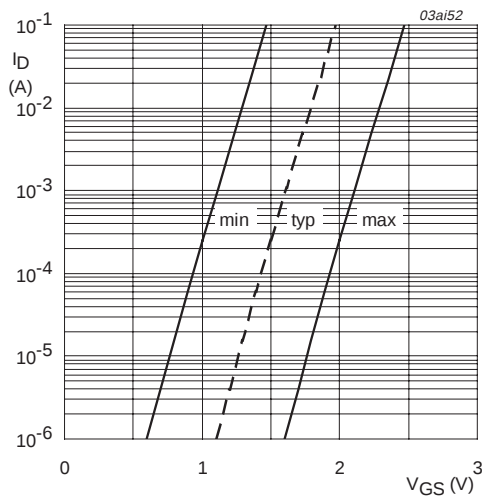


Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.



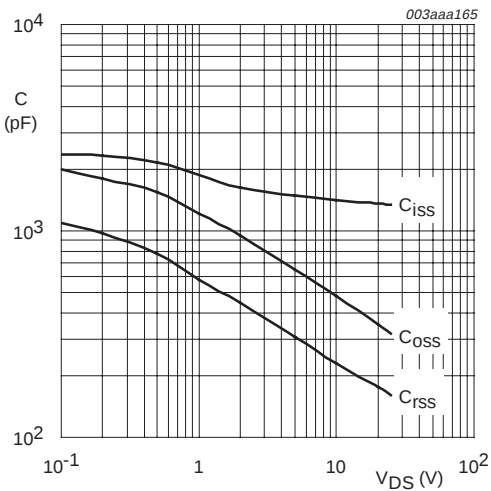
$I_D = 250 \mu A$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



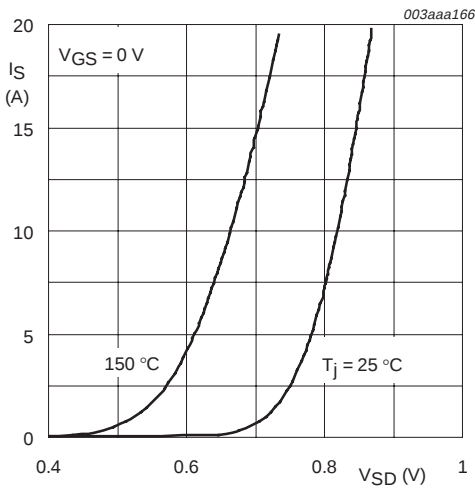
$T_j = 25 \text{ }^\circ\text{C}$; $V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



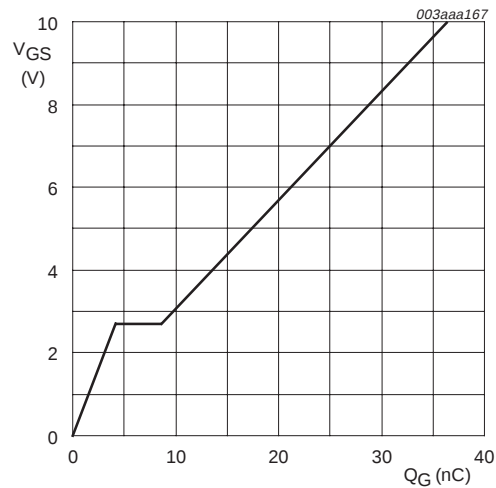
$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25 \text{ }^\circ\text{C}$ and $150 \text{ }^\circ\text{C}$; $V_{GS} = 0 \text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 15\text{ A}; V_{DD} = 16\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

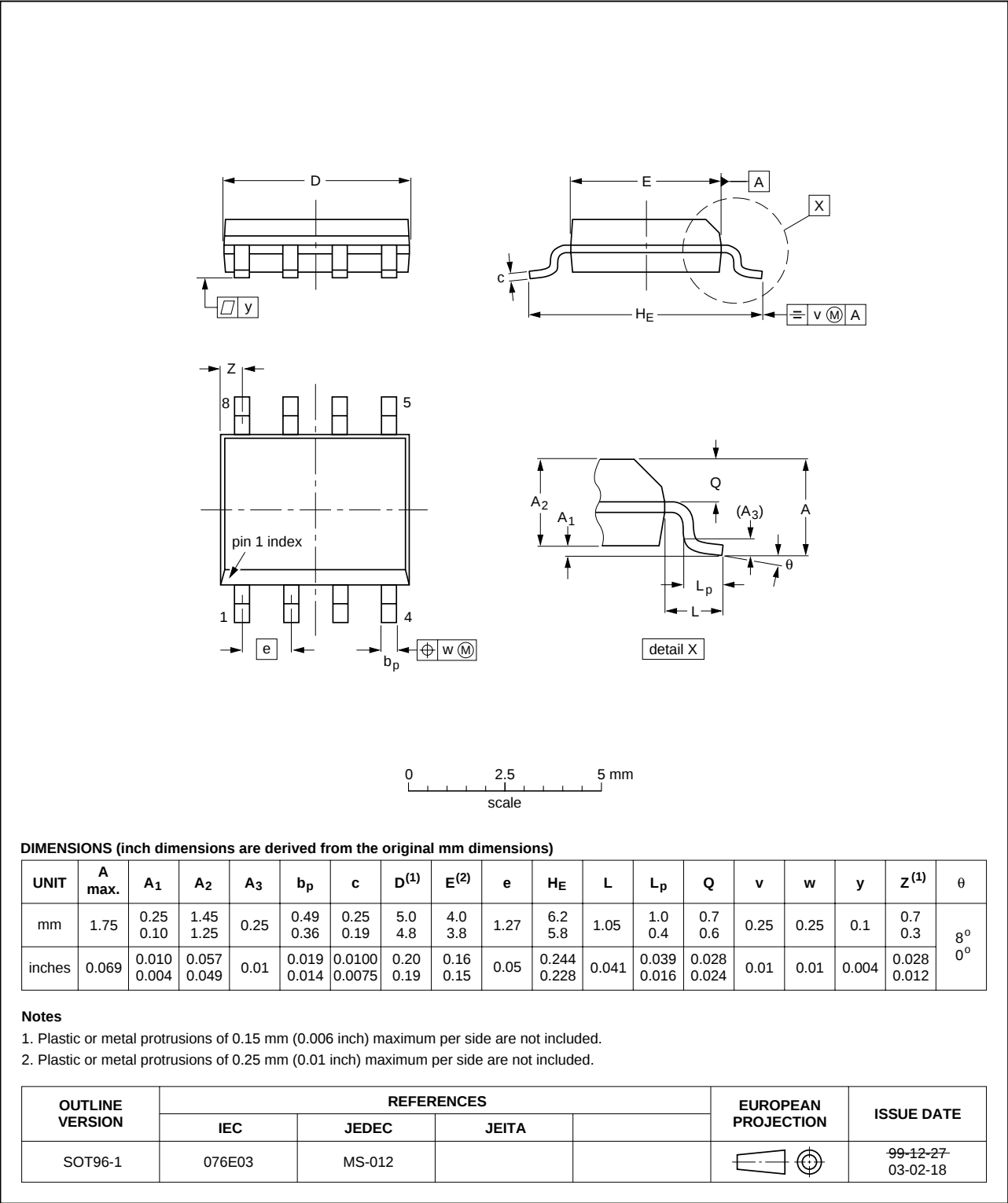


Fig 14. SOT96-1 (SO8).

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	20040302	-	Product data (9397 750 12955) Modifications • Data sheet updated to latest presentation standards. • Section 1.4 “Quick reference data” correction to I_D value. • Section 4 “Limiting values” I_D, I_{DM}, P_{tot} and I_S conditions and values corrected. • Section 4 “Limiting values” Figure 1, 2 and 3 corrected. • Section 4 “Limiting values” E_{DS(AL)S} added. • Section 5 “Thermal characteristics” typ and max values corrected. • Section 5 “Thermal characteristics” Figure 4 corrected. • Section 6 “Characteristics” Figure 13 corrected.
01	20020322	-	Product data (9397 750 09405)

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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