

LMR14020SEVM User's Guide

The Texas Instruments LMR14020SEVM evaluation module (EVM) helps designers evaluate the operation and performance of the LMR14020S wide-input Simple Switcher® buck regulator. This document describes the setup and the input / output connections of the EVM. Included are the board layout, schematic, and bill of materials.

Contents

1	Introdu	ction	2
2	Setup.		2
	2.1	Input/Output Connector Description	2
	2.2	Adjusting the Output Voltage	3
3	Board I	Layout	3
4	Schematic and Bill of Materials		6

Copyright © 2015, Texas Instruments Incorporated

Trademarks

Simple Switcher is a registered trademark of Texas Instruments.

Downloaded from Arrow.com.



1 Introduction

The LMR14020S is a 40-V, 2-A step-down regulator with 40-µA quiescent current. With a wide-input range from 4 V to 40 V, it is suitable for a wide range of applications from automotive to industry for power conditioning from unregulated sources. The LMR14020SEVM evaluation board is designed to provide the design engineer with a fully functional power converter based on the buck topology to evaluate the LMR14020 series operation and performance.

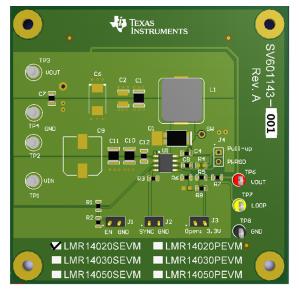


Figure 1. LMR14020SEVM Board

EVM Features

- 7 V to 30 V Input Voltage Range
- Jumper Selectable Output Options (5.0 V or 3.3 V)
- Up to 2 A Output Current
- Switching Frequency 1.6 MHz
- Internal Compensation

The EVM contains one DC / DC converter (See Table 1)

Table 1. Device and Package Configurations

CONVERTER	EVM	IC	PACKAGE	
U1	LMR14020SEVM	LMR14020S	HSOIC-8	

2 Setup

This section describes the jumpers and connectors on the EVM and how to properly connect, set up and use the LMR14020SEVM .

2.1 Input/Output Connector Description

VIN — **Terminal TP1** – is the power input terminal for the converter. Adjacent to it is the GND reference ground. Use this terminal to attach the EVM to a cable harness.

VOUT — **Terminal TP3** – is the regulated output voltage for the converter. Adjacent to it is the GND reference ground.

GND — **Terminal TP2, TP4** – are the ground reference for the converter. Use these terminals to attach the EVM to a cable harness.

EN — **Jumper J1** – is used to enable the switch-mode converter. The device will be enabled when the respective jumper is high or floating, and disabled when low. EN turn off trip point also can be programmed by changing R1 or R2. Refer to LMR14020S datasheet for enable and adjustable undervoltage lockout.



Figure 2. Enable Jumper Setting

SYNC — Jumper J2 – is used to synchronize the switching frequency to external clock. Refer to data sheet for detail application information.

Testpoint — TP6, TP7, TP8 – these are test points used for loop response measurements.

2.2 Adjusting the Output Voltage

The default setting output voltage is 5.0 V. Open J3 will change output voltage from 5.0 V to 3.3 V.

If other outputs need to be configureg, then: open J3 and adjust the feedback resistors using the following equation.

 $V_{OUT} = V_{FB} (1 + (R5 / R6))$

(1)

Where $V_{\mbox{\tiny FB}}$ is 0.75 V

3 Board Layout

Figure 3 to Figure 6 show the board layout for the LMR14020SEVM. The PCB consists of a 4-layer design. 2-oz copper planes are applied on all four layers to dissipate heat with an array of thermal vias under the thermal pad to connect to all four layers.

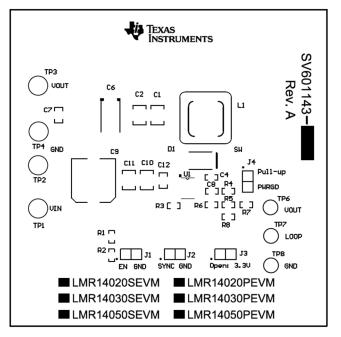


Figure 3. Top Layer

SNVU467–February 2015 Submit Documentation Feedback



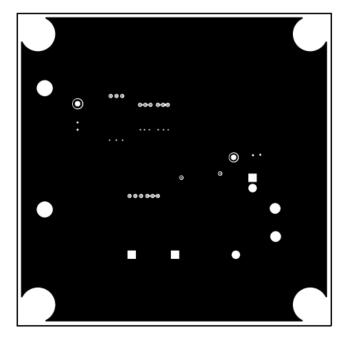


Figure 4. Middle Layer 1

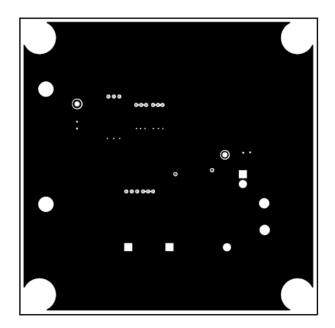


Figure 5. Middle Layer 2



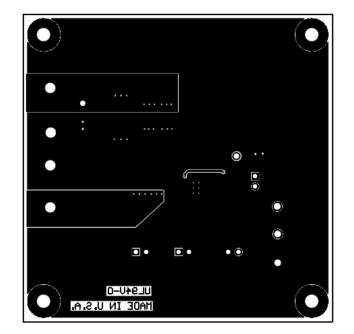


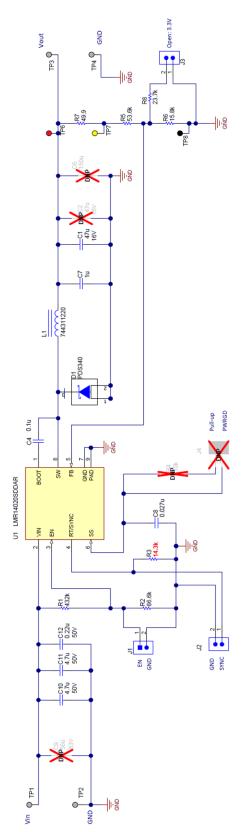
Figure 6. Bottom Layer

Downloaded from Arrow.com.



Schematic and Bill of Materials

4 Schematic and Bill of Materials





Designator	Description	Part Number	Footprint	Quantity
C1	CAP, CERM, 47 μF, 16 V, +/-20%, X5R, 1210	GRM32ER61C476ME15L	1210	2
C4	CAP, CERM, 0.1 μF, 16 V, +/- 10%, X7R, 0603	GRM188R71C104KA01D	0603	1
C7	CAP, CERM, 1 μF 25 V, +/- 10%, X7R, 0805	GRM21BR71E105KA99L	0805	1
C8	CAP, CERM, 0.027 μF, 100 V, +/- 10%, X7R, 0603	C0603C273K1RACTU	0603	1
C10, C11	CAP, CERM, 4.7 μF, 50 V, +/-10%, X7R, 1210	GRM32ER71H475KA88L	1210	2
C12	CAP, CERM, 0.22 μF, 50 V, +/- 10%, X7R, 0805	GRM21BR71H224KA01L	0805	1
D1	Diode, Schottky, 40 V, 3 A, PowerDI5	PDS340-13	PowerDI5	1
J1, J2, J3	Header, 100 mil, 2 x 1, Gold, TH	TSW-102-07-G-S	TSW-102-07-G-S	3
L1	Inductor, 2.2 µH, 9 A, 0.0115 ohm	744311220	WE-HCI	1
R1	RES, 432 k, 1%, 0.1 W, 0603	CRCW0603432KFKEA	0603	1
R2	RES, 86.6 k, 1%, 0.1 W, 0603	CRCW060386K6FKEA	0603	1
R3	RES, 14.3 k, 1%, 0.1 W, 0603	CRCW060314K3FKEA	0603	1
R5	RES, 53.6 k, 1%, 0.1W, 0603	CRCW060353K6FKEA	0603	1
R6	RES, 15.8 k, 1%, 0.1 W, 0603	CRCW060315K8FKEA	0603	1
R7	RES, 49.9 ohm, 1%, 0.1W, 0603	CRCW060349R9FKEA	0603	1
R8	RES, 23.7 k, 1%, 0.1 W, 0603	CRCW060323K7FKEA	0603	1
SH-J1, SH-J3	Shunt, 100 mil, Flash Gold, Black	SPC02SYAN	TSW-102-07-G-S	2
TP1, TP2, TP3, TP4	Terminal, Turret, TH, Double	1502-2	Keystone1502-2	4
TP6	Test Point, TH, Multipurpose, Red	5010	Keystone5010	1
TP7	Test Point, TH, Multipurpose, Yellow	5014	Keystone5014	1
TP8	Test Point, TH, Multipurpose, Black	5011	Keystone5011	1
U1	IC, 40 V, 2 A, Low I _Q , Current Mode, Buck Regulator	LMR14020SDDAR	HSOIC-8	1
PCB	PCB, FR4, 4 Layers, Size 3000 x 3000 mil, Thickness 62 mil	SV601143		1

Table 2. LMR14020SEVM Bill of Materials (BOM)

Downloaded from Arrow.com.

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your noncompliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/stdterms.htm), evaluation

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2017, Texas Instruments Incorporated