

TLP105

Isolated bus drivers

High-speed line receivers

Microprocessor system interfaces

The Toshiba TLP105 consists of an infrared emitting diode optically coupled to a high-gain, high-speed photodetector.

The TLP105 is housed in a 6-pin MFSOP.

With a totem-pole output, the TLP105 is capable of both sinking and sourcing current.

The TLP105 has an internal Faraday shield, which provides a guaranteed common-mode transient immunity of $\pm 10\text{ kV}/\mu\text{s}$.

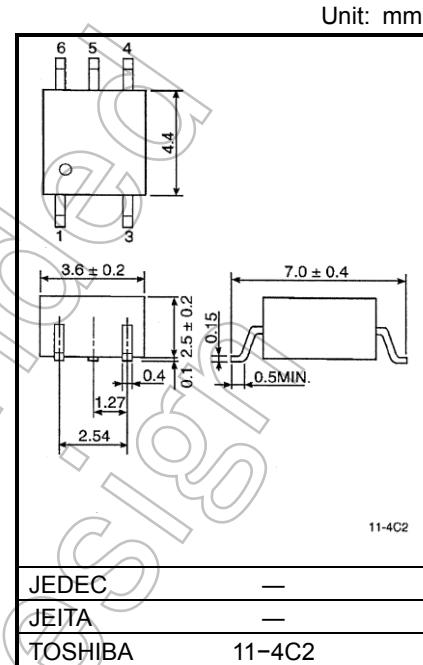
The TLP105 has a noninverting output. An inverting-output version, the TLP108, is also available.

- Buffer logic type (totem-pole output)
- Guaranteed Performance Over Temperature: -40 to 100°C
- Power Supply Voltage: 4.5 to 20 V
- Input Threshold Current: $I_{FLH} = 1.6$ mA (max)
- Switching Time (t_{pLH}/t_{pHL}): 250 ns (max)
- Common mode transient immunity: ± 10 kV/ μ s
- Isolation Voltage: 3750 Vrms
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A
- File No.E67349
- VDE-approved: EN 60747-5-5 (Note 1)

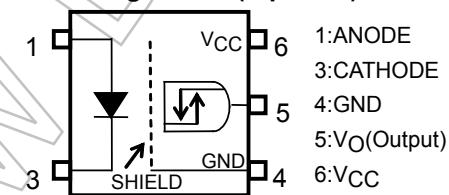
Note 1 : When a VDE approved type is needed,
please designate the **Option(V4)**.

Truth Table

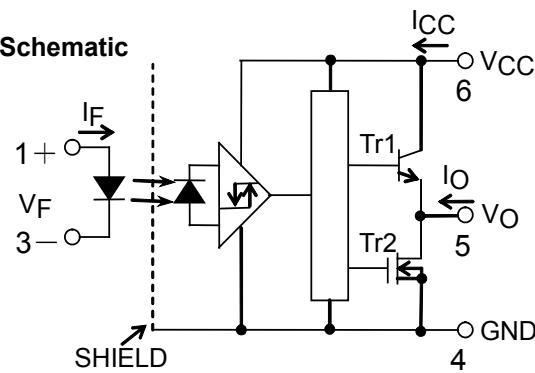
| Input | LED | Tr1 | Tr2 | Output |
|-------|-----|-----|-----|--------|
| H | ON | ON | OFF | H |
| L | OFF | OFF | ON | L |



Pin Configuration (top View)



Schematic



0.1 μ F bypass capacitor must be connected between pin 6 and 4.

Start of commercial production
2008-09

Recommended Operating Conditions

| CHARACTERISTIC | SYMBOL | MIN | TYP. | MAX | UNIT |
|-----------------------|--------------|-----|------|-----|------|
| Input Current, ON | $I_{F(ON)}$ | 2 | — | 10 | mA |
| Input Voltage, OFF | $V_{F(OFF)}$ | 0 | — | 0.8 | V |
| Supply Voltage* | V_{CC} | 4.5 | — | 20 | V |
| Operating Temperature | T_{opr} | -40 | — | 100 | °C |
| Fan-out (TTL Load) | N | — | — | 4 | — |

* This item denotes operating range, not meaning of recommended operating conditions.

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Absolute Maximum Ratings (Ta = 25°C)

| CHARACTERISTIC | SYMBOL | RATING | UNIT |
|---|---|-----------------|-----------------------|
| LED | Forward Current | I_F | 20 mA |
| | Forward Current Derating (Ta ≥ 83°C) | $\Delta F/°C$ | -0.48 mA/°C |
| | Peak Transient Forward Current (Note1) | I_{FPT} | 1 A |
| | Reverse Voltage | V_R | 5 V |
| | Input Power Dissipation | P_D | 40 mW |
| | Input Power Dissipation derating (Ta ≥ 83°C) | $\Delta P_D/°C$ | -0.95 mW/°C |
| DETECTOR | Output Current 1 (Ta ≤ 25°C) | I_{O1} | 25/-15 mA |
| | Output Current 2 (Ta ≤ 100°C) | I_{O2} | 5/-5 mA |
| | Output Current Derating (Ta ≥ 25°C) | $\Delta O1/°C$ | -0.26/-0.13 mA/°C |
| | Peak Output Current (Note2) | I_{OP} | 50/-50 mA |
| | Output Voltage | V_O | -0.5 to 20 V |
| | Output Power Dissipation | P_O | 75 mW |
| | Output Power Dissipation Derating (Ta ≥ 25°C) | $\Delta P_O/°C$ | -0.75 mW/°C |
| | Supply Voltage | V_{CC} | -0.5 to 20 V |
| Operating Temperature Range | | T_{opr} | -40 to 100 °C |
| Storage Temperature Range | | T_{stg} | -55 to 125 °C |
| Lead Solder Temperature (10 s) | | T_{sol} | 260 °C |
| Isolation Voltage (AC, 60 s, R.H. ≤ 60 %) (Note3) | | BV_S | 3750 V _{rms} |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Pulse width ≤ 1 μs, 300 pps.

Note 2: Pulse width ≤ 5 μs, duty cycle ≤ 0.025

Note 3: Device considered a two terminal device: pins 1 and 3 shorted together and pins 4, 5 and 6 shorted together.

Electrical Characteristics

(Unless otherwise specified, $T_a = -40$ to 100°C , $V_{CC} = 4.5$ to 20 V)

| CHARACTERISTIC | SYMBOL | TEST CIRCUIT | CONDITION | MIN | TYP. | MAX | UNIT | |
|--|-------------------------|--------------|---|---|-------------|------------|----------------------------|----|
| Input Forward Voltage | V_F | — | $I_F = 10$ mA, $T_a = 25^\circ\text{C}$ | 1.45 | 1.57 | 1.75 | V | |
| Temperature Coefficient of Forward Voltage | $\Delta V_F/\Delta T_a$ | — | $I_F = 10$ mA | — | -2.0 | — | $\text{mV}/^\circ\text{C}$ | |
| Input Reverse Current | I_R | — | $V_R = 5$ V, $T_a = 25^\circ\text{C}$ | — | — | 10 | μA | |
| Input Capacitance | C_T | — | $V = 0$ V, $f = 1$ MHz, $T_a = 25^\circ\text{C}$ | — | 100 | — | pF | |
| Logic Low Output Voltage | V_{OL} | 1 | $I_{OL} = 3.5$ mA, $V_F = 0.8$ V | — | 0.2 | 0.6 | V | |
| Logic High Output Voltage | V_{OH} | 2 | $I_{OH} = -2.6$ mA, $V_{CC} = 4.5$ V $I_F = 5$ mA, $V_{CC} = 20$ V | 2.7 17.4 | 4.0 19.0 | — — | V | |
| Logic Low Supply Current | I_{CCL} | 3 | $V_F = 0$ V | $V_{CC} = 20$ V $V_{CC} = 5.5$ V | — — | 3.0 3.0 | mA | |
| Logic High Supply Current | I_{CCH} | 4 | $I_F = 5$ mA | $V_{CC} = 20$ V $V_{CC} = 5.5$ V | — — | 3.0 3.0 | mA | |
| Logic Low Short Circuit Output Current (Note 1) | I_{OSL} | 5 | $V_F = 0$ V | $V_{CC} = V_O = 5.5$ V $V_{CC} = V_O = 20$ V | 15 20 | 80 90 | — | mA |
| Logic High Short Circuit Output Current (Note 1) | I_{OSH} | 6 | $I_F = 5$ mA $V_O = \text{GND}$ | $V_{CC} = 5.5$ V $V_{CC} = 20$ V | -5 -10 | -15 -20 | — | mA |
| Input Current Logic High Output | I_{FLH} | — | $I_O = -2.6$ mA, $V_O > 2.4$ V | — | 0.4 | 1.6 | mA | |
| Input Voltage Logic Low Output | V_{FHL} | — | $I_O = 3.5$ mA, $V_O < 0.4$ V | 0.8 | — | — | V | |
| Input Current Hysteresis | I_{HYS} | — | $V_{CC} = 5$ V | — | 0.05 | — | mA | |

*All typical values are at $T_a = 25^\circ\text{C}$

Note 1: Duration of output short circuit time should not exceed 10 ms.

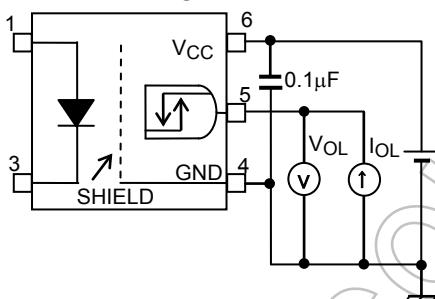
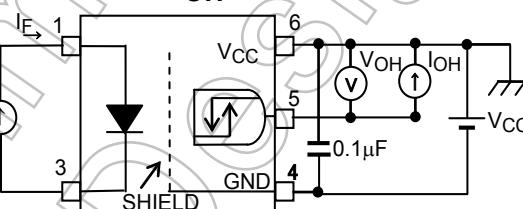
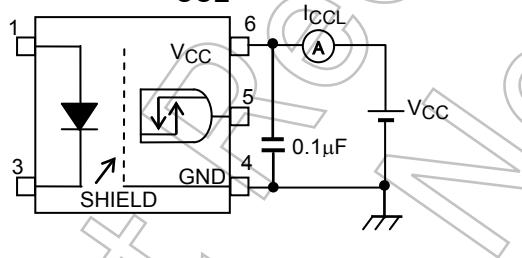
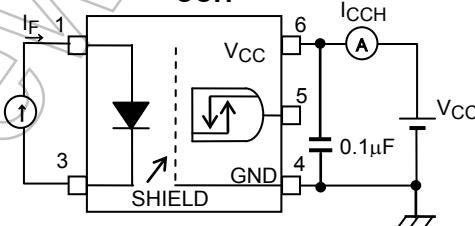
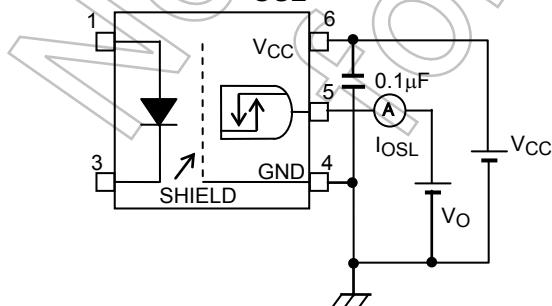
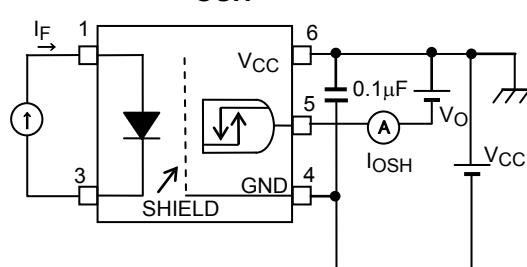
Note : A ceramic capacitor ($0.1 \mu\text{A}$) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.Isolation Characteristics ($T_a = 25^\circ\text{C}$)

| Characteristic | Symbol | Test Condition | Min | Typ. | Max | Unit |
|-----------------------------|----------|----------------------------------|--------------------|-----------|-----|-----------|
| Capacitance input to output | C_S | $V_S = 0$ V, $f = 1$ MHz | — | 0.8 | — | pF |
| Isolation resistance | R_S | $R.H. \leq 60\%$, $V_S = 500$ V | 1×10^{12} | 10^{14} | — | Ω |
| Isolation voltage | B_{VS} | AC, 60 s | 3750 | — | — | V_{rms} |

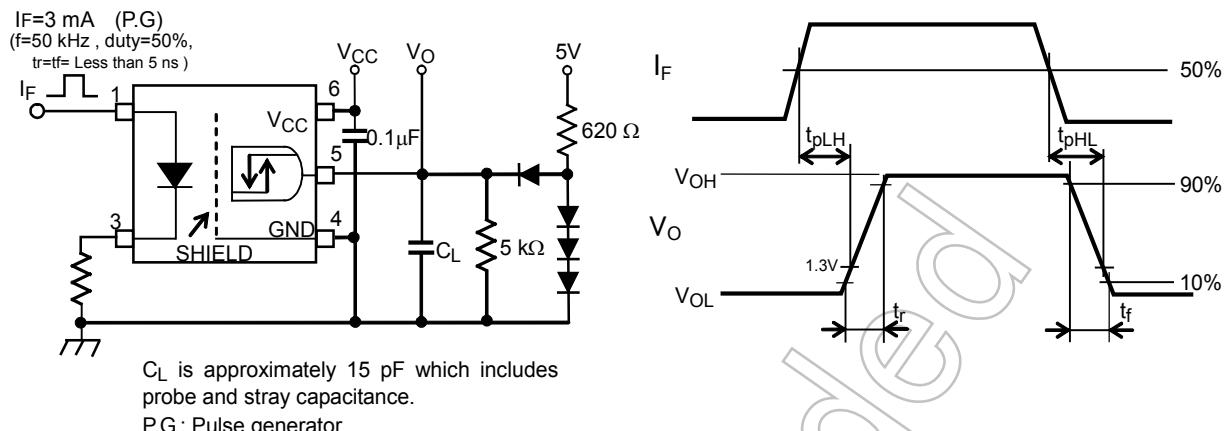
Switching Characteristics

(Unless otherwise specified, $T_a = -40$ to 100°C , $V_{CC} = 4.5$ to 20 V)

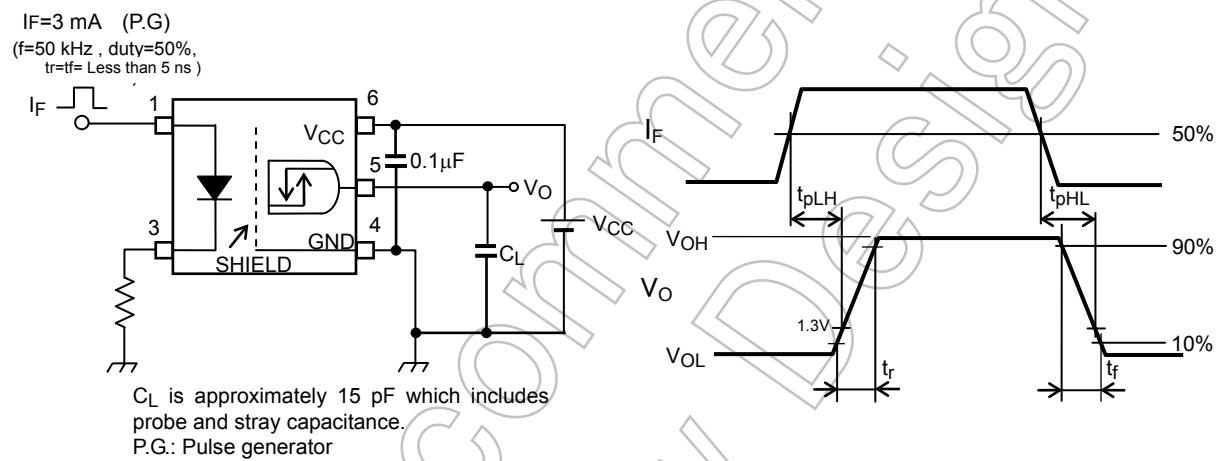
| CHARACTERISTIC | SYMBOL | TEST CIRCUIT | CONDITION | MIN | TYP. | MAX | UNIT |
|---|-----------------------|--------------|--|--------|------|-----|------------|
| Propagation Delay Time to Logic High output | t_{PLH} | 7, 8 | $I_F = 0 \rightarrow 3$ mA | 30 | 150 | 250 | ns |
| Propagation Delay Time to Logic Low output | t_{PHL} | | $I_F = 3 \rightarrow 0$ mA | 30 | 150 | 250 | ns |
| Switching Time Dispersion between ON and OFF | $ t_{PHL} - t_{PLH} $ | | — | — | — | 220 | ns |
| Rise Time (10 – 90 %) | t_r | | $I_F = 0 \rightarrow 3$ mA, $V_{CC} = 5$ V | — | 30 | 75 | ns |
| Fall Time (90 – 10 %) | t_f | | $I_F = 3 \rightarrow 0$ mA, $V_{CC} = 5$ V | — | 30 | 75 | ns |
| Common Mode transient Immunity at High Level Output | CM_H | 9 | $V_{CM} = 1000$ V _{p-p} , $I_F = 5$ mA, $V_{CC} = 20$ V, $T_a = 25^\circ\text{C}$ | -10000 | — | — | V/ μ s |
| Common Mode transient Immunity at Low Level Output | CM_L | | $V_{CM} = 1000$ V _{p-p} , $I_F = 0$ mA, $V_{CC} = 20$ V, $T_a = 25^\circ\text{C}$ | 10000 | — | — | V/ μ s |

*All typical values are at $T_a = 25^\circ\text{C}$ Test Circuit 1: V_{OL} Test Circuit 2: V_{OH} Test Circuit 3: I_{CCL} Test Circuit 4: I_{CCH} Test Circuit 5: I_{OSL} Test Circuit 6: I_{OSH} 

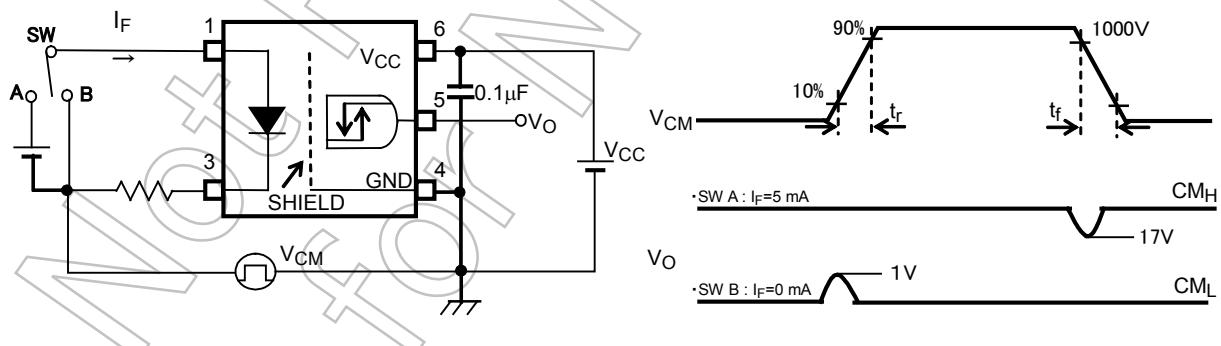
Test Circuit 7: Switching Time Test Circuit



Test Circuit 8: Switching Time Test Circuit



Test Circuit 9: Common Mode Transient Immunity Test Circuit



$$CM_H = \frac{800(V)}{t_f(\mu s)} \quad CM_L = \frac{800(V)}{t_r(\mu s)}$$

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