

**Sensitive Gate Triacs
Silicon Bidirectional Thyristors**

**TRIACS
8 AMPERES RMS
600 VOLTS**

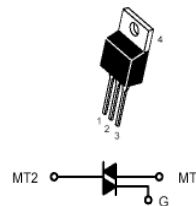
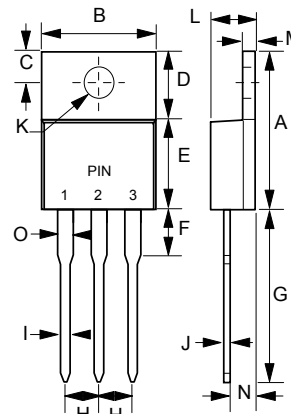
FEATURES

- Blocking Voltage to 600 Volts
- On-State Current Rating of 8.0 Amperes RMS at 100°C
- Uniform Gate Trigger Currents in Three Quadrants
- High Immunity to dv/dt - 500 V/ms minimum at 125°C
- Minimizes Snubber Networks for Protection
- Industry Standard TO-220AB Package
- High Commutating di/dt - 6.5 A/ms minimum at 125°C
- Pb-Free Package

MECHANICAL DATA

- Case: Molded plastic
- Weight: 0.07 ounces, 2.0 grams

TO-220AB



TO-220AB		
DIM.	MIN.	MAX.
A	14.22	15.88
B	9.65	10.67
C	2.54	3.43
D	5.84	6.86
E	8.26	9.28
F	-	6.35
G	12.70	14.73
H	2.29	2.79
I	0.51	1.14
J	0.40	0.67
K	3.53 $\varnothing$	4.09 $\varnothing$
L	3.56	4.83
M	1.14	1.40
N	2.03	2.92
O	1.17	1.37

All Dimensions in millimeter

PIN ASSIGNMENT	
1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

MAXIMUM RATINGS (Tj= 25°C unless otherwise noticed)

Rating	Symbol	Value	Unit
Peak Repetitive Off- State Voltage (1) (Tj= -40 to 125°C, Sine Wave, 50 to 60 Hz; Gate Open)	V _{DRM} , V _{RRM}	600	Volts
On-State RMS Current (Tc = 100°C) Full Cycle Sine Wave 50 to 60 Hz	I _{T(RMS)}	8.0	Amp
Peak Non-Repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, Tj =25°C)	I _{TSM}	80	Amps
Circuit Fusing Consideration (t = 8.3 ms)	I ² t	26	A ² s
Peak Gate Power (Tc = 80°C, Tp ≤1.0 us)	P _{GM}	16	Watt
Average Gate Power (Tc = 80°C, t = 8.3 ms)	P _{G(AV)}	0.35	Watt
Operating Junction Temperature Range	T _J	-40 to +125	°C
Storage Temperature Range	T _{stg}	-40 to +150	°C

Notice: (1) V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

REV. 7, Dec-2010, KTXC07

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance - Junction to Case - Junction to Ambient	RthJC RthJA	2.2 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Seconds	TL	260	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted, Electrical apply in both directions)

Characteristics	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Peak Repetitive Forward or Reverse Blocking Current (V _D =Rated V _{DRM} , V _{RRM} ; Gate Open)	T _J =25°C T _J =125°C	I _{DRM} I _{RRM}	----	----	10 2.0	uA mA
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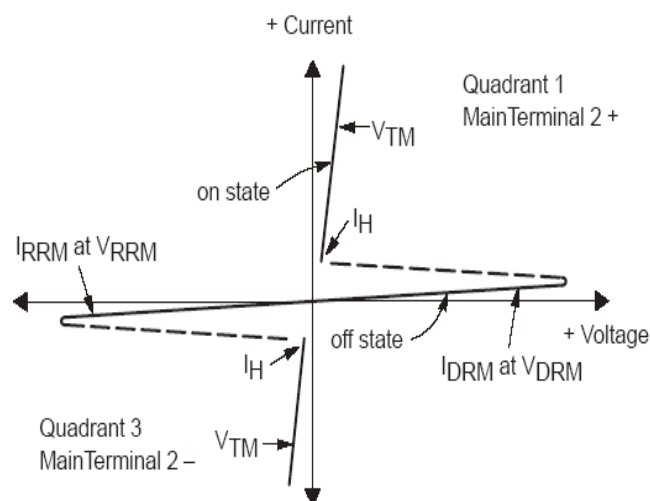
ON CHARACTERISTICS

Peak On-State Voltage (I _{TM} =± 11A Peak @T _p ≤ 2.0 ms, Duty Cycle ≤ 2%)	V _{TM}	----	1.2	1.6	Volts
Gate Trigger Current (V _D = 12V; R _L = 100 Ohms)	I _{GT1} I _{GT2} I _{GT3}	10 10 10	16 18 22	50 50 50	mA
Gate Trigger Voltage (V _D = 12 V; R _L = 100 Ohms)	V _{GT1} V _{GT2} V _{GT3}	0.5 0.5 0.5	0.69 0.77 0.72	1.5 1.5 1.5	Volts
Latching Current (V _D = 24 V, I _G = 50 mA)	I _{L1} I _{L2} I _{L3}	----	20 30 20	50 80 50	mA
Holding Current (V _D = 12 V, Initiating Current = ± 150 mA, Gate Open)	I _H	----	30	50	mA
Gate Non - Trigger Voltage (Main Terminal Voltage=12 V, R _L =100 Ohms, T _J =125°C)	V _{GD}	0.2	----	----	Volts

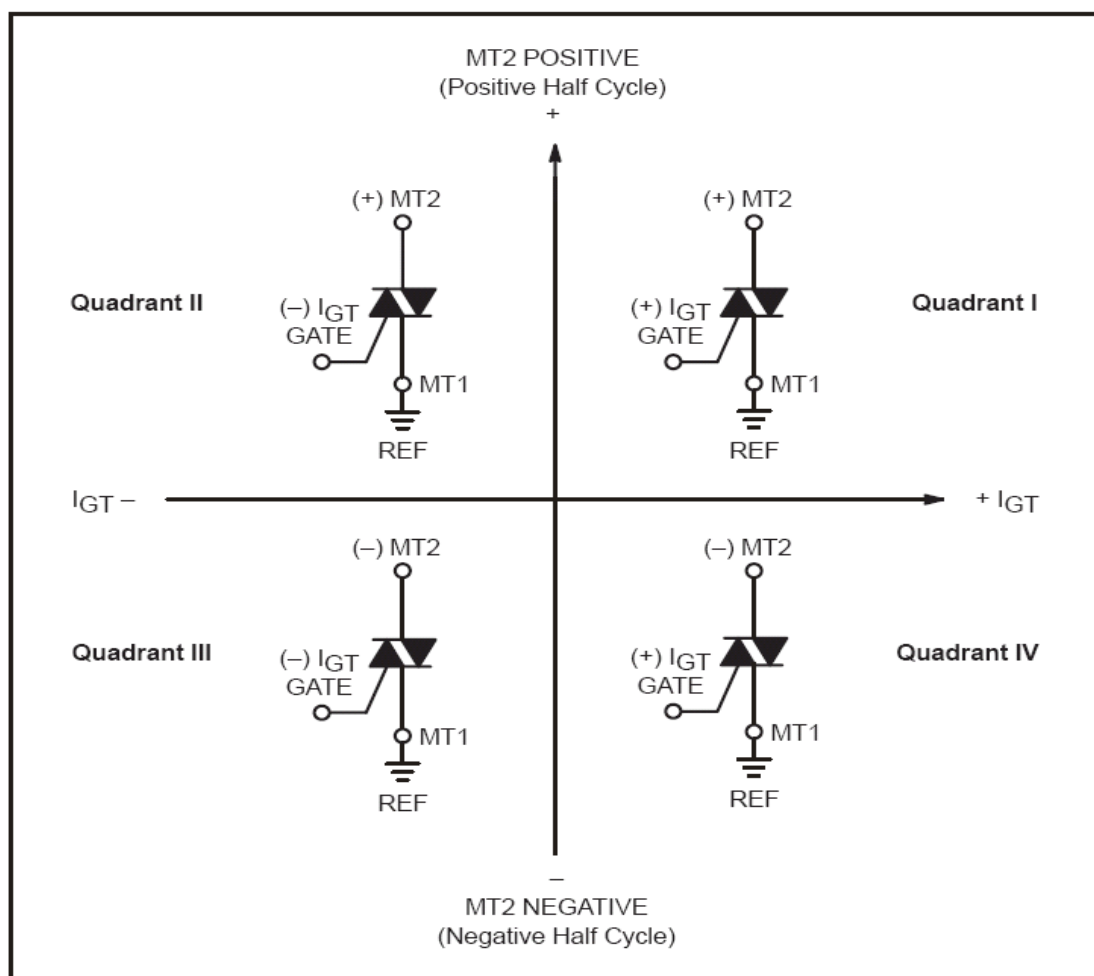
DYNAMIC CHARACTERISTICS

Critical Rate of Rise of Off-State Voltage (V _D =Rated V _{DRM} , Exponential Waveform, T _J =125°C)	dv/dt	500	----	----	V/us
Critical Rate of Rise of Commutation Current (V _D = 400V, I _{TM} = 4.4 A, Commutating di/dt = 18 V/us, Gate Open, T _J = 125°C, f=250Hz, C _L =10 uf, L _L =40 mH, No Snubber)	(di/dt) _c	6.5	----	----	A/ms

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions



All polarities are referenced to MT1

Whith in -phase signal (using standard AC lines) quadrants I and III are used

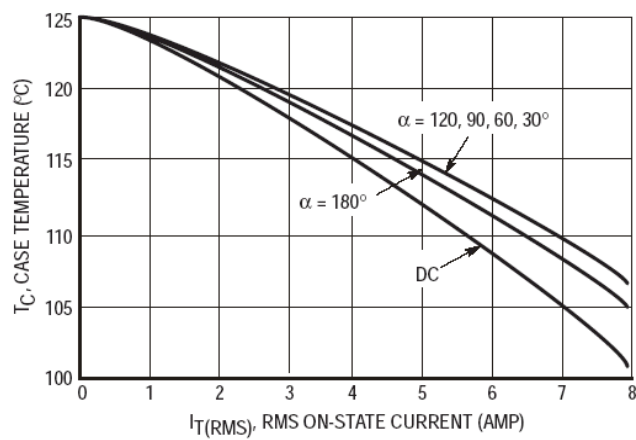


Figure 1. RMS Current Derating

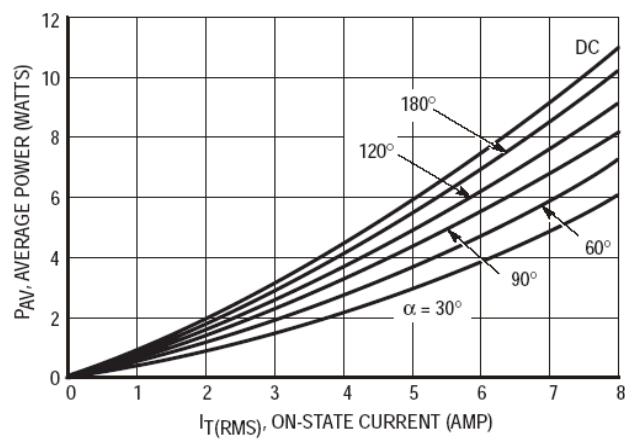


Figure 2. On-State Power Dissipation

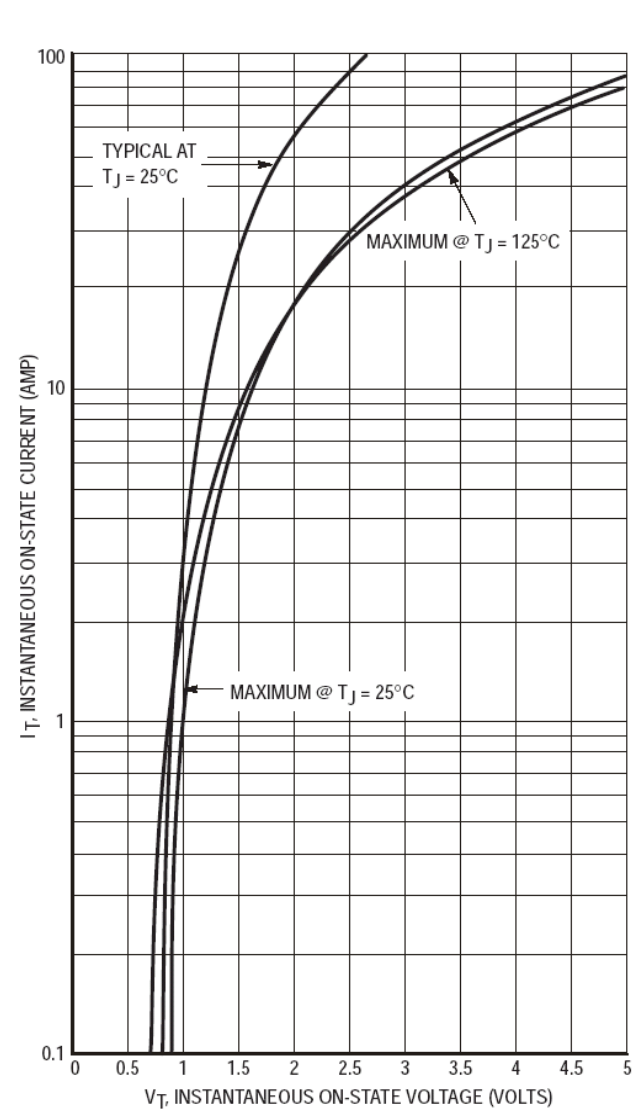


Figure 3. On-State Characteristics

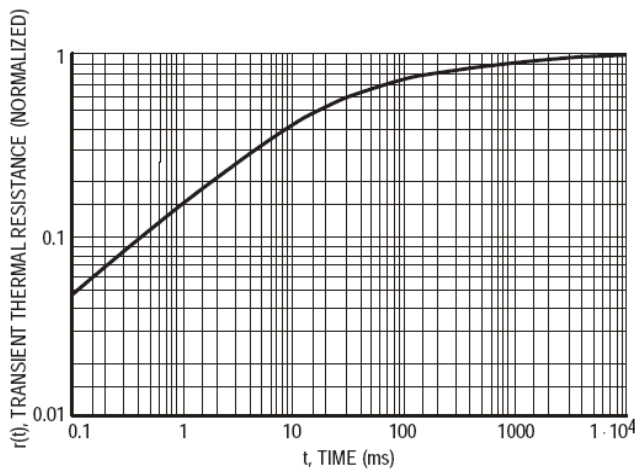


Figure 4. Thermal Response

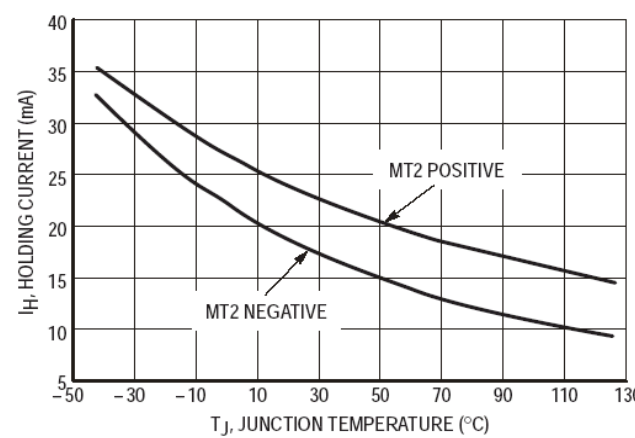


Figure 5. Holding Current Variation

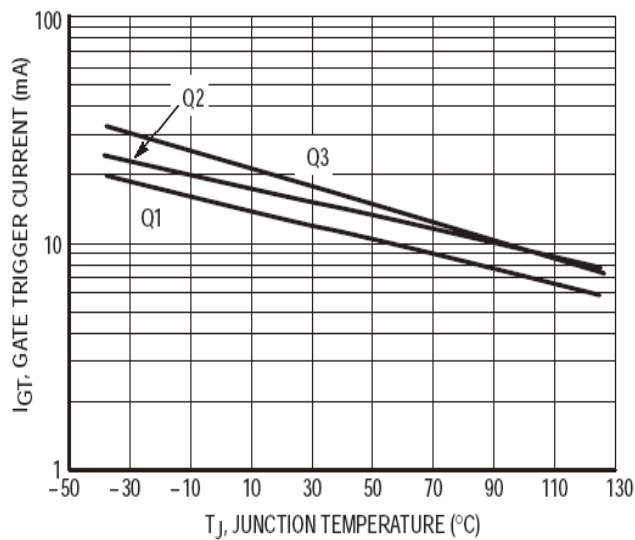


Figure 6. Gate Trigger Current Variation

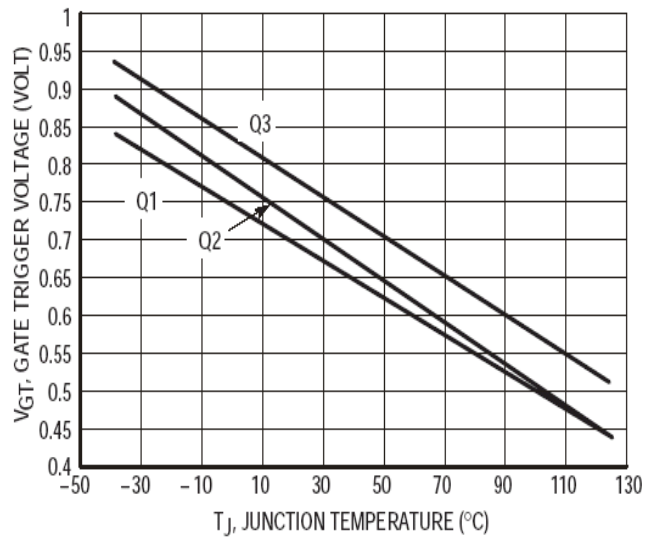


Figure 7. Gate Trigger Voltage Variation

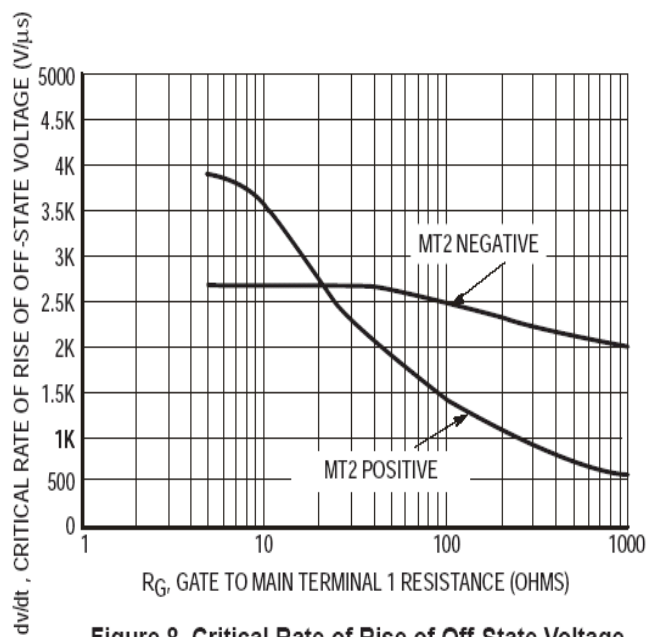


Figure 8. Critical Rate of Rise of Off-State Voltage (Exponential)

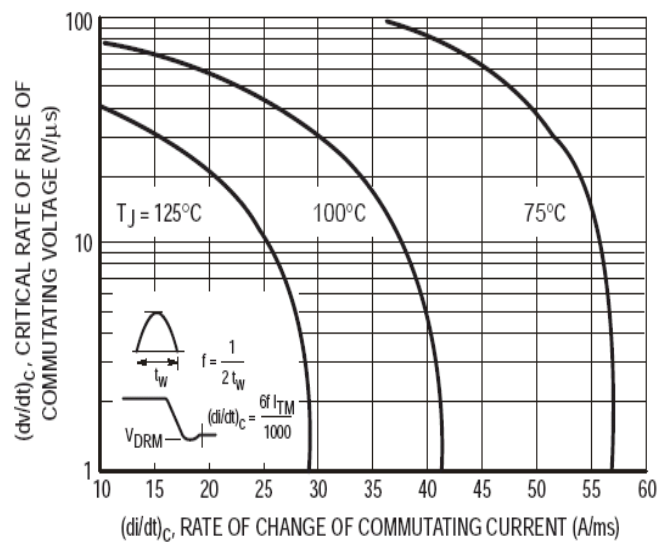


Figure 9. Critical Rate of Rise of Commutating Voltage

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