Data Sheet

ADuM5010

Integrated DC-to-DC Converter

FEATURES

- *iso*Power integrated, isolated dc-to-dc converter
- Regulated 3.15 V to 5.25 V output
- Up to 150 mW output power
- 20-lead SSOP package with 5.3 mm creepage
- High temperature operation: 105°C
- High common-mode transient immunity: >25 kV/µs
- Safety and regulatory approvals
  - UL 1577
    - V_{ISO} = 2500 V rms for 1 minute.
  - IEC/CSA 62368-1
  - IEC/CSA 61010-1
  - CQC GB 4943.1
  - DIN EN IEC 60747-17 (VDE 0884-17)
    - V_{IORM} = 600 V peak

APPLICATIONS

- Power supply start-up bias and gate drives
- Isolated sensor interfaces
- Industrial PLCs

FUNCTIONAL BLOCK DIAGRAM

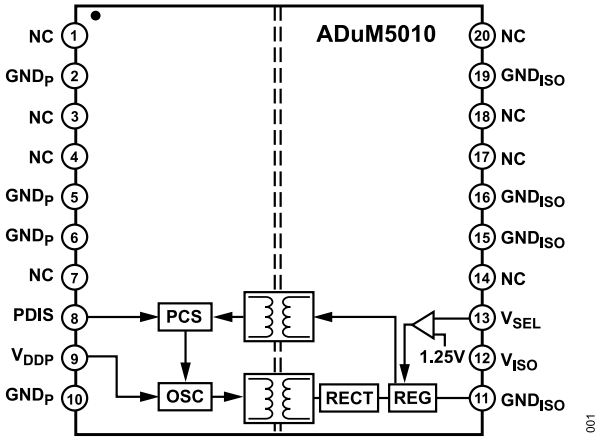

Figure 1.

GENERAL DESCRIPTION

The ADuM5010[1] is an integrated, isolated dc-to-dc converter. Based on the Analog Devices, Inc., *i*Coupler® technology, the dc-to-dc converter provides regulated, isolated power, adjustable between 3.15 V and 5.25 V. Input supply voltages can range from slightly below the required output to significantly higher. Popular combinations and their associated power levels are shown in Table 1.

The *i*Coupler chip-scale transformer technology is used for isolated logic signals and for the magnetic components of the dc-to-dc converter. The result is a small form factor, total isolation solution.

*iso*Power uses high frequency switching elements to transfer power through its transformer. Special care must be taken during printed circuit board (PCB) layout to meet emissions standards. See the AN-0971 Application Note for board layout recommendations.

Table 1. Power Levels

Input Voltage (V)	Output Voltage (V)	Output Power (mW)
5	5	150
5	3.3	100
3.3	3.3	66

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

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REVISION HISTORY

9/2025—Rev. B to Rev. C

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2/2025—Rev. A to Rev. B

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Changes to Table 10 ... 6
Changed DIN EN IEC 60747-17 (VDE V 0884-10) Insulation Characteristics Section to DIN EN IEC 60747-17 (VDE V 0884-17) Insulation Characteristics Section ... 7
Changes to DIN EN IEC 60747-17 (VDE V 0884-17) Insulation Characteristics Section, Table 11, and Figure 2 Caption ... 7
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Deleted Figure 19 to Figure 21; Renumbered Sequentially ... 14

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/5 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, V_{DDP} = V_{ISO} = 5 V, V_{SEL} resistor network: R1 = 10 kΩ, R2 = 30.9 kΩ. Minimum/maximum specifications apply over the entire recommended operation range which is 4.5 V ≤ V_{DDP}, V_{SEL}, V_{ISO} ≤ 5.5 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 2. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V_{ISO}		5.0		V	I_{ISO} = 15 mA, R1 = 10 kΩ, R2 = 30.9 kΩ
Thermal Coefficient	$V_{ISO (TC)}$		−44		µV/°C	
Line Regulation	$V_{ISO (LINE)}$		20		mV/V	I_{ISO} = 15 mA, V_{DDP} = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1.3	3	%	I_{ISO} = 3 mA to 27 mA
Output Ripple	$V_{ISO (RIP)}$		75		mV p-p	20 MHz bandwidth, C_{BO} = 0.1 µF||10 µF, I_{ISO} = 27 mA
Output Noise	$V_{ISO (NOISE)}$		200		mV p-p	C_{BO} = 0.1 µF||10 µF, I_{ISO} = 27 mA
Switching Frequency	f_{OSC}		125		MHz	
Pulse Width Modulation Frequency	f_{PWM}		600		kHz	
Output Supply	$I_{ISO (MAX)}$	30			mA	V_{ISO} > 4.5 V
Efficiency at $I_{ISO (MAX)}$			29		%	I_{ISO} = 27 mA
I_{DDP}, No V_{ISO} Load	$I_{DD1 (Q)}$		6.8	12	mA	
I_{DDP}, Full V_{ISO} Load	$I_{DD1 (MAX)}$		104		mA	
Thermal Shutdown						
Shutdown Temperature			154		°C	
Thermal Hysteresis			10		°C	

Table 3. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDP}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDP}	V	
Undervoltage Lockout						V_{ISO}, V_{DDP} supply
Positive Going Threshold	V_{UV+}		2.7		V	
Negative Going Threshold	V_{UV-}		2.4		V	
Input Currents per Channel	I_{PDIS}	−10	+0.01	+10	µA	0 V ≤ V_{PDIS} ≤ V_{DDP}

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—3.3 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, V_{DDP} = V_{ISO} = 3.3 V, V_{SEL} resistor network: R1 = 10 kΩ, R2 = 16.9 kΩ. Minimum/maximum specifications apply over the entire recommended operation range which is 3.0 V ≤ V_{DDP}, V_{SEL}, V_{ISO} ≤ 3.6 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 4. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V_{ISO}		3.3		V	I_{ISO} = 10 mA, R1 = 10 kΩ, R2 = 16.9 kΩ
Thermal Coefficient	$V_{ISO (TC)}$		−26		µV/°C	I_{ISO} = 20mA
Line Regulation	$V_{ISO (LINE)}$		20		mV/V	I_{ISO} = 10 mA, V_{DDP} = 3.0 V to 3.6 V
Load Regulation	$V_{ISO (LOAD)}$		1.3	3	%	I_{ISO} = 2 mA to 18 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{BO} = 0.1 µF||10 µF, I_{ISO} = 18 mA
Output Noise	$V_{ISO (NOISE)}$		130		mV p-p	C_{BO} = 0.1 µF||10 µF, I_{ISO} = 18 mA
Switching Frequency	f_{OSC}		125		MHz	
Pulse Width Modulation Frequency	f_{PWM}		600		kHz	
Output Supply	$I_{ISO (MAX)}$	20			mA	3.6 V > V_{ISO} > 3 V
Efficiency at $I_{ISO (MAX)}$			27		%	I_{ISO} = 18 mA
I_{DD1}, No V_{ISO} Load	$I_{DD1 (Q)}$		3.3	10.5	mA	
I_{DD1}, Full V_{ISO} Load	$I_{DD1 (MAX)}$		77		mA	
Thermal Shutdown						
Shutdown Temperature			154		°C	
Thermal Hysteresis			10		°C	

Table 5. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDP}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDP}	V	
Undervoltage Lockout						V_{DDP} supply
Positive Going Threshold	V_{UV+}		2.7		V	
Negative Going Threshold	V_{UV-}		2.4		V	
Input Currents per Channel	I_{PDIS}	−10	+0.01	+10	µA	0 V ≤ V_{PDIS} ≤ V_{DDP}

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, V_{DDP} = 5.0 V, V_{ISO} = 3.3 V, V_{SEL} resistor network: R1 = 10 kΩ, R2 = 16.9 kΩ. Minimum/maximum specifications apply over the entire recommended operation range which is 4.5 V ≤ V_{DDP} ≤ 5.5 V, 3.0 V ≤ V_{ISO} ≤ 3.6 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 6. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V_{ISO}		3.3		V	I_{ISO} = 15 mA, R1 = 10 kΩ, R2 = 16.9 kΩ
Thermal Coefficient	$V_{ISO (TC)}$		−26		µV/°C	
Line Regulation	$V_{ISO (LINE)}$		20		mV/V	I_{ISO} = 15 mA, V_{DD1} = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1.3	3	%	I_{ISO} = 3 mA to 27 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{BO} = 0.1 µF||10 µF, I_{ISO} = 27 mA
Output Noise	$V_{ISO (NOISE)}$		130		mV p-p	C_{BO} = 0.1 µF||10 µF, I_{ISO} = 27 mA
Switching Frequency	f_{OSC}		125		MHz	
Pulse Width Modulation Frequency	f_{PWM}		600		kHz	
Output Supply	$I_{ISO (MAX)}$	30			mA	3.6 V > V_{ISO} > 3 V
Efficiency at $I_{ISO (MAX)}$			24		%	I_{ISO} = 27 mA
I_{DD1}, No V_{ISO} Load	$I_{DD1 (Q)}$		3.2	8	mA	
I_{DD1}, Full V_{ISO} Load	$I_{DD1 (MAX)}$		85		mA	
Thermal Shutdown						
Shutdown Temperature			154		°C	
Thermal Hysteresis			10		°C	

Table 7. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDP}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDP}	V	
Undervoltage Lockout						V_{ISO}, V_{DDP} supply
Positive Going Threshold	V_{UV+}		2.7		V	
Negative Going Threshold	V_{UV-}		2.4		V	
Input Currents per Channel	I_{PDIS}	−10	+0.01	+10	µA	0 V ≤ V_{PDIS} ≤ V_{DDP}

SPECIFICATIONS

PACKAGE CHARACTERISTICS

Table 8. Thermal and Isolation Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	θ_{JA}		50		°C/W	Thermocouple located at center of package underside, test conducted on 4-layer board with thin traces[3]

1 The device is considered a 2-terminal device: Pin 1 through Pin 10 are shorted together; and Pin 11 through Pin 20 are shorted together.

2 Input capacitance is from any input data pin to ground.

3 See the Thermal Analysis section for thermal model definitions.

REGULATORY APPROVALS

The ADuM5010 certification approvals are listed in Table 9.

Table 9. ADuM5010 Regulatory Approvals

UL	CSA	CQC	VDE[2]
UL 1577[1] Single protection, 2500 V rms	IEC/CSA 62368-1 Basic insulation, 530 V rms Reinforced insulation, 265 V rms IEC/CSA 61010-1 Basic insulation, 300 V rms, overvoltage category II Reinforced insulation, 150 V rms	GB4943.1 Basic insulation, 520 V rms	DIN EN IEC 60747-17 (VDE 0884-17)[2] Reinforced insulation, 600 V peak
File E214100	File 205078	Certificate No. CQC17001171585	File 40051926

1 In accordance with UL 1577, each ADuM5010 is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 10 µA).

2 In accordance with DIN EN IEC 60747-17 (VDE 0884-17), ADuM5010 is proof tested by applying an insulation test voltage ≥1125 V peak for 1 second (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN EN IEC 60747-17 (VDE 0884-17) approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 10. Critical Safety-Related Dimensions and Material Properties

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)[1, 2]	L(I01)	5.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)[2]	L(I02)	5.3	mm	Measured from input terminals to output terminals,shortest distance path along body
Minimum Internal Gap (Internal Clearance)		21.5	µm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN IEC 112/VDE 0303, Part 1
Material Group		I		Material group per IEC 60664-1

1 Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained

2 In accordance with IEC 62368-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 m.

SPECIFICATIONS

DIN EN IEC 60747-17 (VDE V 0884-17) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by the protective circuits. The asterisk (*) marking on packages denotes DIN EN IEC 60747-17 (VDE 0884-17) approval.

Table 11. VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Overvoltage Category per IEC 60664-1				
≤ 150 V rms			I to IV	
≤ 300 V rms			I to III	
≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Repetitive Isolation Voltage		V_{IORM}	600	V peak
Maximum Working Insulation Voltage		V_{IOWM}	424	V rms
Input-to-Output Test Voltage, Method b1	V_{IORM} × 1.875 = $V_{pd(m)}$, 100% production test, t_{ini} = t_m = 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	1125	V peak
Input-to-Output Test Voltage, Method a				
After Environmental Tests Subgroup 1	V_{IORM} × 1.6 = $V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	960	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	720	V peak
Maximum Transient Isolation voltage	V_{TEST} = 1.2 × V_{IOTM}, t =1s (100% production)	V_{IOTM}	4000	V peak
Maximum Impulse Voltage	Surge voltage in air, waveform per IEC 61000-4-5	V_{IMP}	4000	V peak
Maximum Surge Isolation Voltage	V_{TEST} ≥ 1.3 × V_{IMP} (sample test), tested in oil, waveform per IEC 61000-4-5	V_{IOSM}	10000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure			
Case Temperature	(see Figure 2)	T_S	150	°C
Safety Total Dissipated Power		I_{S1}	2.5	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	>109	Ω

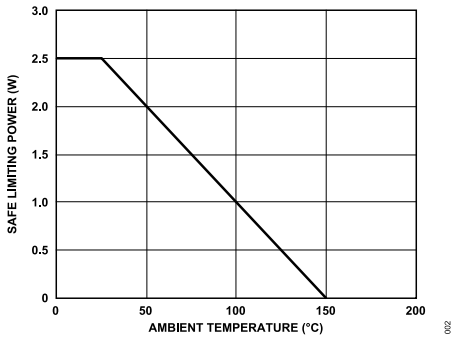

Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN EN IEC 60747-17 (VDE V 0884-17)

RECOMMENDED OPERATING CONDITIONS

Table 12.

Parameter	Symbol	Min	Max	Unit
Operating Temperature[1]	T_A	−40	+105	°C
Supply Voltages[2]				
V_{DD1} at V_{SEL} = 0 V	V_{DD}	3.0	5.5	V
V_{DD1} at V_{SEL} = V_{ISO}		4.5	5.5	V

SPECIFICATIONS

[1] Operation at 105°C requires reduction of the maximum load current as specified in Table 13.

[2] Each voltage is relative to its respective ground.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 13.

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Ambient Operating Temperature (T_A)	−40°C to +105°C
Supply Voltages (V_{DDP}, V_{ISO})[1]	−0.5 V to +7.0 V
V_{ISO} Supply Current[2]	
T_A = −40°C to +105°C	30 mA
Input Voltage (PDIS, V_{SEL})[1, 3]	−0.5 V to V_{DD} + 0.5 V
Common-Mode Transients[4]	−100 kV/µs to +100 kV/µs

1 All voltages are relative to their respective ground.

2 The VISO provides current for dc and dynamic loads on the VISO I/O channels. This current must be included when determining the total VISO supply current.

3 VDD can be either VDDP or VISO depending on the whether the input is on the primary or secondary side of the part respectively.

4 Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability

Table 14. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Applicable Certification
AC Voltage			
Bipolar Waveform	600	V peak	Reinforced insulation rating per IEC 60747-17

1 Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

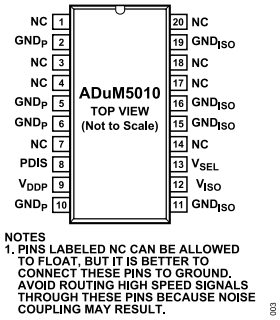

Figure 3. Pin Configuration

Table 15. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 4, 7, 14, 17, 18, 20	NC	This pin is not connected internally (see Figure 3).
2, 5, 6, 10	GND_P	Ground 1. Ground reference for isolator primary. Pin 2 and Pin 10 are internally connected, and it is recommended that all pins be connected to a common ground.
8	PDIS	Power Disable. When this pin is tied to GND_P the power converter is active; when a logic high voltage is applied, the power supply enters a low power standby mode.
9	V_{DDP}	Primary Supply Voltage, 3.0 V to 5.5 V.
11, 15, 16, 19	GND_{ISO}	Ground Reference for Isolator Side 2. Pin 19 and Pin 11 are internally connected, and it is recommended that all pins be connected to a common ground.
12	V_{ISO}	Secondary Supply Voltage Output for External Loads, 3.15 V to 5.5 V depending on voltage divider connected to V_{SEL}.
13	V_{SEL}	Output Voltage select input. A voltage divider attached to this pin between V_{ISO} and GND_{ISO} determines the value of V_{ISO}, see Equation 1.

TRUTH TABLE

Table 16. Truth Table (Positive Logic)

V_{DDP} (V)	V_{SEL} Input	PDIS Input	V_{ISO} Output (V)	Notes
5	R1 = 10 kΩ, R2 = 30.9 kΩ	Low	5	
5	R1 = 10 kΩ, R2 = 30.9 kΩ	High	0	
3.3	R1 = 10 kΩ, R2 = 16.9 kΩ	Low	3.3	
3.3	R1 = 10 kΩ, R2 = 16.9 kΩ	High	0	
5	R1 = 10 kΩ, R2 = 16.9 kΩ	Low	3.3	
5	R1 = 10 kΩ, R2 = 16.9 kΩ	High	0	
3.3	R1 = 10 kΩ, R2 = 30.9 kΩ	Low	5	Configuration not recommended
3.3	R1 = 10 kΩ, R2 = 30.9 kΩ	High	0	

TYPICAL PERFORMANCE CHARACTERISTICS

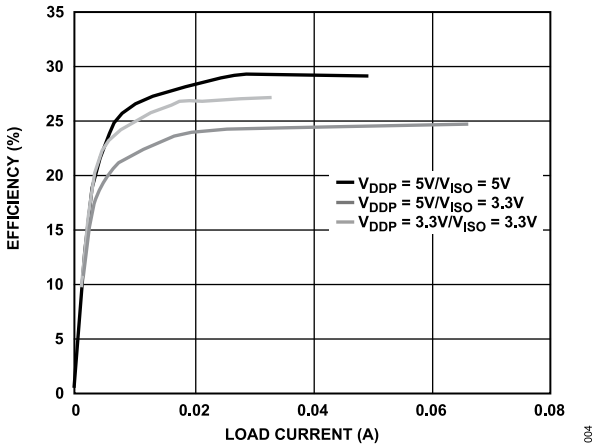

Figure 4. Typical Power Supply Efficiency at 5 V/5 V, 5 V/3.3 V, and 3.3 V/3.3 V

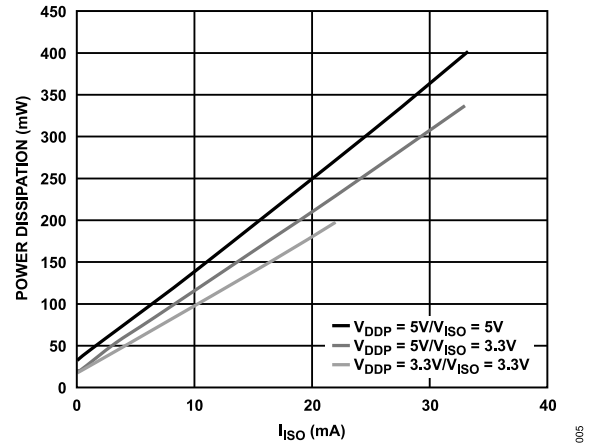

Figure 5. Typical Total Power Dissipation vs. I_{ISO}

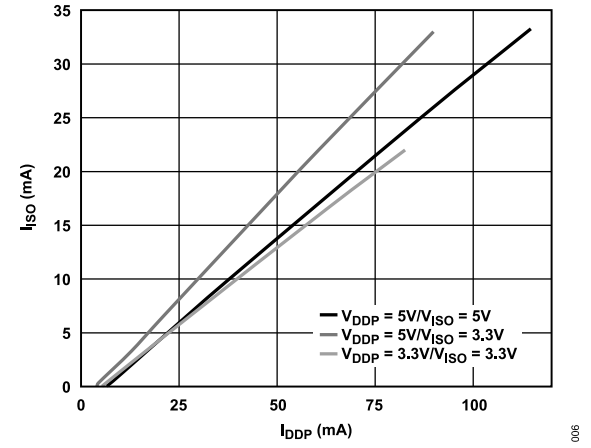

Figure 6. Typical Isolated Output Supply Current, I_{ISO}, as a Function of External Load, at 5 V/5 V, 5 V/3.3 V, and 3.3 V/3.3 V

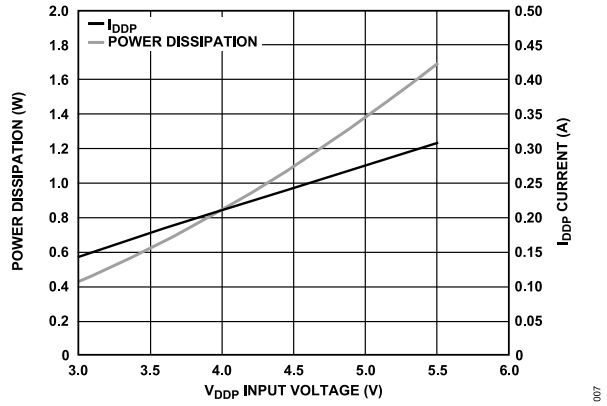

Figure 7. Typical Short-Circuit Input Current and Power vs. V_{DDP} Supply Voltage

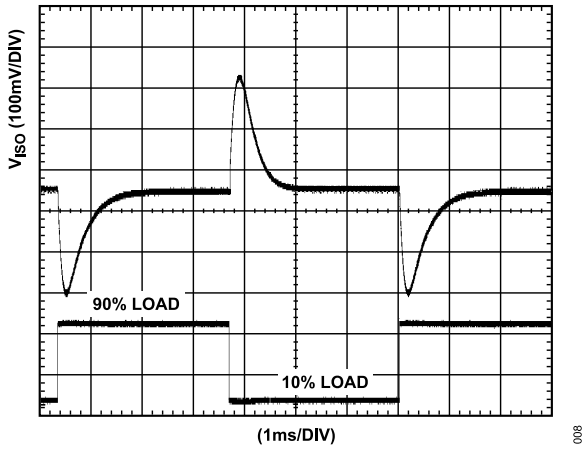

Figure 8. Typical V_{ISO} Transient Load Response, 5 V Output, 10% to 90% Load Step

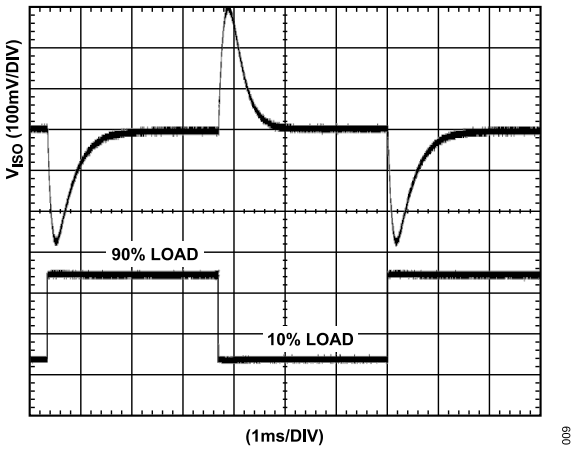

Figure 9. Typical Transient Load Response, 3.3 V Input, 3.3 V Output, 10% to 90% Load Step

TYPICAL PERFORMANCE CHARACTERISTICS

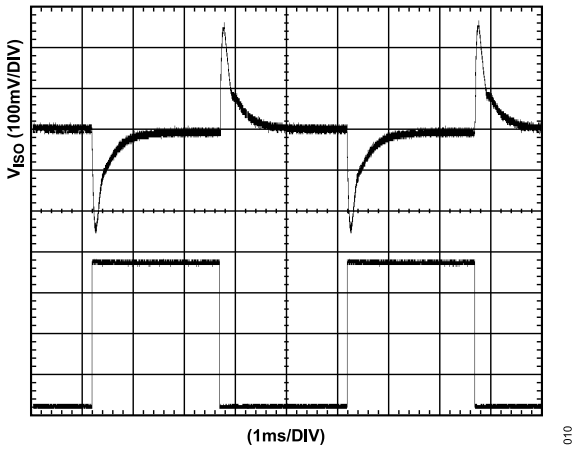

Figure 10. Typical Transient Load Response, 5 V Input, 3.3 V Output, 10% to 90% Load Step

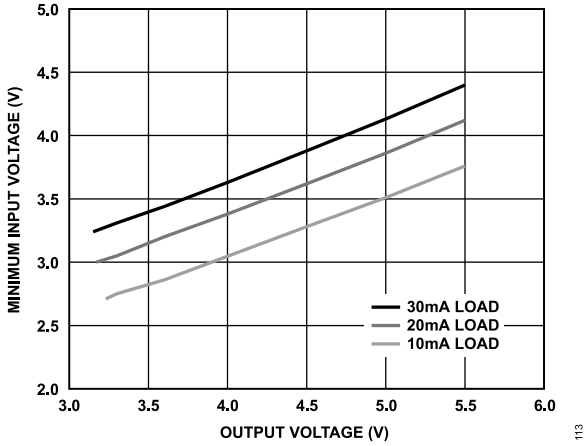

Figure 13. Relationship Between Output Voltage and Required Input Voltage, Under Load, to Maintain >80% Duty Factor in the PWM

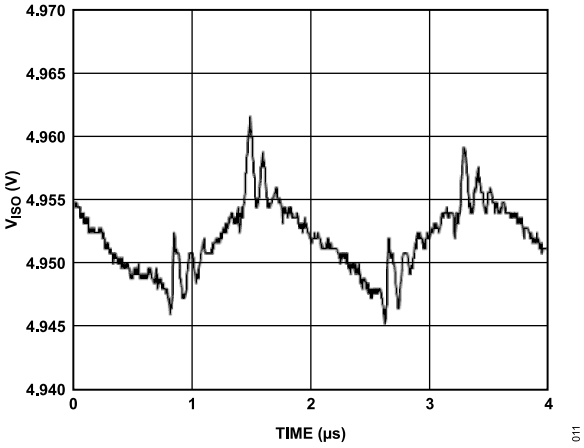

Figure 11. Typical V_{ISO} = 5 V Output Voltage Ripple at 90% Load

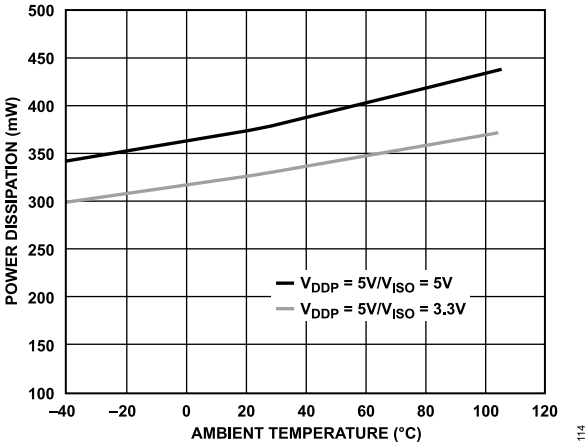

Figure 14. Power Dissipation with a 30 mA Load vs. Temperature

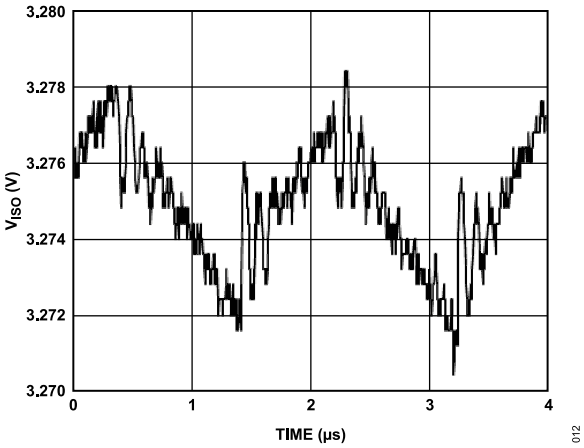

Figure 12. Typical V_{ISO} = 3.3 V Output Voltage Ripple at 90% Load

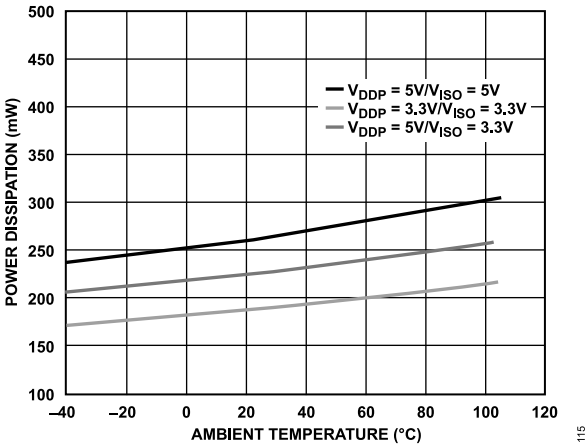

Figure 15. Power Dissipation with a 20 mA Load vs. Temperature

APPLICATIONS INFORMATION

The dc-to-dc converter section of the ADuM5010 works on principles that are common to most modern power supplies. It has split controller architecture with isolated pulse-width modulation (PWM) feedback. V_{DDP} power is supplied to an oscillating circuit that switches current into a chip-scale air core transformer. Power transferred to the secondary side is rectified and regulated to a value between 3.15 V and 5.25 V depending on the setpoint supplied by an external voltage divider (see Equation 1). The secondary (V_{ISO}) side controller regulates the output by creating a PWM control signal that is sent to the primary (V_{DDP}) side by a dedicated *i*Coupler data channel. The PWM modulates the oscillator circuit to control the power being sent to the secondary side. Feedback allows for significantly higher power and efficiency.

$$V_{ISO} = 1.23\ \text{V} \frac{(R1 + R2)}{R1} \quad (1)$$

where:
R1 is a resistor between V_{SEL} and GND_{ISO}.
R2 is a resistor between V_{SEL} and V_{ISO}.

Because the output voltage can be adjusted continuously there are an infinite number of operating conditions. This data sheet addresses three discrete operating conditions in the Specifications tables. Many other combinations of input and output voltage are possible; Figure 13 depicts the supported voltage combinations at room temperature. Figure 13 was generated by fixing the V_{ISO} load and decreasing the input voltage until the PWM was at 80% duty cycle. Each of the curves represents the minimum input voltage that is required for operation under this criterion. For example, if the application requires 30 mA of output current at 5 V, the minimum input voltage at V_{DDP} is 4.25 V. Figure 13 also illustrates why the V_{DDP} = 3.3 V input and V_{ISO} = 5 V configuration is not recommended. Even at 10 mA of output current, the PWM cannot maintain less than 80% duty factor, leaving no margin to support load or temperature variations.

Typically, the ADuM5010 dissipates about 17% more power between room temperature and maximum temperature; therefore, the 20% PWM margin covers temperature variations.

The ADuM5010 implements undervoltage lockout (UVLO) with hysteresis on the primary and secondary sides I/O pins as well as the V_{DDP} power input. This feature ensures that the converter does not go into oscillation due to noisy input power or slow power-on ramp rates.

PCB LAYOUT

The ADuM5010 digital isolator, with a 0.15 W *iso*Power integrated dc-to-dc converter, requires no external interface circuitry for the logic interfaces. Power supply bypassing with a low ESR capacitor is required as close to the chip pads as possible. The *iso*Power inputs require several passive components to bypass the power effectively as well as to set the output voltage and to bypass the core voltage regulator (see Figure 16 through Figure 18).

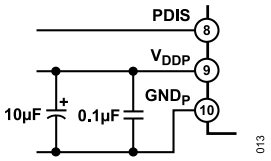

Figure 16. V_{DDP} Bias and Bypass Components

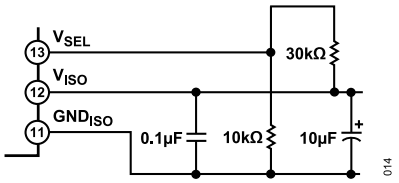

Figure 17. V_{ISO} Bias and Bypass Components

The power supply section of the ADuM5010 uses a 125 MHz oscillator frequency to efficiently pass power through its chip-scale transformers. Bypass capacitors must do more than one job and must be chosen carefully. Noise suppression requires a low inductance, high frequency capacitor; ripple suppression and proper regulation require a large value bulk capacitor. These capacitors are most conveniently connected between Pin 9 and Pin 10 for V_{DDP} and between Pin 11 and Pin 12 for V_{ISO}. To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required. The recommended capacitor values are 0.1 µF and 10 µF for V_{DD1}. The smaller capacitor must have a low ESR; for example, use of an NPO or X5R ceramic capacitor is advised. Ceramic capacitors are also recommended for the 10 mF bulk capacitance. An additional 10 nF capacitor can be added in parallel if further EMI/EMC control is desired.

Note that the total lead length between the ends of the low ESR capacitor and the input power supply pin must not exceed 2 mm.

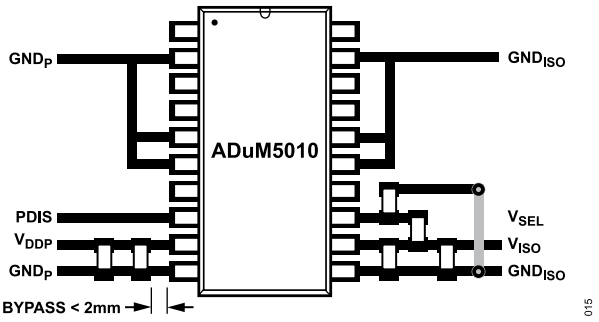

Figure 18. Recommended PCB Layout

In applications involving high common-mode transients, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins, exceeding the absolute

APPLICATIONS INFORMATION

maximum ratings specified in Table 13, and thereby leading to latch-up and/or permanent damage.

THERMAL ANALYSIS

The ADuM5010 consist of two internal die attached to a split lead frame with two die attach paddles. For the purposes of thermal analysis, the chip is treated as a thermal unit, with the highest junction temperature reflected in the θ_{JA} from Table 8. The value of θ_{JA} is based on measurements taken with the parts mounted on a JEDEC standard, 4-layer board with fine width traces and still air. Under normal operating conditions, the ADuM5010 can operate at full load across the full temperature range without derating the output current.

Power dissipation in the part varies with ambient temperature due to the characteristics of the switching and rectification elements. Figure 14 and Figure 15 show the relationship between total power dissipation at two load conditions and ambient temperature. This information can be used to determine the junction temperature at various operating conditions to ensure that the part does not go into thermal shutdown unexpectedly.

EMI CONSIDERATIONS

The dc-to-dc converter section of the ADuM5010 components must, of necessity, operate at a very high frequency to allow efficient power transfer through the small transformers. This creates high frequency currents that can propagate in circuit board ground and power planes, causing edge and dipole radiation. Grounded enclosures are recommended for applications that use these devices. If grounded enclosures are not possible, follow good RF design practices in the layout of the PCB. See the AN-0971 Application Note at www.analog.com for the most current PCB layout recommendations for the ADuM5010.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. Analog Devices conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM5010.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 14 summarize the maximum continuous working voltages as per IEC 60747-17. Operation at working voltages higher than the service life voltage listed leads to premature insulation failure.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
RS-20	SSP	20-Lead Shrink Small Outline Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADuM5010ARSZ	−40°C to +105°C	20-Lead SSOP	RS-20
ADuM5010ARSZ-RL7	−40°C to +105°C	20-Lead SSOP	RS-20

[1] Tape and reel are available. The addition of an RL suffix designates a 7" tape and reel option.

[2] Z = RoHS Compliant Part.