Single-Chip, Li-Ion Charge Management IC for Handheld Applications (bqTINY™)

Check for Samples: bq24010, bq24012, bq24013, bq24014, bq24018

FEATURES

- **Small 3-mm × 3-mm MLP (QFN) Package**
- **Ideal for Low-Dropout Designs for Single-Cell Li-Ion or Li-Pol Packs in Space Limited Applications**
- **Integrated Power FET and Current Sensor for Up to 1-A Charge Applications**
- **Reverse Leakage Protection Prevents Battery Drainage**
- **Integrated Current and Voltage Regulation**
- **±0.5% Voltage Regulation Accuracy**
- **Charge Termination by Minimum Current and Time**
- **Pre-Charge Conditioning With Safety Timer**
- **Status Outputs for LED or System Interface Indicates Charge and Fault Conditions**
- **Battery Insertion and Removal Detection**
- **Works With Regulated and Unregulated Supplies**
- **Short-Circuit Protection**
- **Charge Voltage Options: 4.2 V and 4.36 V**

APPLICATIONS

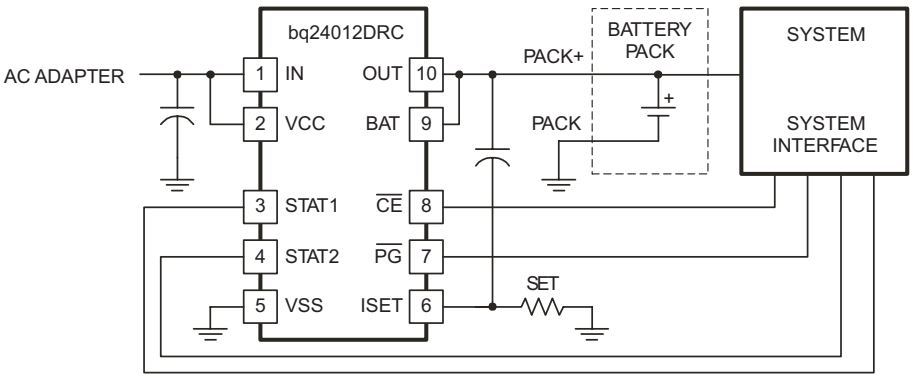
- **Cellular Phones**
- **PDAs**
- **MP3 Players**
- **Digital Cameras**
- **Internet Appliances**

DESCRIPTION

The bqTINY™ series are highly integrated Li-Ion and Li-Pol linear charge management devices targeted at space limited portable applications. The bqTINY™ series offer integrated powerFET and current sensor, reverse blocking protection, high accuracy current and voltage regulation, charge status, and charge termination, in a small package.

The bqTINY™ charges the battery in three phases: conditioning, constant current, and constant voltage. Charge is terminated based on minimum current. An internal charge timer provides a backup safety feature for charge termination. The bqTINY™ automatically restarts the charge if the battery voltage falls below an internal threshold. The bqTINY™ automatically enters sleep mode when V_{CC} supply is removed.

In addition to the standard features, different versions of the bqTINY™ offer a multitude of additional features. These include temperature sensing input for detecting hot or cold battery packs; power good ($\overline{PG}$) output indicating the presence of valid input power; a TTL-level charge-enable input (CE) used to disable or enable the charge process; and a TTL-level timer and termination enable (TTE) input used to disable or enable the fast-charge timer and charge termination.



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bqTINY is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

			VALUE	UNIT
	Supply voltage range, (V_{CC} all with respect to V_{SS})		–0.3 to 18	V
	Input voltage range(2)	IN, STAT1, STAT2, TS, $\overline{PG}$, $\overline{CE}$, $\overline{TTE}$	–0.3 to VCC	V
		BAT, OUT, ISET	–0.3 to 7	VDC
	Voltage difference between V_{CC} and IN inputs V_{CC} – V_{IN}		±0.5	V
	Output sink/source current	STAT1, STAT2, $\overline{PG}$	15	
	Output current	IN, OUT	1.5	
T_A	Operating free-air temperature range		–40 to 125	°C
T_J	Junction temperature range			
T_{stg}	Storage temperature		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are DC and with respect to VSS.

DISSIPATION RATINGS

PACKAGE	θ_{JA}	T_A < 40°C POWER RATING	DERATING FACTOR ABOVE T_A = 40°C
DRC(1)	47°C/W	1.5 W	0.021 W/°C1

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a copper pad on the board. This is connected to the ground plane by a 2x3 via matrix.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage(1) (2)	3		16.5	V
V_{IN}	Input voltage(1) (2)	3		16.5	V
T_J	Operating junction temperature range	–40		125	°C

(1) Pins V_{CC} and IN must be tied together.
(2) If Vin is between UVLO and 4.35V, and above the battery voltage, then the IC is active (can deliver some charge to the battery), but the IC will have limited or degraded performance (some functions may not meet data sheet specifications). The battery may be undercharged ($V_{O(reg)}$ less than in the specification), but will not be overcharged ($V_{O(reg)}$ will not exceed specification).

ELECTRICAL CHARACTERISTICS

over 0°C ≤ T_J ≤ 125°C and recommended supply voltage, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENT						
$I_{CC(VCC)}$	VCC current	V_{CC} > $V_{CC(min)}$, STATx pins in OFF state	0	3.5	5	mA
$I_{CC(SLP)}$	Sleep current	Sum of currents into OUT and BAT pins, V_{CC} < $V_{(SLP)}$			5	µA
$I_{IB(BAT)}$	Input bias current on BAT pin				500	nA
$I_{IB(TS)}$	Input current on TS pin	$V_{I(TS)}$ ≤ 10 V			1	µA
$I_{IB(CE)}$	Input current on $\overline{CE}$ pin				1	
$I_{IB(\overline{TTE})}$	Input bias current on $\overline{TTE}$ pin				1	
VOLTAGE REGULATION $V_{O(REG)}$ + $V_{(DO-MAX)}$ ≤ V_{CC}, $I_{(TERM)}$ < $I_{O(OUT)}$ ≤ 1 A						
	Output voltage, $V_{O(REG)}$	bq24010, bq24012, bq24013, bq24014		4.2		V
		bq24018		4.36		

ELECTRICAL CHARACTERISTICS (continued)

over 0°C ≤ T_J ≤ 125°C and recommended supply voltage, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Voltage regulation accuracy	T_A = 25°C		–0.5%		0.5%	
				–1%		1%	
$V_{(DO)}$	Dropout voltage ($V_{(IN)} – V_{(OUT)}$)	$V_{O(REG)} + V_{(DO–MAX)}) \le V_{CC}$, $I_{O(OUT)}$ = 1A			650	790	mV
CURRENT REGULATION							
$I_{O(OUT)}$ (1)	Output current range	V_{CC} ≥ 4.5 V, V_{IN} ≥ 4.5 V, $V_{I(BAT)} > V_{(LOWV)}$, $V_{IN} – V_{I(BAT)} > V_{(DO–MAX)}$		100		1000	mA
		See note (2)		25		100	
$V_{(SET)}$	Output current set voltage	Voltage on ISET pin, V_{CC} ≥ 4.5 V, V_{IN} ≥ 4.5 V, $V_{I(BAT)} > V_{(LOWV)}$, $V_{IN} – V_{I(BAT)} > V_{(DO–MAX)}$, $V_{O(REG)}$ = 4.2 V	bq24010, bq24012, bq24013, bq24014	2.45	2.50	2.55	V
			bq24018	2.548	2.6	2.652	V
$K_{(SET)}$	Output current ISET factor	50 mA ≤ $I_{O(OUT)}$ ≤ 1000 mA, $V_{(LOWV)} < V_{(OUT)} < V_{(RCH)}$		315	335	355	
		25 mA ≤ $I_{O(OUT)}$ < 50 mA, $V_{(LOWV)} < V_{(OUT)} < V_{(RCH)}$		315	372	430	
		10 mA ≤ $I_{O(OUT)}$ < 100 mA, $V_{(OUT)} < V_{(LOWV)}$		350		1000	
		2.5 mA ≤ $I_{O(OUT)}$ < 10 mA, $V_{(OUT)} < V_{(LOWV)}$			450		
		2.5 mA ≤ $I_{O(OUT)} < I_{(PGM)}$, $V_{(OUT)} < V_{(RCH)}$			355 (3)		
PRE-CHARGE AND SHORT-CIRCUIT CURRENT REGULATION							
$V_{(LOWV)}$	Pre-charge to fast-charge transition threshold	Voltage on BAT pin		2.80	2.95	3.10	V
$V_{(SC)}$	Pre-charge to short-charge transition threshold	Voltage on BAT pin		1	1.4	1.8	V
$I_{O(PRECHG)}$ (4)	Pre-charge range	$V_{(SC)} < V_{I(BAT)} < V_{(LOWV)}$, $t < t_{(PRECHG)}$		10		100	mV
$V_{(PRECHG)}$	Pre-charge set voltage	Voltage on ISET pin, $V_{(SC)} < V_{I(BAT)} < V_{(LOWV)}$		225	250	280	mV
I_{SC}	Short circuit current	$V_{(SC)} > V_{I(BAT)}$		660	900	1200	µA

$$I_{O(OUT)} = \frac{\left(K_{(SET)} \times V_{(SET)}\right)}{R_{(SET)}}$$

(1)

(2) Specified by design. Not production tested.

(3) The ISET pin may be used as a current monitor during voltage regulation by applying the following equation:

$$I_{O(OUT)} = K_{(ISET)} \times \left(\frac{V_{(ISET)}}{R_{(ISET)}} + 10\ \mu A\right)$$

This equation is also used for calculating the termination point.

$$I_{O(PRECHG)} = \frac{\left(K_{(SET)} \times V_{(PRECHG)}\right)}{R_{(SET)}}$$

(4)

ELECTRICAL CHARACTERISTICS (Continued)

over 0°C ≤ T_J ≤ 125°C and recommended supply voltage, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHARGE TAPER AND TERMINATION DETECTION						
$I_{(TAPER)}$ (1)	Charge taper detection range	$V_{I(BAT)} > V_{(RCH)}$, $t < t_{(TAPER)}$	10		100	mA
$V_{(TAPER)}$	Charge taper detection set voltage	Voltage on ISET pin, $V_{I(BAT)} > V_{(RCH)}$, $t < t_{(TAPER)}$, $V_{I(BAT)} = V_{O(REG)}$	225	250	275	mV
$V_{(TERM)}$	Charge termination detection set voltage	Voltage on ISET pin, $V_{I(BAT)} = V_{O(REG)}$, $V_{I(BAT)} > V_{(RCH)}$, $I_{(TERM)} = K_{(SET)} \times V_{(TERM)} / R_{(SET)}$	5	17.5	50	mV
TEMPERATURE COMPARATOR						
$V_{(TS1)}$	Lower threshold	Voltage on TS pin	29	30	31	%VCC
$V_{(TS2)}$	Upper threshold	Voltage on TS pin	60	61	62	
	Hysteresis			1		
BATTERY RECHARGE THRESHOLD						
$V_{(RCH)}$	Recharge threshold		$V_{O(REG)}$ –0.135	$V_{O(REG)}$ –0.1	$V_{O(REG)}$ –0.075	V
STAT1, STAT2, AND $\overline{PG}$ OUTPUTS						
V_{OL}	Output (low) saturation voltage	I_O = 10 mA			0.5	V
CHARGE ENABLE ($\overline{CE}$) AND TIMER AND TERMINATION ENABLE ($\overline{TTE}$) INPUTS						
V_{IL}	Low-level input voltage	I_{IL} = 1 µA	0		0.8	V
V_{IH}	High-level input voltage	I_{IL} = 1 µA	2.0			
TIMERS						
$t_{(PRECHG)}$	Pre-charge time		1 548	2,065	2,581	s
$t_{(TAPER)}$	Taper time		1 548	2,065	2,581	
$t_{(CHG)}$	Charge time		15 480	20,650	25,810	
SLEEP COMPARATOR						
V_{SLP}	Sleep mode entry threshold voltage	$V_{POR} \le V_{(IBAT)} \le V_{O(REG)}$			$V_{CC} \le V_{I(BAT)}$ +30 mV	V
	Sleep mode exit threshold voltage	$V_{POR} \le V_{(IBAT)} \le V_{O(REG)}$	$V_{CC} \ge V_{I(BAT)}$ +22 mV			
	Sleep mode deglitch time	VCC decreasing below threshold, 100-ns fall time, 10-mV overdrive	250		650	ms
BATTERY DETECTION THRESHOLDS						
$I_{(DETECT)}$	Battery detection current	2 V ≤ $V_{(IBAT)}$ ≤ $V_{(RCH)}$	–3.1	–4.6	–6.1	mA
$I_{(DETECT)}$	battery detection time	2 V ≤ $V_{(IBAT)}$ ≤ $V_{(RCH)}$	100	125	150	ms
$I_{(FAULT)}$	Fault current	$V_{(IBAT)} < V_{(RCH)}$ and/or $t > t_{(PRECHG)}$	660	900	1200	µA
POWER-ON RESET AND INPUT VOLTAGE RAMP RATE						
V_{POR} (2)	Power-on reset threshold voltage		225	2.5	2.75	V

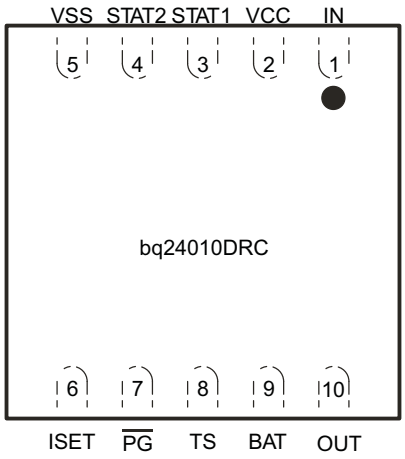
$$I_{O(TAPER)} = \frac{\left(K_{(SET)} \times V_{(TAPER)}\right)}{R_{(SET)}}$$

(1)

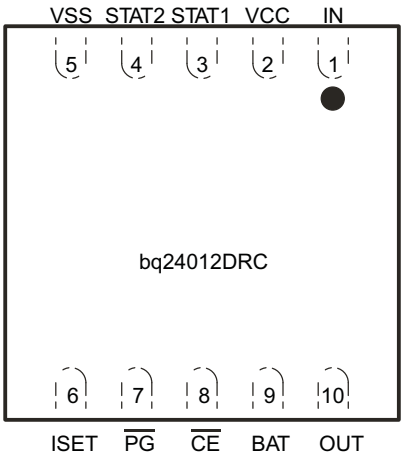
(2) Specified by design. Not production tested.

DEVICE INFORMATION

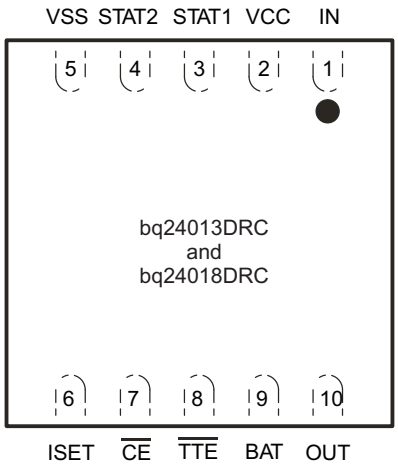
DRC PACKAGE
(TOP VIEW)



DRC PACKAGE
(TOP VIEW)



DRC PACKAGE
(TOP VIEW)



DRC PACKAGE
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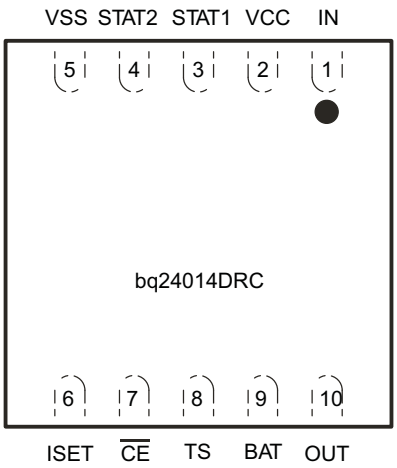
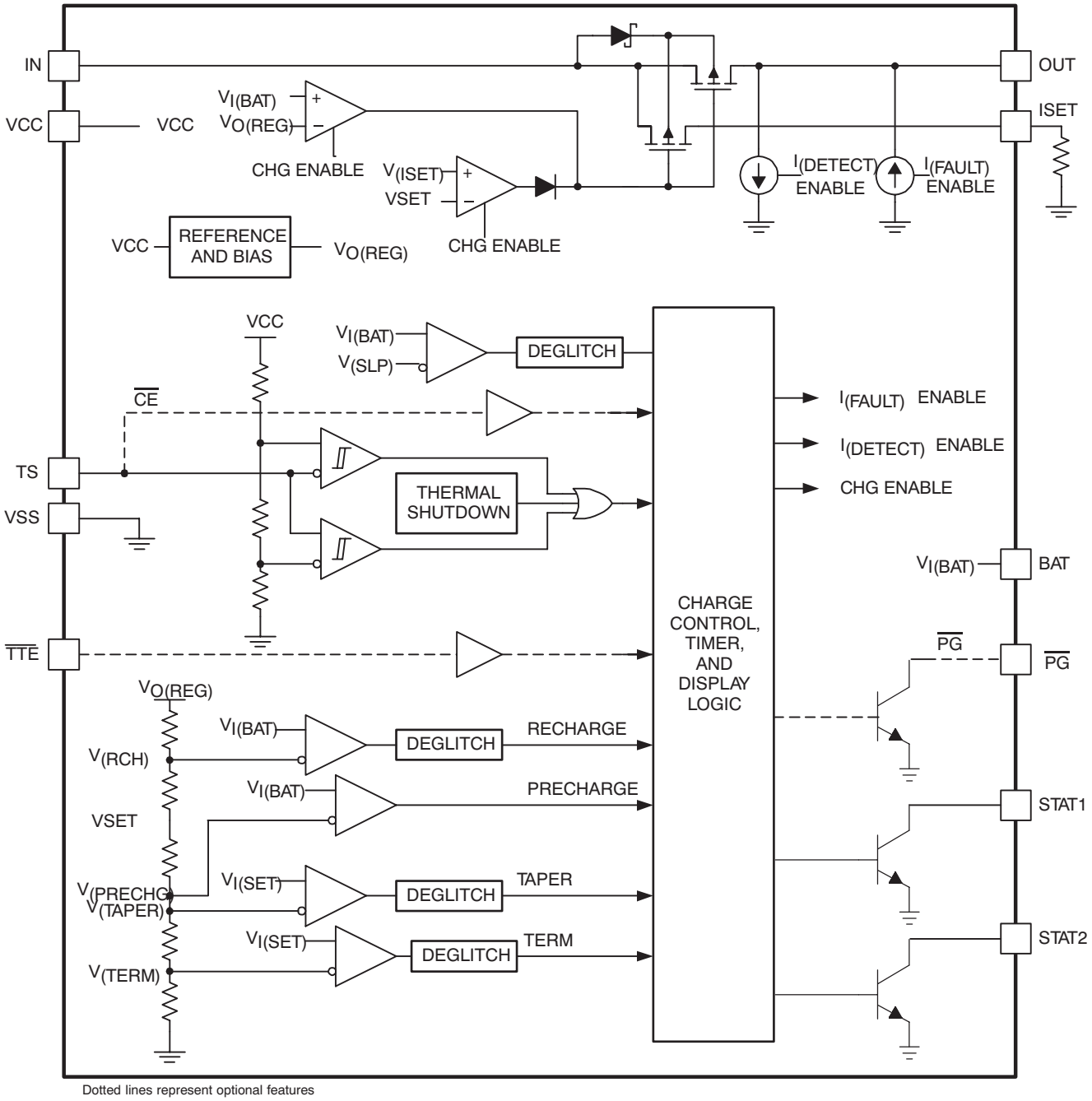


Table 1. TERMINAL FUNCTIONS

TERMINAL					I/O	DESCRIPTION
NAME	bq24010	bq24012	bq24013 and bq24018	bq24014		
BAT	9	9	9	9	I	Battery voltage sense input
$\overline{CE}$	–	8	7	7	I	Charge enable input (active low)
IN	1	1	1	1	I	Charge input voltage. This input must be tied to the VCC pin.
ISET	6	6	6	6	O	Charge current set point
OUT	10	10	10	10	O	Charge current output
$\overline{PG}$	7	7	–	–	O	Power good status output (open collector)
STAT1	3	3	3	3	O	Charge status output 1 (open collector)
STAT2	4	4	4	4	O	Charge status output 2 (open collector)
$\overline{TTE}$	–	–	8	–	I	Timer and termination enable input (active low)
TS	8	–	–	8	I	Temperature sense input
VCC	2	2	2	2	I	VCC supply input
VSS	5	5	5	5	–	Ground input
Exposed Thermal PAD	Pad	Pad	Pad	Pad	–	There is an internal electrical connection between the exposed thermal pad and V_{SS} pin of the device. The exposed thermal pad must be connected to the same potential as the Vss pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

FUNCTIONAL BLOCK DIAGRAM



Dotted lines represent optional features

TYPICAL CHARACTERISTICS

FUNCTIONAL DESCRIPTION

The bqTINY™ supports a precision Li-Ion, Li-Pol charging system suitable for single-cells. Figure 2 shows a typical charge profile, application circuit, and Figure 5 shows an operational flow chart.

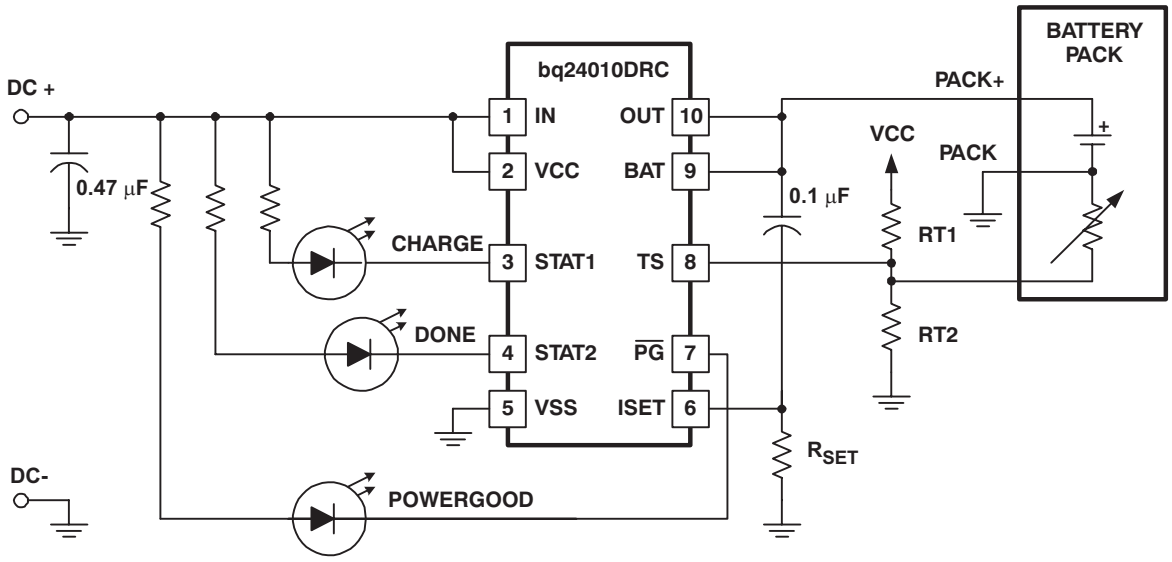


Figure 3. Typical Application Circuit

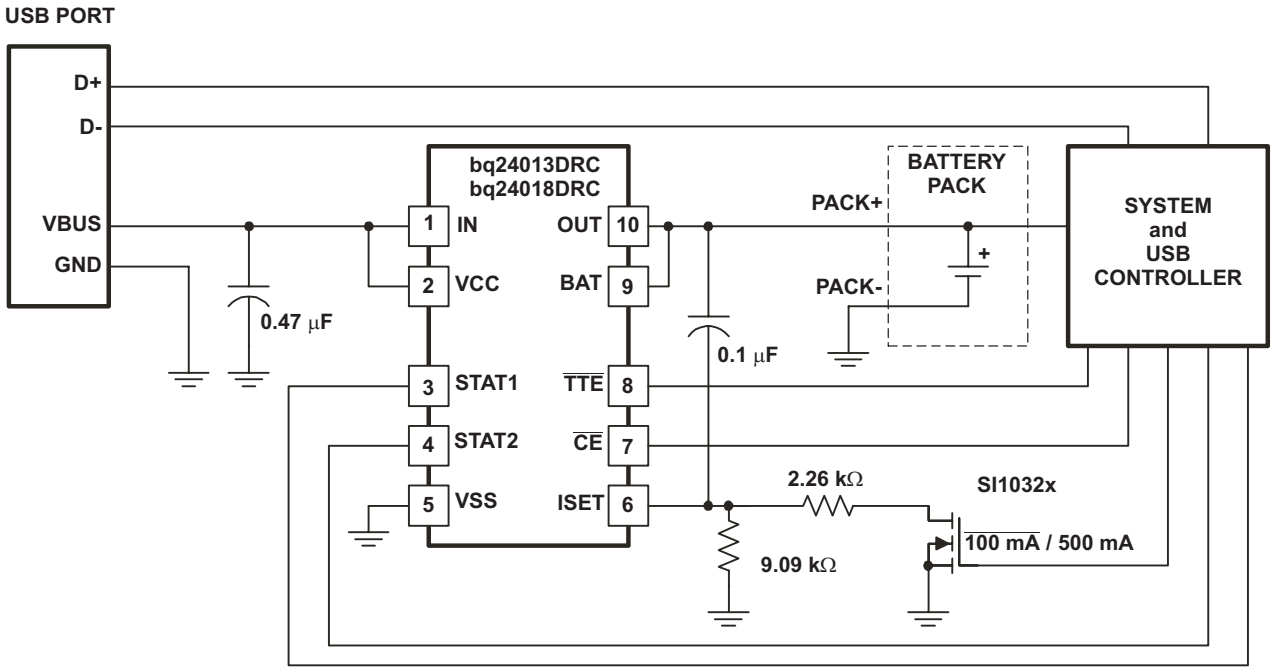


Figure 4. USB Charger Circuit

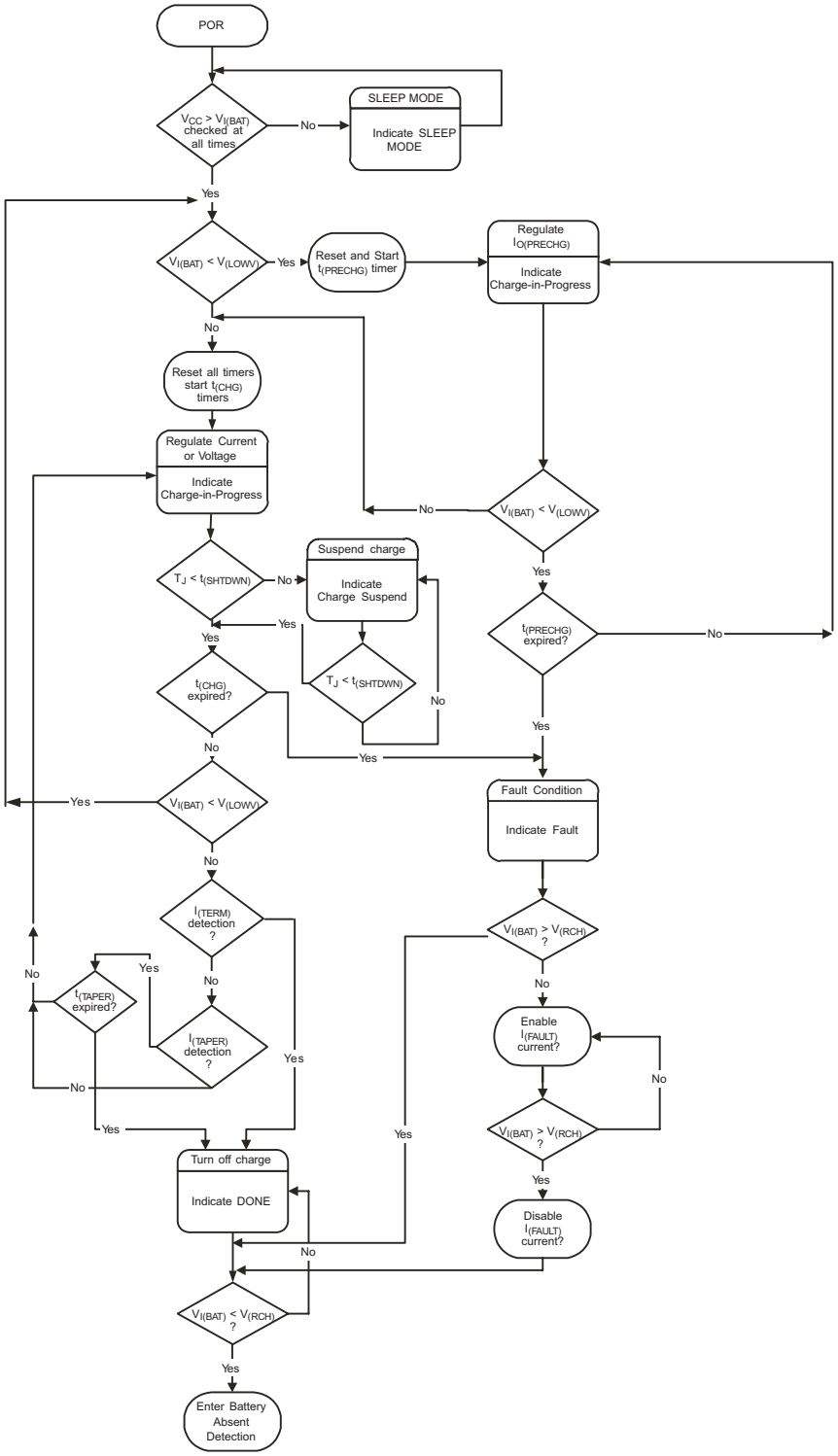


Figure 5. Operational Flow Chart

TEMPERATURE QUALIFICATION

NOTE

The temperature qualifications apply only to versions with temperature sense input (TS) pin option (bq24020 and bq24014).

Versions of the bqTINY with the TS pin option, continuously monitor battery temperature by measuring the voltage between the TS and VSS pins. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develops this voltage (see Figure 3). The bqTINY compare this voltage against the internal $V_{(TS1)}$ and $V_{(TS2)}$ thresholds to determine if charging is allowed (see Figure 6). The temperature sensing circuit is immune to any fluctuation in V_{CC} since both the external voltage divider and the internal thresholds are ratiometric to V_{CC}.

Once a temperature outside the $V_{(TS1)}$ and $V_{(TS2)}$ thresholds is detected the bqTINY immediately suspend the charge. The bqTINY suspends charge by turning off the power FET and holding the timer value (i.e. timers are NOT reset). Charge resumes when the temperature returns to the typical range.

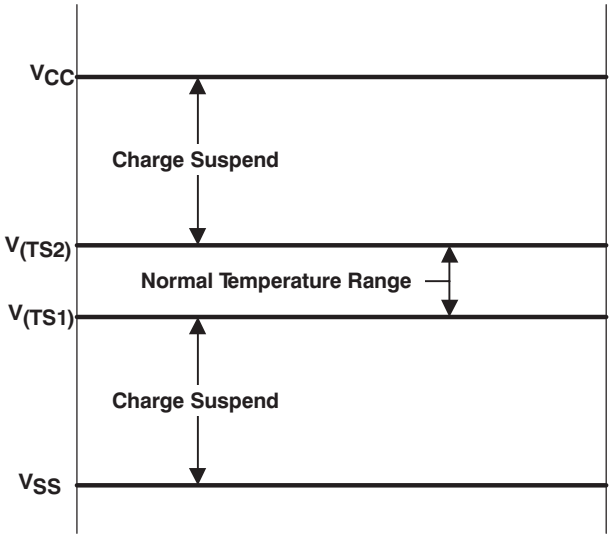


Figure 6. TS Pin Thresholds

The resistor values of R_{T1} and R_{T2} are calculated by Equation 1 and Equation 2 (for NTC Thermistors).

$$R_{T1} = \frac{(5 \times R_{TH} \times R_{TC})}{(3 \times (R_{TC} - R_{TH}))} \quad (1)$$

$$R_{T2} = \frac{(5 \times R_{TH} \times R_{TC})}{(2 \times R_{TC}) - (7 \times R_{TH})} \quad (2)$$

Where R_{TC} is the cold temperature resistance and R_{TH} is the hot temperature resistance of thermistor, as specified by the thermistor manufacturer.

R_{T1} or R_{T2} can be omitted If only one temperature (hot or cold) setting is required. Applying a constant voltage between the V_{TS1} and V_{TS2} thresholds to pin TS disables the temperature-sensing feature.

BATTERY PRE-CONDITIONING

During a charge cycle, if the battery voltage is below the $V_{(LOWV)}$ threshold, the bqTINY applies a pre-charge current, $I_{O(PRECHG)}$, to the battery. This feature revives deeply discharged cells. The resistor connected between the ISET and V_{SS}, R_{SET}, determines the pre-charge rate. The $V_{(PRECHG)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{O(PRECHG)} = \frac{\left(V_{(PRECHG)} \times K_{(SET)}\right)}{R_{(SET)}} \quad (3)$$

The bqTINY activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If $V_{(LOWV)}$ threshold is not reached within the timer period, the bqTINY turns off the charger and enunciates FAULT on the STAT1 and STAT2 pins. Refer to *Timer Fault Recovery* section for additional details.

BATTERY CHARGE CURRENT

The bqTINY offers on-chip current regulation with programmable set point. The resistor connected between the ISET and V_{SS}, R_{SET}, determines the charge rate. The $V_{(SET)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{O(OUT)} = \frac{\left(K_{(SET)} \times V_{(SET)}\right)}{R_{(SET)}} \quad (4)$$

BATTERY VOLTAGE REGULATION

Voltage regulation feedback is accomplished through the BAT pin. This input is tied directly and close to the positive side of the battery pack. The bqTINY monitors the battery-pack voltage between the BAT and VSS pins. When the battery voltage rises to $V_{O(REG)}$ threshold, the voltage regulation phase begins and the charging current begins to taper down.

As a safety backup, the bqTINY also monitors the charge time in the charge mode. If termination does not occur within this time period, $t_{(CHG)}$, the bqTINY turns off the charger and enunciates FAULT on the STAT1 and STAT1 pins. Refer to the *Timer Fault Recovery* section for additional details.

CHARGE TAPER DETECTION, TERMINATION AND RECHARGE

The bqTINY monitors the charging current during the voltage regulation phase. Once the taper threshold, $I_{(TAPER)}$, is detected the bqTINY initiates the taper timer, $t_{(TAPER)}$. Charge terminates after the timer expires. The resistor connected between the ISET and V_{SS}, R_{SET}, determines the taper detection level. The $V_{(TAPER)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{(TAPER)} = \frac{\left(V_{(TAPER)} \times K_{(SET)}\right)}{R_{(SET)}} \quad (5)$$

The bqTINY resets the taper timer in the event that the charge current returns above the taper threshold, $I_{(TAPER)}$.

In addition to the taper current detection, the bqTINY terminates charge in the event that the charge current falls below the $I_{(TERM)}$ threshold. This feature allows for quick recognition of a battery removal condition or insertion of a fully charged battery. Note that taper timer is not used for $I_{(TERM)}$ detection. The resistor connected between the ISET and V_{SS}, R_{SET}, determines the taper detection level. The $V_{(TERM)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{(TERM)} = \frac{\left(V_{(TERM)} \times K_{(SET)}\right)}{R_{(SET)}} \quad (6)$$

After charge termination, the bqTINY restarts the charge once the voltage on the BAT pin falls below the V(RCH) threshold. This feature keeps the battery at full capacity at all times. See the *Battery Absent Detection section* for additional details.

SLEEP MODE

The bqTINY enters the low-power sleep mode if the V_{CC} is removed from the circuit ($\overline{PG}$ pin is high impedance). This feature prevents draining the battery during the absence of V_{CC}. The status pins do not function when in sleep mode or when $V_{CC} < V_{POR}$ and default to the OFF state.

CHARGE STATUS OUTPUTS

The open-collector STAT1 and STAT2 outputs indicate various charger operations as shown in the following table. These status pins can be used to drive LEDs or communicate to the host processor. Note that OFF indicates the open-collector transistor is turned off. When $V_{CC} < V_{POR}$ or $V_{CC} < V_{BAT}$ (Sleep Mode – PG OFF) the STAT pins default to their OFF state. Note that this STAT1 or STAT2 OFF/OFF state is shared by several operating conditions. Decode the actual fault condition by monitoring IN, BAT, $\overline{PG}$, and TS.

Table 2. Status Pins Summary

CHARGE STATE	STAT1	STAT2
Charge-in-progress	ON	OFF
Charge done	OFF(1)	ON
Battery absent Charge suspend (temperature) Timer fault Sleep mode	OFF	OFF

(1) OFF means the open-collector output transistor on the STAT1 or STAT2 pins is in an off state.

$\overline{PG}$ OUTPUT

The open-collector $\overline{PG}$ (power good) indicates when the AC adapter (i.e., V_{CC}) is present. The $\overline{PG}$ bipolar transistor turns ON when a valid V_{CC} is detected. This output is turned off in the sleep mode. The PG pin can be used to drive an LED or communicate to the host processor.

$\overline{CE}$ INPUT (CHARGE ENABLE)

The $\overline{CE}$ digital input is used to disable or enable the charge process. A low-level signal on this pin enables the charge and a high-level signal disables the charge. A high-to-low transition on this pin also resets all timers and fault conditions and starts a new charge cycle.

$\overline{TTE}$ INPUT (TIMER AND TERMINATION ENABLE)

The $\overline{TTE}$ digital input is used to disable or enable the fast-charge timer and charge termination. A low-level signal on this pin enables the fast-charge timer and termination and a high-level signal disables this feature. A high-to-low transition on this pin also resets all timers.

THERMAL SHUTDOWN AND PROTECTION

The bqTINY monitors the junction temperature, T_J, of the die and suspends charging if T_J exceeds 155°C. Charging resumes when T_J falls below approximately 130°C.

BATTERY ABSENT DETECTION

For applications with removable battery packs, bqTINY provides a battery absent detection scheme to reliably detect insertion or removal of battery packs, or both.

The voltage at the BAT pin is held above the battery recharge threshold, $V_{(RCH)}$, by the charged battery following fast charging. When the voltage at the BAT pin falls to the recharge threshold, either by a load on the battery or due to battery removal, the bqTINY begins a battery absent detection test. This test involves enabling a detection current, $I_{(DETECT)}$, for a period of $t_{(DETECT)}$ and checking to see if the battery voltage is below the pre-charge threshold, $V_{(LOWV)}$. Following this, the pre-charge current, $I_{O(PRECHG)}$ is applied for a period of $t_{(DETECT)}$ and the battery voltage checked again to be above the recharge threshold. The purpose is to attempt to close a battery pack with an open protector, if one is connected to the bqTINY. Passing both of the discharge and charging tests indicates a battery absent fault at the STAT pins. Failure of either test starts a new charge cycle. For the absent battery condition the voltage on the BAT pin rises and falls between the $V_{(LOWV)}$ and $V_{O(REG)}$ thresholds indefinitely. See Figure 7.

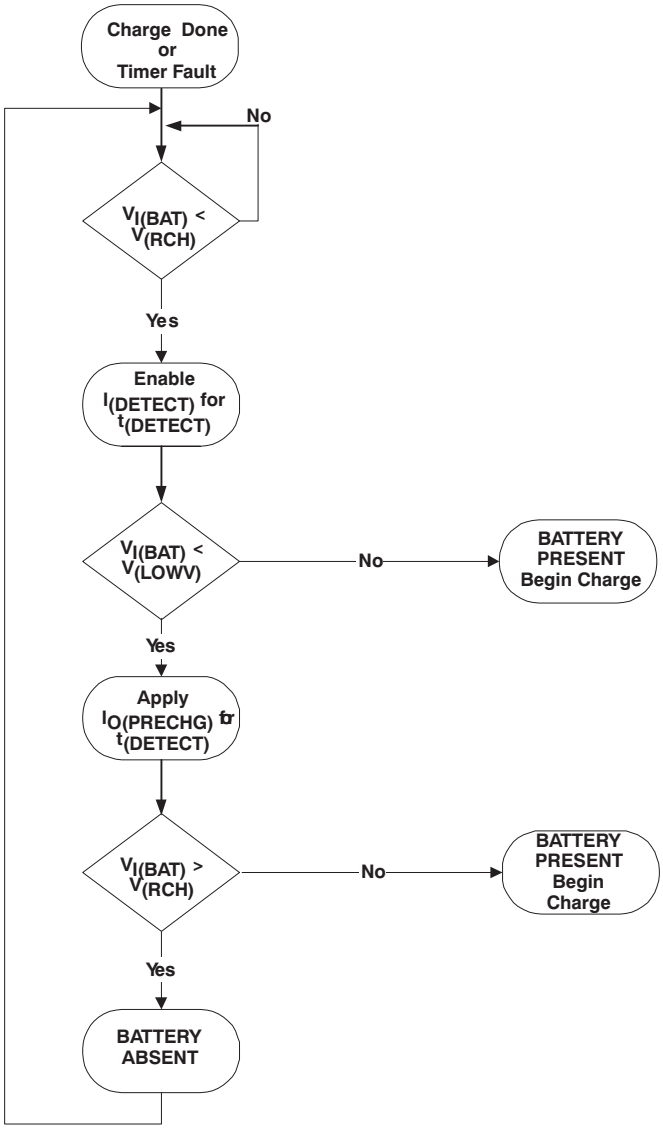


Figure 7. Battery Absent Detection

TIMER FAULT RECOVERY

As shown in Figure 5, bqTINY provides a recovery method to deal with timer fault conditions. The following conditions summarize this method.

Condition 1: Charge voltage above recharge threshold ($V_{(RCH)}$) and timeout fault occurs

Recovery method: bqTINY waits for the battery voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge, or battery removal. Once the battery falls below the recharge threshold, the bqTINY clears the fault and enters the battery absent detection routine. A POR or CE toggle also clears the fault.

Condition 2: Charge voltage below recharge threshold ($V_{(RCH)}$) and timeout fault occurs.

Recovery method: Under this scenario, the bqTINY applies the $I_{(FAULT)}$ current. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, then the bqTINY disables the $I_{(FAULT)}$ current and executes the recovery method described for condition #1. Once the battery falls below the recharge threshold, the bqTINY clears the fault and enters the battery absent detection routine. A POR or CE toggle also clears the fault.

APPLICATION INFORMATION

SELECTING INPUT CAPACITOR

In most applications, all that is needed is a high-frequency decoupling capacitor. A 0.47-µF ceramic, placed in close proximity to V_{CC} and V_{SS} pins, works well. The bqTINY is designed to work with both regulated and unregulated external DC supplies. If a non-regulated supply is chosen, the supply unit should have enough capacitance to hold up the supply voltage to the minimum required input voltage at maximum load. If not, more capacitance has to be added to the input of the charger.

SELECTING OUTPUT CAPACITOR

The bqTINY requires only a small output capacitor for loop stability. A 0.1-µF ceramic capacitor placed between the BAT and ISET pins is typically sufficient for embedded applications (for example non-removable battery packs). For application with removable battery packs a 1-µF ceramic capacitor ensure proper operation of the battery detection circuitry. Note that the output capacitor can also be placed between BAT and VSS pins.

THERMAL CONSIDERATIONS

The bqTINY is packaged in a thermally enhanced MLP (also referred to as QFN) package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled, *QFN/SON PCB Attachment* application note (SLUA271).

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the device junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA} = \frac{T_J \times T_A}{P} \tag{7}$$

Where:

T_J = device junction temperature

T_A = ambient temperature

P = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflown
- Whether other surfaces are in close proximity to the device being tested

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation:

$$P = \left(V_{IN} - V_{I(BAT)}\right) \times I_{O(OUT)} \tag{8}$$

Due to the charge profile of Li-xx batteries, the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. See Figure 2.

PCB LAYOUT CONSIDERATIONS

It is important to pay special attention to the PCB layout. The following list provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from V_{CC} to V_{SS} and the output filter capacitors from BAT to ISET should be placed as close as possible to the bqTINY, with short trace runs to both signal and V_{SS} pins.
- All low-current V_{SS} connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The BAT pin is the voltage feedback to the device and should be connected with its trace as close to the battery pack as possible.
- The high current charge paths into IN and from the OUT pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bqTINY is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note* (SLUA271).
- There is an internal electrical connection between the exposed thermal pad and V_{SS} pin of the device. The exposed thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. V_{SS} pin must be connected to ground at all times.

REVISION HISTORY

Changes from Revision J (December 2008) to Revision K	Page
• Updated $I_{O(OUT)}$ equation	3

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ24010DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AZN
BQ24012DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AZP
BQ24013DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AZQ
BQ24013DRCRG4	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AZQ
BQ24014DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AZR
BQ24014DRCRG4	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AZR
BQ24018DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BZH
BQ24018DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BZH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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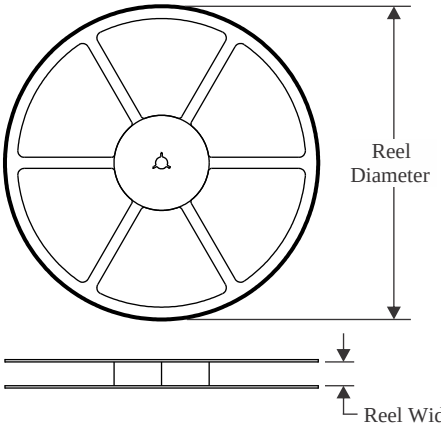
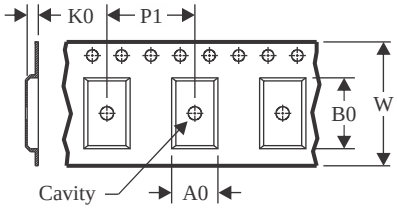
TAPE AND REEL INFORMATION

REEL DIMENSIONS

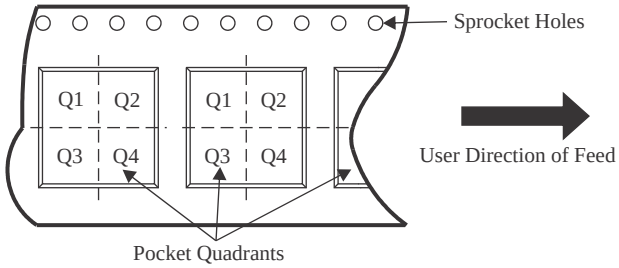


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

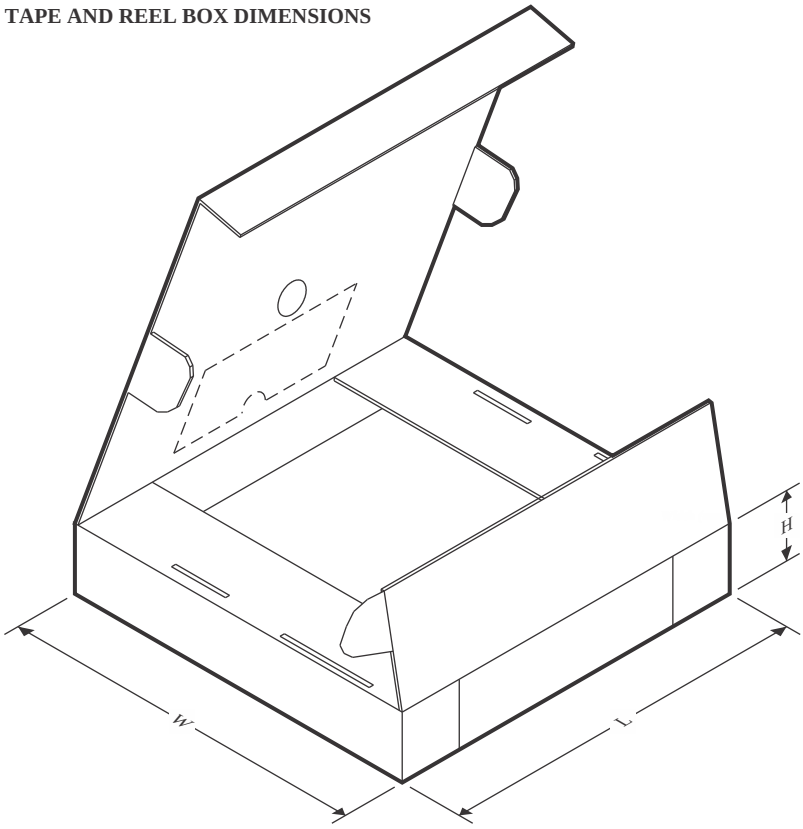
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24010DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24010DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24012DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24012DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24013DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24013DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24014DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24014DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24018DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24018DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24010DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
BQ24010DRCR	VSON	DRC	10	3000	338.0	355.0	50.0
BQ24012DRCR	VSON	DRC	10	3000	338.0	355.0	50.0
BQ24012DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
BQ24013DRCR	VSON	DRC	10	3000	338.0	355.0	50.0
BQ24013DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
BQ24014DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
BQ24014DRCR	VSON	DRC	10	3000	338.0	355.0	50.0
BQ24018DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
BQ24018DRCT	VSON	DRC	10	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

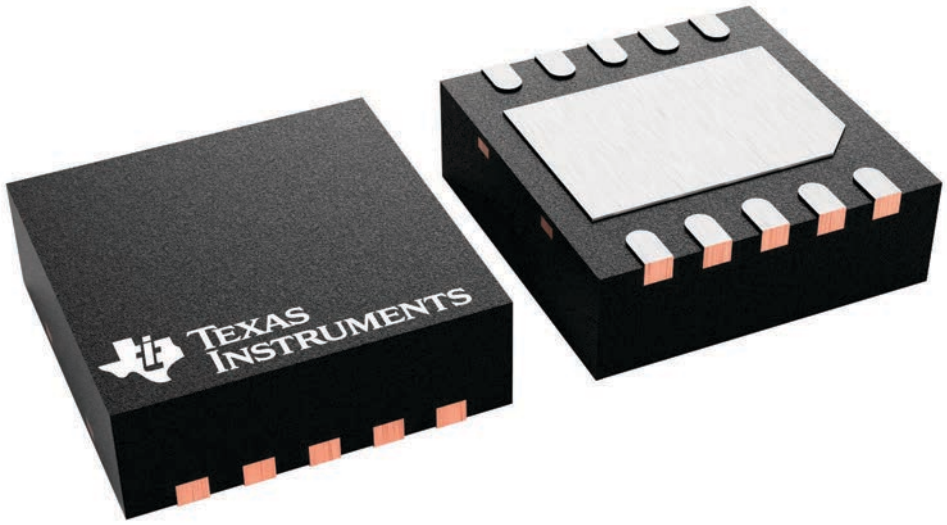
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



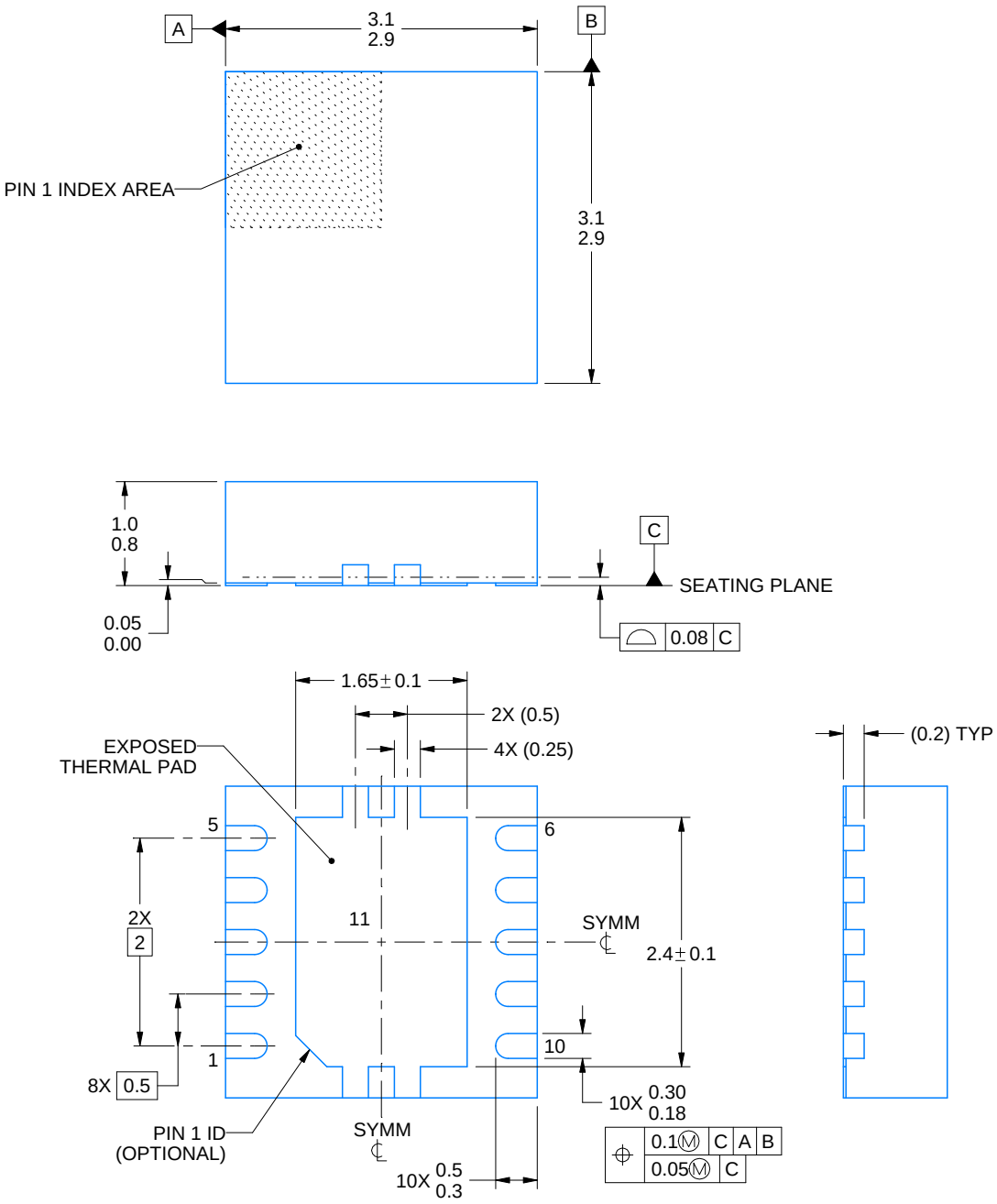
4226193/A

PACKAGE OUTLINE

DRC0010J

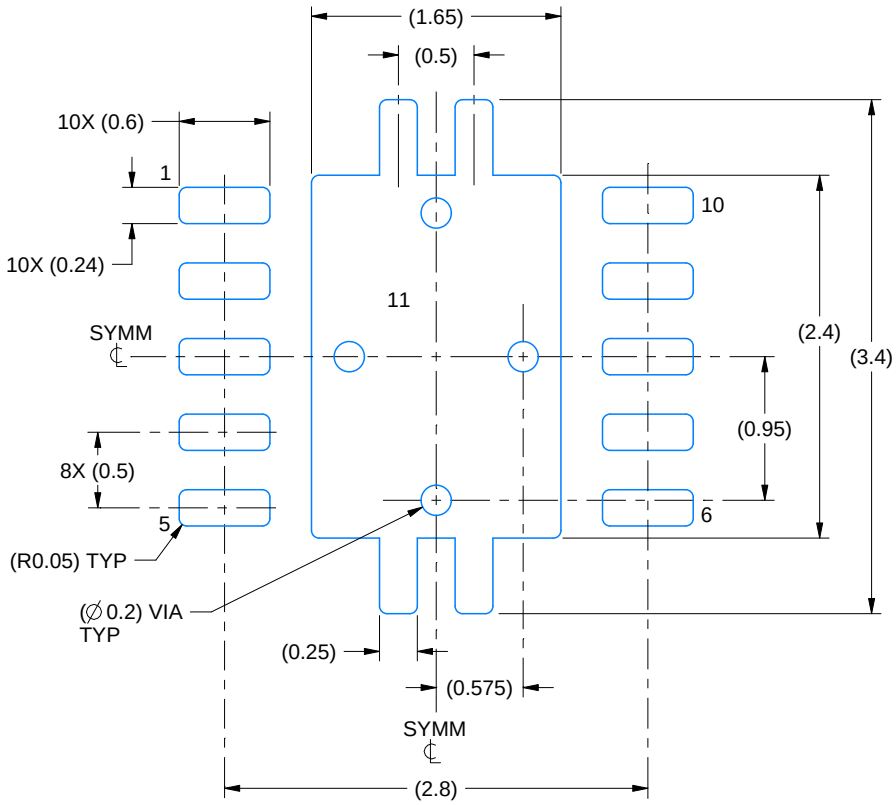
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

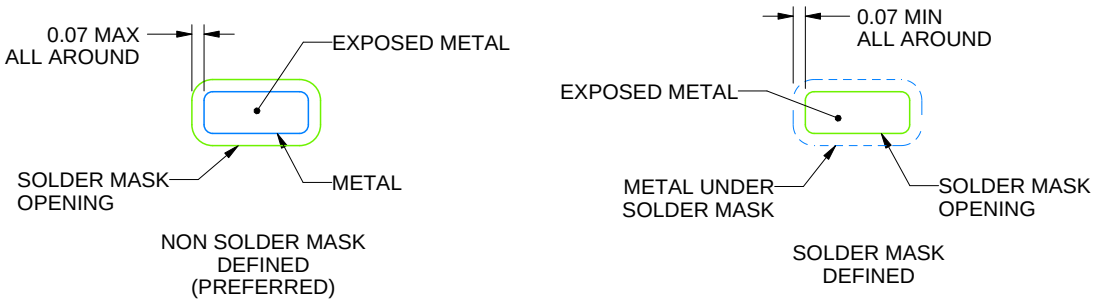


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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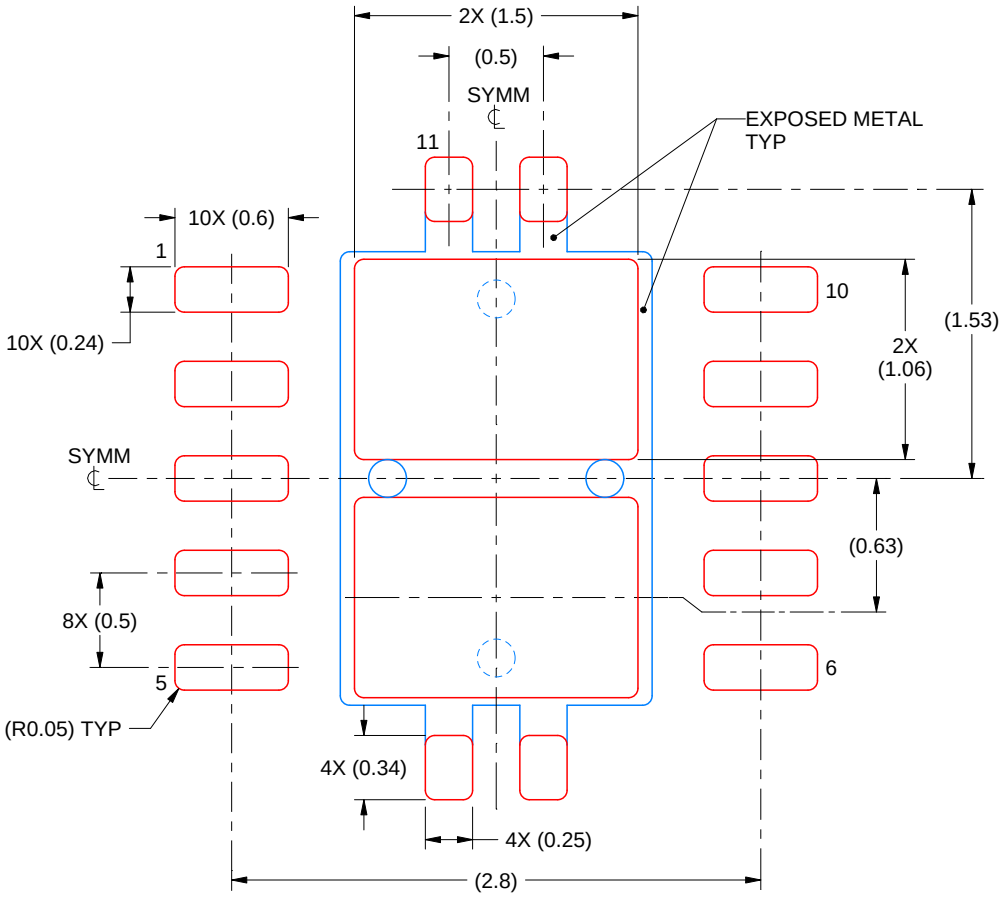
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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