UCC28056 6-Pin Single-Phase Transition-Mode PFC Controller

1 Features

- Transition Mode PFC
  - Good Efficiency
  - Low EMI at High Output Power
- Unified Algorithm for Working in CrM and DCM (with high power factor across the entire operating range)
- Fast, Enhanced Dynamic Response
- 1.0-A and 0.7-A Drive Capability
- User Adjustable Valley Switching
- Industry Best Audibility Performance Over Entire Load Range
- Industry Best Light-Load Efficiency with Advanced Frequency Shaping in DCM and CrM
- Small Footprint 6-pin SOT-23(6) Package
- No ZCD Winding for Valley Detection
- Helps Enable Compliance to IEC61000-3-2
- Create a Custom Design Using the UCC28056 With the WEBENCH® Power Designer

2 Applications

- Desktop Computing
- Digital TV SMPS
- Gaming
- Set Top Box
- AC Adapter Front End
- Electronic Lamp Ballast
- Entry-Level Server and Web Server

3 Description

UCC28056 is a fully featured PFC controller offering excellent light load efficiency and standby power. UCC28056 simplifies the design of power supply system's requiring good power factor, that must also be capable of meeting today's tough standards for efficiency and standby power. At full load, UCC28056 operates the PFC power stage at maximum switching frequency in Transition Mode. At reduced load, the part transitions seamlessly into Discontinuous Conduction mode, automatically reducing switching frequency for maximum efficiency. At light load, DCM operation is combined with Burst Mode operation to further improve light load efficiency and standby power. UCC28056 integrates all the features necessary to implement a high performance and robust PFC stage into a 6-pin package and requires a minimal number of external components to interface with the power stage.

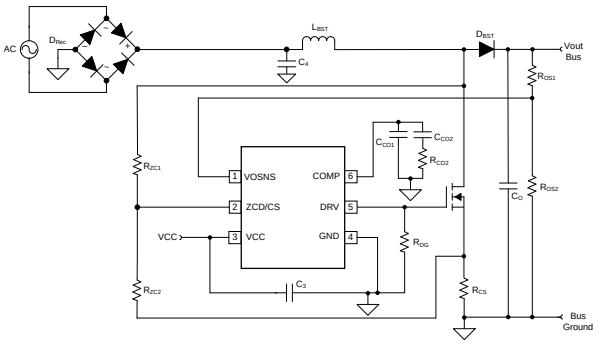
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC28056	SOT-23(6)	2.90 mm x 1.6 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

ADVANCE INFORMATION

Simplified Schematic



Standby Power

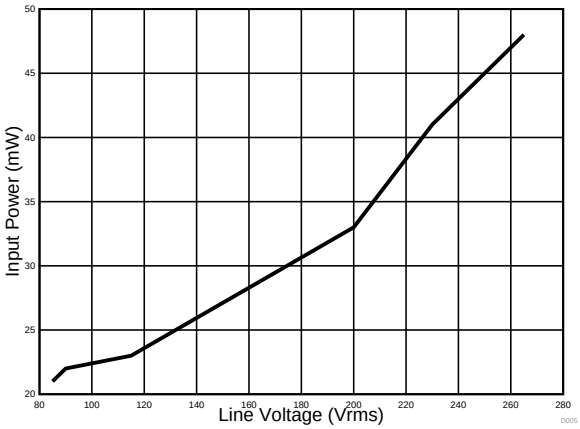


Table of Contents

ADVANCE INFORMATION

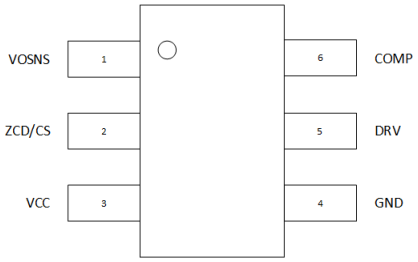
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2017) to Revision A	Page
• Added WEBENCH links to data sheet	1

5 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP	6	I/O	Output of the internal transconductance error amplifier and power demand input. Compensation of the voltage loop is achieved by connecting a suitable RC network from this pin to GND. The error amplifier output is internally limited to V_{COClmp} . An internal resistor, $R_{CODisch}$, discharges the external compensation network when the controller is in its Stopb state. Switching stops, and the controller enters a low power state (BstOffb), when the voltage on the COMP pin drops below $V_{BSTFall}$. Switching resumes when the COMP pin voltage exceeds $V_{BSTRise}$.
DRV	5	I/O	GATE connection to drive the main power MOSFET. This output is internally limited to V_{DRHigh} . This is done to reduce power dissipation in the internal driver and allow device operation from high VCC voltages. An external resistor connected from DRV to GND adjusts the delay between the Drain waveform falling below VIN and the DRV rising edge, allowing the turn on transition to be aligned to the valley minimum accurately over a wide range of idle ring oscillating frequency.
GND	4	G	Controller Ground reference pin. Connect to the power stage at the lower terminal of the current sense resistor, R_{CS}, only.
VCC	3	P	Positive supply voltage. Switching operation can start once VCC exceeds $V_{CCStart}$. Switching operate will cease if VCC drops below V_{CCStop} for longer than $T_{UVLOBlank}$.
VOSNS	1	I	Voltage error amplifier inverting input. The error amplifier non - inverting input connects to internal reference voltage V_{OSReg} . Error amplifier gain increases with error magnitude to improve transient response without compromising Line current distortion. Output over-voltage protection is implemented on this pin. Switching operation halts if the voltage on this pin exceeds $V_{Ovp1Rise}$ and resumes when it drops below $V_{Ovp1Fall}$
ZCD/CS	2	I	This pin is fed by a potential divider connected across the Drain & Source pins of the power MOSFET switch. While the DRV pin is high this pin monitors the voltage across the current sense resistor, R_{CS} . It is used to implement over-current protection functions. While the DRV pin in low this pin monitors the Drain voltage waveform. Input voltage applied to the power stage can be obtained by filtering the Drain waveform. Input voltage is used to provide Line voltage feed - forward and Line Brown - Out protection features. Drain voltage waveform is also used to provide ZCD detection, valley synchronization and second level output over - voltage protection features

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VCC	-0.5	36	V
	ZCD/CS	-0.5	7	
	VOSNS	-0.5	7	
Output voltage	COMP	-0.5	7	V
	DRV	-0.3	20	
Junction temperature range	T_J	-40	150	°C
Storage temperature range, T_{stg}	T_{stg}	-65	150	
Lead temperature	Soldering, 10 second		300	
	Reflow		260	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VCC	Input voltage		12		V
T_A	Operating ambient temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC28056 SOT23-6 6 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	116.4	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	74.9	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	36.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	36.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

ADVANCE INFORMATION

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{CCStart}$	Turn-on threshold	VCC Rising		10.65	11	V
V_{CCStop}	Turn-off threshold	VCC Falling	8.5	8.85	9.2	V
V_{CCHyst}	UVLO Hysteresis ($V_{CCStart}$ - V_{CCStop}) (1)		1.5			V
$T_{UVLOBlk}$	Turn-OFF Blanking Time		27	35	39	µs
SUPPLY CURRENT						
$I_{CC\_Startup}$	Current consumption before startup	VCC = $V_{CCStart}$-200mV, T_A < 110℃			46	µA
I_{CC_FAULT}	Current consumption during fault condition	VCC = 12V			125	µA
I_{CC_BSTOFF}	Current consumption during Burst OFF period	VCC = 12V			125	µA
I_{CC_RUN}	Operating current with DRV pin unloaded	VCC = 12V		1.8	2.2	mA
GATE DRIVE						
V_{DRLow}	DRV output low voltage	I_{DR} = 100mA			0.9	V
V_{DRHigh}	DRV output voltage high level, limited	VCC = 25V, I_{DR} = -10mA	10	13.7	15	V
$V_{DRHighMin}$	DRV minimum high voltage level	VCC = V_{CCStop} + 200 mV, I_{DR} = -8mA	8			V
R_{DRH}	DRV, Pull-up resistance	T_A = -40°C to 125°C, I_{DR} = -8mA, VCC=12V		9.7	15	Ω
R_{DRL}	DRV, Pull-down resistance	T_A = -40°C to 125°C, I_{DR} = 100mA	2.0	4.6	9	Ω
t_R	Rise Time	CLOAD=1nF, DRV=1V to 6V, VCC=12V	14	34	61	ns
t_F	Fall Time	CLOAD=1nF, DRV=6V to 1V, VCC=12V	9	19	40	ns
Isource	Source peak current on DRV Pin (1)			-0.7		A
Isink	Sink peak current on DRV Pin (1)			1		A
R_{DG0}	DRV to GND resistance value to select T_{ZCDR0} (1)		130	200		kΩ
R_{DG1}	DRV to GND resistance value to select T_{ZCDR1} (1)		81.18	82	91.02	kΩ
R_{DG2}	DRV to GND resistance value to select T_{ZCDR2} (1)		61.38	62	68.82	kΩ
R_{DG3}	DRV to GND resistance value to select T_{ZCDR3} (1)		42.57	43	47.73	kΩ
R_{DG4}	DRV to GND resistance value to select T_{ZCDR4} (1)		26.73	27	29.97	kΩ
R_{DG5}	DRV to GND resistance value to select T_{ZCDR5} (1)		17.82	18	19.98	kΩ
R_{DG6}	DRV to GND resistance value to select T_{ZCDR6} (1)		12.87	13	14.43	kΩ
R_{DG7}	DRV to GND resistance value to select T_{ZCDR7} (1)		9	9.1	10.101	kΩ
T_{DGSmpl}	Time needed to detect R_{DG} value.	T_A < 85℃	4.05	4.5	4.95	ms
V_{DGClmp}	Maximum voltage that will be applied on DRV pin while detecting R_{DG} value.		1	1.05	1.1	V

(1) Not production tested. Specified by design.

ADVANCE INFORMATION

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
V_{OSReg}	Feedback voltage reference		2.45	2.5	2.55	V
I_{OSBias}	ISNS pin bias current	$V_{OS} = V_{OSReg}$	-100		100	nA
g_M	Error Amplifier Transconductance Gain	$\lvert V_{OS}-V_{OSReg}\rvert$ < DSuThs		50		µS
g_{MNL}	Error Amplifier Transconductance Gain for large error	$\lvert V_{OS}-V_{OSReg}\rvert$ > DSuThs		300		µS
DSuThs	Non-Linear Gain Threshold		67			mV
$R_{CODisch}$	Internal COMP to GND resistance when in STOPb state.		4.3	5	5.7	kΩ
V_{COClmp}	COMP pin internal high clamp voltage		5.5	5.6	5.71	V
V_{COSat}	COMP pin internal low clamp voltage	(1)		0		V
I_{COMin}	COMP Maximum Source Current			-120		µA
I_{COMax}	COMP Maximum Sink Current			120		µA

ADVANCE INFORMATION

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LINE VOLTAGE FEED-FORWARD						
$T_{HLinMax}$	Line peak sampling window (1)	While switching	11	12.3	13.6	ms
$V_{FF0Rise}$	Comparator rising threshold switching from G_{FF0} to G_{FF1} (1)			0.348		V
$V_{FF1Rise}$	Comparator rising threshold switching from G_{FF1} to G_{FF2} (1)			0.406		V
$V_{FF2Rise}$	Comparator rising threshold switching from G_{FF2} to G_{FF3} (1)			0.473		V
$V_{FF3Rise}$	Comparator rising threshold switching from G_{FF3} to G_{FF4} (1)			0.552		V
$V_{FF4Rise}$	Comparator rising threshold switching from G_{FF4} to G_{FF5} (1)			0.644		V
$V_{FF5Rise}$	Comparator rising threshold switching from G_{FF5} to G_{FF6} (1)			0.751		V
$V_{FF6Rise}$	Comparator rising threshold switching from G_{FF6} to G_{FF7} (1)			0.875		V
$V_{FF0Fall}$	Comparator falling threshold switching from G_{FF1} to G_{FF0} (1)	Peak value of $V_{InSynth}$ within $T_{HLinMax}$ Window		0.331		V
$V_{FF1Fall}$	Comparator falling threshold switching from G_{FF2} to G_{FF1} (1)	Peak value of $V_{InSynth}$ within $T_{HLinMax}$ Window		0.386		V
$V_{FF2Fall}$	Comparator falling threshold switching from G_{FF3} to G_{FF2} (1)	Peak value of $V_{InSynth}$ within $T_{HLinMax}$ Window		0.45		V
$V_{FF3Fall}$	Comparator falling threshold switching from G_{FF4} to G_{FF3} (1)	Peak value of $V_{InSynth}$ within $T_{HLinMax}$ Window		0.524		V
$V_{FF4Fall}$	Comparator falling threshold switching from G_{FF5} to G_{FF4} (1)	Peak value of $V_{InSynth}$ within $T_{HLinMax}$ Window		0.612		V
$V_{FF5Fall}$	Comparator falling threshold switching from G_{FF6} to G_{FF5} (1)	Peak value of $V_{InSynth}$ within $T_{HLinMax}$ Window		0.713		V
$V_{FF6Fall}$	Comparator falling threshold switching from G_{FF7} to G_{FF6} (1)	Peak value of $V_{InSynth}$ within $T_{HLinMax}$ Window		0.832		V
G_{FF0}	Line Feed-Forward gain level 0 (1)			1		V
G_{FF1}	Line Feed-Forward gain level 1 (1)			0.735		V
G_{FF2}	Line Feed-Forward gain level 2 (1)			0.541		V
G_{FF3}	Line Feed-Forward gain level 3 (1)			0.398		V
G_{FF4}	Line Feed-Forward gain level 4 (1)			0.292		V
G_{FF5}	Line Feed-Forward gain level 5 (1)			0.215		V
G_{FF6}	Line Feed-Forward gain level 6 (1)			0.158		V
G_{FF7}	Line Feed-Forward gain level 7 (1)			0.116		V

ADVANCE INFORMATION

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MAXIMUM ON TIME						
T_{ONMAX0}	Maximum ON time when $G_{FF} = G_{FF0}$	OTP_TONMAX = 0b	12.25	12.8	13.2	µs
T_{ONMAX1}	Maximum ON time when $G_{FF} = G_{FF1}$	OTP_TONMAX = 0b	10.42	10.98	11.28	µs
T_{ONMAX2}	Maximum ON time when $G_{FF} = G_{FF2}$	OTP_TONMAX = 0b	8.85	9.41	9.64	µs
T_{ONMAX3}	Maximum ON time when $G_{FF} = G_{FF3}$	OTP_TONMAX = 0b	7.59	8.07	8.32	µs
T_{ONMAX4}	Maximum ON time when $G_{FF} = G_{FF4}$	OTP_TONMAX = 0b	6.52	6.92	7.18	µs
T_{ONMAX5}	Maximum ON time when $G_{FF} = G_{FF5}$	OTP_TONMAX = 0b	5.56	5.93	6.16	µs
T_{ONMAX6}	Maximum ON time when $G_{FF} = G_{FF6}$	OTP_TONMAX = 0b	4.73	5.09	5.28	µs
T_{ONMAX7}	Maximum ON time when $G_{FF} = G_{FF7}$	OTP_TONMAX = 0b	4.07	4.36	4.57	µs
BURST MODE OPERATION						
$V_{BSTFall}$	VCOMP Burst Threshold Falling	OTP_BST_F=00b		0.5		V
$V_{BSTRise}$	VCOMP Burst Threshold Rising	OTP_BST_R=00b		0.625		V
ZERO CURRENT DETECTION AND VALLEY SYNCH						
$V_{ZcdVinHyst}$	ZcdVin Comparator hysteresis (1)		12	19	26	mV
$T_{DCHVinMin}$	ZcdVin Comparator blanking from DRV falling edge (1)		250	358	467	ns
T_{ZCDTo}	If no negative transitions on Vin comparator for this period then do not wait for valleys		2.1	2.5	3.0	µs
T_{ZCDR0}	Minimum ZCD to DRV delay.	From $V_{ZC} < V_{InSynth}$ to DRV = 7V, C_{DR} = 1nF, Fres = 1.2MHz, $R_{DG} = R_{DG0}$		170	230	ns
ΔT_{ZCDR1}	$T_{ZCDR1} = T_{ZCDR0} + \Delta T_{ZCDR1}$	$R_{DG} = R_{DG1}$	40	45.5	52.5	ns
ΔT_{ZCDR2}	$T_{ZCDR2} = T_{ZCDR0} + \Delta T_{ZCDR2}$	$R_{DG} = R_{DG2}$	81	90	97	ns
ΔT_{ZCDR3}	$T_{ZCDR3} = T_{ZCDR0} + \Delta T_{ZCDR3}$	$R_{DG} = R_{DG3}$	119	130	140	ns
ΔT_{ZCDR4}	$T_{ZCDR4} = T_{ZCDR0} + \Delta T_{ZCDR4}$	$R_{DG} = R_{DG4}$	148	165	182	ns
ΔT_{ZCDR5}	$T_{ZCDR5} = T_{ZCDR0} + \Delta T_{ZCDR5}$	$R_{DG} = R_{DG5}$	220	245	270	ns
ΔT_{ZCDR6}	$T_{ZCDR6} = T_{ZCDR0} + \Delta T_{ZCDR6}$	$R_{DG} = R_{DG6}$	292	325	358	ns
ΔT_{ZCDR7}	$T_{ZCDR7} = T_{ZCDR0} + \Delta T_{ZCDR7}$	$R_{DG} = R_{DG7}$	364	405	446	ns
V_{DDAmpl}	Amplitude of 500 kHz sinewave signal on ZCD/CS pin needed to trigger knee detector		25			mV
$T_{DCHDDMin}$	Knee point detector blanking period (1)	Measured from falling edge of DRV pulse		1.5		µs
FAULT PROTECTION						
$T_{LongFlt}$	Long Fault Duration (1)			1		s
LINE BROWN-OUT PROTECTION						
$V_{ZCBoRise}$	Brown-out Protection Threshold when in Stopb state	Peak cycle average voltage on ZCD/CS Pin. OTPBoExb = 0b	0.282	0.3	0.318	V
$V_{ZCBoFall}$	Brown-out Protection Threshold when switching	Peak cycle average voltage on ZCD/CS Pin. OTPBoExb = 0b	0.249	0.265	0.28	V
$V_{ZCBoHyst}$	$V_{ZCBoRise} - V_{ZCBoFall}$ (1)	OTPBoExb = 0b	0.031			V
I_{ZCBias}	ZCD/CS Pin Bias Current (1)	$V_{ZC} = V_{ZCBoFall}$	-100		100	nA
$T_{BoBlank}$	Brown-out Filter Duration (1)		90	100	110	ms

ADVANCE INFORMATION

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVER-CURRENT PROTECTION						
V_{ZCOcp1}	ZCD/CS First Level over-current protection threshold		450	500	550	mV
V_{ZCOcp2}	ZCD/CS Second Level over-current protection threshold		670	750	825	mV
$T_{Ocp1Blk}$	ZCD/CS blanking time from DRV rising edge to Enable Ocp1 Comparator Output (1)			450		ns
$T_{Ocp2Blk}$	ZCD/CS blanking time from DRV rising edge to Enable Ocp2 Comparator Output (1)			250		ns
$T_{OcpDrvDel}$	ZCD/CS crossing V_{OcpxTh} to DRV falling edge.			64	120	ns
$T_{DCHMax0}$	Max duration of T_{DCHb} state if no ZCD signal detected. After no OCPx Events (1)			250		µS
$T_{DCHMax1}$	Max duration of T_{DCHb} state if no ZCD signal detected. After one OCPx Events (1)			500		µS
$T_{DCHMax2}$	Max duration of T_{DCHb} state if no ZCD signal detected. After two consecutive OCPx Events (1)			1000		µS
OUTPUT OVER-VOLTAGE PROTECTION						
$V_{OSOovp1Rise}$	VOSNS over-voltage threshold, rising	VCC=12V	2.69	2.75	2.81	V
$V_{OSOovp1Fall}$	VOSNS over-voltage threshold, falling	VCC=12V	2.60	2.675	2.73	V
$V_{OSOovp1Hyst}$	$V_{OSOovp1Rise}$ - $V_{OSOovp1Fall}$ (1)		0.072			V
V_{Ovp2Th}	Second level output over-voltage fault Threshold		1.102	1.125	1.148	V
THERMAL PROTECTION						
$T_{TSDRise}$	Thermal Shutdown Rising Threshold	While switching	135	145	155	°C
$T_{TSDFall}$	Thermal Shutdown Falling Threshold	While not switching	95	105	115	°C
$T_{TSDHyst}$	$T_{TSDRise}$ - $T_{TSDFall}$		38	40	42	°C

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

UCC28056 is designed to partner with UCC25630x to control a complete PFC+LLC isolated off-Line power supply system delivering more than 300W. The combined power supply is designed to meet tough modern efficiency and standby power requirements without the need for an Auxiliary Flyback converter and with no need to switch off the PFC under light load conditions. It allows designers to meet modern green power standards with a simpler and cheaper power supply.

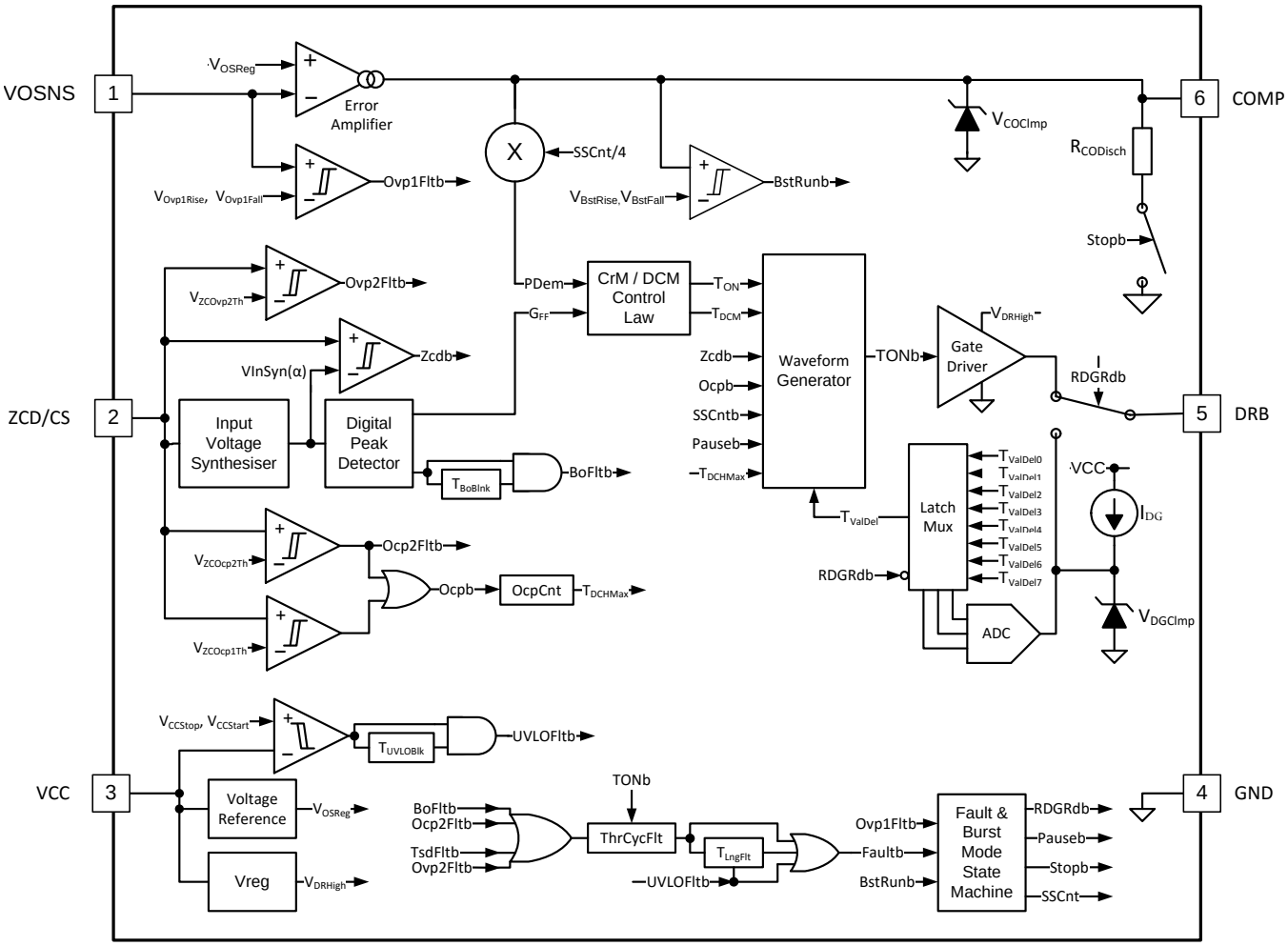
UCC28056 contains a number of features designed to maximize operating efficiency across the entire range of Line and Load. A versatile CrM/DCM control algorithm allows UCC28056 to operate in transition mode at full power and then transition seamlessly into DCM at reduced load without compromising Line current harmonics or power factor. It will operate at maximum frequency (Transition mode) when delivering full load and then automatically reduce switching frequency, moving to DCM operation, when delivering reduced load for maximum efficiency.

Light load efficiency and standby power are further enhanced by transitioning automatically to a burst mode of operation when delivering less than 10% load. During the burst OFF periods, UCC28056 powers down most of its internal circuits to minimize controller power consumption.

UCC28056 includes a comprehensive list of fault protection features. These include cycle-by-cycle current limit, over-current protection, dual independent output over-voltage protection, Line Brown-out, Over-temperature protection and supply under-voltage lockout (UVLO).

Quantised 7-level line voltage feed-forward ensures that the loop gain is almost independent of line voltage, to ease design of the output voltage control loop. A non-linear error amplifier greatly improves the response to large steps in load without compromising steady state Line current harmonics.

7.2 Functional Block Diagram



ADVANCE INFORMATION

7.3 Feature Description

7.3.1 CrM/DCM Control Principle

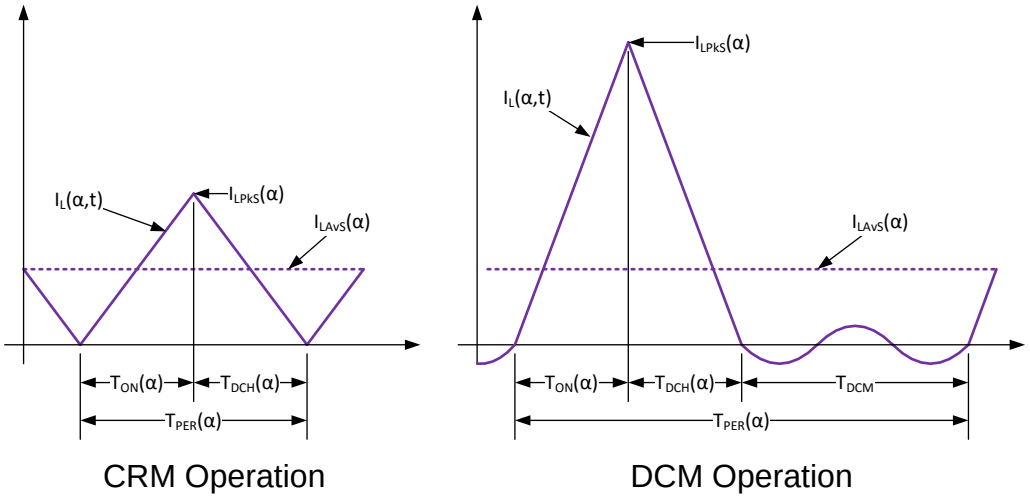


Figure 1. PFC Inductor Current Waveform for CrM and DCM Operation

Consider a single switching cycle that occurs at angle (α) during the Line Cycle. Assuming ideal CrM operation the average inductor current ($I_{LAvS(\alpha)}$) that flows during the switching cycle is given by:

$$I_{LAvS}(\alpha) = \frac{I_{LPkS}(\alpha)}{2} = V_L(\alpha) \cdot \frac{T_{ON}(\alpha)}{2 \cdot L_{PFC}} = \frac{V_L(\alpha)}{R_{InEq}} \quad (1)$$

A fixed circuit has constant inductance (LP_{FC}) so if the switch ON duration $T_{ON}(\alpha)$ is held constant (T_{ON}) , across the Line Cycle, then average input current is proportional to input voltage. In other words, when controlled in this way the Boost converter behaves like a resistive load (R_{InEq}) connected across the Line.

$$R_{InEq} = \frac{2 \cdot L_{PFC}}{T_{ON}} \quad (2)$$

Now consider DCM operation. In this case the average inductor current that flows during the switching cycle is given by:

$$I_{LAvS}(\alpha) = \frac{I_{LPkS}(\alpha)}{2} \cdot \frac{T_{ON}(\alpha) + T_{DCH}(\alpha)}{T_{PER}(\alpha)} = V_L(\alpha) \cdot \frac{T_{ON}(\alpha) \cdot \delta_{ONDCH}(\alpha)}{2 \cdot L_{PFC}} = \frac{V_L(\alpha)}{R_{InEq}} \quad (3)$$

Now to ensure average input current proportional to input voltage it is necessary to ensure that the product $T_{ON}(\alpha) * \delta_{ONDCH}(\alpha)$ is kept constant across the Line Cycle. In this case the equivalent input resistance is given by:

$$R_{InEq} = \frac{2 \cdot L_{PFC}}{T_{ON} \cdot \delta_{ONDCH}} \quad (4)$$

The minimum effective input resistance ($R_{InEqMin}$)is needed to draw maximum power (P_{NOM})from minimum Line voltage ($V_{LMinPkL}$):

$$P_{NOM} = \frac{V_{LMInPkL}^2}{2 \cdot R_{InEqMin}} \quad (5)$$

ADVANCE INFORMATION

Feature Description (continued)

Assume that full power operation at minimum Line operation will be in CrM mode. In this case, the PFC inductor value required to deliver maximum power from minimum Line can be calculated from the maximum switch ON time (T_{ONMAX0}) using following expression:

$$R_{InEqMin} = \frac{2 \cdot L_{PFC}}{T_{ONMAX0}} \tag{6}$$

Input power demand is expressed as the ratio of input power over maximum input power

$$P_{DEM} = \frac{P_{In}}{P_{Nom}} = \frac{V_{LPkL}^{2}}{V_{LMinPkL}^{2}} \cdot \frac{R_{InEqMin}}{R_{InEq}} = \frac{V_{LPkL}^{2}}{V_{LMInPkL}^{2}} \cdot \frac{T_{ON}(\alpha) \cdot \delta_{ONDCH}(\alpha)}{T_{ONMAX0}} \tag{7}$$

Arranging this to express $T_{ON}(\alpha)$ time as a function of power demand gives:

$$T_{ON}(\alpha) = P_{DEM} \cdot \frac{V_{LMInPkL}^{2}}{V_{LPkL}^{2}} \cdot \frac{T_{ONMAX0}}{\delta_{ONDCH}(\alpha)} = \frac{V_{CO}}{V_{COMax}} G_{FF} \cdot \frac{T_{ONMAX0}}{\delta_{ONDCH}(\alpha)} \tag{8}$$

Equation (8) represents the CrM/DCM T_{ON} control principle implemented by UCC28056. This equation is quadratic in nature but UCC28056 employs the value of $\delta_{ONDCH}(\alpha)$ from previous cycles as the basis for computing $T_{ON}(\alpha)$ for the current cycle. The process is much the same as solving an equation numerically by iteration.

For light load operation the CrM/DCM controller is faced with a range of possible operating frequencies. At one extreme, it can operate at high frequency with low current pulses in CrM mode (T_{DCM} = 0). At the other extreme it can operate, in DCM mode, at minimum frequency (T_{DCM} = T_{DCMMax}) with current pulses of maximum amplitude. The controller can select a T_{DCM} value that lies anywhere between these two extremes. Conduction loss will normally dominate when operating at minimum operating frequency leading to reduced efficiency. Switching loss will normally dominate when operating at maximum operating frequency (CrM) also leading to reduced efficiency. Typically the most efficient operating frequency occurs when the pulse current amplitude is around one third of its maximum value.

$$\frac{I_{LPkOpt}}{I_{LMaxPkLPkS}} = \frac{1}{3} \tag{9}$$

$$I_{LMaxPkLPkS} = \frac{V_{LMInPkL} \cdot T_{ONMAX0}}{L_{PFC}} \tag{10}$$

UCC28056 transitions from CrM to DCM operation when the peak inductor current across a Line Cycle drops below I_{LPkOpt}. While in DCM operation it adjusts the switching frequency to ensure that the peak inductor current across a Line Cycle remains close to I_{LPkOpt} for all Line and Load conditions. In this way, UCC28056 attempts to maximize efficiency for all loads and for all Line voltages.

ADVANCE INFORMATION

Feature Description (continued)

7.3.2 Line Voltage Feed-Forward

Line Voltage Feed-Forward is applied to the COMP pin voltage (V_{CO}) before it is used to compute the T_{ON} and TD_{CM} durations. Doing this ensures that COMP voltage represents input power regardless of Line voltage. This ensures that Burst operation occurs at the same level of output power for all Line voltages. It also ensures fixed gain between the COMP pin voltage and input power simplifying compensation of the voltage control loop

$$G_{FF} = \frac{V_{LMInPkL}^{2}}{V_{LPkL}} \tag{11}$$

For ease of computation, UCC28056 employs seven discrete G_{FF} levels, the most appropriate value being selected by a series of comparators monitoring the peak input voltage level. Hysteresis is built into each comparator to avoid repetitive changes in the selected GFF value and the step change in Line current that would result. The comparator thresholds and G_{FF} levels are selected to ensure that the demand to input power gain (P_{In}/V_{CO}) does not change by more than ±20% over the full Universal Line voltage range (90 - 264 V_{RMS}).

7.3.2.1 Peak Line Voltage Detection

UCC28056 internally reconstructs the input voltage waveform for the purpose of Peak Line voltage sensing and Zero Current Detection (ZCD). In DCM or CrM mode the average voltage across the PFC inductor must be zero. UCC28056 generates an internal representation of input voltage by extracting the Drain waveform from the ZCD/CS pin waveform and filtering it to extract the average Drain voltage across a switching cycle ($VI_{nSyn}(\alpha)$)

A digital peak detector is used to select the value of G_{FF} based upon the highest comparator threshold crossed over the period $T_{HLinMax}$. The switch to a higher G_{FF} value is implemented as soon as the corresponding threshold is crossed. The switch to a lower G_{FF} value is only implemented once the period $T_{HLinMax}$ expires and the peak detector has captured the line voltage peak. The $T_{HLinMax}$ timer is not synchronized to the Line operating frequency.

Prior to the start of switching operation, at power - up or after a Burst - OFF period, the ZCD/CS pin voltage is sampled and used to select the appropriate starting G_{FF} level. This method assumes that the input rectifier and capacitor after the rectifier bridge will have captured the peak Line voltage during the period of no switching.

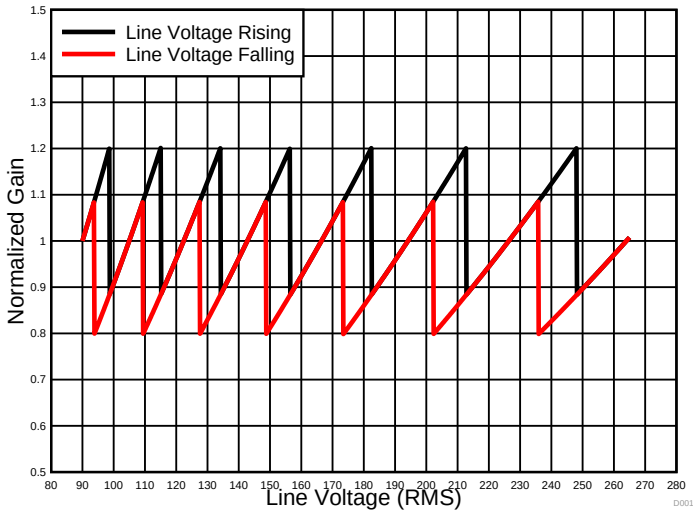


Figure 2. Normalized Gain vs Line Voltage

Feature Description (continued)

7.3.3 Valley Switching and CrM/DCM Hysteresis

UCC28056 aims for maximum efficiency by turning on the power switch when its drain voltage of the MOSFET is at a minimum, or valley, of the resonance that occurs during the T_{DCM} period . Any energy stored in the drain node capacitance (C_{DE}) is dissipated in the power switch during its turn - on transition. Valley switching ensures minimum energy is stored in C_{DE} prior to turn - on and hence minimum switching loss. After the calculated T_{DCM} period, UCC28056 waits for the next available valley on the drain voltage before initiating a new switching cycle. The actual T_{DCM} duration is therefore always an integer multiple of the drain resonance period. If the calculated T_{DCM} period extends over a valley boundary the actual T_{DCM} duration will step up in value by on e resonant period. This step change in T_{DCM} duration will cause a step change in Line current that will rapidly decay as the $T_{ON}(\alpha)$ computation iterates to a new solution to reflect the step change in T_{DCM} duration. Line current distortion, resulting from valley transitions, is kept to a minimum by computing the T_{DCM} duration from the COMP voltage. The COMP voltage varies little over the period of a Line cycle and hence the calculated T_{DCM} duration will also change little over the period of a Line cycle.

Line current distortion is particularly severe during the transition from the first valley (CrM) to the second valley (DCM) operation while the input voltage is low. In this region, the first valley duration is extended by the clamping action of the power switch body diode. In this region Line current is reduced when switching on the first valley,(CrM) , because the inductor current is negative at the start of the on period. The reduction in Line current is not observed for second or subsequent valley (DCM) operation because the inductor current starts the on period from zero. UCC28056 implements hysteresis in the T_{DCM} computation to virtually eliminate the possibility of repeated CrM/DCM transitions across a Line cycle. Such transitions can only occur if the twice Line frequency ripple on the COMP voltage is greater than 12% at the CrM/DCM boundary.

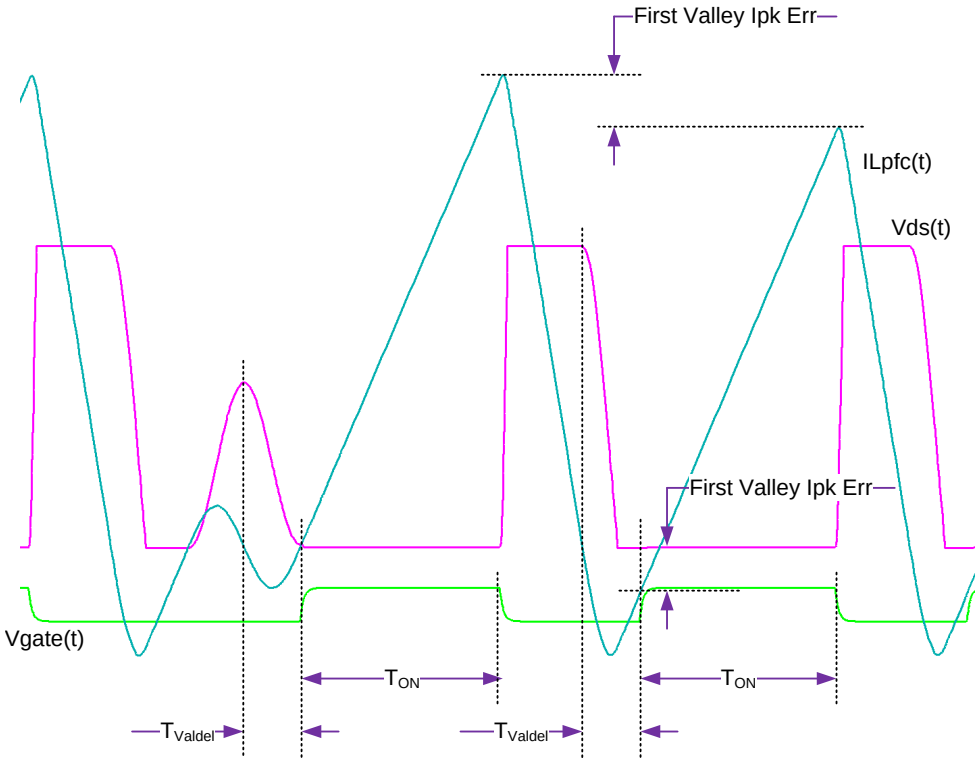


Figure 3. Drain Voltage and Inductor Current Transitioning from DCM to CrM

7.3.3.1 Valley Delay Adjustment

UCC28056 can deliver maximum efficiency when controlling power stages with widely differing natural resonant frequencies. This is achieved by allowing the designer to program externally the delay between the ZcdVIn comparator crossing and the rising edge of DRV (T_{ZCDR}). This allows the designer to ensure ideal valley switching for different power stage designs that may have very different natural resonant frequencies.

ADVANCE INFORMATION

Feature Description (continued)

The T_{ZCDR} delay can be set to one of 8 different values (T_{ZCDR0} - T_{ZCDR7}) by setting the value of a resistor (R_{DG}) connected externally between the DRV and GND pins. During start - up or when recovering from a long fault, UCC28056 transitions from its Stopb state to its RDGRdb state and then to its BstOffb state. While in the RDGRdb state an internal current source (I_{DG}) is switched to the DRV pin and the voltage that results from this current is detected and used to select the appropriate T_{ZCDR} delay. Once set, this delay will be used for all valley switching operation until a long fault causes the controller to return to its Stopb state.

After entering its RDGRdb state, UCC28056 waits for T_{DGSmpl} before reading the pin voltage. The total external capacitance connected between the DRV and GND pins should not exceed 12nF to ensure that the external resistance value is always detected correctly.

7.3.4 Transconductance Amplifier with Transient Speed-up Function

The voltage error amplifier is a transconductance amplifier. Voltage loop compensation is connected from the error amplifier output, COMP, to ground. The recommended type-II compensation network is shown in Figure 5. For loop-stability purposes, the compensation network values are calculated based on small-signal perturbations of the output voltage using the nominal transconductance gain g_M.

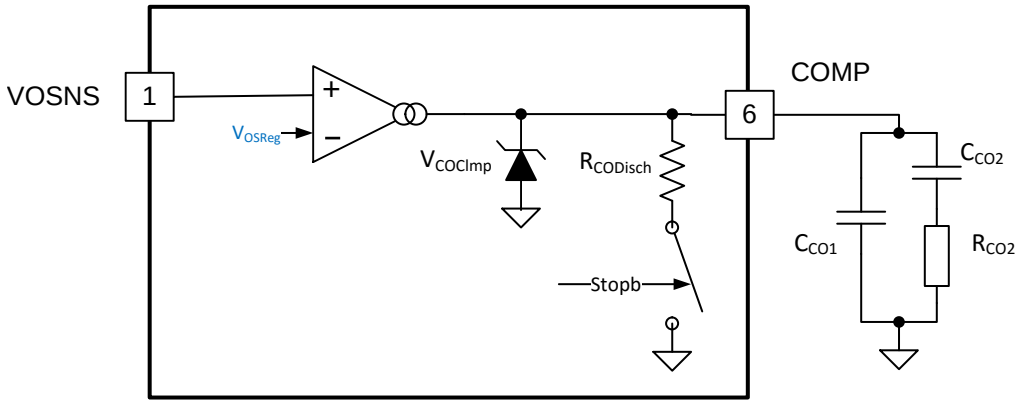


Figure 4. Transconductance Error Amplifier with Typical Compensation Network

To improve the transient response to large perturbations, the error amplifier gain increases by a factor of 6x when the error amp input deviates more than ±3% from the nominal regulation voltage, V_{OSReg}. This increase allows faster charging and discharging of the compensation components following sudden load-current increases or decreases.

7.3.5 Faults and Protections

UCC28056 includes a comprehensive set of protection features to ensure safe and robust operation under all operating conditions.

ADVANCE INFORMATION

Feature Description (continued)

7.3.5.1 Supply Under-Voltage Lockout

Supply Under-Voltage LockOut protection (UVLO) is provided to ensure that UCC28056 will only operate while the supply voltage is in a range that ensures correct operation and adequate Gate drive amplitude for the power switch.

UCC28056 remains in a dormant state, consuming little I_{CC} current ($I_{CC\_Startup}$), until the VCC pin voltage exceeds $V_{CCStart}$. Once $V_{CCStart}$ is exceeded, the controller wakes into its Stopb state. After this the controller will proceed with its normal start-up process.

UCC28056 will stop switching if the VCC pin voltage falls below V_{CCStop} for a period longer than $T_{UVLOBlk}$. The controller will then return to its dormant condition where it will remain, consuming little I_{CC} current, until the $V_{CCStart}$ threshold is exceeded once more.

7.3.5.2 Two Level Over-Current Protection

UCC28056 includes two over-current protection mechanisms to deliver safe robust protection without danger of false tripping during operating transients. During the ON period of the switch, inductor current is sensed by a current sense resistor (R_{CS}) connected in the source lead of the power switch. The voltage across the current sense resistor is detected via the ZCD/CS pin. The current sense voltage signal applied to the ZCD/CS pin may be expressed as follows. Typically the second term in the bracket will be much smaller than R_{CS} and can be neglected.

$$V_{ZC} = I_{LPFC} \cdot \left(R_{CS} + R_{DSON} \cdot \frac{R_{ZC2}}{R_{ZC1} + R_{ZC2}}\right) \approx I_{LPFC} \cdot R_{CS} \quad (12)$$

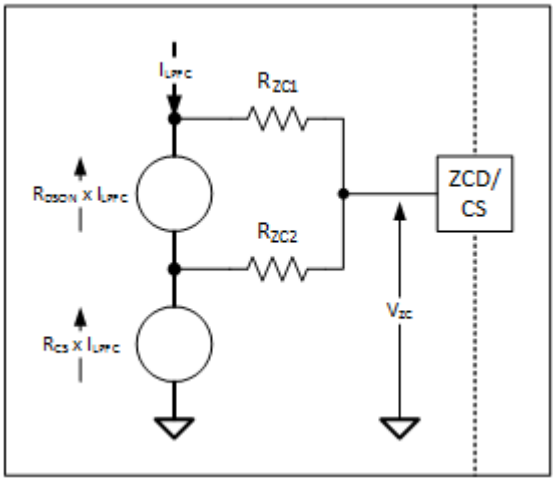


Figure 5. Equivalent Circuit of External Current Sense Network

7.3.5.2.1 Cycle-by-Cycle Current Limit Ocp1

Cycle-by-cycle peak current protection (Ocp1) terminates the T_{ON} duration early if the current sense voltage rises above 0.5V. This current protection method will limit the peak inductor current, thus avoiding inductor saturation or damage to the power stage. When cycle-by-cycle current limit is active, it will impact Line current distortion, but in all other respects normal switching operation continues and output regulation is maintained.

Leading edge blanking is applied to the current sense voltage signal. This ensures that the leading edge current spike caused by discharging C_{DE} does not cause the Ocp1 comparator to terminate the DRV pulse too early.

ADVANCE INFORMATION

Feature Description (continued)

7.3.5.2.2 Ocp2 Gross Over-Current or CCM Protection

A second comparator (Ocp2) with a higher threshold, and shorter blanking time, also monitors the current sense voltage signal. If triggered this second Ocp2 comparator will also terminate the current T_{ON} duration early. In addition, if the Ocp2 comparator is triggered on three consecutive switching cycles, it will trigger a long fault. The long fault halts switching operation and prevents restart for a period $T_{LongFlt}$. After this delay the controller will proceed with its normal start-up process. In all transient or mild fault conditions the Ocp1 comparator, with its lower threshold, will trigger first and prevent the Ocp2 comparator from acting. The Ocp2 comparator will only act if there is a gross fault such as a shorted output capacitor or bypass diode.

Under some fault conditions, including output overload, inductor current may become continuous because the reset voltage is low. In this case even the short Ocp1 blanking time may allow the inductor current to continue ramping up. UCC28056 addresses this condition by reducing the switching frequency to allow a longer period for the inductor current to ramp down between T_{ON} pulses.

The maximum allowed diode conduction period (T_{DCMMax}) is doubled in the sequence (250µs, 500µs, 1000µs) each time the T_{ON} duration is terminated early by either one of the Ocp comparators. If there is also no ZCD signal to indicate that the inductor current has fallen to zero, then the T_{DCHMax} interval must expire before the next switching cycle so the switching frequency is halved. T_{DCHMax} is halved to reverse the sequence each time the T_{ON} period is not terminated early by one of the Ocp comparators to restore the switching frequency. If the ZCD signal indicates that inductor current has reached zero, then T_{DCHMax} has no effect and normal operation will resume automatically.

7.3.5.3 Output Over-Voltage Protection

UCC28056 provides two independent forms of output over-voltage protections. This is done to ensure that no single fault can result in excessive output voltage.

7.3.5.3.1 First Level Output Over-Voltage Protection (Ovp1)

The VOSNS pin monitors output capacitor voltage via an external resistor divider comprising R_{OS1} and R_{OS2}. An internal comparator (Ovp1) monitors the VOSNS pin voltage level (V_{OS}). If the voltage on this pin rises above $V_{Ovp1Rise}$, indicating excessive output capacitor voltage, then UCC28056 transitions to its BstOffb state. In this state switching is halted to prevent further increase in the output capacitor voltage. UCC28056 will transition back to its Runb state, and resume switching operation, only once V_{OS} has fallen below $V_{Ovp1Fall}$, indicating that the output voltage is back within its normal range. To limit audible noise the T_{ON} pulse duration is ramped during the transition between Runb and BstOffb states. The method used is identical to that for Burst Mode operation.

7.3.5.3.2 Second Level Over-Voltage Protection (Ovp2)

While the Boost diode is conducting the Drain node will be one forward diode drop above the output capacitor voltage. While the power switch is off, UCC28056 monitors the Drain node via an external resistor divider network comprising R_{ZC1} and (R_{ZC2}+R_{CS}). A second over-voltage comparator (Ovp2) monitors the ZCD/CS pin voltage (V_{ZC}) during the period when the DRV pin is low and the power switch is off. If the voltage V_{ZC} rises above V_{Ovp2Th} while the DRV pin is low on four consecutive switching cycles then an Ovp2 Fault is triggered. The Ovp2 comparator output is blanked for a fixed time period after the DRV pin goes low to ensure it is not triggered by noise around DRV falling edge. An Ovp2 Fault halts switching operation and the controller transitions to its Stopb state for a period $T_{LongFlt}$. After this delay the controller will proceed with its normal start-up process.

7.3.5.4 Thermal Shutdown Protection

UCC28056 includes an internal temperature sensor. While switching, a Thermal ShutDown (TSD) fault will be triggered if the internal silicon temperature exceeds $T_{TSDRise}$ for three consecutive switching cycles. The TSD fault will halt switching operation and cause the controller to transition to its Stopb state for a period $T_{LongFlt}$. After this delay the controller will proceed with its normal start-up process.

The controller will not leave its Stopb state and begin switching operation while the internal silicon temperature is above $T_{TSDFall}$.

ADVANCE INFORMATION

Feature Description (continued)

7.3.5.5 Line Under-Voltage or Brown-Out

UCC28056 monitors the Line voltage applied to the input of the power stage. It will not allow switching operation to begin until the Line voltage is high enough to sustain normal operation. Once operating if the Line voltage falls too low to sustain normal operation then switching will be stopped. A Line Brown-Out blanking timer ensures that short dips in Line voltage do not cause unnecessary drops in output voltage.

The Line voltage start comparator will not allow the controller to leave its Stopb state until the ZCD/CS pin voltage (V_{ZC}) rises above its $V_{ZCBoRise}$ threshold.

During switching operation, UCC28056 generates an internal representation of the power stage input voltage $V_{InSyn}(\alpha)$. $V_{InSyn}(\alpha)$ is compared with the brown-out falling threshold $V_{ZCBoFall}$ by the brown-out comparator. If the output of this comparator (BoCmpb) does not go high for a full period of the LinUpdClk signal ($T_{HLinMax}$) then the brown-out timer starts to ramp up. A Line voltage brown-out fault will be triggered once the brown-out timer reaches $T_{BoBlank}$. A Line voltage brown-out fault will halt switching operation and cause the controller to transition to its Stopb state for a period $T_{LongFlt}$. After this delay the controller will proceed with its normal start-up process. If at any time, while the brown-out timer is ramping up, the brown-out comparator goes high the counter will reverse direction and start to ramp down towards zero. It will continue to ramp down to zero until the brown-out comparator output once more remains low for a full period of LinUpdClk.

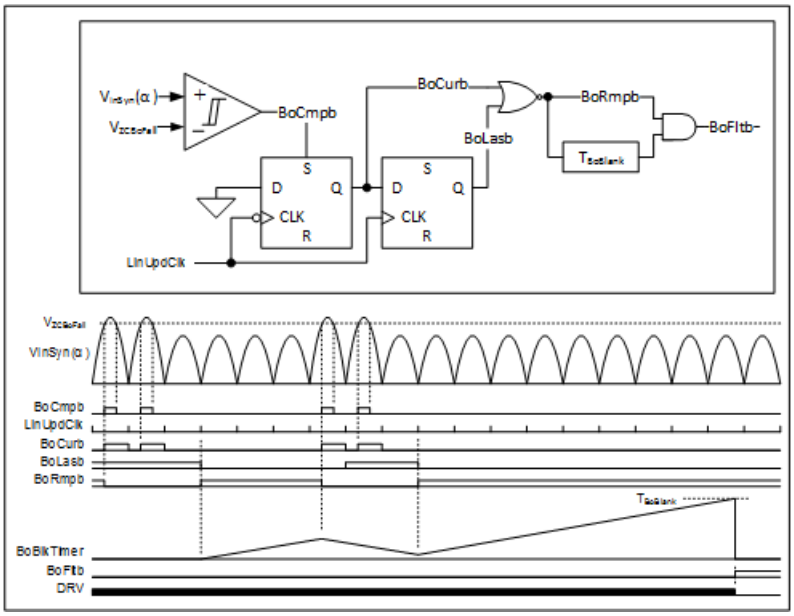


Figure 6. Line Brown-Out Protection Functional Schematic and Waveforms

7.3.6 High Current Driver

An integrated high current driver allows the power MOSFET switch to be driven directly by the UCC28056 controller. Voltage applied to the DRV pin is internally limited to V_{DRHigh}. This enables the part to be driven from a high VCC supply rail without exceeding the V_{GS} voltage rating of the power MOSFET. It also reduces power dissipation in the internal gate driver when operating from a VCC rail that is higher than V_{DRHigh}.

The integrated driver is protected against temporary short circuit of the DRV and GND pins.

ADVANCE INFORMATION

7.4 Device Functional Modes

7.4.1 Burst Mode Operation

UCC28056 provides leading light load efficiency and standby power. This is achieved by implementing Burst mode of operation with the following key features:

1. Power during burst is controlled to be approximately 11% of maximum output power for all Line voltage levels.
2. During the Burst OFF period, the current consumption of UCC28056 drops to less than 125μA.
3. The T_{ON} pulse width is ramped up over the first four cycles, and ramped down over the last four cycles of each Burst - on period. This Soft-ON/OFF scheme ramps the Line current at the edge of each Burst ON period to limit audible noise and disturbance of the EMI filter.

Two comparator thresholds applied to the COMP pin voltage provide Burst Mode Operation. Switching halts after four soft-OFF cycles when the COMP pin voltage falls below the $V_{COBstFall}$ threshold. Switching resumes with four Soft-ON cycles, when the COMP pin voltage rises above the $V_{COBstRise}$ threshold. The average voltage of these two thresholds represents approximately 11% V_{COMax}, The power delivered during Burst ON is around 11% of maximum input power.

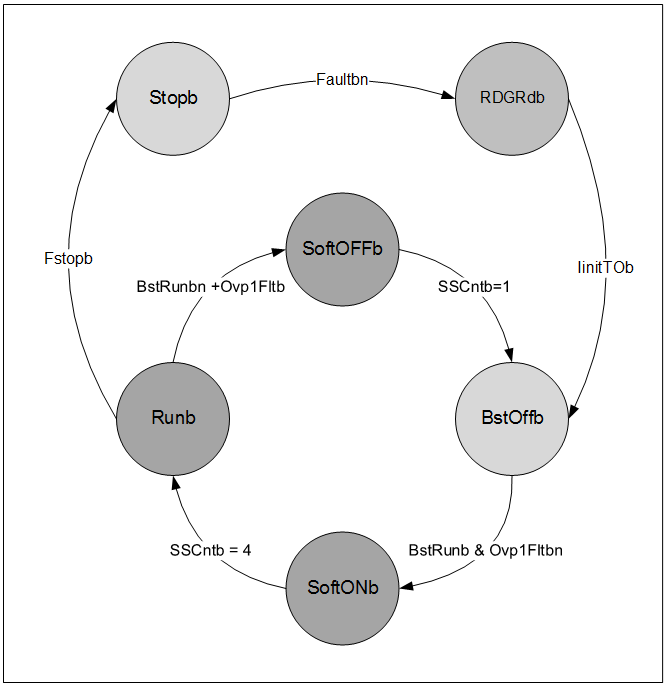


Figure 7. Fault and Burst Mode State Diagram

7.4.2 Soft Start

While in the Stopb state, an internal resistor ($R_{CODisch}$) is connected between the COMP and GND pins to discharge the external compensation network. Start-up transitions through the BstOffb state and switching will only commence when the COMP pin voltage rises above its $V_{BstRise}$ threshold. Switching will therefore always start with the power demand at 12.5% of its maximum value. In addition to this the Soft-ON feature ensures that the T_{ON} duration ramps up over the first four switching cycles to the demanded value. These features are provided to limit audible noise at start-up.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

UCC28056 can be used in a wide range of applications in which a PFC stage is needed. In order to make this device easier to use, TI has prepared a list of materials to demonstrate the features of the device:

- Full Featured EVM hardware
- Excel design calculator

In the following sections, a typical design example is presented.

8.2 Typical Application

The circuit in the Figure 8 below shows a typical application of the UCC28056 as a preregulator with high power factor and efficiency. The assembly consists of two distinct parts; the control circuit centering on the UCC28056, and the power section. The power section is a Boost converter, with the inductor operating in Transition Mode (TM/CRM) or Discontinuous Mode (DCM) according to Line and Load.

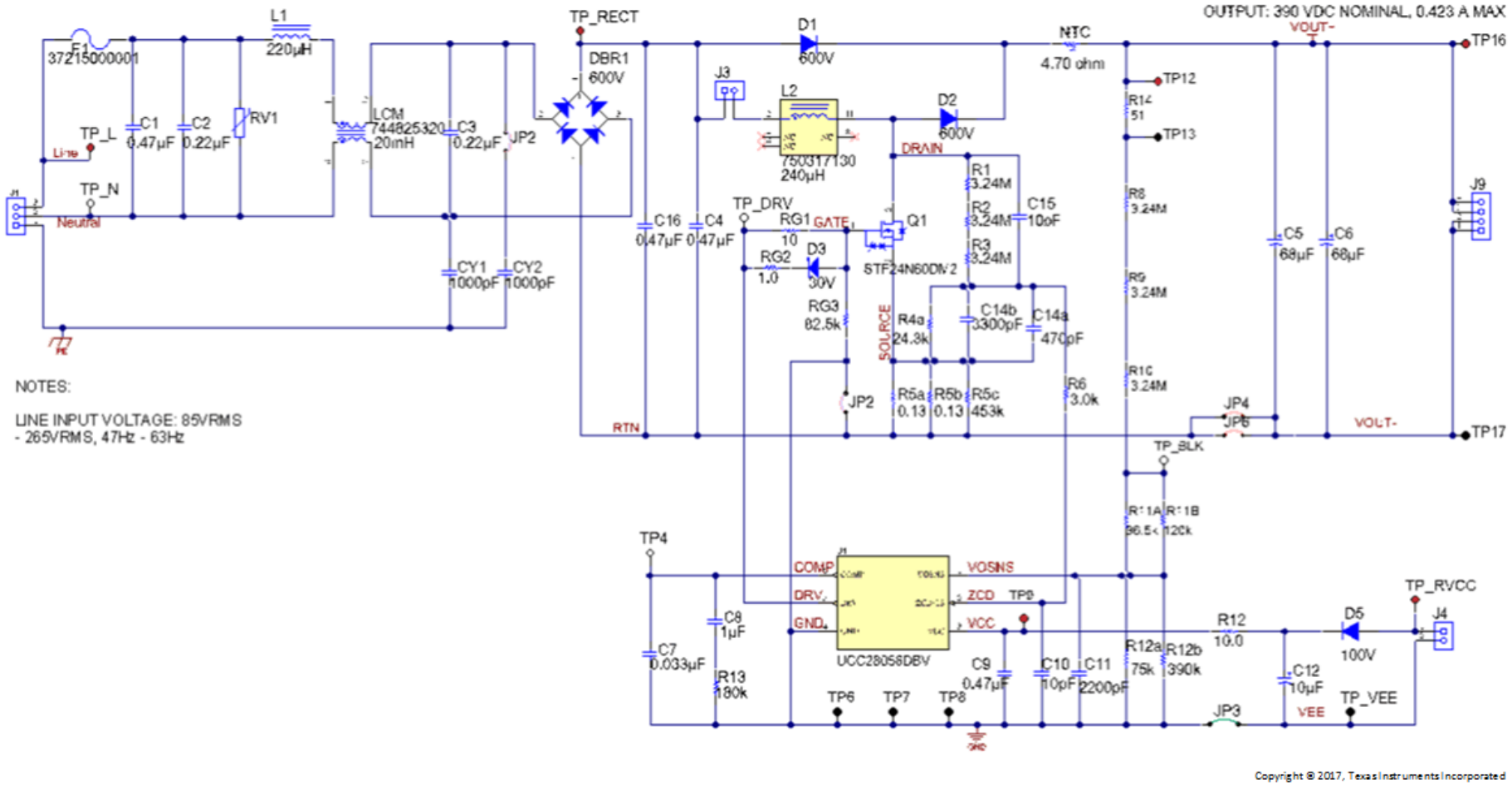


Figure 8. Typical Application Circuit for 165-W Pre-Regulator

8.2.1 Design Requirements

For this design example, use the parameters listed in the table below as the input parameters.

Table 1. System Design Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
AC Voltage range		85		265	VAC
AC Voltage frequency		47		63	Hz
OUTPUT CHARACTERISTICS					
Output Power, P_{LdMax}	85 VAC to 265 VAC			165	W

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC28056 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Power Stage Design

The first step in the power stage design is to calculate the PFC inductor value needed to achieve the specification. Once this has been done the ratings for all other power components can be computed.

8.2.2.2.1 Boost Inductor Design

The minimum equivalent resistance presented, to the Line, by the input of the Boost PFC stage changes according to the current Line Feed-Forward setting. RIn_{EqMin0} and $R_{InEqMin1}$ present the minimum equivalent input resistance for the first two Line Feed-Forward levels

$$R_{InEqMin0} = \frac{2 \cdot L_{PFC}}{T_{ONMAX0}} \tag{13}$$

$$R_{InEqMin1} = \frac{2 \cdot L_{PFC}}{T_{ONMAX1}} \tag{14}$$

The maximum input power that can be drawn from a given Line voltage is expressed in . The maximum input power is set to 110% of PLdMax to account for power stage efficiency.

$$P_{InMax} = \frac{V_{LinRMS}^{2}}{R_{InEqMin}} = 110\% \cdot P_{LdMax} \tag{15}$$

The Boost inductance value required to ensure that maximum load can be delivered from minimum Line voltage may be expressed as follows:

ADVANCE INFORMATION

$$L_{PFC0} = \frac{V_{LinRMSMin}^{2}}{110\% \cdot P_{LdMax}} \cdot \frac{T_{ONMAX0}}{2} = 255\mu H \tag{16}$$

It is also necessary to ensure that PLdMax can be delivered from the lowest Line voltage for G_{FF1}. The Boost inductor value required to achieve this is calculated as follows.

$$L_{PFC1} = \frac{(K_{ZC} \cdot V_{FF0\_F})^{2}}{110\% \cdot 2 \cdot P_{LdMax}} \cdot \frac{T_{ONMAX1}}{2} = 266\mu H \tag{17}$$

The Boost inductor values used should be the lower of the two values calculated above (L_{PFC0}, L_{PFC1}). A smaller inductance value can be used but it will compromise light load efficiency. A larger inductance value will be unable to deliver the required maximum load power (P_{LdMax}) across the required range of Line voltage.

$$L_{PFC} = 250\mu H \tag{18}$$

To deliver maximum load power the inductor must be able to operate with a peak current that is greater than both $I_{LPFCPk0}$ & $I_{LPFCPk1}$.

$$L_{LPFCk0} = \frac{V_{LinRMSMin} \cdot \sqrt{2} \cdot T_{ONMAX0}}{L_{PFC}} = 6.2A \tag{19}$$

$$L_{LPFCk1} = \frac{K_{ZC} \cdot V_{FF0\_F} \cdot T_{ONMAX1}}{L_{PFC}} = 5.8A \tag{20}$$

$$L_{LPFCk} = L_{LPFCk0} = 6.2A \tag{21}$$

The current sense resistor should be calculated to ensure that the required peak inductor current (I_{LPFCPk}) does not lead to early termination of the T_{ON} period

$$R_{CS} = \frac{V_{ZCOcp1Min}}{I_{LPFCPk}} = 73m\Omega \tag{22}$$

This value can be obtained by connecting three readily available resistors connected in parallel.

$$R_{CS} = \frac{1}{\frac{2}{0.15\Omega} + \frac{1}{3\Omega}} = 73m\Omega \tag{23}$$

The inductor should be designed to have a saturation current above the maximum Ocp1 current limit value.

$$I_{LPFCSat} \geq \frac{V_{ZCOcp1Max}}{R_{CS}} = 7.5A \tag{24}$$

Maximum current in the power components flows while delivering maximum load when supplied from minimum Line voltage. In this condition, the UCC28056 always operates in transition mode (CRM). The inductor current waveforms for ideal CRM operation are presented in Figure 9.

ADVANCE INFORMATION

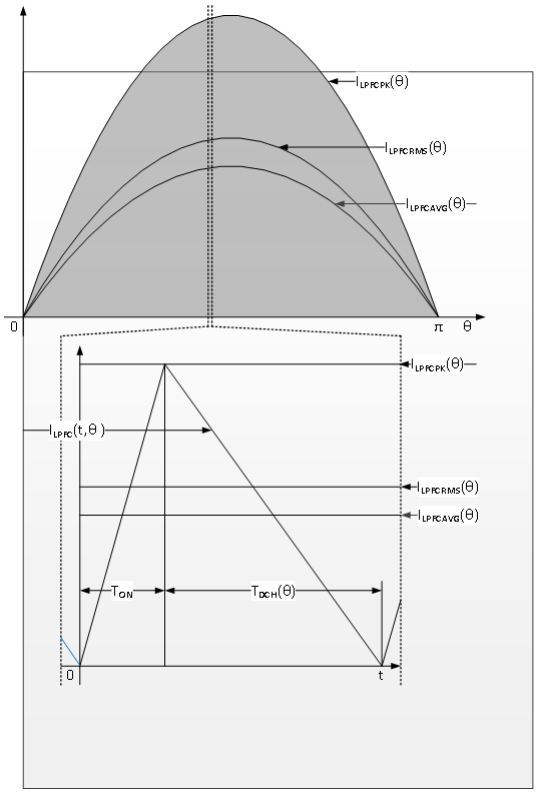


Figure 9. Ideal Transition Mode (CRM) Inductor Current

The Boost inductor RMS current over a single switching cycle, at angle θ through the Line half-cycle, is given by equation (25)

$$I_{LPFCRMS}(\theta) = \frac{2 \cdot I_{LPFCAVG}(\theta)}{\sqrt{3}} = \frac{2}{\sqrt{3}} \cdot \frac{V_{LinPK}}{R_{InEq}} \cdot \sin(\theta) \tag{25}$$

The Boost inductor RMS current over a complete Line cycle is given by equation (26).

$$I_{LPFCRMS} = \sqrt{\frac{1}{\pi} \cdot \int_0^{\pi} I_{LPFCRMS}(\theta)^2 \cdot d\theta} = \frac{2}{\sqrt{3}} \cdot \frac{V_{LinRMS}}{R_{InEq}} \tag{26}$$

Maximum Boost inductor RMS current occurs at minimum Line voltage and maximum input power.

$$I_{LPFCRMSMax} = \frac{2}{\sqrt{3}} \cdot \frac{110\% \cdot P_{LdMax}}{V_{LinRMSMin}} = 2.47A \tag{27}$$

Based upon the inductor requirements, a custom magnetic can be designed, or a suitable catalogue part selected.

Table 2. Inductor Requirements

Description	Value	Unit
Inductance	250	µH
RMS Current	2.5	A
Saturation Current	8.2	A

ADVANCE INFORMATION

8.2.2.2.2 Boost Switch Selection

The power switch carries the Boost inductor current during its ON period (T_{ON}). It carries no current during its OFF period (T_{DCH}). The switch RMS current, over a single switching cycle, at angle θ in the Line half-cycle is expressed by equation (28).

$$I_{MosRMS}(\theta) = I_{LPFCPK}\sqrt{\frac{\delta_{Mos}(\theta)}{3}} = 2\cdot\frac{V_{LinPK}}{R_{InEq}}\cdot\sin(\theta)\cdot\sqrt{\frac{\delta_{Mos}(\theta)}{3}} \tag{28}$$

The duty cycle of switch conduction for ideal transition mode (CRM) operation is given by equation (29).

$$\delta_{Mos}(\theta) = 2\cdot\frac{T_{ON}}{T_{ON}+T_{DCH}(\theta)} \tag{29}$$

The switch ON time is constant across the Line cycle but the OFF time will vary according to the position in the Line half-cycle. Volt-second balance across the Boost inductor within each switching cycle requires that.

$$\frac{T_{DCH}(\theta)}{T_{ON}} = \frac{|V_{Lin}(\theta)|}{V_{Out}+|V_{Lin}(\theta)|} \tag{30}$$

Hence duty cycle of switch conduction may be expressed as follows:

$$\delta_{Mos}(\theta) = 1-\sqrt{2}\cdot\frac{V_{LinRMS}}{V_{Out}}\cdot|\sin(\theta)| \tag{31}$$

The RMS switch current across a complete Line half-cycle may therefore be expressed as follows:

$$I_{MosRMS} = \sqrt{\frac{1}{\pi}\cdot\int_0^{\pi} I_{MosRMS}(\theta)^2\cdot d\theta} = \frac{V_{LinRMS}}{R_{InEq}}\sqrt{\frac{4}{3}-\frac{32\cdot\sqrt{2}\cdot V_{LinRMS}}{9\cdot\pi\cdot V_{Out}}} \tag{32}$$

Maximum RMS current in the switch occurs at maximum load and minimum Line.

$$I_{MosRMSMax} = \frac{110\%\cdot P_{LdMax}}{V_{LinRMSMin}}\sqrt{\frac{4}{3}-\frac{32\cdot\sqrt{2}\cdot V_{LinRMSMin}}{9\cdot\pi\cdot V_{Out}}} = 2.1A \tag{33}$$

MOSFET selection for the Boost switch can now be done on the following basis:

- The voltage rating must be greater than the maximum output voltage. Under transient or Line surge testing the output voltage may rise well above its normal regulation level. For this design example, a MOSFET voltage rating of 650V is chosen to support a regulated output voltage of 390V.
- Based upon an acceptable level of conduction loss in the MOSFET, the R_{DSON} value required can be calculated from the maximum RMS current. For this example design an STF24N60DM2 MOSFET, from STMicrolelectronics was selected with R_{DSON}@125°C = 0.37 Ohms, giving maximum conduction power loss in the MOSFET below 1.7W.
- For best efficiency a MOSFET that incorporates a fast body diode should be used. Operating with discontinuous inductor current (DCM) from a low input voltage will incur additional switching power loss if a MOSFET with slow body diode is used

ADVANCE INFORMATION

8.2.2.2.3 Boost Diode Selection

The Boost diode carries the Boost inductor current while the switch is OFF (T_{DCH}), and carries zero current while the switch is ON (T_{ON}). The RMS diode current over a single switching cycle, at angle in the Line half-cycle is expressed by equation (34).

$$I_{DioRMS}(\theta) = I_{LPFCPK}\sqrt{\frac{\delta_{Dio}(\theta)}{3}} = 2 \cdot \frac{V_{LinPK}}{R_{InEq}} \cdot \sin(\theta) \cdot \sqrt{\frac{\delta_{Dio}(\theta)}{3}} \quad (34)$$

The duty cycle of Boost diode conduction for ideal transition mode operation is given by equation (35).

$$\delta_{Dio}(\theta) = 1 - \delta_{Mos}(\theta) = \sqrt{2} \cdot \frac{V_{LinRMS}}{V_{Out}} \cdot \left|\sin(\theta)\right| \quad (35)$$

The RMS Boost diode current across a complete Line half-cycle is given by equation (36).

$$I_{DioRMS} = \sqrt{\frac{1}{\pi} \cdot \int_0^{\pi} I_{DioRMS}(\theta)^2 \cdot d\theta} = \frac{4}{3} \cdot \frac{V_{LinRMS}}{R_{InEq}} \sqrt{\frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{V_{LinRMS}}{V_{Out}}} \quad (36)$$

The maximum RMS current in the Boost diode occurs at maximum load and minimum Line.

$$I_{DioRMSMax} = \frac{4}{3} \cdot \frac{110\% \cdot P_{LdMax}}{V_{LinRMSMin}} \sqrt{\frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{V_{LinRMS}}{V_{Out}}} = 1.3A \quad (37)$$

Conduction power loss in the Boost diode is primarily a function of the average output current.

$$I_{DioAVGMax} = \frac{P_{LdMax}}{V_{Out}} = 0.42A \quad (38)$$

Boost diode selection can now be made on the following basis:

- The Boost diode requires the same voltage rating as the Boost MOSFET switch.
- The Boost diode must have average and RMS current ratings that are higher than the numbers calculated by equation (37) and equation (38).
- Diodes are available with a range of different speed/recovery charge. Fast diodes, with low reverse recovery charge, typically have higher forward voltage drop. Fast diodes will therefore have higher conduction loss but lower switching loss. Slow diodes, with high reverse recovery charge, typically have lower forward voltage drop. Slow diodes will therefore have lower conduction loss but higher switching loss. Maximum efficiency is achieved when the diode speed rating matches the application
- When Line voltage is first applied, to the Boost converter input, an uncontrolled current flows through the Boost diode while the output capacitor charges to the Line voltage peak level. The charging current is limited only by the impedance of the Line and EMI filter stage, and may reach a very high magnitude during the output capacitor charging period. Any diode carrying this current must be rated to carry this non-repetative surge current. It is normal practice to add a bypass diode to divert most of this charging current away from the Boost diode. The bypass diode can be a slow type with lower forward voltage drop. It is therefore cheaper and more robust than the faster Boost diode.
- For this example design the STTH5L06 diode from STMicroelectronics was selected. This diode has a voltage rating of 600V and an average current rating of 5A. It has a forward voltage drop of around 0.85V giving a conduction loss in the Boost diode of less than 0.5W

ADVANCE INFORMATION

8.2.2.2.4 Output Capacitor Selection

Power drawn by the PFC stage from the Line supply may be represented by the following expression.

$$P_{Lin}(\theta) = 2 \cdot V_{LinRMS} \cdot I_{LinRMS} \cdot (\sin\theta)^2 \tag{39}$$

Assuming a typical application with constant load power, for some parts of the Line cycle excess power is drawn from the supply and stored in the output capacitor. In other parts of the Line cycle load power exceeds input power and this deficit must be supplied from the output capacitor. This process of energy transfer to an from the output capacitor necessarily results in twice Line frequency output voltage ripple. The amplitude of this twice Line frequency ripple depends only upon the ratio P_{Ld}/C_{Blk} and the Line frequency.

$$\nabla V_{Blkpp} = \frac{P_{Ld}}{C_{Blk}} \frac{1}{2 \cdot \pi \cdot F_{Lin} \cdot V_{BlkReg}} \tag{40}$$

The choice of output capacitor value is determined by one of a number of application requirements:

- Twice Line frequency output ripple voltage at maximum load.
- Output voltage hold-up time after the Line supply has been disconnected.
- Output voltage deviation as a result of a transient load step.

For this design example assume that the twice Line frequency output ripple voltage amplitude should be less than 3% of its regulation level. The P_{Ld}/C_{Blk} ratio required to achieve this can be calculated using equation (41)

$$\frac{P_{LdMax}}{C_{Blk}} \le 2 \cdot \pi \cdot F_{Lin} \cdot V_{BlkReg}{}^2 \cdot 3\% = 1.43 \cdot \frac{W}{\mu F} \tag{41}$$

For this 165W example design, the capacitance value required is.

$$C_{Blk} \ge \frac{165W}{1.43 \cdot \frac{W}{\mu F}} = 115 \cdot \mu F \tag{42}$$

For best Line current THD the maximum output voltage ripple amplitude should satisfy the condition presented in equation (43). This will ensure that the error amplifier non-linear gain is not activated by extremes of the output voltage ripple.

$$\frac{\nabla V_{Blkpp}}{V_{BlkReg}} \le \frac{2 \cdot DSuThs}{V_{OSReg}} = 5.4\% \tag{43}$$

The maximum RMS ripple current flowing in the output capacitor is expressed by equation (44).

$$I_{CBlkRMSMax} = \sqrt{I_{DioRMSMax}{}^2 - \left(\frac{P_{LdMax}}{V_{BlkReg}}\right)^2} = 1.19A \tag{44}$$

This current flowing into the output capacitor is made up of a switching frequency component ($I_{CBlkRMSHF}$) and a twice Line frequency ripple component ($I_{CBlkRMSLF}$).

$$I_{CBlkRMSLF} = \frac{1}{\sqrt{2}} \cdot \frac{P_{LdMax}}{V_{BlkReg}} = 0.3A \tag{45}$$

$$I_{CBlkRMSHF} = \sqrt{I_{DioRMSMAX}{}^2 - \frac{3}{2} \cdot \left(\frac{P_{LdMax}}{V_{BlkReg}}\right)^2} = 1.15A \tag{46}$$

ADVANCE INFORMATION

Electrolytic capacitors typically have a ripple current rating at twice Line frequency (120Hz) and a different ripple current rating at switching frequency (100kHz). This reflects the fact that the capacitor ESR is higher at twice Line frequency and hence ripple current at this frequency will lead to higher power loss than the same amplitude of switching frequency ripple. The correct capacitor selection is made by determining the equivalent high frequency ripple current flowing in the capacitor.

$$I_{CEquRMSHF} = \sqrt{I_{CBlkRMSLF}^{2} \cdot K_{HLF}^{2} + I_{CBlkRMSHF}^{2}} \tag{47}$$

The parameter K_{HLF} is the ratio of high frequency to low frequency RMS ripple current rating for the particular capacitor series to be used.

$$K_{HLF} = \frac{100kHz\ RMS\ ripple\ current\ rating}{120Hz\ RMS\ ripple\ current\ rating} \tag{48}$$

In this example design, for reasons of size and rating, two 68uF 450V capacitors are selected from Rubycon BXW series (450BXW68MEFC12.5X45), connected in parallel. In this way, both the capacitance value requirement and ripple current rating are met with some additional margin.

$$C_{Blk} = 2 \cdot 68\mu F = 136\mu F \tag{49}$$

$$I_{CEquRMSHF} = \sqrt{0.3^{2} \cdot \left(\frac{1.525}{0.610}\right)^{2} + 1.15^{2}} = 1.37A \tag{50}$$

8.2.2.3 ZCD/CS Pin

An external divider network attached to the ZCD/CS pin transfers both the attenuated Drain voltage waveform (V_{DS}) and the current sense signal (V_{CS}) into the controller. This is possible because the current sense signal only needs to be observed when the switch is ON and the V_{DS} signal is close to zero. While the Drain voltage waveform only needs to be sensed when the switch is OFF and the current sense signal is close to zero.

$$V_{ZC}(t) = V_{CS}(t) + V_{DS}(t) \cdot \frac{Z_{ZC2}}{Z_{ZC1} + Z_{ZC2}} \tag{51}$$

During the T_{ON} period when the MOSFET is switched ON this may be expressed as follows:

$$V_{ZC}(t) = I_{LPFC}(t) \cdot \left(R_{CS} + R_{DSON} \cdot \frac{Z_{ZC2}}{Z_{ZC1} + Z_{ZC2}} \right) \tag{52}$$

The ON state resistance of the MOSFET (R_{DSON}) typically has a similar value to the current sense resistor R_{CS}. The attenuation of the divider (Z_{ZC1},Z_{ZC2}) is 1/401 and hence the second term of equation (52) may be neglected.

$$V_{ZC}(t) \approx I_{LPFC}(t) \cdot R_{CS} \tag{53}$$

Hence the required current sense resistor value can be calculated from the maximum peak inductor current in section 6.3.2.1

Outside the T_{ON} period, when the MOSFET is switched OFF, the current flowing through the current sense resistor is close to zero. In this case equation (52) may be expressed as follows.

$$V_{ZC}(t) \approx V_{DS}(t) \cdot \frac{Z_{ZC2}}{Z_{ZC1} + Z_{ZC2}} \tag{54}$$

UCC28056 prevents the start of a new switching cycle until increasing negative slope is detected on the ZCD/CS pin voltage waveform. The increasing negative slope indicates that the inductor current has fallen to zero so the output diode is already OFF. Turn-ON switching loss is further reduced by synchronizing the start of each new switching cycle with a minimum, or valley, on the Drain waveform.

ADVANCE INFORMATION

In theory a simple resistor divider can be used to attenuate the Drain voltage waveform fed into the ZCD/CS pin. In practice the parasitic capacitance associated with the PCB traces and the ZCD/CS pin itself will filter the attenuated signal and introduce phase shift. The resulting distortion and phase shift will negatively impact the ability of the part to synchronize to the zero inductor current transitions. The problem is compounded by the desire to limit power dissipation in the resistive divider, which dictates the use of high resistance values, and increased filtering of the attenuated signal.

Adding a capacitor divider in parallel with the resistor divider allows the use of high value resistors without introducing filtering and associated phase shift. To achieve this the reactive divider ratio should be equal to the resistor divider ratio.

$$\frac{R_{ZC2}}{R_{ZC1}+R_{ZC2}}=\frac{X_{ZC2}}{X_{ZC1}+X_{ZC2}} \tag{55}$$

Hence:

$$\frac{R_{ZC1}}{R_{ZC2}}=\frac{C_{ZC2}}{C_{ZC1}} \tag{56}$$

There are number of internal voltage thresholds driven by the attenuated Drain voltage signal supplied to the ZCD/CS pin. These include Brown-Out ($V_{ZCBoRise}$, $V_{ZCBoFall}$), Line feed-forward ($V_{FFxRise}$, $V_{FFxFall}$) and second output over-voltage (V_{Ovp2Th}). All these thresholds are driven by the same external divider ratio (K_{ZC}). Scope to vary the attenuation ratio specified is limited since it will impact of all these thresholds in unison.

$$K_{ZC}=\frac{R_{ZC1}}{R_{ZC2}}+1=401 \tag{57}$$

$$V_{LinStartRMS}=\frac{K_{ZC}}{\sqrt{2}}\cdot V_{ZCBoRise}=85V \tag{58}$$

$$V_{LinStopRMS}=\frac{K_{ZC}}{\sqrt{2}}\cdot V_{ZCBoFall}=75V \tag{59}$$

UCC28056 infers Line voltage from the switching cycle average voltage on the Drain node. Neglecting any resistive voltage drop in the PFC inductor this must be equal to the voltage supplied from the input rectifier, provided the Boost inductor current returns to zero at the end of each cycle (TM/CRM/DCM). Voltage drops in the input rectifier bridge and EMI filter stage will be observed as an error between predicted and measured threshold values. An internal peak detector is used to determine the peak input voltage across a Line half-cycle. Equation (58) and equation (59) above convert this peak value to an RMS quantity, but assume an ideal sinusoidal Line supply

The output voltage required to trigger the second output over-voltage fault is calculated as follows:

$$V_{BlkOvp2}=K_{ZC}\cdot V_{Ovp2Th}=451V \tag{60}$$

This parameter is observed via the Drain waveform, voltage drops in the Boost Diode and NTC resistor, will result in load dependent error in the measured second output over-voltage threshold level.

Power dissipation in the Drain sensing resistor divider chain will be highest during the Burst OFF condition. In this state the Drain voltage is approximates to a DC voltage equal to the Line voltage peak. This assumes the time constant C_{IN} x (R_{ZC1}+ R_{ZC2}) is long compared with a Line half period. Under no-load conditions the Burst OFF duty cycle is high therefore maximum power dissipation in the Drain sensing resistor divider chain, occurs at high Line and no-load, and is given by equation (61)

$$P_{ZCMax}=\frac{2\cdot V_{LinRMSMax}^{2}}{R_{ZC1}+R_{ZC2}} \tag{61}$$

ADVANCE INFORMATION

Allowing a budget of 1% error, due to input bias current (I_{ZCBias}), on the lowest voltage threshold ($V_{ZCBoFall}$), the maximum value of R_{ZC1} can be determined as follows.

$$R_{ZC1} \le \frac{Err\% \cdot K_{ZC} \cdot V_{ZCBoFall}}{I_{ZCBias}} = \frac{1\% \cdot 401 \cdot 0.265V}{100nA} = 10.6M\Omega \quad (62)$$

The upper resistor in the divider chain (R_{ZC1}) must withstand the peak output voltage under a surge test. For a rugged solution the resistor(s) in this location should have a voltage rating above the avalanche rating of the Boost MOSFET. A series chain of three 1206 SMT 3.24 MΩ resistors was selected for this location giving a DC voltage withstand capability above 600V.

$$R_{ZC1} = 3 \cdot 3.24M\Omega = 9.72M\Omega \quad (63)$$

$$R_{ZC2} = \frac{R_{ZC1}}{K_{ZC} - 1} = 24.3k\Omega \quad (64)$$

The power dissipation in the ZCD/CS pin divider resistors can be calculated using equation (61).

$$P_{ZCMax} = \frac{2 \cdot V_{LinRMSMax}^{2}}{R_{ZC1} + R_{ZC2}} = 9.5mW \quad (65)$$

Once arranged on the PCB, the resistor divider circuit will have some parasitic capacitance across both the upper (R_{ZC1}) and lower (R_{ZC2}) resistors. Experience suggests a parasitic capacitance (C_{ZC1}) of around 0.1pF will be present across resistor R_{ZC1}, when it is made up of three 1206 SMT parts, assuming a 'compact' PCB layout. In theory this parasitic capacitance could be used to form the entire value of C_{ZC1} and an appropriate value of C_{ZC2} added to achieve the ratio required by equation (56). In practice most designers will choose to add an explicit capacitor in this location to improve tolerance to small changes in layout, such as may occur when connecting oscilloscope probes. The time constant for the divider should not extend over many switching cycles. This ensures that transient events, such as Line surge or system ESD, may disturb the ZCD/CS pin DC level but will not persist over an excessive number of switching cycles.

For C_{ZC1} we will select a single 10-pF 1000-V 0805 SMT capacitor with 5% tolerance. This value of capacitance being readily available with the required voltage range in SMT form.

$$C_{ZC1} = 10pF \quad (66)$$

To achieve the required capacitor divider ratio the lower divider capacitor value should be.

$$C_{ZC2} = C_{ZC1} \cdot K_{ZC} = 4.01nF \quad (67)$$

In practice once the final PCB layout is complete it will be necessary to adjust the lower capacitor value to account for parasitic capacitances present on the PCB. This tuning process is best done by observing both the Drain & ZCD/CS pin waveforms and adjusting the lower capacitance value (C_{ZC2}) until the required ratio in signal amplitude is achieved. For this purpose a low capacitance probe should be used for the ZCD/CS pin connection. Figure 10,Figure 11 and Figure 12 presents the type of waveforms that may be observed during this tuning process.

ADVANCE INFORMATION

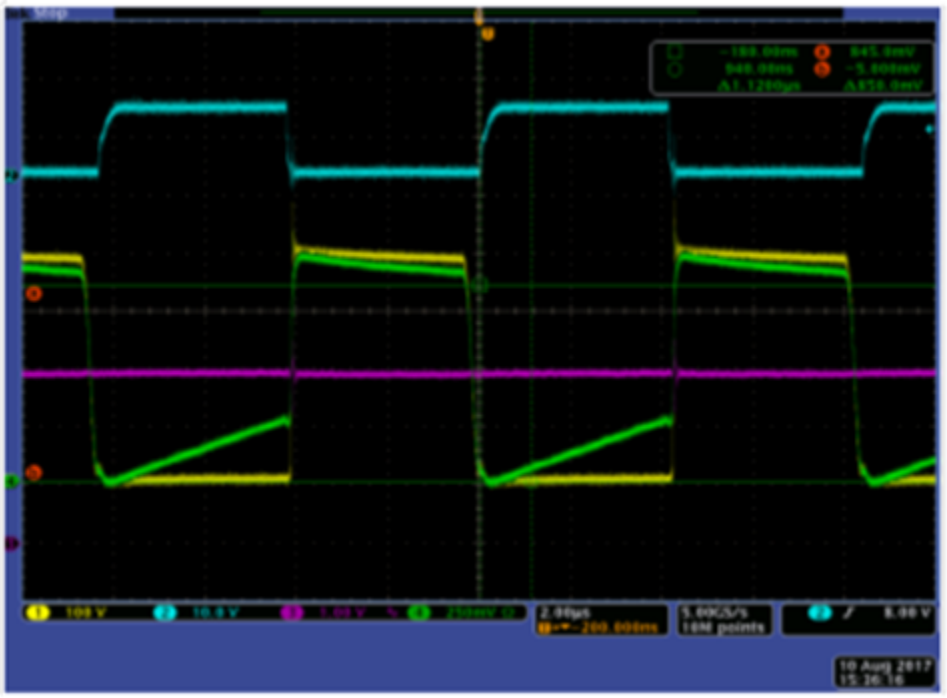


Figure 10. Amplitude V_{ZC} < (V_{DS}/401). Reduce C_{ZC2} Capacitance. CH1 = V_{DS}, CH2 = V_{DR}, CH3 = V_{CO}, CH3 = V_{ZC}

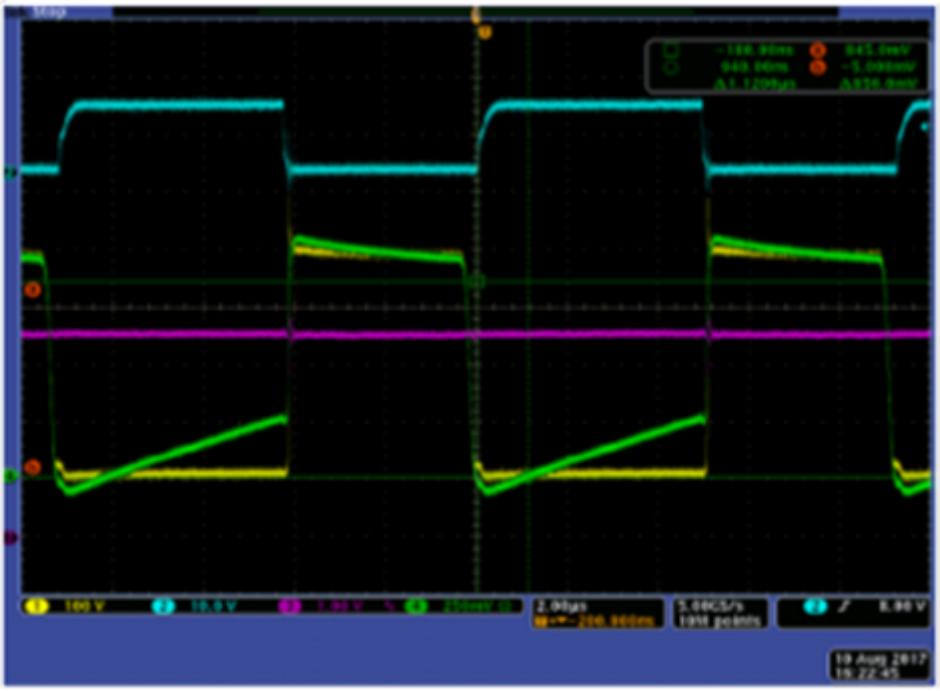


Figure 11. Amplitude V_{ZC} < (V_{DS}/401). Reduce C_{ZC2} Capacitance. CH1 = V_{DS}, CH2 = V_{DR}, CH3 = V_{CO}, CH3 = V_{ZC}

ADVANCE INFORMATION

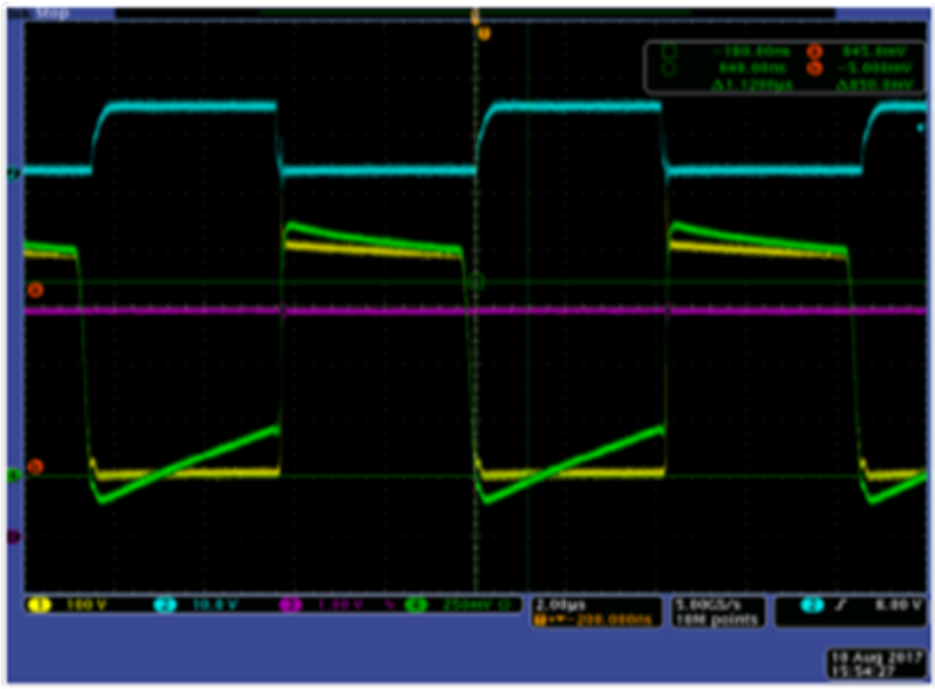


Figure 12. Amplitude V_{ZC} < (V_{DS}/401). Reduce C_{ZC2} Capacitance. CH1 = V_{DS}, CH2 = V_{DR}, CH3 = V_{CO}, CH3 = V_{ZC}

As a final check of the ZCD/CS pin divider ratio, remove all oscilloscope probes and measure the Line voltage start & stop levels using the test procedure outlined below. The measured voltage of these two parameters should be within a few volts of the values predicted by equation (58) and equation (59). A larger error on the Line start voltage level ($V_{LinStartRMS}$) suggests that the resistor divider ratio is incorrect. A larger error on the Line stop voltage level ($V_{LinStopRMS}$) indicates that the capacitor divider ratio is incorrect. If the measured Line stop voltage is too high it can be reduced by decreasing the value of C_{ZC2}.

ADVANCE INFORMATION

8.2.2.3.1 Measuring the Line Start Voltage Level

Connect an AC voltmeter across the input terminals of the rectifier bridge as shown in Figure 13. Apply voltage (VCC = 12V) to the controller and load the PFC output stage with a resistor that will draw full power when regulating. Using an electronic AC source or variable transformer ramp slowly the Line voltage used to supply the PFC stage until switching operation begins. The Line start voltage is the measured AC voltage indicated on the voltmeter immediately prior to the start of switching operation. Once switching starts the voltmeter reading will decrease slightly due to resistance of the EMI filter stage.

8.2.2.3.2 Measuring the Line Stop Voltage Level

Use an identical setup to that used to measure the Line start voltage level. First increase the AC supply voltage above its Line start level so that switching operation begins. Now slowly decrease the Line voltage until switching operation stops. The Line voltage stop voltage level is the value indicated in the AC voltmeter immediately before switching operation stops. Again the measured AC voltage is likely to rise slightly after switching operation stops due to resistance of the EMI filter stage.

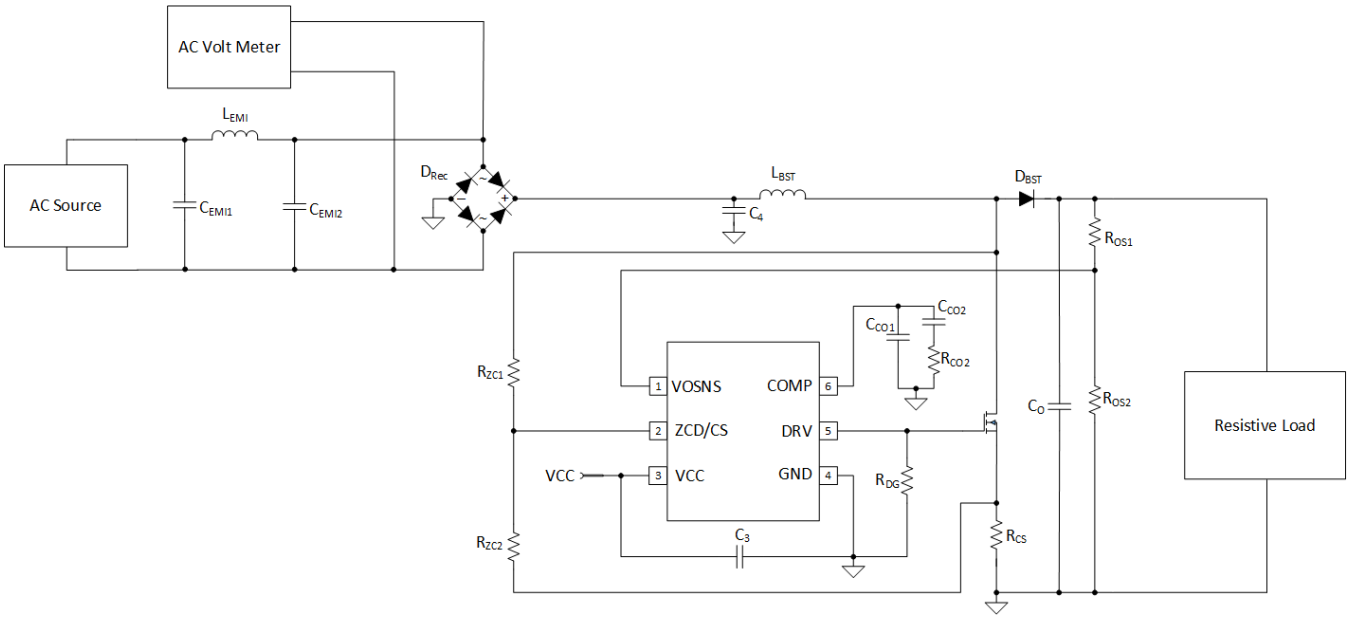


Figure 13. Test Circuit used to Measure Line Start/Stop Levels

8.2.2.3.3 Voltage Spikes on the ZCD/CS pin Waveform

Significant voltage offset on the ZCD/CS pin is likely to result from high amplitude switching edge spikes on the waveform applied to this pin. These switching edge spikes are clamped by any non-linear device, such as the internal ESD structures, and upset the DC operating point of the divider. This can be observed as a voltage offset on the ZCD/CS pin signal, particularly at times when rate of change of current is highest (high load around the Line voltage peaks). Care should be taken, when laying out the ZCD/CS pin divider, to prevent it from picking up switching edge spikes. Use of a low inductance type current sense resistor is also important for the same reason. If necessary an RC filter, with a time constant of around 30ns, may be added between the voltage divider and the ZCD/CS pin to attenuate switching edge spikes. The capacitance used (C_{ZC3}) for this filter should be small relative to C_{ZC2}. To limit the error introduced by the RC filter to less than 1%, the series resistance used in this RC filter should be below the value calculated with equation (68).

$$R_{ZC3} < \frac{V_{ZCBoFall}}{I_{ZCBias}} \cdot 1\% = 26k\Omega \tag{68}$$

For this example design, the following values were selected for the RC filter to attenuate switching edge spikes.

$$R_{ZC3} = 3k\Omega \tag{69}$$

$$C_{ZC3} = 10\,pF \tag{70}$$

8.2.2.4 VOSNS Pin

The VOSNS pin voltage is applied to the inverting input of an internal trasnconductance error amplifier. A fixed reference voltage (V_{OSReg}) being applied to the non-inverting input. The error amplifier has high gain hence in steady-state, assuming VCOMP<5V, average voltage on the VOSNS pin must be approximately equal to the reference voltage (V_{OSReg}). Output voltage regulation set point (V_{BlkReg}) is therefore determined by the external resistor divider network connecting the output voltage to the VOSNS pin according to the following expression.

$$V_{BlkReg} = V_{OSReg} \cdot \left(\frac{R_{OS1}}{R_{OS2}} + 1 \right) \tag{71}$$

The resistive divider that feeds the VOSNS pin makes a significant contribution to the unloaded input power. Higher resistor values will reduce power consumption of the divider.

$$P_{OSdiv} = \frac{V_{BlkReg}^{2}}{R_{OS1} + R_{OS2}} \tag{72}$$

Regulation accuracy degrades with increased resistor values due to the effect of VOSNS pin bias current (I_{OSBias}).

$$\frac{\Delta V_{OSReg}}{V_{OSReg}} = \frac{I_{OSBias} \cdot R_{OS1}}{V_{BlkReg}} \tag{73}$$

To ensure that VOSNS pin bias current degrades output voltage regulation by less than 1%, the upper voltage divider resistor value must be constrained as follows:

$$R_{OS1} < 1\% \cdot \frac{V_{BlkReg}}{I_{OSBias}} = 1\% \cdot \frac{390V}{100nA} = 39M\Omega \tag{74}$$

It should therefore be possible to reduce VOSNS divider dissipation below 4mW without spoiling regulation accuracy.

The PFC stage, of this design example, is to be followed by an LLC stage, that is controlled by UCC25630x. UCC28056 and UCC25630x are designed to operate together to form a complete off-Line power supply system with excellent light load efficiency and standby power. To limit no-load input power a single resistor divider is used to feed both the VOSNS pin (UCC28056) and the BLK pin (UCC25630x). A resistor divider with two taps is required since UCC28056 requires a different divide ratio (K_{OS}) to that required for UCC25630x (K_{BLK}). The upper divider resistor (R_{OS1}) is divided into two parts (R_{OS11}, R_{OS12}) to achieve the additional tap.

$$K_{OS} = \frac{V_{BlkReg}}{V_{OSReg}} = \frac{R_{OS11} + R_{OS12} + R_{OS2}}{R_{OS2}} = 156 \tag{75}$$

$$K_{BLK} = \frac{R_{OS11} + R_{OS12} + R_{OS2}}{R_{OS12} + R_{OS2}} = 108 \tag{76}$$

For this design example select an upper divider resistor made up of three series connected 3.24-MΩ 1206 SMT resistors. This is a compact and cost effective way of producing a suitable high-voltage resistor. If a single resistor is preferred, it should be of a high voltage type, rated for the maximum voltage that can appear across the output capacitor during a line surge test.

$$R_{OS11} = 3 \cdot 3.24M\Omega = 9.72M\Omega \tag{77}$$

Solving equation (75) and equation (76) simultaneously results in:

$$R_{OS12} = \frac{R_{OS11}}{K_{OS}} \cdot \left(\frac{K_{OS} - 1}{K_{BLK} - 1} - 1 \right) = 27.95k\Omega \tag{78}$$

ADVANCE INFORMATION

$$R_{OS2} = \frac{R_{OS11} + R_{OS12}}{K_{OS} - 1} = 62.89k\Omega \quad (79)$$

These two divider resistor values can be implemented using easily obtainable values as follows:

$$R_{OS12} = 36.5k\Omega \,//\, 120k\Omega = 27.98k\Omega \quad (80)$$

$$R_{OS2} = 75k\Omega \,//\, 390k\Omega = 62.90k\Omega \quad (81)$$

Actual regulation set point is therefore:

$$V_{BlkReg} = \frac{R_{OS11} + R_{OS12} + R_{OS2}}{R_{OS2}} \cdot V_{OSReg} = 390V \quad (82)$$

Power dissipated in the VOSNS resistor divider is:

$$P_{OSdiv} = \frac{V_{BlkReg}^{2}}{R_{OS11} + R_{OS12} + R_{OS2}} = 15.5mW \quad (83)$$

8.2.3 Application Curves

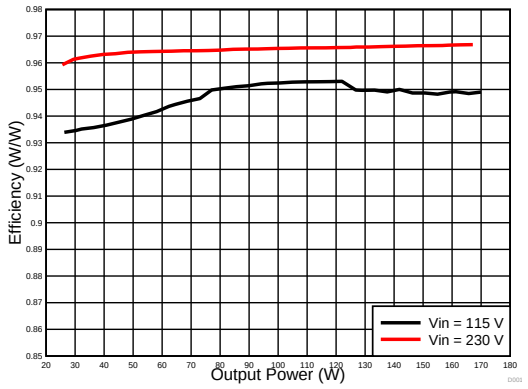


Figure 14. Efficiency vs Output Power

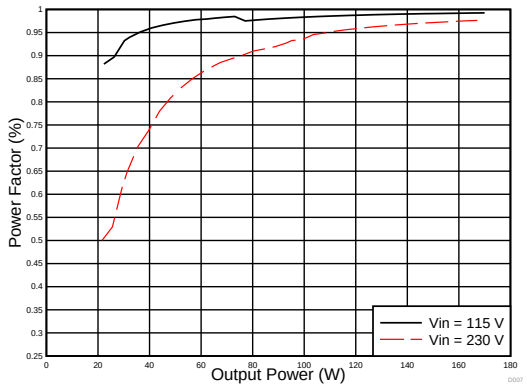


Figure 15. Power Factor vs Output Power

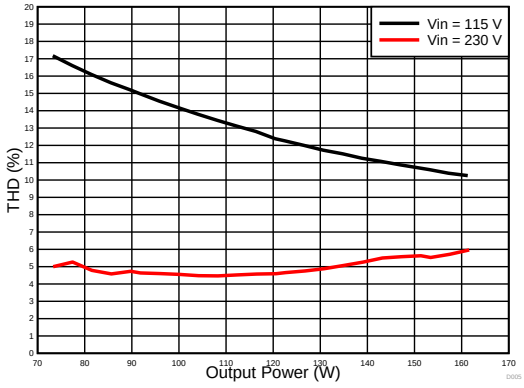


Figure 16. THD vs Output Power

ADVANCE INFORMATION

9 Power Supply Recommendations

To operate UCC28056 must be powered from an external VCC supply voltage of 11 V to - 34 V. To limit package dissipation it is recommended that the supply voltage should be not more than 12 V. The VCC supply should be locally decoupled with a capacitor of at least 1 µF connected between the VCC and GND pins via short PCB traces. UCC28056 may consume current from its VCC rail for a significant period of time, exact duration depends upon Line and load, before the output voltage (V_{Blk}) reaches regulation. The supply used to power UCC28056 must be able to source this energy during the period that output voltage is attaining regulation.

10 Layout

10.1 Layout Guidelines

10.1.1 VOSNS Pin

R_{OS2} and C_{OS2} devices should be located adjacent to the VOSNS pin along with the lowest resistor(s) making up R_{OS1}. High voltage is dropped across the resistor(s) that make up R_{OS1}. Allow adequate spacing around the high voltage nodes connecting to and within R_{OS1} to avoid air discharge across the PCB surface.

10.1.2 ZCD/CS Pin

Switching edge spikes imposed on the signal feeding this pin may cause its internal ESD structures to conduct causing offset voltage to appear on the capacitive divider feeding this pin. To limit this risk the voltage divider should be located close to the ZCD/CS pin and away from the region of fast changing magnetic field shaded in Figure 18. Keep all nets between the resistor(s)/capacitor(s) in the divider small to limit capacitive pickup within the divider chain. The loop identified in Figure 17 should be kept small and contain the minimum area to limit magnetic pickup. Connections between the current sense resistor and UCC28056 should run directly to the terminals of resistor and not be shared with power circuit traces.

When laying out the PCB start with the ZCD/CS pin divider placement and routing to ensure that the needs of this pin come first.

10.1.3 VCC Pin

A local decoupling capacitor should be connected directly between the VCC and GND pins via short, dedicated, PCB traces. This capacitor supplies the high current pulses needed to charge the gate capacitance of the power MOSFET.

10.1.4 GND Pin

Keep PCB traces for the GND net of UCC28056 separate from the power circuit GND net. UCC28056 GND should connect to the power circuit GND only at one terminal of the current sense resistor. This is done to ensure that the voltage between UCC28056 GND and ZCD/CS pins is equivalent to the voltage across the current sense resistor during the MOSFET conduction period.

10.1.5 DRV Pin

Avoid running the DRV pin traces close to other high impedance nets such as ZCD/CS or VOSNS. The fast rising and falling edges associated with the waveform on this pin may capacitively couple onto these high impedance nets causing disturbance around the switching edges.

10.1.5.1 COMP Pin

Locate the RC network attached to this pin close to the pin. Return to the GND pin should be via a short PCB trace.

10.2 Layout Example

ADVANCE INFORMATION

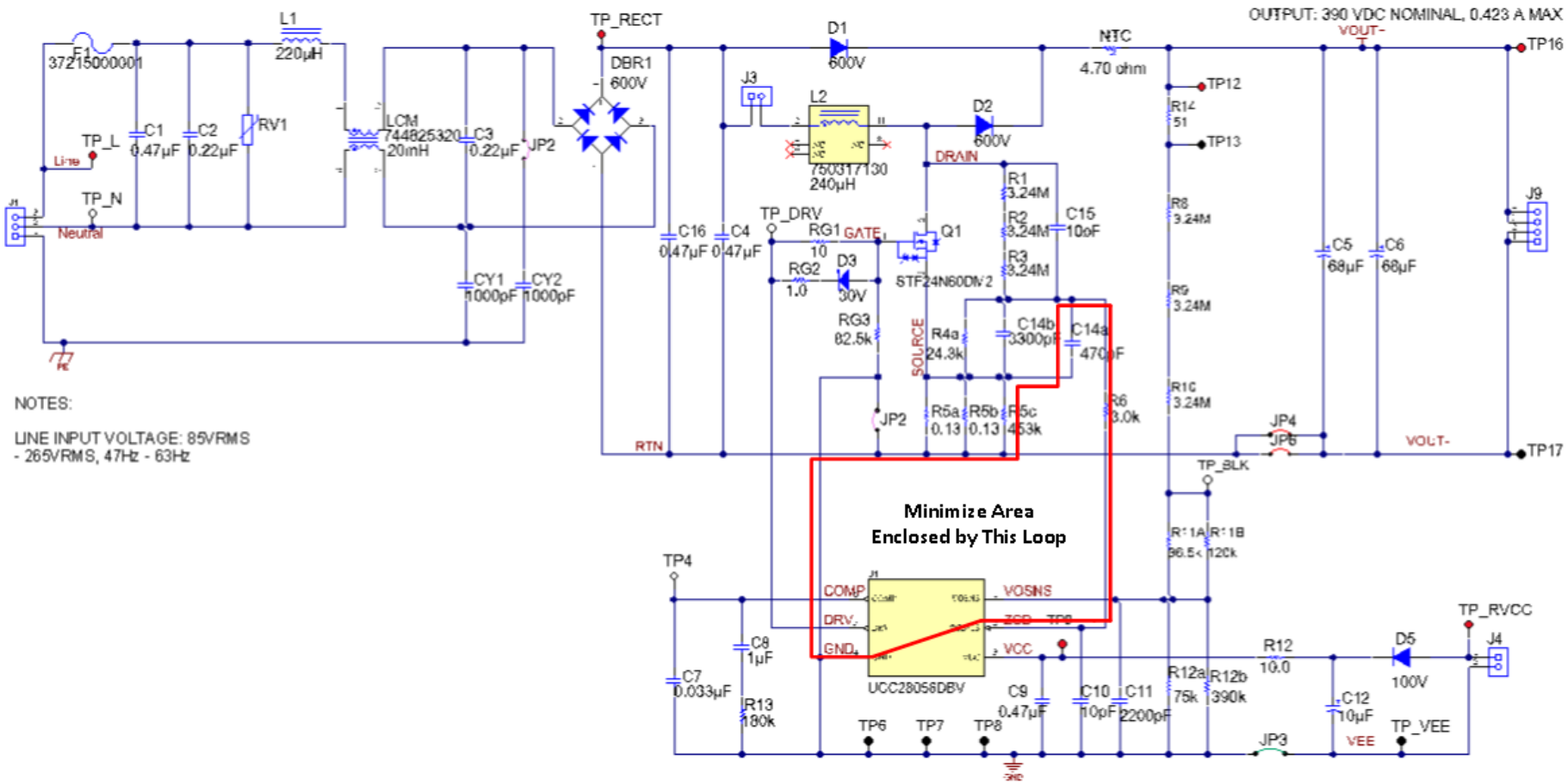


Figure 17. Schematic with Layout Guidelines

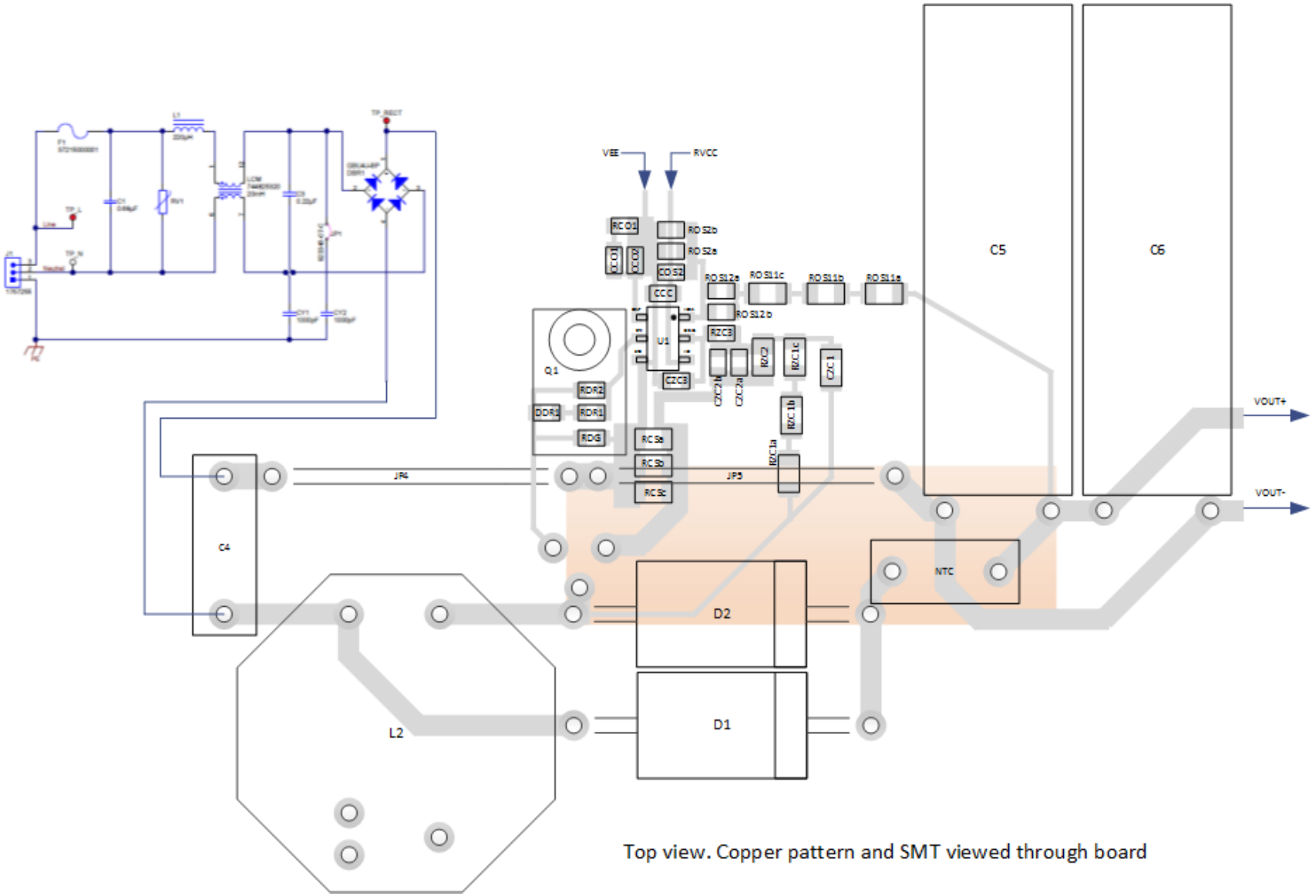


Figure 18. Recommended PCB Layout (Single-Sided Assembly)

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC28056 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28056DBVR	PREVIEW	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	8056	
UCC28056DBVT	PREVIEW	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	8056	
XUCC28056DBV	ACTIVE	SOT-23	DBV	6	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

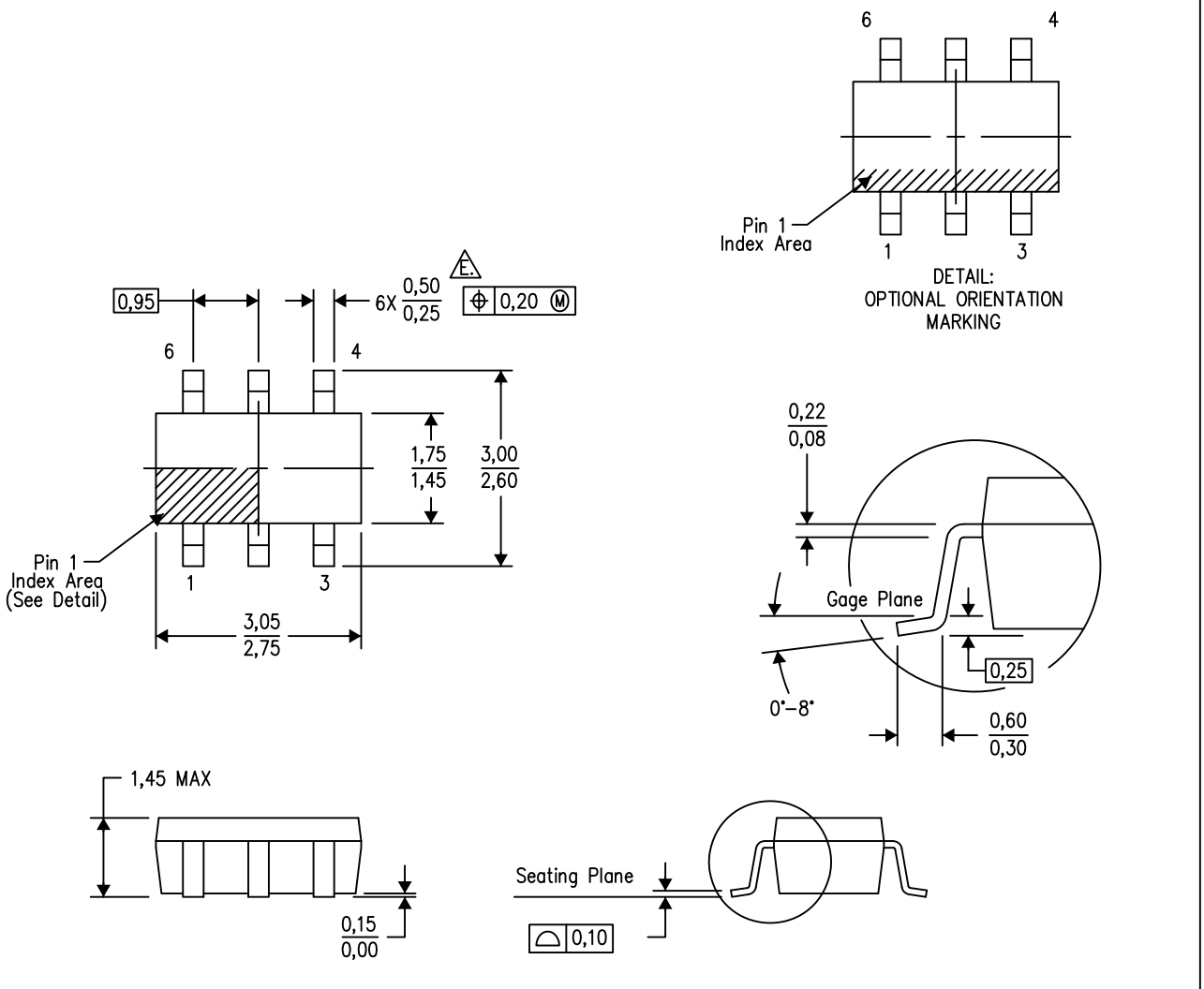
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

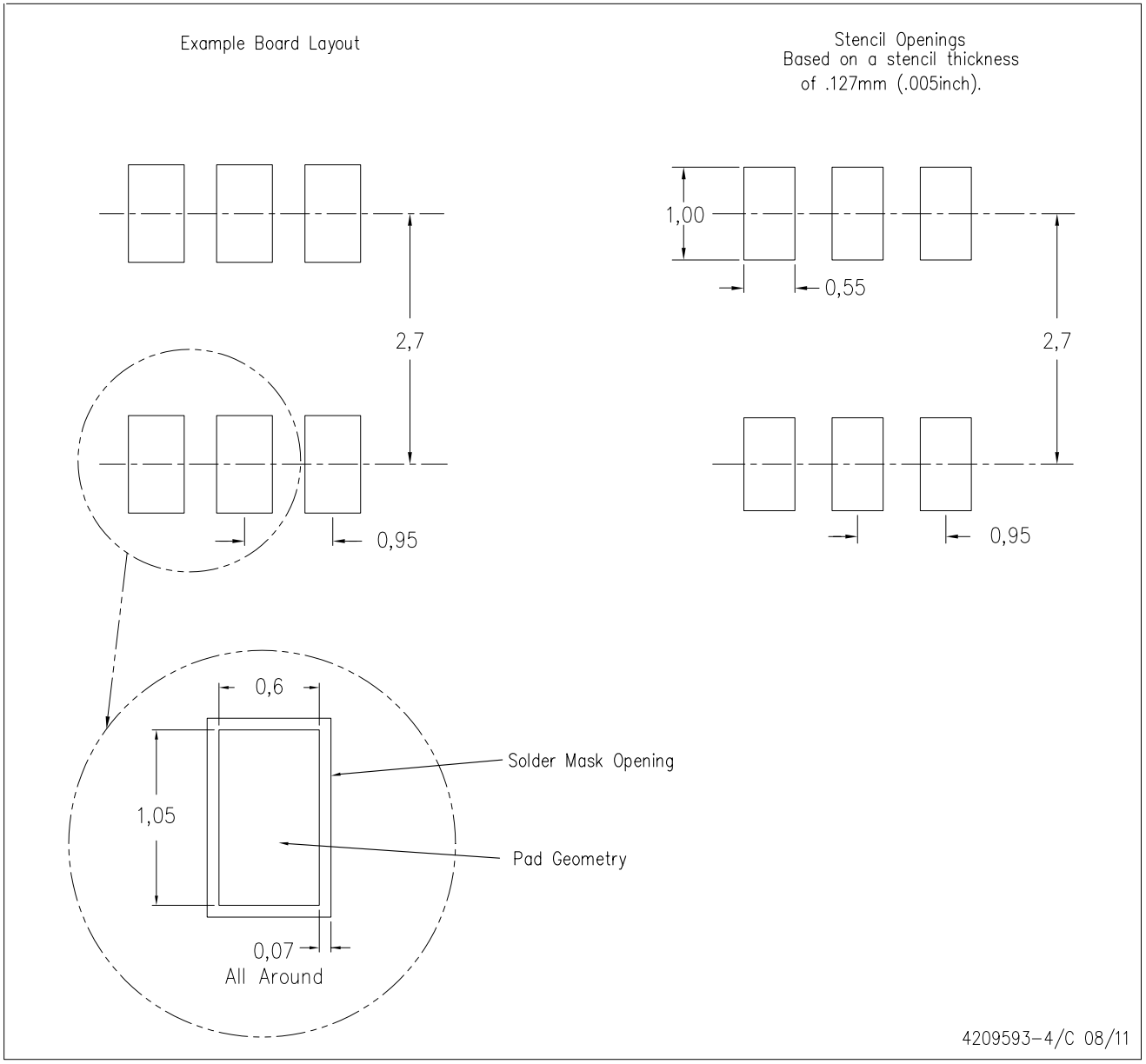
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265