

TOSHIBA Power MOS FET Module Silicon N&P Channel MOS Type (Six L²-π-MOSV inOne)

MP6404

High Power High Speed Switching Applications

3-Phase Motor Drive and Stepping Motor Drive Applications

- 4-V gate drivability
- Small package by full molding (SIP 12 pins)
- High drain power dissipation (6-device operation)
: PT = 36 W (Tc = 25°C)
- Low drain-source ON resistance: RDS (ON) = 120 mΩ (typ.) (Nch)
160 mΩ (typ.) (Pch)
- High forward transfer admittance: |Yfs| = 5.0 S (typ.) (Nch)
4.0 S (typ.) (Pch)
- Low leakage current: IGSS = ±10 µA (max) (VGS = ±16 V)
IDSS = 100 µA (max) (VDS = 60 V)
- Enhancement-mode: Vth = 0.8 V to 2.0 V (VDS = 10 V, ID = 1 mA)

Absolute Maximum Ratings (Ta = 25°C)

| Characteristics | | Symbol | Rating | | Unit |
|---|--------------------|------------------|------------|-----|------|
| | | | Nch | Pch | |
| Drain-source voltage | | V _{DSS} | 60 | -60 | V |
| Drain-gate voltage (R _{GS} = 20 kΩ) | | V _{DGR} | 60 | -60 | V |
| Gate-source voltage | | V _{GSS} | ±20 | ±20 | V |
| Drain current | DC | I _D | 5 | -5 | A |
| | Pulse | I _{DP} | 20 | -20 | |
| Drain power dissipation (1-device operation, Ta = 25°C) | | P _D | 2.2 | | W |
| Drain power dissipation (6-device operation) | Ta = 25°C | P _{DT} | 4.4 | | W |
| | Tc = 25°C | | 36 | | |
| Single pulse avalanche energy (Note 1) | | E _{AS} | 129 | 273 | mJ |
| Avalanche current | | I _{AR} | 5 | -5 | A |
| Repetitive avalanche energy (Note 2) | 1 device operation | E _{AR} | 0.22 | | mJ |
| | 6 device operation | E _{ART} | 0.44 | | |
| Channel temperature | | T _{ch} | 150 | | °C |
| Storage temperature range | | T _{stg} | -55 to 150 | | °C |

Note 1: Condition for avalanche energy (single pulse)

Nch: V_{DD} = 25 V, starting T_{ch} = 25°C, L = 7 mH, R_G = 25 Ω, I_{AR} = 5 APch: V_{DD} = -25 V, starting T_{ch} = 25°C, L = 14.84 mH, R_G = 25 Ω, I_{AR} = -5 A

Note 2: Repetitive rating; pulse width limited by maximum channel temperature

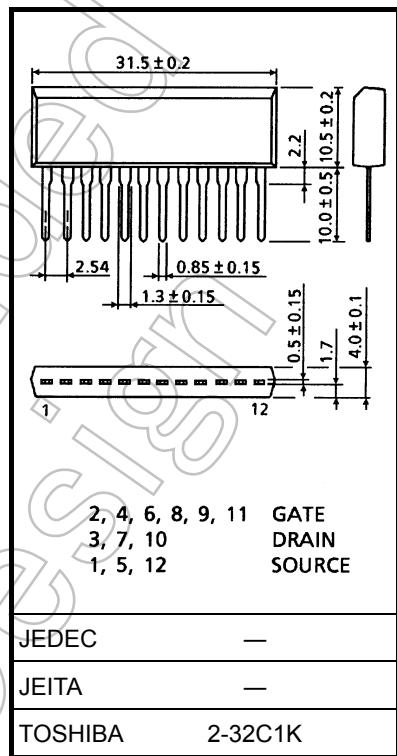
Note 3: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

This transistor is an electrostatic-sensitive device. Please handle with caution.

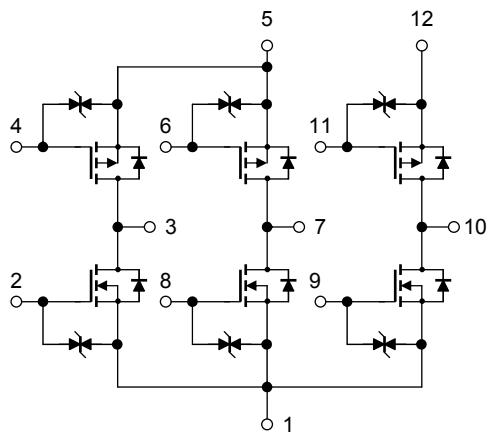
Industrial Applications

Unit: mm



Weight: 3.9 g (typ.)

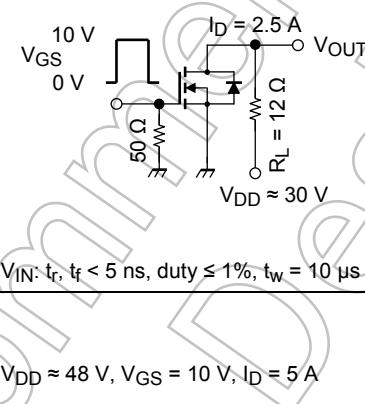
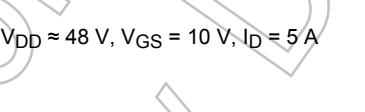
Array Configuration



Thermal Characteristics

| Characteristics | Symbol | Max | Unit |
|--|-------------------------------------|------|--------------------|
| Thermal resistance of channel to ambient (6-device operation, $T_a = 25^\circ\text{C}$) | $\Sigma R_{\text{th}}(\text{ch-a})$ | 28.4 | $^\circ\text{C/W}$ |
| Thermal resistance of channel to case (6-device operation, $T_c = 25^\circ\text{C}$) | $\Sigma R_{\text{th}}(\text{ch-c})$ | 3.47 | $^\circ\text{C/W}$ |
| Maximum lead temperature for soldering purposes (3.2 mm from case for $t = 10\text{ s}$) | T_L | 260 | $^\circ\text{C}$ |

Electrical Characteristics (Ta = 25°C) (Nch MOS FET)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|-----------------------|--|---|------|------|------|
| Gate leakage current | I _{GSS} | V _{GS} = ±16 V, V _{DS} = 0 V | — | — | ±10 | µA |
| Drain cut-off current | I _{DSS} | V _{DS} = 60 V, V _{GS} = 0 V | — | — | 100 | µA |
| Drain source breakdown voltage | V _{(BR) DSS} | I _D = 10 mA, V _{GS} = 0 V | 60 | — | — | V |
| Gate threshold voltage | V _{th} | V _{DS} = 10 V, I _D = 1 mA | 0.8 | — | 2.0 | V |
| Drain-source ON resistance | R _{DS (ON)} | V _{GS} = 4 V, I _D = 2.5 A | — | 0.21 | 0.32 | Ω |
| | | V _{GS} = 10 V, I _D = 2.5 A | — | 0.12 | 0.16 | |
| Forward transfer admittance | Y _{fsl} | V _{DS} = 10 V, I _D = 2.5 A | 3.0 | 5.0 | — | S |
| Input capacitance | C _{iss} | V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz | — | 370 | — | pF |
| Reverse transfer capacitance | C _{rss} | | — | 60 | — | pF |
| Output capacitance | C _{oss} | | — | 180 | — | pF |
| Switching time | Rise time | t _r |  | — | 18 | — |
| | Turn-on time | t _{on} | | — | 25 | — |
| | Fall time | t _f | | — | 55 | — |
| | Turn-off time | t _{off} | | — | 170 | — |
| Total gate charge (gate-source plus gate-drain) | Q _g |  | — | 12 | — | nC |
| Gate-source charge | Q _{gs} | | — | 8 | — | nC |
| Gate-drain ("miller") charge | Q _{gd} | | — | 4 | — | nC |

Source-Drain Diode Ratings and Characteristics (Ta = 25°C)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|----------------------------------|------------------|--|-----|------|------|------|
| Continuous drain reverse current | I _{DR} | — | — | — | 5 | A |
| Pulse drain reverse current | I _{DRP} | — | — | — | 20 | A |
| Diode forward voltage | V _{DSF} | I _{DR} = 5 A, V _{GS} = 0 V | — | — | -1.7 | V |
| Reverse recovery time | t _{rr} | I _{DR} = 5 A, V _{GS} = 0 V dI _{DR} /dt = 50 A/µs | — | 70 | — | ns |
| Reverse recovery charge | Q _{rr} | | — | 0.1 | — | µC |

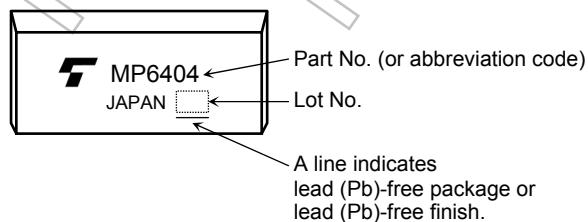
Electrical Characteristics ($T_a = 25^\circ\text{C}$) (Pch MOS FET)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit | |
|---|-----------------------------|--|---|------|----------|---------------|-------------|
| Gate leakage current | I_{GSS} | $V_{GS} = \pm 16\text{ V}$, $V_{DS} = 0\text{ V}$ | — | — | ± 10 | μA | |
| Drain cut-off current | I_{DSS} | $V_{DS} = -60\text{ V}$, $V_{GS} = 0\text{ V}$ | — | — | -100 | μA | |
| Drain source breakdown voltage | $V_{(\text{BR})\text{DSS}}$ | $I_D = -10\text{ mA}$, $V_{GS} = 0\text{ V}$ | -60 | — | — | V | |
| Gate threshold voltage | V_{th} | $V_{DS} = -10\text{ V}$, $I_D = -1\text{ mA}$ | -0.8 | — | -2.0 | V | |
| Drain-source ON resistance | $R_{DS\text{ (ON)}}$ | $V_{GS} = -4\text{ V}$, $I_D = -2.5\text{ A}$ | — | 0.24 | 0.28 | Ω | |
| | | $V_{GS} = -10\text{ V}$, $I_D = -2.5\text{ A}$ | — | 0.16 | 0.19 | | |
| Forward transfer admittance | $ Y_{fs} $ | $V_{DS} = -10\text{ V}$, $I_D = -2.5\text{ A}$ | 2.0 | 4.0 | — | S | |
| Input capacitance | C_{iss} | $V_{DB} = -10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$ | — | 630 | — | pF | |
| Reverse transfer capacitance | C_{rss} | | — | 95 | — | pF | |
| Output capacitance | C_{oss} | | — | 290 | — | pF | |
| Switching time | Rise time | t_r | | — | 25 | — | |
| | Turn-on time | t_{on} | | — | 45 | — | |
| | Fall time | t_f | | — | 55 | — | |
| | Turn-off time | t_{off} | | — | 200 | — | |
| Total gate charge (gate-source plus gate-drain) | | Q_g | $V_{DD} \approx -48\text{ V}$, $V_{GS} = -10\text{ V}$, $I_D = -5\text{ A}$ | — | 22 | — | nC |
| Gate-source charge | | Q_{gs} | | — | 16 | — | nC |
| Gate-drain ("miller") charge | | Q_{gd} | | — | 6 | — | nC |

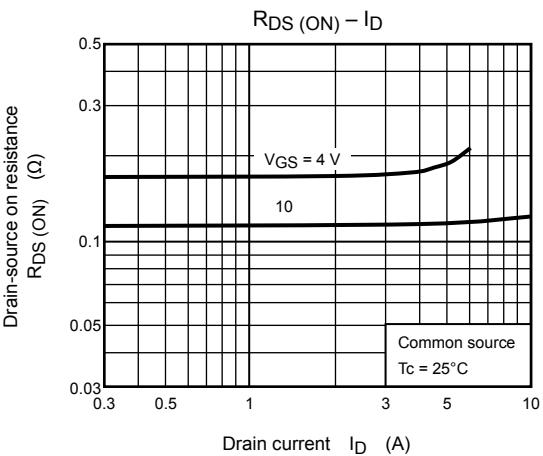
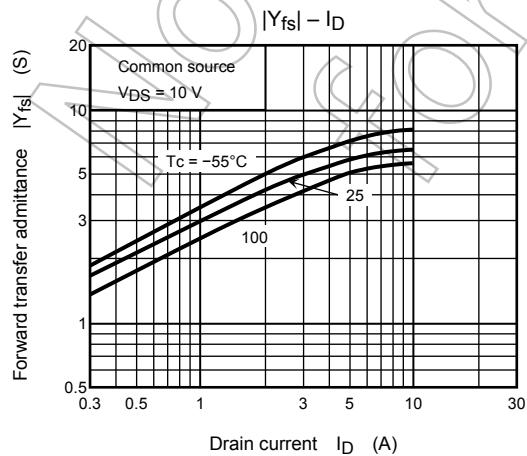
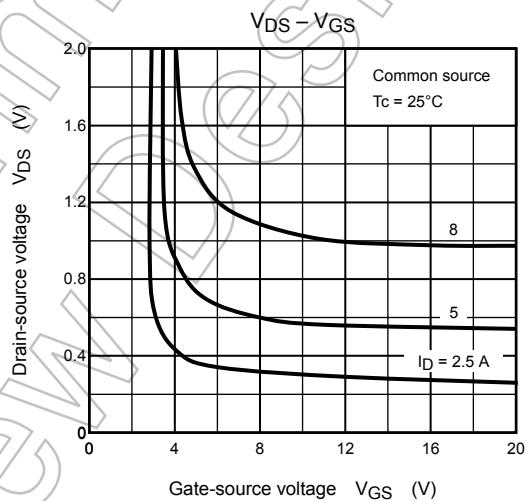
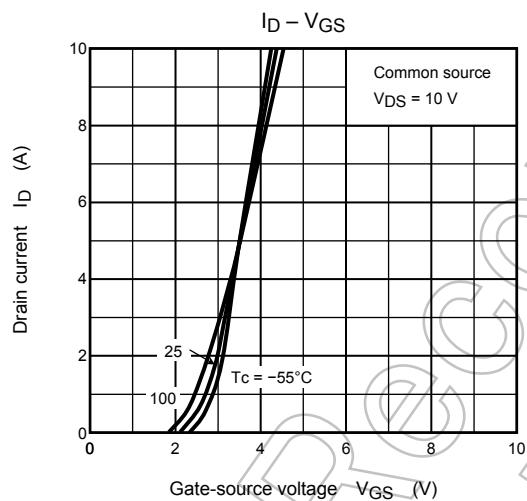
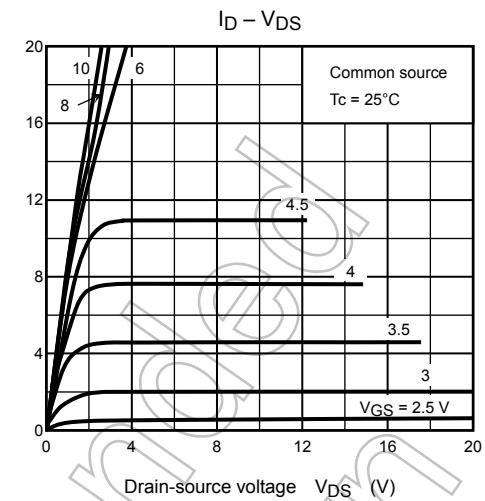
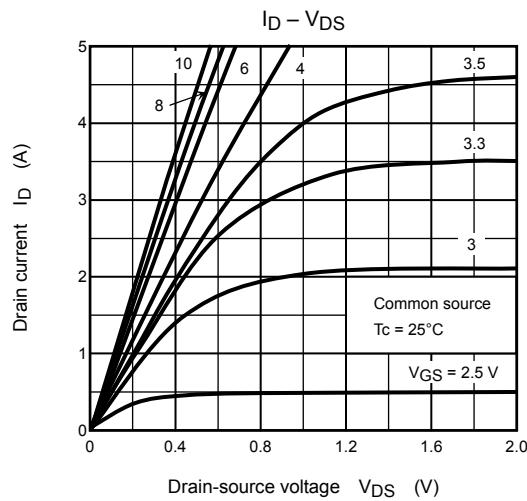
Source-Drain Diode Ratings and Characteristics ($T_a = 25^\circ\text{C}$)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|----------------------------------|-----------|--|-----|------|-----|---------------|
| Continuous drain reverse current | I_{DR} | — | — | — | -5 | A |
| Pulse drain reverse current | I_{DRP} | — | — | — | -20 | A |
| Diode forward voltage | V_{DSF} | $I_{DR} = -5\text{ A}$, $V_{GS} = 0\text{ V}$ | — | — | 1.7 | V |
| Reverse recovery time | t_{rr} | $I_{DR} = -5\text{ A}$, $V_{GS} = 0\text{ V}$ $dI_{DR}/dt = 50\text{ A}/\mu\text{s}$ | — | 80 | — | ns |
| Reverse recovery charge | Q_{rr} | | — | 0.1 | — | μC |

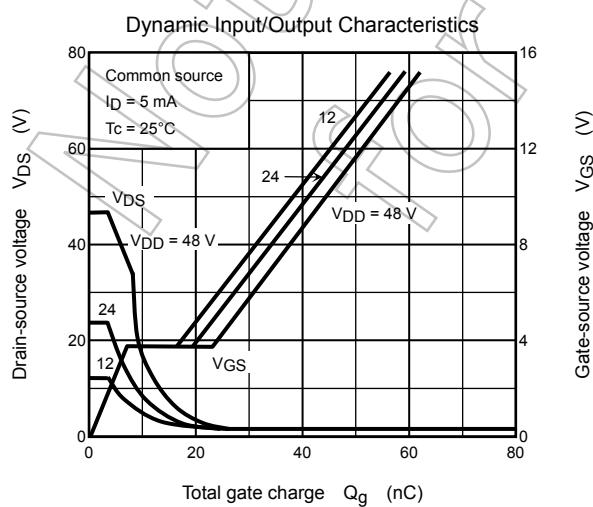
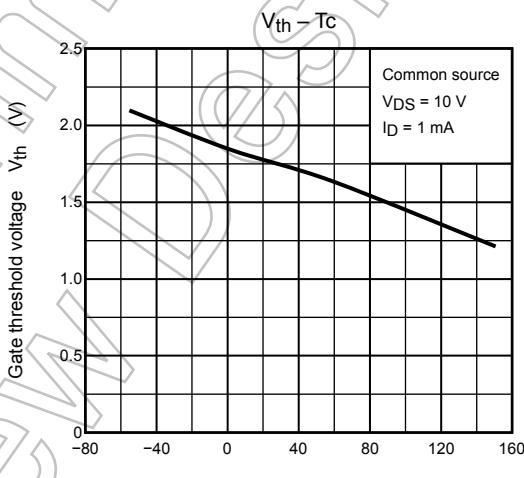
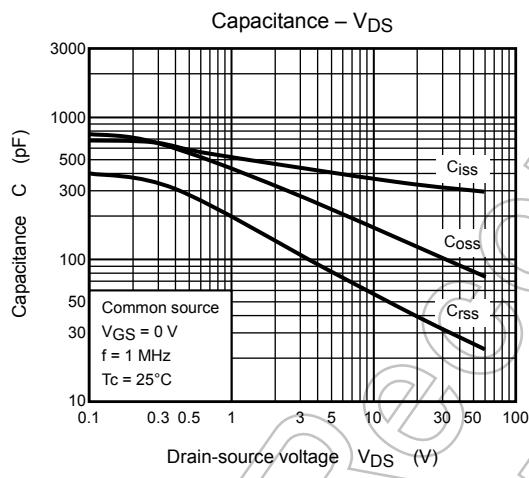
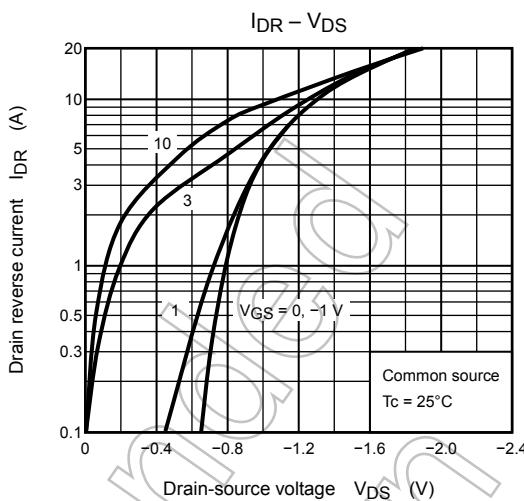
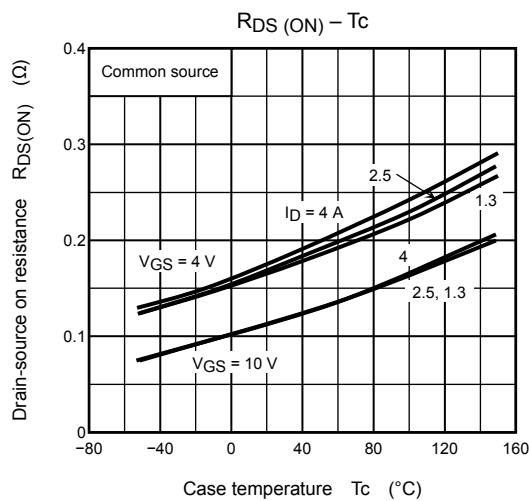
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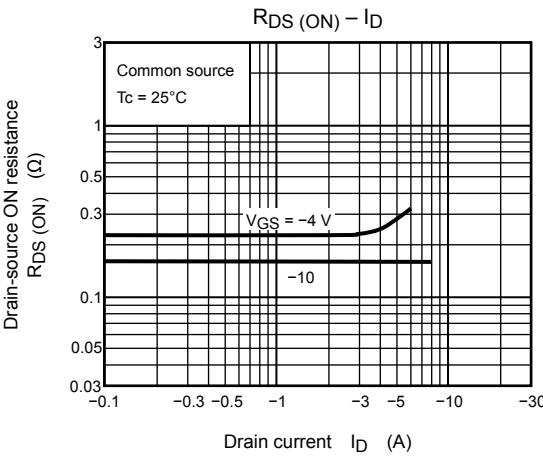
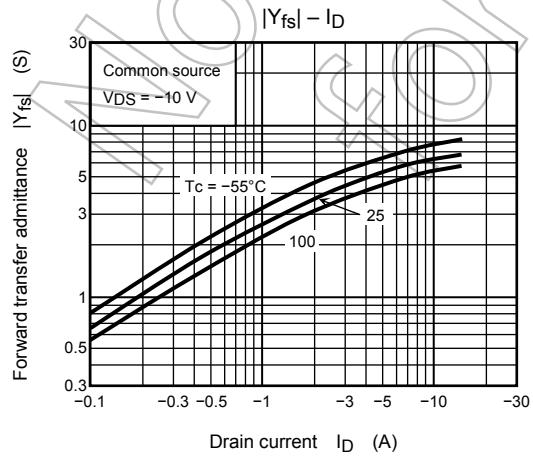
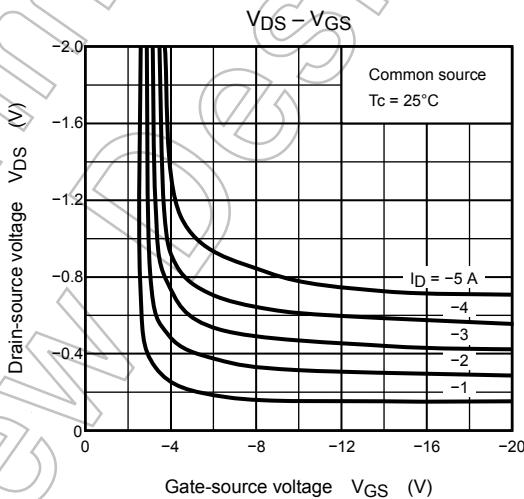
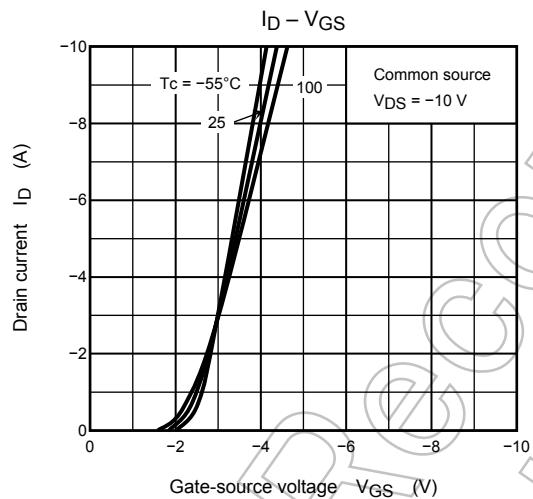
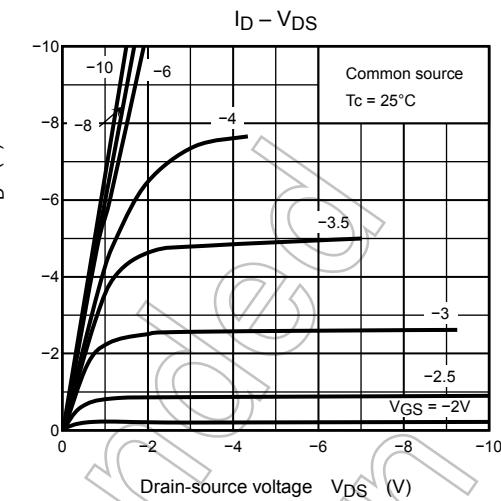
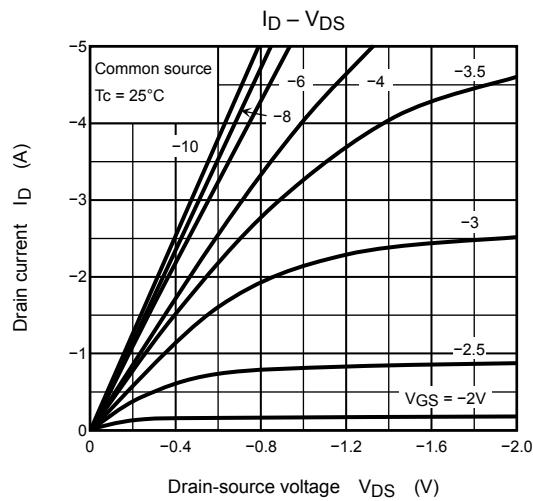
Nch MOS FET



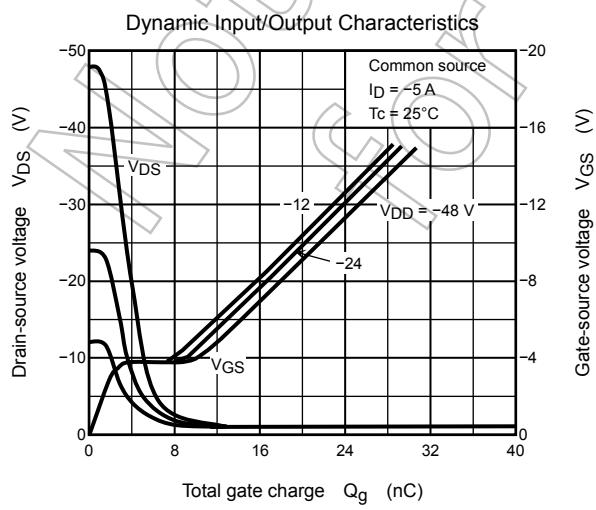
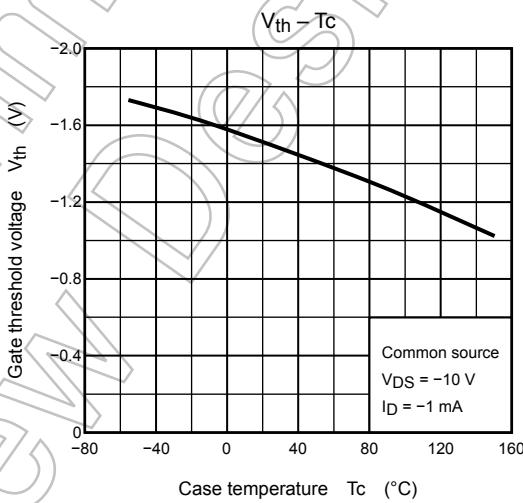
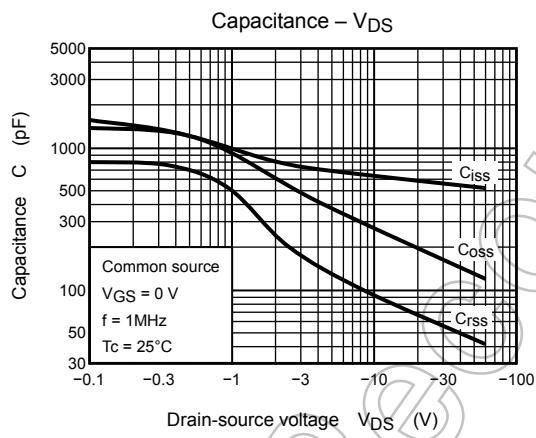
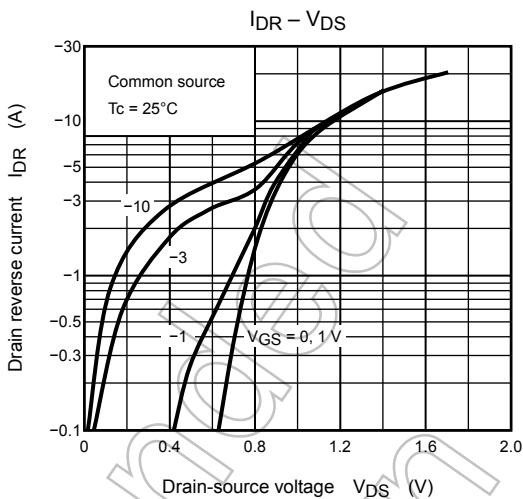
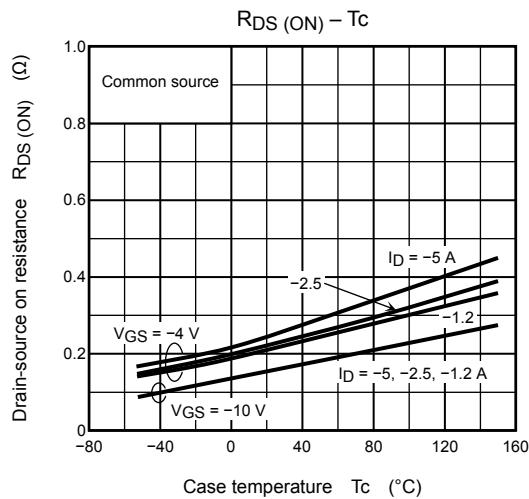
Nch MOS FET

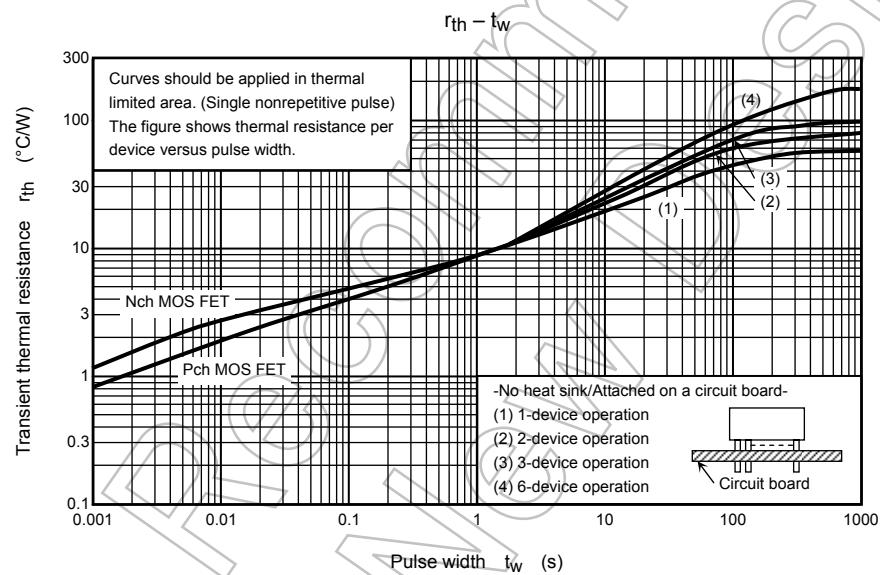
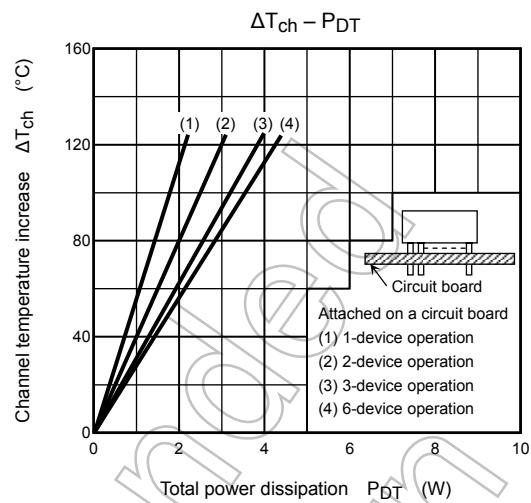
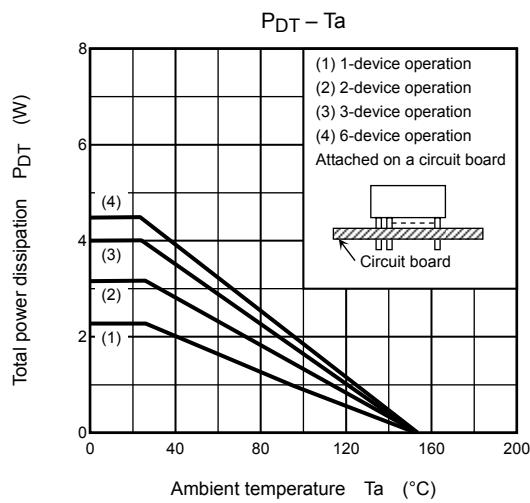


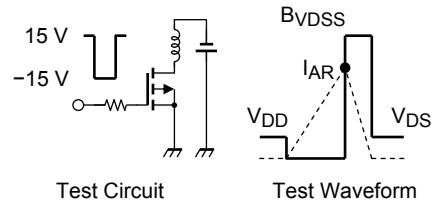
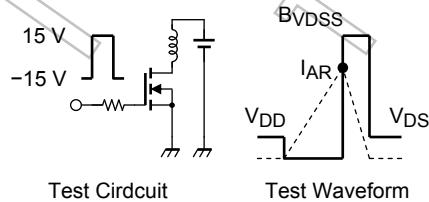
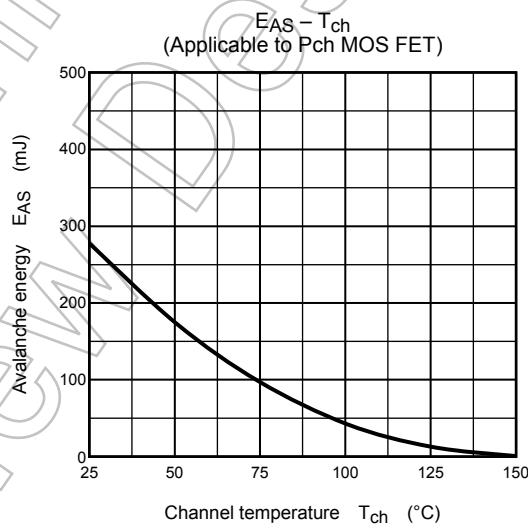
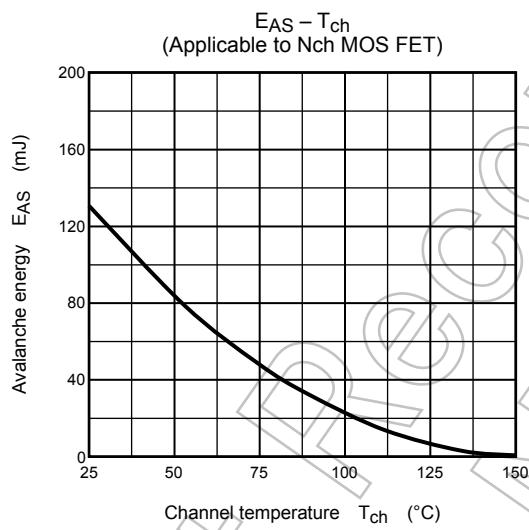
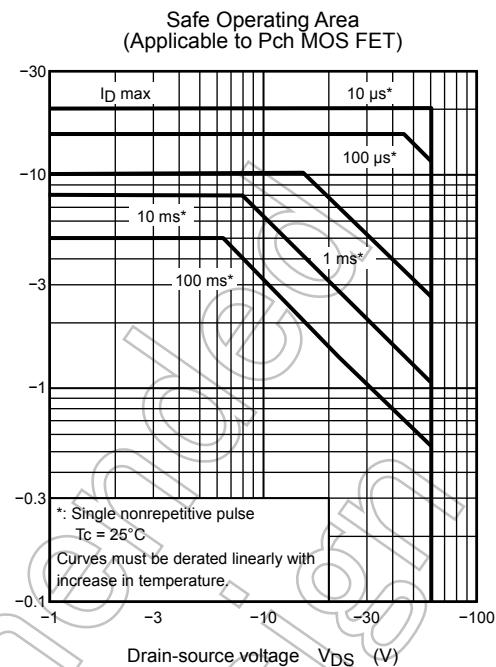
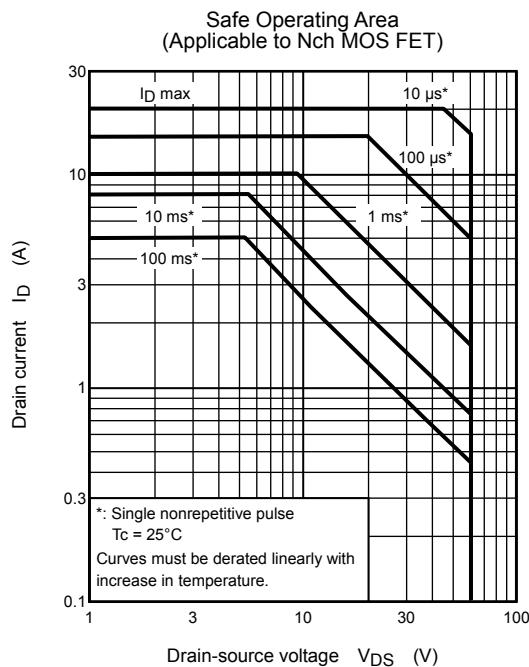
Pch MOS FET



Pch MOS FET







Peak $I_{AR} = 5 A$, $R_G = 25 \Omega$
 $V_{DD} = 25 V$, $L = 7 mH$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

Peak $I_{AR} = -5 A$, $R_G = 25 \Omega$
 $V_{DD} = -25 V$, $L = 14.84 mH$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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