CY8C20236A

# Automotive CapSense® Applications

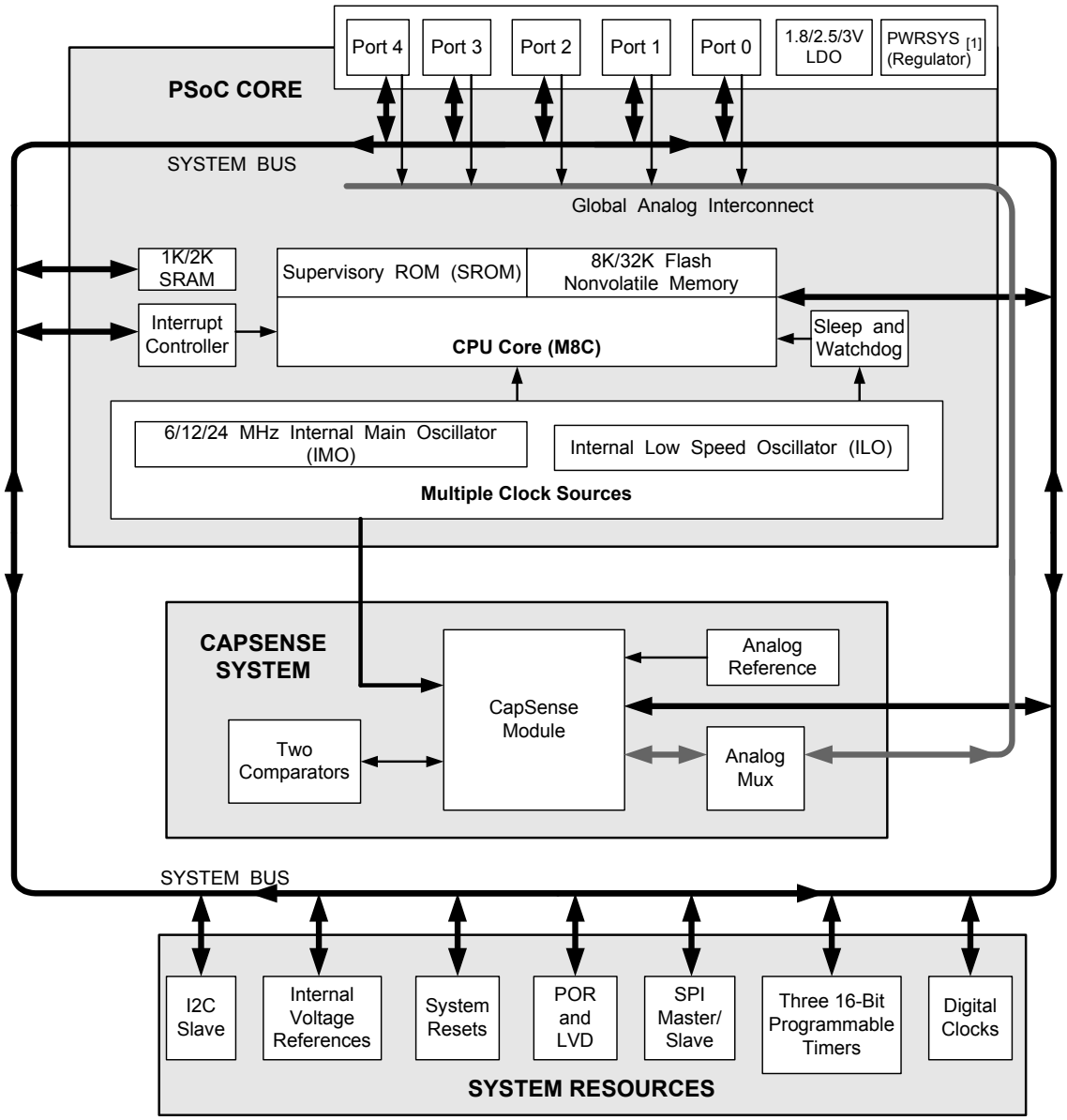
## Features

- Automotive Electronics Council (AEC) Q100 qualified
- Operating Range: 1.71 V to 5.5 V
- Low power CapSense® block
  - Configurable capacitive sensing elements
  - Supports SmartSense
  - Supports a combination of CapSense buttons, sliders, touchpads, touchscreens, and proximity sensors
- Powerful Harvard-architecture processor
  - M8C CPU speed can be up to 24 MHz or sourced by an external crystal, resonator, or clock signal
  - Low power at high speed
  - Interrupt controller
  - Temperature range: –40 °C to +85 °C
- Flexible on-chip memory
  - Two program/data storage size options:
    - CY8C20x36A: 8 KB flash/1 KB SRAM
  - 1,000 flash erase/write cycles
  - Partial flash updates
  - Flexible protection modes
  - In-system serial programming (ISSP)
- Precision, programmable clocking
  - Internal main oscillator (IMO): 6/12/24 MHz ± 5%
  - Internal low speed oscillator (ILO) at 32 kHz for watchdog and sleep timers
  - Precision 32 kHz oscillator for optional external crystal
- Programmable pin configurations
  - Up to 36 general-purpose I/Os (GPIOs) (depending on package)
  - Dual mode GPIO: All GPIOs support digital I/O and analog inputs
  - 25-mA sink current on each GPIO
    - 120 mA total sink current on all GPIOs
  - Pull-up, high Z, open-drain modes on all GPIOs
  - CMOS drive mode – 5 mA source current on ports 0 and 1 and 1 mA on ports 2, 3, and 4
    - 20 mA total source current on all GPIOs
  - Selectable, regulated digital I/O on port 1
  - Configurable input threshold on port 1
  - Hot-swap capability on all Port 1 GPIO
- Versatile analog mux
  - Common internal analog bus
  - Simultaneous connection of I/O
  - High power supply rejection ratio (PSRR) comparator
  - Low-dropout voltage regulator for all analog resources
- Additional system resources
  - $I^2C$ Slave:
    - Selectable to 50 kHz, 100 kHz, or 400 kHz
    - No clock stretching (under most conditions)
    - Implementation during sleep modes with less than 100 µA
    - Hardware address validation
  - SPI master and slave: Configurable 46.9 kHz to 12 MHz
  - Three 16-bit timers
  - Watchdog and sleep timers
  - Internal voltage reference
  - Integrated supervisory circuit
  - 8 to 10-bit incremental analog-to-digital converter (ADC)
  - Two general-purpose high speed, low power analog comparators
- Complete development tools
  - Free development tool (PSoC Designer™)
  - Full-featured, in-circuit emulator (ICE) and programmer
  - Full-speed emulation
  - Complex breakpoint structure
  - 128 KB trace memory
- Package options
  - CY8C20x36A:16-pin QFN (3 × 3 × 0.6 mm)



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## Logic Block Diagram




**Note**
1. Internal voltage regulator for internal circuitry.



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## PSoC® Functional Overview

The PSoC family consists of on-chip controller devices, which are designed to replace multiple traditional microcontroller unit (MCU)-based components with one, low cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the Logic Block Diagram on page 2, consists of three main areas:

- The Core
- CapSense Analog System

A common, versatile bus allows connection between I/O and the analog system.

Each CY8C20x36A PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 36 GPIO are also included. The GPIO provides access to the MCU and analog mux.

### PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard-architecture microprocessor.

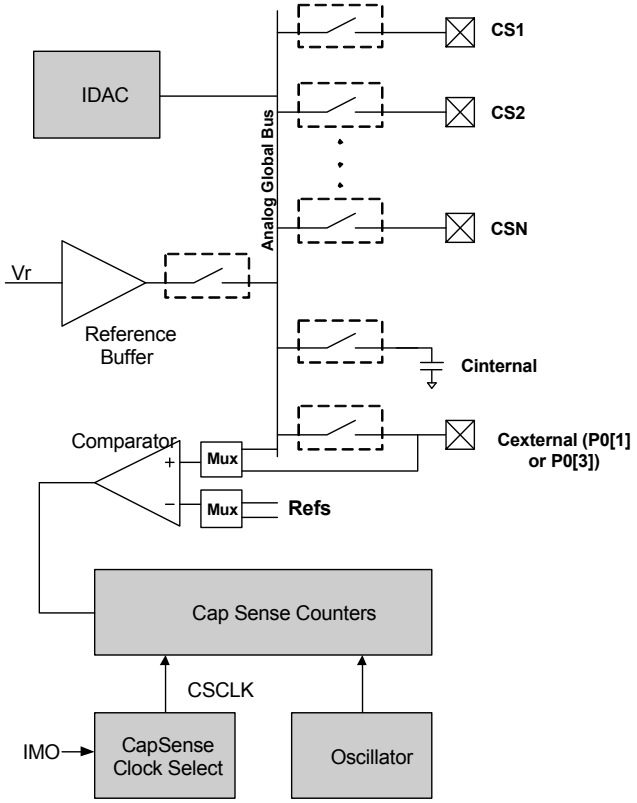
### CapSense System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. The analog system is composed of the CapSense PSoC block and an internal 1 V or 1.2 V analog reference, which together support capacitive sensing of up to 33 inputs[2]. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

*SmartSense™*

SmartSense is an innovative solution from Cypress that removes manual tuning of CapSense applications. This solution is easy to use and provides a robust noise immunity. It is the only auto-tuning solution that establishes, monitors, and maintains all required tuning parameters. SmartSense allows engineers to go from prototyping to mass production without re-tuning for manufacturing variations in PCB and/or overlay material properties.

**Figure 1. CapSense System Block Diagram**




*Analog Multiplexer System*

The Analog Mux Bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces, such as sliders and touchpads.
- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

**Note**
2. 36 GPIOs = 33 pins for capacitive sensing+2 pins for $I^2C$ + 1 pin for modulator capacitor.



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### Additional System Resources

System resources provide additional capability, such as I²C slave, SPI master, or SPI slave interfaces, three 16-bit programmable timers, and various system resets supported by the M8C.

These system resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The merits of each system resource are listed here:

- The I²C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I²C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- The I²C enhanced slave interface appears as a 32-byte RAM buffer to the external I²C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave does not stall the bus when receiving data bytes in active mode. For usage details, refer to the application note I2C Enhanced Slave Operation - AN56007.
- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on-reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

## Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the Technical Reference Manual for the CY8C20x36A PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at www.cypress.com/psoc.

### Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located at www.cypress.com/psoc. Select Application Notes under the Documentation tab.

### Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark. Refer to Development Kits on page 23.

### Training

Free PSoC and CapSense technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

### CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

### Solutions Library

Visit our growing library of solution focused designs at www.cypress.com/solutions. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

### Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, create a technical support case or call technical support at 1-800-541-4736.



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## Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select User Modules
2. Configure User Modules
3. Organize and Connect
4. Generate, Verify, and Debug

### Select Components

PSoC Designer provides a library of pre-built, pre-tested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

### Configure Components

Each of the User Modules you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more

digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the User Module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

### Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

### Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition

to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.



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## Pinouts

The CY8C20x36A PSoC device is available in a variety of packages, which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O and connection to the common analog bus. However, $V_{SS}$, $V_{DD}$, and XRES are not capable of Digital I/O.

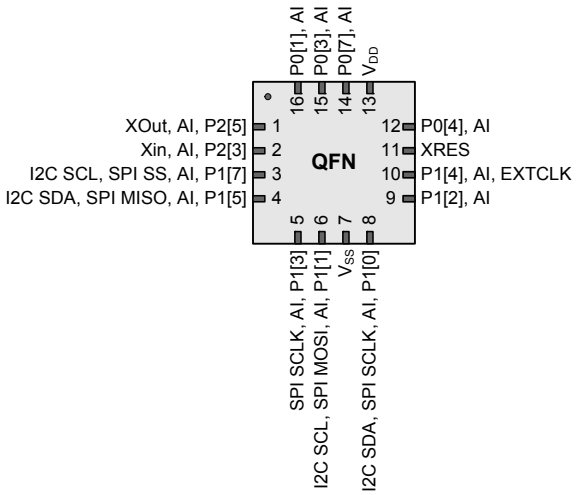
### 16-pin QFN (No E-Pad)

**Table 1. Pin Definitions – CY8C20236A PSoC Device**

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | I/O | I | P2[5] | ECO output (XOut) |
| 2 | I/O | I | P2[3] | ECO input (XIn) |
| 3 | I/OHR | I | P1[7] | $I^2C$ SCL, SPI SS |
| 4 | I/OHR | I | P1[5] | $I^2C$ SDA, SPI MISO |
| 5 | I/OHR | I | P1[3] | SPI SCLK |
| 6 | I/OHR | I | P1[1] | ISSP CLK[3], $I^2C$ SCL, SPI MOSI |
| 7 | Power | | $V_{SS}$ | Ground connection |
| 8 | I/OHR | I | P1[0] | ISSP DATA[3], $I^2C$ SDA, SPI CLK[4] |
| 9 | I/OHR | I | P1[2] | |
| 10 | I/OHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 11 | Input | | XRES | Active high external reset with internal pull-down |
| 12 | I/OH | I | P0[4] | |
| 13 | Power | | $V_{DD}$ | Supply voltage |
| 14 | I/OH | I | P0[7] | |
| 15 | I/OH | I | P0[3] | Integrating input |
| 16 | I/OH | I | P0[1] | Integrating input |

**LEGEND** A = Analog, I = Input, O = Output, H = 5 mA High Output Drive, R = Regulated Output.

**Figure 2. CY8C20236A PSoC Device**




**Notes**

3. On power-up , the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1])line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
4. Alternate SPI clock.

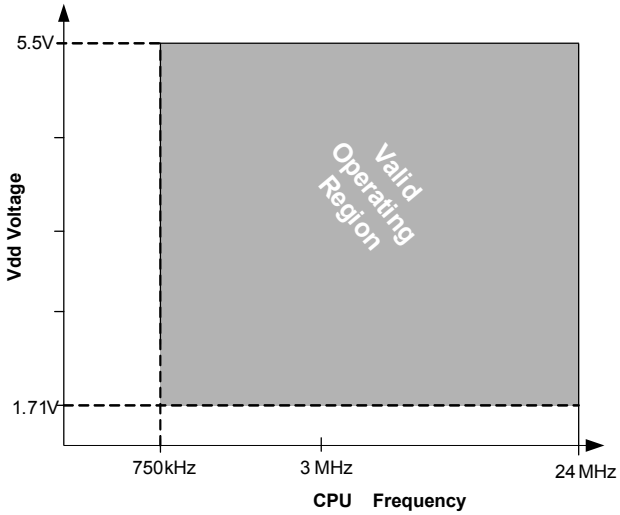


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## Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20x36A PSoC devices. For the latest electrical specifications, confirm that you have the most recent datasheet by visiting the web at http://www.cypress.com/psoc.

**Figure 3. Voltage versus CPU Frequency**




### Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

**Table 2. Absolute Maximum Ratings**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability. | –55 | +25 | +125 | °C |
| $V_{DD}$ | Supply voltage relative to $V_{SS}$ | – | –0.5 | – | +6.0 | V |
| $V_{IO}$ | DC input voltage | – | $V_{SS}$ – 0.5 | – | $V_{DD}$ + 0.5 | V |
| $V_{IOZ}$ | DC voltage applied to tristate | – | $V_{SS}$ – 0.5 | – | $V_{DD}$ + 0.5 | V |
| $I_{MIO}$ | Maximum current into any port pin | – | –25 | – | +50 | mA |
| ESD | Electro static discharge voltage | Human body model ESD | 2000 | – | – | V |
| LU | Latch-up current | In accordance with JESD78 standard | – | – | 200 | mA |

### Operating Temperature

**Table 3. Operating Temperature**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_A$ | Ambient temperature | – | –40 | – | +85 | °C |
| $T_J$ | Operational die temperature | The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 22. The user must limit the power consumption to comply with this requirement. | –40 | – | +100 | °C |



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## DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 4. DC Chip-Level Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$[5, 6, 7] | Supply voltage | Refer the table DC POR and LVD Specifications on page 14 | 1.71 | – | 5.50 | V |
| $I_{DD24}$ | Supply current, IMO = 24 MHz | Conditions are $V_{DD} \leq 3.0$ V, $T_A$ = 25 °C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current | – | 3.32 | 4.00 | mA |
| $I_{DD12}$ | Supply current, IMO = 12 MHz | Conditions are $V_{DD} \leq 3.0$ V, $T_A$ = 25 °C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current | – | 1.86 | 2.60 | mA |
| $I_{DD6}$ | Supply current, IMO = 6 MHz | Conditions are $V_{DD} \leq 3.0$ V, $T_A$ = 25 °C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current | – | 1.13 | 1.80 | mA |
| $I_{SB0}$ | Deep sleep current | $V_{DD} \leq 3.0$ V, $T_A$ = 25 °C, I/O regulator turned off | – | 0.10 | 0.50 | µA |
| $I_{SB1}$ | Standby current with POR, LVD and sleep timer | $V_{DD} \leq 3.0$ V, $T_A$ = 25 °C, I/O regulator turned off | – | 1.07 | 1.50 | µA |

**Notes**

5. When $V_{DD}$ remains in the range from 1.71 V to 1.9 V for more than 50 µsec, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 µsec to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the $SR_{POWER_UP}$ parameter.
6. If powering down in standby sleep mode, to properly detect and recover from a $V_{DD}$ brown out condition any of the following actions must be taken:
   a. Bring the device out of sleep before powering down.
   b. Assure that $V_{DD}$ falls below 100 mV before powering back up.
   c. Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
   d. Increase the buzz rate to assure that the falling edge of $V_{DD}$ is captured. The rate is configured through the PSSDC bits in the SLP_CFG register. For the referenced registers, refer to the *CY8C20x36 Technical Reference Manual*. In deep sleep mode, additional low power voltage monitoring circuitry allows $V_{DD}$ brown out conditions to be detected for edge rates slower than 1V/ms.
7. For proper CapSense block functionality, if the drop in $V_{DD}$ exceeds 5% of the base $V_{DD}$, the rate at which $V_{DD}$ drops should not exceed 200 mV/s. Base $V_{DD}$ can be between 1.8 V and 5.5 V.



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## DC GPIO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ $T_A$ ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ $T_A$ ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters apply to 5V and 3.3 V at 25 C and are for design guidance only.

**Table 5. 3.0-V to 5.5-V DC GPIO Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull-up resistor | – | 4 | 5.60 | 8 | kΩ |
| $V_{OH1}$ | High output voltage Port 2 or 3 pins | IOH ≤ 10 µA, maximum of 10 mA source current in all I/Os | $V_{DD}$ – 0.20 | – | – | V |
| $V_{OH2}$ | High output voltage Port 2 or 3 Pins | IOH = 1 mA, maximum of 20 mA source current in all I/Os | $V_{DD}$ – 0.90 | – | – | V |
| $V_{OH3}$ | High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1 | IOH < 10 µA, maximum of 10 mA source current in all I/Os | $V_{DD}$ – 0.20 | – | – | V |
| $V_{OH4}$ | High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1 | IOH = 5 mA, maximum of 20 mA source current in all I/Os | $V_{DD}$ – 0.90 | – | – | V |
| $V_{OH5}$ | High output voltage Port 1 Pins with LDO Regulator Enabled for 3 V out | IOH < 10 µA, $V_{DD}$ > 3.1 V, maximum of 4 I/Os all sourcing 5 mA | 2.85 | 3.00 | 3.30 | V |
| $V_{OH6}$ | High output voltage Port 1 pins with LDO regulator enabled for 3 V out | IOH = 5 mA, $V_{DD}$ > 3.1V, maximum of 20 mA source current in all I/Os | 2.20 | – | – | V |
| $V_{OH7}$ | High output voltage Port 1 pins with LDO enabled for 2.5 V out | IOH < 10 µA, $V_{DD}$ > 2.7 V, maximum of 20 mA source current in all I/Os | 2.35 | 2.50 | 2.75 | V |
| $V_{OH8}$ | High output voltage Port 1 pins with LDO enabled for 2.5 V out | IOH = 2 mA, $V_{DD}$ > 2.7 V, maximum of 20 mA source current in all I/Os | 1.90 | – | – | V |
| $V_{OH9}$ | High output voltage Port 1 pins with LDO enabled for 1.8 V out | IOH < 10 µA, $V_{DD}$ > 2.7 V, maximum of 20 mA source current in all I/Os | 1.60 | 1.80 | 2.10 | V |
| $V_{OH10}$ | High output voltage Port 1 pins with LDO enabled for 1.8 V out | IOH = 1 mA, $V_{DD}$ > 2.7 V, maximum of 20 mA source current in all I/Os | 1.20 | – | – | V |
| $V_{OL}$ | Low output voltage | IOL = 25 mA, $V_{DD}$ > 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]) | – | – | 0.75 | V |
| $V_{IL}$ | Input low voltage | – | – | – | 0.80 | V |
| $V_{IH}$ | Input high voltage | – | 2.00 | – | – | V |
| $V_H$ | Input hysteresis voltage | – | – | 80 | – | mV |
| $I_{IL}$ | Input leakage (Absolute Value) | – | – | 0.001 | 1 | µA |
| $C_{PIN}$ | Pin capacitance | Package and pin dependent Temp = 25 °C | 0.50 | 1.70 | 7 | pF |



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**Table 6. 2.4-V to 3.0-V DC GPIO Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull-up resistor | – | 4 | 5.60 | 8 | kΩ |
| $V_{OH1}$ | High output voltage Port 2 or 3 pins | IOH < 10 μA, maximum of 10 mA source current in all I/Os | $V_{DD}$ - 0.20 | – | – | V |
| $V_{OH2}$ | High output voltage Port 2 or 3 Pins | IOH = 0.2 mA, maximum of 10 mA source current in all I/Os | $V_{DD}$ - 0.40 | – | – | V |
| $V_{OH3}$ | High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1 | IOH < 10 μA, maximum of 10 mA source current in all I/Os | $V_{DD}$ - 0.20 | – | – | V |
| $V_{OH4}$ | High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1 | IOH = 2 mA, maximum of 10 mA source current in all I/Os | $V_{DD}$ - 0.50 | – | – | V |
| $V_{OH5A}$ | High output voltage Port 1 pins with LDO enabled for 1.8 V out | IOH < 10 μA, $V_{DD}$ > 2.4 V, maximum of 20 mA source current in all I/Os | 1.50 | 1.80 | 2.10 | V |
| $V_{OH6A}$ | High output voltage Port 1 pins with LDO enabled for 1.8 V out | IOH = 1 mA, $V_{DD}$ > 2.4 V, maximum of 20 mA source current in all I/Os | 1.20 | – | – | V |
| $V_{OL}$ | Low output voltage | IOL = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]) | – | – | 0.75 | V |
| $V_{IL}$ | Input low voltage | – | – | – | 0.72 | V |
| $V_{IH}$ | Input high voltage | – | 1.40 | – | | V |
| $V_H$ | Input hysteresis voltage | – | – | 80 | – | mV |
| $I_{IL}$ | Input leakage (absolute value) | – | – | 1 | 1000 | nA |
| $C_{PIN}$ | Capacitive load on pins | Package and pin dependent Temp = 25 °C | 0.50 | 1.70 | 7 | pF |



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**Table 7. 1.71-V to 2.4-V DC GPIO Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull-up resistor | – | 4 | 5.60 | 8 | kΩ |
| $V_{OH1}$ | High output voltage Port 2 or 3 pins | IOH = 10 µA, maximum of 10 mA source current in all I/Os | $V_{DD}$ – 0.20 | – | – | V |
| $V_{OH2}$ | High output voltage Port 2 or 3 pins | IOH = 0.5 mA, maximum of 10 mA source current in all I/Os | $V_{DD}$ – 0.50 | – | – | V |
| $V_{OH3}$ | High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1 | IOH = 100 µA, maximum of 10 mA source current in all I/Os | $V_{DD}$ – 0.20 | – | – | V |
| $V_{OH4}$ | High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1 | IOH = 2 mA, maximum of 10 mA source current in all I/Os | $V_{DD}$ – 0.50 | – | – | V |
| $V_{OL}$ | Low output voltage | IOL = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]) | – | – | 0.40 | V |
| $V_{IL}$ | Input low voltage | – | – | – | 0.30 × $V_{DD}$ | V |
| $V_{IH}$ | Input high voltage | – | 0.65 × $V_{DD}$ | – | – | V |
| $V_H$ | Input hysteresis voltage | – | – | 80 | – | mV |
| $I_{IL}$ | Input leakage (absolute value) | – | – | 1 | 1000 | nA |
| $C_{PIN}$ | Capacitive load on pins | Package and pin dependent temp = 25 °C | 0.50 | 1.70 | 7 | pF |

## DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 8. DC Analog Mux Bus Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{SW}$ | Switch resistance to common analog bus | – | – | – | 800 | Ω |
| $R_{GND}$ | Resistance of initialization switch to $V_{SS}$ | – | – | – | 800 | Ω |

The maximum pin voltage for measuring $R_{SW}$ and $R_{GND}$ is 1.8 V

## DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 9. DC Comparator Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{LPC}$ | Low power comparator (LPC) common mode | Maximum voltage limited to $V_{DD}$ | 0.0 | – | 1.8 | V |
| $I_{LPC}$ | LPC supply current | – | – | 10 | 40 | µA |
| $V_{OSLPC}$ | LPC voltage offset | – | – | 2.5 | 30 | mV |



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## Comparator User Module Electrical Specifications

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: –40°C ≤ TA ≤ 85°C, 1.71V ≤ $V_{DD}$ ≤ 5.5V.

**Table 10. Comparator User Module Electrical Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{COMP}$ | Comparator response time | 50 mV overdrive | – | 70 | 100 | ns |
| Offset | | Valid from 0.2 V to $V_{DD}$ – 0.2 V | – | 2.5 | 30 | mV |
| Current | | Average DC current, 50 mV overdrive | – | 20 | 80 | µA |
| PSRR | Supply voltage > 2 V | Power supply rejection ratio | – | 80 | – | dB |
| | Supply voltage < 2 V | Power supply rejection ratio | – | 40 | – | dB |
| Input range | | – | 0 | | 1.5 | V |

## ADC Electrical Specifications

**Table 11. ADC User Module Electrical Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Input** | | | | | | |
| $V_{IN}$ | Input voltage range | – | 0 | – | VREFADC | V |
| $C_{IIN}$ | Input capacitance | – | – | – | 5 | pF |
| $R_{IN}$ | Input resistance | Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution | 1/(500fF × data clock) | 1/(400fF × data clock) | 1/(300fF × data clock) | Ω |
| **Reference** | | | | | | |
| $V_{REFADC}$ | ADC reference voltage | – | 1.14 | – | 1.26 | V |
| **Conversion Rate** | | | | | | |
| $F_{CLK}$ | Data clock | Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy | 2.25 | – | 6 | MHz |
| S8 | 8-bit sample rate | Data clock set to 6 MHz. sample rate = 0.001/ (2^Resolution/Data Clock) | – | 23.43 | – | ksps |
| S10 | 10-bit sample rate | Data clock set to 6 MHz. sample rate = 0.001/ (2^resolution/data clock) | – | 5.85 | – | ksps |
| **DC Accuracy** | | | | | | |
| RES | Resolution | Can be set to 8-, 9-, or 10-bit | 8 | – | 10 | bits |
| DNL | Differential nonlinearity | – | –1 | – | +2 | LSB |
| INL | Integral nonlinearity | – | –2 | – | +2 | LSB |
| $E_{OFFSET}$ | Offset error | 8-bit resolution | 0 | 3.20 | 19.20 | LSB |
| | | 10-bit resolution | 0 | 12.80 | 76.80 | LSB |
| $E_{GAIN}$ | Gain error | For any resolution | –5 | – | +5 | %FSR |
| **Power** | | | | | | |
| $I_{ADC}$ | Operating current | – | – | 2.10 | 2.60 | mA |
| PSRR | Power supply rejection ratio | PSRR ($V_{DD}$ > 3.0 V) | – | 24 | – | dB |
| | | PSRR ($V_{DD}$ < 3.0 V) | – | 30 | – | dB |



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## DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 12. DC POR and LVD Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{POR0}$ | 1.66 V selected in PSoC Designer | $V_{DD}$ must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog. | 1.61 | 1.66 | 1.71 | V |
| $V_{POR1}$ | 2.36 V selected in PSoC Designer | | – | 2.36 | 2.41 | |
| $V_{POR2}$ | 2.60 V selected in PSoC Designer | | – | 2.60 | 2.66 | |
| $V_{POR3}$ | 2.82 V selected in PSoC Designer | | – | 2.82 | 2.95 | |
| $V_{LVD0}$ | 2.45 V selected in PSoC Designer | – | 2.40 | 2.45 | 2.51 | V |
| $V_{LVD1}$ | 2.71 V selected in PSoC Designer | | 2.64[8] | 2.71 | 2.78 | |
| $V_{LVD2}$ | 2.92 V selected in PSoC Designer | | 2.85[9] | 2.92 | 2.99 | |
| $V_{LVD3}$ | 3.02 V selected in PSoC Designer | | 2.95[10] | 3.02 | 3.09 | |
| $V_{LVD4}$ | 3.13 V selected in PSoC Designer | | 3.06 | 3.13 | 3.20 | |
| $V_{LVD5}$ | 1.90 V selected in PSoC Designer | | 1.84 | 1.90 | 2.32 | |
| $V_{LVD6}$ | 1.80 V selected in PSoC Designer | | 1.75[11] | 1.80 | 1.84 | |
| $V_{LVD7}$ | 4.73 V selected in PSoC Designer | | 4.62 | 4.73 | 4.83 | |

## DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 13. DC Programming Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{DDIWRITE}$ | Supply voltage for flash write operations | – | 1.71 | – | 5.25 | V |
| $I_{DDP}$ | Supply current during programming or verify | – | – | 5 | 25 | mA |
| $V_{ILP}$ | Input low voltage during programming or verify | See the appropriate DC GPIO Specifications on page 10 | – | – | $V_{IL}$ | V |
| $V_{IHP}$ | Input high voltage during programming or verify | See appropriate DC GPIO Specifications on page 10 table on pages 15 or 16 | $V_{IH}$ | – | – | V |
| $I_{ILP}$ | Input current when Applying $V_{ILP}$ to P1[0] or P1[1] during programming or verify | Driving internal pull-down resistor | – | – | 0.2 | mA |
| $I_{IHP}$ | Input current when applying $V_{IHP}$ to P1[0] or P1[1] during programming or verify | Driving internal pull-down resistor | – | – | 1.5 | mA |
| $V_{OLP}$ | Output low voltage during programming or verify | | – | – | $V_{SS}$ + 0.75 | V |
| $V_{OHP}$ | Output high voltage during programming or verify | See appropriate DC GPIO Specifications on page 10 table on page 16. For $V_{DD}$ > 3V use $V_{OH4}$ in Table 3 on page 8. | $V_{OH}$ | – | $V_{DD}$ | V |
| $Flash_{ENPB}$ | Flash write endurance | Erase/write cycles per block | 50,000 | – | – | – |
| $Flash_{DR}$ | Flash data retention | Following maximum Flash write cycles; ambient temperature of 55 °C | 20 | – | – | Years |

**Notes**
8. Always greater than 50 mV above $V_{PPOR1}$ voltage for falling supply.
9. Always greater than 50 mV above $V_{PPOR2}$ voltage for falling supply.
10. Always greater than 50 mV above $V_{PPOR3}$ voltage for falling supply.
11. Always greater than 50 mV above $V_{PPOR0}$ voltage for falling supply.



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## AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 14. AC Chip-Level Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{IMO24}$ | Internal main oscillator frequency at 24 MHz Setting | – | 22.8 | 24 | 25.2 | MHz |
| $F_{IMO12}$ | Internal main oscillator frequency at 12 MHz setting | – | 11.4 | 12 | 12.6 | MHz |
| $F_{IMO6}$ | Internal main oscillator frequency at 6 MHz setting | – | 5.7 | 6.0 | 6.3 | MHz |
| $F_{CPU}$ | CPU frequency | – | 0.75 | – | 25.20 | MHz |
| $F_{32K1}$ | Internal low speed oscillator frequency | – | 19 | 32 | 50 | kHz |
| $F_{32K_U}$ | Internal low speed oscillator (ILO) untrimmed frequency) | – | 13 | 32 | 82 | kHz |
| $DC_{IMO}$ | Duty cycle of IMO | – | 40 | 50 | 60 | % |
| $DC_{ILO}$ | Internal low speed oscillator duty cycle | – | 40 | 50 | 60 | % |
| $SR_{POWER_UP}$ | Power supply slew rate | $V_{DD}$ slew rate during power-up | – | – | 250 | V/ms |
| $t_{XRST}$ | External reset pulse width at power-up | After supply voltage is valid | 1 | – | – | ms |
| $t_{XRST2}$ | External reset pulse width after power-up[12] | Applies after part has booted | 10 | – | – | µs |

**Note**

12. The minimum required XRES pulse length is longer when programming the device (see Table 18 on page 17).



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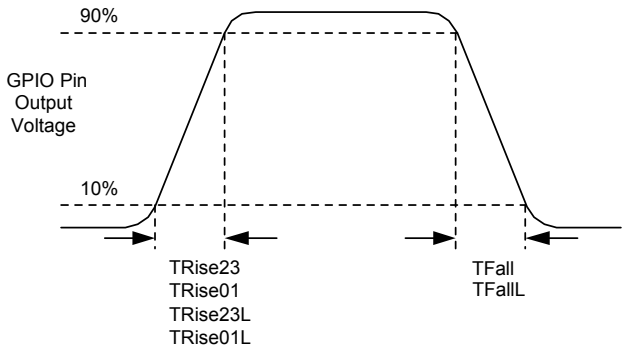
## AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 15. AC GPIO Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GPIO}$ | GPIO operating frequency | Normal strong mode Port 0, 1 | 0<br>0 | –<br>– | 6 MHz for 1.71 V <$V_{DD}$ < 2.40 V<br>12 MHz for 2.40 V < $V_{DD}$< 5.50 V | MHz<br>MHz |
| $t_{RISE23}$ | Rise time, strong mode, Cload = 50 pF Ports 2 or 3 | $V_{DD}$ = 3.0 to 3.6 V, 10% to 90% | 15 | – | 80 | ns |
| $t_{RISE23L}$ | Rise time, strong mode low supply, Cload = 50 pF, Ports 2 or 3 | $V_{DD}$ = 1.71 to 3.0 V, 10% to 90% | 15 | – | 80 | ns |
| $t_{RISE01}$ | Rise time, strong mode, Cload = 50 pF Ports 0 or 1 | $V_{DD}$ = 3.0 to 3.6 V, 10% to 90% LDO enabled or disabled | 10 | – | 50 | ns |
| $t_{RISE01L}$ | Rise time, strong mode low supply, Cload = 50 pF, Ports 0 or 1 | $V_{DD}$ = 1.71 to 3.0 V, 10% to 90% LDO enabled or disabled | 10 | – | 80 | ns |
| $t_{FALL}$ | Fall time, strong mode, Cload = 50 pF all ports | $V_{DD}$ = 3.0 to 3.6 V, 10% to 90% | 10 | – | 50 | ns |
| $t_{FALLL}$ | Fall time, strong mode low supply, Cload = 50 pF, all ports | $V_{DD}$ = 1.71 to 3.0 V, 10% to 90% | 10 | – | 70 | ns |

**Figure 4. GPIO Timing Diagram**




## AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 16. AC Low Power Comparator Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{LPC}$ | Comparator response time, 50 mV overdrive | 50 mV overdrive does not include offset voltage. | – | – | 100 | ns |

## AC External Clock Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 17. AC External Clock Specifications**

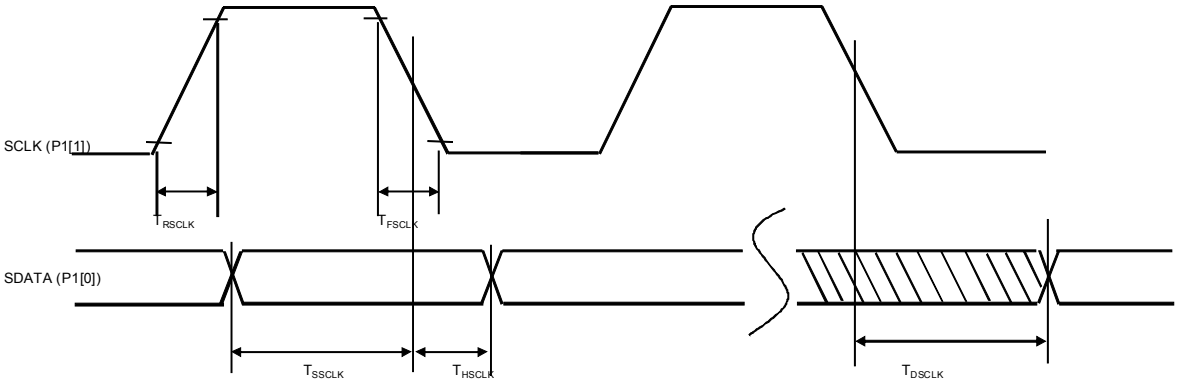
| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{OSCEXT}$ | Frequency (external oscillator frequency) | – | 0.75 | – | 25.20 | MHz |
| | High period | – | 20.60 | – | 5300 | ns |
| | Low period | – | 20.60 | – | – | ns |
| | Power-up IMO to switch | – | 150 | – | – | µs |



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## AC Programming Specifications

**Figure 5. AC Waveform**




The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 18. AC Programming Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{RSCLK}$ | Rise time of SCLK | – | 1 | – | 20 | ns |
| $t_{FSCLK}$ | Fall time of SCLK | – | 1 | – | 20 | ns |
| $t_{SSCLK}$ | Data setup time to falling edge of SCLK | – | 40 | – | – | ns |
| $t_{HSCLK}$ | Data hold time from falling edge of SCLK | – | 40 | – | – | ns |
| $F_{SCLK}$ | Frequency of SCLK | – | 0 | – | 8 | MHz |
| $t_{ERASEB}$ | Flash erase time (block) | – | – | – | 18 | ms |
| $t_{WRITE}$ | Flash block write time | – | – | – | 25 | ms |
| $t_{DSCLK}$ | Data out delay from falling edge of SCLK | $3.6 < V_{DD}$ | – | – | 60 | ns |
| $t_{DSCLK3}$ | Data out delay from falling edge of SCLK | $3.0 \le V_{DD} \le 3.6$ | – | – | 85 | ns |
| $t_{DSCLK2}$ | Data out delay from falling edge of SCLK | $1.71 \le V_{DD} \le 3.0$ | – | – | 130 | ns |
| $t_{XRST3}$ | External reset pulse width after power-up | Required to enter programming mode when coming out of sleep | 300 | – | – | µs |
| $t_{XRES}$ | XRES pulse length | – | 300 | – | – | µs |
| $t_{VDDWAIT}$ | $V_{DD}$ stable to wait-and-poll hold off | – | 0.1 | – | 1 | ms |
| $t_{VDDXRES}$ | $V_{DD}$ stable to XRES assertion delay | – | 14.27 | – | – | ms |
| $t_{POLL}$ | SDATA high pulse time | – | 0.01 | – | 200 | ms |
| $t_{ACQ}$ | “Key window” time after a $V_{DD}$ ramp acquire event, based on 256 ILO clocks. | – | 3.20 | – | 19.60 | ms |
| $t_{XRESINI}$ | “Key window” time after an XRES event, based on 8 ILO clocks | – | 98 | – | 615 | µs |



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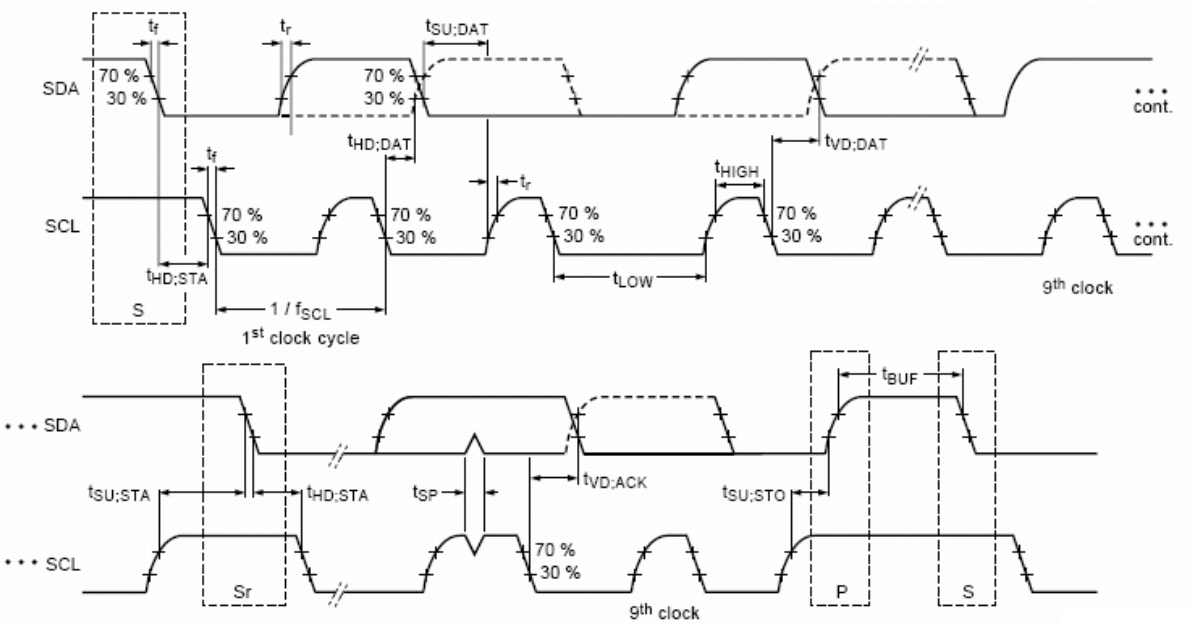
## AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 19. AC Characteristics of the I²C SDA and SCL Pins**

| Symbol | Description | Standard Mode | | Fast Mode | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $f_{SCL}$ | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{HD;STA}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated | 4.0 | – | 0.6 | – | µs |
| $t_{LOW}$ | LOW period of the SCL clock | 4.7 | – | 1.3 | – | µs |
| $t_{HIGH}$ | HIGH Period of the SCL clock | 4.0 | – | 0.6 | – | µs |
| $t_{SU;STA}$ | Setup time for a repeated START condition | 4.7 | – | 0.6 | – | µs |
| $t_{HD;DAT}$ | Data hold time | 0 | 3.45 | 0 | 0.90 | µs |
| $t_{SU;DAT}$ | Data setup time | 250 | – | 100[13] | – | ns |
| $t_{SU;STO}$ | Setup time for STOP condition | 4.0 | – | 0.6 | – | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 4.7 | – | 1.3 | – | µs |
| $t_{SP}$ | Pulse width of spikes are suppressed by the input filter | – | – | 0 | 50 | ns |

**Figure 6. Definition for Timing for Fast/Standard Mode on the I²C Bus**




**Note**

13. A Fast-Mode I²C-bus device can be used in a standard mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.



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**Table 20. SPI Master AC Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{SCLK}$ | SCLK clock frequency | $V_{DD} \geq 2.4$ V<br>$V_{DD} < 2.4$ V | –<br>– | –<br>– | 6<br>3 | MHz<br>MHz |
| DC | SCLK duty cycle | – | – | 50 | – | % |
| $t_{SETUP}$ | MISO to SCLK setup time | $V_{DD} \geq 2.4$ V<br>$V_{DD} < 2.4$ V | 60<br>100 | –<br>– | –<br>– | ns<br>ns |
| $t_{HOLD}$ | SCLK to MISO hold time | – | 40 | – | – | ns |
| $t_{OUT_VAL}$ | SCLK to MOSI valid time | – | – | – | 40 | ns |
| $t_{OUT_HIGH}$ | MOSI high time | – | 40 | – | – | ns |

**Figure 7. SPI Master Mode 0 and 2**

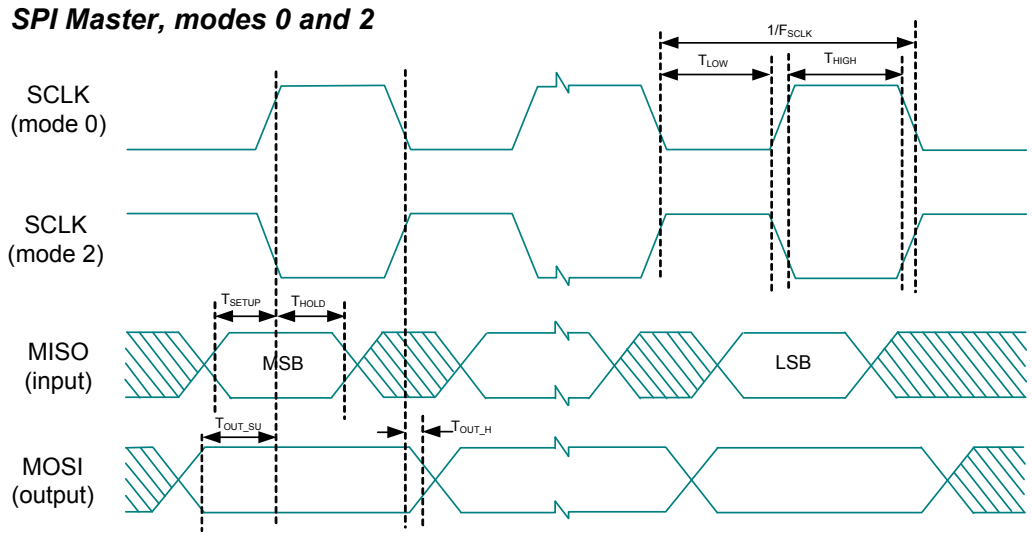
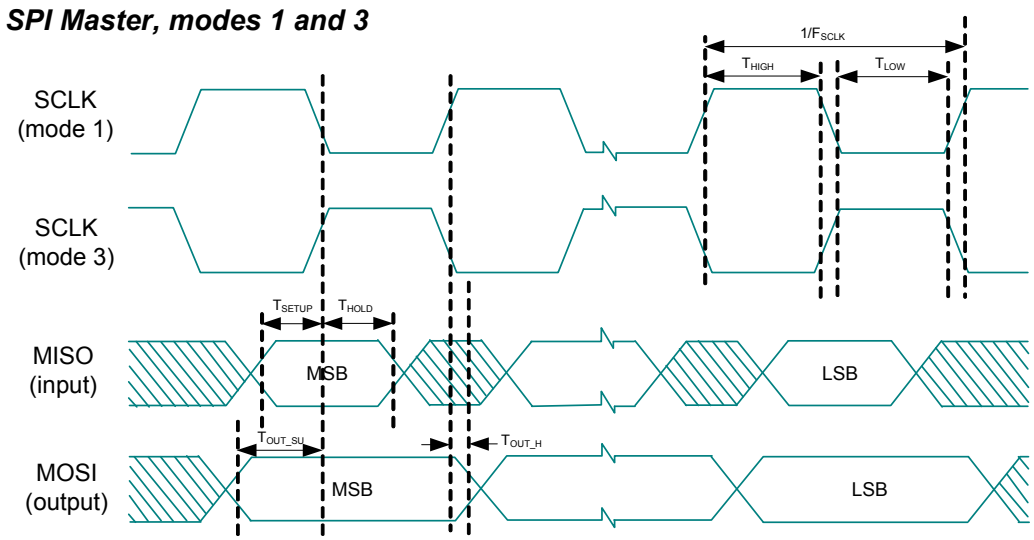



**Figure 8. SPI Master Mode 1 and 3**






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**Table 21. SPI Slave AC Specifications**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{SCLK}$ | SCLK clock frequency | $V_{DD} \geq 2.4$ V<br>$V_{DD} < 2.4$ V | –<br>– | –<br>– | 12<br>6 | MHz<br>MHz |
| $t_{LOW}$ | SCLK low time | – | 42 | – | – | ns |
| $t_{HIGH}$ | SCLK high time | – | 42 | – | – | ns |
| $t_{SETUP}$ | MOSI to SCLK setup time | – | 30 | – | – | ns |
| $t_{HOLD}$ | SCLK to MOSI hold time | – | 50 | – | – | ns |
| $t_{SS_MISO}$ | SS high to MISO valid | – | – | – | 153 | ns |
| $t_{SCLK_MISO}$ | SCLK to MISO valid | – | – | – | 125 | ns |
| $t_{SS_HIGH}$ | SS high time | – | 50 | – | – | ns |
| $t_{SS_CLK}$ | Time from SS low to first SCLK | – | 2/SCLK | – | – | ns |
| $t_{CLK_SS}$ | Time from last SCLK to SS high | – | 2/SCLK | – | – | ns |

**Figure 9. SPI Slave Mode 0 and 2**

***SPI Slave, modes 0 and 2***

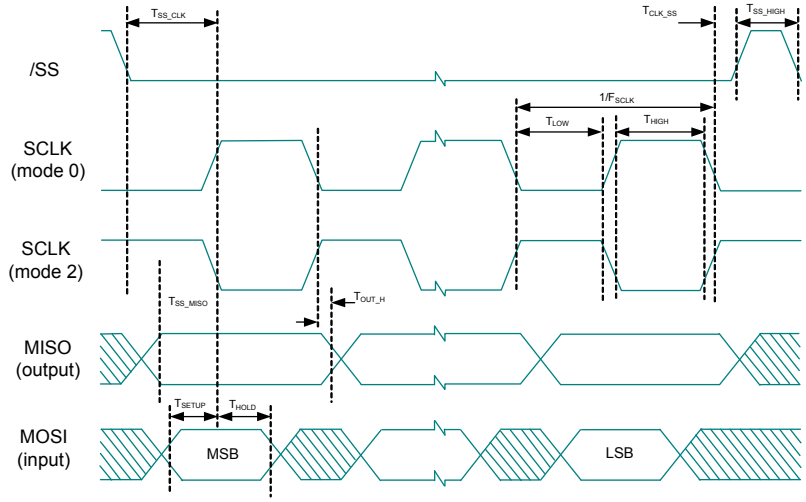
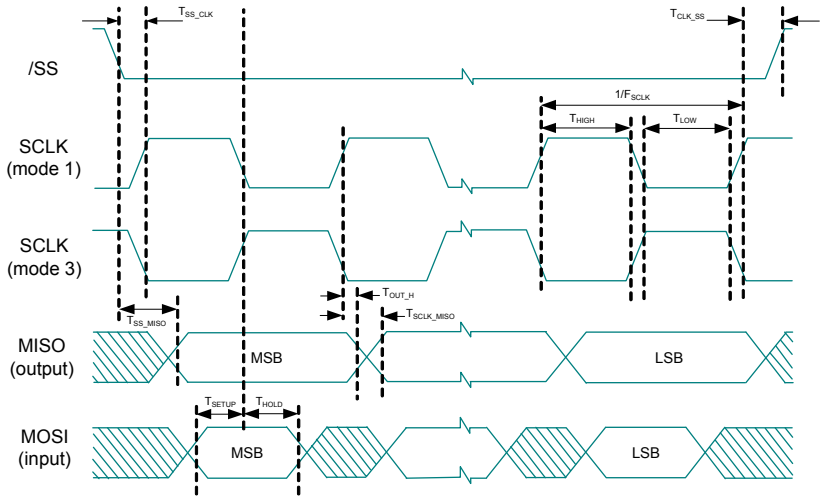



**Figure 10. SPI Slave Mode 1 and 3**

***SPI Slave, modes 1 and 3***





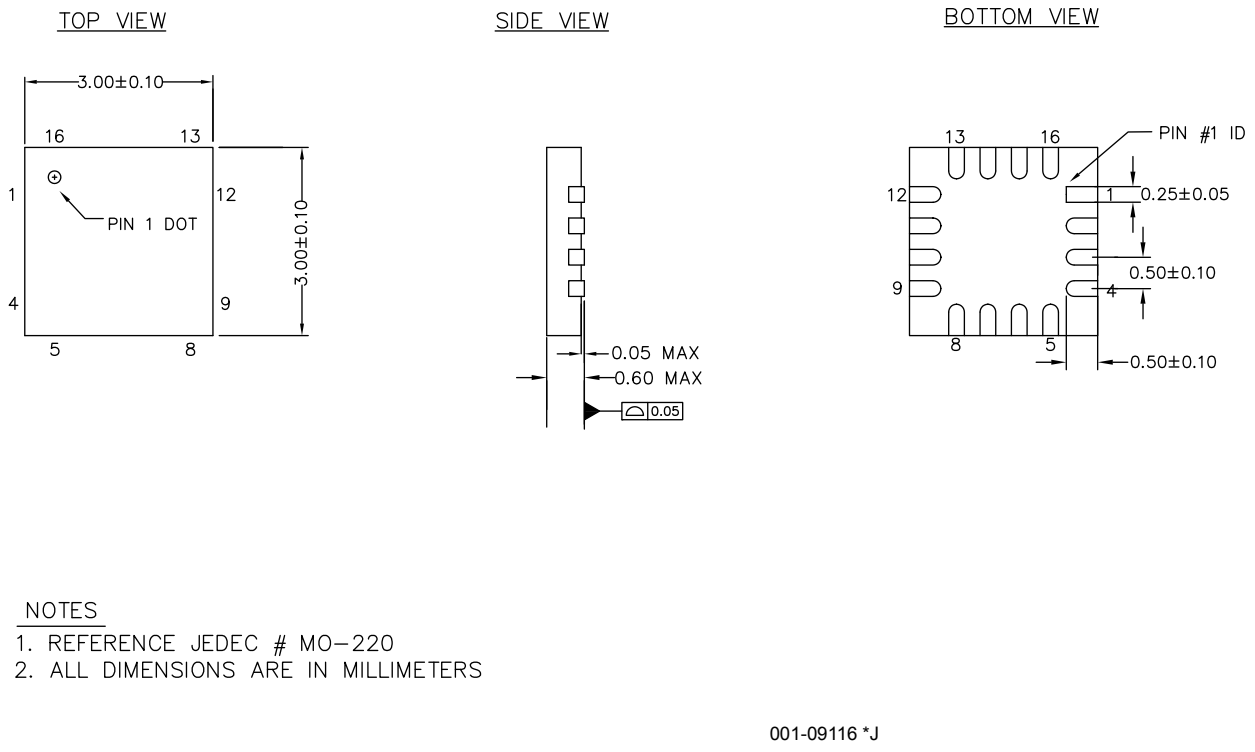

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## Packaging Information

This section illustrates the packaging specifications for the CY8C20x36A PSoC device, along with the thermal impedances for each package.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

**Figure 11. 16-pin QFN (3 × 3 × 0.6 mm) LG16A/LD16A (Sawn) Package Outline, 001-09116**




NOTES
1. REFERENCE JEDEC # MO−220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 *J

**Important Note** For information on the preferred dimensions for mounting QFN packages, refer to Application Note, Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages available at http://www.amkor.com.



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## Thermal Impedances

**Table 22. Thermal Impedances per Package**

| Package | Typical $\theta_{JA}$ [14] |
|---|---|
| 16-pin QFN | 33 °C/W |

## Solder Reflow Specifications

Table 23 shows the solder reflow temperature limits that must not be exceeded.

**Table 23. Solder Reflow Specifications**

| Package | Maximum Peak Temperature ($T_C$) | Maximum Time above $T_C$ – 5 °C |
|---|---|---|
| 16-pin QFN | 260 °C | 30 seconds |

**Note**
14. $T_J = T_A + \text{Power} \times \theta_{JA}$.



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## Development Tool Selection

### Software

*PSoC Designer*

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for years. PSoC Designer is available free of charge at http://www.cypress.com. PSoC Designer comes with a free C compiler.

**PSoC Designer Software Subsystems**

You choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. You configure the user modules for your chosen application and connect them to each other and to the proper pins. Then you generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time. Code Generation Tools PSoC Designer supports multiple third-party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

**Assemblers.** The assemblers allow assembly code to be merged seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

**C Language Compilers.** C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

*Debugger*

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear break-points, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

*In-Circuit Emulator*

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices. The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24MHz) operation.

Standard Cypress PSoC IDE tools are available for debugging the CY8C20x36A family of parts. However, the additional trace length and a minimal ground plane in the Flex-Pod can create noise problems that make it difficult to debug the design. A custom bonded On-Chip Debug (OCD) device is available in a 48-pin QFN package. The OCD device is recommended for debugging designs that have high current and/or high analog accuracy requirements. The QFN package is compact and is connected to the ICE through a high density connector.

*PSoC Programmer*

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube in-circuit emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com/psocprogrammer.

### Development Kits

All development kits are sold at the Cypress Online Store.

*CY3215-DK Basic Development Kit*

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66A Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466A-24PXI 28-PDIP Chip Samples



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## Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

*CY3210-MiniProg1*

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466A-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443A-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

*CY3210-PSoCEval1*

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466A-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

*CY3280-20x66 Universal CapSense Controller*

The CY3280-20X66 CapSense Controller Kit is designed for easy prototyping and debug of CY8C20xx6A CapSense Family designs with pre-defined control circuitry and plug-in hardware. Programming hardware and an I2C-to-USB bridge are included for tuning and data acquisition.

The kit includes:

- CY3280-20x66 CapSense Controller Board
- CY3240-I2USB Bridge
- CY3210 MiniProg1 Programmer
- USB 2.0 Retractable Cable
- CY3280-20x66 Kit CD

### Device Programmers

All device programmers are purchased from the Cypress Online Store.

*CY3207ISSP In-System Serial Programmer (ISSP)*

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment.
Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

### Accessories (Emulation and Programming)

**Table 24. Emulation and Programming Accessories**

| Part Number | Pin Package | Flex-Pod Kit[15] | Foot Kit[16] | Adapter[17] |
|---|---|---|---|---|
| CY8C20236A-24LKXA | 16-pin QFN | CY3250-20246QFN | CY3250-16QFN-FK | – |

**Notes**
15. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
16. Foot kit includes surface mount feet that can be soldered to the target PCB.
17. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.



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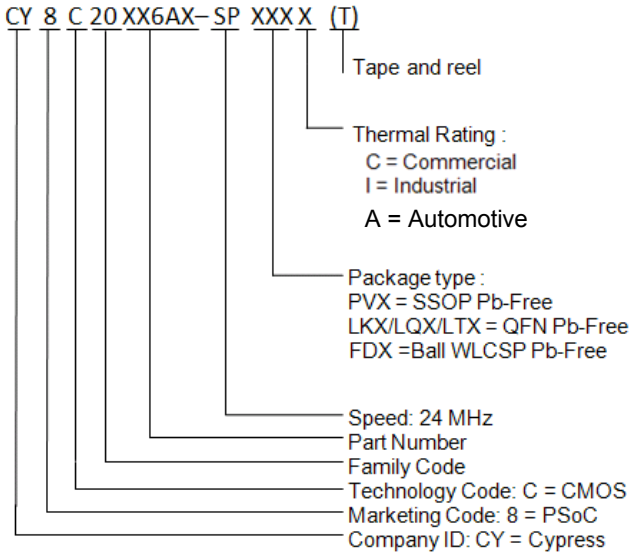
## Ordering Information

The following table lists the CY8C20x36A PSoC devices' key package features and ordering codes..

**Table 25. PSoC Device Key Features and Ordering Information**

| Package | Ordering Code | Flash (Bytes) | SRAM (Bytes) | CapSense Blocks | Digital I/O Pins | Analog Inputs[18] | XRES Pin | ADC |
|---|---|---|---|---|---|---|---|---|
| 16-Pin (3 × 3 × 0.6 mm) QFN | CY8C20236A-24LKXA | 8K | 1K | 1 | 13 | 13 | Yes | Yes |
| 16-Pin (3 × 3 × 0.6 mm) QFN (Tape and Reel) | CY8C20236A-24LKXAT | 8K | 1K | 1 | 13 | 13 | Yes | Yes |

### Ordering Code Definitions




**Note**
18. Dual-function Digital I/O Pins also connect to the common analog mux.



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## Acronyms

The following table lists the acronyms that are used in this document.

**Table 26. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| AC | alternating current |
| ADC | analog-to-digital converter |
| API | application programming interface |
| CMOS | complementary metal oxide semiconductor |
| CPU | central processing unit |
| DAC | digital-to-analog converter |
| DC | direct current |
| EOP | end of packet |
| FSR | full scale range |
| GPIO | general purpose input/output |
| GUI | graphical user interface |
| $I^2C$ | inter-integrated circuit |
| ICE | in-circuit emulator |
| IDAC | digital analog converter current |
| ILO | internal low speed oscillator |
| IMO | internal main oscillator |
| I/O | input/output |
| ISSP | in-system serial programming |
| LCD | liquid crystal display |
| LDO | low dropout (regulator) |
| LSB | least-significant bit |
| LVD | low voltage detect |
| MCU | micro-controller unit |
| MIPS | mega instructions per second |
| MISO | master in slave out |
| MOSI | master out slave in |
| MSB | most-significant bit |
| OCD | on-chip debugger |
| POR | power on reset |
| PPOR | precision power on reset |
| PSRR | power supply rejection ratio |
| PWRSYS | power system |
| PSoC® | Programmable System-on-Chip |
| SLIMO | slow internal main oscillator |
| SRAM | static random access memory |
| SNR | signal to noise ratio |
| QFN | quad flat no-lead |
| SCL | serial I2C clock |
| SDA | serial I2C data |
| SDATA | serial ISSP data |
| SPI | serial peripheral interface |
| SS | slave select |
| SSOP | shrink small outline package |
| TC | test controller |
| USB | universal serial bus |
| WLCSP | wafer level chip scale package |
| XTAL | crystal |

## Reference Documents

- *Technical reference manual for CY8C20xx6 devices*
- *In-system Serial Programming (ISSP) protocol for 20xx6* (AN2026C)
- *Host Sourced Serial Programming for 20xx6 devices* (AN59389)

## Document Conventions

### Units of Measure

Table 27 lists all the abbreviations used to measure the PSoC devices.

**Table 27. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| dB | decibels |
| fF | femto farad |
| g | gram |
| Hz | hertz |
| KB | 1024 bytes |
| Kbit | 1024 bits |
| KHz | kilohertz |
| Ksps | kilo samples per second |
| kΩ | kilohm |
| MHz | megahertz |
| MΩ | megaohm |
| µA | microampere |
| µF | microfarad |
| µH | microhenry |
| µs | microsecond |
| µW | microwatts |
| mA | milli-ampere |
| ms | milli-second |
| mV | milli-volts |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolts |
| W | ohm |
| pA | picoampere |
| pF | picofarad |
| pp | peak-to-peak |
| ppm | parts per million |
| ps | picosecond |
| sps | samples per second |
| s | sigma: one standard deviation |
| V | volts |
| W | watt |



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### Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimal.

## Glossary

| | |
|---|---|
| Crosspoint connection | Connection between any GPIO combination via analog multiplexer bus. |
| Differential non-linearity | Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step. |
| Hold time | Hold time is the time following a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct. |
| $I^2C$ | It is a serial multi-master bus used to connect low speed peripherals to MCU. |
| Integral nonlinearity | It is a term describing the maximum deviation between the ideal output of a DAC/ADC and the actual output level. |
| Latch-up current | Current at which the latch-up test is conducted according to JESD78 standard (at 125 degree celsius) |
| Power supply rejection ratio (PSRR) | The PSRR is defined as the ratio of the change in supply voltage to the corresponding change in output voltage of the device. |
| Scan | The conversion of all sensor capacitances to digital values. |
| Setup time | Period required to prepare a device, machine, process, or system for it to be ready to function. |
| Signal-to-noise ratio | The ratio between a capacitive finger signal and system noise. |
| SPI | Serial peripheral interface is a synchronous serial data link standard. |



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## Document History Page

| Document Title: CY8C20236A, Automotive CapSense® Applications<br>Document Number: 001-63115 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Origin of Change** | **Submission Date** | **Description of Change** |
| ** | 2989484 | BTK | 07/21/10 | New data sheet. |
| *A | 3262255 | BTK | 05/19/11 | Changed status from Advance to Preliminary.<br>Added preliminary information to data sheet. |
| *B | 3311559 | BTK | 07/13/11 | Changed status from Preliminary to Final.<br>Removed “Capacitance on Crystal Pins” section. |
| *C | 4478256 | KUK | 08/19/2014 | Updated Document Title as “CY8C20236A, Automotive CapSense® Applications”.<br>Removed CY8C20566A related information in all instances across the document.<br>Removed 48-pin SSOP package related information in all instances across the document.<br>Updated PSoC® Functional Overview:<br>Updated description.<br>Updated Electrical Specifications:<br>Updated DC Chip-Level Specifications:<br>Updated Table 4:<br>Removed the Note “For USB mode, the $V_{DD}$ supply for bus-powered application should be limited to 4.35 V–5.35 V. For self-powered application, $V_{DD}$ should be 3.15 V–3.45 V.” and its reference in $V_{DD}$ parameter.<br>Updated Packaging Information:<br>spec 001-09116 – Changed revision from *E to *J.<br>Removed spec 51-85061 *D<br>Updated Ordering Information:<br>Updated part numbers.<br>Removed the column “USB”.<br>Updated to new template.<br>Completing Sunset Review. |
| *D | 5873117 | SNPR | 09/05/2017 | Updated to new template.<br>Completing Sunset Review. |



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