Output Coupling Capacitor-less Line Amplifier

BD8876FV, BD8878FV

Description

BD8876FV, BD8878FV are output coupling capacitor-less line amplifiers. These IC have a negative voltage generator built-in and generate the negative voltage from the supply voltage. It is possible to drive in a ground reference with both voltage of the supply voltage and the negative voltage. Therefore, these line amplifiers have wide output range, and they can output 2Vrms(5.65V_{P-P}) with the single-supply 5V.

Features

- Possible to output 2Vrms with single-supply 5V
- Output Coupling Capacitor-less
- Variable Gain（+6dB / +9dB Typ.） [BD8876FV]
- Fixed Gain（+6.7dB Typ.）[BD8878FV]
- Integrated Negative Power Supply
- Ground-Referenced Outputs
- Integrated Short-Circuit and Thermal Protection

Applications

Video game console, Projector, Set Top Box, Blu-ray player etc.

Key Specifications

- Power Supply voltage: 3V to 5.5V
- THD+N: 0.003% (Typ)
  (V_{CC}=5V, R_L=10kΩ, Vo=2Vrms, 20kHz LPF)
- Maximum Output Voltage: 2Vrms (Min)@V_{CC}=5V
- Output Noise: 10μVrms (Typ)
- Circuit Current (Active): 3.2mA (Typ)
- Operating Temperature Range: -40°C to +85°C

Package

	W(Typ) x D(Typ) x H(Max)
SSOP-B14	5.00mm x 6.40mm x 1.35mm



SSOP-B14

Typical Application Circuit

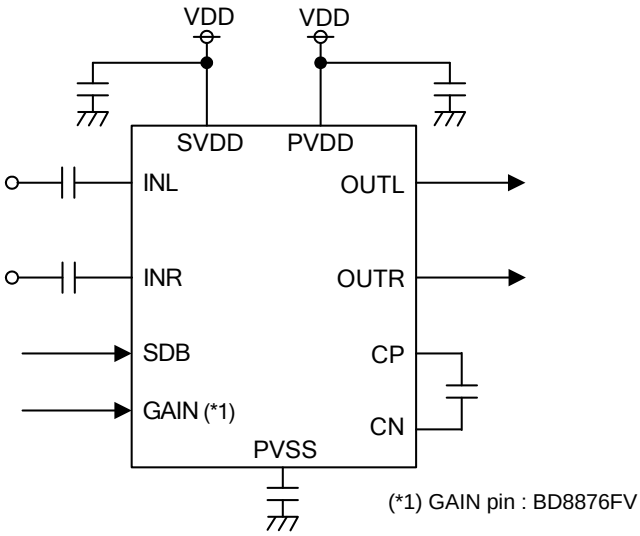


Figure 1. Typical Application Circuit

	BD8876FV	BD8878FV
Amplifier type	Inverting amplifier	Non-inverting amplifier
Gain	+6.0dB / +9.0dB (Changed by GAIN pin)	+6.7dB
Package	SSOP-B14	

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Pin Configurations

(TOP VIEW)

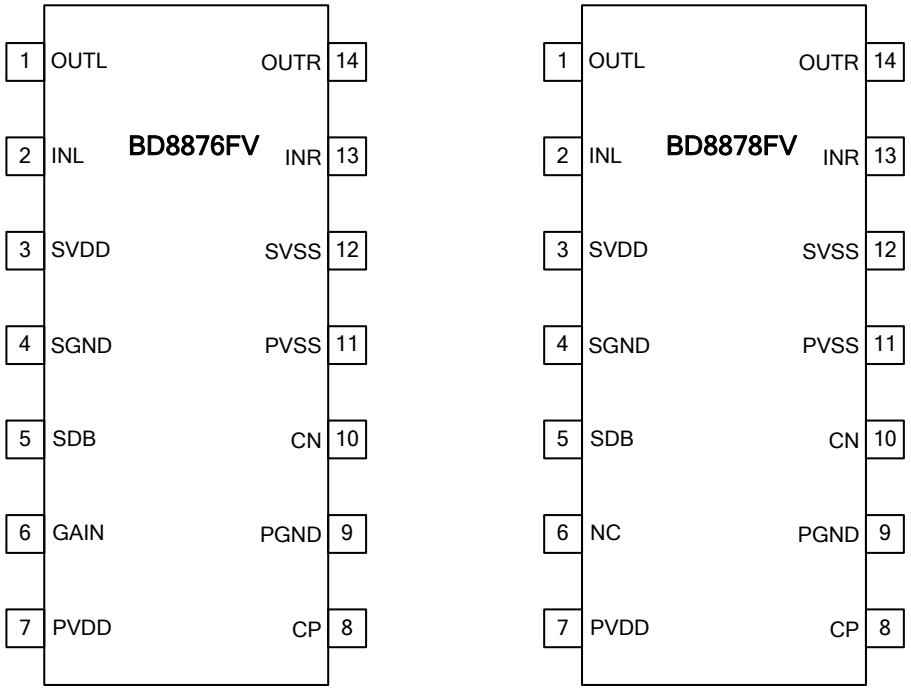
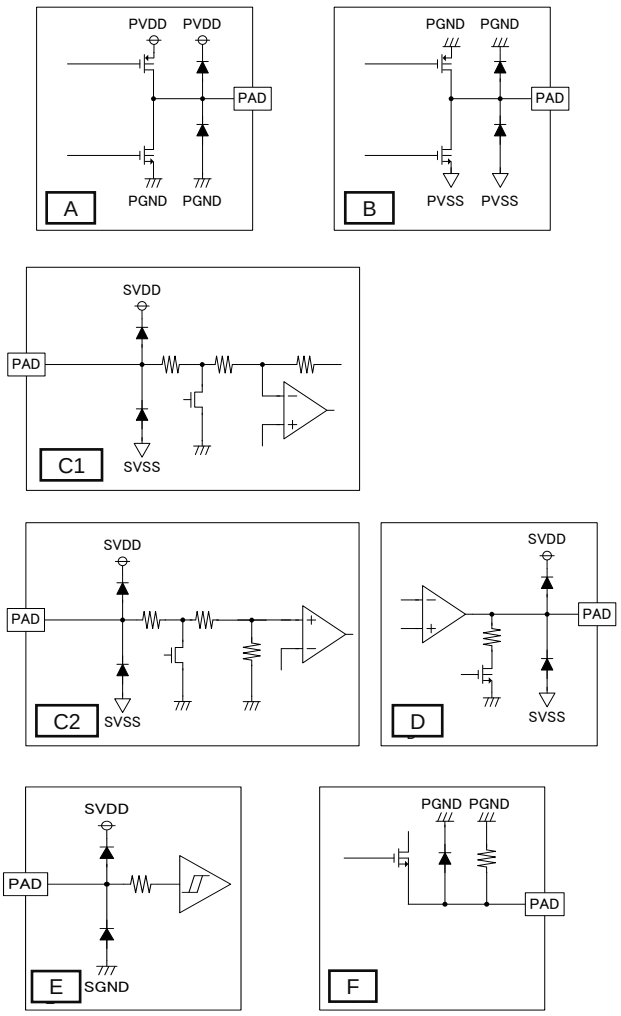


Figure 2. Pin Configurations

Pin Description/Function

PIN No.	Pin name	Function	Equivalence Circuit
1	OUTL	Line amplifier (Lch) output	D
2	INL	Line amplifier (Lch) input	C1 (BD8876FV) C2 (BD8878FV)
3	SVDD	Line amplifier supply voltage	-
4	SGND	Line amplifier ground	-
5	SDB	Shutdown control (H: active, L: shutdown)	E
6	GAIN (BD8876FV)	Gain control (H: 9.0dB, L:6.0dB)	E
	NC (BD8878FV)	No Connection	-
7	PVDD	Charge pump supply voltage	-
8	CP	Flying capacitor positive terminal	A
9	PGND	Charge pump ground	-
10	CN	Flying capacitor negative terminal	B
11	PVSS	Charge pump output voltage	F
12	SVSS	Line amplifier negative supply input	F
13	INR	Line amplifier (Rch) input	C1 (BD8876FV) C2 (BD8878FV)
14	OUTR	Line amplifier (Rch) output	D

Equivalence Circuit



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Block Diagrams

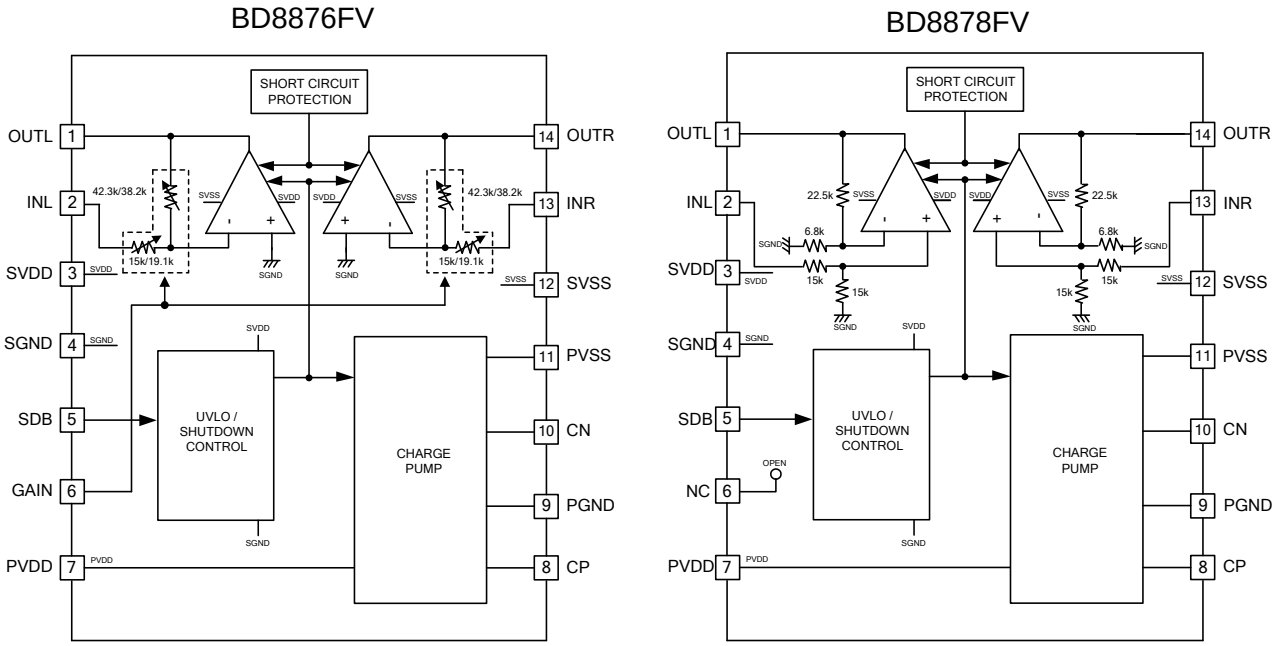


Figure 3. Block Diagrams

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
SVDD-PVDD Voltage	V_{DD}	0	V
SGND-PGND Voltage	V_{GG}	0	V
SVSS-PVSS Voltage	V_{SS}	0	V
SVDD, PVDD-SGND or PGND Voltage	V_{DG}	-0.3～6.0	V
SVSS, PVSS-SGND or PGND Voltage	V_{SG}	-6.0～0.3	V
IN_-SGND Voltage	V_{IN}	(SVSS-0.3)～(SVDD+0.3)	V
OUT_-SGND Voltage	V_{OUT}	(SVSS-0.3)～(SVDD+0.3)	V
CP-PGND Voltage	V_{CP}	(PGND-0.3)～(PVDD+0.3)	V
CN-PGND Voltage	V_{CN}	(PVSS-0.3)～(PGND+0.3)	V
SDB-SGND Voltage	V_{SH}	(SGND-0.3)～(SVDD+0.3)	V
GAIN-SGND Voltage	V_{GA}	(SGND-0.3)～(SVDD+0.3)	V
Input current	I_{IN}	-10～10	mA
Power Dissipation (NOTE 1)	P_D	0.87	W
Storage Temperature Range	T_{STG}	-55～+150	°C

(Note 1) Derate by 6.96mW/°C when operating above 25°C when mounted on 70mm x 70mm x 1.6mm, FR4.1-layer glass epoxy board.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Supply Voltage Range	V_{SVDD}, V_{PVDD}	3.0	-	5.5	V
Operating Temperature Range	T_{OPR}	-40	-	+85	°C
Minimum Load Impedance	Z_L	550	-	-	Ω

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Electrical Characteristics

(Unless otherwise specified, Ta=25°C, SVDD=PVDD=5V, SGND=PGND=0V, SDB=H, GAIN=L [BD8876FV], C_1=C_2=1µF, R_L=10kΩ, Input coupling capacitor=1µF)

Parameter	Symbol	Limit						Unit	Remarks
		BD8876FV			BD8878FV				
		Min	Typ	Max	Min	Typ	Max		
Circuit current									
Circuit Current (Shutdown)	I_{ST}	-	0.1	2	-	0.1	2	µA	SDB=L
Circuit Current (Active)	I_{DD}	-	3.2	8.2	-	3.2	10.5	mA	SDB=H, No signal, RL=No load
SDB pin/GAIN pin									
H Level Input Voltage	V_{IH}	0.7 x SVDD	-	-	0.7 x SVDD	-	-	V	
L Level Input Voltage	V_{IL}	-	-	0.3 x SVDD	-	-	0.3 x SVDD	V	
Input Leak Current	I_{LEAK}	-	-	±1	-	-	±1	µA	
Line amplifier									
Start up time	t_{SON}	-	470	-	-	470	-	µsec	SDB=L→H
Offset Voltage	V_{IS}	-	±0.5	±5	-	±1	±10	mV	
Maximum Output Voltage	V_{OUT}	2.5	3.5	-	2.05	3.0	-	Vrms	f=1kHz , THD+N≦-40dB, 20kHz LPF
THD+N	THD+N	-	0.003	0.032	-	0.003	0.032	%	f=1kHz, VOUT=2Vrms, 20kHz LPF
Input Impedance	Z_{IN1} *1	12	19	26	20	30	40	kΩ	*1 GAIN=L (6dB mode) *2 GAIN=H (9dB mode)
	Z_{IN2} *2	10	15	20					
Gain	A_{V1} *1	5.0	6.0	7.0	5.7	6.7	7.7	dB	*1 GAIN=L (6dB mode) *2 GAIN=H (9dB mode)
	A_{V2} *2	8.0	9.0	10.0					
Gain mismatch	ΔA_V	-	1	-	-	1	-	%	
Output Noise	V_N	-	8	-	-	10	-	µVrms	20kHz LPF+A-Weight filter, Rg=0ohm
Slew Rate	SR	-	3.0	-	-	3.0	-	V/µsec	
Maximum Capacitive Load	C_L	-	-	250	-	-	250	pF	
Crosstalk	CT	-	-80	-	-	-65	-	dB	f=1kHz, VOUT=200mV$_{P-P}$, 1kHz BPF
Power Supply Rejection Ratio	PSRR	-	-65	-	-	-65	-	dB	f=1kHz, V_{ripple}=100mV$_{P-P}$, 1kHz BPF
Charge-Pump Oscillator Frequency	f_{OSC}	150	300	450	150	300	450	kHz	

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(Unless otherwise specified, Ta=25°C, SVDD=PVDD=5V, SGND=PGND=0V, SDB=H, GAIN=L [BD8876FV], C_1=C_2=1µF, R_L=10kΩ, Input coupling capacitor=1µF) * SVDD, PVDD shows as "VDD" in the following graphs.

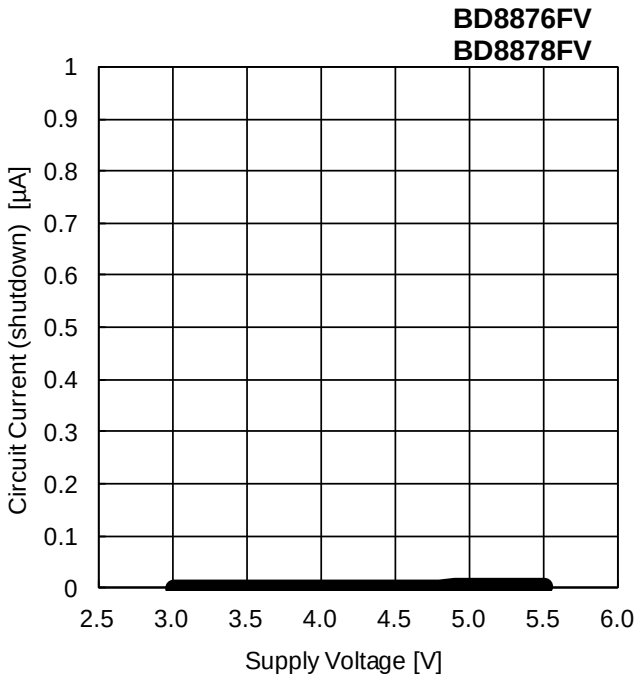


Figure 4.
Circuit Current (Shutdown)
vs. Supply Voltage

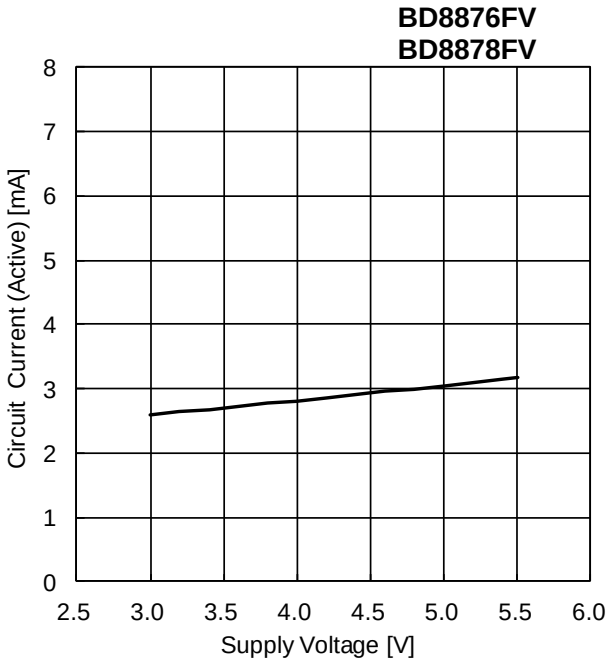


Figure 5.
Circuit Current (Active)
vs. Supply Voltage

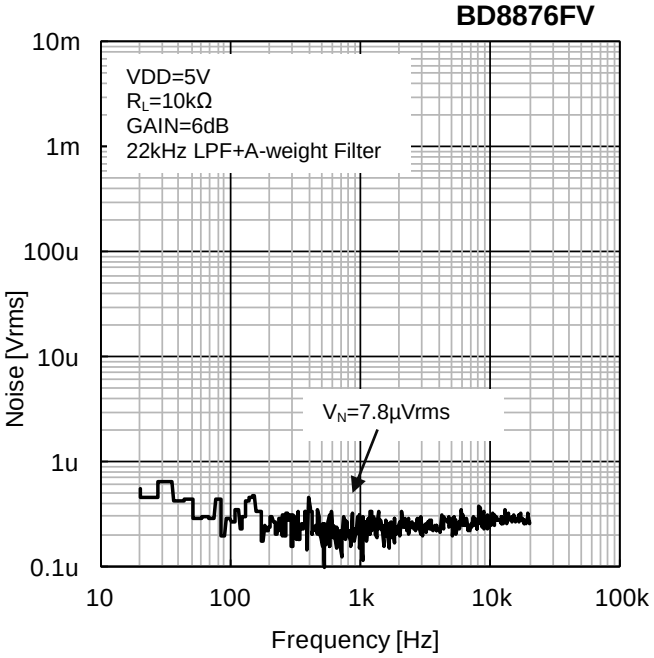


Figure 6.
Noise Level (BD8876FV)

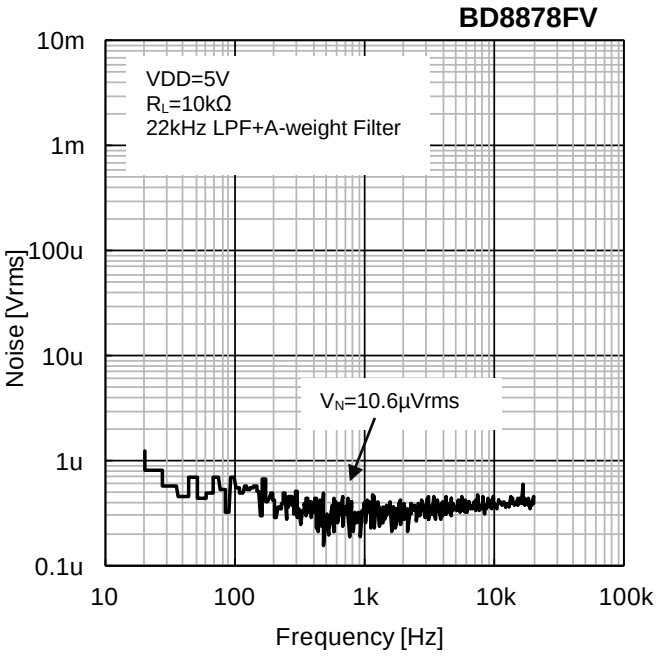


Figure 7.
Noise Level (BDD8878FV)

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(Unless otherwise specified, Ta=25°C, SVDD=PVDD=5V, SGND=PGND=0V, SDB=H, GAIN=L [BD8876FV], C_1=C_2=1µF, R_L=10kΩ, Input coupling capacitor=1µF) * SVDD, PVDD shows as "VDD" in the following graphs.

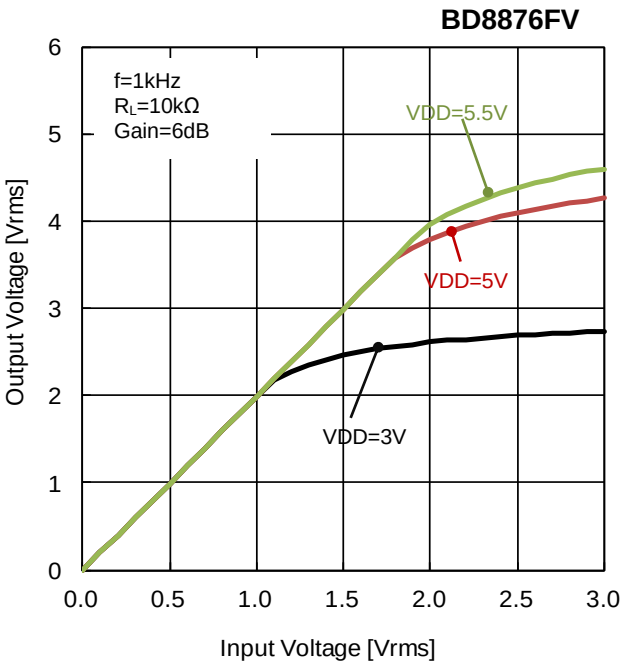


Figure 8.
Output Voltage vs. Input Voltage
(BD8876FV, 6dB)

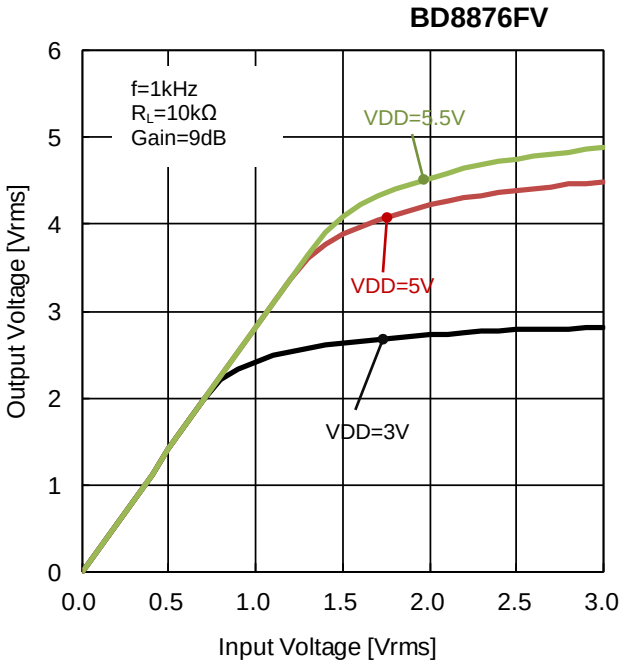


Figure 9.
Output Voltage vs. Input Voltage
(BD8876FV, 9dB)

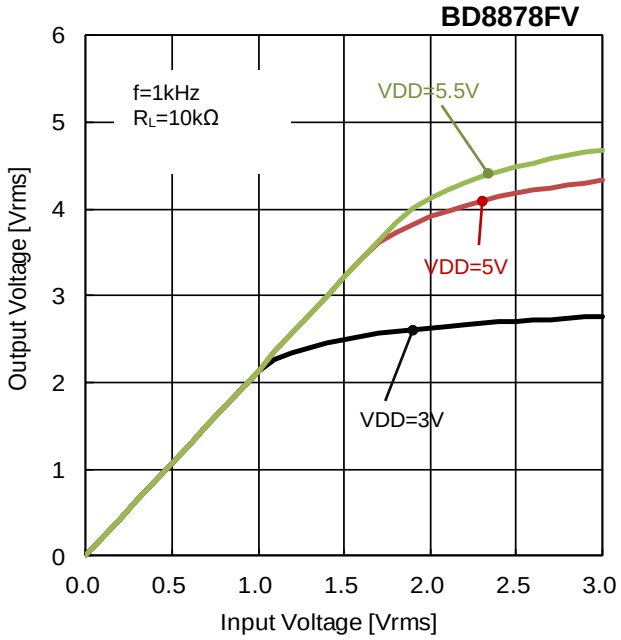


Figure 10.
Output Voltage vs. Input Voltage
(BD8878FV)

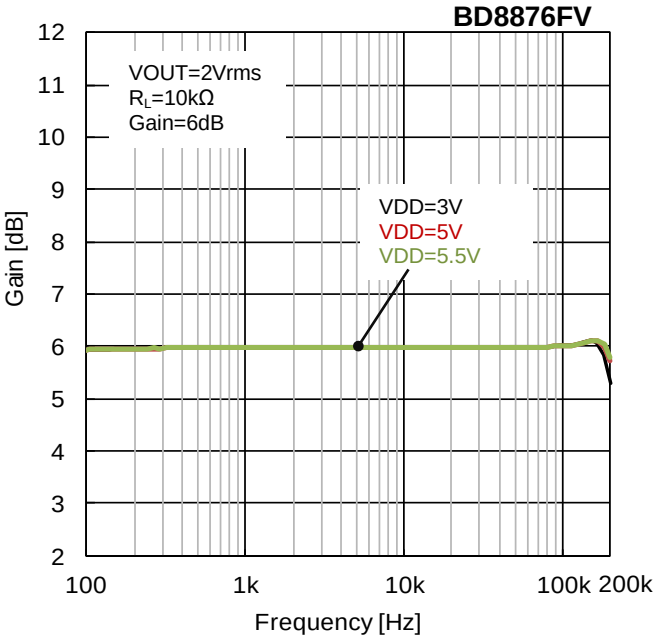


Figure 11.
Gain vs. Frequency
(BD8876FV, 6dB)

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(Unless otherwise specified, Ta=25°C, SVDD=PVDD=5V, SGND=PGND=0V, SDB=H, GAIN=L [BD8876FV], C_1=C_2=1µF, R_L=10kΩ, Input coupling capacitor=1µF) * SVDD, PVDD shows as "VDD" in the following graphs.

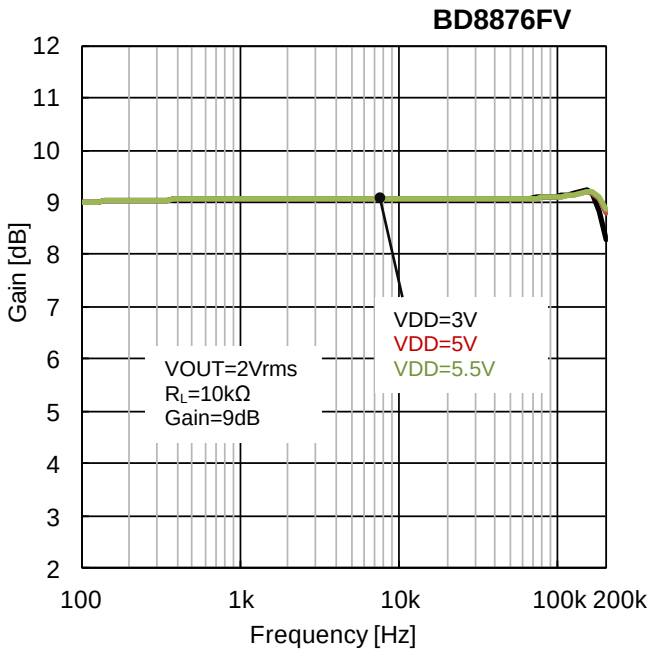


Figure 12.
Gain vs. Frequency
(BD8876FV, 9dB)

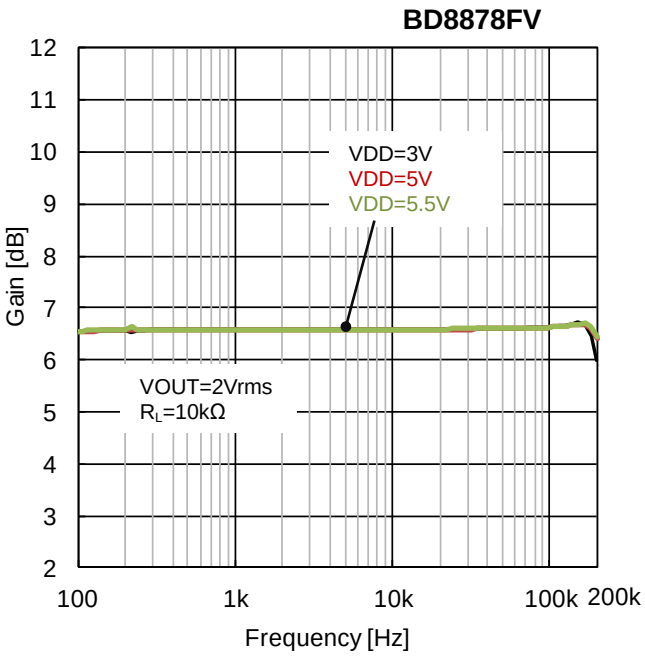


Figure 13.
Gain vs. Frequency
(BD8878FV)

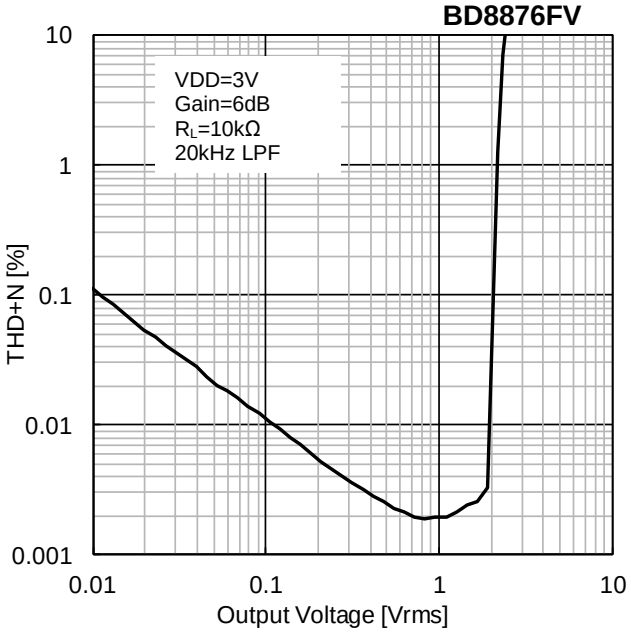


Figure 14.
THD+N vs. Output Voltage
(BD8876FV, 3V)

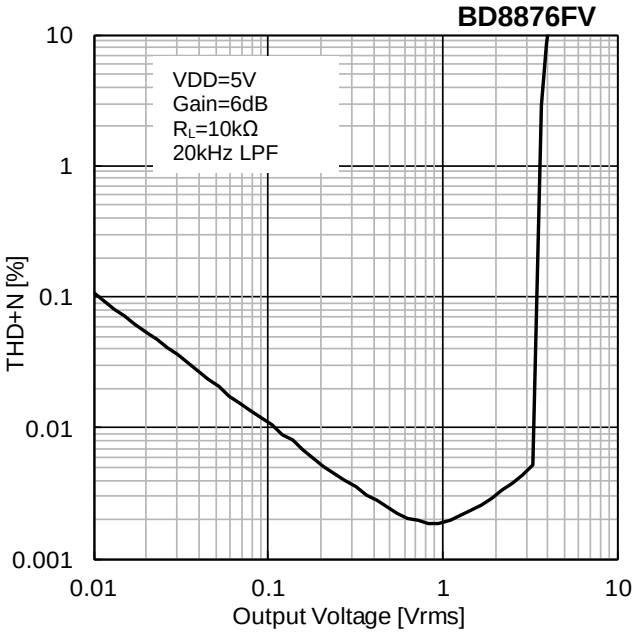


Figure 15.
THD+N vs. Output Voltage
(BD8876FV, 5V)

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(Unless otherwise specified, Ta=25°C, SVDD=PVDD=5V, SGND=PGND=0V, SDB=H, GAIN=L [BD8876FV], C_1=C_2=1µF, R_L=10kΩ, Input coupling capacitor=1µF) * SVDD, PVDD shows as "VDD" in the following graphs.

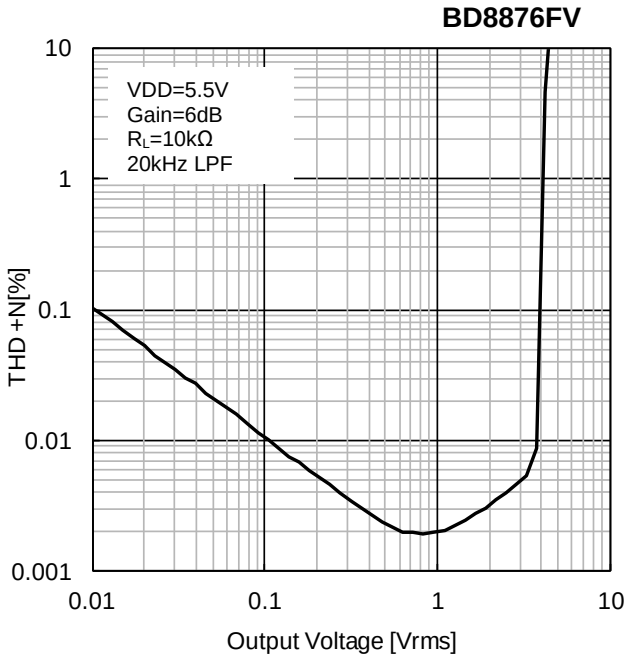


Figure 16.
THD+N vs. Output Voltage
(BD8876FV, 5.5V)

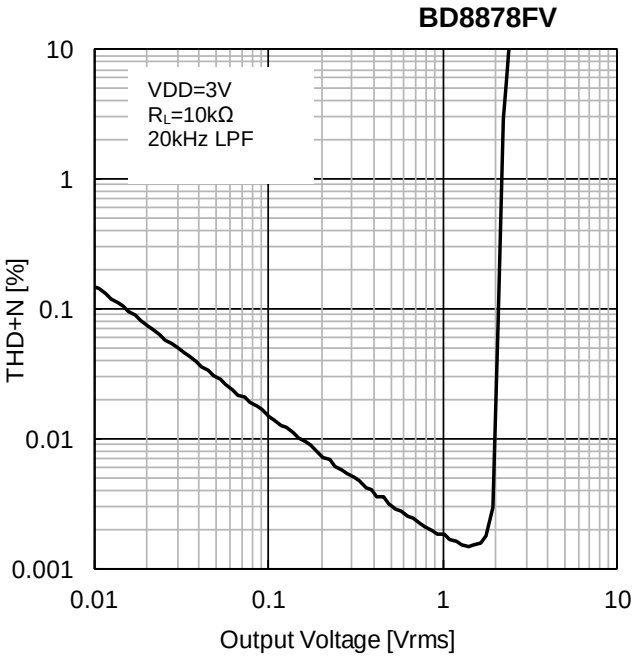


Figure 17.
THD+N vs. Output Voltage
(BD8878FV, 3V)

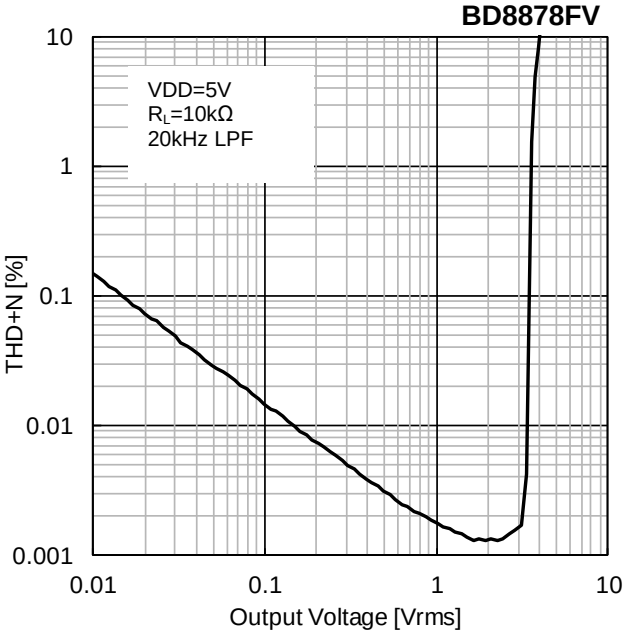


Figure 18.
THD+N vs. Output Voltage
(BD8878FV, 5V)

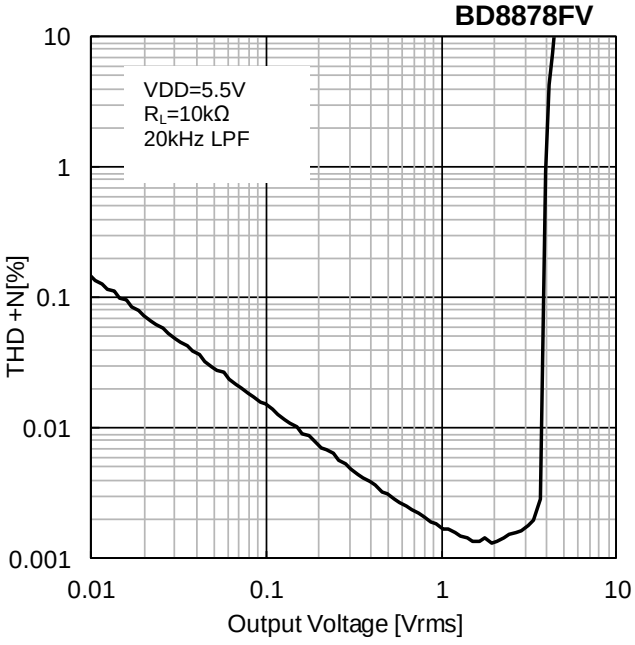


Figure 19.
THD+N vs. Output Voltage
(BD8878FV, 5.5V)

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(Unless otherwise specified, Ta=25°C, SVDD=PVDD=5V, SGND=PGND=0V, SDB=H, GAIN=L [BD8876FV], C_1=C_2=1µF, R_L=10kΩ, Input coupling capacitor=1µF) * SVDD, PVDD shows as "VDD" in the following graphs.

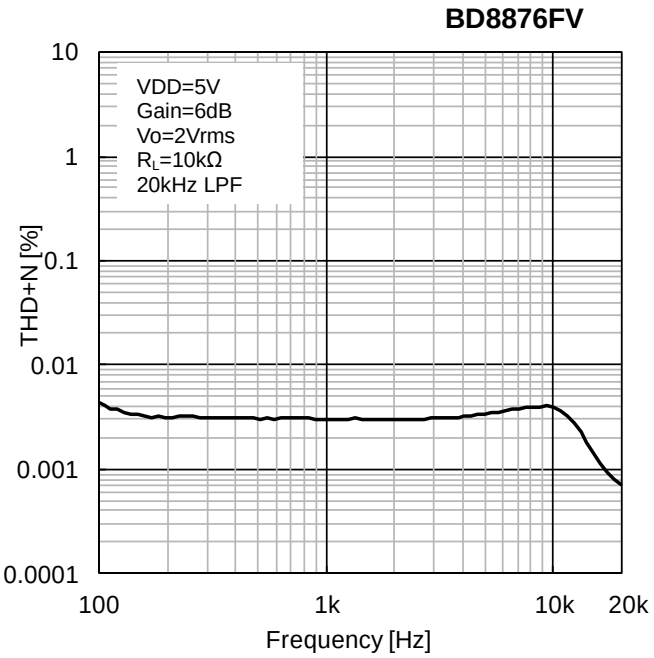


Figure 20.
THD+N vs. Frequency
(BD8876FV)

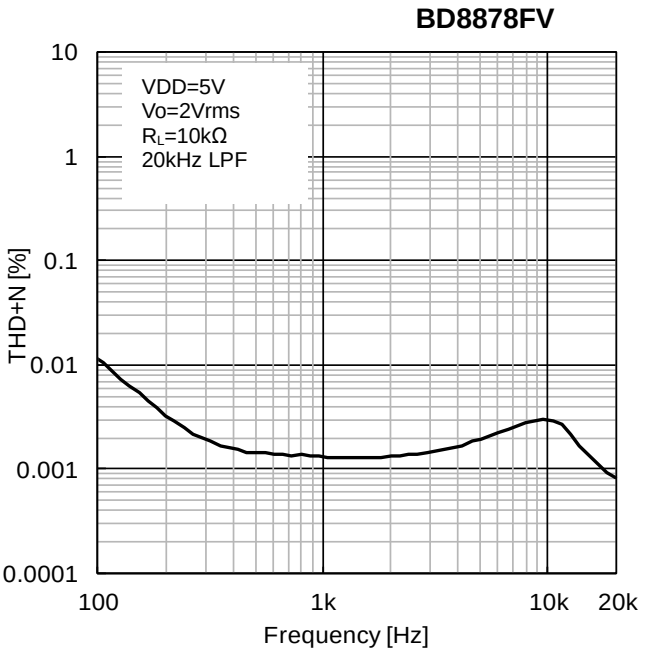


Figure 21.
THD+N vs. Frequency
(BD8878FV)

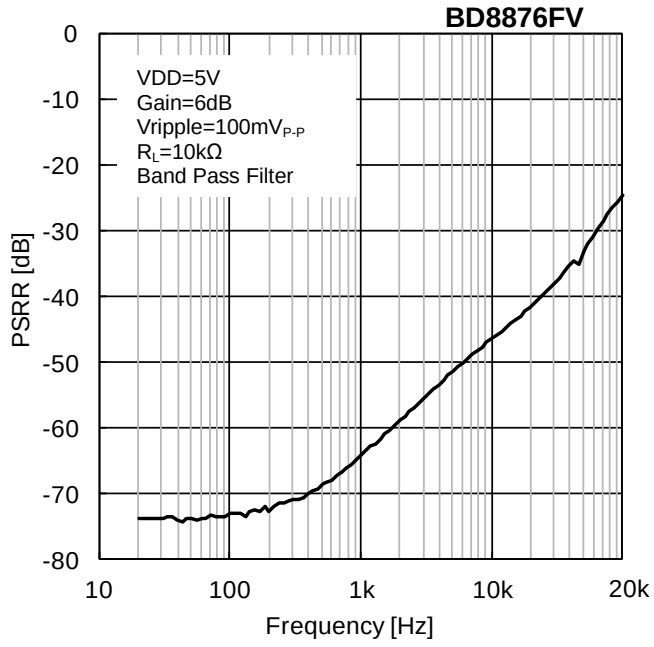


Figure 22.
PSRR vs. Frequency
(BD8876FV)

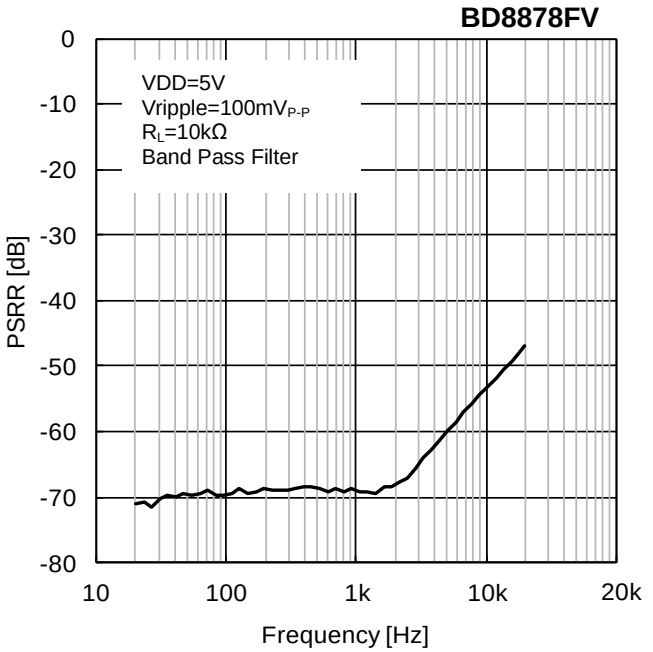


Figure 23.
PSRR vs. Frequency
(BD8878FV)

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(Unless otherwise specified, Ta=25°C, SVDD=PVDD=5V, SGND=PGND=0V, SDB=H, GAIN=L [BD8876FV], C_1=C_2=1µF, R_L=10kΩ, Input coupling capacitor=1µF) * SVDD, PVDD shows as "VDD" in the following graphs.

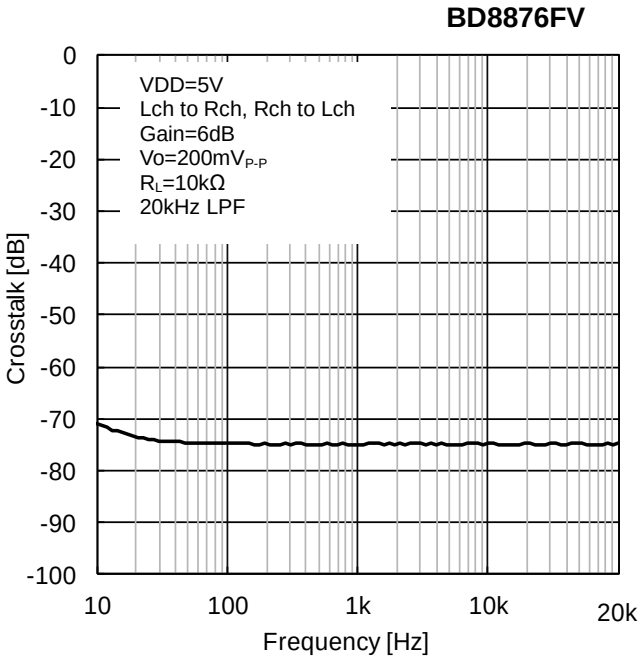


Figure 24.
Crosstalk vs. Frequency
(BD8876FV, 200mV$_{P-P}$)

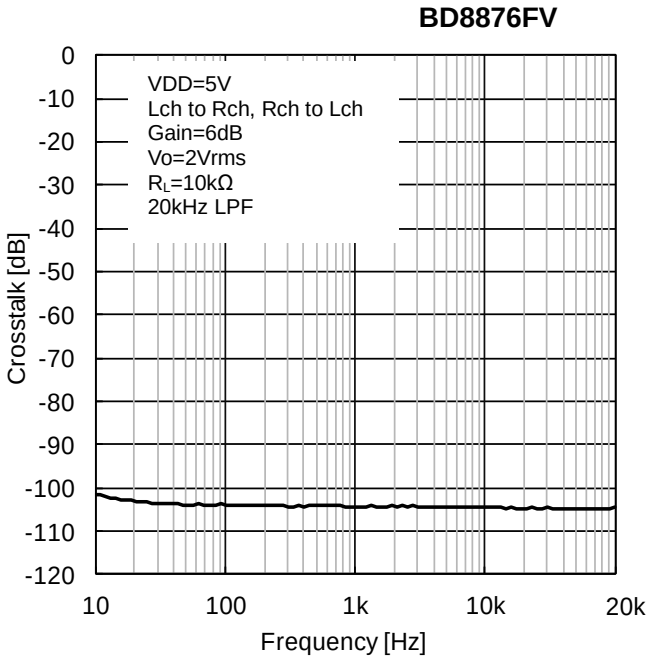


Figure 25.
Crosstalk vs. Frequency
(BD8876FV, 2Vrms)

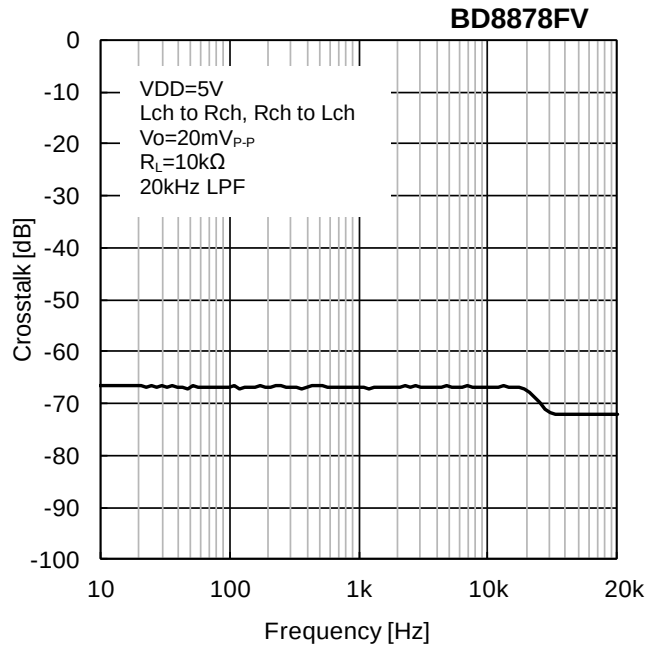


Figure 26.
Crosstalk vs. Frequency
(BD8878FV, 200mV$_{P-P}$)

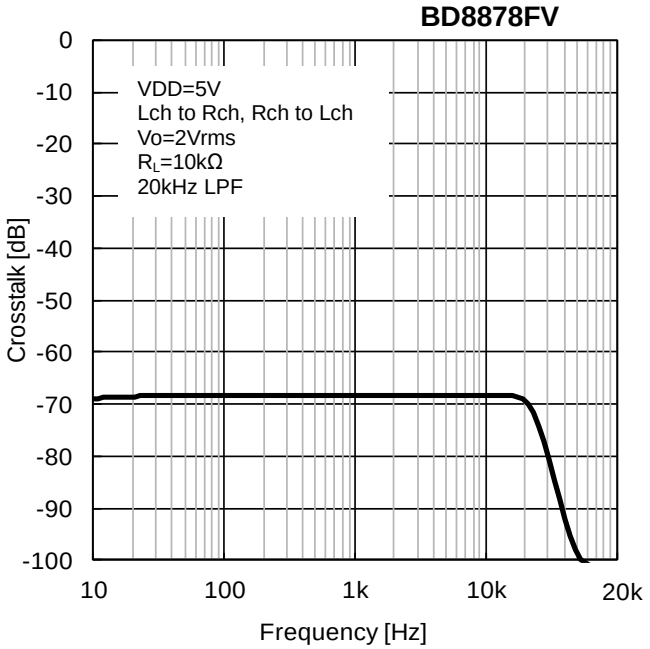


Figure 27.
Crosstalk vs. Frequency
(BD8878FV, 2Vrms)

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Application Examples

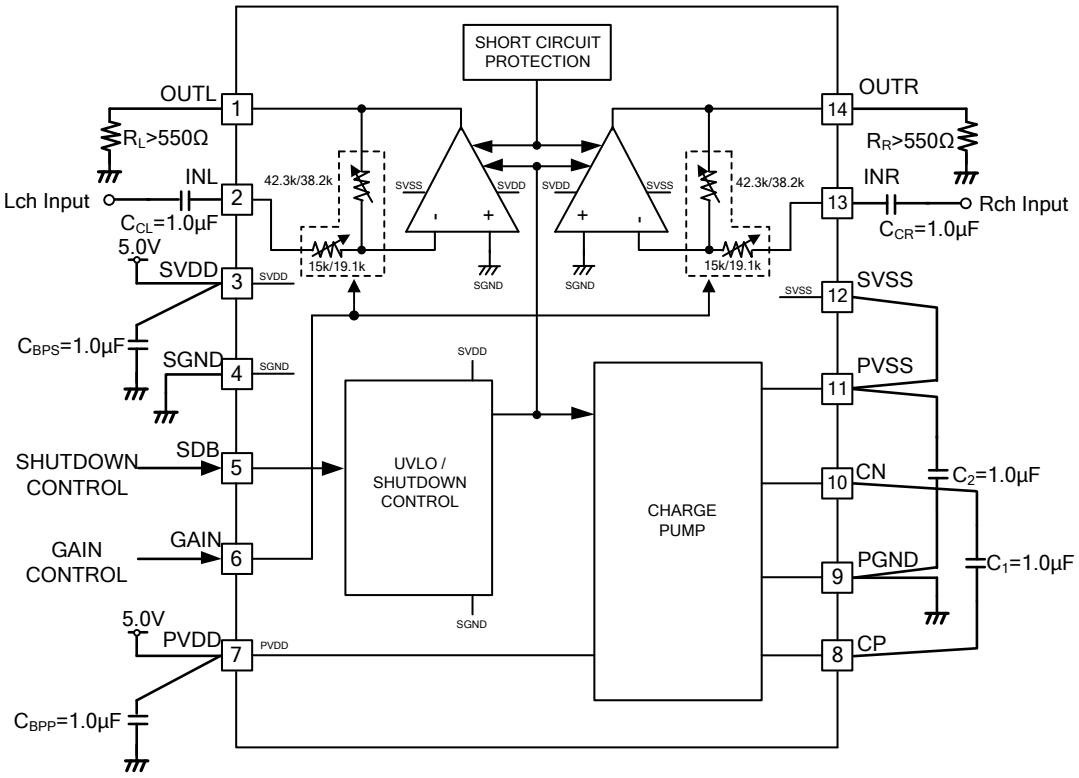


Figure 28. BD8876FV Application circuit example

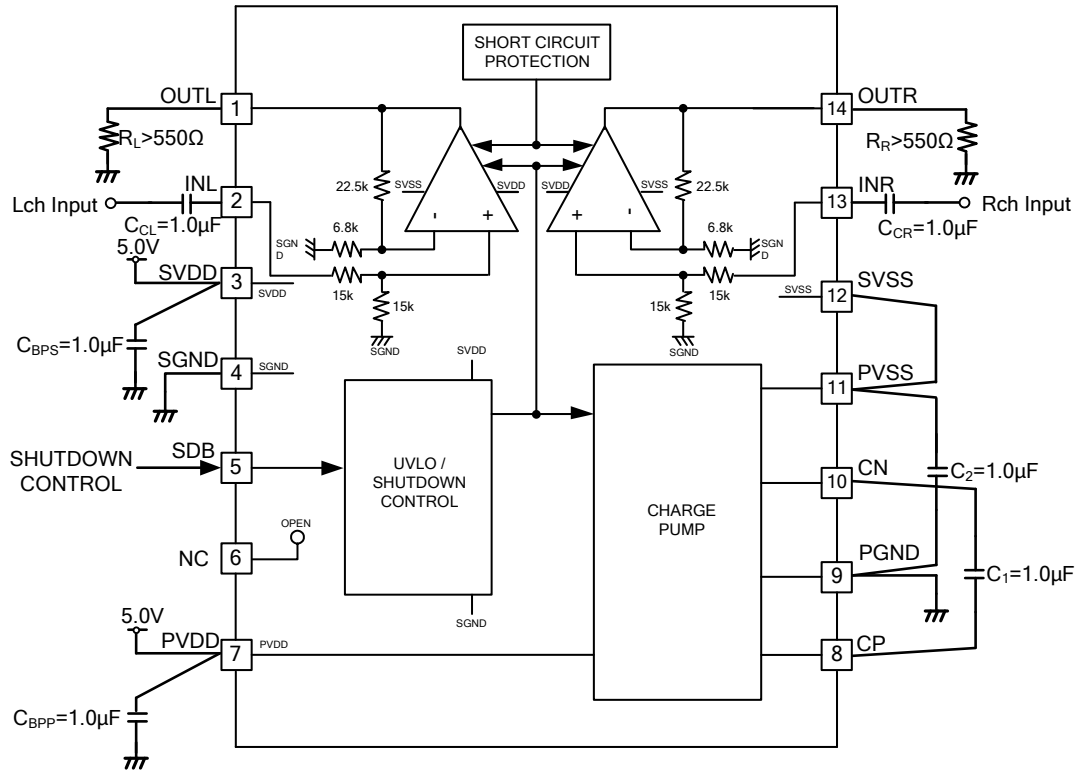


Figure 29. BD8878FV Application circuit example

* PVSS and SVSS are connected each other inside IC. But, please connect PVSS and SVSS outside IC, also.

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Timing Chart

< Sequence of start-up / power-down>

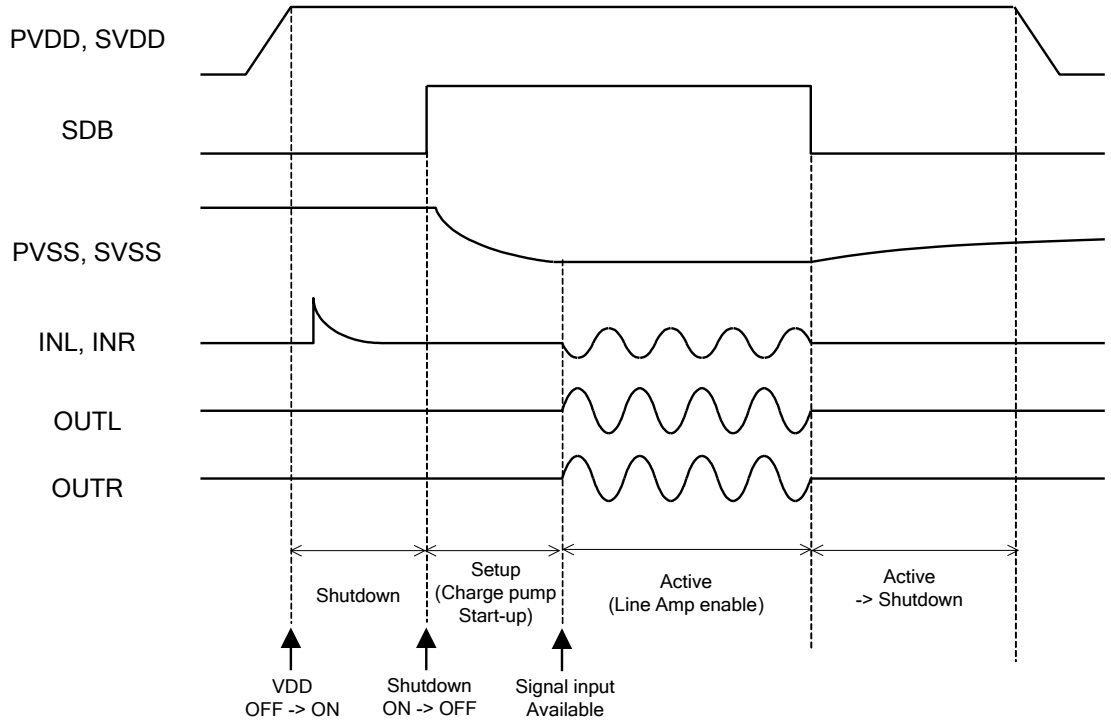


Figure 30. Sequence of start-up / power-down

① The term from “PVDD, SVDD : ON” to “shutdown ON->OFF”

When power supply (PVDD, SVDD) is applied, it is started that charging input coupling capacitors. Therefore, the input terminal voltage ”Vin” is changed as following Figure 31. Time constant “ τ ” of charging input coupling capacitor is decided by input coupling capacitor Cin and Internal input impedance Rin (See formula (1)). Internal impedance Rin in term of shutdown is 7.5kΩ(typ) for making time constant τ shorten. If “SDB” is changed “L” to “H” (shutdown ON -> OFF) during input DC voltage (Vin) is changing, pop noise may occur. It is recommended that shutdown ON -> OFF (“SDB” : L -> H) after 5τ ~ 6τ.

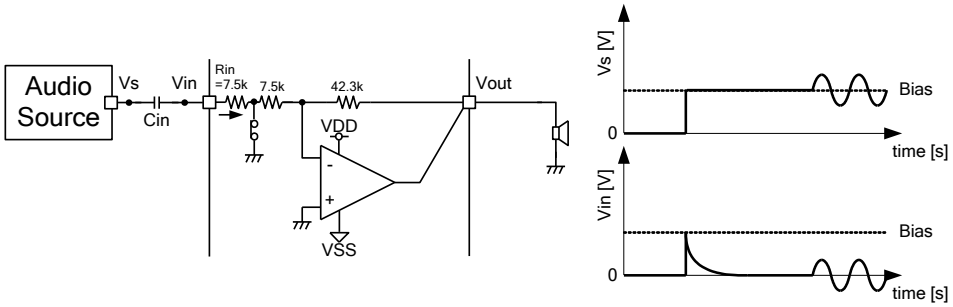


Figure 31. Fluctuation of input terminal voltage when charging input coupling capacitor

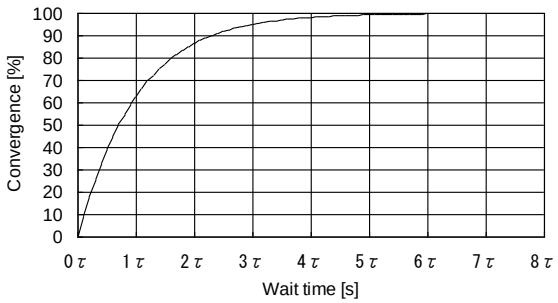


Figure 32. Wait time vs. convergence

$$\tau = Rin \times Cin \quad (1)$$

(e.g.) in case of Cin =1.0μF,
τ = Rin x Cin
=7.5kΩ x 1.0μF
= 7.5 msec(typ)
6τ = 6 x 7.5msec
= 45 msec (typ)

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② The term from shutdown OFF to line amplifier start-up

When shutdown is ON -> OFF, charge pump starts up. Line amplifier is stopped during “t_{SON} (start-up time of charge pump, 470µsec typ.)” for preventing irregular output. Please input audio signal after “t_{SON}”.

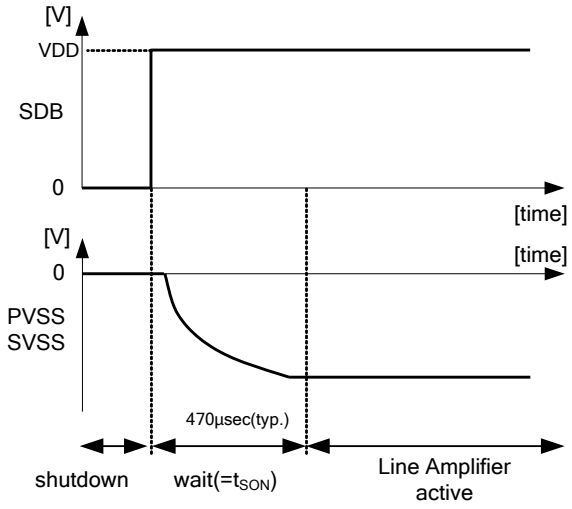


Figure 33. Wait time for Line amplifier from “shutdown ON -> OFF”

Functional Descriptions / Application Information

The composition of conventional line amplifier is shown in Figure 34. Output signal swings in reference to Middle DC bias (e.g. VDD/2). Therefore, Output dynamic range of line amplifier limits until “VDD”.

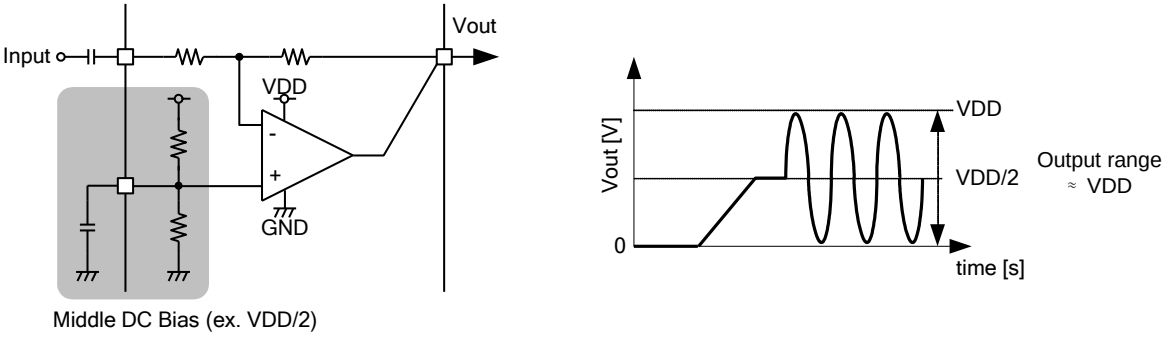


Figure 34. The composition of conventional line amplifier

The composition of BD8876FV/BD8878FV is shown to Figure 35. Output signal swings in reference to ground level. Line amplifier can output between from VSS (-VDD) to VDD. Therefore, Output dynamic range of line amplifier expands “2 x VDD”. And, it is possible to drive 2Vrms ($5.65V_{P-P}$) with single supply voltage 5V.

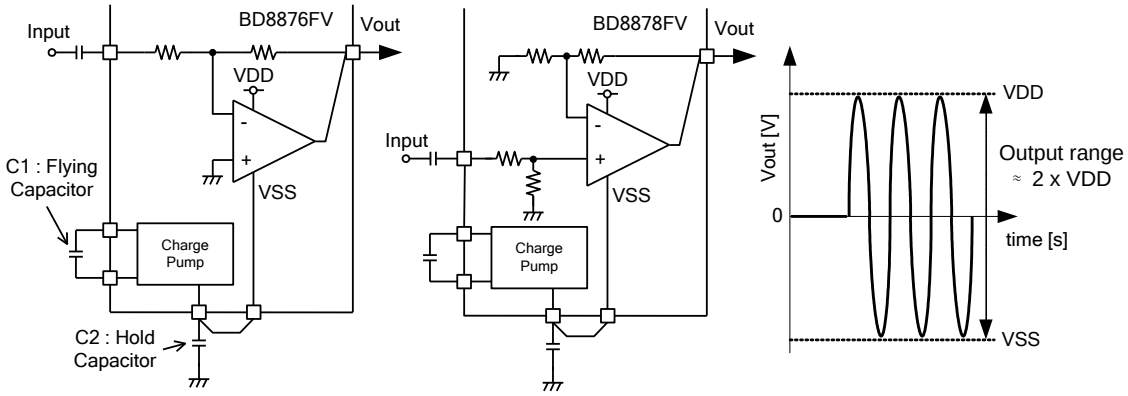


Figure 35. The composition of BD8876FV/BD8878FV

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■ CHARGE PUMP

The negative power supply circuit is composed of the regulated charge-pump. This circuit outputs the negative voltage (PVSS) from positive power-supply voltage (PVDD).
The negative power supply circuit starts when “SDB=H”, and power is downed when “SDB=L”(See Table 1).

Table 1. Control of the charge pump circuit

SDB	Control
L	Power down
H	Power on

＜The flying capacitor and the hold capacitor＞

The flying capacitor (Figure 35. C1) and the hold capacitor (Figure 35. C2) have great influences on the characteristic of the charge pump. Please select capacitors that have low ESR characteristic and low voltage coefficient, low temperature coefficient for C1, C2. And, please connect these capacitors as near as possible to IC.

＜Over-current Protection＞

The charge pump has the over-current protection function. If the terminals of charge pump (CP, CN, PVSS, SVSS) are under the abnormal connecting conditions (e.g. shorting to ground), this function shutdown IC and protect it from the damage.

■Line Amplifier

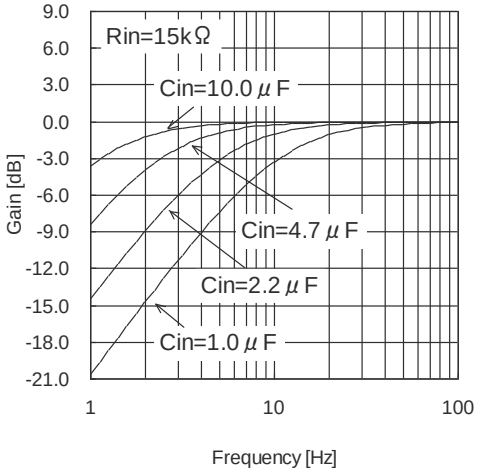
The line amplifier is driven by power-supply voltage (SVDD) and negative voltage (SVSS) based on ground (SGND). Therefore, the amplifier can output 2Vrms for RL=10kohm with the single supply voltage 5V. And BD8876FV can change the gain 6dB and 9dB. The gain of BD8878FV is 6.7dB (fixed).
The both of Lch and Rch of the line amplifier are simultaneously controlled by SDB logic (See Table 2).
In addition, the over-current protection circuit is built in. The amplifier is shutdown, when the over-current occurs because of the output short-circuit etc., and IC is protected from being destroyed.

Table 2. Control of the Line amplifier circuit

SDB	Lch/Rch amplifier control
L	Power down
H	Power on

＜Input coupling capacitor＞

Input DC voltage level of BD8876FV/BD8878FV is 0V (SGND). Therefore, input coupling capacitor is needed.
Gain is decreased in low frequency because of composing the high-pass filter by input coupling capacitor Cin and internal input impedance Rin of BD8876FV/BD8878FV.
Input impedance R_{in} of BD8876FV is 15kΩ (Typ, Gain=+9dB), and R_{in} of BD8878FV is 30kΩ (Typ).
Cut-off frequency of the high-pass filter is shown to the following formula (2).



$$f_c = \frac{1}{2\pi R_{in} C_{in}} \quad (2)$$

Figure 36. Frequency response by the input coupling capacitor (Reference data: Calculated value)

The degradation of THD happens because of the input coupling capacitor. Therefore, please consider the applied voltage dependence and the temperature characteristic of the capacitor when selecting parts.

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- UVLO / SHUTDOWN CONTROL

BD8876FV/BD8878FV has low voltage protection function (UVLO: Under Voltage Lock Out).
UVLO function protects from abnormal operation under lower power supply voltage than the recommended supply voltage range. The detection voltage is 2.8V (Typ). It does not influence the recommended operation voltage (3.0V (Min)). The power control by UVLO works for the whole of IC, and power down the both of the negative power supply charge pump and the line amplifier. If power supply voltage recovers over recommended range (3.0V), all function also recover automatically.

Power Dissipation

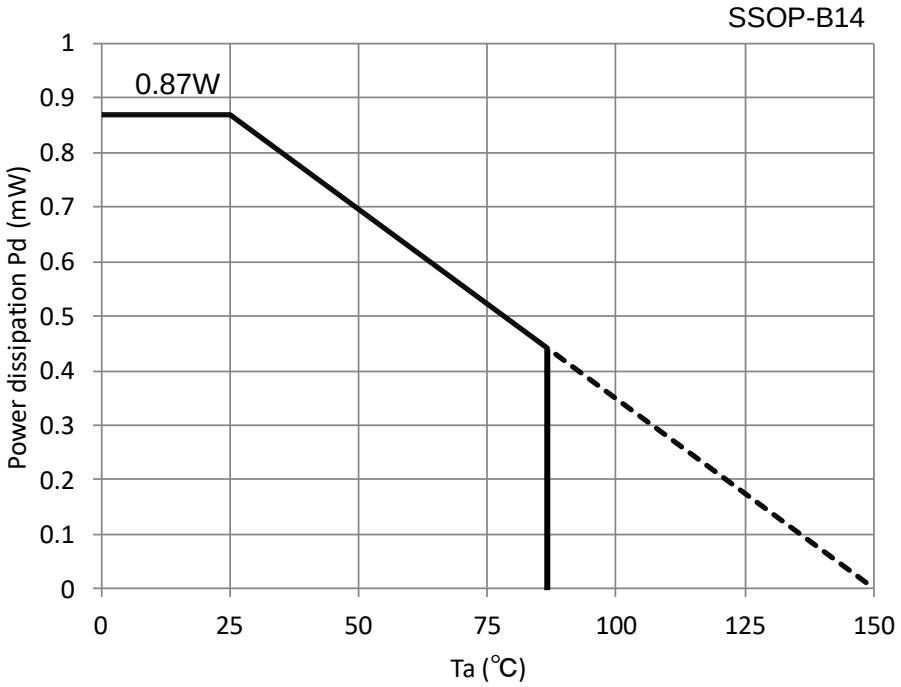


Figure 37. Power Dissipation Curve

Measurement Condition: Mounted on ROHM standard board, glass-epoxy
Board size: 74.2mm×74.2mm×1.6mm (1-layer)
Material: FR4

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Rush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Terminals**
    Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

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Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

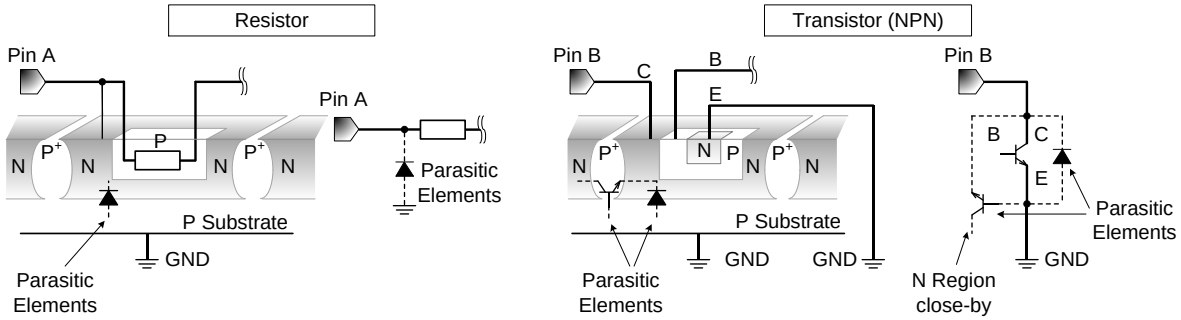


Figure 38. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

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Ordering Information

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B	D	8	8	7	8	F	V	-	E	2

Part Number

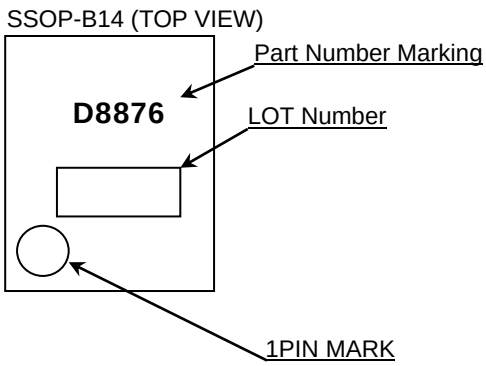
Package
FV: SSOP-B14

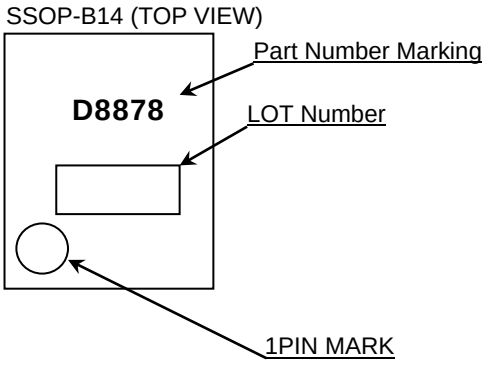
Packaging and forming specification
E2: Embossed tape and reel

Line-up

	BD8876FV	BD8878FV
Amplifier type	Inverting amplifier	Non-inverting amplifier
Gain	+6dB / +9dB (Changed by Gain pin)	+6.7dB
Package	SSOP-B14	

Marking Diagram



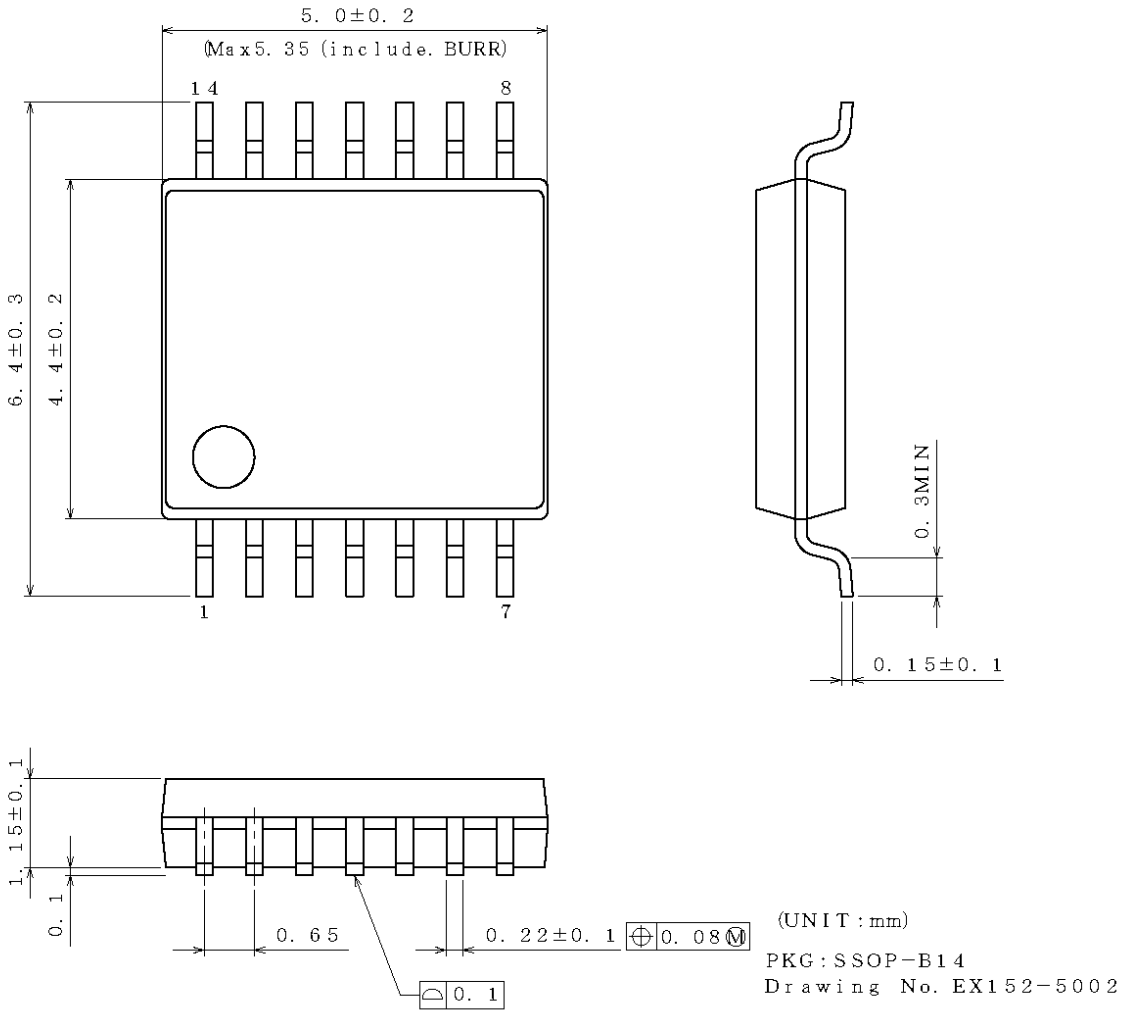


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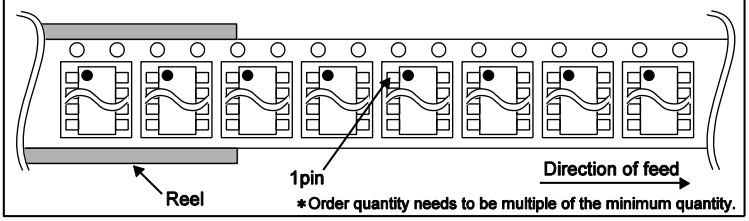
Physical Dimension, Tape and Reel Information

Package Name	SSOP-B14



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
30.Oct.2015	001	First version
18.Jan.2021	002	Updated packages and part numbers P.20-2,P20-3

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Ordering Information

B	D	8	8	7	6	F	V	-	Z	E	2
B	D	8	8	7	8	F	V	-	Z	E	2

Part Number

Package
FV: SSOP-B14K

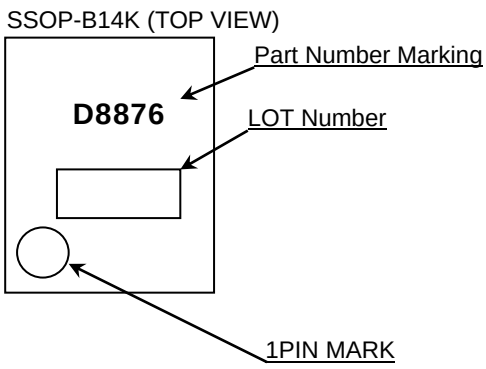
Packaging and forming specification
E2: Embossed tape and reel

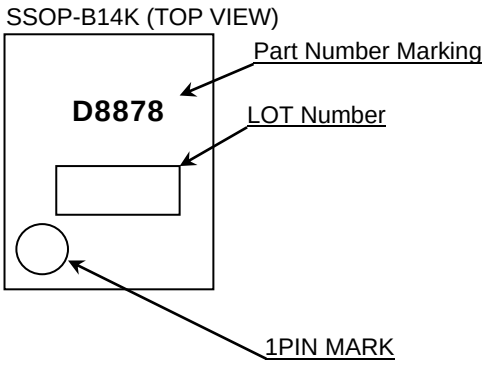
Production site
Z: Added

Line-up

	BD8876FV	BD8878FV
Amplifier type	Inverting amplifier	Non-inverting amplifier
Gain	+6dB / +9dB (Changed by Gain pin)	+6.7dB
Package	SSOP-B14K	

Marking Diagram



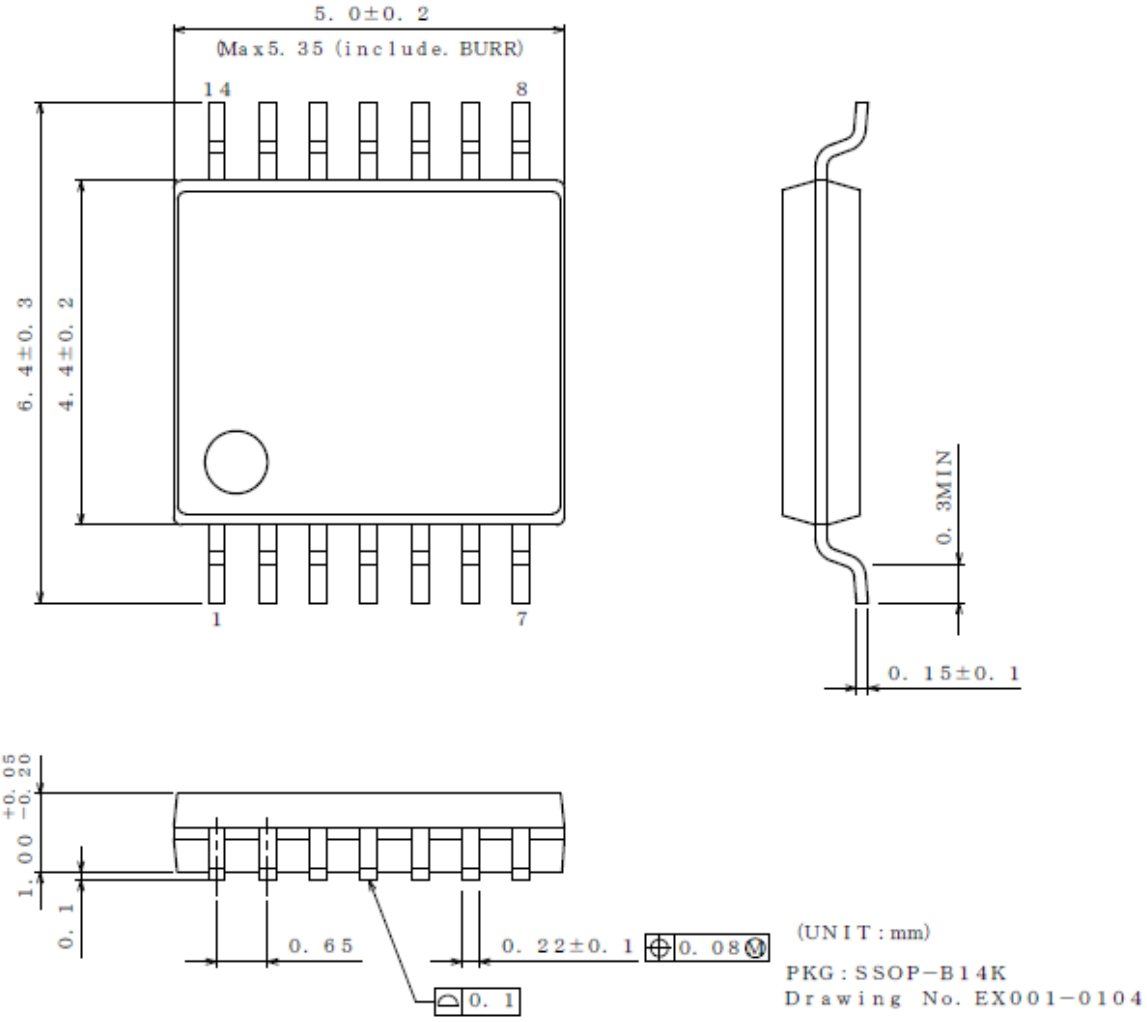


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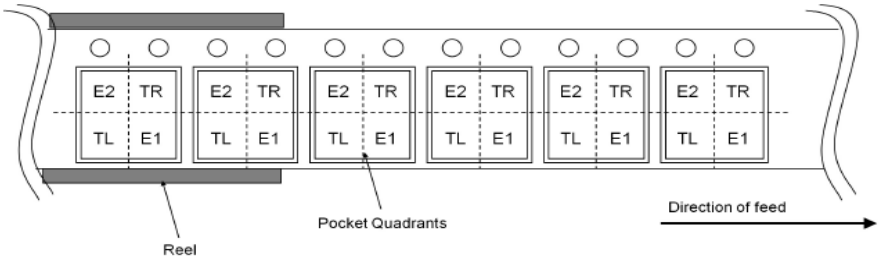
Physical Dimension and Packing Information

Package Name	SSOP-B14K



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

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6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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