SY89206V

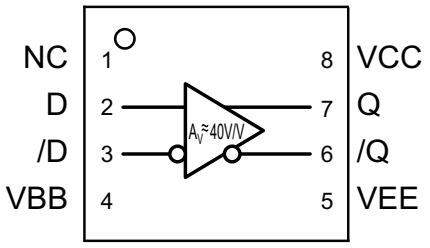
3.3V/5V 1 GHz Differential PECL/ECL Receiver/Buffer

Features

- Maximum Frequency >1.0 GHz
- 3.3V and 5V Power Supply Options
- 250 ps Typical Propagation Delay
- High Bandwidth Output Transitions
- Internal 75 kΩ Input Pull-Down Resistors
- 100k PECL/ECL Compatible
- Open Input Default State
- Industrial Temperature Range: –40°C to +85°C
- Available in an Ultra-Small 8-Pin 2 mm x 2 mm VDFN Package

Package Type

SY89206V
8-Lead VDFN



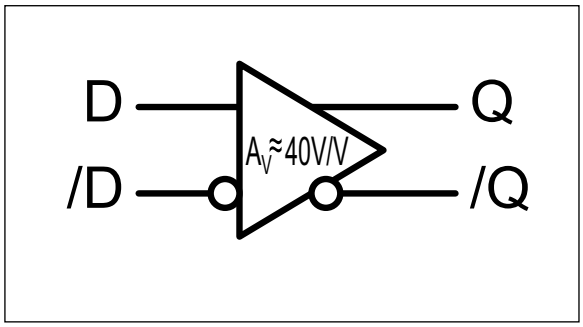
General Description

The SY89206V is a differential PECL/ECL receiver/buffer in a space-saving (2 mm x 2 mm) VDFN package. The device is functionally equivalent to the SY100EL16V, but features a 70% smaller footprint.

The SY89206V provides a VBB output for either single-ended use or as a DC bias for AC-coupling to the device. The VBB pin should be used only as a bias for the SY89206V as its current sink/source capability is limited. Whenever used, the VBB pin should be bypassed with a 0.01 µF capacitor to VCC.

Under open input conditions (pulled to VEE), internal input clamps will force the Q output LOW.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

PECL Power Supply Voltage (V_{CC}) (Note 1) ..... +8V
NECL Power Supply Voltage (V_{EE}) (Note 2) ..... –8V
PECL Mode Input Voltage (V_{IN}) (Note 3) ..... +6V
NECL Mode Input Voltage (V_{IN}) (Note 4) ..... –6V
Continuous Output Current (I_{OUT}) ..... 50 mA
Surge Output Current (I_{OUT}) ..... 100 mA

† Notice: Stresses above those listed under “Absolute Maximum ratings” may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: V_{EE} = 0V.

2: V_{CC} = 0V.

3: V_{EE} = 0V, $V_{IN} \leq V_{CC}$.

4: V_{CC} = 0V, $V_{IN} \geq V_{EE}$.

5: Mil Std. 883 Human Body Model, all pins

DC ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: V_{CC} = 3.0V to 5.5V; V_{EE} = 0V or V_{EE} = –5.5V to –3.0V; V_{CC} = 0V; T_A = -40˚C to +85˚C, unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Current	I_{EE}	—	21	26	mA	—
Output High Voltage (Note 2)	V_{OH}	V_{CC} - 1.085	—	V_{CC} - 0.88	V	—
Output Low Voltage (Note 2)	V_{OL}	V_{CC} - 1.830	—	V_{CC} - 1.555	V	—
Input High Voltage (Single-Ended)	V_{IH}	V_{CC} - 1.165	—	V_{CC} - 0.880	V	—
Input Low Voltage (Single-Ended)	V_{IL}	V_{CC} - 1.810	—	V_{CC} - 1.475	V	—
Output Reference Voltage	V_{BB}	V_{CC} - 1.38	—	V_{CC} - 1.26	V	—
Common Mode Range (Note 3)	V_{IHCMR}	V_{EE} + 2.0	—	V_{CC} - 0.4	V	—
Input High Current	I_{IH}	—	—	150	µA	—
Input Low Current	I_{IL}	0.5	—	—	µA	—

Note 1: Devices are designed to meet the DC specifications shown in the above table after thermal equilibration has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

2: Outputs are terminated through a 50Ω resistor to V_{CC} - 2.0V.

3: The CMR range is referenced to the most positive side of the differential input voltage. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between 150 mV and 1V.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.3V to 5.5V, V_{EE} = 0V or V_{EE} = –5.5V to –3.0V; V_{CC} = 0V; T_A = -40˚C to +85˚C, unless otherwise stated. R_L = 50Ω to V_{CC} - 2.0V

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Frequency	f_{MAX}	1.0	—	—	GHz	V_{OUT} ≥ 400 mV
Propagation Delay D to Q (Differential)	t_{PLH}, t_{PHL}	125	250	375	ps	—
Propagation Delay D to Q (Single-Ended)	t_{PLH}, t_{PHL}	75	250	425	ps	—
Duty Cycle Skew (Note 1)	t_{SKEW}	—	5	20	ps	—
Input Swing (Note 2)	V_{PP}	150	—	1000	mV	—
Output Rise/Fall Time Q (20% to 80%)	t_r/t_f	100	225	350	ps	—

Note 1: Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.

2: Input swing for which AC parameters are ensured. The device has a DC gain of ≈40.

TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	–40	—	+85	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, 20 sec.
Package Thermal Resistance (DFN)						
Junction-to-Ambient	θ_{JA}	—	93	—	°C/W	Still-Air
		—	87	—		500 lfpm
Junction-to-Case	θ_{JC}	—	45	—	°C/W	—

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Type	Description
2, 3	D, /D	100K ECL Input	Differential PECL/ECL Input: The signal inputs include internal 75 kΩ pull-down resistors. If inputs are left open, Q output will default to LOW. See **Section 3.0 "Input Interface Application"** for single-ended inputs.
7, 6	Q, /Q	100K ECL Output	Differential PECL/ECL Output: Q output defaults to LOW if D inputs left open. See **Section 4.0 "Termination Recommendations"** for recommendations on terminations.
8	VCC	Positive Power Supply	Positive Power Supply: Bypass with 0.1 µF//0.01 µF low ESR capacitors.
5	VEE Exposed Pad	Negative Power Supply	Negative Power Supply: VEE and exposed pad must be tied to most negative supply. For PECL/LVPECL connect to ground.
4	VBB	Reference Voltage Output	Bias Voltage: V_{CC} - 1.32V. Used as reference voltage when AC coupling to the D, /D inputs. Max sink/source is ±0.5 mA.
1	NC	—	No connection.

3.0 INPUT INTERFACE APPLICATION

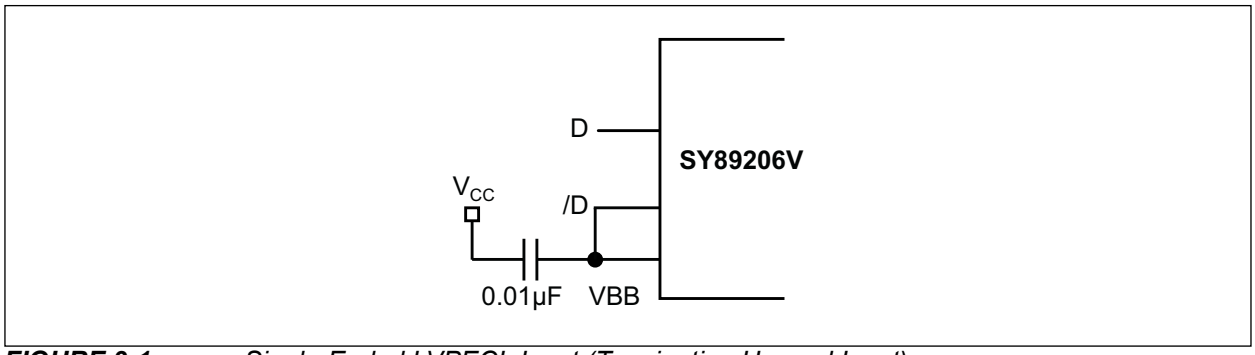


FIGURE 3-1: *Single-Ended LVPECL Input (Terminating Unused Input).*

4.0 TERMINATION RECOMMENDATIONS

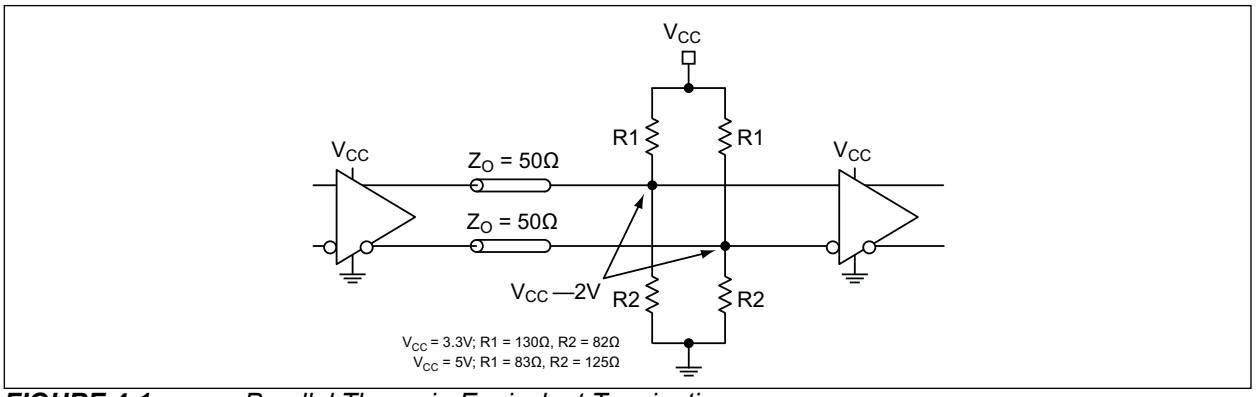


FIGURE 4-1: *Parallel Thevenin-Equivalent Termination.*

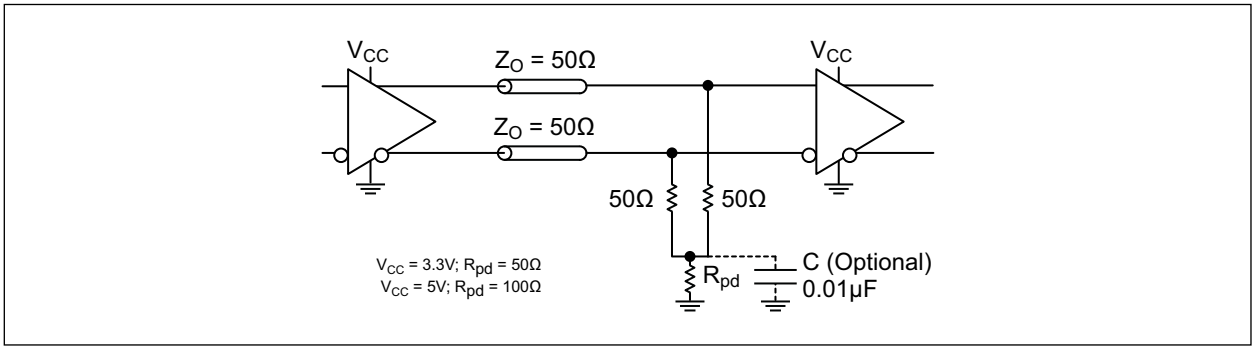


FIGURE 4-2: *Three Resistor Y -Termination.*

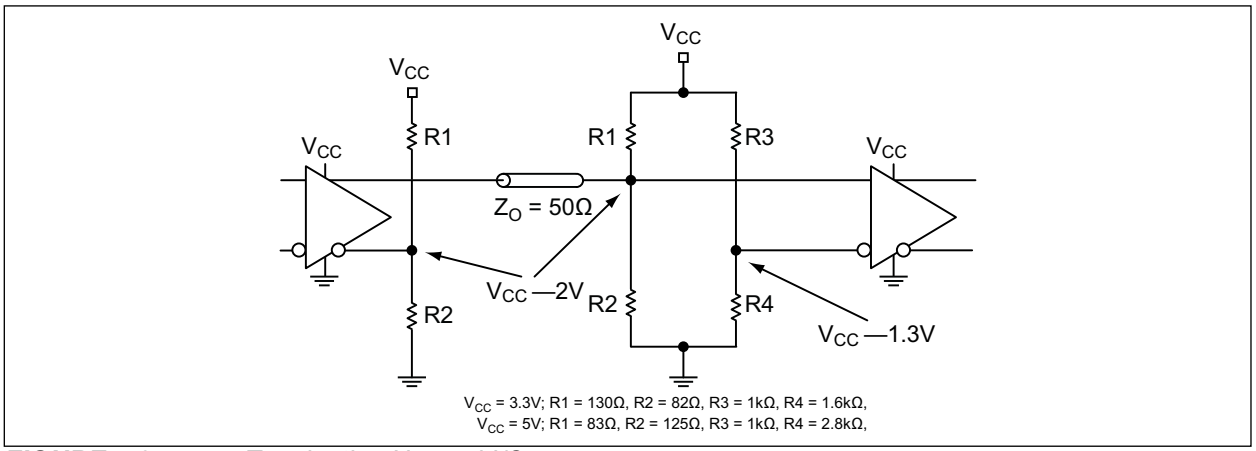
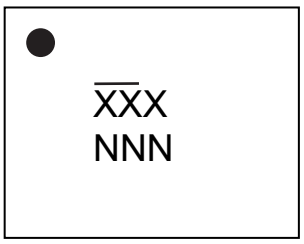


FIGURE 4-3: *Terminating Unused I/O.*

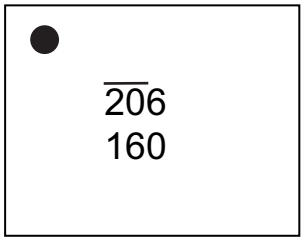
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

8-Lead VDFN*



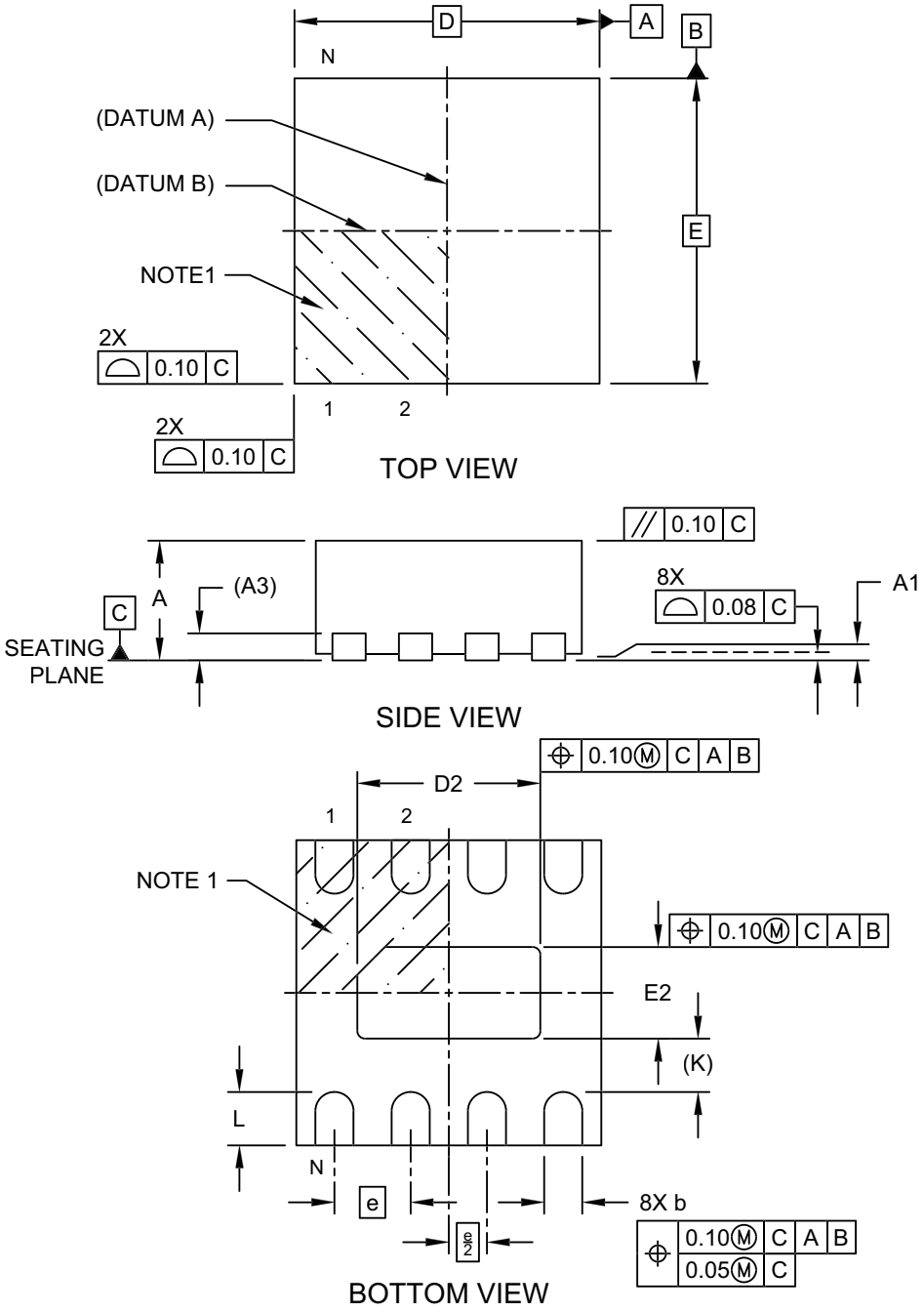
Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (‾) symbol may not be to scale.	

8-Lead Very Thin Plastic Dual Flat, No Lead Package (6XW) - 2x2x1.0 mm Body [VDFN] With 1.20x0.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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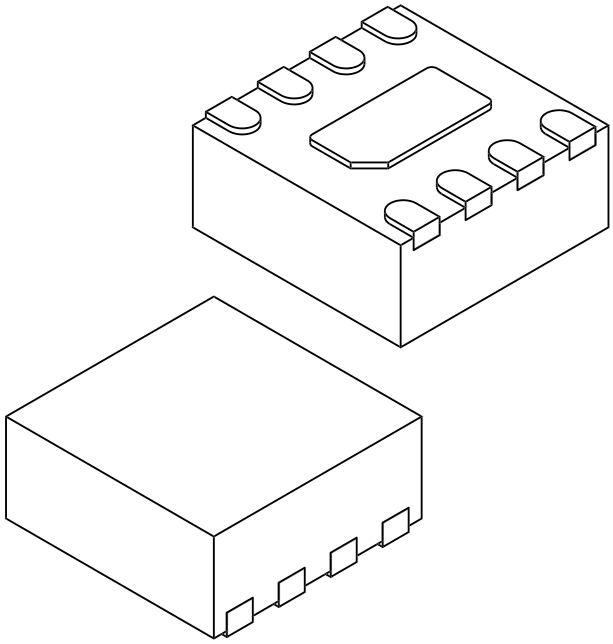
8-Lead Very Thin Plastic Dual Flat, No Lead Package (6XW) - 2x2x1.0 mm Body [VDFN] With 1.20x0.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.10	1.20	1.30
Overall Width	E		2.00 BSC	
Exposed Pad Width	E2	0.50	0.60	0.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.35	0.40
Terminal-to-Exposed-Pad	K		0.35 REF	

Notes:

1. Pin 1 visual index feature may vary but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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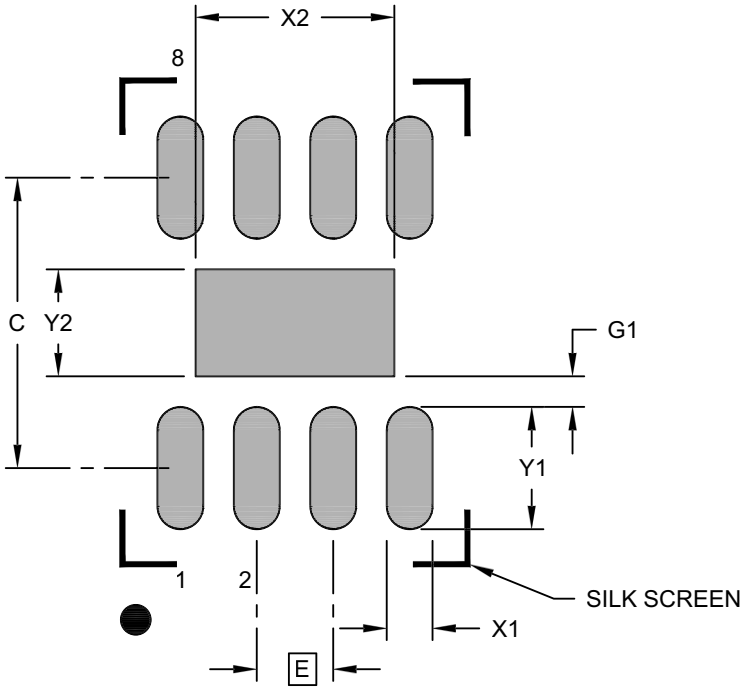
8-Lead Very Thin Plastic Dual Flat, No Lead Package (6XW) - 2x2x1.0 mm Body [VDFN] With 1.20x0.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			1.30
Optional Center Pad Length	Y2			0.70
Contact Pad Spacing	C		1.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X8)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, please refer to current industry standard IPC-7093

Microchip Technology Drawing C04-02637 Rev. B

APPENDIX A: REVISION HISTORY

Revision A (June 2019)

- Converted Micrel document SY89206V to Microchip data sheet DS20006210A.
- Minor text changes throughout.
- Removed all reference to the EOL SY89216V.
- Updated DC and AC parameter tables in the **1.0 "Electrical Characteristics"** section.

Revision B (August 2019)

- Updated minimum value for Common Mode Range in DC Electrical Characteristics (Note 1).

Revision C (July 2025)

- Updated the package outline drawing and changed all instances of DFN to VDFN.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XX
Device	Voltage Option	Package	Temperature Range	Special Processing

Device:	SY89206:	1 GHz Differential PECL/ECL Receiver/Buffer	
Voltage Option:	V	=	3.3V, 5V
Package:	M	=	8-Lead VDFN
Temperature Range:	G	=	–40°C to +85°C (NiPdAu Pb-Free)
Special Processing:	TR	=	1,000/Reel

Examples:

a) SY89206VMG-TR: 1 GHz Differential PECL/ECL Receiver/Buffer, 3.3V/5V, –40°C to +85°C, 8-Lead VDFN, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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