

TC74ACT138FN

3-to-8 Line Decoder

The TC74ACT138 is an advanced high speed CMOS 3-to-8 LINE DECODER fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

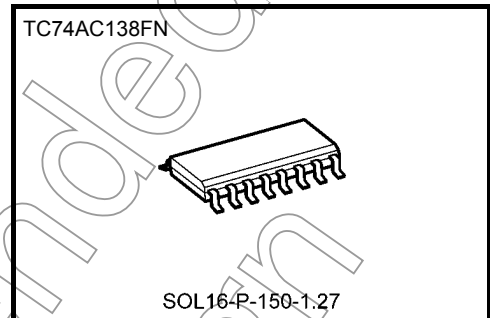
When the device is enabled, 3 Binary Select inputs (A, B and C) determine which one of the outputs ($\bar{Y}_0 - \bar{Y}_7$) will go low.

When enable input G1 is held low or either $\bar{G}_2A$ or $\bar{G}_2B$ is held high, decoding function is inhibited and all outputs go high.

G1, $\bar{G}_2A$, and $\bar{G}_2B$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Note: xxxFN (JEDEC SOP) is not available in Japan.

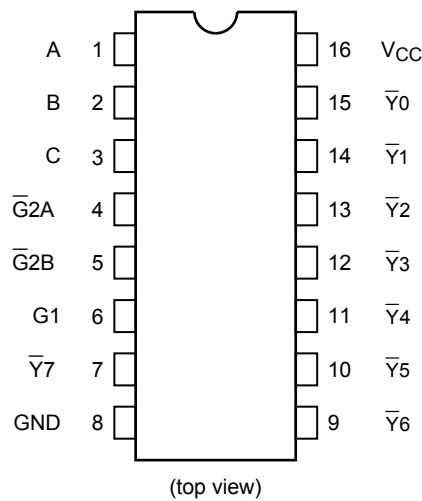


Weight
SOL16-P-150-1.27 : 0.13 g (typ.)

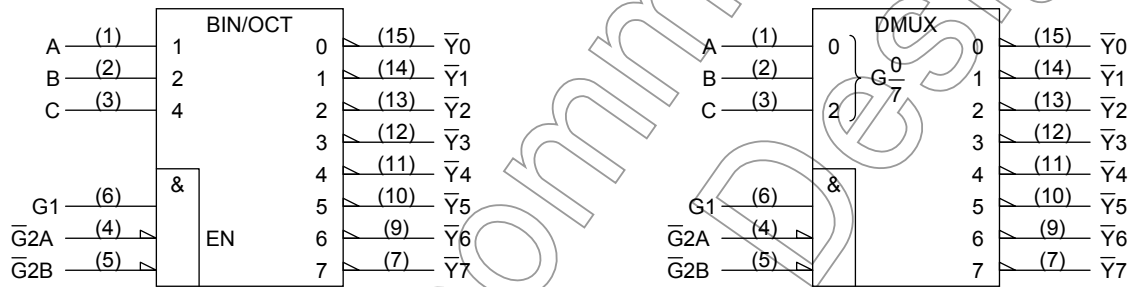
Features

- High speed: $t_{pd} = 6.0 \text{ ns (typ.)}$ at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 8 \mu\text{A (max)}$ at $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs: $V_{IL} = 0.8 \text{ V (max)}$
 $V_{IH} = 2.0 \text{ V (min)}$
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 24 \text{ mA (min)}$
Capability of driving 50Ω transmission lines.
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- Pin and function compatible with 74F138

Pin Assignment



IEC Logic Symbol

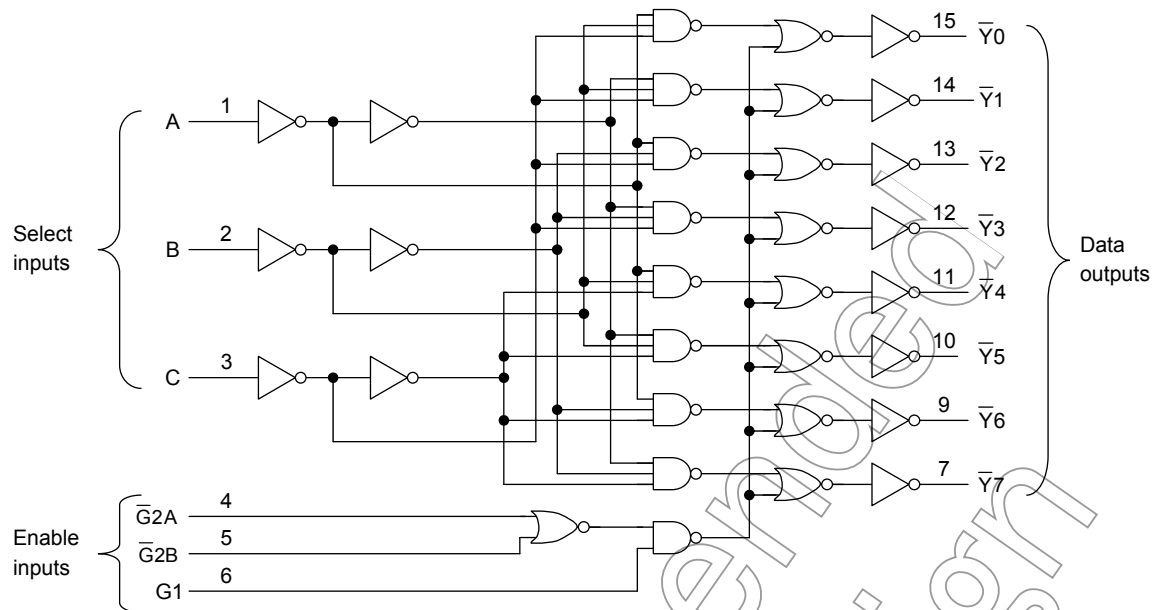


Truth Table

Inputs						Outputs								Selected Output
Enable			Select			$\bar{Y}0$	$\bar{Y}1$	$\bar{Y}2$	$\bar{Y}3$	$\bar{Y}4$	$\bar{Y}5$	$\bar{Y}6$	$\bar{Y}7$	
G1	$\bar{G}2A$	$\bar{G}2B$	C	B	A									
L	X	X	X	X	X	H	H	H	H	H	H	H	H	None
X	H	X	X	X	X	H	H	H	H	H	H	H	H	None
X	X	H	X	X	X	H	H	H	H	H	H	H	H	None
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\bar{Y}0$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\bar{Y}1$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\bar{Y}2$
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\bar{Y}3$
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\bar{Y}4$
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\bar{Y}5$
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\bar{Y}6$
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\bar{Y}7$

X: Don't care

Logic Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 50	mA
DC output current	I_{OUT}	± 50	mA
DC V_{CC} /ground current	I_{CC}	± 200	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dV	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
			V _{CC} (V)	Min	Typ.	Max	Min	Max	
High-level input voltage	V _{IH}	—	4.5 to 5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V _{IL}	—	4.5 to 5.5	—	—	0.8	—	0.8	V
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 µA I _{OH} = -24 mA I _{OH} = -75 mA (Note)	4.5	4.4	4.5	—	4.4	—	V
			4.5	3.94	—	—	3.80	—	
			5.5	—	—	—	3.85	—	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 µA I _{OL} = 24 mA I _{OL} = 75 mA (Note)	4.5	—	0.0	0.1	—	0.1	V
			4.5	—	—	0.36	—	0.44	
			5.5	—	—	—	—	1.65	
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND	5.5	—	—	±0.1	—	±1.0	µA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	8.0	—	80.0	µA
	I _C	Per input: V _{IN} = 3.4 V Other input: V _{CC} or GND	5.5	—	—	1.35	—	1.5	mA

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

AC Characteristics (C_L = 50 pF, R_L = 500 Ω, input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
			V _{CC} (V)	Min	Typ.	Max	Min	Max	
Propagation delay time (A, B, C- $\bar{Y}$)	t _{pLH}	—	5.0 ± 0.5	—	6.7	10.1	1.0	11.5	ns
	t _{pHL}	—	5.0 ± 0.5	—	6.8	10.5	1.0	12.0	
Propagation delay time (G1- $\bar{Y}$)	t _{pLH}	—	5.0 ± 0.5	—	6.8	10.5	1.0	12.0	ns
	t _{pHL}	—	5.0 ± 0.5	—	6.9	11.0	1.0	12.5	
Propagation delay time ($\bar{G}2$ - $\bar{Y}$)	t _{pLH}	—	5.0 ± 0.5	—	6.9	11.0	1.0	12.5	ns
	t _{pHL}	—	5.0 ± 0.5	—	6.9	11.0	1.0	12.5	
Input capacitance	C _{IN}	—	—	—	5	10	—	10	pF
Power dissipation capacitance	C _{PD}	(Note)	—	—	55	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

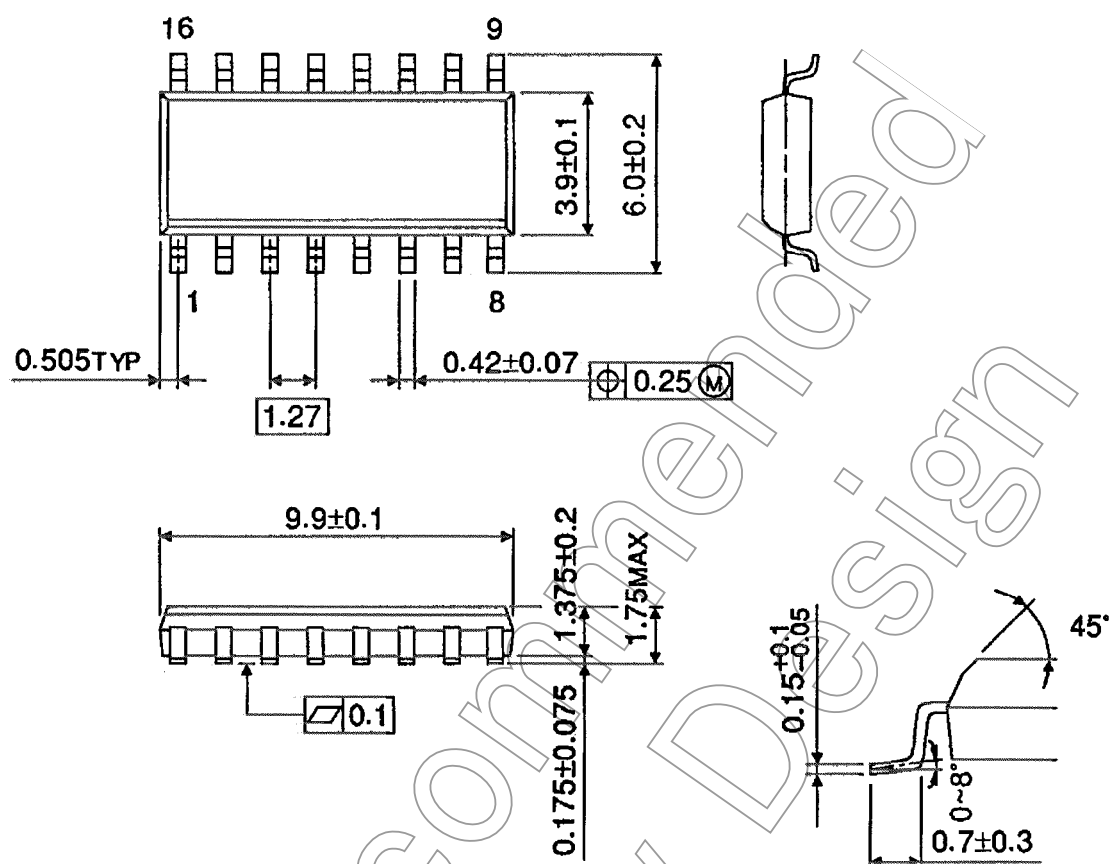
Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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