

MOSFET - Power, DUAL COOL® N-Channel, PQFN8 150 V, 11.4 mΩ, 80 A NTMFSC012N15MC

Features

- Advanced Dual-sided Cooled Packaging
- Ultra Low $R_{DS(on)}$
- MSL1 Robust Packaging Design

Typical Applications

- Primary DC-DC FET
- Synchronous Rectifier
- DC-DC Conversion

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V _{DSS}	150	V
Gate-to-Source Voltage		V _{GS}	±20	V
Continuous Drain Current R _{θJC} (Notes 1, 3)	Steady State	T _C = 25°C	I _D	80
		T _C = 100°C		50
Power Dissipation R _{θJC} (Note 1)		T _C = 25°C	P _D	147
		T _C = 100°C		58
Continuous Drain Current R _{θJA} (Notes 1, 2, 3)	Steady State	T _A = 25°C	I _D	10
		T _A = 100°C		6
Power Dissipation R _{θJA} (Notes 1, 2)		T _A = 25°C	P _D	2.7
		T _A = 100°C		1
Pulsed Drain Current	T _C = 25°C, t _p = 10 µs	I _{DM}	1067	A
Operating Junction / Storage Temperature Max		T _J , T _{stg}	+150	°C
Source Current (Body Diode)		I _S	122	A
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 35 A)		E _{AS}	161	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)		T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

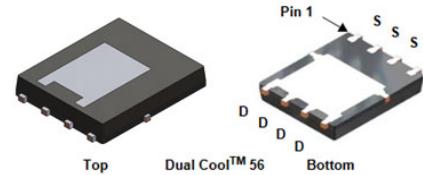
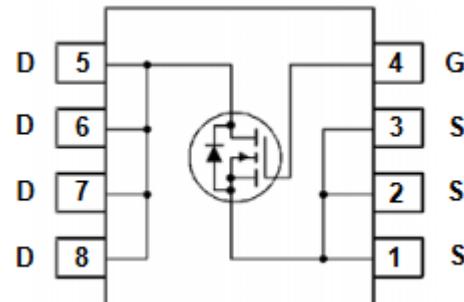
THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	R _{θJC}	0.85	°C/W
Junction-to-Case Top - Steady State	R _{θJT}	1.5	
Junction-to-Ambient - Steady State (Note 2)	R _{θJA}	46	

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
- Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

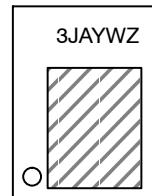
V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
150 V	11.4 mΩ @ 10 V	44 A
	14.5 mΩ @ 8 V	22 A

N-CHANNEL MOSFET



DFN8 5x6.15
CASE 506EG

MARKING DIAGRAM



3J = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
Z = Assembly Lot Code

ORDERING INFORMATION

Device	Package	Shipping [†]
NTMFSC012N15MC	PQFN8 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMFSC012N15MC

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	150				V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	I _D = 250 μA, ref to 25°C		6.9			mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 150 V	T _J = 25°C		1		μA
			T _J = 125°C			100	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 194 μA	2.5		4.5		V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J	I _D = 194 μA, ref to 25°C		8			mV/°C
Drain-to-Source On Resistance	R _{DSS(on)}	V _{GS} = 10 V	I _D = 44 A		8.9	11.4	mΩ
		V _{GS} = 8 V	I _D = 22 A		9.5	14.5	
Gate-Resistance	R _G	T _A = 25°C			0.7		Ω
CHARGES & CAPACITANCES							
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 75 V		2490			pF
Output Capacitance	C _{OSS}			676			
Reverse Transfer Capacitance	C _{rss}			9.0			
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 6 V, V _{DS} = 75 V, I _D = 44 A		20.4			nC
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 75 V, I _D = 44 A		32.4			
Gate-to-Source Charge	Q _{GS}			13.9			
Gate-to-Drain Charge	Q _{GD}			5.5			
Plateau Voltage	V _{GP}			5.7			V

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 75 V, I _D = 44 A, R _G = 2.5 Ω		18.4		ns
Rise Time	t _r			3.7		
Turn-Off Delay Time	t _{d(OFF)}			21.3		
Fall Time	t _f			3		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 44 A	T _J = 25°C		0.88		V
			T _J = 125°C		0.76		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 1000 A/μs, I _S = 44 A			42.7		ns
Reverse Recovery Charge	Q _{RR}				559		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

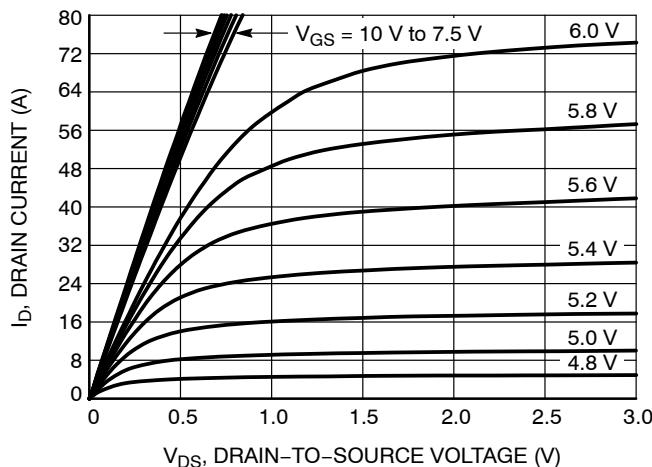


Figure 1. On-Region Characteristics

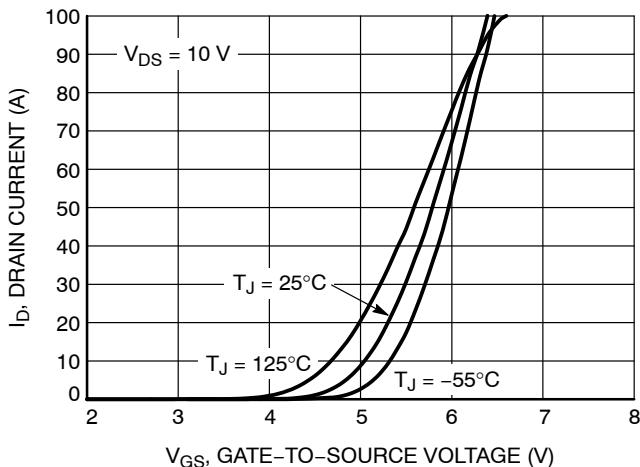


Figure 2. Transfer Characteristics

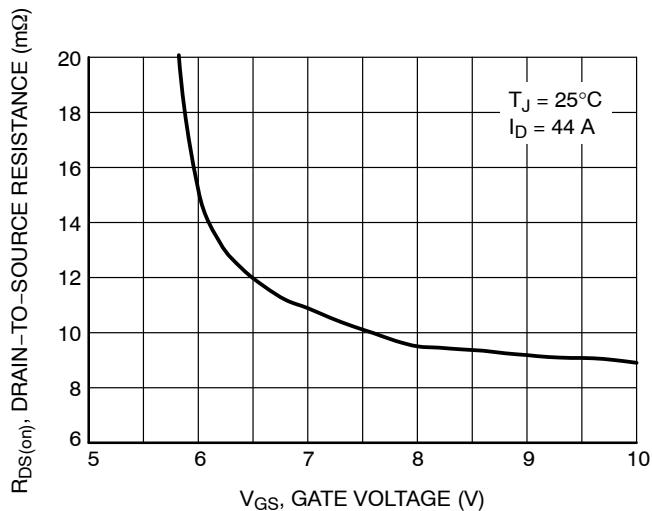


Figure 3. On-Resistance vs. Gate-to-Source Voltage

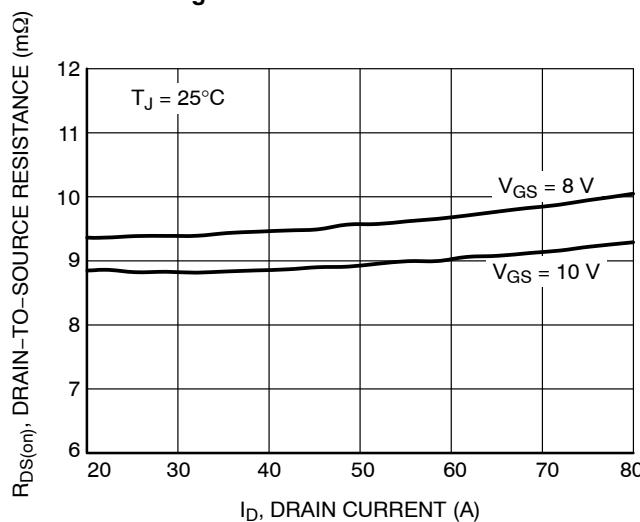


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

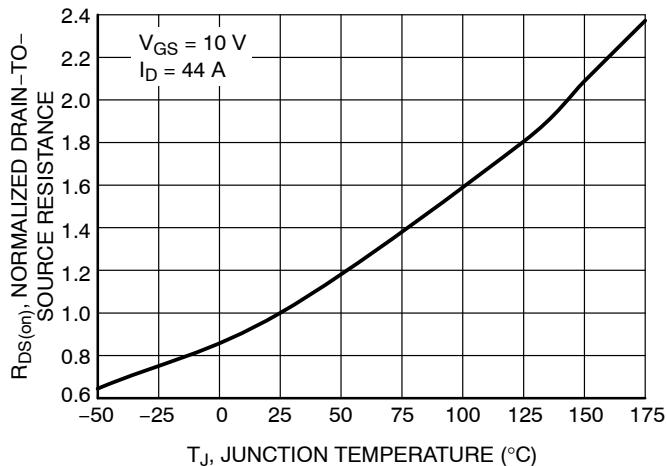


Figure 5. On-Resistance Variation with Temperature

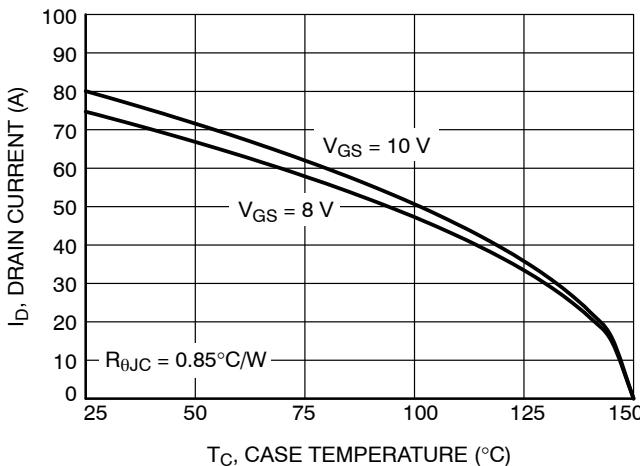


Figure 6. Maximum Continuous Drain Current vs. Case Temperature

TYPICAL CHARACTERISTICS

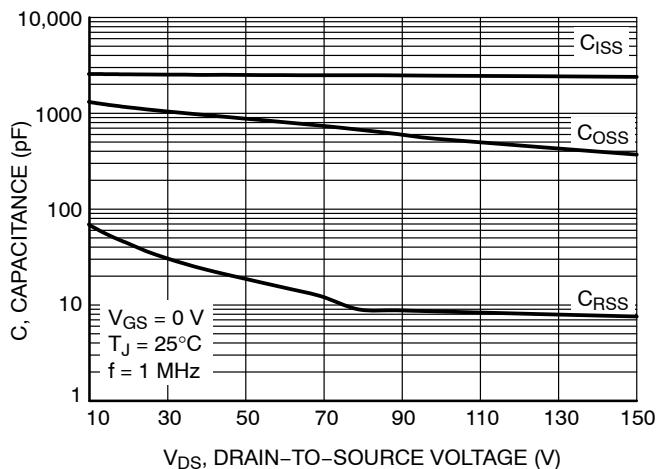


Figure 7. Capacitance Variation

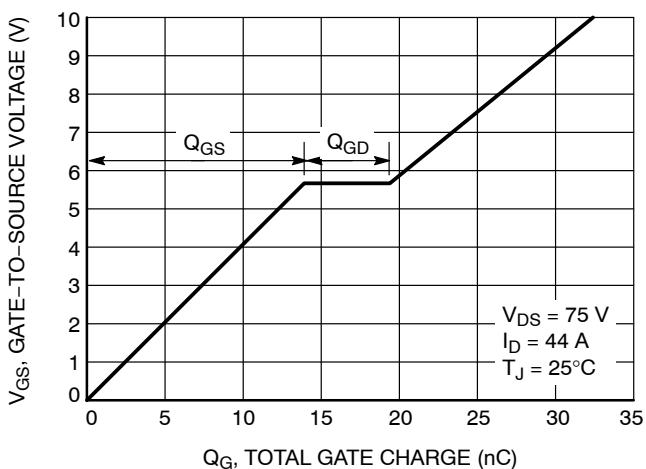


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

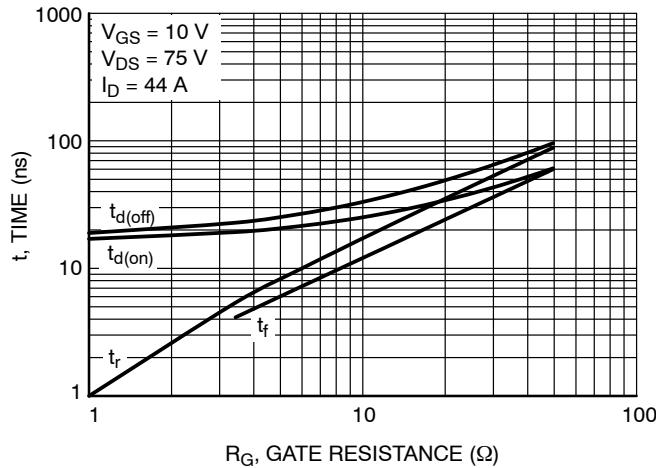


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

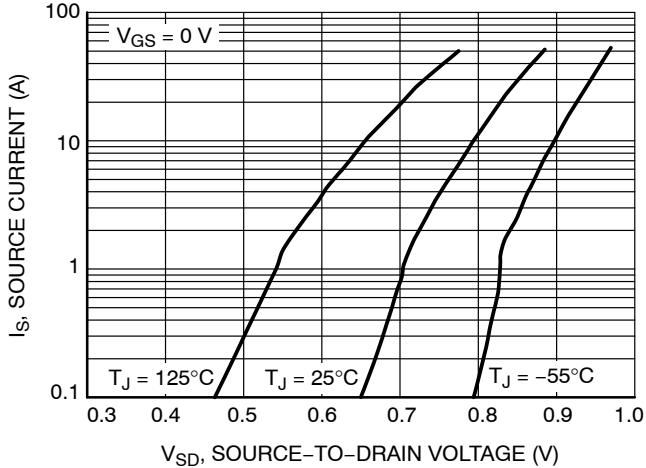


Figure 10. Diode Forward Voltage vs. Current

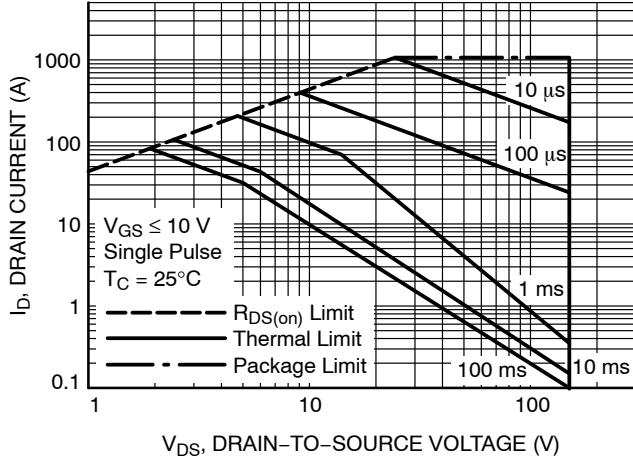
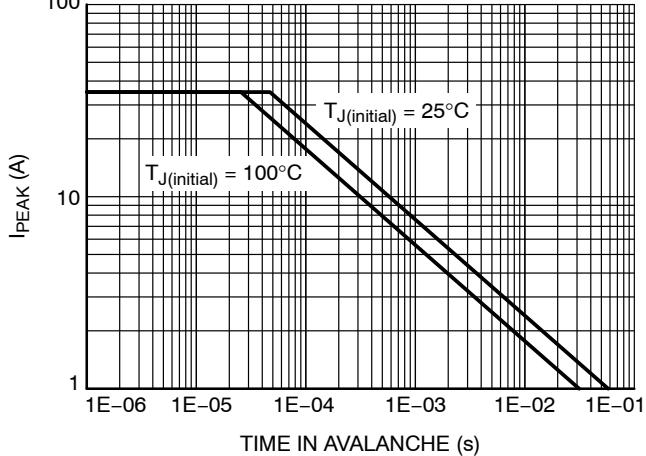


Figure 11. Safe Operating Area

Figure 12. I_{PEAK} vs. Time in Avalanche

NTMFSC012N15MC

TYPICAL CHARACTERISTICS

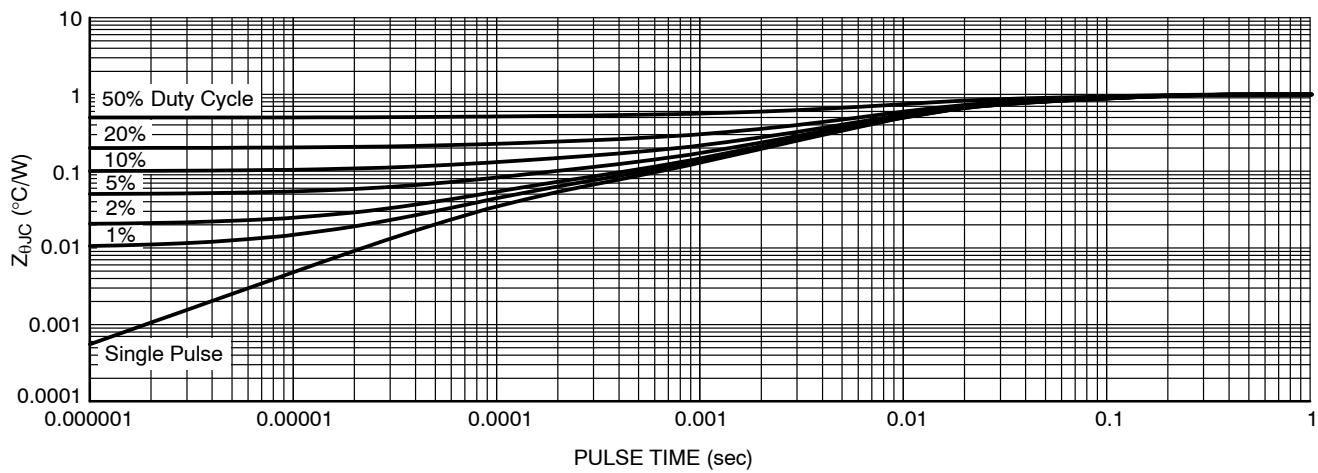


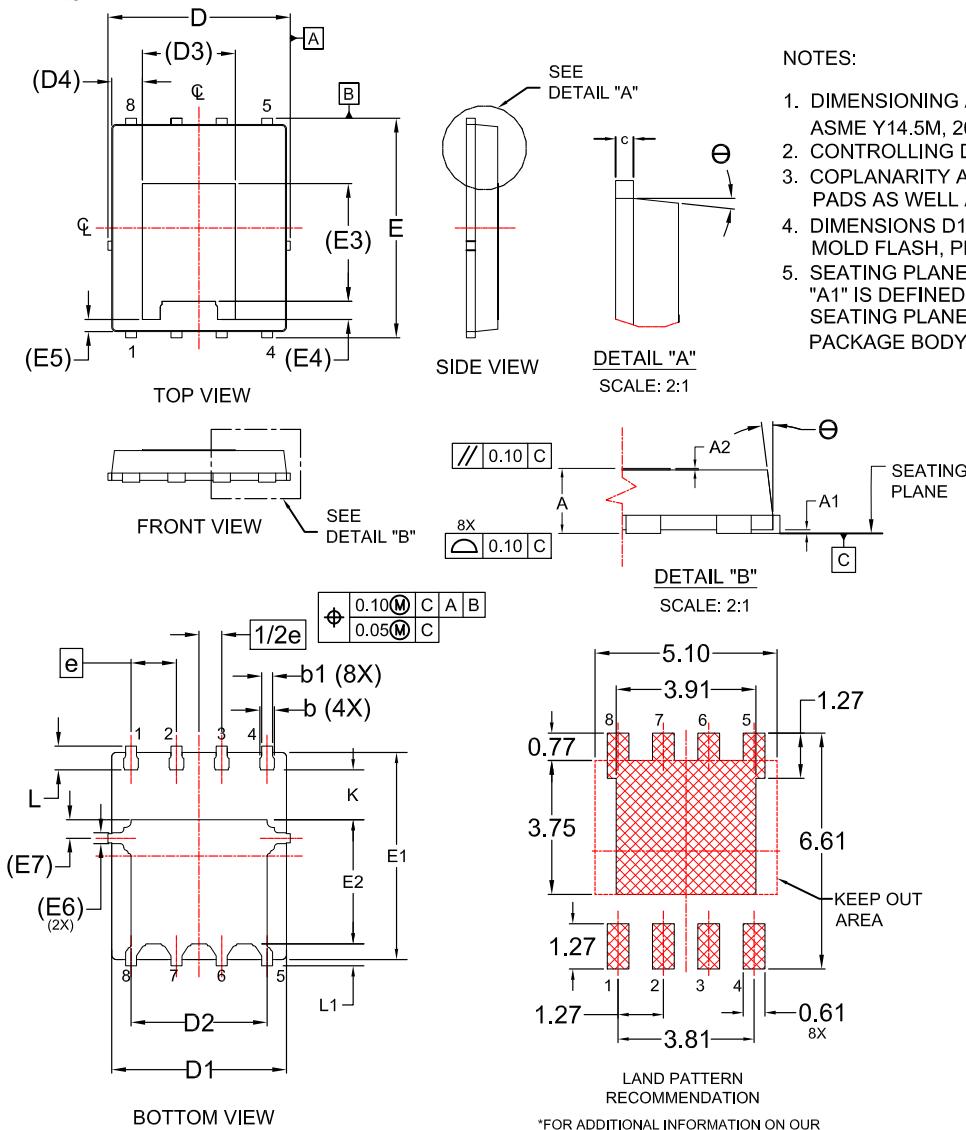
Figure 13. Thermal Characteristics

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DFN8 5x6.15, 1.27P, DUAL COOL
CASE 506EG
ISSUE D

DATE 25 AUG 2020



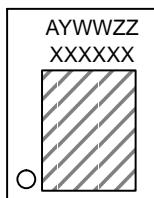
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
Θ	0°	---	12°

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SODERRM/D.

**GENERIC
MARKING DIAGRAM***



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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