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DATA SHEET
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SyncFET™ – N-Channel, POWERTRENCH®

30 V, 42 A, 4.9 mΩ

FDMS0312S

V_{DS} MAX	$r_{DS(on)}$ MAX	I_D MAX
30 V	4.9 mΩ @ 10 V	42 A
	5.8 mΩ @ 4.5 V	

General Description

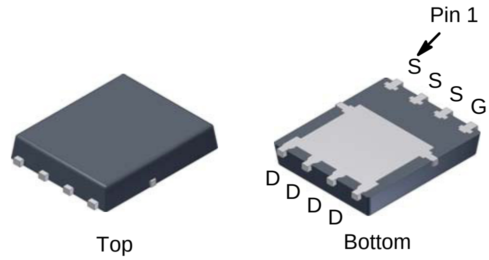
The FDMS0312S has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

Features

- Max $r_{DS(on)}$ = 4.9 mΩ at V_{GS} = 10 V, I_D = 18 A
- Max $r_{DS(on)}$ = 5.8 mΩ at V_{GS} = 4.5 V, I_D = 14 A
- Advanced Package and Silicon Combination for Low $r_{DS(on)}$ and High Efficiency
- SyncFET Schottky Body Diode
- MSL1 Robust Package Design
- 100% UIL Tested
- This Device is Pb−Free, Halide Free and is RoHS Compliant

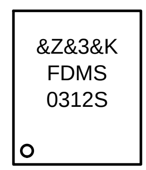
Applications

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/GPU Low Side Switch
- Networking Point of Load Low Side Switch
- Telecom Secondary Side Rectification



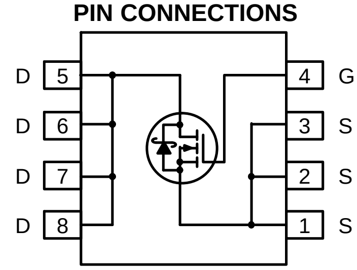
PQFN8 5X6, 1.27P
(Power 56)
CASE 483AE

MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = 3−Digit Date Code
&K = 2−Digits Lot Run Code
FDMS0312S = Specific Device Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

MOSFET MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage (Note 4)	±20	V
I_D	Drain Current − Continuous (Package Limited) T_C = 25°C − Continuous (Silicon Limited) T_C = 25°C − Continuous T_A = 25°C (Note 1a) − Pulsed	 42 83 19 90	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	60	mJ
P_D	Power Dissipation T_C = 25°C T_A = 25°C (Note 1a)	 46 2.5	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

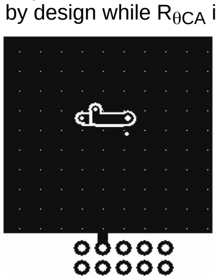
Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.7	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

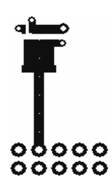
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, referenced to 25°C	–	18	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	–	–	500	μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 1 mA	1.2	1.9	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 10 mA, referenced to 25°C	–	−5	–	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 18 A	–	3.6	4.9	mΩ
		V_{GS} = 4.5 V, I_D = 14 A	–	4.7	5.8	
		V_{GS} = 10 V, I_D = 18 A, T_J = 125°C	–	5	6.2	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 18 A	–	97	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	–	2120	2820	pF
C_{oss}	Output Capacitance		–	735	975	pF
C_{rss}	Reverse Transfer Capacitance		–	90	135	pF
R_g	Gate Resistance		–	1.1	2.2	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 15 V, I_D = 18 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	12	21	ns
t_r	Rise Time		–	5	10	ns
$t_{d(off)}$	Turn−Off Delay Time		–	28	44	ns
t_f	Fall Time		–	4	10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 15 V, I_D = 18 A	–	33	46	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V, V_{DD} = 15 V, I_D = 18 A	–	15	22	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 15 V, I_D = 18 A	–	6.5	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	4.0	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)	–	0.48	0.7	V
		V_{GS} = 0 V, I_S = 18 A (Note 2)	–	0.80	1.2	
t_{rr}	Reverse Recovery Time	I_F = 18 A, di/dt = 300 A/μs	–	26	42	ns
Q_{rr}	Reverse Recovery Charge		–	26	42	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 60 mJ is based on starting T_J = 25°C, L = 1 mH, I_{AS} = 11 A, V_{DD} = 27 V, V_{GS} = 10 V. 100% test at L = 0.3 mH, I_{AS} = 16 A.
4. As an N−ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS

(T_J = 25°C UNLESS OTHERWISE NOTED)

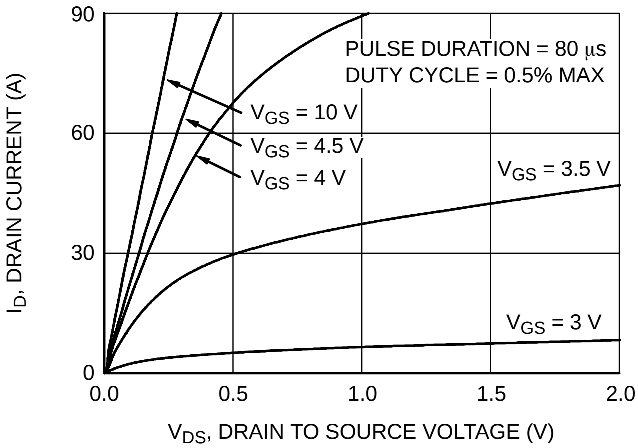


Figure 1. On−Region Characteristics

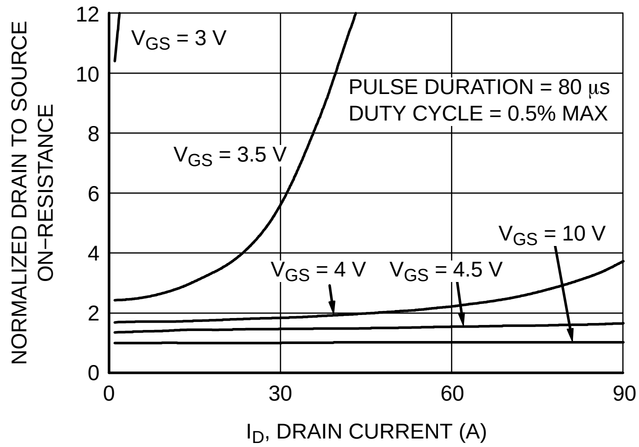


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

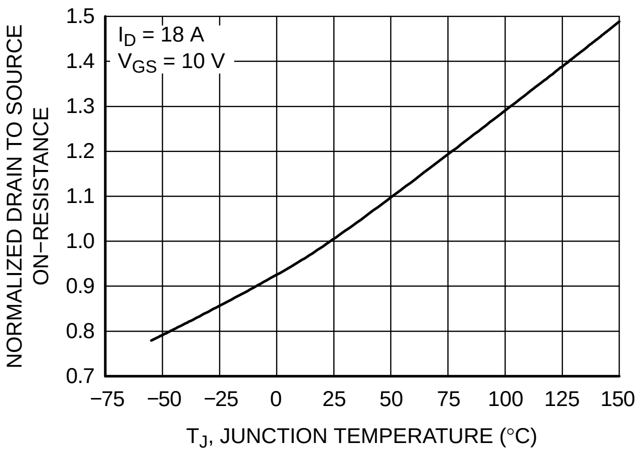


Figure 3. Normalized On−Resistance vs. Junction Temperature

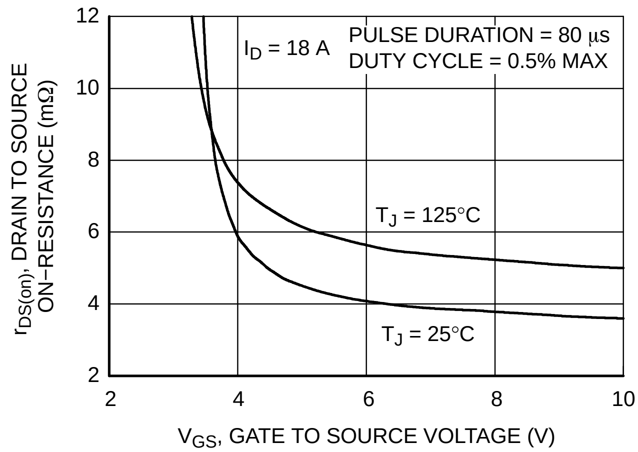


Figure 4. On−Resistance vs. Gate to Source Voltage

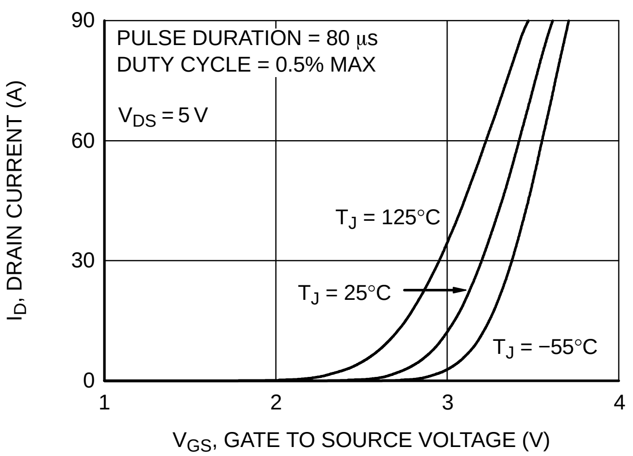


Figure 5. Transfer Characteristics

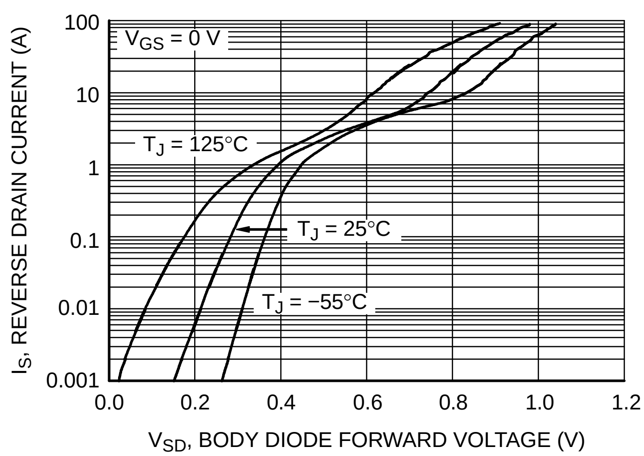


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS

(T_J = 25°C UNLESS OTHERWISE NOTED) (CONTINUED)

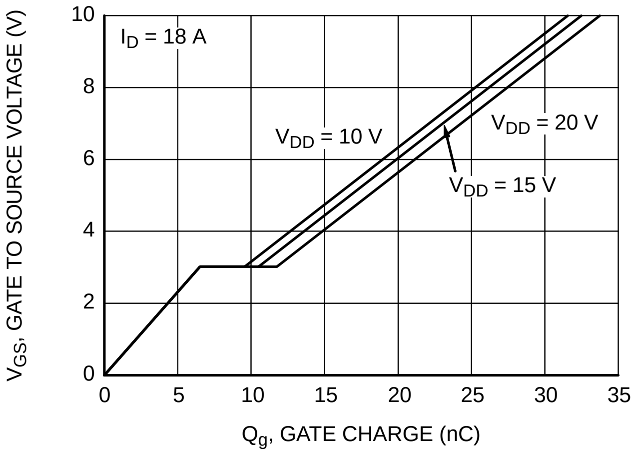


Figure 7. Gate Charge Characteristics

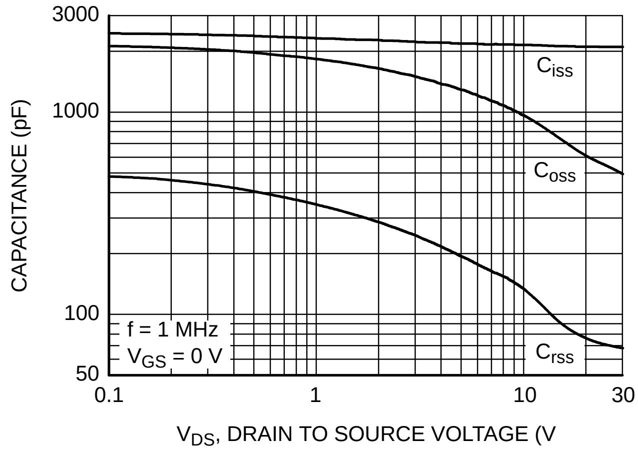


Figure 8. Capacitance vs. Drain to Source Voltage

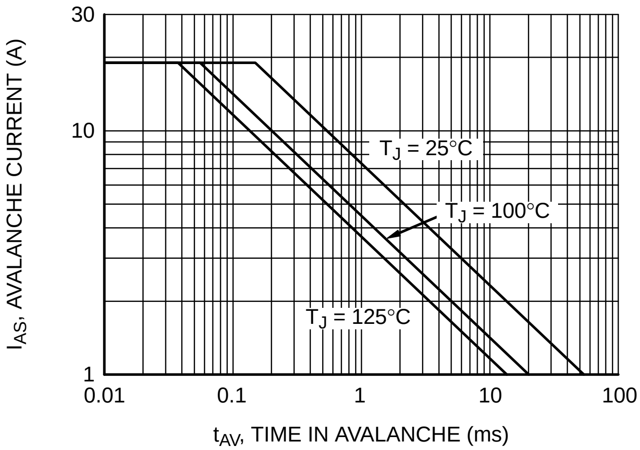


Figure 9. Unclamped Inductive Switching Capability

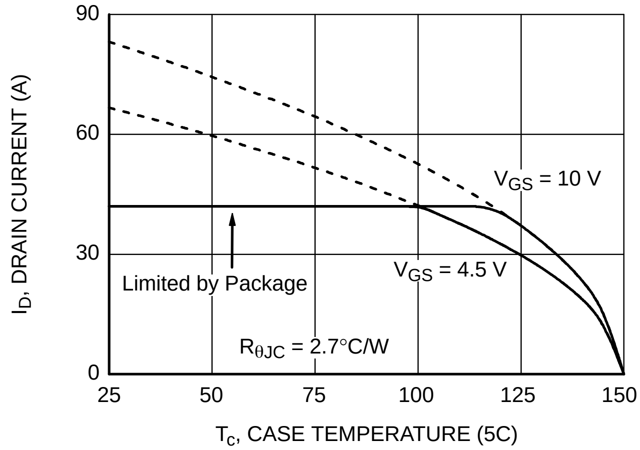


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

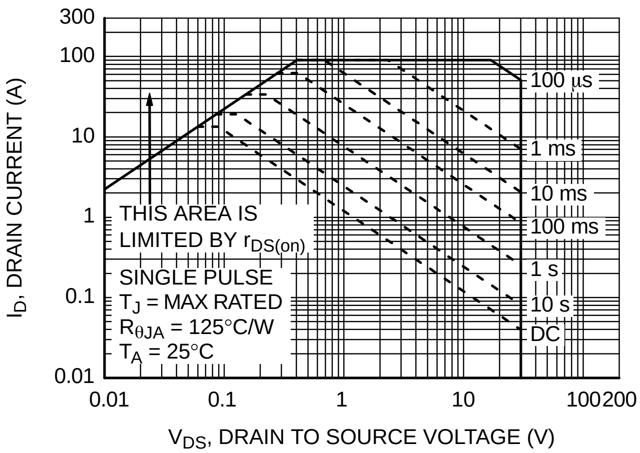


Figure 11. Forward Bias Safe Operating Area

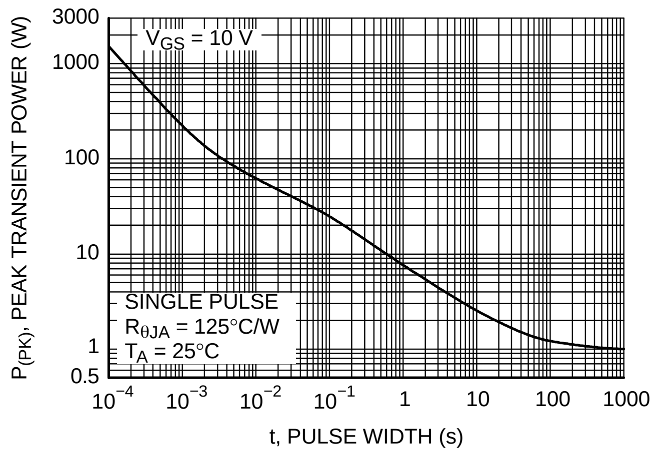


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

(T_J = 25°C UNLESS OTHERWISE NOTED) (CONTINUED)

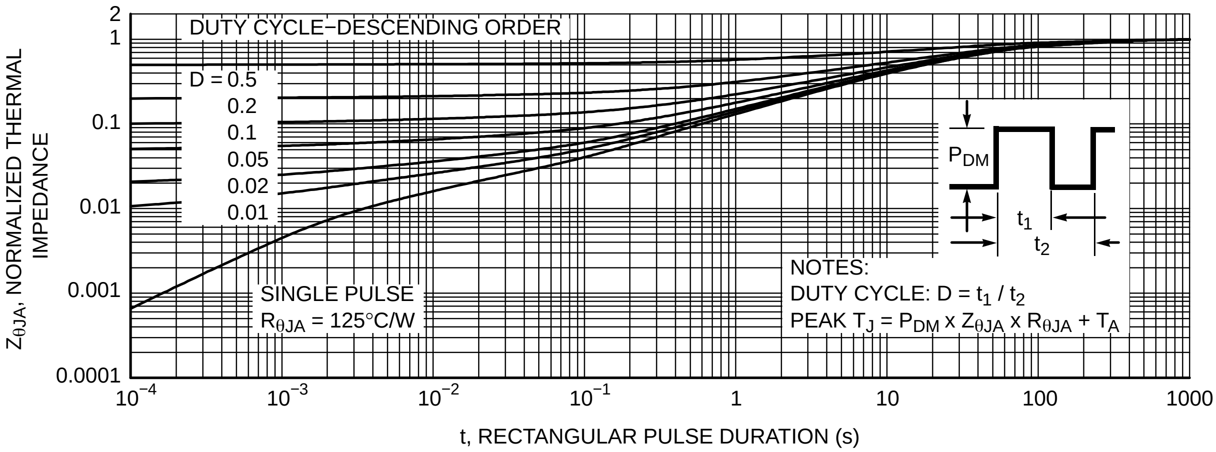


Figure 13. Junction−to−Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (CONTINUED)

SyncFET Schottky Body Diode Characteristics

onsemi's SyncFET process embeds a Schottky diode in parallel with POWERTRENCH MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverses recovery characteristic of the FDMS0312S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

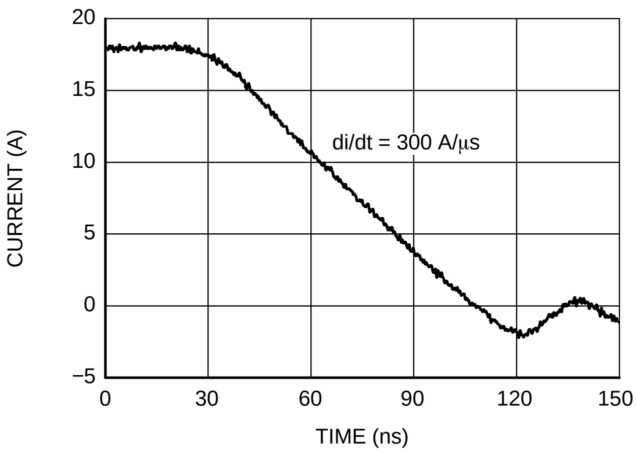


Figure 14. FDMS0312S SyncFET Body Diode Reverse Recovery Characteristic

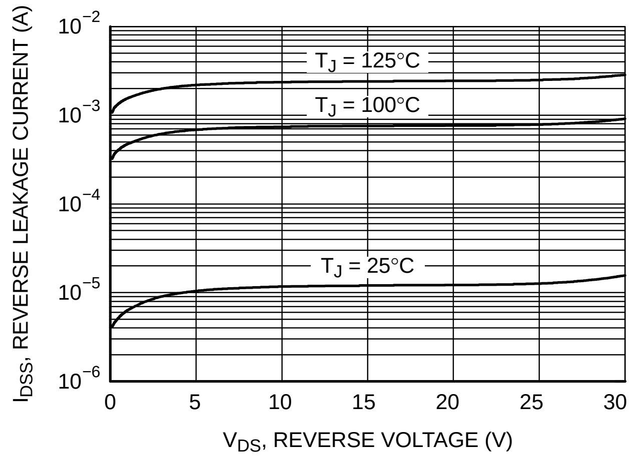
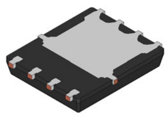


Figure 15. SyncFET Body Diode Reverses Leakage vs. Drain−Source Voltage

PACKAGE MARKING AND ORDERING INFORMATION

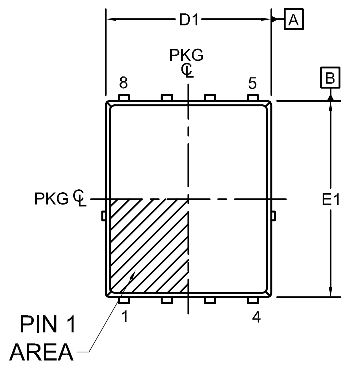
Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping†
FDMS0312S	FDMS0312S	PQFN8 5X6, 1.27P (Power 56) (Pb−Free, Halide Free)	13"	12 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

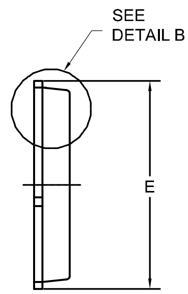


PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

DATE 21 JAN 2022



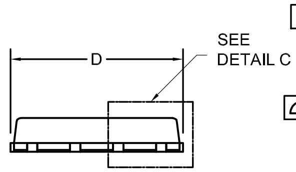
TOP VIEW



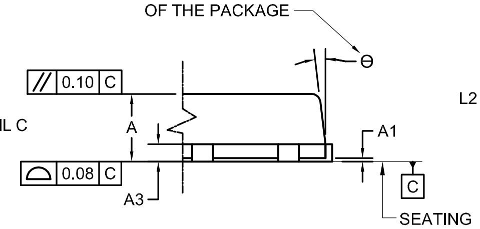
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

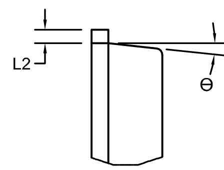
OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



SIDE VIEW

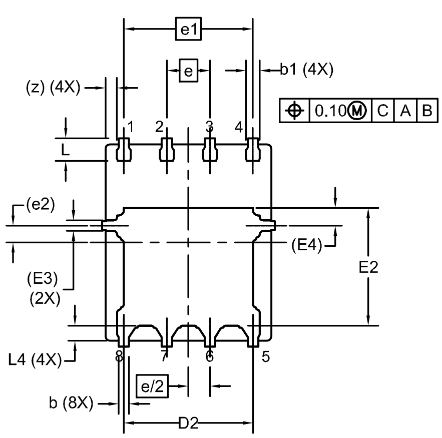


DETAIL C
SCALE: 2:1

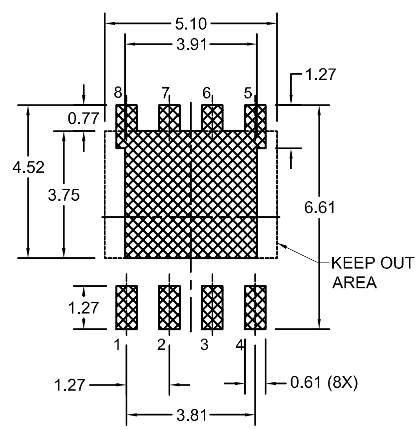


DETAIL B
SCALE: 2:1

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
Θ	0°	-	12°



BOTTOM VIEW



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	PQFN8 5X6, 1.27P	PAGE 1 OF 1

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