HIGH-FREQUENCY HALF-BRIDGE GATE DRIVER WITH PROGRAMMABLE DEADTIME

Description

The DGD0506A is a high-frequency half-bridge gate driver capable of driving n-channel MOSFETs in a half-bridge configuration. The floating high-side driver is rated up to 50V.

The DGD0506A logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with MCUs. UVLO for high-side and low-side will protect a MOSFET with loss of supply. To protect MOSFETs, cross conduction prevention logic prevents the HO and LO outputs from being on at the same time.

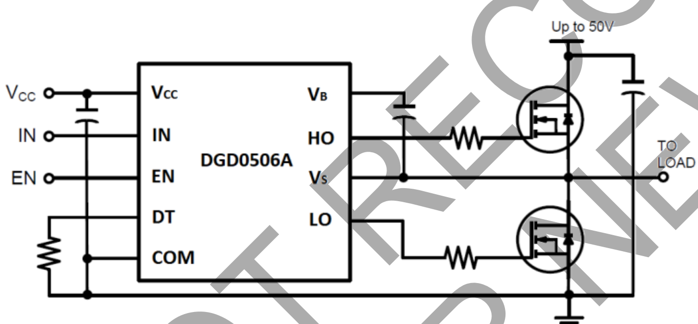
Fast and well-matched propagation delays allow a higher switching frequency, enabling a smaller, more compact power switching design using smaller associated components. The DGD0506A is offered in the W-DFN3030-10 (Type TH) and MSOP-10 packages and operates over an extended -40°C to +125°C temperature range.

Features

- 50V Floating High-Side Driver
- Drives Two N-Channel MOSFETs in a Half-Bridge Configuration
- 1.5A Source/2.0A Sink Output Current Capability
- Internal Bootstrap Diode Included
- Undervoltage Lockout for High-Side and Low-Side Drivers
- Programmable Deadtime to Protect MOSFETs
- Logic Input (IN and EN) 3.3V Capability
- Ultra-Low Standby Currents (< 1µA)
- Extended Temperature Range: -40°C to +125°C
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- DC-DC converters
- Motor control
- Battery-powered hand tools
- eCig devices
- Class D power amplifiers



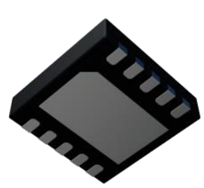
Typical Configuration

Mechanical Data

- Packages: W-DFN3030-10, MSOP-10
- Package Material: Molded Plastic. "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 (e3)
- Weight:
  - W-DFN3030-10 (Type TH): 0.017 grams (Approximate)
  - MSOP-10: 0.0286 grams (Approximate)

W-DFN3030-10 (Type TH)

Top View



Bottom View

MSOP-10

Top View

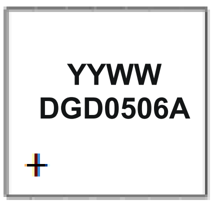
Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Ordering Information (Note 4)

Orderable Part Number	Package	Marking	Reel Size (inches)	Tape Width (mm)	Packing	
					Qty.	Carrier
DGD0506AFN-7	W-DFN3030-10 (Type TH)	DGD0506A	7	8	3,000	Reel
DGD0506AM10-13	MSOP-10	DGD0506A	13	12	2,500	Reel

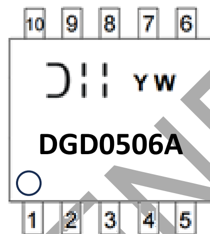
Note: 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



DGD0506A = Product Type Marking Code
YY = Year (ex: 25 = 2025)
WW = Week (01 to 53)

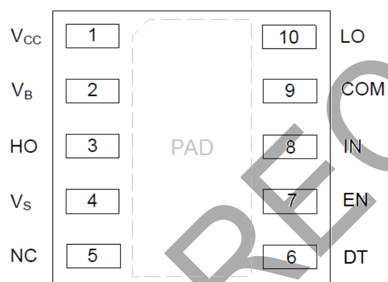
W-DFN3030-10 (Type TH)



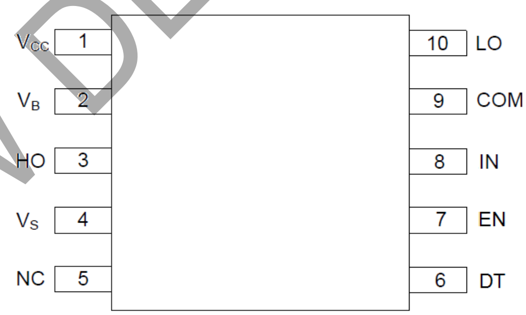
= Manufacturer's Marking
DGD0506A = Product Type Marking Code
Y = Year (ex: 5 = 2025)
W = Week (A to Z: week 1 to 26)
(a to z: week 27 to 52)

MSOP-10

Pin Diagrams



Top View: W-DFN3030-10 (Type TH)

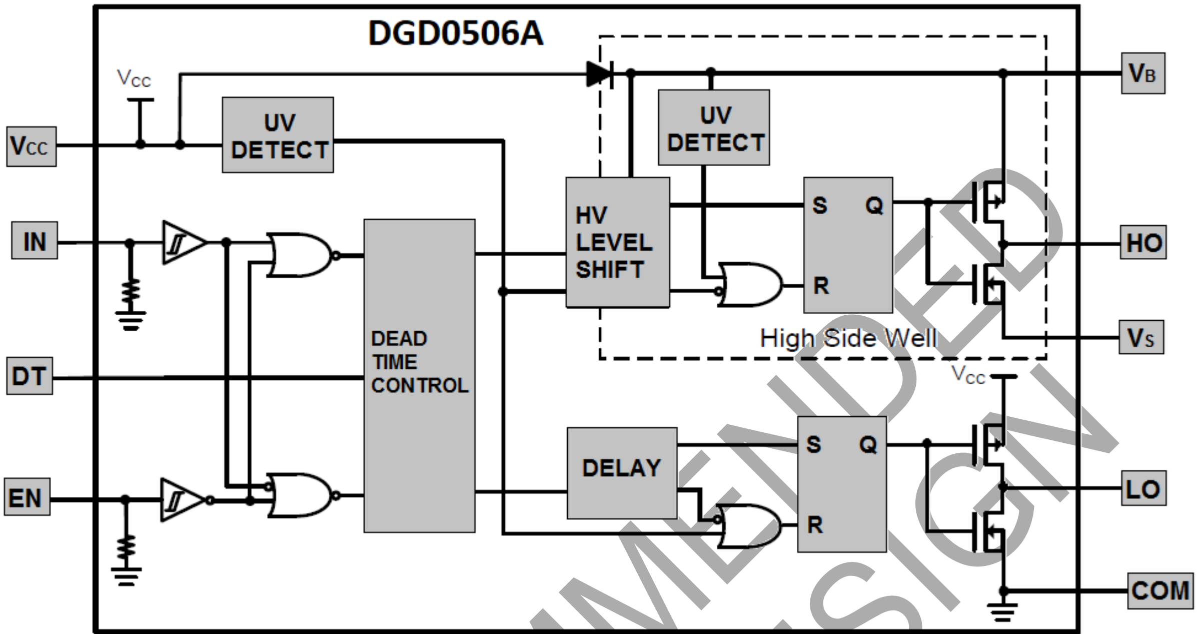


Top View: MSOP-10

Pin Descriptions

Pin Number	Pin Name	Function
1	V_{CC}	Low-Side and Logic Supply
2	V_B	High-Side Floating Supply
3	HO	High-Side Gate Drive Output
4	V_S	High-Side Floating Supply Return
5	NC	No Connect (No Internal Connection)
6	DT	Deadtime Control
7	EN	Logic Input Enable, a Logic Low turns off Gate Driver
8	IN	Logic Input for High-Side and Low-Side Gate Driver Outputs (HO and LO), in Phase with HO
9	COM	Low-Side and Logic Return
10	LO	Low-Side Gate Drive Output
PAD	Substrate	Connect to COM on PCB

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
High-Side Floating Positive Supply Voltage	V_B	-0.3 to +60	V
High-Side Floating Negative Supply Voltage	V_S	V_B-14 to V_B+0.3	V
High-Side Floating Output Voltage	V_{HO}	V_S-0.3 to V_B+0.3	V
Offset Supply Voltage Transient	dV_S/dt	50	V/ns
Logic and Low-Side Fixed Supply Voltage	V_{CC}	-0.3 to +14	V
Low-Side Output Voltage	V_{LO}	-0.3 to V_{CC}+0.3	V
Logic Input Voltage (IN and EN)	V_{IN}	-0.3 to V_{CC}+0.3	V

Thermal Characteristics – W-DFN3030-10 (Type TH) (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation Linear Derating Factor (Note 5)	P_D	0.4	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	64	°C/W
Thermal Resistance, Junction to Case (Note 5)	$R_{\theta JC}$	42	°C/W
Operating Temperature	T_J	+150	
Lead Temperature (Soldering, 10s)	T_L	+300	°C
Storage Temperature Range	T_{STG}	-55 to +150	

Note: 5. When mounted on a standard JEDEC 2-layer FR-4 board.

Thermal Characteristics – MSOP-10 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation Linear Derating Factor (Note 6)	P_D	0.75	W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	166	°C/W
Thermal Resistance, Junction to Case (Note 6)	$R_{\theta JC}$	32	°C/W
Operating Temperature	T_J	+150	
Lead Temperature (Soldering, 10s)	T_L	+300	°C
Storage Temperature Range	T_{STG}	-55 to +150	

Note: 6. When mounted on a standard JEDEC 2-layer FR-4 board with minimum recommended pad layout.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
High-Side Floating Supply	V_B	V_S + 8	V_S + 14	V
High-Side Floating Supply Offset Voltage	V_S	(Note 7)	50 (Note 8)	V
High-Side Floating Output Voltage	V_{HO}	V_S	V_B	V
Logic and Low-Side Fixed Supply Voltage	V_{CC}	8	14	V
Low-Side Output Voltage	V_{LO}	0	V_{CC}	V
Logic Input Voltage (IN and EN)	V_{IN}	0	5	V
Ambient Temperature	T_A	-40	+125	°C

Notes: 7. Logic operation for V_S of -5V to +50V.
8. Provided V_B does not exceed absolute maximum rating of 60V.

DC Electrical Characteristics (V_{CC} = V_{BS} = 12V, COM = V_S = 0, @T_A = +25°C, unless otherwise specified.) (Note 9)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Logic "1" Input Voltage	V_{IH}	2.4	—	—	V	—
Logic "0" Input Voltage	V_{IL}	—	—	0.8	V	—
Enable Logic "1" Input Voltage	V_{ENIH}	1.5	—	—	V	—
Enable Logic "0" Input Voltage	V_{ENIL}	—	—	0.7	V	—
Input Voltage Hysteresis	V_{INHYS}	—	0.6	—	V	—
High-Level Output Voltage, V_{BIAS} - V_O	V_{OH}	—	0.45	0.6	V	I_{O+} = 100mA
Low-Level Output Voltage, V_O	V_{OL}	—	0.15	0.22	V	I_{O-} = 100mA
Offset Supply Leakage Current	I_{LK}	—	10	50	µA	V_B = V_S = 60V
V_{CC} Shutdown Supply Current	I_{CCSD}	—	0	1	µA	V_{IN} = 0 or 5V, V_{EN} = 0
V_{CC} Quiescent Supply Current	I_{CCQ}	—	0.28	0.5	mA	V_{IN} = 0 or 5V R_{DT} = 100kΩ
V_{CC} Operating Supply Current	I_{CCOP}	—	7.6	—	mA	f_S = 500kHz, C_L = 1000pF
V_{BS} Quiescent Supply Current	I_{BSQ}	—	32	100	µA	V_{IN} = 0 or 5V
V_{BS} Operating Supply Current	I_{BSOP}	—	7.6	—	mA	f_S = 500kHz, C_L = 1000pF
Logic "1" Input Bias Current	I_{IN+}	—	25	60	µA	V_{IN} = 5V
Logic "0" Input Bias Current	I_{IN-}	—	0	1	µA	V_{IN} = 0
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}	6.0	7.0	8.0	V	—
V_{BS} Supply Undervoltage Negative Going Threshold	V_{BSUV-}	5.6	6.6	7.6	V	—
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	6.0	7.0	8.0	V	—
V_{CC} Supply Undervoltage Negative Going Threshold	V_{CCUV-}	5.6	6.6	7.6	V	—
Output High Short-Circuit Pulsed Current	I_{O+}	0.9	1.5	—	A	V_O = 0, PW ≤ 10µs
Output Low Short-Circuit Pulsed Current	I_{O-}	1.5	2.0	—	A	V_O = 15V, PW ≤ 10µs
Forward Voltage of Bootstrap Diode	V_{F1}	—	0.67	—	V	I_F = 100µA
Forward Voltage of Bootstrap Diode	V_{F2}	—	1.7	—	V	I_F = 100mA

Note: 9. The V_{IN} and I_{IN} parameters are applicable to the two logic pins: IN and EN. The V_O and I_O parameters are applicable to the respective output pins: HO and LO.

AC Electrical Characteristics (V_{CC} = V_{BS} = 12V, COM = V_S = 0, C_L = 1000pF, @T_A = +25°C, unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Turn-On Propagation Delay, HO & LO	t_{on}	65	96	125	ns	R_{DT} = 10kΩ
		350	463	580	ns	R_{DT} = 100kΩ
Turn-Off Propagation Delay, HO & LO	t_{off}	—	22	56	ns	—
Turn-On Rise Time	t_r	—	17	35	ns	—
Turn-Off Fall Time	t_f	—	12	25	ns	—
Delay Matching	t_{DM}	—	—	50	ns	—
Deadtime: $t_{DT\ LO-HO}$ & $t_{DT\ HO-LO}$	t_{DT}	40	70	100	ns	R_{DT} = 10kΩ
		300	430	560	ns	R_{DT} = 100kΩ
Deadtime Matching	t_{MDT}	—	—	50	ns	R_{DT} = 100kΩ

Timing Waveforms

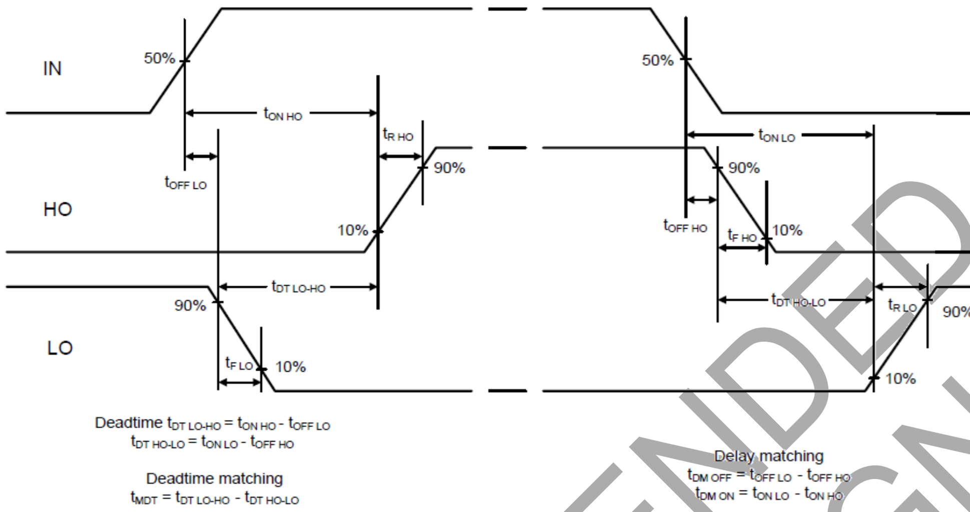


Figure 1. Switching Time Waveform Definitions

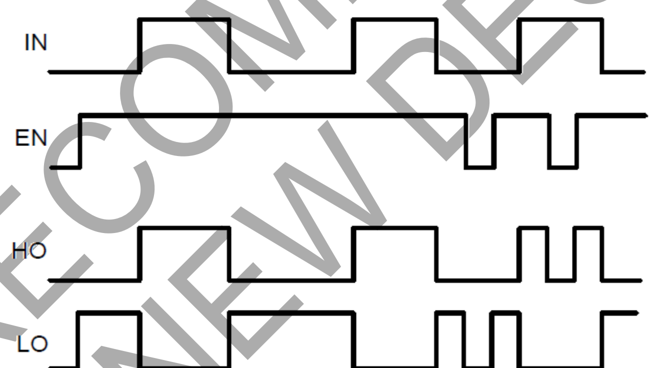


Figure 2. Input / Output Timing Diagram

Typical Performance Characteristics (VCC = 12V, @TA = +25°C, unless otherwise specified.)

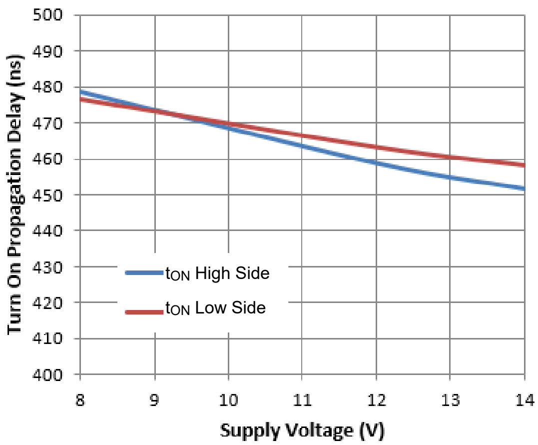


Figure 3. Turn-on Propagation Delay vs. Supply Voltage

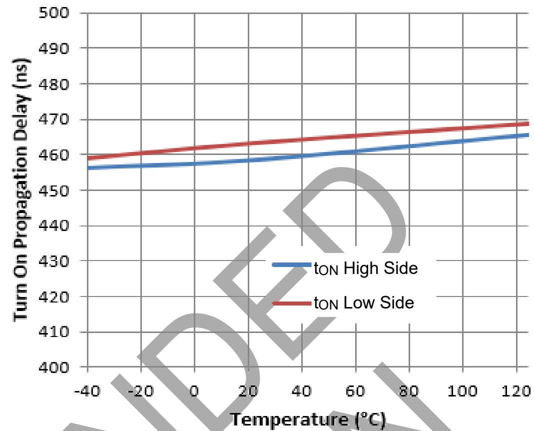


Figure 4. Turn-on Propagation Delay vs. Temperature

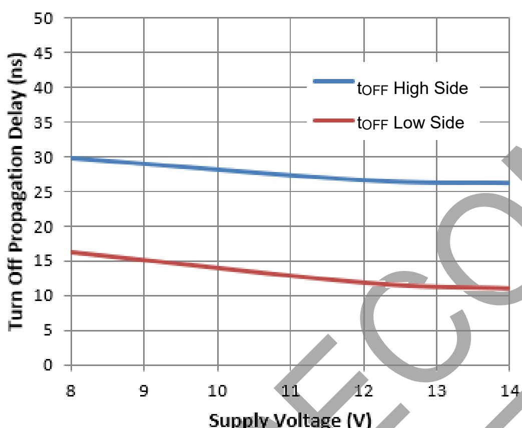


Figure 5. Turn-off Propagation Delay vs. Supply Voltage

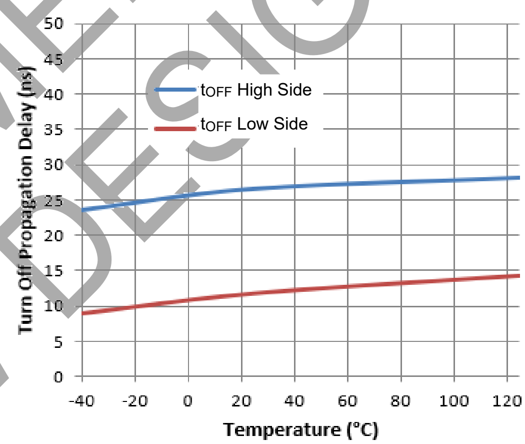


Figure 6. Turn-off Propagation Delay vs. Temperature

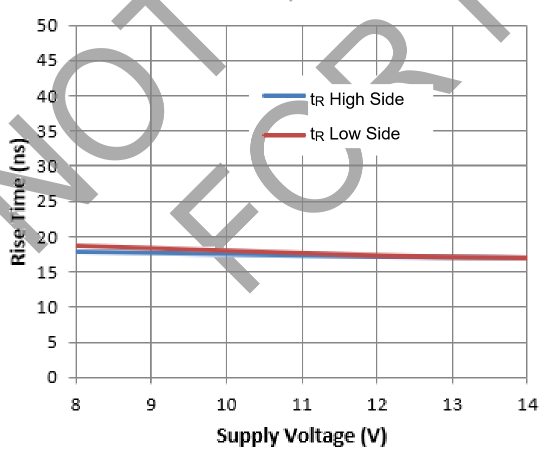


Figure 7. Rise Time vs. Supply Voltage

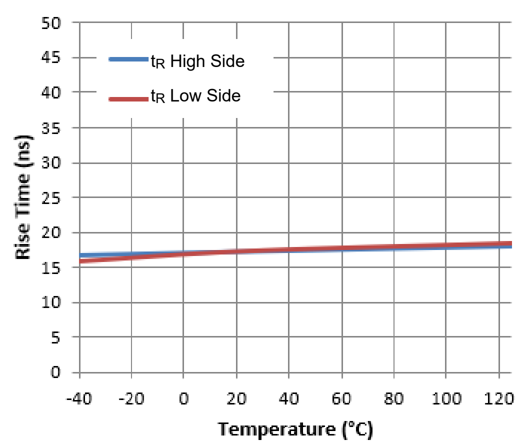


Figure 8. Rise Time vs. Temperature

Typical Performance Characteristics (V_{CC} = 12V, @T_A = +25°C, unless otherwise specified.) (continued)

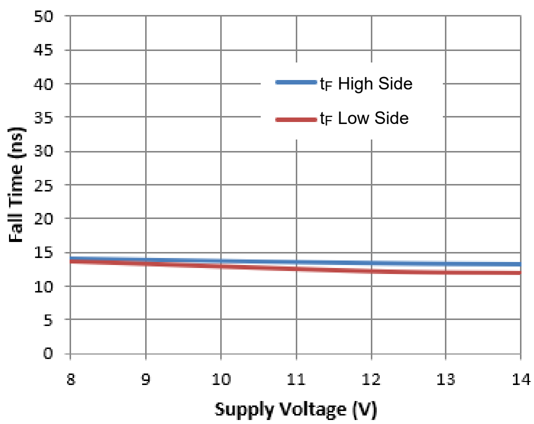


Figure 9. Fall Time vs. Supply Voltage

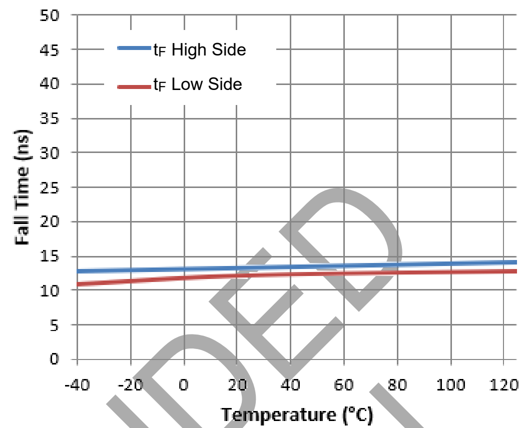


Figure 10. Fall Time vs. Temperature

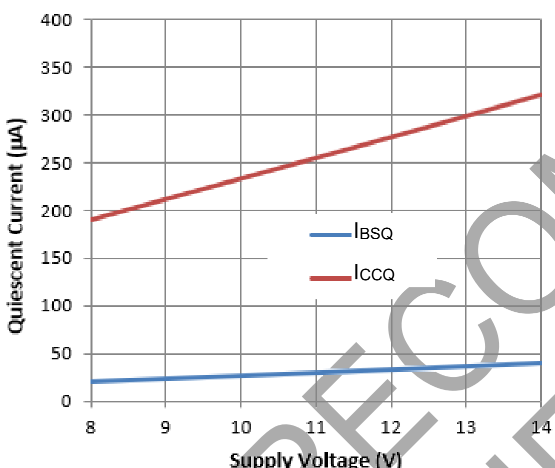


Figure 11. Quiescent Current vs. Supply Voltage

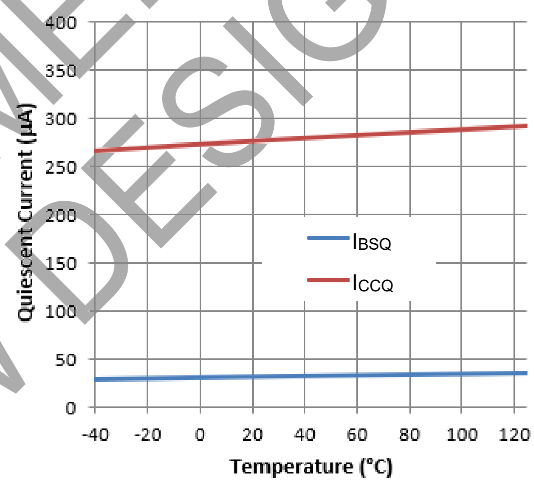


Figure 12. Quiescent Current vs. Temperature

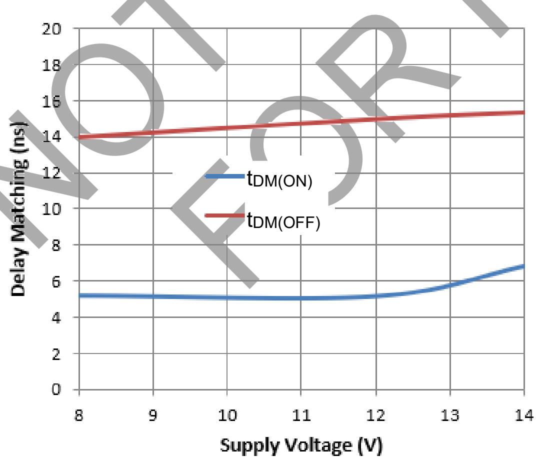


Figure 13. Delay Matching vs. Supply Voltage

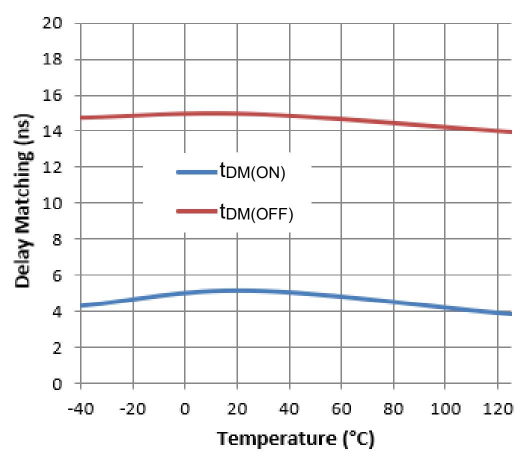


Figure 14. Delay Matching vs. Temperature

Typical Performance Characteristics (VCC = 12V, @TA = +25°C, unless otherwise specified.) (continued)

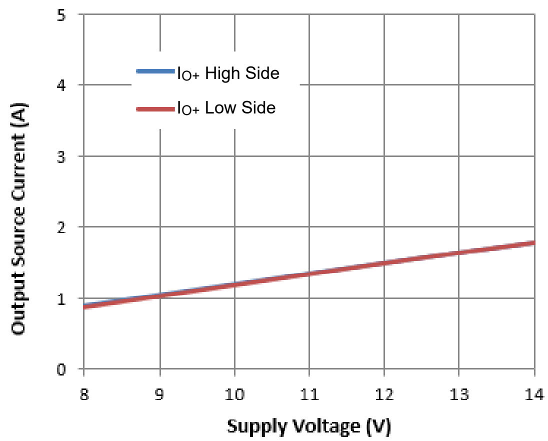


Figure 15. Output Source Current vs. Supply Voltage

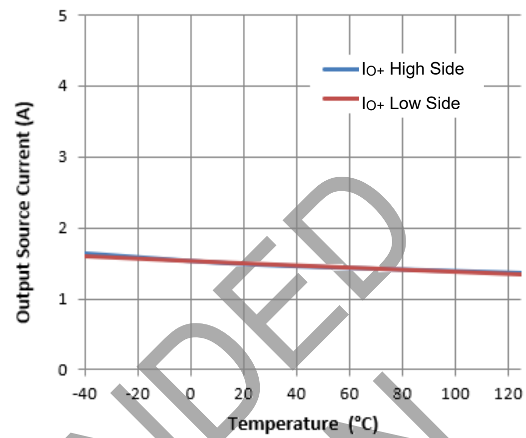


Figure 16. Output Source Current vs. Temperature

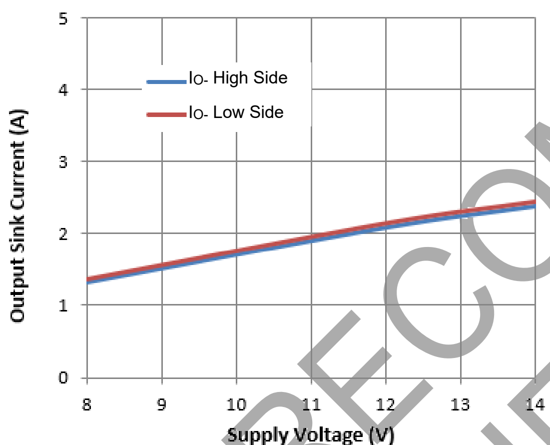


Figure 17. Output Sink Current vs. Supply Voltage

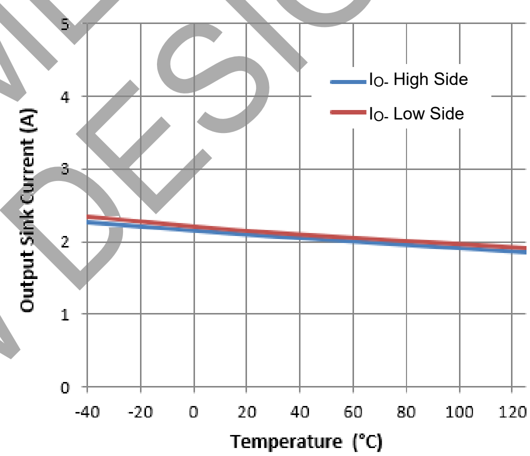


Figure 18. Output Sink Current vs. Temperature

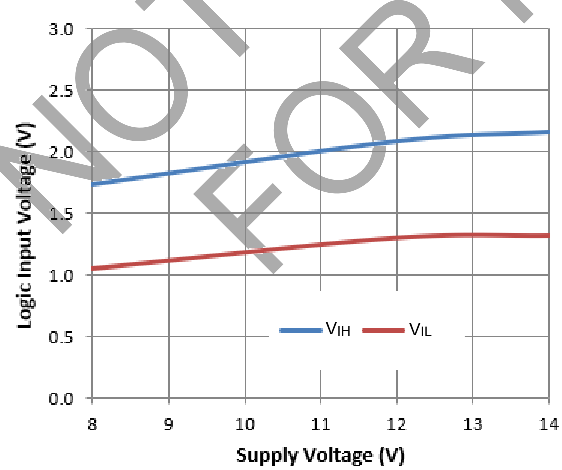


Figure 19. Logic Input Voltage vs. Supply Voltage

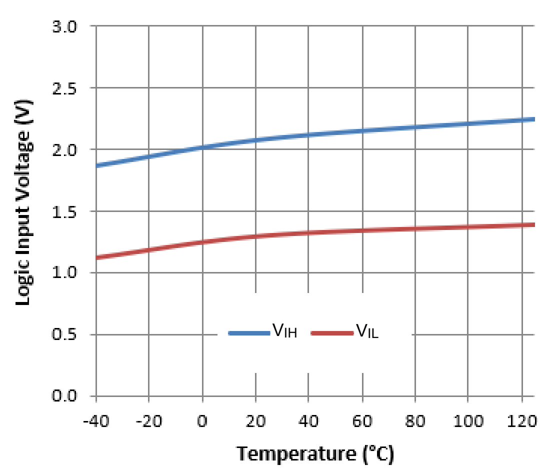


Figure 20. Logic Input Voltage vs. Temperature

Typical Performance Characteristics (V_{CC} = 12V, @T_A = +25°C, unless otherwise specified.) (continued)

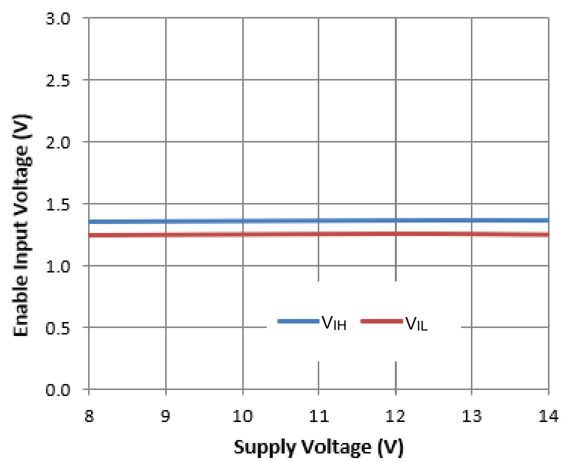


Figure 21. Enable Input Voltage vs. Supply Voltage

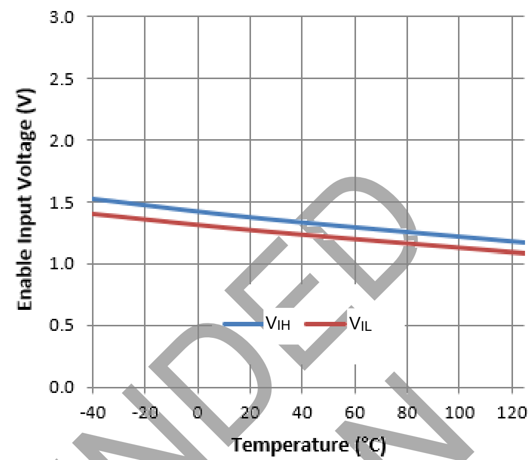


Figure 22. Enable Input Voltage vs. Temperature

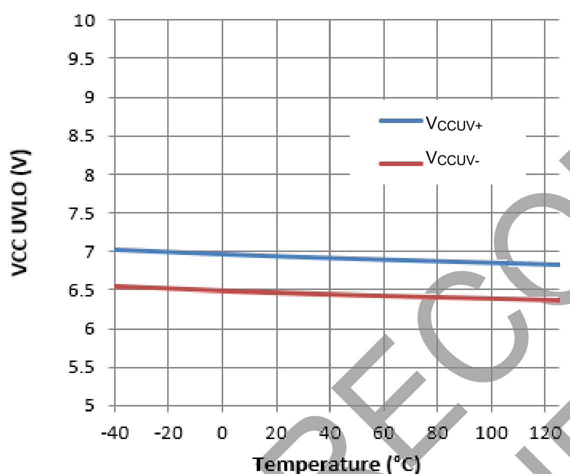


Figure 23. VCC UVLO vs. Temperature

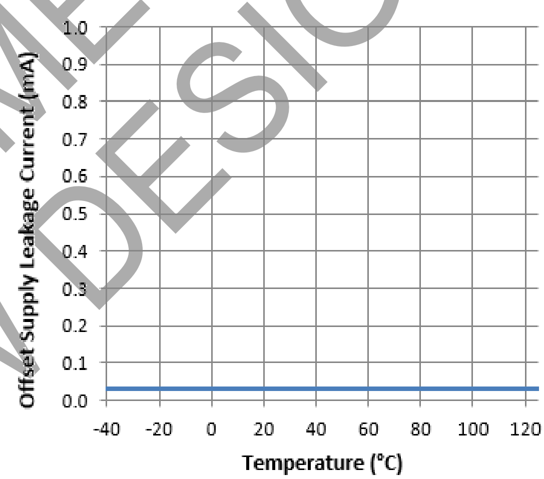
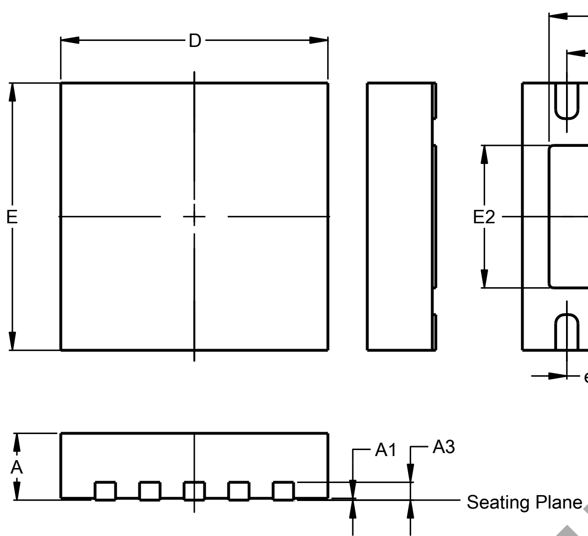


Figure 24. Offset Supply Leakage Current vs. Temperature

Package Outline Dimensions

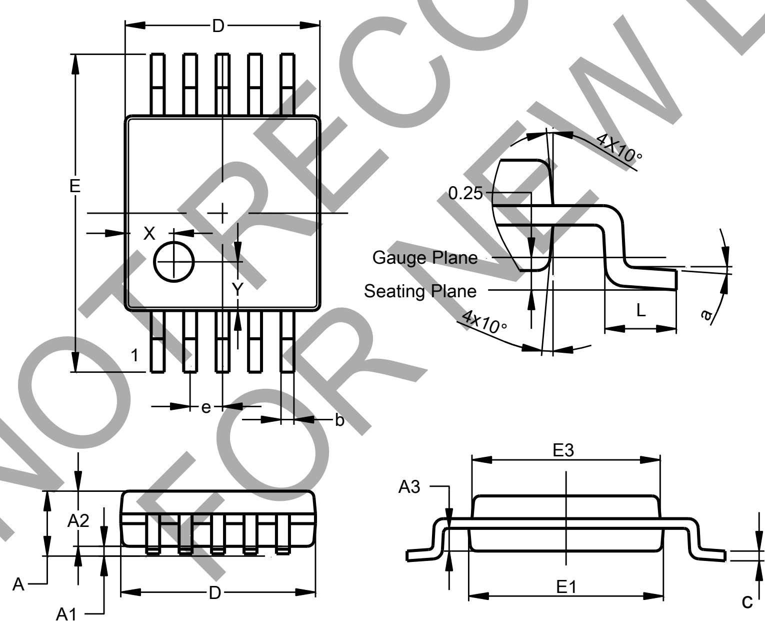
Please see http://www.diodes.com/package-outlines.html for the latest version.

W-DFN3030-10 (Type TH)



W-DFN3030-10 (Type TH)			
Dim	**Min**	**Max**	**Typ**
A	0.70	0.80	0.75
A1	--	0.05	0.02
A3	0.18	0.25	0.20
b	0.18	0.30	0.25
D	2.90	3.10	3.00
D2	2.40	2.60	2.50
e	0.50BSC		
e1	2.00BSC		
E	2.90	3.10	3.00
E2	1.45	1.65	1.55
h	0.20	0.30	0.25
L	0.30	0.50	0.40
All Dimensions in mm			

MSOP-10

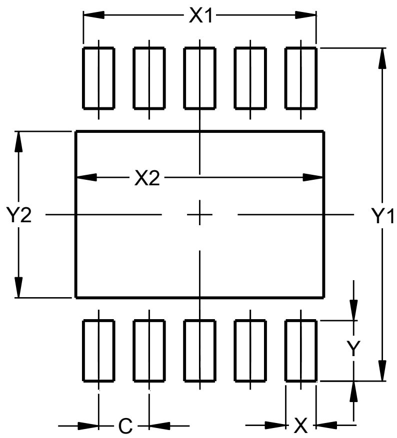


MSOP-10			
Dim	**Min**	**Max**	**Typ**
A	-	1.10	-
A1	0.05	0.15	0.10
A2	0.75	0.95	0.86
A3	0.29	0.49	0.39
b	0.17	0.27	0.20
c	0.08	0.23	0.15
D	2.95	3.05	3.00
e	-	-	0.50
E	4.80	5.00	4.90
E1	2.95	3.05	3.00
E3	2.85	3.05	2.95
L	0.40	0.80	0.60
X	--	--	0.750
Y	--	--	0.750
a	0°	8°	4°
All Dimensions in mm			

Suggested Pad Layout

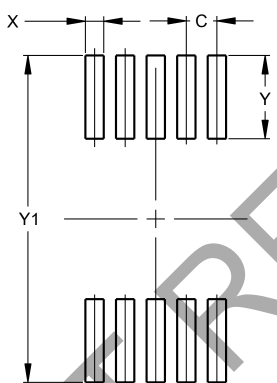
Please see http://www.diodes.com/package-outlines.html for the latest version.

W-DFN3030-10 (Type TH)



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	2.300
X2	2.600
Y	0.600
Y1	3.300
Y2	1.650

MSOP-10



Dimensions	Value (in mm)
C	0.50
X	0.30
Y	1.35
Y1	5.30

Note: 10. For high-voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

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