

### Radiation Tolerant UltraCMOS® Integer-N Frequency Synthesizer for Low Phase Noise Applications

#### Product Description

Peregrine's PE97240 is a radiation tolerant high-performance Integer-N PLL capable of frequency synthesis up to 5 GHz. The device is designed for commercial space applications and optimized for superior phase noise performance.

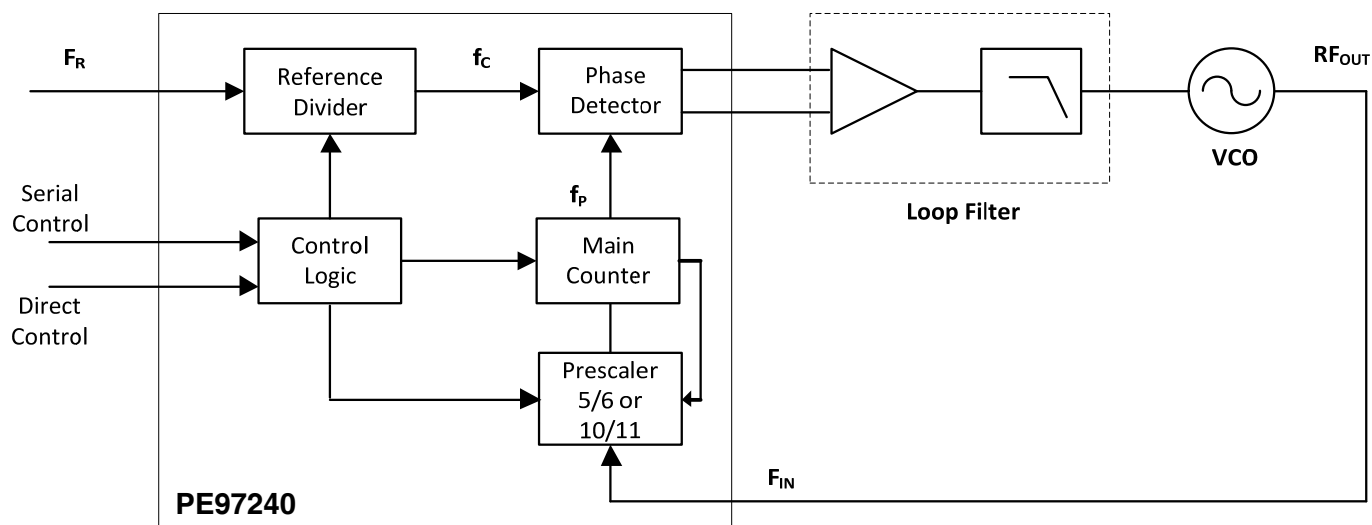
The PE97240 features a selectable prescaler modulus of 5/6 or 10/11, counters and a phase comparator as shown in *Figure 1*. Counter values are programmable through either a serial interface or directly hard-wired.

The PE97240 is available in a 44-lead CQFP and is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering excellent RF performance and intrinsic radiation tolerance.

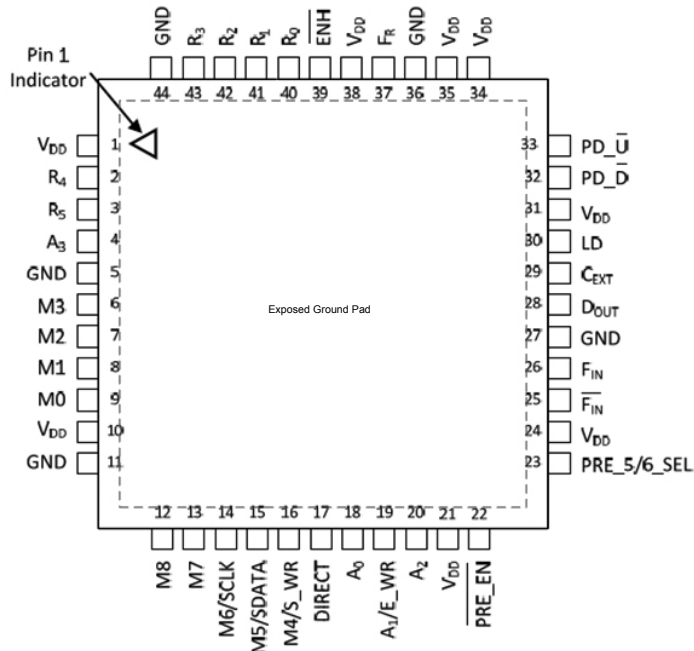
#### Features

- Frequency range
  - 5 GHz in 10/11 prescaler modulus
  - 4 GHz in 5/6 prescaler modulus
- Phase noise floor figure of merit: -230 dBc/Hz
- Low power: 75 mA @ 2.7V
- Serial or direct mode access
- Packaged in a 44-lead CQFP
- 100 kRad(Si) total dose

**Figure 1. Functional Diagram**



**Figure 2. Pin Configuration (Top View)**



**Figure 3. Package Type**  
44-lead CQFP



**Table 1. Pin Descriptions**

Pin #	Pin Name	Interface Mode	Type	Description
1	V <sub>DD</sub>	Both	Note 1	Power supply input. Input may range from 2.6–2.8V. Bypassing recommended.
2	R <sub>4</sub>	Direct	Input	R counter bit4
3	R <sub>5</sub>	Direct	Input	R counter bit5
4	A <sub>3</sub>	Direct	Input	A counter bit3
5	GND	Both		Ground
6	M <sub>3</sub>	Direct	Input	M counter bit3
7	M <sub>2</sub>	Direct	Input	M counter bit2
8	M <sub>1</sub>	Direct	Input	M counter bit1
9	M <sub>0</sub>	Direct	Input	M counter bit0
10	V <sub>DD</sub>	Both	Note 1	Power supply input. Input may range from 2.6–2.8V. Bypassing recommended.
11	GND	Both		Ground
12	M <sub>8</sub>	Direct	Input	M counter bit8
13	M <sub>7</sub>	Direct	Input	M counter bit7
14	SCLK	Serial	Input	Serial clock input. SDATA is clocked serially into the 21-bit primary register (E_WR “low”) or the 8-bit enhancement register (E_WR “high”) on the rising edge of SCLK.
	M <sub>6</sub>	Direct	Input	M counter bit6
15	SDATA	Serial	Input	Binary serial data input. Input data entered MSB first.
	M <sub>5</sub>	Direct	Input	M counter bit5
16	S_WR	Serial	Input	Serial load enable input. While S_WR is “low”, SDATA can be serially clocked. Primary register data is transferred to the secondary register on S_WR or Hop_WR rising edge.
	M <sub>4</sub>	Direct	Input	M counter bit4

**Table 1. Pin Descriptions (continued)**

Pin No.	Pin Name	Interface Mode	Type	Description
17	Direct	Direct	Input	Select “High” enables Direct Mode. Select “Low” enables Serial Mode.
18	A0	Direct	Input	A counter bit0
19	A1	Direct	Input	A counter bit1
	E_WR	Serial	Input	Enhancement register write enable. While E_WR is “high”, SDATA can be serially clocked into the enhancement register on the rising edge of SCLK.
20	A2	Direct	Input	A counter bit2
21	V <sub>DD</sub>	Both	Note 1	Power supply input. Input may range from 2.6–2.8V. Bypassing recommended.
22	$\overline{\text{Pre\_en}}$	Direct	Input	Prescaler enable, active “low”. When “high”, F <sub>IN</sub> bypasses the prescaler.
23	Pre_5/6_Sel	Direct	Input	5/6 modulus select, active “High.” When “Low,” 10/11 modulus selected.
24	V <sub>DD</sub>	Both	Note 1	Power supply input. Input may range from 2.6–2.8V. Bypassing recommended.
25	$\overline{\text{F}}_{\text{IN}}$	Both	Input	Prescaler complementary input. A 22 pF bypass capacitor should be placed as close as possible to this pin and be connected in series with a 50Ω resistor to ground.
26	F <sub>IN</sub>	Both	Input	Prescaler input from the VCO, 5.0 GHz max frequency. A 22 pF coupling capacitor should be placed as close as possible to this pin and be connected in shunt to a 50Ω resistor to ground.
27	GND	Both		Ground
28	D <sub>OUT</sub>	Serial	Output	Data Out. The MSEL signal and the raw prescaler output are available on Dout through enhancement register programming.
29	C <sub>EXT</sub>	Both	Output	Logical “NAND” of PD <sub><math>\overline{\text{D}}</math></sub> and PD <sub><math>\overline{\text{U}}</math></sub> terminated through an on chip, 2 kΩ series resistor. Connecting Cext to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD.
30	LD	Both	Output	Lock detect and open drain logical inversion of C <sub>EXT</sub> . When the loop is in lock, LD is high impedance, otherwise LD is a logic low (“0”).
31	V <sub>DD</sub>	Both	Note 1	Power supply input. Input may range from 2.6V to 2.8V. Bypassing recommended.
32	PD <sub><math>\overline{\text{D}}</math></sub>	Both	Output	PD <sub><math>\overline{\text{D}}</math></sub> is pulse down when f <sub>p</sub> leads f <sub>c</sub>
33	PD <sub><math>\overline{\text{U}}</math></sub>	Both	Output	PD <sub><math>\overline{\text{U}}</math></sub> is pulse down when f <sub>c</sub> leads f <sub>p</sub>
34	V <sub>DD</sub>	Both	Note 1	Power supply input. Input may range from 2.6–2.8V. Bypassing recommended.
35	V <sub>DD</sub>	Both	Note 1	Power supply input. Input may range from 2.6–2.8V. Bypassing recommended.
36	GND	Both		Ground
37	F <sub>R</sub>	Both	Input	Reference frequency input
38	V <sub>DD</sub>	Both	Note 1	Power supply input. Input may range from 2.6–2.8V. Bypassing recommended.
39	$\overline{\text{ENH}}$	Serial	Input	Enhancement mode. When asserted low (“0”), enhancement register bits are functional.
40	R0	Direct	Input	R counter bit0
41	R1	Direct	Input	R counter bit1
42	R2	Direct	Input	R counter bit2
43	R3	Direct	Input	R counter bit3
44	GND	Both		Ground
Pad	GND			Exposed pad: Grounded for proper operation

Notes: 1. V<sub>DD</sub> pins 1, 10, 21, 24, 31, 34, 35 and 38 are connected by diodes and must be supplied with the same positive voltage level.  
2. All digital input pins have 70 kΩ pull-down resistors to ground.

**Table 2. Operating Ratings**

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	$V_{DD}$	2.6	2.8	V
Operating ambient temperature range	$T_A$	-40	+85	°C

**Table 3. Absolute Maximum Ratings**

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	$V_{DD}$	-0.3	3.3	V
Voltage on any input	$V_I$	-0.3	$V_{DD} + 0.3$	V
DC into any input	$I_I$	-10	+10	mA
DC into any output	$I_O$	-10	+10	mA
RF input power, CW 50 MHz–5 GHz	$P_{MAX\_CW}$		10	dBm
Thermal resistance	$T_{JC}$		33.4	°C/W
Junction temperature maximum	$T_J$		+125	°C
Storage temperature range	$T_{ST}$	-65	+150	°C
ESD voltage HBM <sup>1</sup> All pins except pin 28	$V_{ESD\_HBM}$		1000	V
ESD voltage HBM <sup>1,2</sup> On pin 28			300	V

Notes: 1. Human Body Model (MIL-STD-883 Method 3015).  
2. Pin 28 is not used in normal operation.

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

## Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

## Latch-Up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

## ELDRS

UltraCMOS devices do not include bipolar minority carrier elements, and therefore do not exhibit enhanced low dose rate sensitivity.

**Table 4. Single Event Effects<sup>1</sup>**

SEE Mode	Effective Linear Energy Transfer (LET) <sup>2</sup>
SEL	86 MeV•cm <sup>2</sup> /mg
SEFI	86 MeV•cm <sup>2</sup> /mg
SEU	86 MeV•cm <sup>2</sup> /mg
SET	30 MeV•cm <sup>2</sup> /mg <sup>3</sup>

Notes: 1. Testing performed using serial programming mode.  
2. SEE testing was conducted with Au, Ho, Xe, Kr, Cu ion species at 0° incidence.  
3. Minor transients (phase errors) observed resulting in self-recovering operation without intervention.

**Table 5. DC Characteristics @  $V_{DD} = 2.7V$ ,  $-40\text{ }^{\circ}C < T_A < +85\text{ }^{\circ}C$ , unless otherwise specified**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I <sub>DD</sub>	Operational supply current	Prescaler disabled, f <sub>C</sub> = 50 MHz, F <sub>IN</sub> = 500 MHz V <sub>DD</sub> = 2.6–2.8V		34	50	mA
		5/6 prescaler, f <sub>C</sub> = 50 MHz, F <sub>IN</sub> = 3 GHz V <sub>DD</sub> = 2.6–2.8V		72	105	mA
		10/11 prescaler, f <sub>C</sub> = 50 MHz, F <sub>IN</sub> = 3 GHz V <sub>DD</sub> = 2.6–2.8V		74	110	mA
Digital Inputs: All except F <sub>R</sub> , F <sub>IN</sub> , $\overline{F_{IN}}$						
V <sub>IH</sub>	High level input voltage	V <sub>DD</sub> = 2.6–2.8V	0.7 x V <sub>DD</sub>			V
V <sub>IL</sub>	Low level input voltage	V <sub>DD</sub> = 2.6–2.8V			0.3 x V <sub>DD</sub>	V
I <sub>IH</sub>	High level input current	V <sub>IH</sub> = V <sub>DD</sub> = 2.8V			70	μA
I <sub>IL</sub>	Low level input current	V <sub>IL</sub> = 0, V <sub>DD</sub> = 2.8V	–10			μA
Reference Divider input: F <sub>R</sub>						
I <sub>IHR</sub>	High level input current	V <sub>IH</sub> = V <sub>DD</sub> = 2.8V			300	μA
I <sub>ILR</sub>	Low level input current	V <sub>IL</sub> = 0, V <sub>DD</sub> = 2.8V	–300			μA
Counter and phase detector outputs: PD_0, PD_1						
V <sub>OLD</sub>	Output voltage LOW	I <sub>out</sub> = 6 mA			0.4	V
V <sub>OHD</sub>	Output voltage HIGH	I <sub>out</sub> = –3 mA	V <sub>DD</sub> – 0.4			V
Lock detect outputs: C <sub>EXT</sub> , LD						
V <sub>OLC</sub>	Output voltage LOW, C <sub>EXT</sub>	I <sub>out</sub> = 100 μA			0.4	V
V <sub>OHC</sub>	Output voltage HIGH, C <sub>EXT</sub>	I <sub>out</sub> = –100 μA	V <sub>DD</sub> – 0.4			V
V <sub>OLLD</sub>	Output voltage LOW, LD	I <sub>out</sub> = 1 mA			0.4	V

**Table 6. AC Characteristics @  $V_{DD} = 2.7V$ ,  $-40\text{ }^{\circ}C < T_A < +85\text{ }^{\circ}C$ , unless otherwise specified**

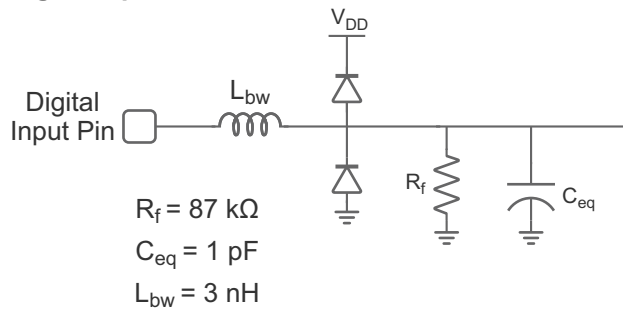
Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Control interface and latches (see Figures 16 and 17)<sup>1</sup></b>						
$f_{CLK}$	Serial data clock frequency <sup>2</sup>				10	MHz
$t_{CLKH}$	Serial clock HIGH time		30			ns
$t_{CLKL}$	Serial clock LOW time		30			ns
$t_{DSU}$	SDATA set-up time after SCLK rising edge		10			ns
$t_{DHLd}$	SDATA hold time after SCLK rising edge		10			ns
$t_{PW}$	S_WR pulse width		30			ns
$t_{CWR}$	SCLK rising edge to S_WR rising edge		30			ns
$t_{CE}$	SCLK falling edge to E_WR transition		30			ns
$t_{WRC}$	S_WR falling edge to SCLK rising edge		30			ns
$t_{EC}$	E_WR transition to SCLK rising edge		30			ns
<b>Main divider 5/6 (including prescaler)</b>						
$F_{IN}$	Operating frequency		800		4000	MHz
$P_{F\_IN}$	Input level range	External AC coupling 800 MHz–4 GHz	$-5^3$		7	dBm
<b>Main divider 10/11 (including prescaler)</b>						
$F_{IN}$	Operating frequency		800		5000	MHz
$P_{F\_IN}$	Input level range	External AC coupling 800 MHz–<4 GHz 4–5 GHz	$-5^3$ 2		7 7	dBm dBm
<b>Main divider (prescaler bypassed)</b>						
$F_{IN}$	Operating frequency		50		800	MHz
$P_{F\_IN}$	Input level range	External AC coupling	$-5^3$		7	dBm
<b>Reference divider</b>						
$F_R$	Operating frequency				100	MHz
$P_{F\_R}$	Reference input power <sup>4</sup>	Single-ended input	$-5^5$		7	dBm
<b>Phase detector</b>						
$f_c$	Comparison frequency				100	MHz

**Table 6. AC Characteristics @  $V_{DD} = 2.7V$ ,  $-40\text{ }^{\circ}C < T_A < +85\text{ }^{\circ}C$ , unless otherwise specified (continued)**

Symbol	Parameter	Condition	Min	Typical	Max	Unit
<b>SSB phase noise 5/6 prescaler (<math>F_{IN} = 3\text{ GHz}</math>, <math>P_{F\_R} = +5\text{ dBm}</math>, <math>f_c = 50\text{ MHz}</math>, <math>LBW = 500\text{ kHz}</math>)</b>						
$\Phi_N$	Phase noise	100 Hz offset		-100	-92	dBc/Hz
$\Phi_N$	Phase noise	1 kHz offset		-109	-103	dBc/Hz
$\Phi_N$	Phase noise	10 kHz offset		-116	-110	dBc/Hz
$\Phi_N$	Phase noise	100 kHz offset		-118	-115	dBc/Hz
<b>SSB phase noise 10/11 prescaler (<math>F_{IN} = 3\text{ GHz}</math>, <math>P_{F\_R} = +5\text{ dBm}</math>, <math>f_c = 50\text{ MHz}</math>, <math>LBW = 500\text{ kHz}</math>)</b>						
$\Phi_N$	Phase noise	100 Hz offset		-98	-91	dBc/Hz
$\Phi_N$	Phase noise	1 kHz offset		-104	-98	dBc/Hz
$\Phi_N$	Phase noise	10 kHz offset		-111	-107	dBc/Hz
$\Phi_N$	Phase noise	100 kHz offset		-117	-113	dBc/Hz
<b>Phase noise figure of merit (FOM)<sup>6</sup></b>						
$FOM_{flicker}$	Flicker figure of merit	5/6 prescaler		-268	-265	dBc/Hz
		10/11 prescaler		-263	-259	dBc/Hz
$FOM_{floor}$	Floor figure of merit	5/6 prescaler		-230	-227	dBc/Hz
		10/11 prescaler		-229	-225	dBc/Hz
$FOM_{flicker}$	$PN_{flicker} = FOM_{flicker} + 20\log(F_{IN}) - 10\log(f_{offset})$					dBc/Hz
$FOM_{floor}$	$PN_{floor} = FOM_{floor} + 10\log(f_c) + 20\log(F_{IN}/f_c)$					dBc/Hz
$FOM_{total}$	$PN_{total} = 10\log(10 [PN_{flicker}/10] + 10 [PN_{floor}/10])$					dBc/Hz

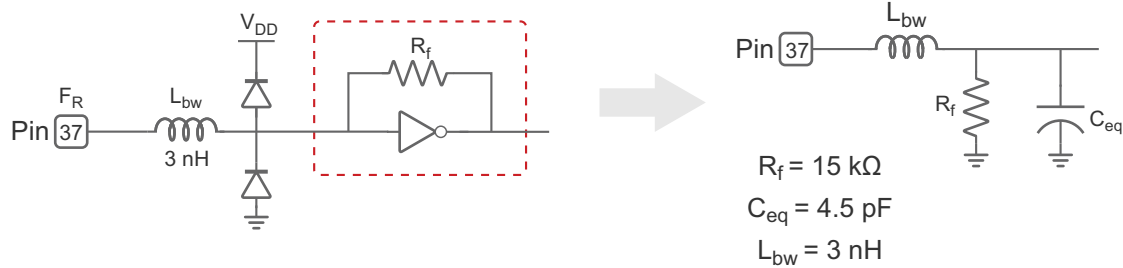
- Notes:
1. Timing parameters are guaranteed through design characterization and not tested in production.
  2.  $f_{clk}$  is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify  $f_{clk}$  specification.
  3. 0 dBm minimum is recommended for improved phase noise performance when sine-wave is applied.
  4. CMOS logic levels can be used to drive the reference input. If the  $V_{DD}$  of the CMOS driver matches the  $V_{DD}$  of the PLL IC, then the reference input can be DC coupled. Otherwise, the reference input should be AC coupled. For sine-wave inputs, the minimum amplitude needs to be  $0.5 V_{PP}$ . The maximum level should be limited to prevent ESD diodes at the pin input from turning on. Diodes will turn on at one forward-bias diode drop above  $V_{DD}$  or below GND. The DC voltage at the Reference input is  $V_{DD}/2$ .
  5. +2 dBm or higher is recommended for improved phase noise performance.
  6. The phase noise can be separated into two normalized specifications: a floor figure of merit and a flicker figure of merit. To accurately measure the phase noise floor without the contribution of the flicker noise, the loop bandwidth is set to 500 kHz and the phase noise is measured at a frequency offset near 100 kHz. The flicker noise is measured at a frequency offset  $\leq 1000\text{ Hz}$ . The formula assumes a -10 dB/decade slope versus frequency offset.

**Figure 4. Equivalent Input Diagram: Digital Input**  
Digital Input



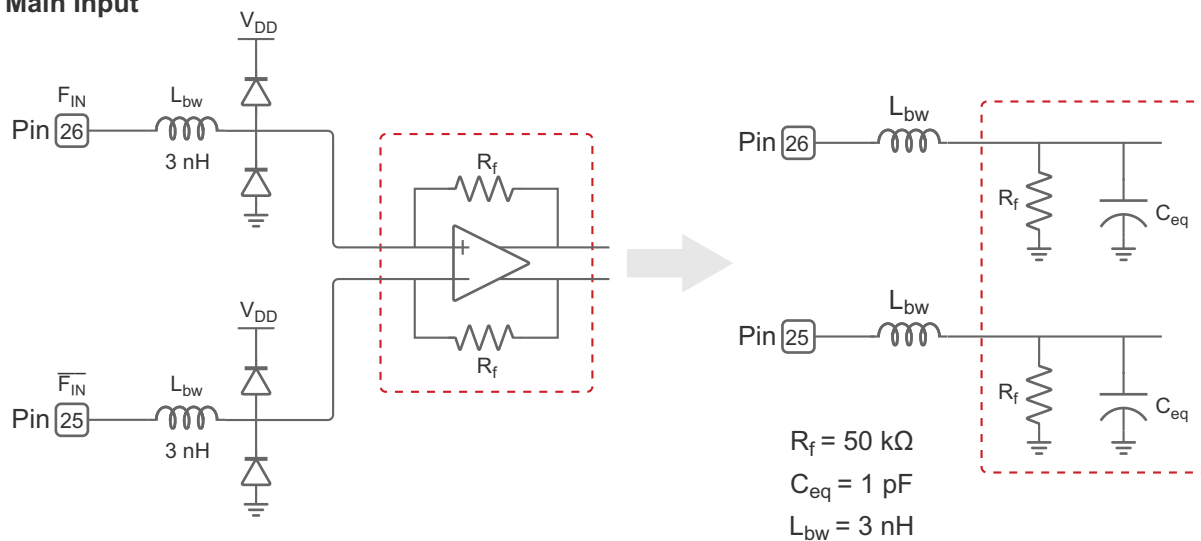
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**Figure 5. Equivalent Input Diagram: Reference Input**  
Reference Input



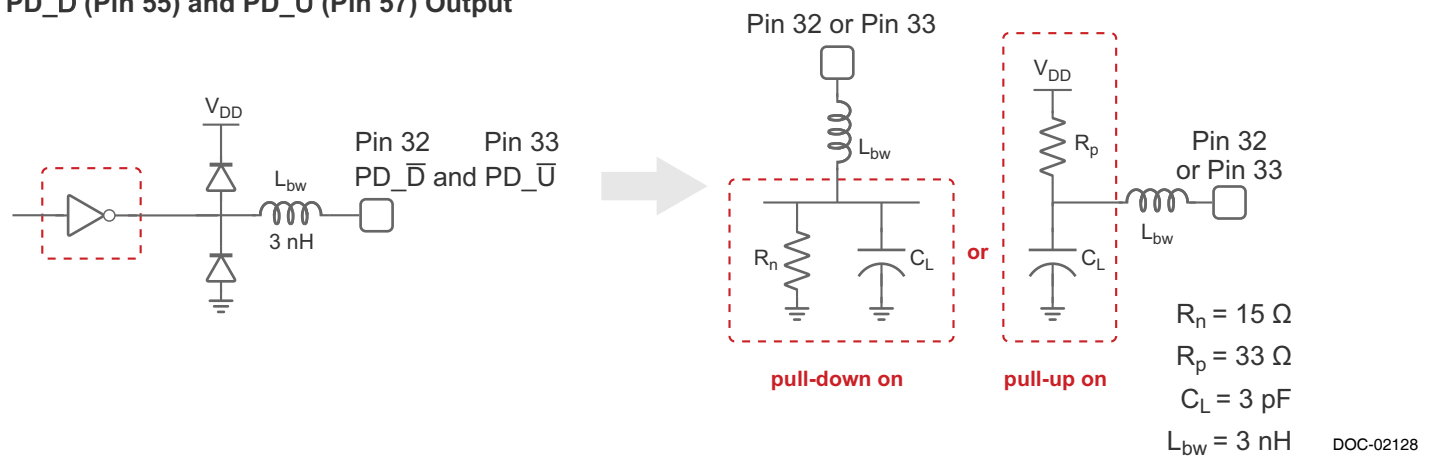
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**Figure 6. Equivalent Input Diagram: Main Input**  
Main Input



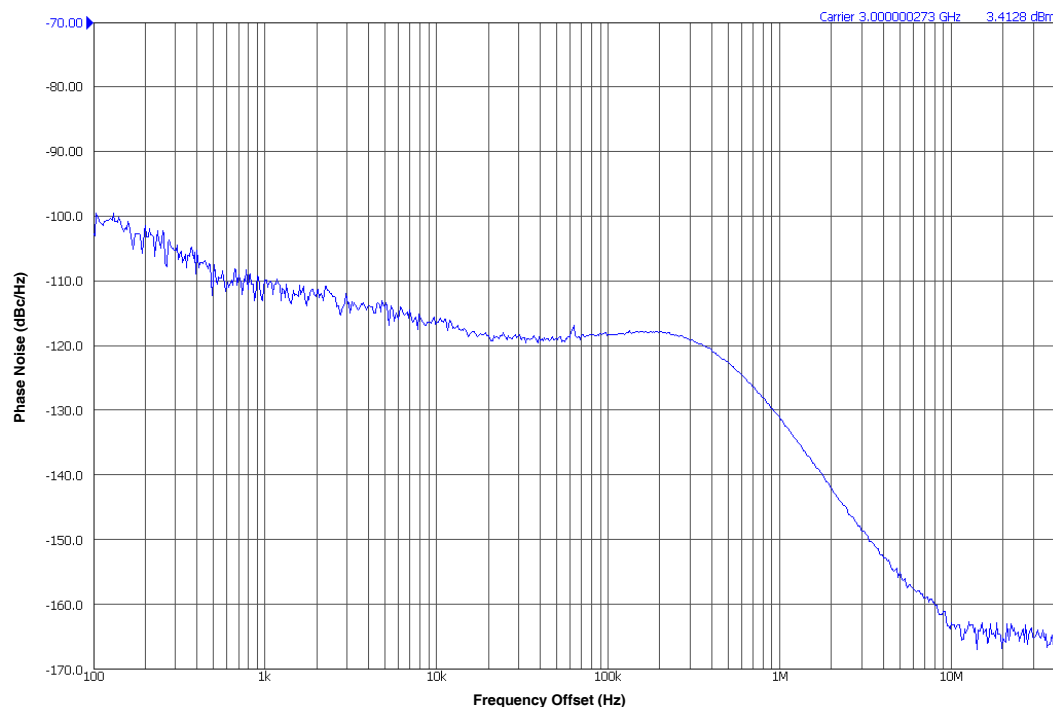
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**Figure 7. Equivalent Output Diagram**  
**PD<sub>̄</sub> (Pin 55) and PD<sub>̄</sub> (Pin 57) Output**

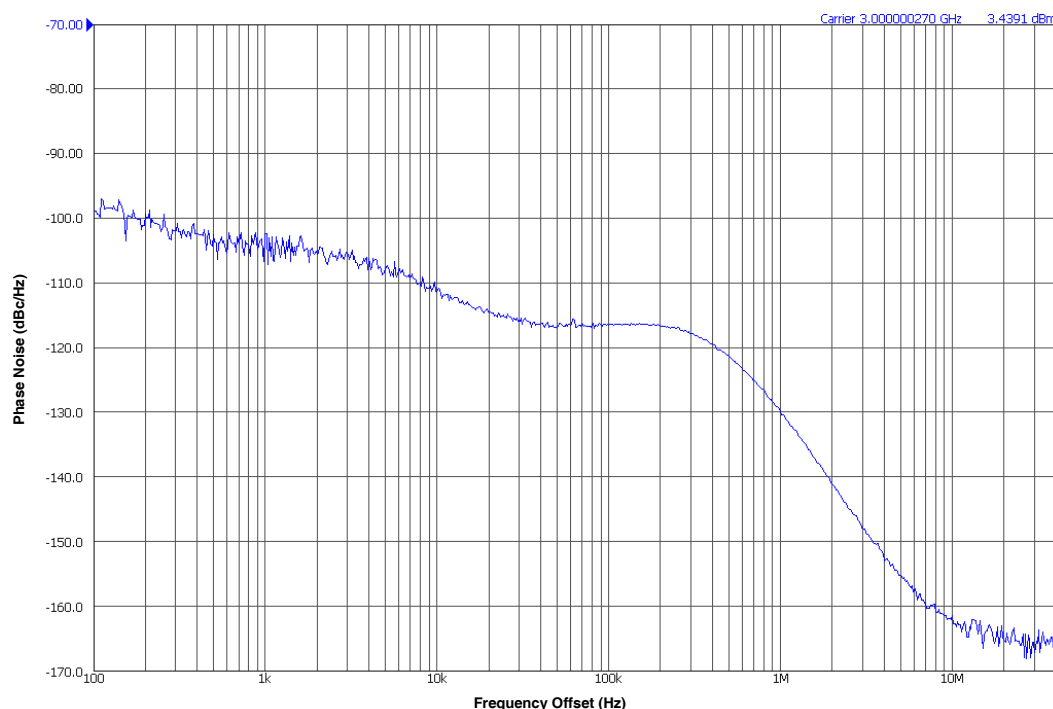


Typical Performance Data@  $V_{DD} = 2.6\text{--}2.8\text{V}$ ,  $-40\text{ }^{\circ}\text{C} < T_A < +85\text{ }^{\circ}\text{C}$ ,  $f_c = 50\text{ MHz}$  and  $F_{IN} = 3\text{ GHz}$

**Figure 8. Typical Phase Noise 5/6 Prescaler**  
 $F_{IN} = 3\text{ GHz}$ ,  $V_{DD} = 2.7\text{V}$ , Loop Bandwidth = 500 kHz,  $+25\text{ }^{\circ}\text{C}$



**Figure 9. Typical Phase Noise 10/11 Prescaler**  
 $F_{IN} = 3\text{ GHz}$ ,  $V_{DD} = 2.7\text{V}$ , Loop Bandwidth = 500 kHz,  $+25\text{ }^{\circ}\text{C}$



Typical Performance Data @  $V_{DD} = 2.6\text{--}2.8\text{V}$ ,  $-40\text{ }^{\circ}\text{C} < T_A < +85\text{ }^{\circ}\text{C}$ ,  $f_C = 50\text{ MHz}$  and  $F_{IN} = 3\text{ GHz}$

Figure 10. FOM vs. Reference Power and Temp (5/6 Prescaler,  $V_{DD} = 2.7\text{V}$ )

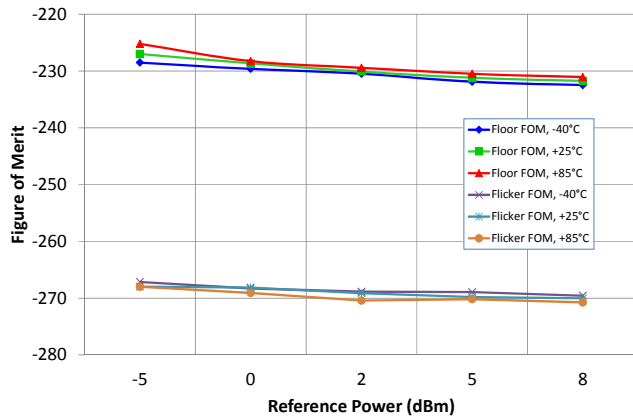


Figure 11. FOM vs. Reference Power and Temp (10/11 Prescaler,  $V_{DD} = 2.7\text{V}$ )

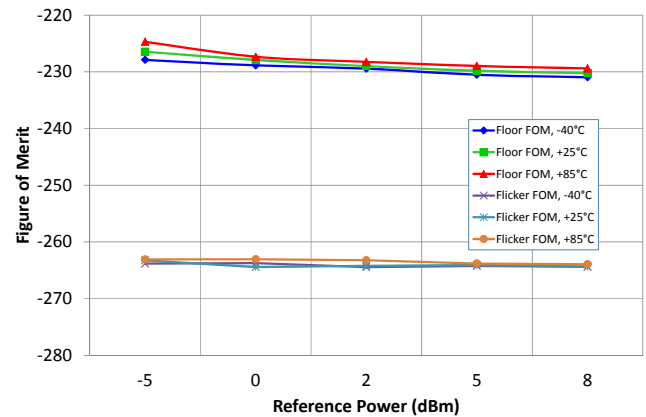


Figure 12. FOM vs. Temp and Supply Voltage (5/6 Prescaler,  $P_{F\_IN} = 2\text{ dBm}$ )

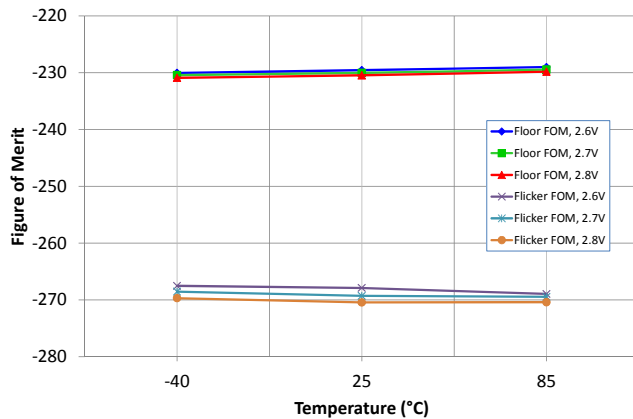


Figure 13. FOM vs. Temp and Supply Voltage (10/11 Prescaler,  $P_{F\_IN} = 2\text{ dBm}$ )

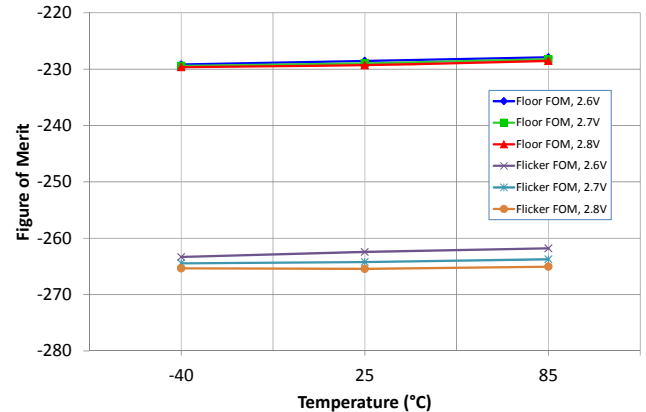


Figure 14. RF Sensitivity vs.  $F_{IN}$  and Temp (5/6 Prescaler,  $V_{DD} = 2.6\text{V}$ )\*

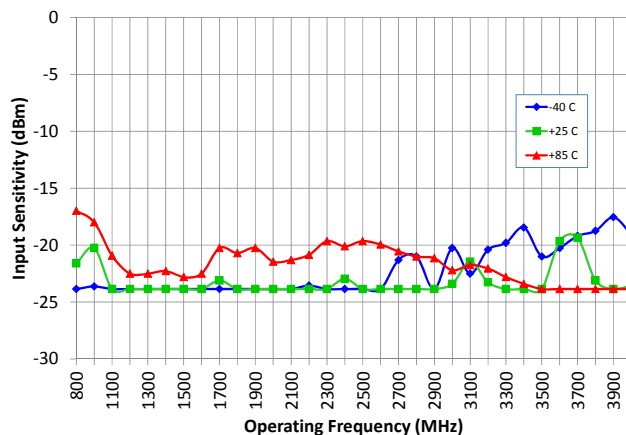
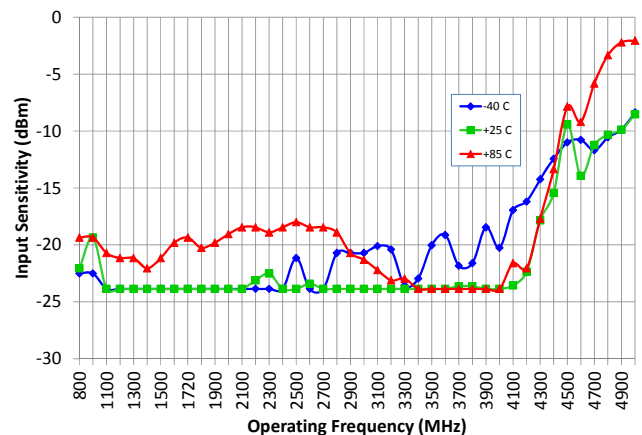


Figure 15. RF Sensitivity vs.  $F_{IN}$  and Temp (10/11 Prescaler,  $V_{DD} = 2.6\text{V}$ )\*



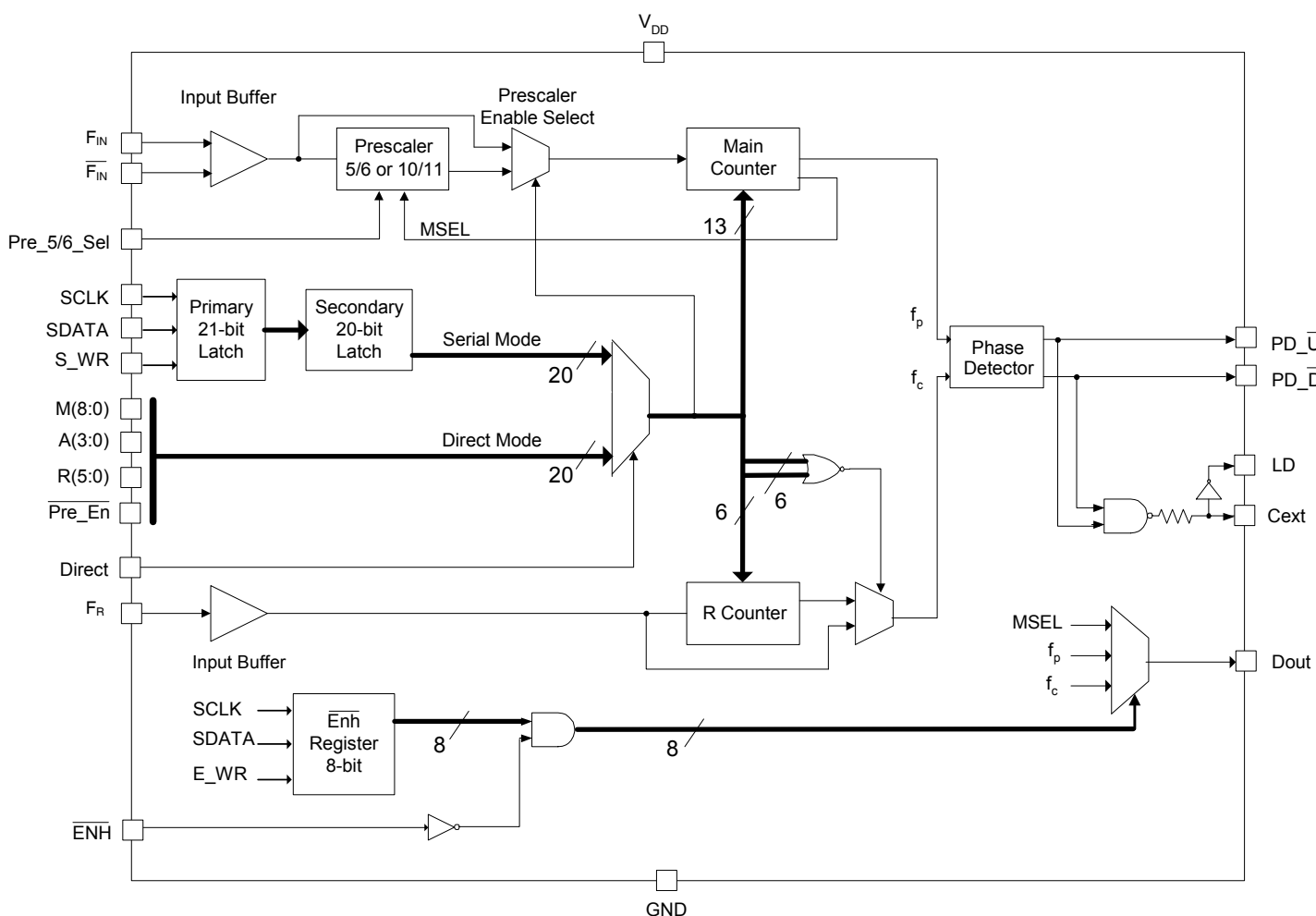
Note: \* RF sensitivity is the minimum input power level required for the PLL to maintain lock. Operating at these levels does not guarantee the SSB phase noise performance in Table 6.

## Functional Description

The PE97240 consists of a prescaler, counters, a phase detector, and control logic. The dual modulus prescaler divides the VCO frequency by either 5/6 or 10/11, depending on the value of the modulus select. Counters “R” and “M” divide the reference and prescaler output, respectively, by integer values stored in a 21-bit register. An additional counter (“A”) is used in the modulus

select logic. The phase-frequency detector generates up and down frequency control signals. The control logic includes a selectable chip interface. Data can be written via serial bus or hardwired directly to the pins. There are also various operational and test modes and a lock detect output.

**Figure 16. Functional Block Diagram**



## Main Counter Chain

### Normal Operating Mode

The main counter chain divides the RF input frequency,  $F_{IN}$ , by an integer derived from the user-defined values in the “M” and “A” counters. It is composed of the 5/6 or 10/11 selectable modulus prescaler, modulus select logic, and 9-bit M counter. The prescaler can be set to either 5/6 or 10/11 based on the Pre\_5/6\_SEL pin. Setting  $\overline{\text{Pre\_en}}$  “low” enables the 5/6 or 10/11 prescaler. Setting  $\overline{\text{Pre\_en}}$  “high” allows  $F_{IN}$  to bypass the prescaler and powers down the prescaler.

The output from the main counter chain,  $f_p$ , is related to the VCO frequency,  $F_{in}$ , by the following equation:

$$f_p = F_{IN} / [10 \times (M + 1) + A] \quad (1)$$

where  $A \leq M + 1$ ,  $1 \leq M \leq 511$

Or

$$f_p = F_{IN} / [5 \times (M + 1) + A]$$

where  $A \leq M + 1$ ,  $1 \leq M \leq 511$

When the loop is locked,  $F_{IN}$  is related to the reference frequency,  $F_R$ , by the following equation:

$$F_{IN} = [10 \times (M + 1) + A] \times [F_R / (R + 1)] \quad (2)$$

where  $A \leq M + 1$ ,  $1 \leq M \leq 511$

Or

$$F_{IN} = [5 \times (M + 1) + A] \times [F_R / (R + 1)]$$

where  $A \leq M + 1$ ,  $1 \leq M \leq 511$

A consequence of the upper limit on A is that in Integer-N mode, to obtain contiguous channels,

**$F_{IN}$  must be  $= 90 \times [F_R / (R + 1)]$  with 10/11 modulus**

**$F_{IN}$  must be  $= 20 \times [F_R / (R + 1)]$  with 5/6 modulus**

The A counter can accept values as high as 15, but in typical operation it will cycle from 0 to 9 between increments in M. Programming the M counter with the minimum allowed value of “1” will result in a minimum M counter divide ratio of “2”.

### Prescaler Bypass Mode

Setting  $\overline{\text{Pre\_en}}$  “high” allows  $F_{IN}$  to bypass and power down the prescaler. In this mode, the 5/6 or 10/11 prescaler and A register are not active, and the input VCO frequency is divided by the M counter directly. The following equation relates  $F_{in}$  to the reference frequency,  $F_R$ :

$$F_{IN} = (M + 1) \times [F_R / (R + 1)] \quad (3)$$

where  $1 \leq M \leq 511$

### Reference Counter

The reference counter chain divides the reference frequency,  $F_R$ , down to the phase detector comparison frequency,  $f_c$ .

The output frequency of the 6-bit R counter is related to the reference frequency by the following equation:

$$f_c = F_R / (R + 1) \quad (4)$$

where  $0 \leq R \leq 63$

Note that programming R with “0” will pass the reference frequency,  $F_R$ , directly to the phase detector.

### Serial Interface Mode

While the E\_WR input is “low” and the S\_WR input is “low”, serial input data (SDATA input), B<sub>0</sub> to B<sub>20</sub>, is clocked serially into the primary register on the rising edge of SCLK, MSB (B<sub>0</sub>) first. The contents from the primary register are transferred into the secondary register on the rising edge of S\_WR according to the timing diagram shown in *Figure 17*. Data is transferred to the counters as shown in *Table 7*.

While the E\_WR input is “high” and the S\_WR input is “low”, serial input data (SDATA input), B<sub>0</sub> to B<sub>7</sub>, is clocked serially into the enhancement register on the rising edge of SCLK, MSB (B<sub>0</sub>) first. The enhancement register is double buffered

to prevent inadvertent control changes during serial loading, with buffer capture of the serially-entered data performed on the falling edge of E\_WR according to the timing diagram shown in *Figure 17*. After the falling edge of E\_WR, the data provides control bits as shown in *Tables 8 and 9* with bit functionality enabled by asserting the  $\overline{\text{ENH}}$  input “low”.

### Direct Interface Mode

Direct Interface Mode is selected by setting the Direct input “high”.

Counter control bits are set directly at the pins as shown in *Table 7*.

**Table 7. Primary Register Programming**

Interface Mode	ENH	R <sub>5</sub>	R <sub>4</sub>	M <sub>8</sub>	M <sub>7</sub>	$\overline{\text{Pre\_en}}$	M <sub>6</sub>	M <sub>5</sub>	M <sub>4</sub>	M <sub>3</sub>	M <sub>2</sub>	M <sub>1</sub>	M <sub>0</sub>	R <sub>3</sub>	R <sub>2</sub>	R <sub>1</sub>	R <sub>0</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	ADDR
Serial*	1	B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>	B <sub>4</sub>	B <sub>5</sub>	B <sub>6</sub>	B <sub>7</sub>	B <sub>8</sub>	B <sub>9</sub>	B <sub>10</sub>	B <sub>11</sub>	B <sub>12</sub>	B <sub>13</sub>	B <sub>14</sub>	B <sub>15</sub>	B <sub>16</sub>	B <sub>17</sub>	B <sub>18</sub>	B <sub>19</sub>	B <sub>20</sub>
Direct	1	R <sub>5</sub>	R <sub>4</sub>	M <sub>8</sub>	M <sub>7</sub>	$\overline{\text{Pre\_en}}$	M <sub>6</sub>	M <sub>5</sub>	M <sub>4</sub>	M <sub>3</sub>	M <sub>2</sub>	M <sub>1</sub>	M <sub>0</sub>	R <sub>3</sub>	R <sub>2</sub>	R <sub>1</sub>	R <sub>0</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	0

Note: \* Serial data clocked serially on SCLK rising edge while E\_WR “low” and captured in secondary register on S\_WR rising edge.

↑  
MSB (first in)

↑  
(last in) LSB

**Table 8. Enhancement Register Programming**

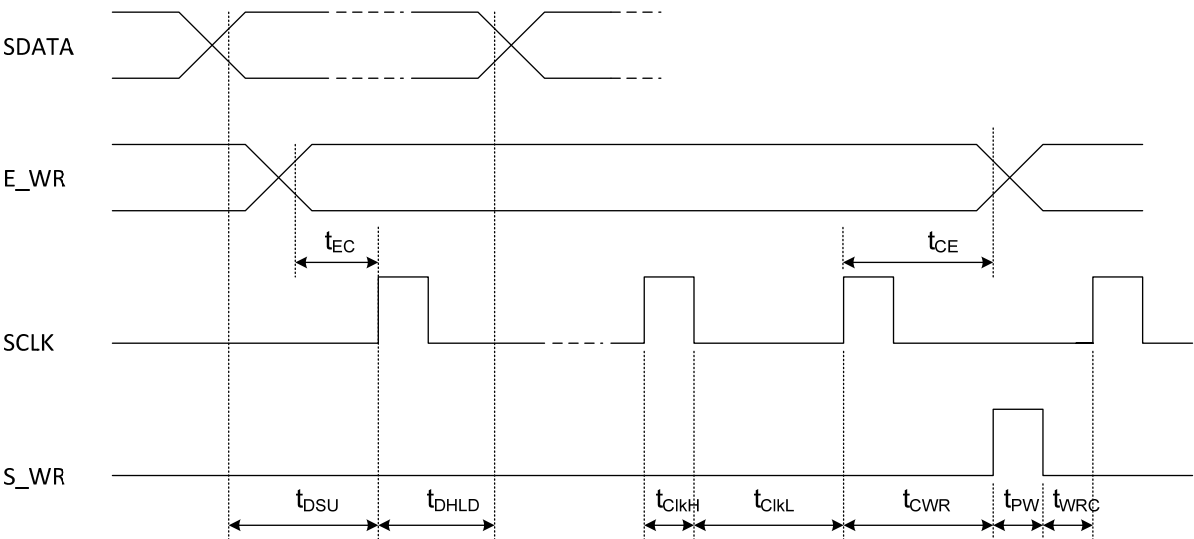
Interface Mode	ENH	Direct	Reserved	Reserved	f <sub>p</sub> output	Power Down	Counter load	MSEL output	f <sub>c</sub> output	LD Disable
Serial*	0	0	B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>	B <sub>4</sub>	B <sub>5</sub>	B <sub>6</sub>	B <sub>7</sub>

Note: \* Serial data clocked serially on SCLK rising edge while E\_WR “high” and captured in the double buffer on E\_WR falling edge.

↑  
MSB (first in)

↑  
(last in) LSB

Figure 17. Serial Interface Mode Timing Diagram



### Enhancement Register

The functions of the enhancement register bits are shown below with all bits active “high”.

Table 9. Enhancement Register Bit Functionality

Bit Function		Description
Bit 0	Reserve*	Reserved.
Bit 1	Reserve*	Reserved.
Bit 2	$f_p$ output	Drives the M counter output onto the D <sub>OUT</sub> output.
Bit 3	Power down	Power down of all functions except programming interface.
Bit 4	Counter load	Immediate and continuous load of counter programming.
Bit 5	MSEL output	Drives the internal dual modulus prescaler modulus select (MSEL) onto the D <sub>OUT</sub> output.
Bit 6	$f_c$ output	Drives the reference counter output onto the D <sub>OUT</sub> output.
Bit 7	LD Disable	Disables the LD pin for quieter operation.

Note: \* Program to 0.

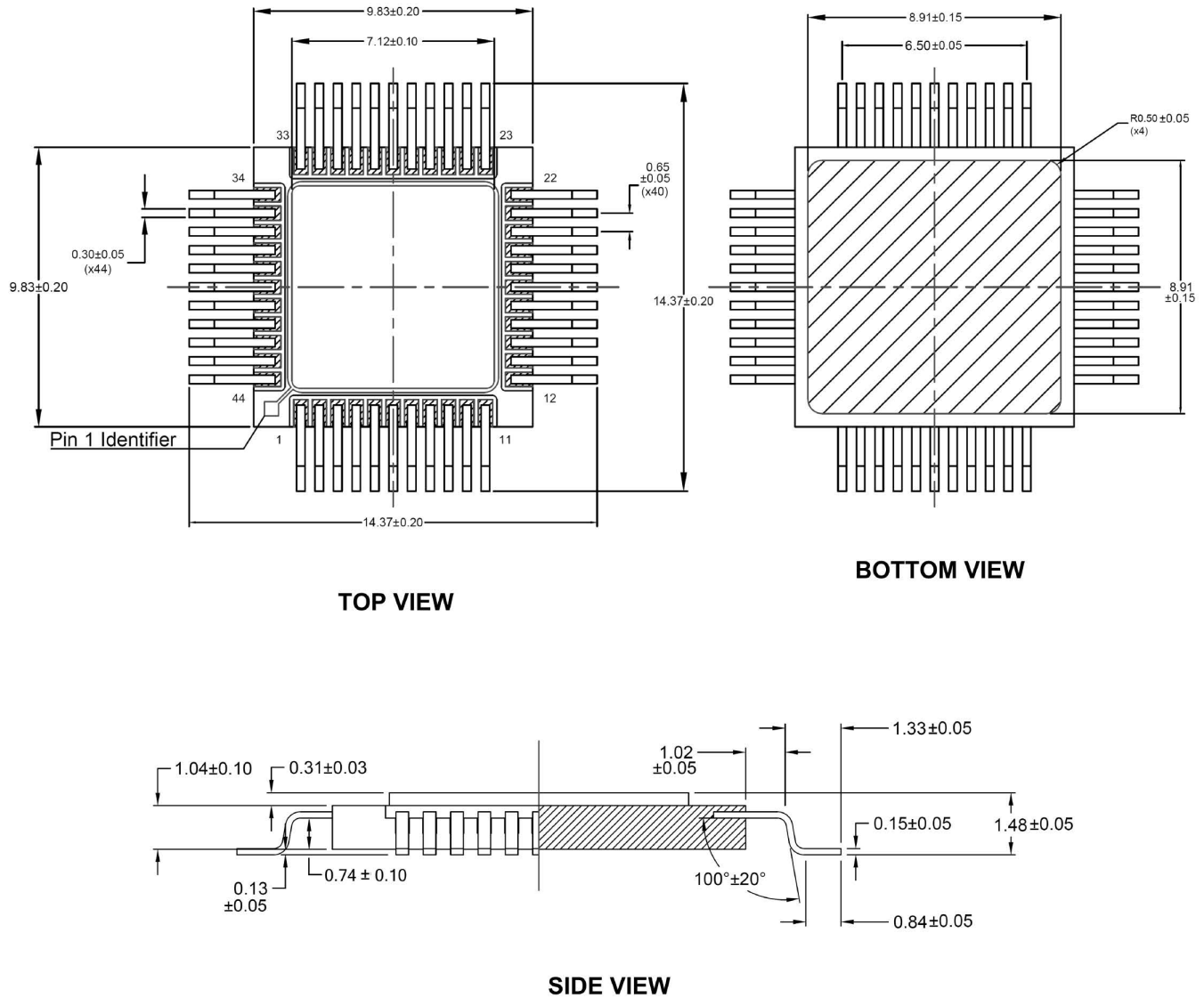
## Phase Detector

The phase detector is triggered by rising edges from the main Counter ( $f_p$ ) and the reference counter ( $f_c$ ). It has two outputs, namely  $PD_{\overline{U}}$ , and  $PD_{\overline{D}}$ . If the divided VCO leads the divided reference in phase or frequency ( $f_p$  leads  $f_c$ ),  $PD_{\overline{D}}$  pulses “low”. If the divided reference leads the divided VCO in phase or frequency ( $f_r$  leads  $f_p$ ),  $PD_{\overline{U}}$  pulses “low”. The width of either pulse is directly proportional to phase offset between the two input signals,  $f_p$  and  $f_c$ . The phase detector gain is 400 mV/radian.

$PD_{\overline{U}}$  and  $PD_{\overline{D}}$  are designed to drive an active loop filter which controls the VCO tune voltage.  $PD_{\overline{U}}$  pulses result in an increase in VCO frequency and  $PD_{\overline{D}}$  results in a decrease in VCO frequency.

A lock detect output, LD is also provided, via the pin  $C_{EXT}$ .  $C_{EXT}$  is the logical “NAND” of  $PD_{\overline{U}}$  and  $PD_{\overline{D}}$  waveforms, which is driven through a series 2 k $\Omega$  resistor. Connecting  $C_{EXT}$  to an external shunt capacitor provides integration.  $C_{EXT}$  also drives the input of an internal inverting comparator with an open drain output. Thus LD is an “AND” function of  $PD_{\overline{U}}$  and  $PD_{\overline{D}}$ . See *Figure 16* for a functional block diagram of this circuit.

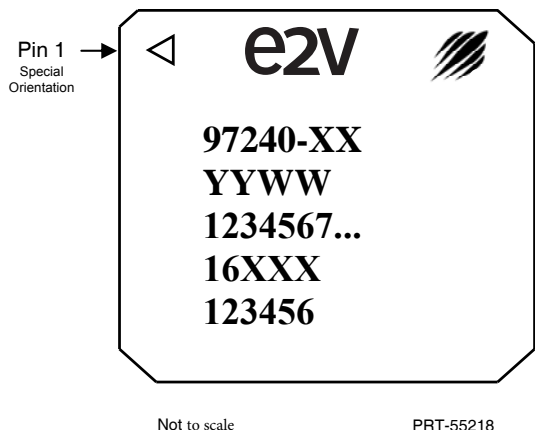
**Figure 21. Package Drawing (dimensions are in millimeters)**  
44-lead CQFP



DIMS IN MM  
NOT TO SCALE

Rev. 01 050317  
IIGNALB

**Figure 22. Top Marking Specifications**



Line 1: Pin 1 indicator  $\triangle$ , e2v and Peregrine logo  
Line 2: Part number (XX will be specified by the purchase order)  
Line 3: Date code (last two digits of the year and work week)  
Line 4: Wafer lot # (as many characters as room allows)  
Line 5: DOP # (e2v internal / 5 digits / optional, as room allows)  
Line 6: Serial # (5 digits minimum)

Note: There is **NO** backside marking on any of the Peregrine products.

**Table 10. Ordering Information**

Order Code	Description	Package	Shipping Method
97240-01*	Engineering samples	44-lead CQFP	40 units/tray
97240-11	Flight units	44-lead CQFP	40 units/tray
97240-00	Evaluation kit	Evaluation kit	1/box

Note: \* The PE97240-01 devices are ES (Engineering Sample) prototype units intended for use as initial evaluation units for customers of the PE97240-11 flight units. The PE97240-01 device provides the same functionality and footprint as the PE97240-11 space qualified device, and intended for engineering evaluation only. They are tested at +25 °C only and processed to a non-compliant flow (e.g. No burn-in, non-hermetic, etc). These units are non-hermetic and are not suitable for qualification, production, radiation testing or flight use.

## Sales Contact and Information

**Contact Information:**  
e2v ~ <http://www.teledyne-e2v.com> ~ [inquiries@e2v-us.com](mailto:inquiries@e2v-us.com)

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**Preliminary Specification:** The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.  
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