DATA SHEET
www.onsemi.com

NPN Silicon Planar Epitaxial Transistor
PZT651

This NPN Silicon Epitaxial transistor is designed for use in industrial and consumer applications. The device is housed in the SOT−223 package which is designed for medium power surface mount applications.

SOT−223 package ensures level mounting, resulting in improved thermal conduction, and allows visual inspection of soldered joints. The formed leads absorb thermal stress during soldering, eliminating the possibility of damage to the die.

Features

- High Current
- The SOT−223 Package can be Soldered Using Wave or Reflow
- PNP Complement is PZT751T1G
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	60	Vdc
Collector−Base Voltage	V_{CBO}	80	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	2.0	Adc
Total Power Dissipation @ T_A = 25°C (Note 1) Derate above 25°C	P_D	 0.8 6.4	W mW/°C
Storage Temperature Range	T_{stg}	−65 to 150	°C
Junction Temperature	T_J	150	°C

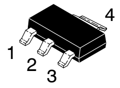
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance from Junction−to−Ambient in Free Air	$R_{\theta JA}$	156	°C/W
Maximum Temperature for Soldering Purposes Time in Solder Bath	T_L	260 10	°C Sec

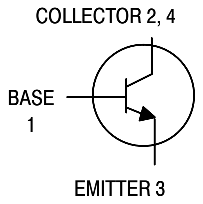
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Device mounted on a FR−4 glass epoxy printed circuit board using minimum recommended footprint.

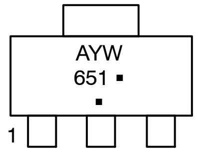
SOT−223 PACKAGE HIGH CURRENT NPN SILICON TRANSISTOR SURFACE MOUNT



SOT−223
CASE 318E−04
STYLE 1



MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
■ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping[†]
PZT651T1G	SOT−223 (Pb−Free)	1,000 / Tape & Reel
SPZT651T1G	SOT−223 (Pb−Free)	1,000 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

June, 2022 − Rev. 11

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	60	–	Vdc
Collector−Emitter Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	80	–	Vdc
Emitter−Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	5.0	–	Vdc
Base−Emitter Cutoff Current (V_{EB} = 4.0 Vdc)	I_{EBO}	–	0.1	μAdc
Collector−Base Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	–	100	nAdc
ON CHARACTERISTICS (Note 2)				
DC Current Gain	h_{FE}			–
(I_C = 50 mAdc, V_{CE} = 2.0 Vdc)		75	–	
(I_C = 500 mAdc, V_{CE} = 2.0 Vdc)		75	–	
(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)		75	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)		40	–	
Collector−Emitter Saturation Voltages	$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 200 mAdc)		–	0.5	
(I_C = 1.0 Adc, I_B = 100 mAdc)		–	0.3	
Base−Emitter Voltages (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	1.0	Vdc
Base−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 100 mAdc)	$V_{BE(sat)}$	–	1.2	Vdc
Current−Gain — Bandwidth (I_C = 50 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	75	–	MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%

TYPICAL CHARACTERISTICS

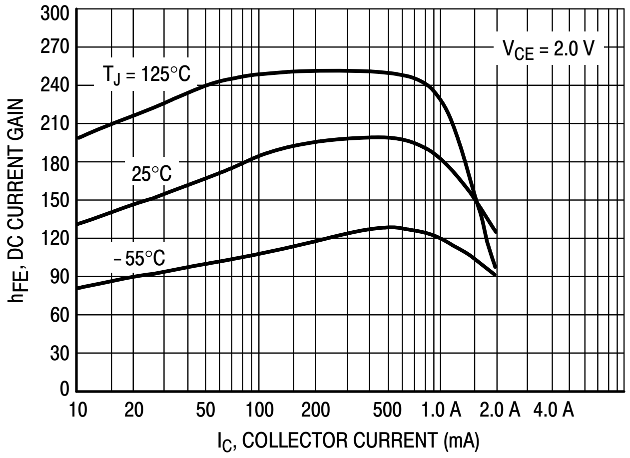


Figure 1. Typical DC Current Gain

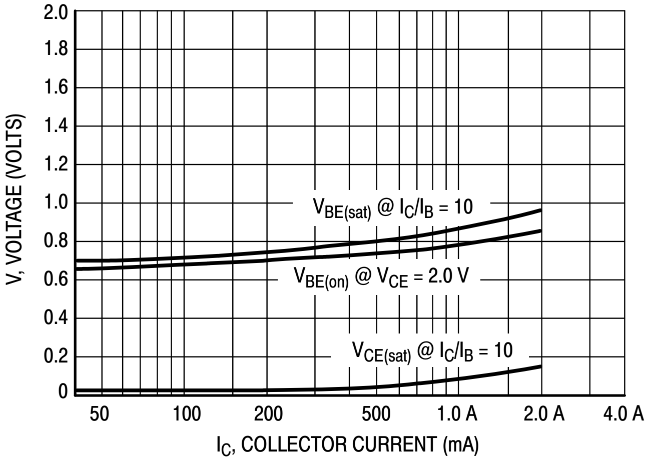


Figure 2. On Voltages

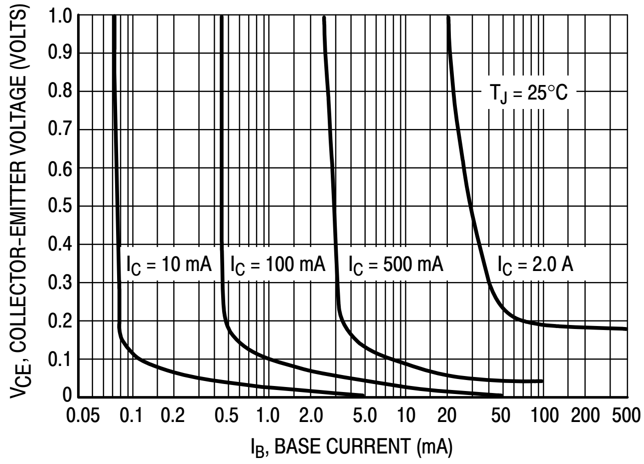


Figure 3. Collector Saturation Region

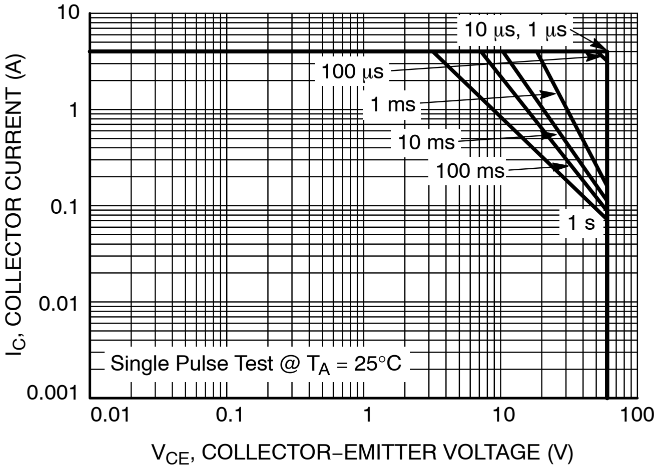
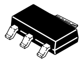


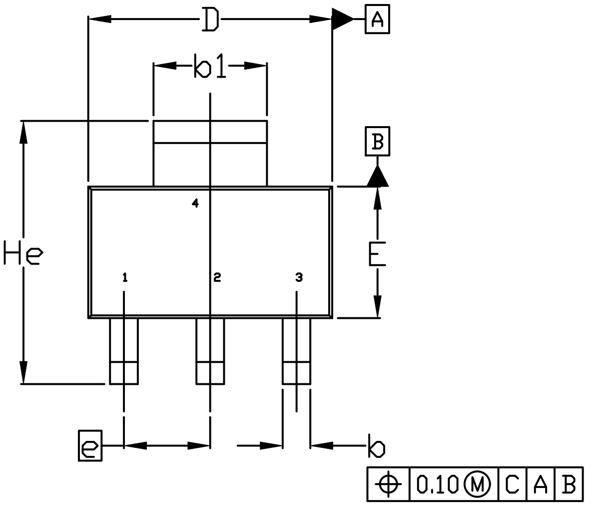
Figure 4. Safe Operating Area



SCALE 1:1

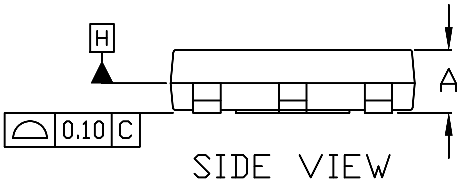
SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

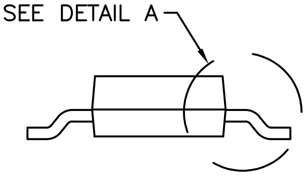


NOTE 5

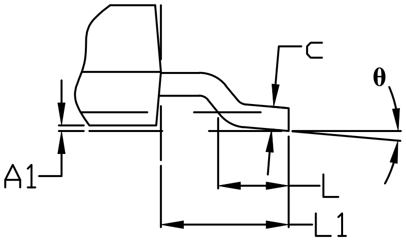
TOP VIEW



SIDE VIEW



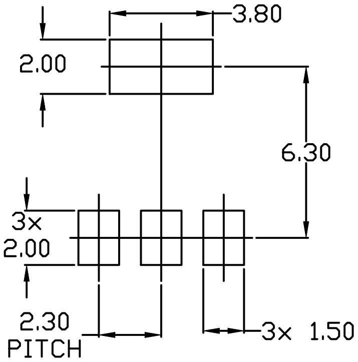
FRONT VIEW



DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

DOCUMENT NUMBER:	**98ASB42680B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOT−223 (TO−261)**	**PAGE 1 OF 2**

SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
  2. COLLECTOR
  3. EMITTER
  4. COLLECTOR

STYLE 2:
PIN 1. ANODE
  2. CATHODE
  3. NC
  4. CATHODE

STYLE 3:
PIN 1. GATE
  2. DRAIN
  3. SOURCE
  4. DRAIN

STYLE 4:
PIN 1. SOURCE
  2. DRAIN
  3. GATE
  4. DRAIN

STYLE 5:
PIN 1. DRAIN
  2. GATE
  3. SOURCE
  4. GATE

STYLE 6:
PIN 1. RETURN
  2. INPUT
  3. OUTPUT
  4. INPUT

STYLE 7:
PIN 1. ANODE 1
  2. CATHODE
  3. ANODE 2
  4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
  2. GROUND
  3. LOGIC
  4. GROUND

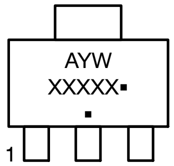
STYLE 10:
PIN 1. CATHODE
  2. ANODE
  3. GATE
  4. ANODE

STYLE 11:
PIN 1. MT 1
  2. MT 2
  3. GATE
  4. MT 2

STYLE 12:
PIN 1. INPUT
  2. OUTPUT
  3. NC
  4. OUTPUT

STYLE 13:
PIN 1. GATE
  2. COLLECTOR
  3. EMITTER
  4. COLLECTOR

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASB42680B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOT−223 (TO−261)**	**PAGE 2 OF 2**

onsemi, onsemi, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

◊

Downloaded from Arrow.com.