Capacitive Switch Controller ICs

Capacitive Switch Controller IC

BU21182FS

General Description

BU21182FS is a capacitive switch controller for switch operation. Based on the result of detecting changes in capacitance, judge the operation of Switch ON / OFF / Long Press.

Features

- 20 Capacitive Sensor Ports.
- Switch ON / OFF / Long Press Detection.
- Information by Interrupt Terminal.
- Noise Calibration Function.
- Drift Calibration Function.
- Adjust Switch Detection Time Function.
- 2-wire Serial Bus Interface.
- Single Power Supply.

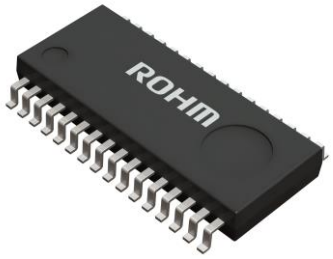
Applications

- Office Automation Appliance as Printer.
- AV Appliance as TV and HDD Recorder.
- Home Appliance as Air Conditioner, Refrigerator and Rice Cooker.
- Electrical Equipment with Multiple Switches.

Key Specifications

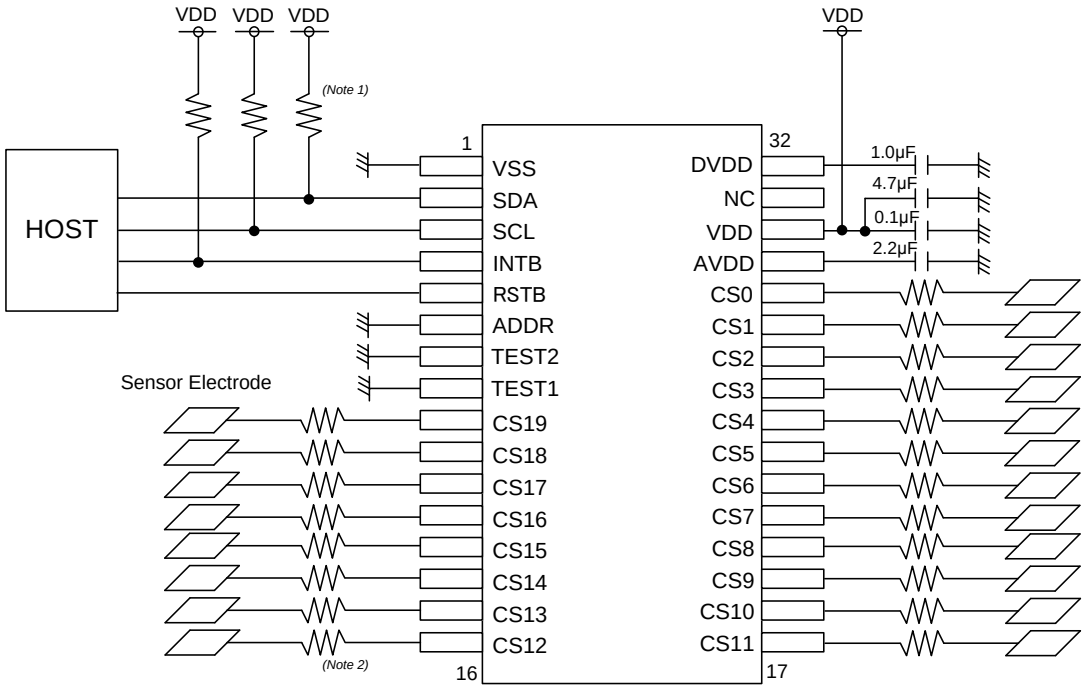
- Power Supply Voltage Range: 3.0V to 5.5V
- Operating Temperature Range: -25°C to +85°C
- Operating Current: 3.5mA(Typ)

Package	W(Typ) x D(Typ) x H(Max)
SSOP-A32	13.60mm x 7.80mm x 2.01mm



SSOP-A32

Typical Application Circuit



(Note 1) The pull-up resistors must be connected to VDD.
Choose the value of the pull-up resistors so as to meet 2-wire Serial Bus Interface Electrical Characteristics.
(Note 2) For noise protection, choose the value of the resistors by evaluation.

Figure 1. Typical Application Circuit

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Pin Configuration

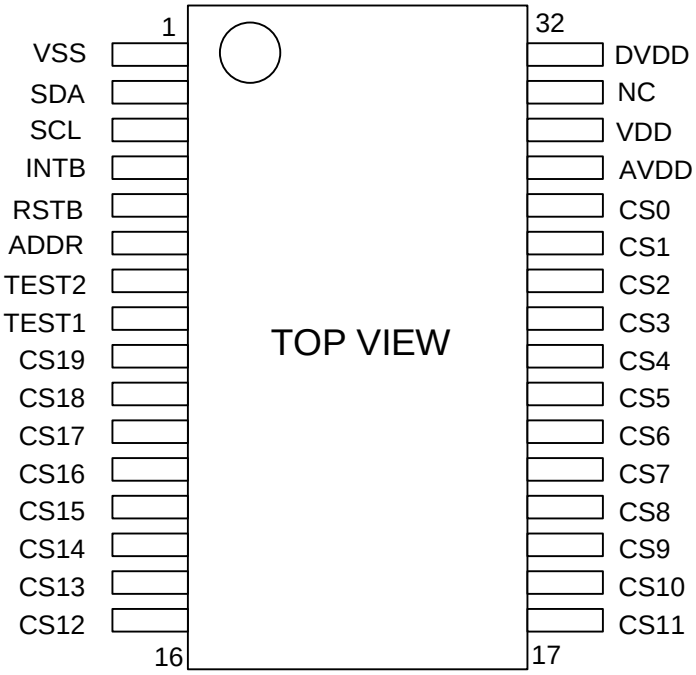


Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	I/O Type	Function	Power	Initial Condition (RSTB=L)	I/O Equivalent Circuit
1	VSS	-	Ground	-	-	-
2	SDA	IN/OUT	Host interface pin: Serial Data Line	VDD	HIZ	Figure 3
3	SCL	IN/OUT	Host interface pin: Serial Clock Line	VDD	HIZ	Figure 3
4	INTB	OUT	Interrupt pin Active low interrupt	VDD	HIZ	Figure 3
5	RSTB	IN	Reset pin L : Reset H : Normal Operate	VDD	L	Figure 4
6	ADDR	IN	7bit Slave address selection pin L : Slave address 0x5C H : Slave address 0x5D	VDD	HIZ	Figure 4
7	TEST2	IN	Test pin Connect to Ground.	VDD	HIZ	Figure 4
8	TEST1	IN	Test pin Connect to Ground.	VDD	HIZ	Figure 4
9	CS19	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
10	CS18	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
11	CS17	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
12	CS16	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
13	CS15	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
14	CS14	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
15	CS13	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
16	CS12	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5

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Pin Description - continued

Pin No.	Pin Name	I/O Type	Function	Power	Initial Condition (RSTB=L)	I/O Equivalent Circuit
17	CS11	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
18	CS10	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
19	CS9	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
20	CS8	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
21	CS7	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
22	CS6	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
23	CS5	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
24	CS4	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
25	CS3	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
26	CS2	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
27	CS1	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
28	CS0	IN/OUT	Sensor pin(Note 3)	AVDD	HIZ	Figure 5
29	AVDD	OUT	LDO output pin for sensor block	-	0V	-
30	VDD	-	Power	-	-	-
31	NC	-	No Connect pin with pull-down resistor This pin should be left as open circuit	-	-	-
32	DVDD	OUT	LDO output pin for digital block	-	1.5V	-

(Note 3) If not used, this pin must be left as an open circuit.

I/O Equivalent Circuit

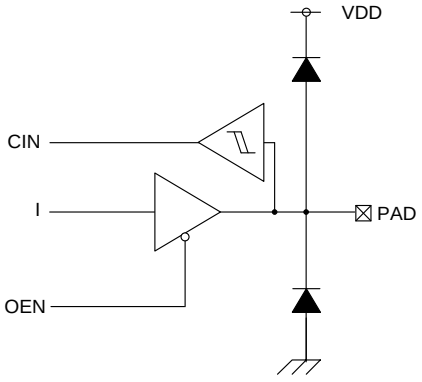


Figure 3. I/O Equivalent Circuit

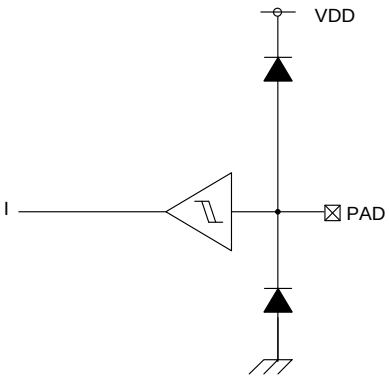


Figure 4. I/O Equivalent Circuit

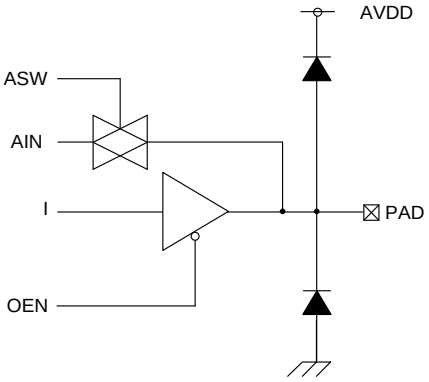


Figure 5. I/O Equivalent Circuit

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Block Diagram

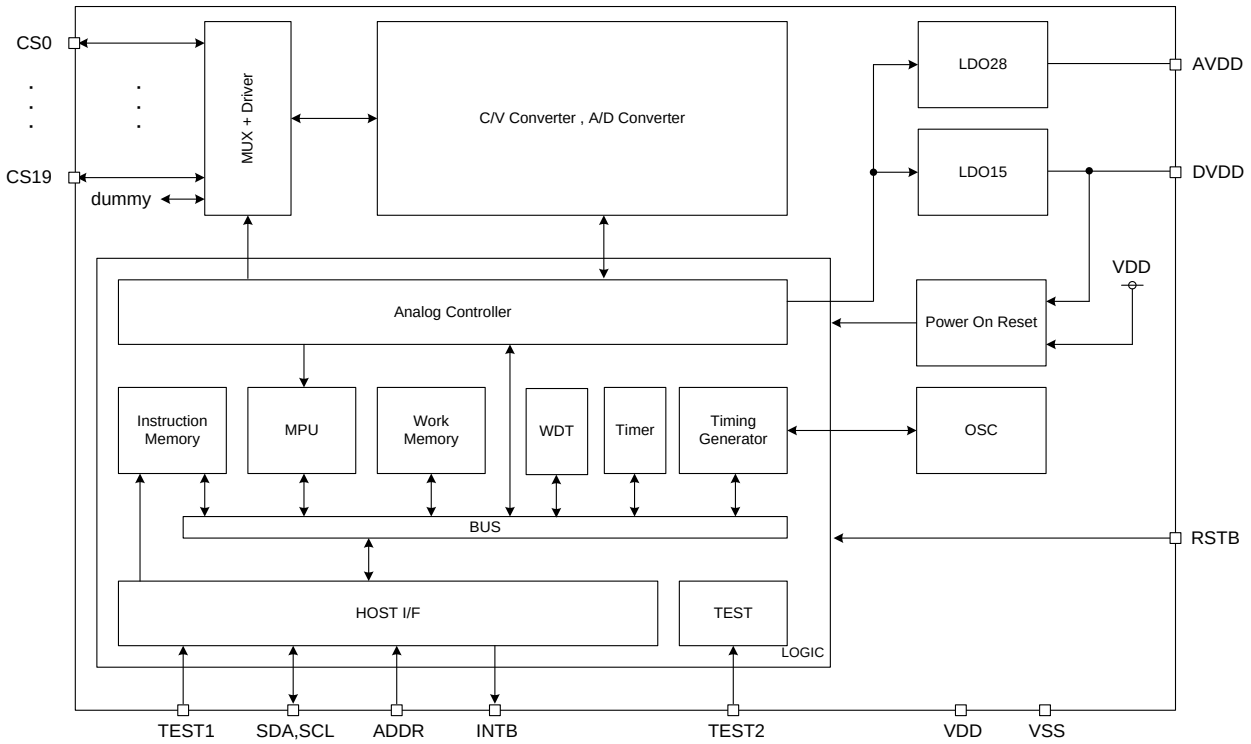


Figure 6. Block Diagram

Description of Block

MUX, Driver, C/V Converter, A/D Converter
This block converts from capacitance to voltage and the voltage to digital value for each sensor.

LDO28
This block is AVDD LDO that supplies 2.8V to MUX, Driver, C/V Converter and A/D Converter. Referred to as AVDD in this document.

LDO15
This block is DVDD LDO that supplies 1.5V to OSC and LOGIC. Referred to as DVDD in this document.

OSC
This block is ring oscillator for MPU and LOGIC.

MPU
This block detects ON / OFF / Long Press of switches and performs automatic calibration based on the detection results. The result is informed by the INTB pin.

Instruction Memory
This block is Program ROM for MPU.

Work Memory
This block is Working RAM for MPU.

HOST I/F
2-wire serial bus interface compatible with I^2C protocol.

Analog Controller
This block is control sequencer for MUX, Driver, C/V Converter and A/D Converter.

WDT
This block is watchdog timer reset. When the MPU is hang-upped, the system is reset by WDT.

Timing Generator, Timer
This block generates clock for MPU peripherals based on OSC clock.

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Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Terminal Voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Maximum Junction Temperature	Tjmax	125	°C
Storage Temperature Range	Tstg	-55 to +125	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance*(Note 4)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 6)*	2s2p*(Note 7)*	
SSOP-A32				
Junction to Ambient	θ_{JA}	82.9	45.2	°C/W
Junction to Top Characterization Parameter*(Note 5)*	Ψ_{JT}	6	6	°C/W

(Note 4) Based on JESD51-2A(Still-Air)

(Note 5) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 6) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 7) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	3.0	5.0	5.5	V
Operating Temperature	Topr	-25	+25	+85	°C

Electrical Characteristics (Unless otherwise specified V_{DD}=5.0V Ta=25°C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input High Voltage	V_{IH}	V_{DD} x 0.7	-	V_{DD} + 0.3	V	-
Input Low Voltage	V_{IL}	V_{SS} - 0.3	-	V_{DD} x 0.3	V	-
Output High Voltage	V_{OHCS}	V_{AVDD} x 0.7	-	V_{AVDD}	V	I_{OH} = -1mA (CS pin)
Output Low Voltage	V_{OLCS}	V_{SS}	-	V_{AVDD} x 0.3	V	I_{OL} = +1mA (CS pin)
	V_{OL1}	V_{SS}	-	V_{SS} + 0.4	V	I_{OL} = +3mA (SDA/SCL/INTB pin)
	V_{OL2}	V_{SS}	-	V_{SS} + 0.6	V	I_{OL} = +6mA (SDA/SCL/INTB pin)
Oscillator Clock Frequency	f_{OSC}	45	50	55	MHz	-
DVDD LDO Output Voltage	V_{DVDD}	1.35	1.50	1.65	V	-
AVDD LDO Output Voltage	V_{AVDD}	2.67	2.80	2.93	V	When AVDD is set to 2.8V.
Standby Current	I_{STBY}	-	70	200	µA	RSTB=L
Active Current	I_{ACT}	1.9	3.5	5.0	mA	RSTB=H and Sensor enable CS terminals: No load

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Interface Specification

2-wire Serial Bus Interface
Compatible with I²C Protocol
Support Slave Mode Only
7bit Slave Address = 0x5C (in case of ADDR=L) / 0x5D (in case of ADDR=H)
Support Sequential Read
Support Clock Stretching

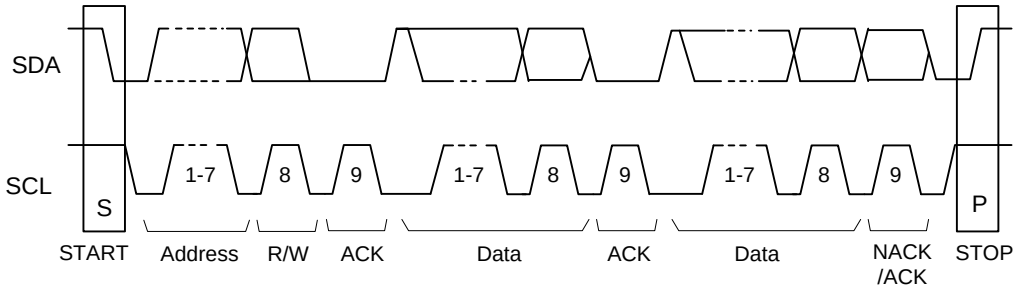


Figure 7. 2-wire Serial Bus Data Format

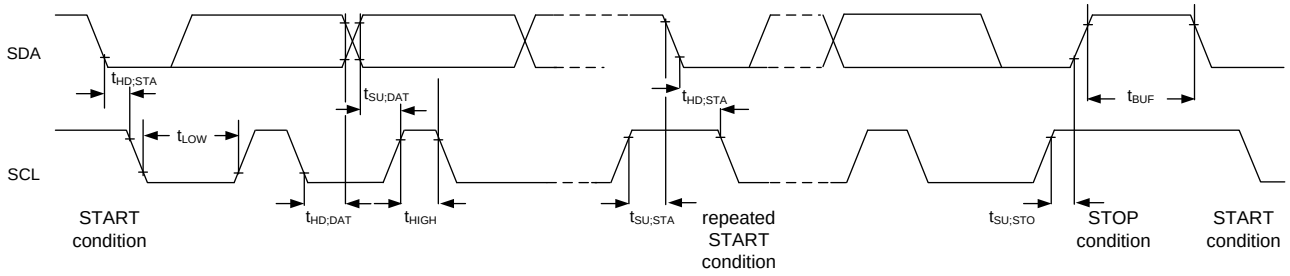


Figure 8. 2-wire Serial Bus Data Timing Chart

2-wire Serial Bus Interface Electrical Characteristics (Unless otherwise specified V_{DD}=5.0V Ta=25°C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
SCL Clock Frequency	f_{SCL}	0	-	400	kHz	-
Hold Time (repeated) START Condition	$t_{HD;STA}$	0.6	-	-	µs	-
Low Period of the SCL Clock	t_{LOW}	1.3	-	-	µs	-
High Period of the SCL Clock	t_{HIGH}	0.6	-	-	µs	-
Data Hold Time	$t_{HD;DAT}$	0	-	-	µs	-
Data Set-up Time	$t_{SU;DAT}$	0.1	-	-	µs	-
Set-up Time for a Repeated START Condition	$t_{SU;STA}$	0.6	-	-	µs	-
Set-up Time for STOP Condition	$t_{SU;STO}$	0.6	-	-	µs	-
Bus Free Time between STOP and START Condition	t_{BUF}	1.3	-	-	µs	-

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2-wire Serial Bus Protocol

Write Protocol

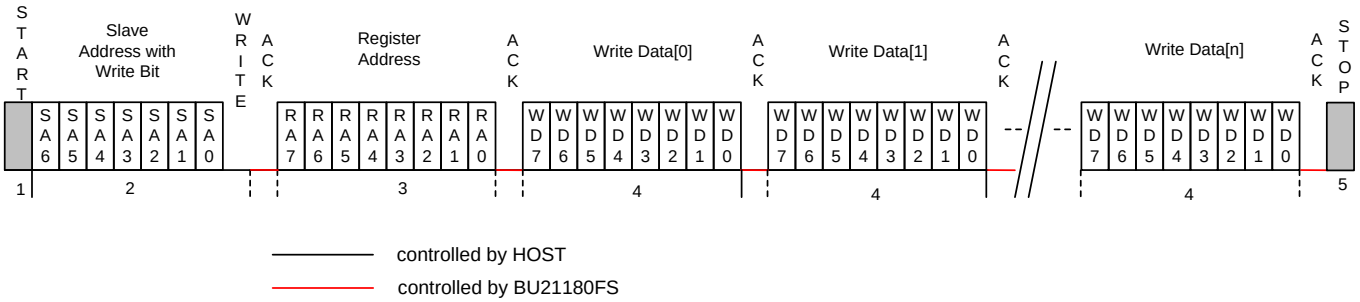


Figure 9. 2-wire Serial Bus Write Protocol

1: The communication starts when IC received the START condition.
2: IC transmits ACK signal when 7-bit slave address and write bit are received. IC carries out processing by MPU after the transmission of ACK signal. Clock stretch is carried out during the processing.
3: IC transmits ACK signal when 8-bit write register address are received. IC carries out processing by MPU after the transmission of ACK signal. Clock stretch is carried out during the processing.
4: IC transmits ACK signal when 8-bit write data are received. IC carries out processing by MPU after the transmission of ACK signal. Clock stretch is carried out during the processing. IC supports sequential write. So the register address is incremented, and the next of 0xFF becomes 0x00.
5: The communication finishes when IC received the STOP condition.

Read Protocol

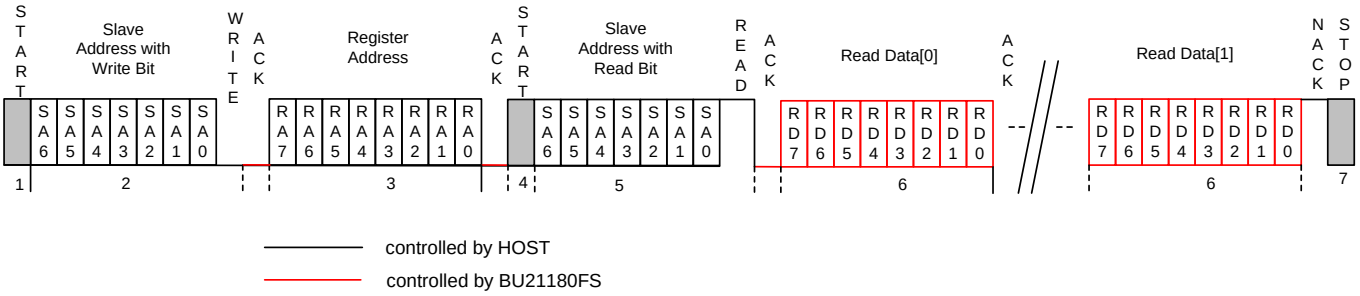


Figure 10. 2-wire Serial Bus Read Protocol

1: The communication starts when IC received the START condition.
2: IC transmits ACK signal when 7-bit slave address and write bit are received. IC carries out processing by MPU after the transmission of ACK signal. Clock stretch is carried out during the processing.
3: IC transmits ACK signal when 8-bit read register address are received. IC carries out processing by MPU after the transmission of ACK signal. Clock stretch is carried out during the processing.
4: The communication continues when IC received start condition signal.
5: IC transmits ACK signal when 7-bit slave address and read bit are received. IC carries out processing by MPU after the transmission of ACK signal. Clock stretch is carried out during the processing.
6: IC transmits read data every clock is received until NACK signal. IC carries out processing by MPU after receiving ACK or NACK signal. Clock stretch is carried out during the processing. IC supports sequential read. So the register address is incremented, and the next of 0xFF becomes 0x00.
7: The communication finishes when IC received the STOP condition.

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Power-on Sequence / Reset Timing

Built-in LDO (DVDD) boots after VDD power is supplied. The reset condition is released by setting RSTB from low to high after DVDD booted. IC is accessible from host after initializing MPU. IC is accessible from host after the build-in power-on reset circuit was released in the case the RSTB pin is connected to the VDD pin. The filter circuit is integrated for the RSTB pin. The signal less than “Rejected RSTB Pulse Width” are rejected by the filter. To initialize IC, the signal larger than “Detected RSTB Pulse Width” is required.

Power-on Flowchart

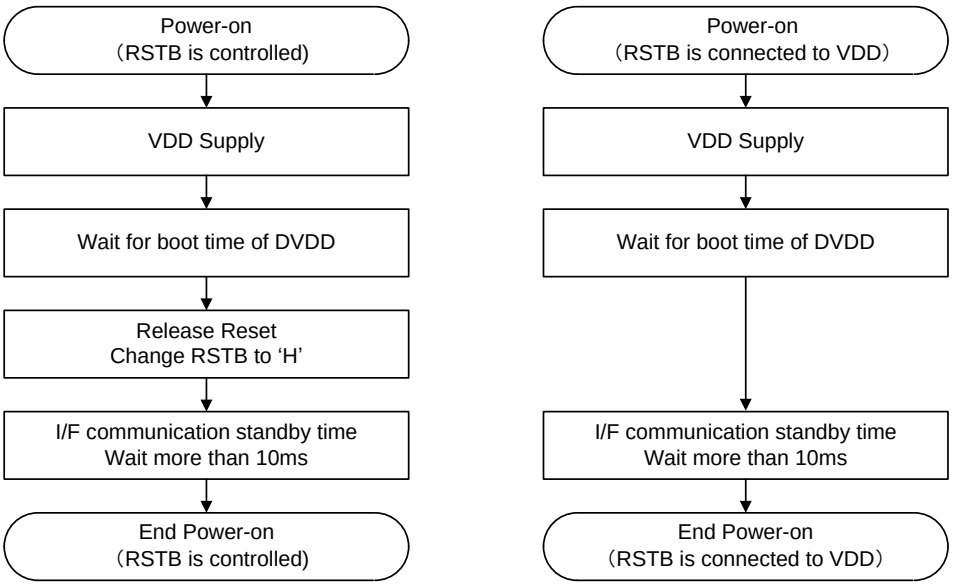


Figure 11. Power-on Flowchart

Power-on Timing

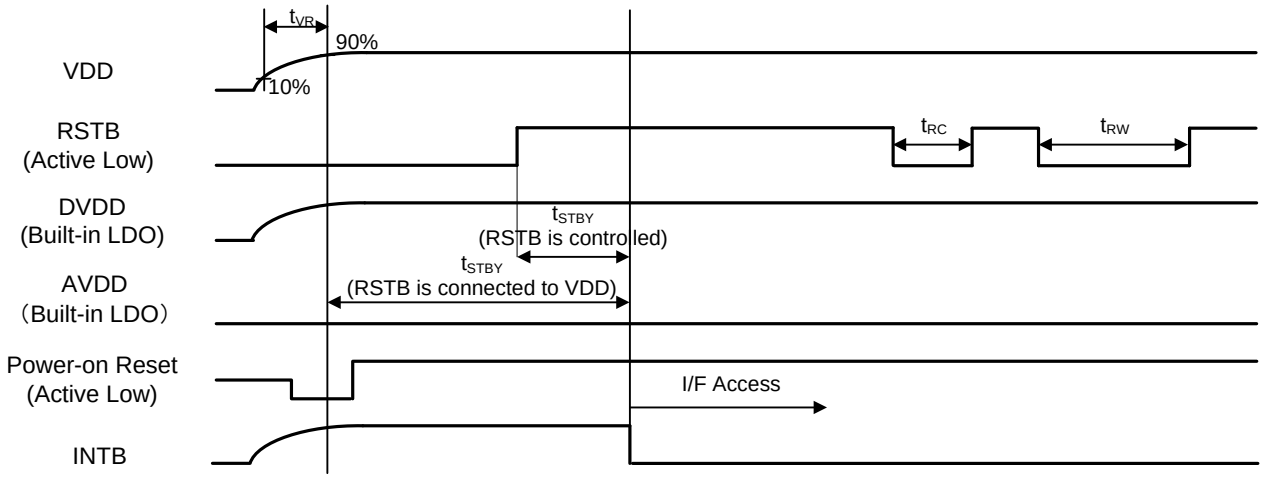


Figure 12. Power-on Timing

Power-on / Reset Timing Electrical Characteristics (Unless otherwise specified V_{DD}=5.0V Ta=25°C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
VDD Rise Time	t_{VR}	1	-	10	ms	-
I/F Communication Standby Time	t_{STBY}	-	-	10	ms	-
Rejected RSTB Pulse Width	t_{RC}	-	-	3	µs	-
Detected RSTB Pulse Width	t_{RW}	10	-	-	µs	-

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Register Map

Unless otherwise specified oscillator frequency is 50MHz.
Accessing the reserved area is prohibited.
Initial value is the value after initialization by MPU.

Status Register

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	R	0x00	DATA_CS0[7:0]							
0x01	R	0x00	DATA_CS1[7:0]							
0x02	R	0x00	DATA_CS2[7:0]							
0x03	R	0x00	DATA_CS3[7:0]							
0x04	R	0x00	DATA_CS4[7:0]							
0x05	R	0x00	DATA_CS5[7:0]							
0x06	R	0x00	DATA_CS6[7:0]							
0x07	R	0x00	DATA_CS7[7:0]							
0x08	R	0x00	DATA_CS8[7:0]							
0x09	R	0x00	DATA_CS9[7:0]							
0x0A	R	0x00	DATA_CS10[7:0]							
0x0B	R	0x00	DATA_CS11[7:0]							
0x0C	R	0x00	DATA_CS12[7:0]							
0x0D	R	0x00	DATA_CS13[7:0]							
0x0E	R	0x00	DATA_CS14[7:0]							
0x0F	R	0x00	DATA_CS15[7:0]							
0x10	R	0x00	DATA_CS16[7:0]							
0x11	R	0x00	DATA_CS17[7:0]							
0x12	R	0x00	DATA_CS18[7:0]							
0x13	R	0x00	DATA_CS19[7:0]							
0x14	-	-	RESERVED							
0x15	R	0x00	FDATA_CS0[15:8]							
0x16	R	0x00	FDATA_CS0[7:0]							
0x17	R	0x00	FDATA_CS1[15:8]							
0x18	R	0x00	FDATA_CS1[7:0]							
0x19	R	0x00	FDATA_CS2[15:8]							
0x1A	R	0x00	FDATA_CS2[7:0]							
0x1B	R	0x00	FDATA_CS3[15:8]							
0x1C	R	0x00	FDATA_CS3[7:0]							
0x1D	R	0x00	FDATA_CS4[15:8]							
0x1E	R	0x00	FDATA_CS4[7:0]							
0x1F	R	0x00	FDATA_CS5[15:8]							
0x20	R	0x00	FDATA_CS5[7:0]							
0x21	R	0x00	FDATA_CS6[15:8]							
0x22	R	0x00	FDATA_CS6[7:0]							
0x23	R	0x00	FDATA_CS7[15:8]							
0x24	R	0x00	FDATA_CS7[7:0]							
0x25	R	0x00	FDATA_CS8[15:8]							
0x26	R	0x00	FDATA_CS8[7:0]							
0x27	R	0x00	FDATA_CS9[15:8]							
0x28	R	0x00	FDATA_CS9[7:0]							
0x29	R	0x00	FDATA_CS10[15:8]							
0x2A	R	0x00	FDATA_CS10[7:0]							
0x2B	R	0x00	FDATA_CS11[15:8]							
0x2C	R	0x00	FDATA_CS11[7:0]							

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Register Map - continued

Status Register

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x2D	R	0x00	FDATA_CS12[15:8]							
0x2E	R	0x00	FDATA_CS12[7:0]							
0x2F	R	0x00	FDATA_CS13[15:8]							
0x30	R	0x00	FDATA_CS13[7:0]							
0x31	R	0x00	FDATA_CS14[15:8]							
0x32	R	0x00	FDATA_CS14[7:0]							
0x33	R	0x00	FDATA_CS15[15:8]							
0x34	R	0x00	FDATA_CS15[7:0]							
0x35	R	0x00	FDATA_CS16[15:8]							
0x36	R	0x00	FDATA_CS16[7:0]							
0x37	R	0x00	FDATA_CS17[15:8]							
0x38	R	0x00	FDATA_CS17[7:0]							
0x39	R	0x00	FDATA_CS18[15:8]							
0x3A	R	0x00	FDATA_CS18[7:0]							
0x3B	R	0x00	FDATA_CS19[15:8]							
0x3C	R	0x00	FDATA_CS19[7:0]							
0x3D-0x3F	-	-	RESERVED							
0x40	R	0x01	INT_NOISE	INT_UNK	-	-	INT_FALCAL	INT_FINCAL	-	INT_FININI
0x41	R	0x00	-	-	INT_MULT_OFF	INT_MULT_ON	INT_HLDRPT	INT_HLD	INT_SW_OFF	INT_SW_ON
0x42	R	0x00	-	-	-	-	-	-	INT_AVDDOFF	INT_AVDDON
0x43	R	0x00	DET_ON_CS7	DET_ON_CS6	DET_ON_CS5	DET_ON_CS4	DET_ON_CS3	DET_ON_CS2	DET_ON_CS1	DET_ON_CS0
0x44	R	0x00	DET_ON_CS15	DET_ON_CS14	DET_ON_CS13	DET_ON_CS12	DET_ON_CS11	DET_ON_CS10	DET_ON_CS9	DET_ON_CS8
0x45	R	0x00	-	-	-	-	DET_ON_CS19	DET_ON_CS18	DET_ON_CS17	DET_ON_CS16
0x46	R	0x00	DET_OFF_CS7	DET_OFF_CS6	DET_OFF_CS5	DET_OFF_CS4	DET_OFF_CS3	DET_OFF_CS2	DET_OFF_CS1	DET_OFF_CS0
0x47	R	0x00	DET_OFF_CS15	DET_OFF_CS14	DET_OFF_CS13	DET_OFF_CS12	DET_OFF_CS11	DET_OFF_CS10	DET_OFF_CS9	DET_OFF_CS8
0x48	R	0x00	-	-	-	-	DET_OFF_CS19	DET_OFF_CS18	DET_OFF_CS17	DET_OFF_CS16
0x49	R	0x00	DET_HLD_CS7	DET_HLD_CS6	DET_HLD_CS5	DET_HLD_CS4	DET_HLD_CS3	DET_HLD_CS2	DET_HLD_CS1	DET_HLD_CS0
0x4A	R	0x00	DET_HLD_CS15	DET_HLD_CS14	DET_HLD_CS13	DET_HLD_CS12	DET_HLD_CS11	DET_HLD_CS10	DET_HLD_CS9	DET_HLD_CS8
0x4B	R	0x00	-	-	-	-	DET_HLD_CS19	DET_HLD_CS18	DET_HLD_CS17	DET_HLD_CS16
0x4C	R	0x00	DET_HLD RPT_CS7	DET_HLD RPT_CS6	DET_HLD RPT_CS5	DET_HLD RPT_CS4	DET_HLD RPT_CS3	DET_HLD RPT_CS2	DET_HLD RPT_CS1	DET_HLD RPT_CS0
0x4D	R	0x00	DET_HLD RPT_CS15	DET_HLD RPT_CS14	DET_HLD RPT_CS13	DET_HLD RPT_CS12	DET_HLD RPT_CS11	DET_HLD RPT_CS10	DET_HLD RPT_CS9	DET_HLD RPT_CS8
0x4E	R	0x00	-	-	-	-	DET_HLD RPT_CS19	DET_HLD RPT_CS18	DET_HLD RPT_CS17	DET_HLD RPT_CS16
0x4F	R	0x00	DET_MULT_ON_H	DET_MULT_ON_G	DET_MULT_ON_F	DET_MULT_ON_E	DET_MULT_ON_D	DET_MULT_ON_C	DET_MULT_ON_B	DET_MULT_ON_A
0x50	R	0x00	DET_MULT OFF_H	DET_MULT OFF_G	DET_MULT OFF_F	DET_MULT OFF_E	DET_MULT OFF_D	DET_MULT OFF_C	DET_MULT OFF_B	DET_MULT OFF_A
0x51	R	0x00	DET_UNK_CS7	DET_UNK_CS6	DET_UNK_CS5	DET_UNK_CS4	DET_UNK_CS3	DET_UNK_CS2	DET_UNK_CS1	DET_UNK_CS0
0x52	R	0x00	DET_UNK_CS15	DET_UNK_CS14	DET_UNK_CS13	DET_UNK_CS12	DET_UNK_CS11	DET_UNK_CS10	DET_UNK_CS9	DET_UNK_CS8
0x53	R	0x00	-	-	-	-	DET_UNK_CS19	DET_UNK_CS18	DET_UNK_CS17	DET_UNK_CS16
0x54	R	0x00	SW_STAT_CS7	SW_STAT_CS6	SW_STAT_CS5	SW_STAT_CS4	SW_STAT_CS3	SW_STAT_CS2	SW_STAT_CS1	SW_STAT_CS0
0x55	R	0x00	SW_STAT_CS15	SW_STAT_CS14	SW_STAT_CS13	SW_STAT_CS12	SW_STAT_CS11	SW_STAT_CS10	SW_STAT_CS9	SW_STAT_CS8
0x56	R	0x00	-	-	-	-	SW_STAT_CS19	SW_STAT_CS18	SW_STAT_CS17	SW_STAT_CS16
0x57	R	0x00	-	-	-	-	-	RUN_CAL	RUN_AFE	-
0x58	R	0x00	NUM_FALCAL[7:0]							
0x59-0x5E	-	-	RESERVED							
0x5F	R	0x0D	FW_VER[7:0]							

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Register Map - continued

Configuration Register

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x60	R/W	0x00	CS3_SCAN_SEL[1:0]		CS2_SCAN_SEL[1:0]		CS1_SCAN_SEL[1:0]		CS0_SCAN_SEL[1:0]	
0x61	R/W	0x00	CS7_SCAN_SEL[1:0]		CS6_SCAN_SEL[1:0]		CS5_SCAN_SEL[1:0]		CS4_SCAN_SEL[1:0]	
0x62	R/W	0x50	CS11_SCAN_SEL[1:0]		CS10_SCAN_SEL[1:0]		CS9_SCAN_SEL[1:0]		CS8_SCAN_SEL[1:0]	
0x63	R/W	0x55	CS15_SCAN_SEL[1:0]		CS14_SCAN_SEL[1:0]		CS13_SCAN_SEL[1:0]		CS12_SCAN_SEL[1:0]	
0x64	R/W	0x55	CS19_SCAN_SEL[1:0]		CS18_SCAN_SEL[1:0]		CS17_SCAN_SEL[1:0]		CS16_SCAN_SEL[1:0]	
0x65	-	-	RESERVED							
0x66	R/W	0x7F	VAL_GA_CS1[3:0]				VAL_GA_CS0[3:0]			
0x67	R/W	0x77	VAL_GA_CS3[3:0]				VAL_GA_CS2[3:0]			
0x68	R/W	0x77	VAL_GA_CS5[3:0]				VAL_GA_CS4[3:0]			
0x69	R/W	0x77	VAL_GA_CS7[3:0]				VAL_GA_CS6[3:0]			
0x6A	R/W	0x77	VAL_GA_CS9[3:0]				VAL_GA_CS8[3:0]			
0x6B	R/W	0xFF	VAL_GA_CS11[3:0]				VAL_GA_CS10[3:0]			
0x6C	R/W	0xFF	VAL_GA_CS13[3:0]				VAL_GA_CS12[3:0]			
0x6D	R/W	0xFF	VAL_GA_CS15[3:0]				VAL_GA_CS14[3:0]			
0x6E	R/W	0xFF	VAL_GA_CS17[3:0]				VAL_GA_CS16[3:0]			
0x6F	R/W	0xFF	VAL_GA_CS19[3:0]				VAL_GA_CS18[3:0]			
0x70	R/W	0xC8	VAL_TH_ON_CS0[7:0]							
0x71	R/W	0x64	VAL_TH_OFF_CS0[7:0]							
0x72	R/W	0xC8	VAL_TH_ON_CS1[7:0]							
0x73	R/W	0x64	VAL_TH_OFF_CS1[7:0]							
0x74	R/W	0xC8	VAL_TH_ON_CS2[7:0]							
0x75	R/W	0x64	VAL_TH_OFF_CS2[7:0]							
0x76	R/W	0xC8	VAL_TH_ON_CS3[7:0]							
0x77	R/W	0x64	VAL_TH_OFF_CS3[7:0]							
0x78	R/W	0xC8	VAL_TH_ON_CS4[7:0]							
0x79	R/W	0x64	VAL_TH_OFF_CS4[7:0]							
0x7A	R/W	0xC8	VAL_TH_ON_CS5[7:0]							
0x7B	R/W	0x64	VAL_TH_OFF_CS5[7:0]							
0x7C	R/W	0xC8	VAL_TH_ON_CS6[7:0]							
0x7D	R/W	0x64	VAL_TH_OFF_CS6[7:0]							
0x7E	R/W	0xC8	VAL_TH_ON_CS7[7:0]							
0x7F	R/W	0x64	VAL_TH_OFF_CS7[7:0]							
0x80	R/W	0xC8	VAL_TH_ON_CS8[7:0]							
0x81	R/W	0x64	VAL_TH_OFF_CS8[7:0]							
0x82	R/W	0xC8	VAL_TH_ON_CS9[7:0]							
0x83	R/W	0x64	VAL_TH_OFF_CS9[7:0]							
0x84	R/W	0xC8	VAL_TH_ON_CS10[7:0]							
0x85	R/W	0x64	VAL_TH_OFF_CS10[7:0]							
0x86	R/W	0xC8	VAL_TH_ON_CS11[7:0]							
0x87	R/W	0x64	VAL_TH_OFF_CS11[7:0]							
0x88	R/W	0xC8	VAL_TH_ON_CS12[7:0]							
0x89	R/W	0x64	VAL_TH_OFF_CS12[7:0]							
0x8A	R/W	0xC8	VAL_TH_ON_CS13[7:0]							
0x8B	R/W	0x64	VAL_TH_OFF_CS13[7:0]							
0x8C	R/W	0xC8	VAL_TH_ON_CS14[7:0]							
0x8D	R/W	0x64	VAL_TH_OFF_CS14[7:0]							
0x8E	R/W	0xC8	VAL_TH_ON_CS15[7:0]							
0x8F	R/W	0x64	VAL_TH_OFF_CS15[7:0]							

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Register Map - continued

Configuration Register

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x90	R/W	0xC8	VAL_TH_ON_CS16[7:0]							
0x91	R/W	0x64	VAL_TH_OFF_CS16[7:0]							
0x92	R/W	0xC8	VAL_TH_ON_CS17[7:0]							
0x93	R/W	0x64	VAL_TH_OFF_CS17[7:0]							
0x94	R/W	0xC8	VAL_TH_ON_CS18[7:0]							
0x95	R/W	0x64	VAL_TH_OFF_CS18[7:0]							
0x96	R/W	0xC8	VAL_TH_ON_CS19[7:0]							
0x97	R/W	0x64	VAL_TH_OFF_CS19[7:0]							
0x98	R/W	0x30	VAL_ADJ_DAT[3:0]				-	-	-	-
0x99	R/W	0x50	-	TIM_AFE[2:0]			-	-	-	-
0x9A	R/W	0x03	-	-	-	-	-	FIL_CFG[2:0]		
0x9B	R/W	0x80	MLT_SW _EN	-	-	CAL_SFT _EN	LOWER _CAL_EN	UNK_CAL _EN	ADJ_OFS _ENB	SCAN _SEL
0x9C	R/W	0x03	-	-	-	-	OST[3:0]			
0x9D	R/W	0x09	ADJ_ALL _EN	-	-	ADJ_DET_NUM[4:0]				
0x9E	R/W	0x89	NOISE _SFT_EN	-	-	NOISE_DET_NUM[4:0]				
0x9F	R/W	0x3C	TIME_PERCAL[7:0]							
0xA0-0xA1	R/W	0x00	RESERVED							
0xA2	R/W	0x00	TIME_UNKNOWN_A[7:0]							
0xA3	R/W	0x00	TIME_UNKNOWN_B[7:0]							
0xA4	R/W	0x00	TIME_HLD_A[7:0]							
0xA5	R/W	0x00	TIME_HLD_RPT_A[7:0]							
0xA6	R/W	0x00	TIME_HLD_B[7:0]							
0xA7	R/W	0x00	TIME_HLD_RPT_B[7:0]							
0xA8	R/W	0x00	TIME_HLD_C[7:0]							
0xA9	R/W	0x00	TIME_HLD_RPT_C[7:0]							
0xAA	R/W	0x00	TIME_HLD_D[7:0]							
0xAB	R/W	0x00	TIME_HLD_RPT_D[7:0]							
0xAC	R/W	0x00	TIME_HLD_E[7:0]							
0xAD	R/W	0x00	TIME_HLD_RPT_E[7:0]							
0xAE	R/W	0x00	TIME_HLD_F[7:0]							
0xAF	R/W	0x00	TIME_HLD_RPT_F[7:0]							
0xB0	R/W	0x00	TIME_HLD_G[7:0]							
0xB1	R/W	0x00	TIME_HLD_RPT_G[7:0]							
0xB2	R/W	0x00	UNK_CS1	HLD_CS1[2:0]			UNK_CS0	HLD_CS0[2:0]		
0xB3	R/W	0x00	UNK_CS3	HLD_CS3[2:0]			UNK_CS2	HLD_CS2[2:0]		
0xB4	R/W	0x00	UNK_CS5	HLD_CS5[2:0]			UNK_CS4	HLD_CS4[2:0]		
0xB5	R/W	0x00	UNK_CS7	HLD_CS7[2:0]			UNK_CS6	HLD_CS6[2:0]		
0xB6	R/W	0x00	UNK_CS9	HLD_CS9[2:0]			UNK_CS8	HLD_CS8[2:0]		
0xB7	R/W	0x00	UNK_CS11	HLD_CS11[2:0]			UNK_CS10	HLD_CS10[2:0]		
0xB8	R/W	0x00	UNK_CS13	HLD_CS13[2:0]			UNK_CS12	HLD_CS12[2:0]		
0xB9	R/W	0x00	UNK_CS15	HLD_CS15[2:0]			UNK_CS14	HLD_CS14[2:0]		
0xBA	R/W	0x00	UNK_CS17	HLD_CS17[2:0]			UNK_CS16	HLD_CS16[2:0]		
0xBB	R/W	0x00	UNK_CS19	HLD_CS19[2:0]			UNK_CS18	HLD_CS18[2:0]		

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Register Map - continued

Configuration Register

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xBC	R/W	0x00	TIME_DET[7:0]							
0xBD	R/W	0x00	MULT_A_CS7	MULT_A_CS6	MULT_A_CS5	MULT_A_CS4	MULT_A_CS3	MULT_A_CS2	MULT_A_CS1	MULT_A_CS0
0xBE	R/W	0x00	MULT_A_CS15	MULT_A_CS14	MULT_A_CS13	MULT_A_CS12	MULT_A_CS11	MULT_A_CS10	MULT_A_CS9	MULT_A_CS8
0xBF	R/W	0x00	-	-	-	-	MULT_A_CS19	MULT_A_CS18	MULT_A_CS17	MULT_A_CS16
0xC0	R/W	0x00	MULT_B_CS7	MULT_B_CS6	MULT_B_CS5	MULT_B_CS4	MULT_B_CS3	MULT_B_CS2	MULT_B_CS1	MULT_B_CS0
0xC1	R/W	0x00	MULT_B_CS15	MULT_B_CS14	MULT_B_CS13	MULT_B_CS12	MULT_B_CS11	MULT_B_CS10	MULT_B_CS9	MULT_B_CS8
0xC2	R/W	0x00	-	-	-	-	MULT_B_CS19	MULT_B_CS18	MULT_B_CS17	MULT_B_CS16
0xC3	R/W	0x00	MULT_C_CS7	MULT_C_CS6	MULT_C_CS5	MULT_C_CS4	MULT_C_CS3	MULT_C_CS2	MULT_C_CS1	MULT_C_CS0
0xC4	R/W	0x00	MULT_C_CS15	MULT_C_CS14	MULT_C_CS13	MULT_C_CS12	MULT_C_CS11	MULT_C_CS10	MULT_C_CS9	MULT_C_CS8
0xC5	R/W	0x00	-	-	-	-	MULT_C_CS19	MULT_C_CS18	MULT_C_CS17	MULT_C_CS16
0xC6	R/W	0x00	MULT_D_CS7	MULT_D_CS6	MULT_D_CS5	MULT_D_CS4	MULT_D_CS3	MULT_D_CS2	MULT_D_CS1	MULT_D_CS0
0xC7	R/W	0x00	MULT_D_CS15	MULT_D_CS14	MULT_D_CS13	MULT_D_CS12	MULT_D_CS11	MULT_D_CS10	MULT_D_CS9	MULT_D_CS8
0xC8	R/W	0x00	-	-	-	-	MULT_D_CS19	MULT_D_CS18	MULT_D_CS17	MULT_D_CS16
0xC9	R/W	0x00	MULT_E_CS7	MULT_E_CS6	MULT_E_CS5	MULT_E_CS4	MULT_E_CS3	MULT_E_CS2	MULT_E_CS1	MULT_E_CS0
0xCA	R/W	0x00	MULT_E_CS15	MULT_E_CS14	MULT_E_CS13	MULT_E_CS12	MULT_E_CS11	MULT_E_CS10	MULT_E_CS9	MULT_E_CS8
0xCB	R/W	0x00	-	-	-	-	MULT_E_CS19	MULT_E_CS18	MULT_E_CS17	MULT_E_CS16
0xCC	R/W	0x00	MULT_F_CS7	MULT_F_CS6	MULT_F_CS5	MULT_F_CS4	MULT_F_CS3	MULT_F_CS2	MULT_F_CS1	MULT_F_CS0
0xCD	R/W	0x00	MULT_F_CS15	MULT_F_CS14	MULT_F_CS13	MULT_F_CS12	MULT_F_CS11	MULT_F_CS10	MULT_F_CS9	MULT_F_CS8
0xCE	R/W	0x00	-	-	-	-	MULT_F_CS19	MULT_F_CS18	MULT_F_CS17	MULT_F_CS16
0xCF	R/W	0x00	MULT_G_CS7	MULT_G_CS6	MULT_G_CS5	MULT_G_CS4	MULT_G_CS3	MULT_G_CS2	MULT_G_CS1	MULT_G_CS0
0xD0	R/W	0x00	MULT_G_CS15	MULT_G_CS14	MULT_G_CS13	MULT_G_CS12	MULT_G_CS11	MULT_G_CS10	MULT_G_CS9	MULT_G_CS8
0xD1	R/W	0x00	-	-	-	-	MULT_G_CS19	MULT_G_CS18	MULT_G_CS17	MULT_G_CS16
0xD2	R/W	0x00	MULT_H_CS7	MULT_H_CS6	MULT_H_CS5	MULT_H_CS4	MULT_H_CS3	MULT_H_CS2	MULT_H_CS1	MULT_H_CS0
0xD3	R/W	0x00	MULT_H_CS15	MULT_H_CS14	MULT_H_CS13	MULT_H_CS12	MULT_H_CS11	MULT_H_CS10	MULT_H_CS9	MULT_H_CS8
0xD4	R/W	0x00	-	-	-	-	MULT_H_CS19	MULT_H_CS18	MULT_H_CS17	MULT_H_CS16
0xD5	R/W	0x00	MSK_INT_NOISE	-	-	-	MSK_INT_FALCAL	MSK_INT_FINCAL	-	-
0xD6	R/W	0x00	-	-	-	-	-	-	MSK_INT_AVDDOFF	MSK_INT_AVDDON
0xD7	R/W	0x00	MSK_DET_ON_CS7	MSK_DET_ON_CS6	MSK_DET_ON_CS5	MSK_DET_ON_CS4	MSK_DET_ON_CS3	MSK_DET_ON_CS2	MSK_DET_ON_CS1	MSK_DET_ON_CS0
0xD8	R/W	0x00	MSK_DET_ON_CS15	MSK_DET_ON_CS14	MSK_DET_ON_CS13	MSK_DET_ON_CS12	MSK_DET_ON_CS11	MSK_DET_ON_CS10	MSK_DET_ON_CS9	MSK_DET_ON_CS8
0xD9	R/W	0x00	-	-	-	-	MSK_DET_ON_CS19	MSK_DET_ON_CS18	MSK_DET_ON_CS17	MSK_DET_ON_CS16
0xDA	R/W	0x00	MSK_DET_OFF_CS7	MSK_DET_OFF_CS6	MSK_DET_OFF_CS5	MSK_DET_OFF_CS4	MSK_DET_OFF_CS3	MSK_DET_OFF_CS2	MSK_DET_OFF_CS1	MSK_DET_OFF_CS0
0xDB	R/W	0x00	MSK_DET_OFF_CS15	MSK_DET_OFF_CS14	MSK_DET_OFF_CS13	MSK_DET_OFF_CS12	MSK_DET_OFF_CS11	MSK_DET_OFF_CS10	MSK_DET_OFF_CS9	MSK_DET_OFF_CS8
0xDC	R/W	0x00	-	-	-	-	MSK_DET_OFF_CS19	MSK_DET_OFF_CS18	MSK_DET_OFF_CS17	MSK_DET_OFF_CS16
0xDD	R/W	0x00	MSK_UNK_CS7	MSK_UNK_CS6	MSK_UNK_CS5	MSK_UNK_CS4	MSK_UNK_CS3	MSK_UNK_CS2	MSK_UNK_CS1	MSK_UNK_CS0
0xDE	R/W	0x00	MSK_UNK_CS15	MSK_UNK_CS14	MSK_UNK_CS13	MSK_UNK_CS12	MSK_UNK_CS11	MSK_UNK_CS10	MSK_UNK_CS9	MSK_UNK_CS8
0xDF	R/W	0x00	-	-	-	-	MSK_UNK_CS19	MSK_UNK_CS18	MSK_UNK_CS17	MSK_UNK_CS16

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Register Map - continued

Command Register

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE0	R/W	0x00	CLR_INT_NOISE	-	-	-	CLR_INT_FALCAL	CLR_INT_FINCAL	-	CLR_INT_FININI
0xE1	R/W	0x00	-	-	-	-	-	-	CLR_INT_AVDDOFF	CLR_INT_AVDDON
0xE2	R/W	0x00	CLR_DET_ON_CS7	CLR_DET_ON_CS6	CLR_DET_ON_CS5	CLR_DET_ON_CS4	CLR_DET_ON_CS3	CLR_DET_ON_CS2	CLR_DET_ON_CS1	CLR_DET_ON_CS0
0xE3	R/W	0x00	CLR_DET_ON_CS15	CLR_DET_ON_CS14	CLR_DET_ON_CS13	CLR_DET_ON_CS12	CLR_DET_ON_CS11	CLR_DET_ON_CS10	CLR_DET_ON_CS9	CLR_DET_ON_CS8
0xE4	R/W	0x00	-	-	-	-	CLR_DET_ON_CS19	CLR_DET_ON_CS18	CLR_DET_ON_CS17	CLR_DET_ON_CS16
0xE5	R/W	0x00	CLR_DET_OFF_CS7	CLR_DET_OFF_CS6	CLR_DET_OFF_CS5	CLR_DET_OFF_CS4	CLR_DET_OFF_CS3	CLR_DET_OFF_CS2	CLR_DET_OFF_CS1	CLR_DET_OFF_CS0
0xE6	R/W	0x00	CLR_DET_OFF_CS15	CLR_DET_OFF_CS14	CLR_DET_OFF_CS13	CLR_DET_OFF_CS12	CLR_DET_OFF_CS11	CLR_DET_OFF_CS10	CLR_DET_OFF_CS9	CLR_DET_OFF_CS8
0xE7	R/W	0x00	-	-	-	-	CLR_DET_OFF_CS19	CLR_DET_OFF_CS18	CLR_DET_OFF_CS17	CLR_DET_OFF_CS16
0xE8	R/W	0x00	CLR_HLD_CS7	CLR_HLD_CS6	CLR_HLD_CS5	CLR_HLD_CS4	CLR_HLD_CS3	CLR_HLD_CS2	CLR_HLD_CS1	CLR_HLD_CS0
0xE9	R/W	0x00	CLR_HLD_CS15	CLR_HLD_CS14	CLR_HLD_CS13	CLR_HLD_CS12	CLR_HLD_CS11	CLR_HLD_CS10	CLR_HLD_CS9	CLR_HLD_CS8
0xEA	R/W	0x00	-	-	-	-	CLR_HLD_CS19	CLR_HLD_CS18	CLR_HLD_CS17	CLR_HLD_CS16
0xEB	R/W	0x00	CLR_HLD RPT_CS7	CLR_HLD RPT_CS6	CLR_HLD RPT_CS5	CLR_HLD RPT_CS4	CLR_HLD RPT_CS3	CLR_HLD RPT_CS2	CLR_HLD RPT_CS1	CLR_HLD RPT_CS0
0xEC	R/W	0x00	CLR_HLD RPT_CS15	CLR_HLD RPT_CS14	CLR_HLD RPT_CS13	CLR_HLD RPT_CS12	CLR_HLD RPT_CS11	CLR_HLD RPT_CS10	CLR_HLD RPT_CS9	CLR_HLD RPT_CS8
0xED	R/W	0x00	-	-	-	-	CLR_HLD RPT_CS19	CLR_HLD RPT_CS18	CLR_HLD RPT_CS17	CLR_HLD RPT_CS16
0xEE	R/W	0x00	CLR_MULT_ON_H	CLR_MULT_ON_G	CLR_MULT_ON_F	CLR_MULT_ON_E	CLR_MULT_ON_D	CLR_MULT_ON_C	CLR_MULT_ON_B	CLR_MULT_ON_A
0xEF	R/W	0x00	CLR_MULT_OFF_H	CLR_MULT_OFF_G	CLR_MULT_OFF_F	CLR_MULT_OFF_E	CLR_MULT_OFF_D	CLR_MULT_OFF_C	CLR_MULT_OFF_B	CLR_MULT_OFF_A
0xF0	R/W	0x00	CLR_UNK_CS7	CLR_UNK_CS6	CLR_UNK_CS5	CLR_UNK_CS4	CLR_UNK_CS3	CLR_UNK_CS2	CLR_UNK_CS1	CLR_UNK_CS0
0xF1	R/W	0x00	CLR_UNK_CS15	CLR_UNK_CS14	CLR_UNK_CS13	CLR_UNK_CS12	CLR_UNK_CS11	CLR_UNK_CS10	CLR_UNK_CS9	CLR_UNK_CS8
0xF2	R/W	0x00	-	-	-	-	CLR_UNK_CS19	CLR_UNK_CS18	CLR_UNK_CS17	CLR_UNK_CS16
0xF3	R/W	0x00	SRST[7:0]							
0xF4	R/W	0x00	SRST[15:8]							
0xF5-0xFD	-	-	RESERVED							
0xFE	R/W	0x00	-	-	SEL_AVDD[1:0]		-	-	-	AVDD_ON
0xFF	R/W	0x00	-	-	-	-	-	STR_CFG	STR_CAL	STR_AFE

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Register Description

Status Register Description

0x00-0x13: Sensor Data

Name: DATA_CS
Address: 0x00-0x13
Description: These registers show 8-bit sensor data of each sensor. These are compared with the register "Switch ON Threshold / Switch OFF Threshold", and these results are set to the register "Switch ON Detection" and "Switch OFF Detection". These 8-bit sensor data become 0 after calibration.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	R	0x00	DATA_CS0[7:0]							
0x01	R	0x00	DATA_CS1[7:0]							
0x02	R	0x00	DATA_CS2[7:0]							
0x03	R	0x00	DATA_CS3[7:0]							
0x04	R	0x00	DATA_CS4[7:0]							
0x05	R	0x00	DATA_CS5[7:0]							
0x06	R	0x00	DATA_CS6[7:0]							
0x07	R	0x00	DATA_CS7[7:0]							
0x08	R	0x00	DATA_CS8[7:0]							
0x09	R	0x00	DATA_CS9[7:0]							
0x0A	R	0x00	DATA_CS10[7:0]							
0x0B	R	0x00	DATA_CS11[7:0]							
0x0C	R	0x00	DATA_CS12[7:0]							
0x0D	R	0x00	DATA_CS13[7:0]							
0x0E	R	0x00	DATA_CS14[7:0]							
0x0F	R	0x00	DATA_CS15[7:0]							
0x10	R	0x00	DATA_CS16[7:0]							
0x11	R	0x00	DATA_CS17[7:0]							
0x12	R	0x00	DATA_CS18[7:0]							
0x13	R	0x00	DATA_CS19[7:0]							

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0x15-0x3C: Filter Sensor Data

Name: FILTER_DATA_CS
Address: 0x15-0x3C
Description: These registers show RAW sensor data of each sensor from 0 to 5000 after calibration. The values of the register "Sensor Data" are the processed values of the amount of change of these registers. The bit "INT_FALCAL" in the register "Interrupt Factor" is set to 1 and calibration is performed again when this register does not become within the range from 2186 to 2814 after calibration.

The relationship between the register "Sensor Data" and the register "Filter Sensor Data" is as follows. The associated registers are the register "Sensitivity" and the register "Digital Gain".

The register "Sensor Data" =
[(The register "Filter Sensor Data" - 2500) - (315 ÷ The register "Sensitivity")] ÷ (The register "Digital Gain" + 1)

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x15	R	0x00	FDATA_CS0[15:8]							
0x16	R	0x00	FDATA_CS0[7:0]							
0x17	R	0x00	FDATA_CS1[15:8]							
0x18	R	0x00	FDATA_CS1[7:0]							
0x19	R	0x00	FDATA_CS2[15:8]							
0x1A	R	0x00	FDATA_CS2[7:0]							
0x1B	R	0x00	FDATA_CS3[15:8]							
0x1C	R	0x00	FDATA_CS3[7:0]							
0x1D	R	0x00	FDATA_CS4[15:8]							
0x1E	R	0x00	FDATA_CS4[7:0]							
0x1F	R	0x00	FDATA_CS5[15:8]							
0x20	R	0x00	FDATA_CS5[7:0]							
0x21	R	0x00	FDATA_CS6[15:8]							
0x22	R	0x00	FDATA_CS6[7:0]							
0x23	R	0x00	FDATA_CS7[15:8]							
0x24	R	0x00	FDATA_CS7[7:0]							
0x25	R	0x00	FDATA_CS8[15:8]							
0x26	R	0x00	FDATA_CS8[7:0]							
0x27	R	0x00	FDATA_CS9[15:8]							
0x28	R	0x00	FDATA_CS9[7:0]							
0x29	R	0x00	FDATA_CS10[15:8]							
0x2A	R	0x00	FDATA_CS10[7:0]							
0x2B	R	0x00	FDATA_CS11[15:8]							
0x2C	R	0x00	FDATA_CS11[7:0]							
0x2D	R	0x00	FDATA_CS12[15:8]							
0x2E	R	0x00	FDATA_CS12[7:0]							
0x2F	R	0x00	FDATA_CS13[15:8]							
0x30	R	0x00	FDATA_CS13[7:0]							
0x31	R	0x00	FDATA_CS14[15:8]							
0x32	R	0x00	FDATA_CS14[7:0]							
0x33	R	0x00	FDATA_CS15[15:8]							
0x34	R	0x00	FDATA_CS15[7:0]							
0x35	R	0x00	FDATA_CS16[15:8]							
0x36	R	0x00	FDATA_CS16[7:0]							
0x37	R	0x00	FDATA_CS17[15:8]							
0x38	R	0x00	FDATA_CS17[7:0]							
0x39	R	0x00	FDATA_CS18[15:8]							
0x3A	R	0x00	FDATA_CS18[7:0]							
0x3B	R	0x00	FDATA_CS19[15:8]							
0x3C	R	0x00	FDATA_CS19[7:0]							

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0x40-0x42: Interrupt Factor

Name: INTERRUPT
Address: 0x40-0x42
Description: These registers show the interrupt factor. The INTB pin outputs low level when the logical disjunction (hereinafter, referred to as “OR”) of the register address 0x40-0x42 becomes to 1, and outputs HIZ when the result becomes 0. In the case the bit "MLT_SW_EN" in the register "Control Mode" is set to 0, while the OR of the register address 0x41 is 1, the other switch operations are not detected. After the OR becomes 0, the next switch operation is detectable.

0: Interrupt is undetected 1: Interrupt is detected

INT_FININI : Initialization Completion Interrupt
When the initialization of MPU is completed, this bit is set to 1. This bit is cleared by setting 0 to the bit “CLR_INT_FININI” in the register “Clear Interrupt Factor”.

INT_FINCAL : Software Calibration Completion Interrupt
When software calibration is completed, this bit is set to 1. This bit is cleared by setting 0 to the bit “CLR_INT_FINCAL” in the register “Clear Interrupt Factor”.

INT_FALCAL : Calibration Failure Interrupt
When software calibration is failed, this bit is set to 1. This bit is cleared by setting 0 to the bit “CLR_INT_FALCAL” in the register “Clear Interrupt Factor”.

INT_UNK : Unexpected Long Press Detection Interrupt
When unexpected long press is detected, this bit is set to 1. The bit is set to 1 when the OR of the register “Unexpected Long Press Detection” is 1. This bit is cleared by setting 0 to the register “Clear Unexpected Long Press Detection”.

INT_NOISE : Noise Detection Interrupt
When the sensors detect the noise, this bit is set to 1. This bit is cleared by setting 0 to the bit “CLR_INT_NOISE” in the register “Clear Interrupt Factor”.

INT_SW_ON : Switch ON Detection Interrupt
When the OR of the register “Switch ON Detection” is 1, this bit is set to 1. This bit is cleared by setting 0 to the register “Clear Switch ON Detection”.

INT_SW_OFF : Switch OFF Detection Interrupt
When the OR of the register “Switch OFF Detection” is 1, this bit is set to 1. This bit is cleared by setting 0 to the register “Clear Switch OFF Detection”.

INT_HLD : Switch Long Press Detection Interrupt
When the OR of the register “Switch Long Press Detection” is 1, this bit is set to 1. This bit is cleared by setting 0 to the register “Clear Switch Long Press Detection”.

INT_HLDRPT : Switch Repeated Long Press Detection Interrupt
When the OR of the register “Switch Repeated Long Press Detection” is 1, this bit is set to 1. This bit is cleared by setting 0 to the register “Clear Switch Repeated Long Press Detection”.

INT_MULT_ON : Multiple Pattern Switches ON Detection Interrupt
When the OR of the register “Multiple Pattern Switches ON Detection” is 1, this bit is set to 1. This bit is cleared by setting 0 to the register “Clear Multiple Pattern Switches ON Detection”.

INT_MULT_OFF: Multiple Pattern Switches OFF Detection Interrupt
When the OR of the register “Multiple Pattern Switches OFF Detection” is 1, this bit is set to 1. This bit is cleared by setting 0 to the register “Clear Multiple Pattern Switches OFF Detection”.

INT_AVDDON : AVDD ON Detection Interrupt
When AVDD voltage outputs, this bit is set to 1. This bit is cleared by setting 0 to the bit “CLR_INT_AVDDON” in the register “Clear Interrupt Factor”. This function is not for failure diagnosis of AVDD.

INT_AVDDOFF : AVDD OFF Detection Interrupt
When AVDD voltage does not output, this bit is set to 1. This bit is cleared by setting 0 to the bit “CLR_INT_AVDDOFF” in the register “Clear Interrupt Factor”. This function is not for failure diagnosis of AVDD.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x40	R	0x01	INT_ NOISE	INT_UNK	-	-	INT_ FALCAL	INT_ FINCAL	-	INT_ FININI
0x41	R	0x00	-	-	INT_MULT _OFF	INT_MULT _ON	INT_ HLDRPT	INT_HLD	INT_ SW_OFF	INT_ SW_ON
0x42	R	0x00	-	-	-	-	-	-	INT_ AVDDOFF	INT_ AVDDON

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0x43-0x45: Switch ON Detection

Name: DET_ON
Address: 0x43-0x45
Description: These registers show the state of each switch changed from OFF to ON. The bit "INT_SW_ON" in the register "Interrupt Factor" shows the OR of these registers. These are cleared by setting 0 to the register "Clear Switch ON Detection".

0: ON-undetected 1: ON-detected

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x43	R	0x00	DET_ON_CS7	DET_ON_CS6	DET_ON_CS5	DET_ON_CS4	DET_ON_CS3	DET_ON_CS2	DET_ON_CS1	DET_ON_CS0
0x44	R	0x00	DET_ON_CS15	DET_ON_CS14	DET_ON_CS13	DET_ON_CS12	DET_ON_CS11	DET_ON_CS10	DET_ON_CS9	DET_ON_CS8
0x45	R	0x00	-	-	-	-	DET_ON_CS19	DET_ON_CS18	DET_ON_CS17	DET_ON_CS16

0x46-0x48: Switch OFF Detection

Name: DET_OFF
Address: 0x46-0x48
Description: These registers show the state of each switch changed from ON to OFF. The bit "INT_SW_OFF" in the register Interrupt Factor shows the OR of these registers. These are cleared by setting 0 to the register "Clear Switch OFF Detection".

0: OFF-undetected 1: OFF-detected

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x46	R	0x00	DET_OFF_CS7	DET_OFF_CS6	DET_OFF_CS5	DET_OFF_CS4	DET_OFF_CS3	DET_OFF_CS2	DET_OFF_CS1	DET_OFF_CS0
0x47	R	0x00	DET_OFF_CS15	DET_OFF_CS14	DET_OFF_CS13	DET_OFF_CS12	DET_OFF_CS11	DET_OFF_CS10	DET_OFF_CS9	DET_OFF_CS8
0x48	R	0x00	-	-	-	-	DET_OFF_CS19	DET_OFF_CS18	DET_OFF_CS17	DET_OFF_CS16

0x49-0x4B: Switch Long Press Detection

Name: DET_HLD
Address: 0x49-0x4B
Description: These registers show that long press was detected. The bit "INT_HLD" in the register "Interrupt Factor" shows the OR of these registers. These are cleared by setting 0 to the register "Clear Switch Long Press Detection". The long press detect duration is able to be set up to 7 types from A to G. The durations are set by the register "Long Press Detection Time / Repeated Long Press Detection Time". And the duration types are assigned to each sensor by the register "Long Press Detection Assignment / Unexpected Long Press Detection Assignment".

0: Long Press - undetected 1: Long Press - detected

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x49	R	0x00	DET_HLD_CS7	DET_HLD_CS6	DET_HLD_CS5	DET_HLD_CS4	DET_HLD_CS3	DET_HLD_CS2	DET_HLD_CS1	DET_HLD_CS0
0x4A	R	0x00	DET_HLD_CS15	DET_HLD_CS14	DET_HLD_CS13	DET_HLD_CS12	DET_HLD_CS11	DET_HLD_CS10	DET_HLD_CS9	DET_HLD_CS8
0x4B	R	0x00	-	-	-	-	DET_HLD_CS19	DET_HLD_CS18	DET_HLD_CS17	DET_HLD_CS16

0x4C-0x4E: Switch Repeated Long Press Detection

Name: DET_HLDRPT
Address: 0x4C-0x4E
Description: These registers show that repeated long press was detected. The bit "INT_HLD_RPT" in the register "Interrupt Factor" shows the OR of these registers. These are cleared by setting 0 to the register "Clear Switch Repeated Long Press Detection". The repeated long press detect duration is able to be set up to 7 types from A to G. The durations are set by the register "Long Press Detection Time / Repeated Long Press Detection Time". And the duration types are assigned to each sensor by the register "Long Press Detection Assignment / Unexpected Long Press Detection Assignment".

0: Repeated Long Press - undetected 1: Repeated Long Press - detected

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4C	R	0x00	DET_HLD RPT_CS7	DET_HLD RPT_CS6	DET_HLD RPT_CS5	DET_HLD RPT_CS4	DET_HLD RPT_CS3	DET_HLD RPT_CS2	DET_HLD RPT_CS1	DET_HLD RPT_CS0
0x4D	R	0x00	DET_HLD RPT_CS15	DET_HLD RPT_CS14	DET_HLD RPT_CS13	DET_HLD RPT_CS12	DET_HLD RPT_CS11	DET_HLD RPT_CS10	DET_HLD RPT_CS9	DET_HLD RPT_CS8
0x4E	R	0x00	-	-	-	-	DET_HLD RPT_CS19	DET_HLD RPT_CS18	DET_HLD RPT_CS17	DET_HLD RPT_CS16

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0x4F: Multiple Pattern Switches ON Detection

Name: DET_MULT_ON
Address: 0x4F
Description: This register shows that the state of multiple pattern switches changed from OFF to ON simultaneously within the fixed time. The bit "INT_MULT_ON" in the register "Interrupt Factor" shows the OR of this register. This is cleared by setting 0 to the register "Clear Multiple Pattern Switches ON Detection". The fixed time is set by the register "Switch Detection Time". The multiple pattern switch combinations are set by the register "Multiple Pattern Switches Assignment".

0: Multiple Pattern Switches ON - undetected 1: Multiple Pattern Switches ON - detected

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4F	R	0x00	DET_MULT_ON_H	DET_MULT_ON_G	DET_MULT_ON_F	DET_MULT_ON_E	DET_MULT_ON_D	DET_MULT_ON_C	DET_MULT_ON_B	DET_MULT_ON_A

0x50: Multiple Pattern Switches OFF Detection

Name: DET_MULT_OFF
Address: 0x50
Description: This register shows that that the state of multiple pattern switches changed from ON to OFF simultaneously. The bit "INT_MULT_OFF" in the register "Interrupt Factor" shows the OR of this register. This is cleared by setting 0 to the register "Clear Multiple Pattern Switches OFF Detection".

0: Multiple Pattern Switches OFF - undetected 1: Multiple Pattern Switches OFF - detected

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x50	R	0x00	DET_MULT_OFF_H	DET_MULT_OFF_G	DET_MULT_OFF_F	DET_MULT_OFF_E	DET_MULT_OFF_D	DET_MULT_OFF_C	DET_MULT_OFF_B	DET_MULT_OFF_A

0x51-0x53: Unexpected Long Press Detection

Name: DET_UNKNOWN
Address: 0x51-0x53
Description: These registers show that unexpected long press was detected. The bit "INT_UNK" in the register "Interrupt Factor" shows the OR of these registers. These are cleared by setting 0 to the register "Clear Unexpected Long Press Detection". The unexpected long press duration is set by the register "Unexpected Long Press Detection Time".

0: Unexpected Long Press - undetected 1: Unexpected Long Press - detected

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x51	R	0x00	DET_UNK_CS7	DET_UNK_CS6	DET_UNK_CS5	DET_UNK_CS4	DET_UNK_CS3	DET_UNK_CS2	DET_UNK_CS1	DET_UNK_CS0
0x52	R	0x00	DET_UNK_CS15	DET_UNK_CS14	DET_UNK_CS13	DET_UNK_CS12	DET_UNK_CS11	DET_UNK_CS10	DET_UNK_CS9	DET_UNK_CS8
0x53	R	0x00	-	-	-	-	DET_UNK_CS19	DET_UNK_CS18	DET_UNK_CS17	DET_UNK_CS16

0x54-0x56: Switch ON / OFF State

Name: SW_STATE
Address: 0x54-0x56
Description: These registers show ON / OFF state of switch. These states are the result filtered by the register "Oversampling".

0: OFF state 1: ON state

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x54	R	0x00	SW_STAT_CS7	SW_STAT_CS6	SW_STAT_CS5	SW_STAT_CS4	SW_STAT_CS3	SW_STAT_CS2	SW_STAT_CS1	SW_STAT_CS0
0x55	R	0x00	SW_STAT_CS15	SW_STAT_CS14	SW_STAT_CS13	SW_STAT_CS12	SW_STAT_CS11	SW_STAT_CS10	SW_STAT_CS9	SW_STAT_CS8
0x56	R	0x00	-	-	-	-	SW_STAT_CS19	SW_STAT_CS18	SW_STAT_CS17	SW_STAT_CS16

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0x57: State of IC

Name: RUN_STATE
Address: 0x57
Description: This register shows the state of IC.

RUN_AFE: This bit shows the state of sensor.

0: Under suspension 1: Under detection

RUN_CAL: This bit shows the state of calibration.

0: Under no-calibration 1: Under calibration

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x57	R	0x00	-	-	-	-	-	RUN_CAL	RUN_AFE	-

0x58: Calibration Failure Number of Times

Name: NUM_FALCAL
Address: 0x58
Description: This register shows the number of times of calibration failure. It is incremented every time calibration fails. When it reaches 255, the next will be 0.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x58	R	0x00	NUM_FALCAL[7:0]							

0x5F: Firmware Version

Name: FW_VER
Address: 0x5F
Description: This register shows the firmware version.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5F	R	0x0D	FW_VER[7:0]							

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Configuration Register Description

0x60-0x64: Sensor Function

Name: SW_EN_CFG
Address: 0x60-0x64
Description: These registers configure the function of CS pins.

CS*_SCAN_SEL[1:0] = 0x0: The CS pin becomes a capacitive sensor pin.
CS*_SCAN_SEL[1:0] = 0x1: The CS pin outputs low level.
CS*_SCAN_SEL[1:0] = 0x2: The CS pin outputs high level.
CS*_SCAN_SEL[1:0] = 0x3: The CS pin becomes the high impedance.

* represent the sensor number from 0 to 19.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x60	R/W	0x00	CS3_SCAN_SEL[1:0]		CS2_SCAN_SEL[1:0]		CS1_SCAN_SEL[1:0]		CS0_SCAN_SEL[1:0]	
0x61	R/W	0x00	CS7_SCAN_SEL[1:0]		CS6_SCAN_SEL[1:0]		CS5_SCAN_SEL[1:0]		CS4_SCAN_SEL[1:0]	
0x62	R/W	0x50	CS11_SCAN_SEL[1:0]		CS10_SCAN_SEL[1:0]		CS9_SCAN_SEL[1:0]		CS8_SCAN_SEL[1:0]	
0x63	R/W	0x55	CS15_SCAN_SEL[1:0]		CS14_SCAN_SEL[1:0]		CS13_SCAN_SEL[1:0]		CS12_SCAN_SEL[1:0]	
0x64	R/W	0x55	CS19_SCAN_SEL[1:0]		CS18_SCAN_SEL[1:0]		CS17_SCAN_SEL[1:0]		CS16_SCAN_SEL[1:0]	

0x66-0x6F: Sensitivity

Name: VAL_GA_CFG
Address: 0x66-0x6F
Description: These registers configure the sensor sensitivity. The sensitivity adjustment is 15 steps. The smaller the setting value is, the higher the sensor sensitivity is. The sensor which has the unallowable setting value is disabled.

Allowable setting range: 0x1 (high sensitivity) ≤ VAL_GA_CS* ≤ 0xF (low sensitivity)
Recommended setting range: 0x3 (high sensitivity) ≤ VAL_GA_CS* ≤ 0xF (low sensitivity)

* represent the sensor number from 0 to 19.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x66	R/W	0x7F	VAL_GA_CS1[3:0]				VAL_GA_CS0[3:0]			
0x67	R/W	0x77	VAL_GA_CS3[3:0]				VAL_GA_CS2[3:0]			
0x68	R/W	0x77	VAL_GA_CS5[3:0]				VAL_GA_CS4[3:0]			
0x69	R/W	0x77	VAL_GA_CS7[3:0]				VAL_GA_CS6[3:0]			
0x6A	R/W	0x77	VAL_GA_CS9[3:0]				VAL_GA_CS8[3:0]			
0x6B	R/W	0xFF	VAL_GA_CS11[3:0]				VAL_GA_CS10[3:0]			
0x6C	R/W	0xFF	VAL_GA_CS13[3:0]				VAL_GA_CS12[3:0]			
0x6D	R/W	0xFF	VAL_GA_CS15[3:0]				VAL_GA_CS14[3:0]			
0x6E	R/W	0xFF	VAL_GA_CS17[3:0]				VAL_GA_CS16[3:0]			
0x6F	R/W	0xFF	VAL_GA_CS19[3:0]				VAL_GA_CS18[3:0]			

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0x70-0x97: Switch ON Threshold / Switch OFF Threshold

Name: VAL_TH_ON_CFG / VAL_TH_OFF_CFG
Address: 0x70-0x97
Description: These registers configure the threshold to judge the state of switch. The register "Sensor Data" is compared with these registers. The state of switch is ON when the register "Sensor Data" is larger than VAL_TH_ON_CS*. And the state of switch is OFF when the register "Sensor Data" is smaller than VAL_TH_OFF_CS*. The sensor which has the unallowable setting value is disabled.

Allowable setting value range: 0x03 < VAL_TH_OFF_CS* < VAL_TH_ON_CS* < 0xFF
Recommended setting value range: 0x40 ≤ VAL_TH_ON_CS* ≤ 0xE0
0x20 ≤ VAL_TH_OFF_CS*

* represent the sensor number from 0 to 19.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x70	R/W	0xC8	VAL_TH_ON_CS0[7:0]							
0x71	R/W	0x64	VAL_TH_OFF_CS0[7:0]							
0x72	R/W	0xC8	VAL_TH_ON_CS1[7:0]							
0x73	R/W	0x64	VAL_TH_OFF_CS1[7:0]							
0x74	R/W	0xC8	VAL_TH_ON_CS2[7:0]							
0x75	R/W	0x64	VAL_TH_OFF_CS2[7:0]							
0x76	R/W	0xC8	VAL_TH_ON_CS3[7:0]							
0x77	R/W	0x64	VAL_TH_OFF_CS3[7:0]							
0x78	R/W	0xC8	VAL_TH_ON_CS4[7:0]							
0x79	R/W	0x64	VAL_TH_OFF_CS4[7:0]							
0x7A	R/W	0xC8	VAL_TH_ON_CS5[7:0]							
0x7B	R/W	0x64	VAL_TH_OFF_CS5[7:0]							
0x7C	R/W	0xC8	VAL_TH_ON_CS6[7:0]							
0x7D	R/W	0x64	VAL_TH_OFF_CS6[7:0]							
0x7E	R/W	0xC8	VAL_TH_ON_CS7[7:0]							
0x7F	R/W	0x64	VAL_TH_OFF_CS7[7:0]							
0x80	R/W	0xC8	VAL_TH_ON_CS8[7:0]							
0x81	R/W	0x64	VAL_TH_OFF_CS8[7:0]							
0x82	R/W	0xC8	VAL_TH_ON_CS9[7:0]							
0x83	R/W	0x64	VAL_TH_OFF_CS9[7:0]							
0x84	R/W	0xC8	VAL_TH_ON_CS10[7:0]							
0x85	R/W	0x64	VAL_TH_OFF_CS10[7:0]							
0x86	R/W	0xC8	VAL_TH_ON_CS11[7:0]							
0x87	R/W	0x64	VAL_TH_OFF_CS11[7:0]							
0x88	R/W	0xC8	VAL_TH_ON_CS12[7:0]							
0x89	R/W	0x64	VAL_TH_OFF_CS12[7:0]							
0x8A	R/W	0xC8	VAL_TH_ON_CS13[7:0]							
0x8B	R/W	0x64	VAL_TH_OFF_CS13[7:0]							
0x8C	R/W	0xC8	VAL_TH_ON_CS14[7:0]							
0x8D	R/W	0x64	VAL_TH_OFF_CS14[7:0]							
0x8E	R/W	0xC8	VAL_TH_ON_CS15[7:0]							
0x8F	R/W	0x64	VAL_TH_OFF_CS15[7:0]							
0x90	R/W	0xC8	VAL_TH_ON_CS16[7:0]							
0x91	R/W	0x64	VAL_TH_OFF_CS16[7:0]							
0x92	R/W	0xC8	VAL_TH_ON_CS17[7:0]							
0x93	R/W	0x64	VAL_TH_OFF_CS17[7:0]							
0x94	R/W	0xC8	VAL_TH_ON_CS18[7:0]							
0x95	R/W	0x64	VAL_TH_OFF_CS18[7:0]							
0x96	R/W	0xC8	VAL_TH_ON_CS19[7:0]							
0x97	R/W	0x64	VAL_TH_OFF_CS19[7:0]							

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0x98: Digital Gain

Name: GA_DIGI_CFG
Address: 0x98
Description: This register configures low sensitivity. This is used to set lower sensitivity than the setting value of the register "Sensitivity".

The register "Sensor Data" =
[(The register "Filter Sensor Data" - 2500) - (315 ÷ The register "Sensitivity")] ÷ (The register "Digital Gain" + 1)

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x98	R/W	0x30	VAL_ADJ_DAT[3:0]				-	-	-	-

0x99: Sampling Frequency

Name: SENS_CFG
Address: 0x99
Description: This register configures the sampling frequency.

TIM_AFE[2:0]: The Setting of Sampling Frequency

The detect duration per one sensor is like below.

TIM_AFE[2:0]=0x0 : Sampling frequency=1563kHz Detection duration per one sensor=0.2054ms
TIM_AFE[2:0]=0x1 : Sampling frequency=1024kHz Detection duration per one sensor=0.3082ms
TIM_AFE[2:0]=0x2 : Sampling frequency=781kHz Detection duration per one sensor=0.4109ms
TIM_AFE[2:0]=0x3 : Sampling frequency=391kHz Detection duration per one sensor=0.8218ms
TIM_AFE[2:0]=0x4 : Sampling frequency=298kHz Detection duration per one sensor=1.0786ms
TIM_AFE[2:0]=0x5 : Sampling frequency=195kHz Detection duration per one sensor=1.6435ms
TIM_AFE[2:0]=0x6 : Sampling frequency=156kHz Detection duration per one sensor=2.0544ms
TIM_AFE[2:0]=0x7 : Sampling frequency=130kHz Detection duration per one sensor=2.4653ms

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x99	R/W	0x50	-	TIM_AFE[2:0]			-	-	-	-

0x9A: Filter Tap

Name: FIL_CFG
Address: 0x9A
Description: This register configures the filter for the register "Sensor Data". This configures the median filter tap and the kinds of sampling frequency. The sampling frequencies are modulated from the base frequency set by the register "Sampling Frequency".

FIL_CFG[2:0]=0x0 : 1 kind (base frequency) of sampling frequency is used.
Median filter tap length=1
FIL_CFG[2:0]=0x1 : 3 kinds(+6%, ±0%, -6%) of sampling frequency is used.
Median filter tap length=3
FIL_CFG[2:0]=0x2 : 5 kinds(+6%, +3%, ±0%, -3%, -6%) of sampling frequency is used.
Median filter tap length=5
FIL_CFG[2:0]=0x3 : 7 kinds(+6%, +4%, +2%, ±0%, -2%, -4%, -6%) of sampling frequency is used.
Median filter tap length=7
FIL_CFG[2:0]=0x4 : 7 kinds(+6%, +4%, +2%, ±0%, -2%, -4%, -6%) of sampling frequency is used.
Median filter tap length=9
FIL_CFG[2:0]=0x5 : 7 kinds(+6%, +4%, +2%, ±0%, -2%, -4%, -6%) of sampling frequency is used.
Median filter tap length=11
FIL_CFG[2:0]=0x6 : 7 kinds(+6%, +4%, +2%, ±0%, -2%, -4%, -6%) of sampling frequency is used.
Median filter tap length=13
FIL_CFG[2:0]=0x7 : 7 kinds(+6%, +4%, +2%, ±0%, -2%, -4%, -6%) of sampling frequency is used.
Median filter tap length=15

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x9A	R/W	0x03	-	-	-	-	-	FIL_CFG[2:0]		

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0x9B: Control Mode

Name: MODE_CFG
Address: 0x9B
Description: This register configures the functions for calibration and sensor.

SCAN_SEL: Sensor High Impedance

This bit configures the states of enabled sensors during the other sensor is sensing.

0: Sensor outputs low. 1: Sensor becomes high impedance.

ADJ_OFS_ENB: Offset Calibration

This bit configures whether the offset calibration to the register "Filter Sensor Data" is performed or not.

0: Offset calibration is enabled. 1: Offset calibration is disabled.

UNK_CAL_EN: Unexpected Long Press Calibration

This bit configures whether automatic calibration is performed when unexpected long press is detected. This calibration is effective only to the unexpected long press switches.

0: Unexpected Long Press Calibration is disabled. 1: Unexpected Long Press Calibration is enabled.

LOWER_CAL_EN: Lower Calibration

This bit configures whether automatic calibration is performed when the data of the register "Filter Sensor Data" is smaller than the reference value. When the offset calibration is enabled, this calibration is disabled.

0: Lower Calibration is disabled. 1: Lower Calibration is enabled.

CAL_SFT_EN: Sampling Frequency Modulation

This bit configures whether frequency modulation is performed when calibration fails.

0: Frequency modulation is disabled. 1: Frequency modulation is enabled.

MLT_SW_EN: Multiple Switches Control

This bit configures whether multiple switches are usable at the same time. In the case multiple switches are usable, the register "Switch Detection Time" and "Multiple Pattern Switches Assignment" are disabled.

0: Multiple switches are unusable. 1: Multiple switches are usable.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x9B	R/W	0x80	MLT_SW_EN	-	-	CAL_SFT_EN	LOWER_CAL_EN	UNK_CAL_EN	ADJ_OFS_ENB	SCAN_SEL

0x9C: Oversampling

Name: OST_CFG
Address: 0x9C
Description: This register configures the number of oversampling to reject chattering. The result is reflected to the register "Switch ON Detection" and "Switch OFF Detection" when ON / OFF judgment is same as "OST[3:0]+1" times.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x9C	R/W	0x03	-	-	-	-	OST[3:0]			

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0x9D: Drift Calibration

Name: DRIFT_CAL_CFG
Address: 0x9D
Description: This register configures the calibration to be performed at detecting the drift state.

ADJ_DET_NUM[4:0]: Drift Calibration Condition

When the register "Sensor Data" is larger than a quarter value of the register "Switch ON Threshold" or a value of the register "Switch OFF Threshold", the sensor is recognized as the drift state sensor. When the number of the drift state sensors is larger than ADJ_DET_NUM[4:0], drift state is detected and calibration is performed.

ADJ_ALL_EN: Drift Calibration Selection

In the case this bit is set to 0, the drift calibration is performed except the sensor with switch ON state. In the case this bit is set to 1, the drift calibration is performed for all sensors regardless of switch ON / OFF state.

0: The drift calibration is performed except the sensors with switch ON state.
1: The drift calibration is performed for all sensors regardless of switch ON / OFF state.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x9D	R/W	0x09	ADJ_ALL_EN	-	-	ADJ_DET_NUM[4:0]				

0x9E: Noise Calibration

Name: NOISE_CAL_CFG
Address: 0x9E
Description: This register configures the calibration to be performed at detecting the noise state.

NOISE_DET_NUM[4:0]: Noise Calibration Condition

When the plural sensors are simultaneously the switch ON state, the sensors are recognized as the noise state sensor. When the number of the noise state sensors is larger than ADJ_DET_NUM[4:0], noise state is detected and calibration is performed.

NOISE_SFT_EN: Noise Shift Configuration

The noise calibration is performed without the shift of sampling frequency in the case this bit is set to 0. The calibration is performed after shifting sampling frequency in the case this bit is set to 1.

0: Only noise calibration is performed.
1: The noise calibration is performed after shifting sampling frequency.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x9E	R/W	0x89	NOISE_SFT_EN	-	-	NOISE_DET_NUM[4:0]				

0x9F: Periodical Calibration

Name: TIME_PERCAL_CFG
Address: 0x9F
Description: This register configures the interval time of the periodical calibration. In the case this register is set to 0, the periodical calibration is not performed. The periodical calibration is performed for the sensors whose the register "Sensor Data" is not larger than the register "Switch ON Threshold".

Interval time of the periodical calibration = TIME_PERCAL[7:0] x Approximately 5s

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x9F	R/W	0x3C	TIME_PERCAL[7:0]							

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0xA2-0xA3: Unexpected Long Press Detection Time

Name: TIME_UNKNOWN_CFG
Address: 0xA2-0xA3
Description: These registers configure the time until detecting unexpected long press. The data 1 is set to the register "Unexpected Long Press Detection" when unexpected long press is detected. Until unexpected long press is avoided, the unexpected long press is repeatedly detected each configured time.

The time until detecting unexpected long press = TIME_UNKNOWN_*[7:0] x Approximately 1s
In the case TIME_ UNKNOWN_*[7:0] is set to 0, unexpected long press is not detected.

* represent the setting number A and B.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xA2	R/W	0x00	TIME_UNKNOWN_A[7:0]							
0xA3	R/W	0x00	TIME_UNKNOWN_B[7:0]							

0xA4-0xB1: Long Press Detection Time / Repeated Long Press Detection Time

Name: TIME_HLD_CFG
Address: 0xA4-0xB1
Description: Pressing the switch for a fixed time is referred to as "long press". After first long press is detected, subsequent long pressing is referred to as "repeated long press". These registers configure the time until detecting long press and repeated long press. The data 1 is set to the register "Switch Long Press Detection" when long press is detected. And the data 1 is set to the register "Switch Repeated Long Press Detection" when repeated long press is detected.

The time until detecting long press = TIME_HLD_*[7:0] x Approximately 0.1s
In the case TIME_HLD_*[7:0] is set to 0, long press is not detected.

The time until detecting repeated long press = TIME_HLD_RPT_*[7:0] x Approximately 0.1s
In the case TIME_HLD_RPT_*[7:0] is set to 0, repeated long press is not detected.

* represent the setting number from A to G.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xA4	R/W	0x00	TIME_HLD_A[7:0]							
0xA5	R/W	0x00	TIME_HLD_RPT_A[7:0]							
0xA6	R/W	0x00	TIME_HLD_B[7:0]							
0xA7	R/W	0x00	TIME_HLD_RPT_B[7:0]							
0xA8	R/W	0x00	TIME_HLD_C[7:0]							
0xA9	R/W	0x00	TIME_HLD_RPT_C[7:0]							
0xAA	R/W	0x00	TIME_HLD_D[7:0]							
0xAB	R/W	0x00	TIME_HLD_RPT_D[7:0]							
0xAC	R/W	0x00	TIME_HLD_E[7:0]							
0xAD	R/W	0x00	TIME_HLD_RPT_E[7:0]							
0xAE	R/W	0x00	TIME_HLD_F[7:0]							
0xAF	R/W	0x00	TIME_HLD_RPT_F[7:0]							
0xB0	R/W	0x00	TIME_HLD_G[7:0]							
0xB1	R/W	0x00	TIME_HLD_RPT_G[7:0]							

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0xB2-0xBB: Long Press Detection Assignment / Unexpected Long Press Detection Assignment

Name: SENS_HLD_CFG
Address: 0xB2-0xBB
Description: These registers assign the settings of the register "Long Press Detection Time / Repeated Long Press Detection Time" and "Unexpected Long Press Detection Time" to each sensor.

HLD_CS*[2:0] = 0x0: Long press and repeated long press are not detected to CS*.
= 0x1: Long press A and repeated long press A are assigned to CS*.
= 0x2: Long press B and repeated long press B are assigned to CS*.
= 0x3: Long press C and repeated long press C are assigned to CS*.
= 0x4: Long press D and repeated long press D are assigned to CS*.
= 0x5: Long press E and repeated long press E are assigned to CS*.
= 0x6: Long press F and repeated long press F are assigned to CS*.
= 0x7: Long press G and repeated long press G are assigned to CS*.

UNK_CS* = 0x0: Unexpected long press A is assigned to CS*.
= 0x1: Unexpected long press B is assigned to CS*.

* represent the sensor number from 0 to 19.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xB2	R/W	0x00	UNK_CS1	HLD_CS1[2:0]			UNK_CS0	HLD_CS0[2:0]		
0xB3	R/W	0x00	UNK_CS3	HLD_CS3[2:0]			UNK_CS2	HLD_CS2[2:0]		
0xB4	R/W	0x00	UNK_CS5	HLD_CS5[2:0]			UNK_CS4	HLD_CS4[2:0]		
0xB5	R/W	0x00	UNK_CS7	HLD_CS7[2:0]			UNK_CS6	HLD_CS6[2:0]		
0xB6	R/W	0x00	UNK_CS9	HLD_CS9[2:0]			UNK_CS8	HLD_CS8[2:0]		
0xB7	R/W	0x00	UNK_CS11	HLD_CS11[2:0]			UNK_CS10	HLD_CS10[2:0]		
0xB8	R/W	0x00	UNK_CS13	HLD_CS12[2:0]			UNK_CS12	HLD_CS12[2:0]		
0xB9	R/W	0x00	UNK_CS15	HLD_CS15[2:0]			UNK_CS14	HLD_CS14[2:0]		
0xBA	R/W	0x00	UNK_CS17	HLD_CS17[2:0]			UNK_CS16	HLD_CS16[2:0]		
0xBB	R/W	0x00	UNK_CS19	HLD_CS19[2:0]			UNK_CS18	HLD_CS18[2:0]		

0xBC: Switch Detection Time

Name: TIME_DET_CFG
Address: 0xBC
Description: This register configures the time until detecting ON state. IC recognizes the ON state after the delay time by median filter and this function. Second touch is not detected until clearing the interrupt of first touch. Pressing simultaneously within the time is detected as a multiple pattern switch.

The time until detecting the ON state of switch = TIME_DET[7:0] x Approximately 10ms

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xBC	R/W	0x00	TIME_DET[7:0]							

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0xBD-0xD4: Multiple Pattern Switches Assignment

Name: SENS_MULT_CFG
Address: 0xBD-0xD4
Description: These registers configure the combinations of multiple pattern switches detection. The multiple pattern switch combinations are able to be set up to 8 types from A to H. In the case the same combinations are set in 8 types, the combination settings are invalid.

MULT_A_CS*=0: CS* is not assigned to multiple pattern switches A.
MULT_A_CS*=1: CS* is assigned to multiple pattern switches A.

MULT_B_CS*=0: CS* is not assigned to multiple pattern switches B.
MULT_B_CS*=1: CS* is assigned to multiple pattern switches B.

MULT_C_CS*=0: CS* is not assigned to multiple pattern switches C.
MULT_C_CS*=1: CS* is assigned to multiple pattern switches C.

MULT_D_CS*=0: CS* is not assigned to multiple pattern switches D.
MULT_D_CS*=1: CS* is assigned to multiple pattern switches D.

MULT_E_CS*=0: CS* is not assigned to multiple pattern switches E.
MULT_E_CS*=1: CS* is assigned to multiple pattern switches E.

MULT_F_CS*=0: CS* is not assigned to multiple pattern switches F.
MULT_F_CS*=1: CS* is assigned to multiple pattern switches F.

MULT_G_CS*=0: CS* is not assigned to multiple pattern switches G.
MULT_G_CS*=1: CS* is assigned to multiple pattern switches G.

MULT_H_CS*=0: CS* is not assigned to multiple pattern switches H.
MULT_H_CS*=1: CS* is assigned to multiple pattern switches H.

* represent the sensor number from 0 to 19.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xBD	R/W	0x00	MULT_A_CS7	MULT_A_CS6	MULT_A_CS5	MULT_A_CS4	MULT_A_CS3	MULT_A_CS2	MULT_A_CS1	MULT_A_CS0
0xBE	R/W	0x00	MULT_A_CS15	MULT_A_CS14	MULT_A_CS13	MULT_A_CS12	MULT_A_CS11	MULT_A_CS10	MULT_A_CS9	MULT_A_CS8
0xBF	R/W	0x00	-	-	-	-	MULT_A_CS19	MULT_A_CS18	MULT_A_CS17	MULT_A_CS16
0xC0	R/W	0x00	MULT_B_CS7	MULT_B_CS6	MULT_B_CS5	MULT_B_CS4	MULT_B_CS3	MULT_B_CS2	MULT_B_CS1	MULT_B_CS0
0xC1	R/W	0x00	MULT_B_CS15	MULT_B_CS14	MULT_B_CS13	MULT_B_CS12	MULT_B_CS11	MULT_B_CS10	MULT_B_CS9	MULT_B_CS8
0xC2	R/W	0x00	-	-	-	-	MULT_B_CS19	MULT_B_CS18	MULT_B_CS17	MULT_B_CS16
0xC3	R/W	0x00	MULT_C_CS7	MULT_C_CS6	MULT_C_CS5	MULT_C_CS4	MULT_C_CS3	MULT_C_CS2	MULT_C_CS1	MULT_C_CS0
0xC4	R/W	0x00	MULT_C_CS15	MULT_C_CS14	MULT_C_CS13	MULT_C_CS12	MULT_C_CS11	MULT_C_CS10	MULT_C_CS9	MULT_C_CS8
0xC5	R/W	0x00	-	-	-	-	MULT_C_CS19	MULT_C_CS18	MULT_C_CS17	MULT_C_CS16
0xC6	R/W	0x00	MULT_D_CS7	MULT_D_CS6	MULT_D_CS5	MULT_D_CS4	MULT_D_CS3	MULT_D_CS2	MULT_D_CS1	MULT_D_CS0
0xC7	R/W	0x00	MULT_D_CS15	MULT_D_CS14	MULT_D_CS13	MULT_D_CS12	MULT_D_CS11	MULT_D_CS10	MULT_D_CS9	MULT_D_CS8
0xC8	R/W	0x00	-	-	-	-	MULT_D_CS19	MULT_D_CS18	MULT_D_CS17	MULT_D_CS16
0xC9	R/W	0x00	MULT_E_CS7	MULT_E_CS6	MULT_E_CS5	MULT_E_CS4	MULT_E_CS3	MULT_E_CS2	MULT_E_CS1	MULT_E_CS0
0xCA	R/W	0x00	MULT_E_CS15	MULT_E_CS14	MULT_E_CS13	MULT_E_CS12	MULT_E_CS11	MULT_E_CS10	MULT_E_CS9	MULT_E_CS8
0xCB	R/W	0x00	-	-	-	-	MULT_E_CS19	MULT_E_CS18	MULT_E_CS17	MULT_E_CS16
0xCC	R/W	0x00	MULT_F_CS7	MULT_F_CS6	MULT_F_CS5	MULT_F_CS4	MULT_F_CS3	MULT_F_CS2	MULT_F_CS1	MULT_F_CS0
0xCD	R/W	0x00	MULT_F_CS15	MULT_F_CS14	MULT_F_CS13	MULT_F_CS12	MULT_F_CS11	MULT_F_CS10	MULT_F_CS9	MULT_F_CS8
0xCE	R/W	0x00	-	-	-	-	MULT_F_CS19	MULT_F_CS18	MULT_F_CS17	MULT_F_CS16
0xCF	R/W	0x00	MULT_G_CS7	MULT_G_CS6	MULT_G_CS5	MULT_G_CS4	MULT_G_CS3	MULT_G_CS2	MULT_G_CS1	MULT_G_CS0
0xD0	R/W	0x00	MULT_G_CS15	MULT_G_CS14	MULT_G_CS13	MULT_G_CS12	MULT_G_CS11	MULT_G_CS10	MULT_G_CS9	MULT_G_CS8
0xD1	R/W	0x00	-	-	-	-	MULT_G_CS19	MULT_G_CS18	MULT_G_CS17	MULT_G_CS16
0xD2	R/W	0x00	MULT_H_CS7	MULT_H_CS6	MULT_H_CS5	MULT_H_CS4	MULT_H_CS3	MULT_H_CS2	MULT_H_CS1	MULT_H_CS0
0xD3	R/W	0x00	MULT_H_CS15	MULT_H_CS14	MULT_H_CS13	MULT_H_CS12	MULT_H_CS11	MULT_H_CS10	MULT_H_CS9	MULT_H_CS8
0xD4	R/W	0x00	-	-	-	-	MULT_H_CS19	MULT_H_CS18	MULT_H_CS17	MULT_H_CS16

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0xD5-0xD6: Mask Interrupt Factor

Name: MSK_INTERRUPT_CFG
Address: 0xD5-0xD6
Description: These registers are for masking the interrupt of the register "Interrupt Factor". In the case mask is set to 1, Interrupt is not reflected to the register "Interrupt Factor".

0: Interrupt is not masked 1: Interrupt is masked

MSK_INT_FINCAL : Mask Software Calibration Completion Interrupt
In the case this bit is set to 1, interrupt is not reflected to the bit "INT_FINCAL" in the register "Interrupt Factor".

MSK_INT_FALCAL : Mask Software Calibration Failure Interrupt
In the case this bit is set to 1, interrupt is not reflected to the bit "INT_FALCAL" in the register "Interrupt Factor".

MSK_INT_NOISE : Mask Noise Detection Interrupt
In the case this bit is set to 1, interrupt is not reflected to the bit "INT_NOISE" in the register "Interrupt Factor".

MSK_INT_AVDDON : Mask AVDD ON Detection Interrupt
In the case this bit is set to 1, interrupt is not reflected to the bit "INT_AVDDON" in the register "Interrupt Factor".

MSK_INT_AVDDOFF : Mask AVDD OFF Detection Interrupt
In the case this bit is set to 1 interrupt is not reflected to the bit "INT_AVDDOFF" in the register "Interrupt Factor".

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xD5	R/W	0x00	MSK_INT_NOISE	-	-	-	MSK_INT FALCAL	MSK_INT FINCAL	-	-
0xD6	R/W	0x00	-	-	-	-	-	-	MSK_INT AVDDOFF	MSK_INT AVDDON

0xD7-0xD9: Mask Switch ON Detection

Name: MSK_DET_ON_CFG
Address: 0xD7-0xD9
Description: These register are for masking the interrupt of the register "Switch ON Detection". If these bits are set to 1, interrupt is not reflected to the register "Switch ON Detection".

0: Interrupt is not masked 1: Interrupt is masked

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xD7	R/W	0x00	MSK_DET_ON_CS7	MSK_DET_ON_CS6	MSK_DET_ON_CS5	MSK_DET_ON_CS4	MSK_DET_ON_CS3	MSK_DET_ON_CS2	MSK_DET_ON_CS1	MSK_DET_ON_CS0
0xD8	R/W	0x00	MSK_DET_ON_CS15	MSK_DET_ON_CS14	MSK_DET_ON_CS13	MSK_DET_ON_CS12	MSK_DET_ON_CS11	MSK_DET_ON_CS10	MSK_DET_ON_CS9	MSK_DET_ON_CS8
0xD9	R/W	0x00	-	-	-	-	MSK_DET_ON_CS19	MSK_DET_ON_CS18	MSK_DET_ON_CS17	MSK_DET_ON_CS16

0xDA-0xDC: Mask Switch OFF Detection

Name: MSK_DET_OFF_CFG
Address: 0xDA-0xDC
Description: These register are for masking the interrupt of the register "Switch OFF Detection". If these bits are set to 1, interrupt is not reflected to the register "Switch OFF Detection".

0: Interrupt is not masked 1: Interrupt is masked

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xDA	R/W	0x00	MSK_DET_OFF_CS7	MSK_DET_OFF_CS6	MSK_DET_OFF_CS5	MSK_DET_OFF_CS4	MSK_DET_OFF_CS3	MSK_DET_OFF_CS2	MSK_DET_OFF_CS1	MSK_DET_OFF_CS0
0xDB	R/W	0x00	MSK_DET_OFF_CS15	MSK_DET_OFF_CS14	MSK_DET_OFF_CS13	MSK_DET_OFF_CS12	MSK_DET_OFF_CS11	MSK_DET_OFF_CS10	MSK_DET_OFF_CS9	MSK_DET_OFF_CS8
0xDC	R/W	0x00	-	-	-	-	MSK_DET_OFF_CS19	MSK_DET_OFF_CS18	MSK_DET_OFF_CS17	MSK_DET_OFF_CS16

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0xDD-0xDF: Mask Unexpected Long Press Detection

Name: MSK_DET_UNKNOWN_CFG
Address: 0xDD-0xDF
Description: These registers are for masking the interrupt are the register "Unexpected Long Press Detection". If these bits are set to 1, interrupt is not reflected to the register "Unexpected Long Press Detection".

0: Interrupt is not masked 1: Interrupt is masked

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xDD	R/W	0x00	MSK_UNK_CS7	MSK_UNK_CS6	MSK_UNK_CS5	MSK_UNK_CS4	MSK_UNK_CS3	MSK_UNK_CS2	MSK_UNK_CS1	MSK_UNK_CS0
0xDE	R/W	0x00	MSK_UNK_CS15	MSK_UNK_CS14	MSK_UNK_CS13	MSK_UNK_CS12	MSK_UNK_CS11	MSK_UNK_CS10	MSK_UNK_CS9	MSK_UNK_CS8
0xDF	R/W	0x00	-	-	-	-	MSK_UNK_CS19	MSK_UNK_CS18	MSK_UNK_CS17	MSK_UNK_CS16

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Command Register Description

0xE0-0xE1: Clear Interrupt Factor

Name: CLR_INTERRUPT_CMD
Address: 0xE0-0xE1
Description: These are for clearing the interrupt of the register "Interrupt Factor".

0: Interrupt is cleared 1: Interrupt is not cleared

CLR_INT_FININI : Clear Initialization Completion Interrupt
This bit is for clearing the bit "INT_FININI" in the register "Interrupt Factor".

CLR_INT_FINCAL : Clear Software Calibration Completion Interrupt
This bit is for clearing the bit "INT_FINCAL" in the register "Interrupt Factor".

CLR_INT_FALCAL : Clear Software Calibration Failure Interrupt
This bit is for clearing the bit "INT_FALCAL" in the register "Interrupt Factor".

CLR_INT_NOISE : Clear Noise Detection Interrupt
This bit is for clearing the bit "INT_NOISE" in the register "Interrupt Factor".

CLR_INT_AVDDON : Clear AVDD ON Detection Interrupt
This bit is for clearing the bit "INT_AVDDON" in the register "Interrupt Factor".

CLR_INT_AVDDOFF : Clear AVDD OFF Detection Interrupt
This bit is for clearing the bit "INT_AVDDOFF" in the register "Interrupt Factor".

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE0	R/W	0x00	CLR_INT_NOISE	-	-	-	CLR_INT_FALCAL	CLR_INT_FINCAL	-	CLR_INT_FININI
0xE1	R/W	0x00	-	-	-	-	-	-	CLR_INT_AVDDOFF	CLR_INT_AVDDON

0xE2-0xE4: Clear Switch ON Detection

Name: CLR_DET_ON_CMD
Address: 0xE2-0xE4
Description: These registers are for clearing the interrupt of the register "Switch ON Detection".

0: Interrupt is cleared 1: Interrupt is not cleared

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE2	R/W	0x00	CLR_DET_ON_CS7	CLR_DET_ON_CS6	CLR_DET_ON_CS5	CLR_DET_ON_CS4	CLR_DET_ON_CS3	CLR_DET_ON_CS2	CLR_DET_ON_CS1	CLR_DET_ON_CS0
0xE3	R/W	0x00	CLR_DET_ON_CS15	CLR_DET_ON_CS14	CLR_DET_ON_CS13	CLR_DET_ON_CS12	CLR_DET_ON_CS11	CLR_DET_ON_CS10	CLR_DET_ON_CS9	CLR_DET_ON_CS8
0xE4	R/W	0x00	-	-	-	-	CLR_DET_ON_CS19	CLR_DET_ON_CS18	CLR_DET_ON_CS17	CLR_DET_ON_CS16

0xE5-0xE7: Clear Switch OFF Detection

Name: CLR_DET_OFF_CMD
Address: 0xE5-0xE7
Description: These registers are for clearing the interrupt of the register "Switch OFF Detection".

0: Interrupt is cleared 1: Interrupt is not cleared

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE5	R/W	0x00	CLR_DET_OFF_CS7	CLR_DET_OFF_CS6	CLR_DET_OFF_CS5	CLR_DET_OFF_CS4	CLR_DET_OFF_CS3	CLR_DET_OFF_CS2	CLR_DET_OFF_CS1	CLR_DET_OFF_CS0
0xE6	R/W	0x00	CLR_DET_OFF_CS15	CLR_DET_OFF_CS14	CLR_DET_OFF_CS13	CLR_DET_OFF_CS12	CLR_DET_OFF_CS11	CLR_DET_OFF_CS10	CLR_DET_OFF_CS9	CLR_DET_OFF_CS8
0xE7	R/W	0x00	-	-	-	-	CLR_DET_OFF_CS19	CLR_DET_OFF_CS18	CLR_DET_OFF_CS17	CLR_DET_OFF_CS16

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0xE8-0xEA: Clear Switch Long Press Detection

Name: CLR_DET_HLD_CMD
Address: 0xE8-0xEA
Description: These registers are for clearing the interrupt of the register "Switch Long Press Detection".

0: Interrupt is cleared 1: Interrupt is not cleared

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE8	R/W	0x00	CLR_HLD_CS7	CLR_HLD_CS6	CLR_HLD_CS5	CLR_HLD_CS4	CLR_HLD_CS3	CLR_HLD_CS2	CLR_HLD_CS1	CLR_HLD_CS0
0xE9	R/W	0x00	CLR_HLD_CS15	CLR_HLD_CS14	CLR_HLD_CS13	CLR_HLD_CS12	CLR_HLD_CS11	CLR_HLD_CS10	CLR_HLD_CS9	CLR_HLD_CS8
0xEA	R/W	0x00	-	-	-	-	CLR_HLD_CS19	CLR_HLD_CS18	CLR_HLD_CS17	CLR_HLD_CS16

0xEB-0xED: Clear Switch Repeated Long Press Detection

Name: CLR_DET_HLDRPT
Address: 0xEB-0xED
Description: These registers are for clearing the interrupt of the register "Switch Repeated Long Press Detection".

0: Interrupt is cleared 1: Interrupt is not cleared

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xEB	R/W	0x00	CLR_HLD RPT_CS7	CLR_HLD RPT_CS6	CLR_HLD RPT_CS5	CLR_HLD RPT_CS4	CLR_HLD RPT_CS3	CLR_HLD RPT_CS2	CLR_HLD RPT_CS1	CLR_HLD RPT_CS0
0xEC	R/W	0x00	CLR_HLD RPT_CS15	CLR_HLD RPT_CS14	CLR_HLD RPT_CS13	CLR_HLD RPT_CS12	CLR_HLD RPT_CS11	CLR_HLD RPT_CS10	CLR_HLD RPT_CS9	CLR_HLD RPT_CS8
0xED	R/W	0x00	-	-	-	-	CLR_HLD RPT_CS19	CLR_HLD RPT_CS18	CLR_HLD RPT_CS17	CLR_HLD RPT_CS16

0xEE: Clear Multiple Pattern Switches ON Detection

Name: CLR_DET_MULT_ON
Address: 0xEE
Description: This register is for clearing the interrupt of the register "Multiple Pattern Switches ON Detection".

0: Interrupt is cleared 1: Interrupt is not cleared

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xEE	R/W	0x00	CLR_MULT_ON_H	CLR_MULT_ON_G	CLR_MULT_ON_F	CLR_MULT_ON_E	CLR_MULT_ON_D	CLR_MULT_ON_C	CLR_MULT_ON_B	CLR_MULT_ON_A

0xEF: Clear Multiple Pattern Switches OFF Detection

Name: CLR_ DET_MULT_OFF
Address: 0xEF
Description: This register is for clearing clear the interrupt of the register "Multiple Pattern Switches OFF Detection".

0: Interrupt is cleared 1: Interrupt is not cleared

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xEE	R/W	0x00	CLR_MULT_OFF_H	CLR_MULT_OFF_G	CLR_MULT_OFF_F	CLR_MULT_OFF_E	CLR_MULT_OFF_D	CLR_MULT_OFF_C	CLR_MULT_OFF_B	CLR_MULT_OFF_A

0xF0-0xF2: Clear Unexpected Long Press Detection

Name: CLR_DET_UNKNOWN
Address: 0xF0-0xF2
Description: These registers are for clearing the interrupt of the register "Unexpected Long Press Detection".

0: Interrupt is cleared. 1: Interrupt is not cleared

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xF0	R/W	0x00	CLR_UNK_CS7	CLR_UNK_CS6	CLR_UNK_CS5	CLR_UNK_CS4	CLR_UNK_CS3	CLR_UNK_CS2	CLR_UNK_CS1	CLR_UNK_CS0
0xF1	R/W	0x00	CLR_UNK_CS15	CLR_UNK_CS14	CLR_UNK_CS13	CLR_UNK_CS12	CLR_UNK_CS11	CLR_UNK_CS10	CLR_UNK_CS9	CLR_UNK_CS8
0xF2	R/W	0x00	-	-	-	-	CLR_UNK_CS19	CLR_UNK_CS18	CLR_UNK_CS17	CLR_UNK_CS16

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0xF3-0xF4: Software Reset

Name: SWRST_CMD
Address: 0xF3-0xF4
Description: These registers are used for software reset. When the data of register 0xF3 is set to 0x55 and the data of register 0xF4 is set to 0xAA, IC is initialized and all registers are cleared.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xF3	R/W	0x00	SRST[7:0]							
0xF4	R/W	0x00	SRST[15:8]							

0xFE: AVDD LDO Control

Name: AVDD_CMD
Address: 0xFE
Description: This register controls AVDD LDO.

AVDD_ON : AVDD LDO Control

0: AVDD is disable 1: AVDD is enable

SEL_AVDD [1:0]: AVDD LDO Output Voltage

SEL_AVDD [1:0] = 0x0: AVDD voltage = 2.8V
= 0x1: AVDD voltage = 2.7V
= 0x2: AVDD voltage = 2.6V
= 0x3: AVDD voltage = 2.5V

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xFE	R/W	0x00	-	-	SEL_AVDD[1:0]		-	-	-	AVDD_ON

0xFF: Sensor Control

Name: SENS_CMD
Address: 0xFF
Description: This register controls the sensor.

STR_AFE : Control Sensor

0: Detection stops 1: Detection starts

STR_CAL : Software Calibration Control

0: Calibration is not performed 1: Calibration is performed

STR_CFG : Update Configuration Registers

This bit is for updating configuration register. Set 1 to this bit after changing configuration registers.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xFF	R/W	0x00	-	-	-	-	-	STR_CFG	STR_CAL	STR_AFE

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

10. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

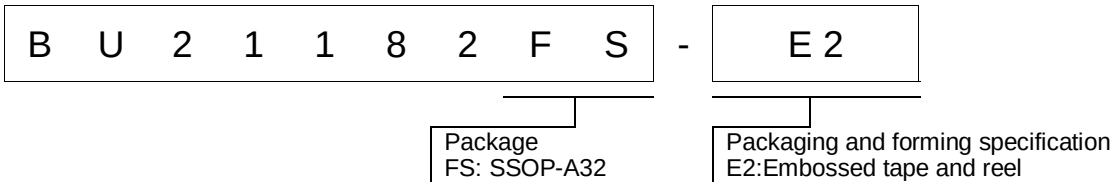
12. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

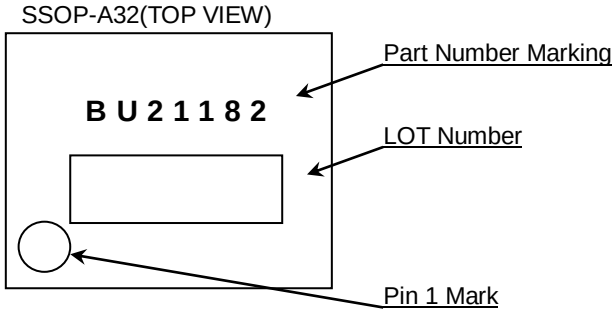
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Ordering Information



Marking Diagram

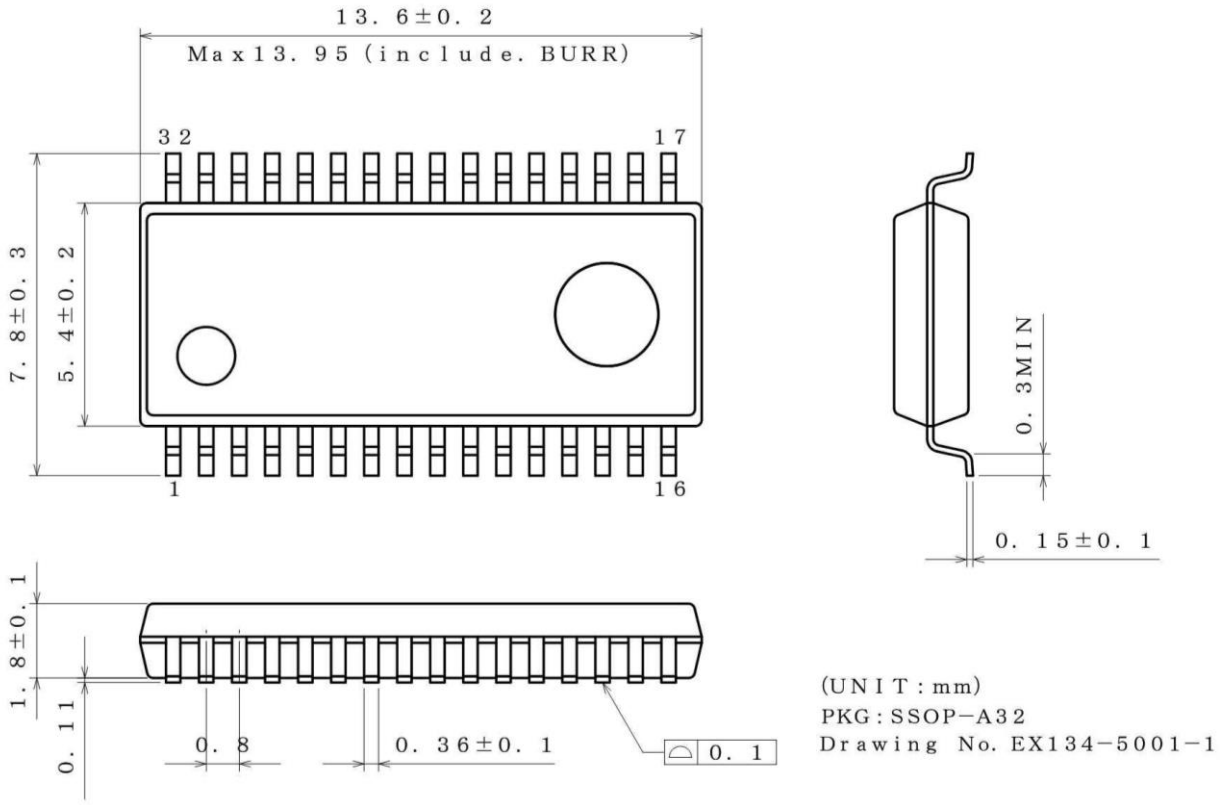


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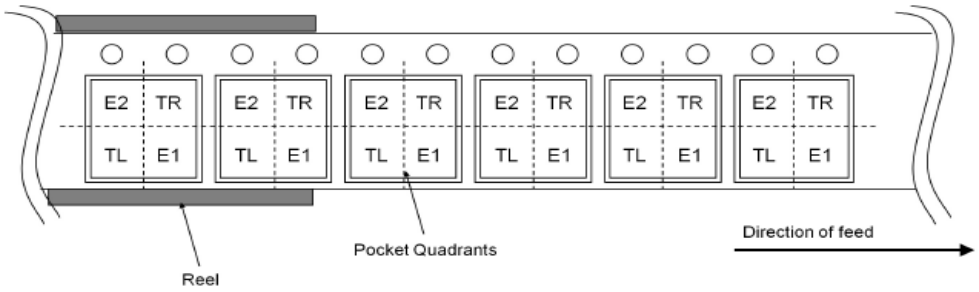
Physical Dimension and Packing Information

Package Name	SSOP-A32



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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Revision History

Date	Revision	Changes
05.Feb.2019	001	New Release

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Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

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