5 V ECL Voltage Controlled Oscillator Amplifier

MC100EL1648



SOIC−8 NB
D SUFFIX
CASE 751−07



TSSOP−8
DT SUFFIX
CASE 948R−02

Description

The MC100EL1648 is a voltage controlled oscillator amplifier that requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C). A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). This device may also be used in many other applications requiring a fixed frequency clock.

The MC100EL1648 is ideal in applications requiring a local oscillator, systems that include electronic test equipment, and digital high−speed telecommunications.

The MC100EL1648 is based on the VCO circuit topology of the MC1648. The MC100EL1648 uses advanced bipolar process technology which results in a design which can operate at an extended frequency range.

The ECL output circuitry of the MC100EL1648 is not a traditional open emitter output structure and instead has an on−chip termination emitter resistor, R_E, with a nominal value of 510 Ω. This facilitates direct ac−coupling of the output signal into a transmission line. Because of this output configuration, an external pull−down resistor is not required to provide the output with a dc current path. This output is intended to drive one ECL load (3.0 pF). If the user needs to fanout the signal, an ECL buffer such as the EL16 (EL11, EL14) type Line Receiver/Driver should be used.

Features

- Typical Operating Frequency Up to 1100 MHz
- Low−Power 19 mA at 5.0 Vdc Power Supply
- PECL Mode Operating Range: V_{CC} = 4.2 V to 5.5 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −4.2 V to −5.5 V
- Input Capacitance = 6.0 pF (TYP)
- These are Pb−Free Devices

NOTE: The MC100EL1648 is NOT useable as a crystal oscillator.

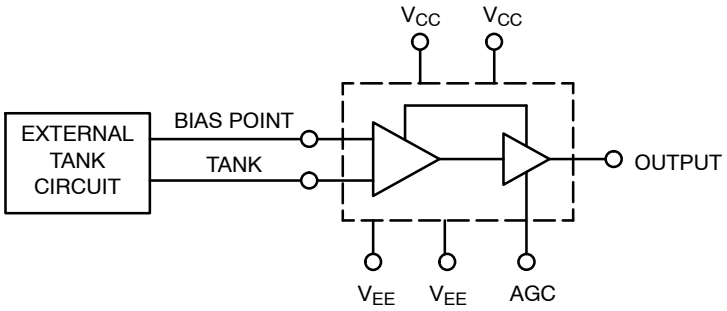
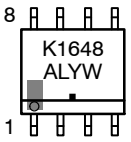
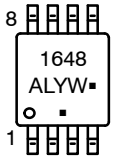


Figure 1. Logic Diagram

MARKING DIAGRAMS*



SOIC−8 NB



TSSOP−8

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

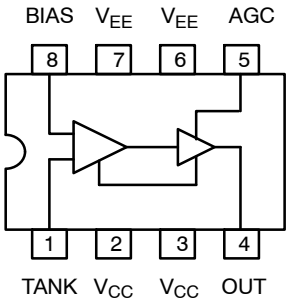
See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

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Table 1. PIN DESCRIPTION

Pin No.	Symbol	Description
1	TANK	OSC Input Voltage
2, 3	V_{CC}	Positive Supply
4	OUT	ECL Output
5	AGC	Automatic Gain Control Input
6, 7	V_{EE}	Negative Output
8	BIAS	OSC Input Reference Voltage



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 2. Pinout Assignments

Table 2. ATTRIBUTES

Characteristic	Value
Internal Input Pulldown Resistor	N/A
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	 > 1 kV > 100 V > 1 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb−Free Pkg
SOIC−8 TSSOP−8	Level 1 Level 3
Flammability Rating Oxygen Index: 23 to 34	 UL 94 V−0 @ 0.125 in
Transistor Count	11
Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test	

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Power Supply PECL Mode	V_{EE} = 0 V		7 to 0	V
V_{EE}	Power Supply NECL Mode	V_{CC} = 0 V		−7 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 to 0 −6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	MA mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	SOIC−8 SOIC−8	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	SOIC−8	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	TSSOP−8 TSSOP−8	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	TSSOP−8	41 to 44	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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Table 4. PECL DC CHARACTERISTICS V_{CC} = 5.0 V; V_{EE} = 0.0 V +0.8 / −0.5 V (Note 2)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	13	19	25	13	19	25	13	19	25	mA
V_{OH}	Output HIGH Voltage (Note 3)	3950	4170	4610	3950	4170	4610	3950	4170	4610	mV
V_{OL}	Output LOW Voltage (Note 3)	3040	3410	3600	3040	3410	3600	3040	3410	3600	mV
AGC	Automatic Gain Control Input	1690		1980	1690		1980	1690		1980	mV
V_{BIAS}	Bias Voltage (Note 4)	1650		1800	1650		1800	1650		1800	mV
V_{IL}		1.5			1.35			1.2			V
V_{IH}				2.0			1.85			1.7	V
I_L	Input Current		−5.0			−5.0			−5.0		mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. Output parameters vary 1:1 with V_{CC}.
3. 1.0 MΩ impedance.
4. This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.

Table 5. NECL DC CHARACTERISTICS V_{CC} = 0.0 V; V_{EE} = −5.0 V +0.8 / −0.5 V (Note 5)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	13	19	25	13	19	25	13	19	25	mA
V_{OH}	Output HIGH Voltage (Note 6)	−1050	−830	−399	−1050	−830	−399	−1050	−830	−399	mV
V_{OL}	Output LOW Voltage (Note 6)	−1960	−1590	−1400	−1960	−1590	−1400	−1960	−1590	−1400	mV
AGC	Automatic Gain Control Input	−3310		−3020	−3310		−3020	−3310		−3020	mV
V_{BIAS}	Bias Voltage (Note 7)	−3350		−3200	−3350		−3200	−3350		−3200	mV
V_{IL}		−3.5			−3.65			−3.8			V
V_{IH}				−3.0			−3.15			−3.3	V
I_L	Input Current		−5.0			−5.0			−5.0		mA

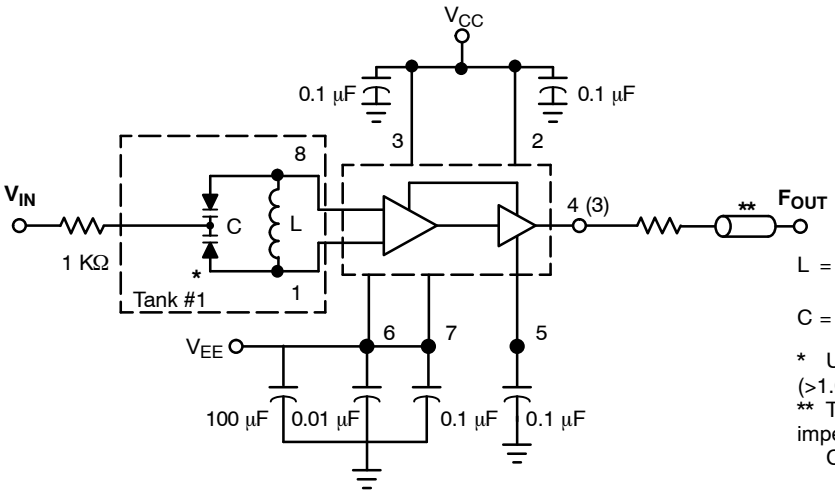
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Output parameters vary 1:1 with V_{CC}.
6. 1.0 MΩ impedance.
7. This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.

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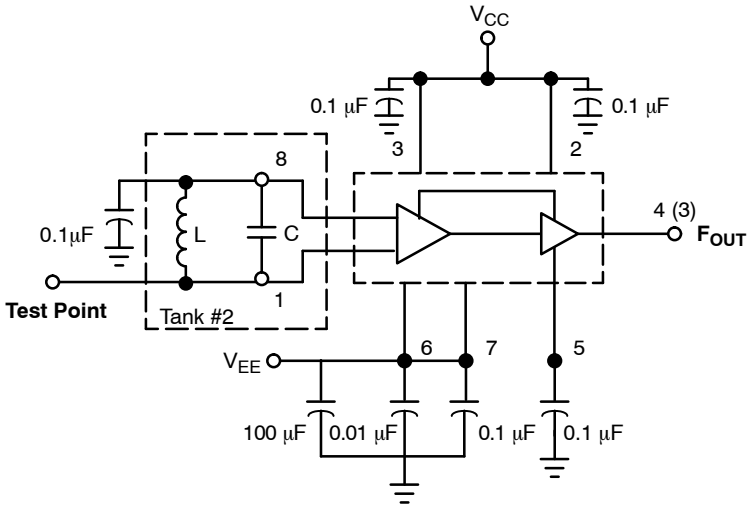
GENERIC TEST CIRCUITS: BYPASS TO SUPPLY OPPOSITE GND



L = Micro Metal torroid #T20−22, 8 turns #30 Enameled Copper wire (@ 40 nH)
C = MMBV609

* Use high impedance probe (>1.0 MΩ must be used).
** The 1200 Ω resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT−070−50 or equivalent.

Tank Circuit Option #1, Varactor Diode



L = Micro Metal torroid #T20−22, 8 turns #30 Enameled Copper wire (@ 40 nH)
C = 3.0−35pF Variable Capacitance (@ 10 pF)

Note 1 Capacitor for tank may be variable type. (See Tank Circuit #3.)
Note 2 Use high impedance probe (> 1 MΩ).

Tank Circuit Option #2, Fixed LC

Figure 3. Typical Test Circuit with Alternate Tank Circuits

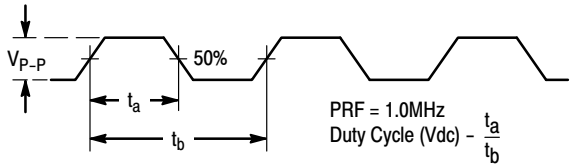


Figure 4. Output Waveform

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OPERATION THEORY

Figure 5 illustrates the simplified circuit schematic for the MC100EL1648. The oscillator incorporates positive feedback by coupling the base of transistor Q6 to the collector of Q7. An automatic gain control (AGC) is incorporated to limit the current through the emitter−coupled pair of transistors (Q7 and Q6) and allow optimum frequency response of the oscillator. In order to maintain the high quality factor (Q) on the oscillator, and provide high spectral purity at the output, transistor Q4 is used to translate the oscillator signal to the output differential pair Q2 and Q3. Figure 16 indicates the high spectral purity of the oscillator output (pin 4 on 8−pin SOIC). Transistors Q2 and Q3, in conjunction with output transistor Q1, provide a highly buffered output that produces a square wave. The typical output waveform can be seen in Figure 4. The bias drive for the oscillator and output buffer is provided by Q9 and Q11 transistors. In order to minimize current, the output circuit is realized as an emitter−follower buffer with an on chip pull−down resistor R_E.

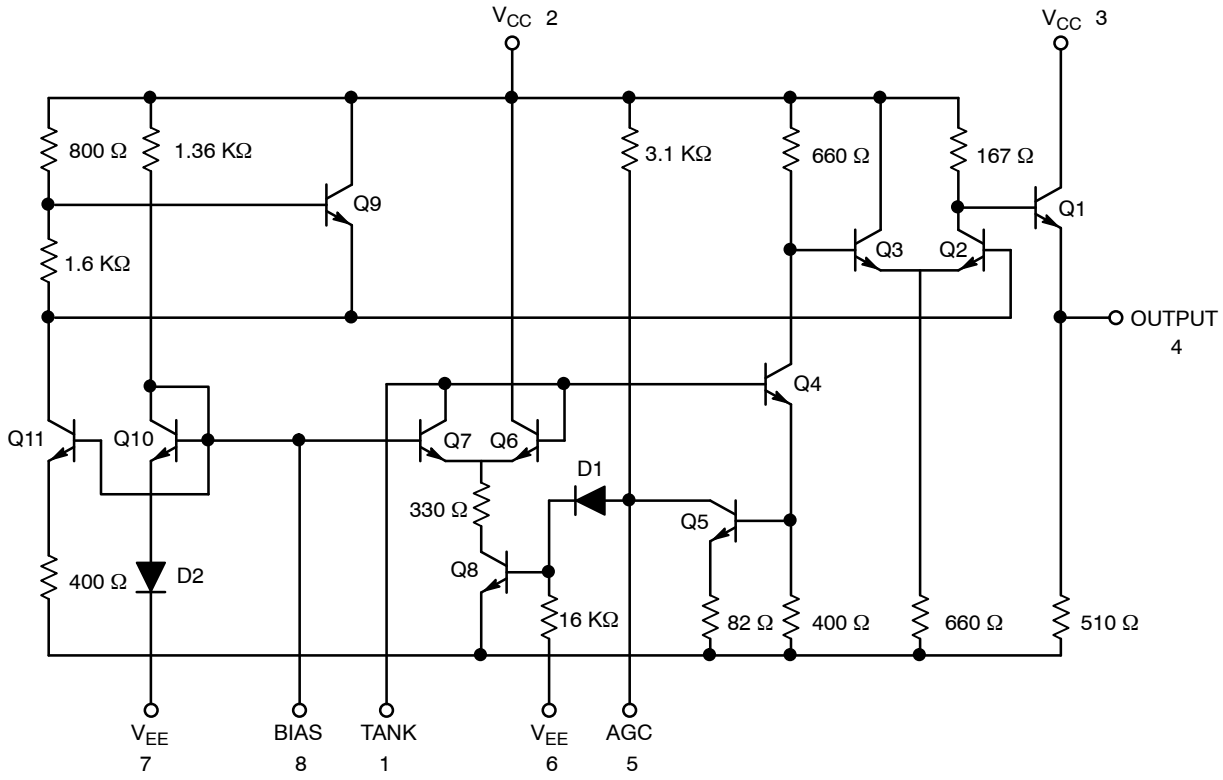


Figure 5. Circuit Schematic

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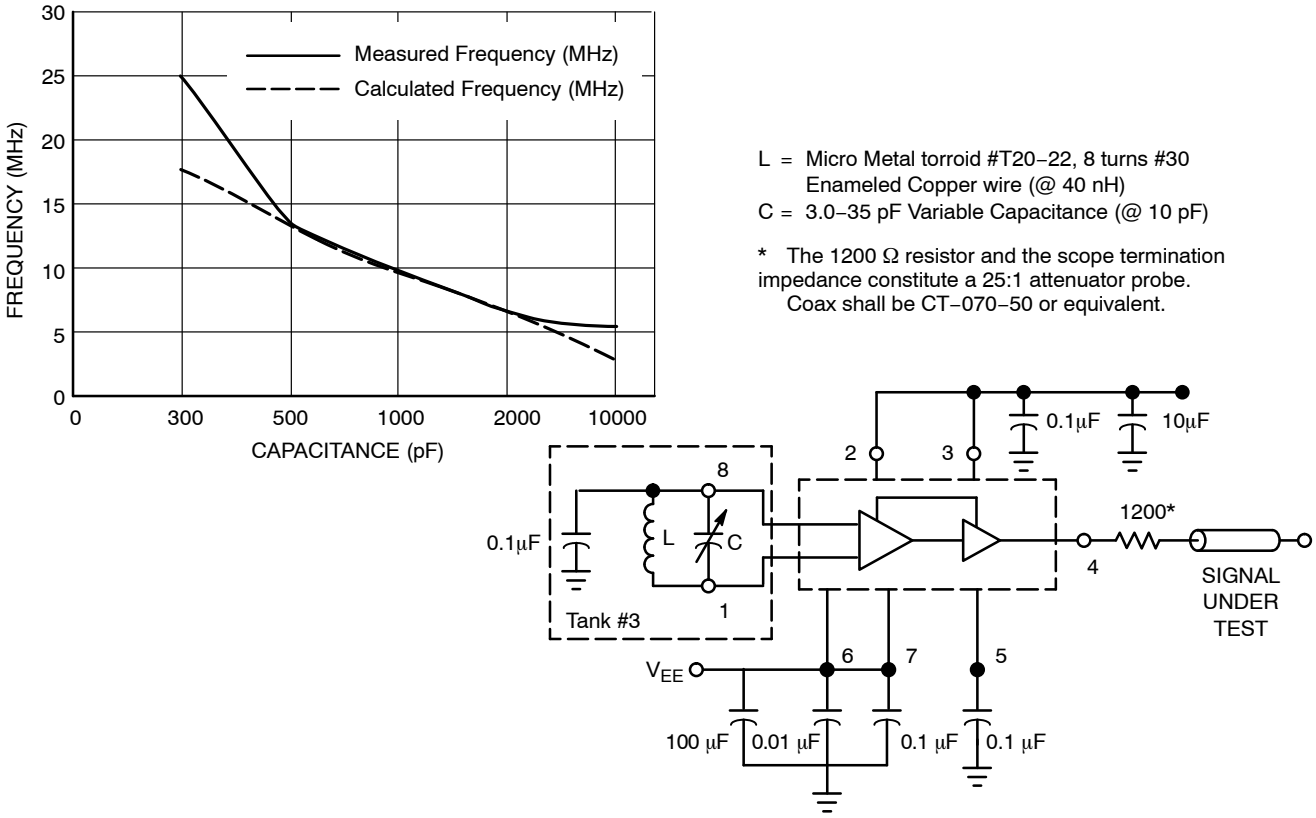


Figure 6. Low Frequency Plot

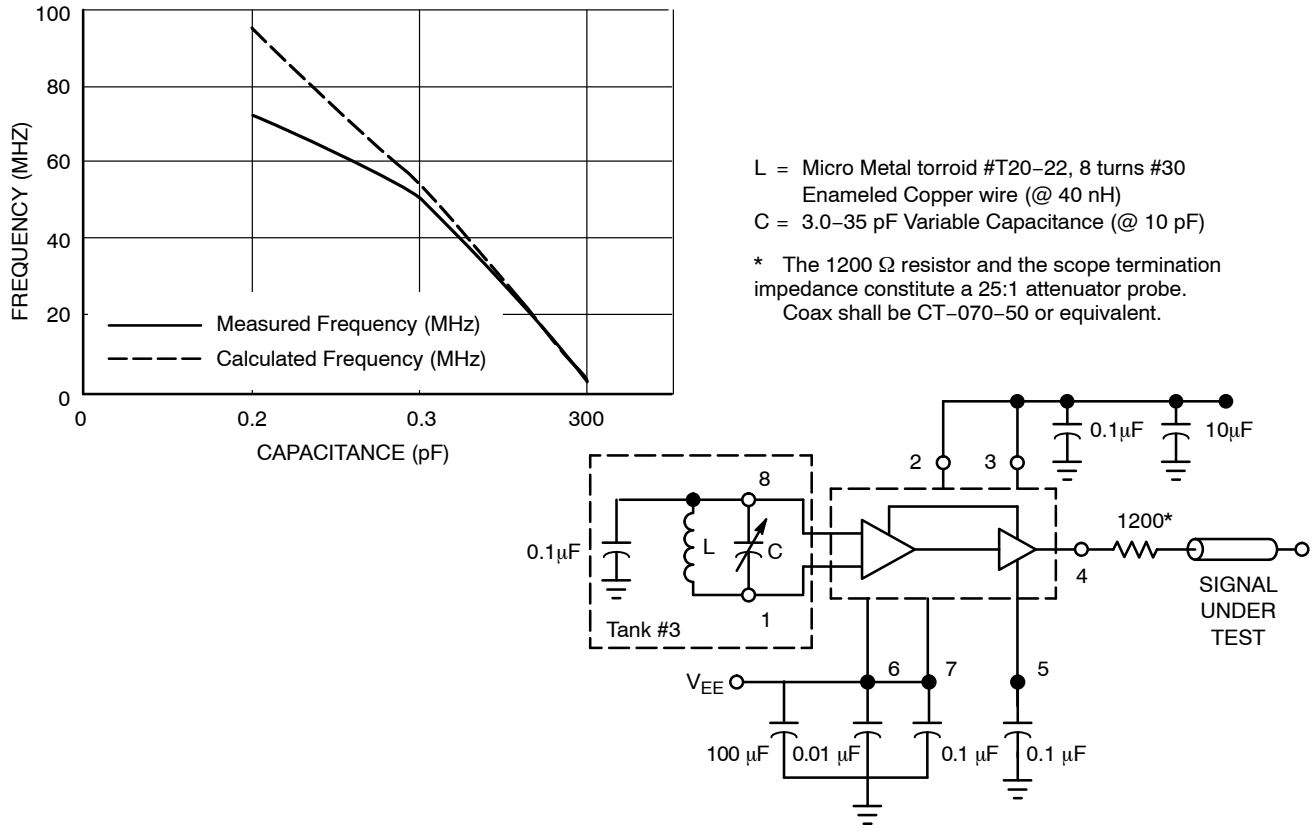


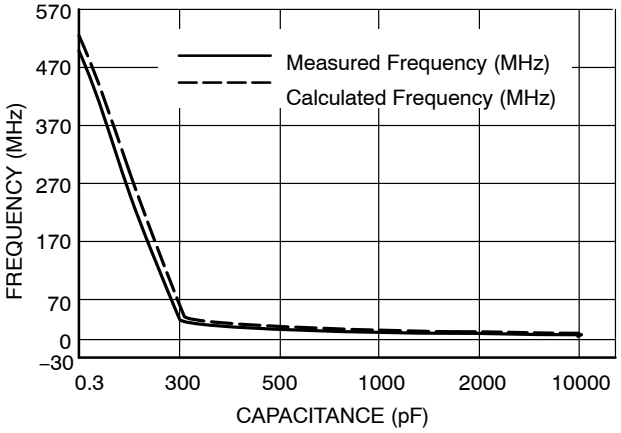
Figure 7. High Frequency Plot

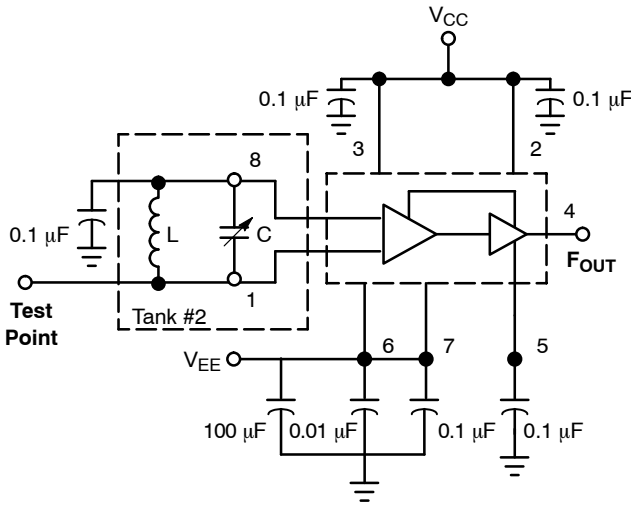
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FIXED FREQUENCY MODE

The MC100EL1648 external tank circuit components are used to determine the desired frequency of operation as shown in Figure 8, tank option #2. The tank circuit components have direct impact on the tuning sensitivity, I_{EE}, and phase noise performance. Fixed frequency of the tank circuit is usually realized by an inductor and capacitor (LC network) that contains a high Quality factor (Q). The plotted curve indicates various fixed frequencies obtained with a single inductor and variable capacitor. The Q of the components in the tank circuit has a direct impact on the resulting phase noise of the oscillator. In general, when the Q is high the oscillator will result in lower phase noise.





L = Micro Metal torroid #T20−22, 8 turns #30 Enameled Copper wire (@ 40 nH)
C = 3.0−35 pF Variable Capacitance (@ 10 pF)
Note 1 Capacitor for tank may be variable type. (See Tank Circuit #3.)
Note 2 Use high impedance probe (> 1 MΩ).

$Q_L \geq 100$

Figure 8. Fixed Frequency LC Tank

Only high quality surface−mount RF chip capacitors should be used in the tank circuit at high frequencies. These capacitors should have very low dielectric loss (high−Q). At a minimum, the capacitors selected should be operating at 100 MHz below their series resonance point. As the desired frequency of operation increases, the values of the tank capacitor will decrease since the series resonance point is a function of the capacitance value. Typically, the inductor is realized as a surface−mount chip or a wound coil. In addition, the lead inductance and board inductance and capacitance also have an impact on the final operating point. The following equation will help to choose the appropriate values for your tank circuit design.

$$f_0 = \frac{1}{2\pi \sqrt{L_T * C_T}}$$

Where L_T = Total Inductance
C_T = Total Capacitance

Figure 9 and Figure 10 represent the ideal curve of inductance/capacitance versus frequency with one known tank component. This helps the designer of the tank circuit to choose desired value of inductor/capacitor component for the wanted frequency. The lead inductance and board inductance and capacitance will also have an impact on the tank component values (inductor and capacitor).

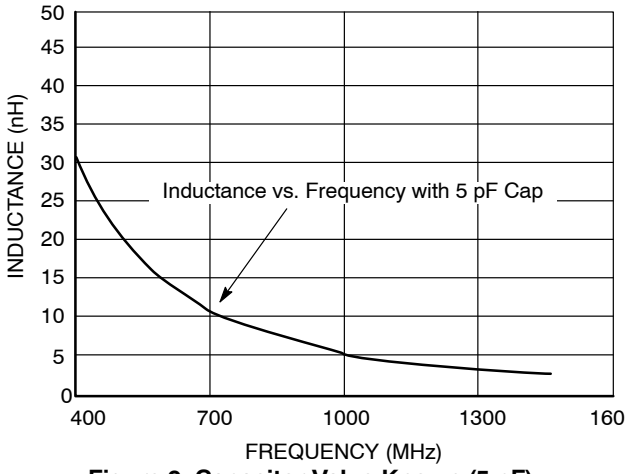


Figure 9. Capacitor Value Known (5 pF)

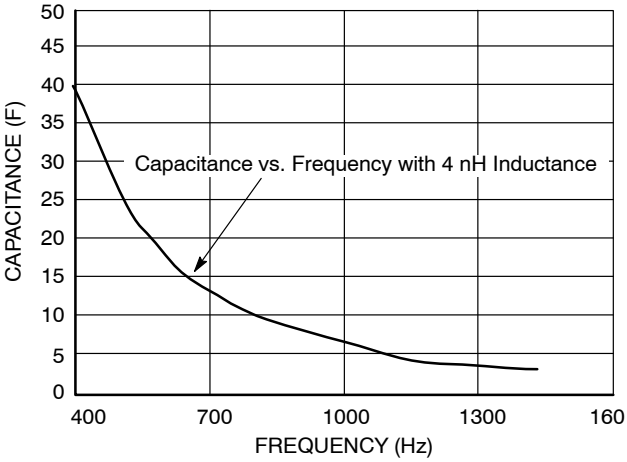


Figure 10. Inductor Value Known (4 nH)

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VOLTAGE CONTROLLED MODE

The tank circuit configuration presented in Figure 11, Voltage Controlled Varactor Mode, allows the VCO to be tuned across the full operating voltage of the power supply. Deriving from Figure 6, the tank capacitor, C, is replaced with a varactor diode whose capacitance changes with the voltage applied, thus changing the resonant frequency at which the VCO tank operates as shown in Figure 3, tank option #1. The capacitive component in Equation 1 also needs to include the input capacitance of the device and other circuit and parasitic elements.

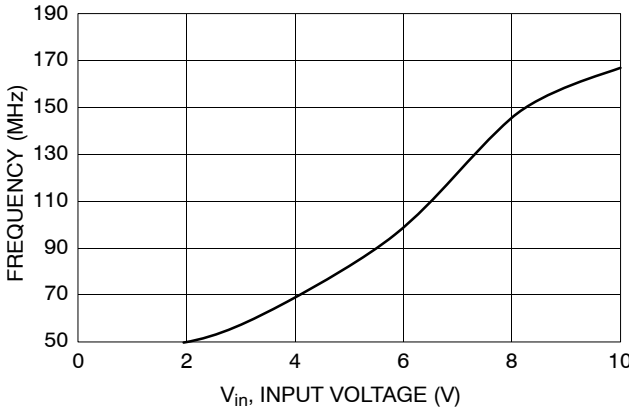
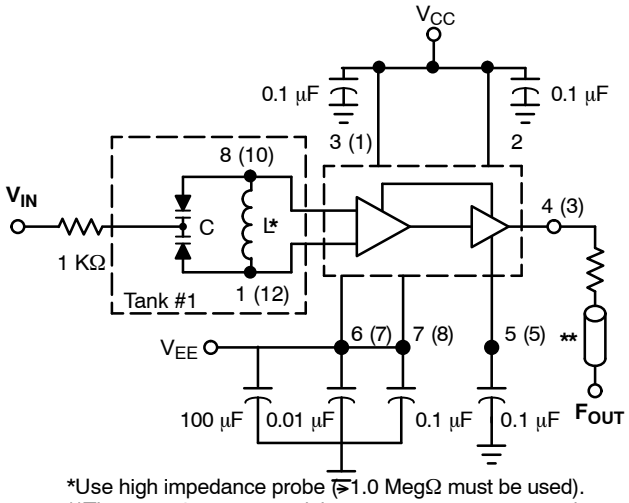


Figure 12. Plot 1. Dual Varactor MMBV609, V_{IN} vs. Frequency



*Use high impedance probe (>1.0 MegΩ must be used).
**The 1200 Ω resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT−070−50 or equivalent.

L = Micro Metal torroid #T20−22, 8 turns #30 Enameled Copper wire (@ 40 nH)
C = MMBV609

Figure 11. Voltage Controlled Varactor Mode

When operating the oscillator in the voltage controlled mode with Tank Circuit #1 (Figure 3), it should be noted that the cathode of the varactor diode (D), pin 8 (for 8 lead package) or pin 10 (for 14 lead package) should be biased at least 1.4 V above V_{EE}.

Typical transfer characteristics employing the capacitance of the varactor diode (plus the input capacitance of the device, about 6.0 pF typical) in the voltage controlled mode is shown in Plot 1, Dual Varactor MMBV609 V_{in} vs. Frequency. Figure 6, Figure 7, and Figure 8 show the accuracy of the measured frequency with the different variable capacitance values. The 1.0 kΩ resistor in Figure 11 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The tuning range of the oscillator in the voltage controlled mode may be calculated as follows:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D(max) + C_S}}{\sqrt{C_D(min) + C_S}}$$

Where

$$f_{min} = \frac{1}{2\pi\sqrt{(L(C_D(max) + C_S)}}$$

Where

C_S = Shunt Capacitance (input plus external capacitance)

C_D = Varactor Capacitance as a function of bias voltage

Good RF and low−frequency bypassing is necessary on the device power supply pins. Capacitors on the AGC pin and the input varactor trace should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points. For output frequency operation between 1.0 MHz and 50 MHz, a 0.1 μF capacitor is sufficient. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At high frequencies, the value of bypass capacitors depends directly on the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance. Several different capacitors may be needed to bypass various frequencies.

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WAVE−FORM CONDITIONING − SINE OR SQUARE WAVE

The peak−to−peak swing of the tank circuit is set internally by the AGC pin. Since the voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the MC100EL1648, a series resistor is tied from the AGC point to the most negative power potential (ground if positive volt supply is used, −5.2 V if a negative supply is used) as shown in Figure 13. At frequencies above 100 MHz typical, it may be desirable to increase the tank circuit peak−to−peak voltage in order to shape the signal into a more square waveform at the output of the MC100EL1648. This is accomplished by tying a series resistor (1.0 kΩ minimum) from the AGC to the most positive power potential (+5.0 V if a positive volt supply is used, ground if a −5.2 V supply is used). Figure 14 illustrates this principle.

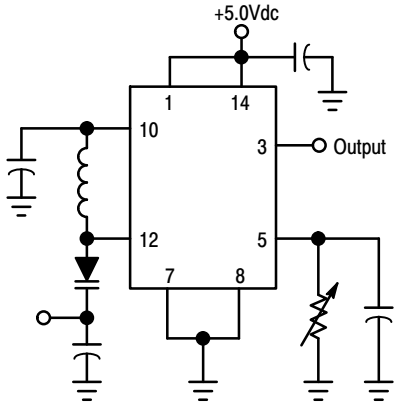


Figure 13. Method of Obtaining a Sine−Wave Output

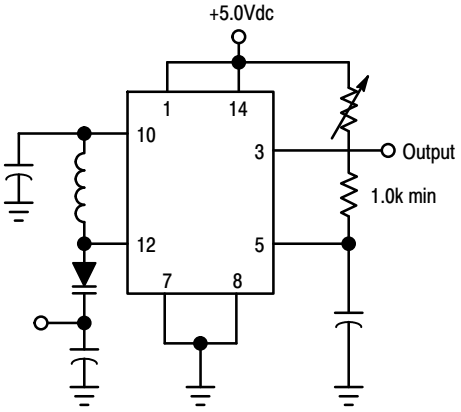
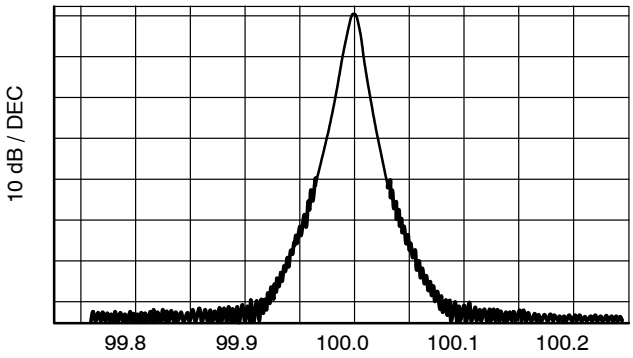


Figure 14. Method of Extending the Useful Range of the MC100EL1648 (Square Wave Output)

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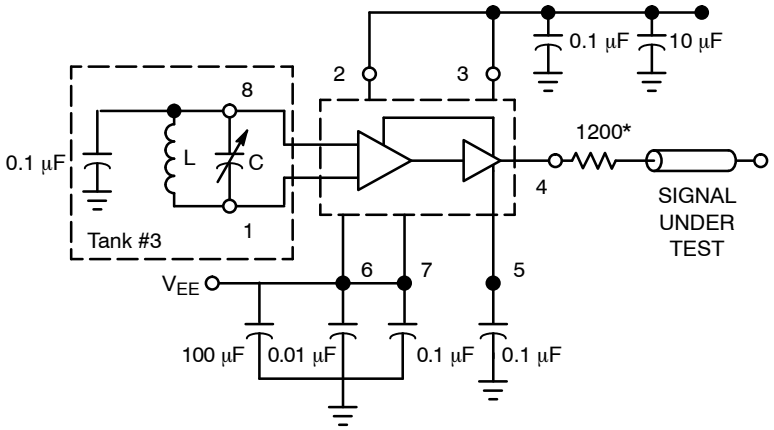
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SPECTRAL PURITY



B.W. = 10 kHz, Center Frequency = 100 MHz
Scan Width = 50 kHz/div, Vertical Scale = 10 dB/div

Figure 15. Spectral Purity



L = Micro Metal torroid #T20−22, 8 turns #30 Enameled Copper wire (@ 40 nH)
C = 3.0−35 pF Variable Capacitance (@ 10 pF)

** The 1200 Ω resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT−070−50 or equivalent.

Spectral Purity Test Circuit

Figure 16. Spectral Purity of Signal Output for 200 MHz Testing

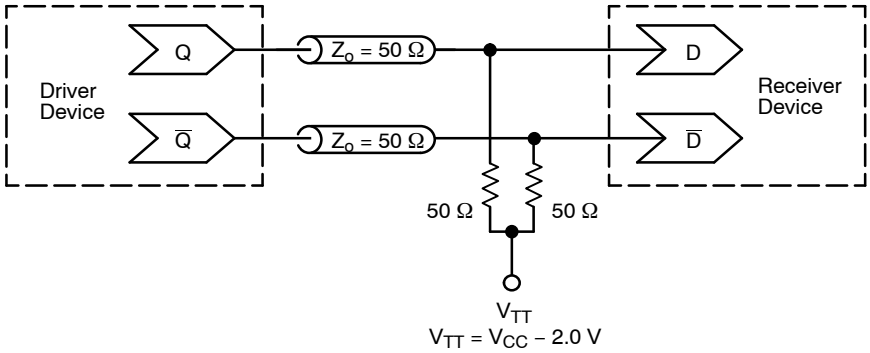


Figure 17. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

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ORDERING INFORMATION

Device	Package	Shipping†
MC100EL1648DG	SOIC−8 NB (Pb−Free)	2500 / Tape & Reel
MC100EL1648DTR2G	TSSOP−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

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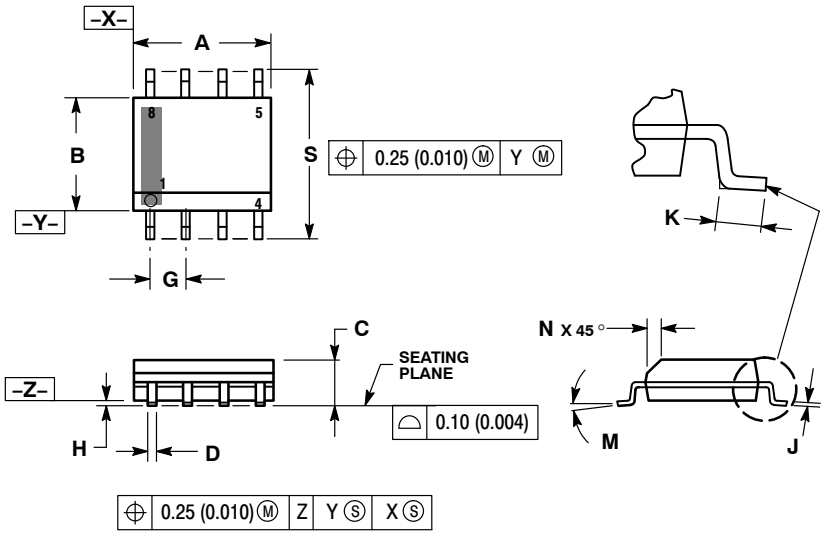
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SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

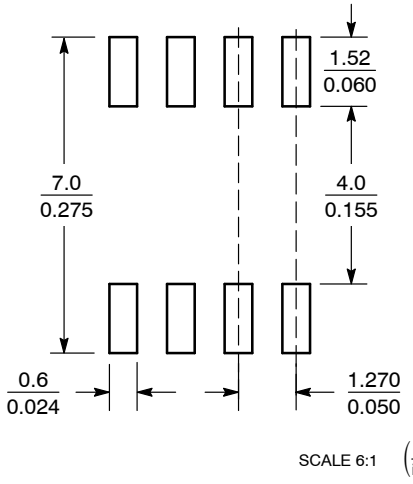
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NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

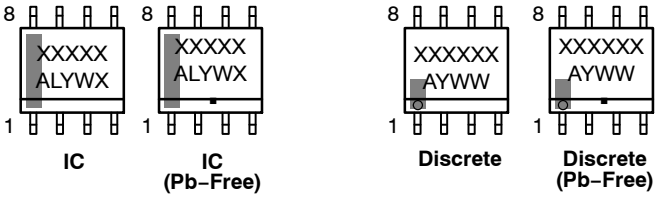
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

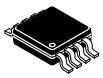
STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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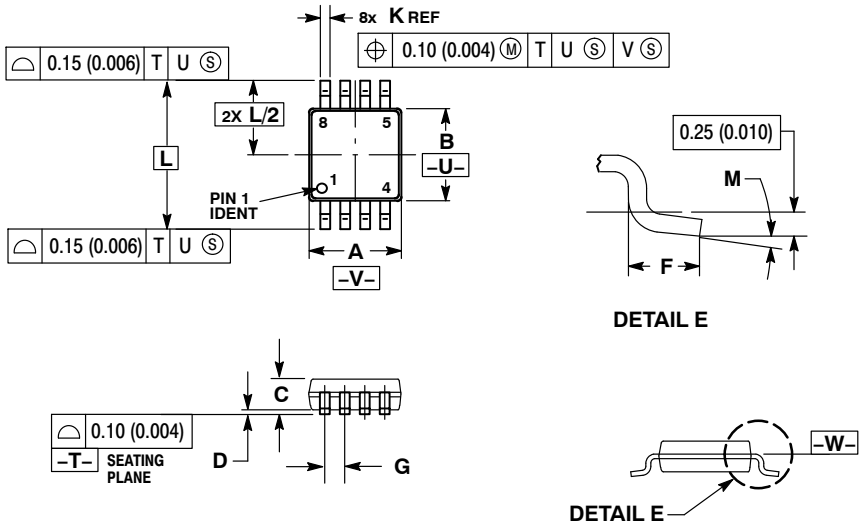
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SCALE 2:1

TSSOP−8 3.00x3.00x0.95
CASE 948R−02
ISSUE A

DATE 07 APR 2000



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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