

MOSFET - N-Channel, SUPERFET[®] II

600 V, 47 A, 70 m Ω

FCH47N60

Description

SuperFET II MOSFET is onsemi's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low onresistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.

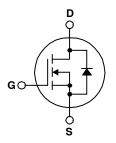
Features

- Typ. $R_{DS(on)} = 58 \text{ m}\Omega$
- $650 \text{ V} @ \text{T}_{\text{J}} = 150^{\circ}\text{C}$
- Ultra Low Gate Charge (Typ. Q_g = 210 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 420 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

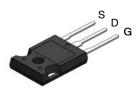
Applications

- Telecom / Sever Power Supplies
- Industrial Power Supplies

V _{DS}	R _{DS(ON)} MAX	I _D MAX	
600 V	70 mΩ @ 10 V	47 A	



N-CHANNEL MOSFET



TO-247-3LD CASE 340CK

MARKING DIAGRAM



\$Y = onsemi Logo = Assembly Plant Code &Z = Numeric Date Code &3 &K = Lot Code

FCH47N60 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C unless otherwise noted)

Symbol	Parameter		FCH47N60	Unit
V_{DSS}	Drain to Source Voltage		600	V
V_{GSS}	Gate to Source Voltage		±30	
I _D	Drain Current:	Drain Current: – Continuous (T _C = 25 °C)		А
		- Continuous (T _C = 100 °C)	29.7]
I _{DM}	Drain Current:	- Pulsed (Note 1)	141	А
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		1800	mJ
I _{AR}	Avalanche Current (Note 1)		47	А
E _{AR}	Repetitive Avalanche Energy (Note 1) Peak Diode Recovery dv/dt (Note 3)		41.7	mJ
dv/dt			4.5	V/ns
P_{D}	Power Dissipation (T _C = 25 °C) - Derate Above 25 °C		417	W
			3.33	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to + 150	°C
TL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Repetitive rating: pulse-width limited by maximum junction temperature. 2. $I_{AS} = 18 \text{ A}, V_{DD} = 50 \text{ V}, R_G = 25 \Omega, \text{ Starting } T_J = 25 ^{\circ}\text{C}.$ 3. $I_{SD} \le 48 \text{ A}, \text{ di/dt} \le 200 \text{ A/}{\mu}\text{s}, V_{DD} \le \text{BV}_{DSS}, \text{ Starting } T_J = 25 ^{\circ}\text{C}.$

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH47N60_F133	FCH47N60	TO-247	Tube	N/A	N/A	30 Units

THERMAL CHARACTERISTICS

Symbol	Parameter	FCH47N60	Unit
R _{θJC} Thermal Resistance, Junction to Case, Max.		0.3	°C/W
R _{θJA} Thermal Resistance, Case-to-Sink, Typ.		0.24	°C/W
R _{θJA} Thermal Resistance, Junction to Ambient, Max.		41.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
OFF CHAR	ACTERISTICS					
BV _{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μ A, T_C = 25 $^{\circ}$ C	600	_	_	V
		$V_{GS} = 0 \text{ V,I}_D = 250 \mu\text{A}, T_C = 150^{\circ}\text{C}$	_	650	_	
$\Delta BV_{DSS} / \Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25 °C	-	0.6	_	V/°C
BV _{DS}	Drain to Source Avalanche Breadown Voltage	V _{GS} = 0 V, I _D = 47 A	-	700	_	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 600 V, V _{GS} = 0 V	_	-	1	μΑ
		V _{DS} = 480 V, T _C = 125 °C	_	-	10	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	_	-	±100	nA
ON CHARA	ACTERISTICS					
V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	3	_	5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 23.5 A	_	0.058	0.070	Ω
9FS	Forward Transconductance	V _{DS} = 40 V, I _D = 23.5 A	_	40	_	S
DYNAMIC (CHARACTERISTICS				•	
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	-	5900	8000	pF
C _{oss}	Output Capacitance		-	3200	4200	pF
C _{rss}	Reverse Transfer Capacitance		-	250	-	pF
C _{oss}	Output Capacitance	V _{DS} = 480 V, V _{GS} = 0 V, f = 1.0 MHz	_	160	-	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	-	420	-	pF
SWITCHIN	G CHARACTERISTICS					
t _{d(on)}	Turn-On Delay Time	V _{DD} = 300 V, I _D = 47 A,	-	185	430	ns
t _r	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, R_g = 25 \Omega$ (Note 4)	_	210	450	ns
t _{d(off)}	Turn-Off Delay Time	7	_	520	1100	ns
t _f	Turn-Off Fall Time	1	_	75	160	ns
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 480 V, I _D = 47 A, V _{GS} = 10 V	_	210	270	nC
Q _{gs}	Gate to Source Gate Charge	(Note 4)	_	38	_	nC
Q _{gd}	Gate to Drain "Miller" Charge	7	-	110	-	nC
	URCE DIODE CHARACTERISTICS	-	-	-	-	-
I _S	Maximum Continuous Source to Drain Diode Forward Current			-	47	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	_	141	Α
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 47 A	-	_	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 47 A,	-	590	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_{F}/dt = 100 A/\mu s$	_	25	-	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

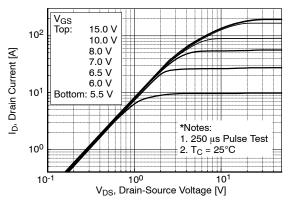


Figure 1. On-Region Characteristics

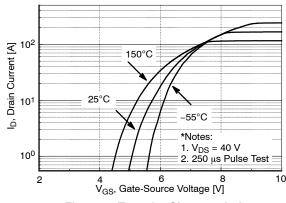


Figure 2. Transfer Characteristics

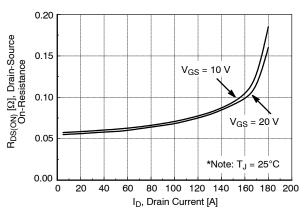


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

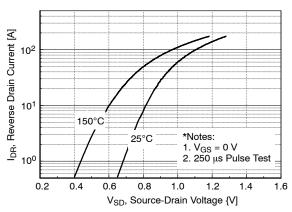


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

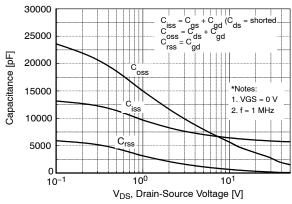


Figure 5. Capacitance Characteristics

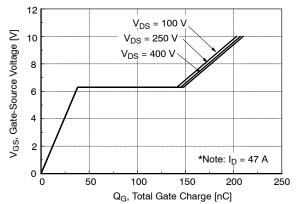


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

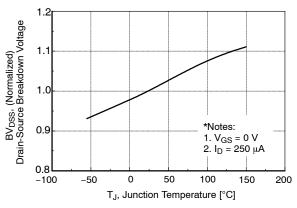


Figure 7. Breakdown Voltage Variation vs. Temperature

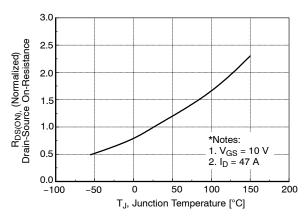


Figure 8. On-Resistance Variation vs. Temperature

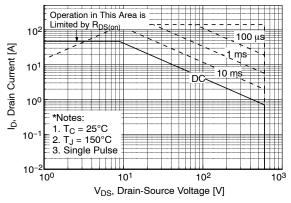


Figure 9. Safe Operating Area

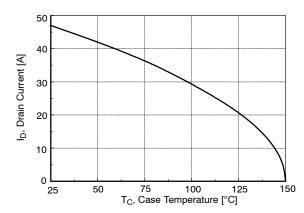


Figure 10. Maximum Drain Current vs.

Case Temperature

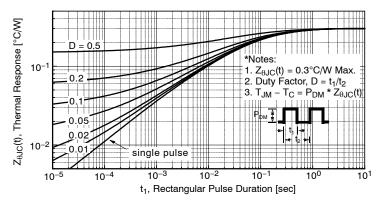


Figure 11. Transient Thermal Response Curve

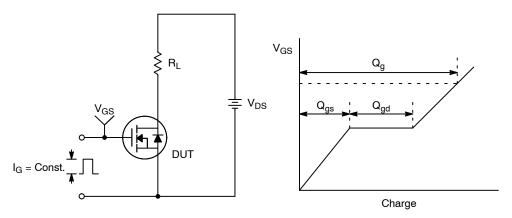


Figure 12. Gate Charge Test Circuit & Waveform

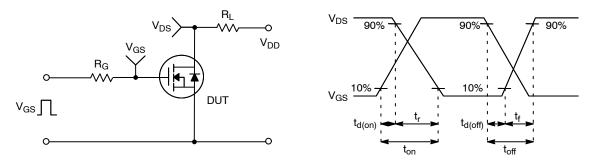


Figure 13. Resistive Switching Test Circuit & Waveforms

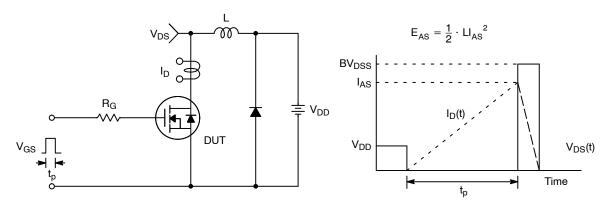


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

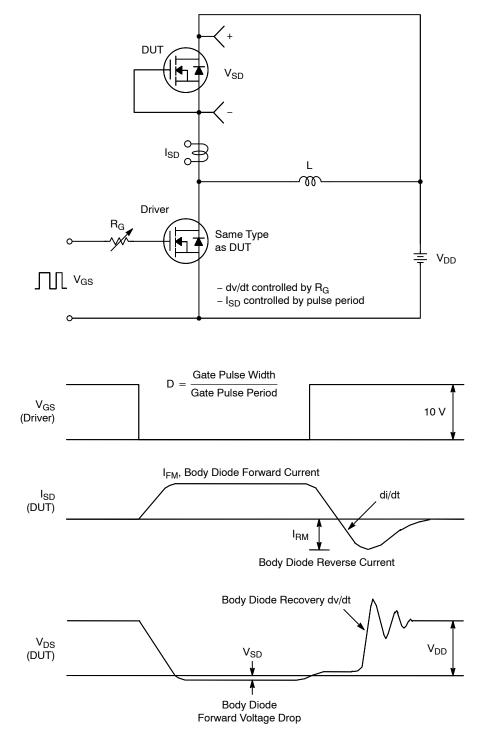


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

SUPERFET is a registered trademark of of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

REVISION HISTORY

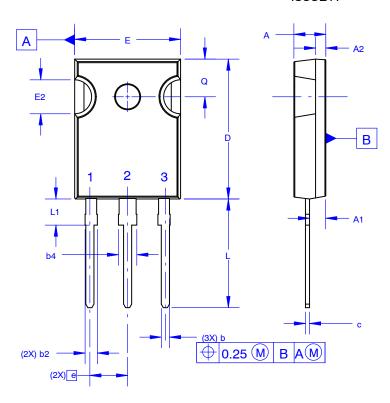
Revision	Description of Changes	Date
4	Rebranded the Data Sheet to onsemi format.	07/23/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



TO-247-3LD SHORT LEAD

CASE 340CK ISSUE A



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code

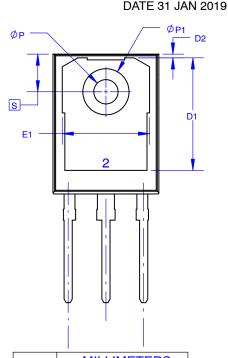
A = Assembly Location

Y = Year

WW = Work Week

ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



DIM	MILLIMETERS			
DIIVI	MIN	NOM	MAX	
Α	4.58	4.70	4.82	
A1	2.20	2.40	2.60	
A2	1.40	1.50	1.60	
b	1.17	1.26	1.35	
b2	1.53	1.65	1.77	
b4	2.42	2.54	2.66	
С	0.51	0.61	0.71	
D	20.32	20.57	20.82	
D1	13.08	~	~	
D2	0.51	0.93	1.35	
E	15.37	15.62	15.87	
E1	12.81	~	~	
E2	4.96	5.08	5.20	
е	~	5.56	~	
L	15.75	16.00	16.25	
L1	3.69	3.81	3.93	
ØΡ	3.51	3.58	3.65	
Ø P1	6.60	6.80	7.00	
Q	5.34	5.46	5.58	
S	5.34	5.46	5.58	

DOCUMENT NUMBER:	98AON13851G	Electronic versions are uncontrolled except when accessed directly from the Document Repositor Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.		
DESCRIPTION:	TO-247-3LD SHORT LEAD		PAGE 1 OF 1	

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, Onsemi, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi's product/patent coverage may be accessed at <a href="www.onsemi.org/www.onsemi.or

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

 $\textbf{Technical Library:} \ \underline{www.onsemi.com/design/resources/technical-documentation}$

onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

