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# NTGD3133P

## Power MOSFET

–20 V, –2.5 A, P–Channel, TSOP–6 Dual

### Features

- Reduced Gate Charge for Fast Switching
- –2.5 V Gate Rating
- Leading Edge Trench Technology for Low On Resistance
- Independent Devices to Provide Design Flexibility
- This is a Pb–Free Device

### Applications

- Li–Ion Battery Charging
- Load Switch / Power Switching
- DC to DC Conversion
- Portable Devices like PDA's, Cellular Phones, and Hard Drives

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain–to–Source Voltage		$V_{DS}$	–20	V
Gate–to–Source Voltage		$V_{GS}$	$\pm 12$	V
Continuous Drain Current (Note 1)	Steady State	$I_D$	$T_A = 25^\circ\text{C}$	A
			$T_A = 85^\circ\text{C}$	
	$t \leq 5 \text{ s}$		$T_A = 25^\circ\text{C}$	
Power Dissipation (Note 1)	Steady State	$P_D$	$T_A = 25^\circ\text{C}$	W
	$t \leq 5 \text{ s}$			
Continuous Drain Current (Note 2)	Steady State	$I_D$	$T_A = 25^\circ\text{C}$	A
			$T_A = 85^\circ\text{C}$	
Power Dissipation (Note 2)		$P_D$	$T_A = 25^\circ\text{C}$	W
Pulsed Drain Current		$t_p = 10 \mu\text{s}$	$I_{DM}$	A
Operating Junction and Storage Temperature		$T_J, T_{STG}$	–55 to 150	$^\circ\text{C}$
Source Current (Body Diode)		$I_S$	–0.8	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

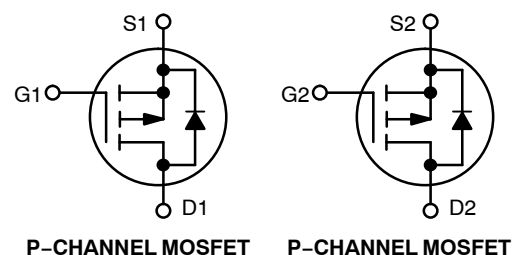
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size (Cu area = 30 mm<sup>2</sup> [2 oz] including traces).



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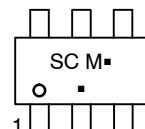
$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
–20 V	145 m $\Omega$ @ –4.5 V	–2.2 A
	200 m $\Omega$ @ –2.5 V	–1.6 A



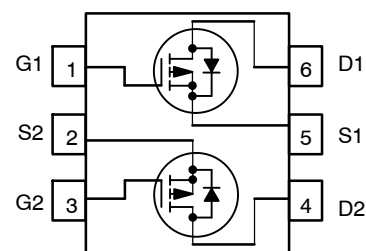
TSOP6  
CASE 318G  
STYLE 13

SC = Specific Device Code  
M = Date Code  
■ = Pb–Free Package  
(Note: Microdot may be in either location)

### MARKING DIAGRAM



### PIN CONNECTION



### ORDERING INFORMATION

Device	Package	Shipping†
NTGD3133PT1G	TSOP6 (Pb–Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	115	°C/W
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	95	
Junction-to-Ambient – Steady State Min Pad (Note 4)	$R_{\theta JA}$	225	

3. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

4. Surface Mounted on FR4 Board using the minimum recommended pad size (Cu area = 30 mm<sup>2</sup> [2 oz] including traces).

MOSFET ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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## OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V	$I_D = -250$ $\mu$ A	-20	–	–	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			–	14.2	–	mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0$ V, $V_{DS} = -16$ V	$T_J = 25^\circ\text{C}$	–	–	-1.0	$\mu$ A
			$T_J = 85^\circ\text{C}$	–	–	-10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 12$ V		–	–	$\pm 100$	nA

## ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$	$I_D = -250$ $\mu$ A	-0.6	-0.95	-1.4	V
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5$ V, $I_D = -2.2$ A		–	90	145	m $\Omega$
		$V_{GS} = -2.5$ V, $I_D = -1.6$ A		–	140	200	
Forward Transconductance	$g_{FS}$	$V_{DS} = -5.0$ V, $I_D = -2.2$ A		–	4.5	–	S

## CHARGES, CAPACITANCES &amp; GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0$ V, $V_{DS} = -10$ V, $f = 1.0$ MHz	–	400	–	pF
Output Capacitance	$C_{OSS}$		–	75	–	
Reverse Transfer Capacitance	$C_{RSS}$		–	40	–	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5$ V, $V_{DS} = -10$ V, $I_D = -2.2$ A	–	3.8	5.5	nC
Threshold Gate Charge	$Q_{G(TH)}$		–	0.5	–	
Gate-to-Source Charge	$Q_{GS}$		–	0.9	–	
Gate-to-Drain Charge	$Q_{GD}$		–	1.0	–	

## SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5$ V, $V_{DD} = -10$ V, $I_D = -1.0$ A, $R_G = 6.0$ $\Omega$	–	6.7	–	ns
Rise Time	$t_r$		–	12.7	–	
Turn-Off Delay Time	$t_{d(OFF)}$		–	13.2	–	
Fall Time	$t_f$		–	11	–	

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, T_J = 25^{\circ}\text{C}$	$I_S = -0.8\text{ A}$	–	–0.8	–1.2	V
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V},$ $dI_{SD} / dt = 100\text{ A}/\mu\text{s}, I_S = -0.8\text{ A}$		–	12	–	ns
Charge Time	$t_a$			–	8.0	–	
Discharge Time	$t_b$			–	4.0	–	
Reverse Recovery Charge	$Q_{RR}$			–	4.0	–	nC

5. Pulse Test: pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2\%$ .

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CHARACTERISTICS

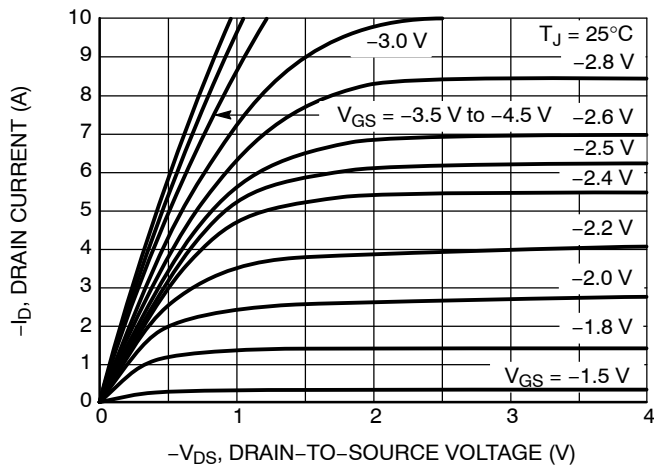


Figure 1. On-Region Characteristics

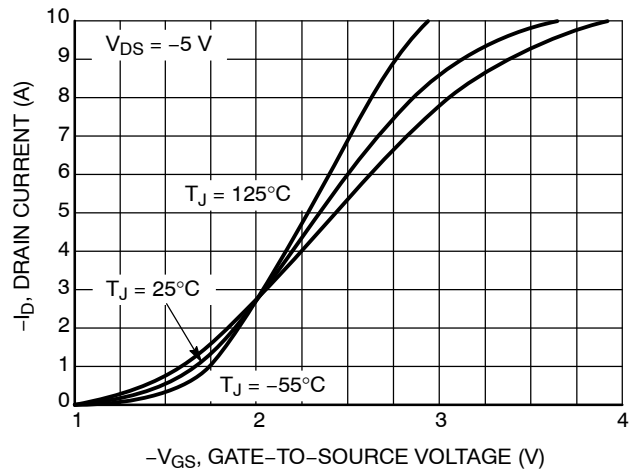


Figure 2. Transfer Characteristics

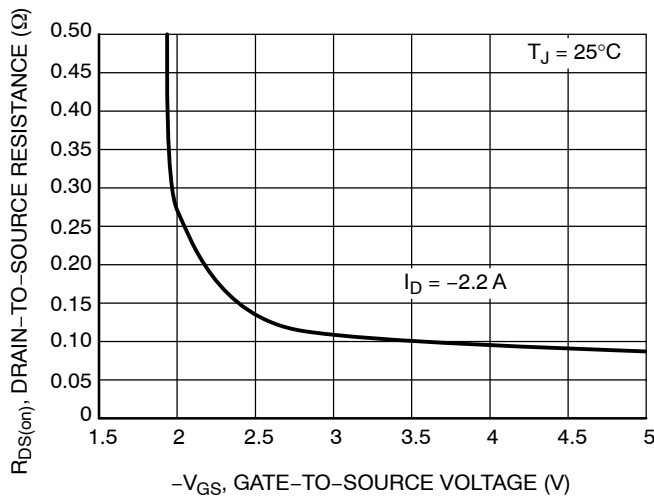


Figure 3. On-Resistance versus Gate-to-Source Voltage

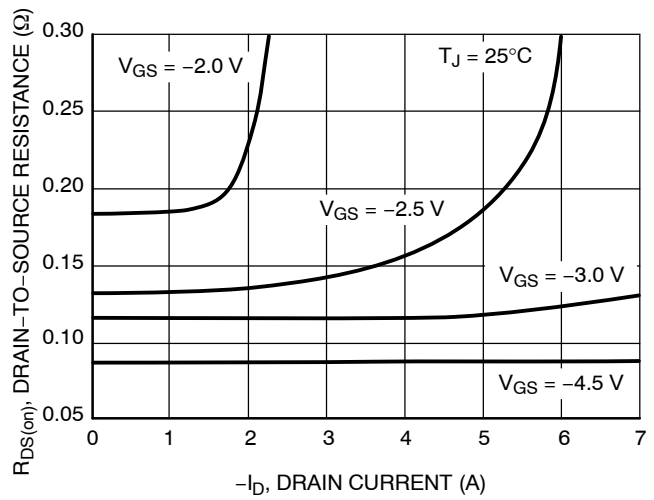


Figure 4. On-Resistance versus Drain Current and Gate Voltage

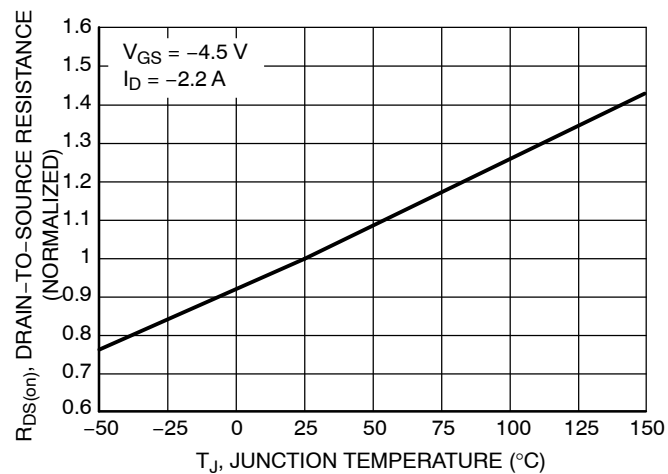


Figure 5. On-Resistance Variation with Temperature

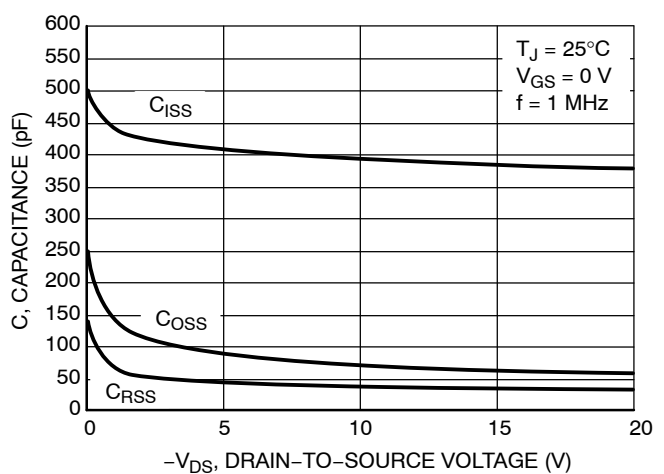


Figure 6. Capacitance Variation

TYPICAL PERFORMANCE CHARACTERISTICS

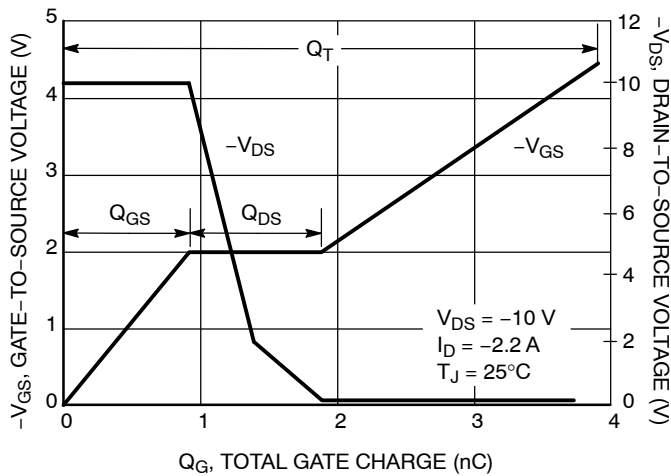


Figure 7. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

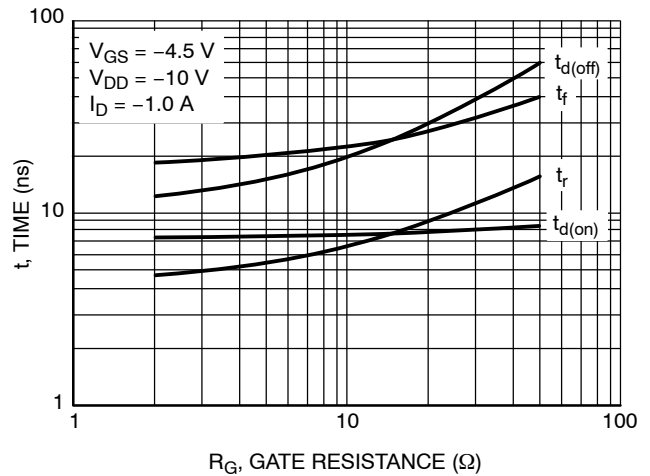


Figure 8. Resistive Switching Time Variation versus Gate Resistance

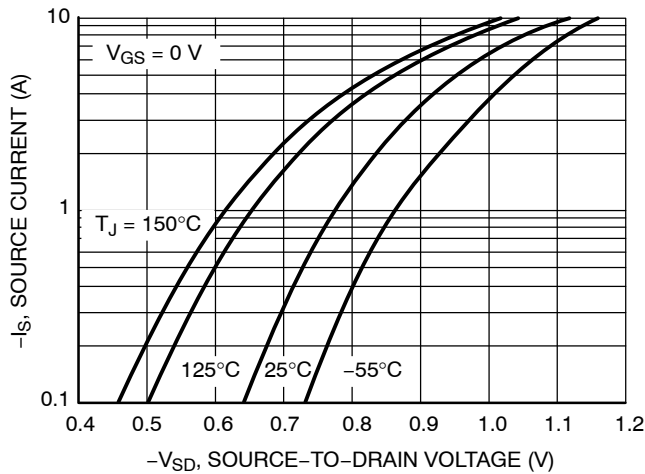


Figure 9. Diode Forward Voltage versus Current

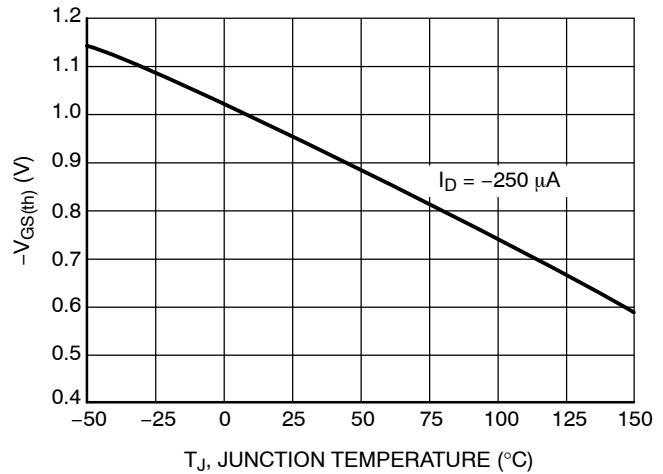


Figure 10. Threshold Voltage

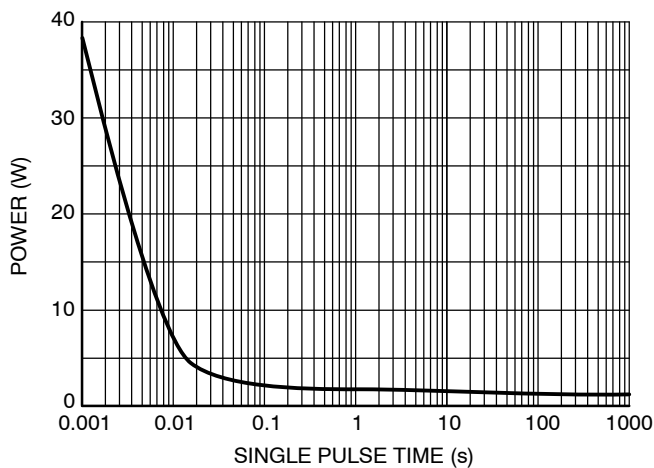


Figure 11. Single Pulse Maximum Power Dissipation

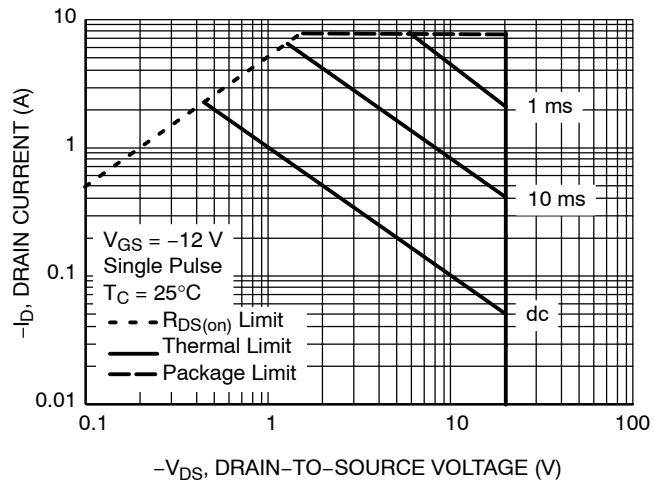


Figure 12. Maximum Rated Forward Biased Safe Operating Area

# NTGD3133P

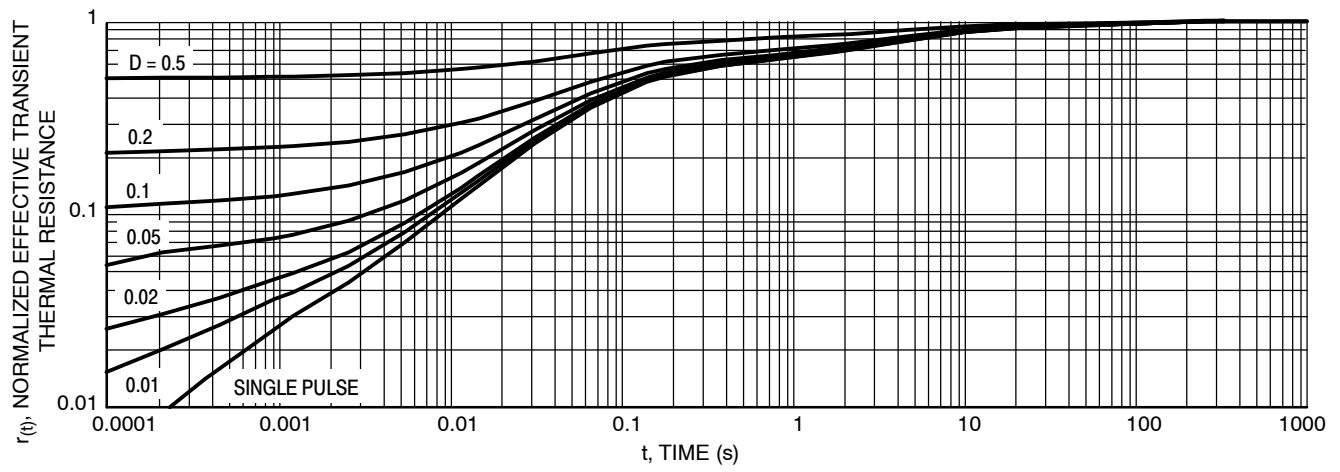


Figure 13. Thermal Response

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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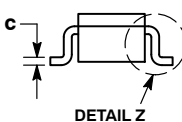
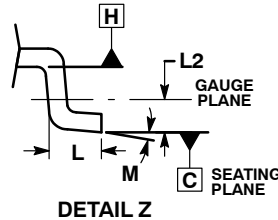
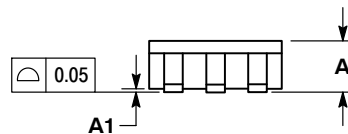
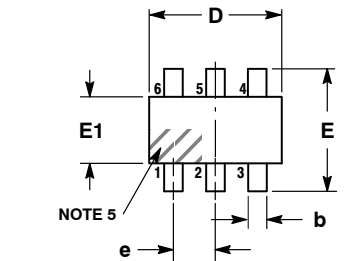
SCALE 2:1

### TSOP-6

#### CASE 318G-02

#### ISSUE V

DATE 12 JUN 2012



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	—	10°

#### STYLE 1:

- PIN 1. DRAIN
- PIN 2. DRAIN
- PIN 3. GATE
- PIN 4. SOURCE
- PIN 5. DRAIN
- PIN 6. DRAIN

#### STYLE 2:

- PIN 1. EMITTER 2
- PIN 2. BASE 1
- PIN 3. COLLECTOR 1
- PIN 4. EMITTER 1
- PIN 5. BASE 2
- PIN 6. COLLECTOR 2

#### STYLE 3:

- PIN 1. ENABLE
- PIN 2. N/C
- PIN 3. R BOOST
- PIN 4. Vz
- PIN 5. V in
- PIN 6. V out

#### STYLE 4:

- PIN 1. N/C
- PIN 2. V in
- PIN 3. NOT USED
- PIN 4. GROUND
- PIN 5. ENABLE
- PIN 6. LOAD

#### STYLE 5:

- PIN 1. EMITTER 2
- PIN 2. BASE 2
- PIN 3. COLLECTOR 1
- PIN 4. EMITTER 1
- PIN 5. BASE 1
- PIN 6. COLLECTOR 2

#### STYLE 6:

- PIN 1. COLLECTOR
- PIN 2. COLLECTOR
- PIN 3. BASE
- PIN 4. EMITTER
- PIN 5. COLLECTOR
- PIN 6. COLLECTOR

#### STYLE 7:

- PIN 1. COLLECTOR
- PIN 2. COLLECTOR
- PIN 3. BASE
- PIN 4. N/C
- PIN 5. COLLECTOR
- PIN 6. EMITTER

#### STYLE 8:

- PIN 1. Vbus
- PIN 2. D(in)
- PIN 3. D(in)+
- PIN 4. D(out)+
- PIN 5. D(out)
- PIN 6. GND

#### STYLE 9:

- PIN 1. LOW VOLTAGE GATE
- PIN 2. DRAIN
- PIN 3. SOURCE
- PIN 4. DRAIN
- PIN 5. DRAIN
- PIN 6. HIGH VOLTAGE GATE

#### STYLE 10:

- PIN 1. D(OUT)+
- PIN 2. GND
- PIN 3. D(OUT)-
- PIN 4. D(IN)-
- PIN 5. VBUS
- PIN 6. D(IN)+

#### STYLE 11:

- PIN 1. SOURCE 1
- PIN 2. DRAIN 2
- PIN 3. DRAIN 2
- PIN 4. SOURCE 2
- PIN 5. GATE 1
- PIN 6. DRAIN 1/GATE 2

#### STYLE 12:

- PIN 1. I/O
- PIN 2. GROUND
- PIN 3. I/O
- PIN 4. I/O
- PIN 5. VCC
- PIN 6. I/O

#### STYLE 13:

- PIN 1. GATE 1
- PIN 2. SOURCE 2
- PIN 3. GATE 2
- PIN 4. DRAIN 2
- PIN 5. SOURCE 1
- PIN 6. DRAIN 1

#### STYLE 14:

- PIN 1. ANODE
- PIN 2. SOURCE
- PIN 3. GATE
- PIN 4. CATHODE/DRAIN
- PIN 5. CATHODE/DRAIN
- PIN 6. CATHODE/DRAIN

#### STYLE 15:

- PIN 1. ANODE
- PIN 2. SOURCE
- PIN 3. GATE
- PIN 4. DRAIN
- PIN 5. N/C
- PIN 6. CATHODE

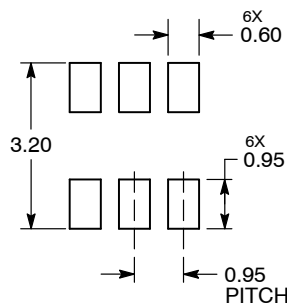
#### STYLE 16:

- PIN 1. ANODE/CATHODE
- PIN 2. BASE
- PIN 3. EMITTER
- PIN 4. COLLECTOR
- PIN 5. ANODE
- PIN 6. CATHODE

#### STYLE 17:

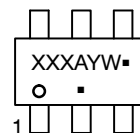
- PIN 1. EMITTER
- PIN 2. BASE
- PIN 3. ANODE/CATHODE
- PIN 4. ANODE
- PIN 5. CATHODE
- PIN 6. COLLECTOR

### RECOMMENDED SOLDERING FOOTPRINT\*

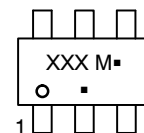


DIMENSIONS: MILLIMETERS

### GENERIC MARKING DIAGRAM\*



IC



STANDARD

XXX = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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DESCRIPTION:	TSOP-6	PAGE 1 OF 1

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