High-speed transceiver family with optimal signal integrity

Stratix II GX FPGAs

Transceiver technology leadership—today and tomorrow

To maximize design resources while meeting time-to-market goals for your high-bandwidth serial communication applications, look to Altera's Stratix® II GX FPGAs. As the industry's only viable transceiver-based production solution for 3.75-Gbps to 6.375-Gbps data rates, Stratix II GX devices are based on the Stratix II GX FPGA's excellent jitter performance, the award-winning Stratix II architecture, and the industry's easiest-to-use design environment, Quartus® II software.

Stratix II GX FPGAs integrate up to 20 serializer/deserializer (SERDES)-based transceivers. The transceivers can drive backplane channels with 50 inches of FR-4 at 6.375 Gbps and are interoperable with backplanes and transceivers from multiple vendors. What's more, the FPGAs are part of a complete serial protocol solution portfolio that also includes intellectual property (IP) cores, development boards, reference designs, and evaluation tools from Altera and Altera's partners.

At a glance

Stratix II GX FPGAs are the only production FPGAs to support 6-Gbps transceiver data rates

- Complete protocol portfolio including transceivers plus IP cores, system models, reference designs, signal integrity tools, and complete documentation
- Plug & Play Signal Integrity technology for designing universal cards for backplane systems
- Dynamic reconfiguration of Stratix II GX transceivers for application flexibility
- I/O signal integrity enhancements: transceiver I/Os, source synchronous I/Os, high-speed memory interfaces

Wide-ranging protocol support

Stratix II GX FPGAs feature built-in physical coding sublayer (PCS) blocks that make designing for a variety of popular protocol standards easier than ever. Basic modes (3G and 6G) provide maximum flexibility in using selected PCS blocks or completely bypassing these blocks. Currently, Stratix II GX FPGAs support PCI Express 2.0 at 5 Gbps, as well as these protocols above 3 Gbps:

- OIF CEI-6G
- Fibre Channel FC-4
- SerialLite II
- Interlaken
- XAUI+

Stratix II GX transceiver protocol support

Protocol		Data rate	Stratix II GX FPGA	Stratix GX FPGA
Protocols up to 6.375 Gbps	PCI Express 2.0	5 Gbps	✔	
	OIF CEI-6G	Up to 6.375 Gbps	✔	
	Fibre Channel FC-4	4.25 Gbps	✔	
	SerialLite II	Up to 6.375 Gbps	✔	
	6G Basic	Up to 6.375 Gbps	✔	
	Interlaken	3.125 to 6.375 Gbps	✔	
	XAUI+	3.75 Gbps	✔	
Protocols up to 3.2 Gbps	PCI Express 1.1	2.5 Gbps	✔	✔
	XAUI	3.125 Gbps	✔	✔
	Serial RapidIO®	1.25, 2.5, 3.125 Gbps	✔	✔
	Gigabit Ethernet	1.25 Gbps	✔	✔
	CPRI	0.614, 1.228, 2.4576 Gbps	✔	
	OBSAI	0.768, 1.536 Gbps	✔	
	Fibre Channel FC-2, FC-1	1.0625, 2.125 Gbps	✔	✔
	GPON	1.24416 Gbps	✔	
	SFI-5	2.7 Gbps	✔	
	SONET OC-12, OC-48	0.622, 2.488 Gbps	✔	
	SDI 3G	3 Gbps	✔	
	SDI SD, HD	0.27, 1.5 Gbps	✔	✔
	SerialLite II	Up to 3.2 Gbps	✔	✔
	3G Basic	Up to 3.2 Gbps	✔	✔

Stratix II GX FPGAs are marked by several distinct capabilities: Plug & Play Signal Integrity, dynamic reconfiguration, and Altera's best-in-class signal integrity. Read on for more details.

Plug & Play Signal Integrity

Altera's hot-socketable transceivers, coupled with adaptive dispersion compensation engine (ADCE) technology, deliver Plug & Play Signal Integrity.

- Allows the design of backplane systems with truly universal cards that can fit into multiple card positions (same card configuration regardless of slot position)
- Flexibility for a wide range of FPGA applications and configurations
- ADCE monitors and adjusts the receiver equalizer for the best eye opening
- Results in very low bit error ratio (BER) operation
- Continuously compensates for environmental variations: humidity, temperature, and aging
- Continuously compensates for manufacturing variations: voltage, materials, and silicon process
- Benefits include reduced card-type inventories, increased system flexibility, reduced maintenance and training costs
- Reduces lab characterization effort and time in determining the best signal integrity settings for each card

Dynamic reconfiguration

Dynamic reconfiguration of the Stratix II GX transceivers allows users to dynamically modify the functionality of each transceiver channel while the transceivers are still operating.

- Transceivers can reconfigure the data-path for different protocols
- Data rates can be dynamically increased or decreased
- Signal integrity settings are optimized for protocol or data rate changes
- Transmit pre-emphasis levels, receive equalization levels, DC gain, and voltage output differential (V_{OD}) settings can be dynamically changed
- Operation of adjacent channels are not interrupted during dynamic reconfiguration

Signal integrity

Stratix II GX FPGAs feature signal integrity enhancements in transceiver I/Os, FPGA I/Os, and package design.

- Transceiver pre-emphasis, equalization, and V_{OD} are all dynamically programmable in Stratix II GX FPGAs
- Dynamic phase alignment (DPA) is used on the source synchronous I/Os
- Enhanced simultaneous switching noise (SSN) support includes increased power/ground pin ratios and enhanced package designs for high-speed I/O performance

Pre-emphasis and equalization link estimator (PELE)

- Altera's PELE saves time in determining settings for optimal link performance
- PELE is now part of the Mentor Graphics Stratix II GX design kit

Want to dig deeper?

For more information about Stratix II GX FPGAs, contact your local Altera FAE or visit **www.altera.com/stratix2gx**.

Stratix II GX device family overview

Feature	EP2SGX30C	EP2SGX30D	EP2SGX60C	EP2SGX60D	EP2SGX60E	EP2SGX90E	EP2SGX90F	EP2SGX130G
Equivalent LEs	33,880	33,880	60,440	60,440	60,440	90,960	90,960	132,540
Total RAM (Kbits)*	1,338	1,338	2,485	2,485	2,485	4,415	4,415	6,590
M512 RAM blocks	202	202	329	329	329	488	488	699
M4K RAM blocks	144	144	255	255	255	408	408	609
M-RAM blocks	1	1	2	2	2	4	4	6
18x18/9x9 embedded multipliers	64/128	64/128	144/288	144/288	144/288	192/384	192/384	252/504
Global and regional clock networks	48	48	48	48	48	48	48	48
PLLs/unique outputs	4/18	4/18	4/18	4/18	8/36	8/36	8/36	8/36
Transceiver channels	4	8	4	8	12	12	16	20
Package (FBGA)	780-pin	780-pin	780-pin	780-pin	1,152-pin	1,152-pin	1,508-pin	1,508-pin

*1 Kbit = 1,024 bits

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