93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C

8-Kbit Microwire-Compatible Serial EEPROM

Device Selection Table

Part Number	Vcc Range	ORG Pin	PE Pin	Word Size	Temp. Ranges	Packages
93AA76A	1.8V-5.5V	No	No	8-bit	I	MS, P, SN, OT, ST
93AA76B	1.8V-5.5V	No	No	16-bit	I	MS, P, SN, OT, ST
93LC76A	2.5V-5.5V	No	No	8-bit	I, E	MS, P, SN, OT, ST
93LC76B	2.5V-5.5V	No	No	16-bit	I, E	MS, P, SN, OT, ST
93C76A	4.5V-5.5V	No	No	8-bit	I, E	MS, P, SN, OT, ST
93C76B	4.5V-5.5V	No	No	16-bit	I, E	MS, P, SN, OT, ST
93AA76C	1.8V-5.5V	Yes	Yes	8-bit or 16-bit	I	MC, MS, P, SN, MN, ST
93LC76C	2.5V-5.5V	Yes	Yes	8-bit or 16-bit	I, E	MC, MS, P, SN, MN, ST, MWF
93C76C	4.5V-5.5V	Yes	Yes	8-bit or 16-bit	I, E	MC, MS, P, SN, MN, ST

Features

- Low-Power CMOS Technology
- ORG Pin to Select Word Size for '76C' Version
- 1024 x 8-bit Organization 'A' Devices (no ORG)
- 512 x 16-bit Organization 'B' Devices (no ORG)
- Program Enable Pin to Write-Protect the Entire Array ('76C' version only)
- Self-Timed Erase/Write Cycles (including Auto-Erase)
- Automatic Erase All (ERAL) Before Write All (WRAL)
- Power-On/Off Data Protection Circuitry
- Industry Standard Three-Wire Serial I/O
- Device Status Signal (Ready/$\overline{\text{Busy}}$)
- Sequential Read Function
- High Reliability:
  - Endurance: 1,000,000 erase/write cycles
  - Data retention > 200 years
  - ESD protection: > 4,000V
- RoHS Compliant
- Temperature Ranges Supported:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C
- AEC-Q100 Automotive Qualified

Packages

- 8-Lead DFN, 8-Lead MSOP, 8-Lead PDIP, 8-Lead SOIC, 6-Lead SOT-23, 8-Lead TDFN, 8-Lead TSSOP and 8-Lead Wettable Flank VDFN

Pin Function Table

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VSS	Ground
PE	Program Enable – 93XX76C only
ORG	Memory Configuration – 93XX76C only
VCC	Power Supply

Description

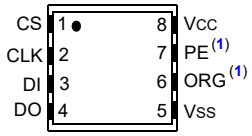
The Microchip Technology Inc. 93XX76A/B/C devices are 8-Kbit, low-voltage, serial Electrically Erasable PROMs (EEPROMs). Word-selectable devices such as the 93XX76C are dependent upon external logic levels driving the ORG pin to set word size. The 93XX76A devices provide dedicated 8-bit memory organization, while the 93XX76B devices provide dedicated 16-bit memory organization. A Program Enable (PE) pin allows the user to write-protect the entire memory array. Advanced CMOS technology makes these devices ideal for low-power, nonvolatile memory applications.

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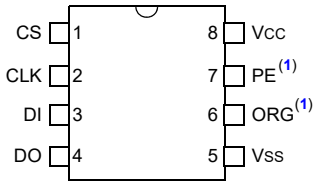
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Package Types (not to scale)

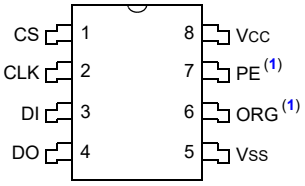
DFN/TDFN/VDFN
(Top View)



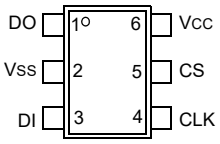
MSOP/TSSOP
(Top View)



PDIP/SOIC
(Top View)



SOT-23
(Top View)



Note 1: 93XX76C only

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....7.0V

All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Electrical Characteristics: Industrial (I): TA = -40°C to +85°C, VCC = +1.8V to 5.5V Extended (E): TA = -40°C to +125°C, VCC = +2.5V to 5.5V				
Param. No.	**Symbol**	**Parameter**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
D1	VIH1	High-Level Input Voltage	2.0	—	VCC +1	V	VCC ≥ 2.7V
	VIH2		0.7 VCC	—	VCC +1	V	VCC < 2.7V
D2	VIL1	Low-Level Input Voltage	-0.3	—	0.8	V	VCC ≥ 2.7V
	VIL2		-0.3	—	0.2 VCC	V	VCC < 2.7V
D3	VOL1	Low-Level Output Voltage	—	—	0.4	V	IOL = 2.1 mA, VCC = 4.5V
	VOL2		—	—	0.2	V	IOL = 100 µA, VCC = 2.5V
D4	VOH1	High-Level Output Voltage	2.4	—	—	V	IOH = -400 µA, VCC = 4.5V
	VOH2		- 0.2 VCC	—	—	V	IOH = -100 µA, VCC = 2.5V
D5	ILI	Input Leakage Current	—	—	±1	µA	VIN = VSS or VCC
D6	ILO	Output Leakage Current	—	—	±1	µA	VOUT = VSS or VCC
D7	CIN, COUT	Pin Capacitance (all inputs/outputs)	—	—	7	pF	VIN/VOUT = 0V (**Note 1**) TA = 25°C, FCLK = 1 MHz
D8	ICCWRITE	Write Current	—	—	3	mA	FCLK = 3 MHz, VCC = 5.5V
			—	500	—	µA	FCLK = 2 MHz, VCC = 2.5V
D9	ICCREAD	Read Current	—	—	1	mA	FCLK = 3 MHz, VCC = 5.5V
			—	—	500	µA	FCLK = 2 MHz, VCC = 3.0V
			—	100	—	µA	FCLK = 2 MHz, VCC = 2.5V
D10	ICCS	Standby Current	—	—	1	µA	I-Temp, CS = 0V ORG = DI = PE = VSS or VCC (**Note 2**, **Note 3**)
			—	—	5	µA	E-Temp, CS = 0V ORG = DI = PE = VSS or VCC (**Note 2**, **Note 3**)
D11	VPOR	VCC Voltage Detect	—	1.5	—	V	93AA76A/B/C, 93LC76A/B/C (**Note 1**)
			—	3.8	—	V	93C76A/B/C (**Note 1**)

Note 1: This parameter is periodically sampled and not 100% tested.

2: ORG and PE pins not available on ‘A’ or ‘B’ versions.

3: Ready/$\overline{\text{Busy}}$ status must be cleared from DO; see **Section 3.4 “Data Out (DO)”**.

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TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): TA = -40°C to +85°C, VCC = +1.8V to 5.5V Extended (E): TA = -40°C to +125°C, VCC = +2.5V to 5.5V			
Param. No.	**Symbol**	**Parameter**	**Min.**	**Max.**	**Units**	**Conditions**
A1	FCLK	Clock Frequency	—	3	MHz	4.5V ≤ VCC < 5.5V
			—	2	MHz	2.5V ≤ VCC < 4.5V
			—	1	MHz	1.8V ≤ VCC < 2.5V
A2	TCKH	Clock High Time	200	—	ns	4.5V ≤ VCC < 5.5V
			250	—	ns	2.5V ≤ VCC < 4.5V
			450	—	ns	1.8V ≤ VCC < 2.5V
A3	TCKL	Clock Low Time	100	—	ns	4.5V ≤ VCC < 5.5V
			200	—	ns	2.5V ≤ VCC < 4.5V
			450	—	ns	1.8V ≤ VCC < 2.5V
A4	TCSS	Chip Select Setup Time	50	—	ns	4.5V ≤ VCC < 5.5V
			100	—	ns	2.5V ≤ VCC < 4.5V
			250	—	ns	1.8V ≤ VCC < 2.5V
A5	TCSH	Chip Select Hold Time	0	—	ns	1.8V ≤ VCC < 5.5V
A6	TCSL	Chip Select Low Time	250	—	ns	1.8V ≤ VCC < 5.5V
A7	TDIS	Data Input Setup Time	50	—	ns	4.5V ≤ VCC < 5.5V
			100	—	ns	2.5V ≤ VCC < 4.5V
			250	—	ns	1.8V ≤ VCC < 2.5V
A8	TDIH	Data Input Hold Time	50	—	ns	4.5V ≤ VCC < 5.5V
			100	—	ns	2.5V ≤ VCC < 4.5V
			250	—	ns	1.8V ≤ VCC < 2.5V
A9	TPD	Data Output Delay Time	—	100	ns	4.5V ≤ VCC < 5.5V, CL = 100 pF
			—	250	ns	2.5V ≤ VCC < 4.5V, CL = 100 pF
			—	400	ns	1.8V ≤ VCC < 2.5V, CL = 100 pF
A10	TCZ	Data Output Disable Time	—	100	ns	4.5V ≤ VCC < 5.5V (**Note 1**)
			—	200	ns	1.8V ≤ VCC < 4.5V (**Note 1**)
A11	TSV	Status Valid Time	—	200	ns	4.5V ≤ VCC < 5.5V, CL = 100 pF
			—	300	ns	2.5V ≤ VCC < 4.5V, CL = 100 pF
			—	500	ns	1.8V ≤ VCC < 2.5V, CL = 100 pF
A12	TWC	Program Cycle Time	—	5	ms	Erase/Write mode (AA and LC versions)
A13	TWC		—	2	ms	Erase/Write mode (93C versions)
A14	TEC		—	6	ms	ERAL mode, 4.5V ≤ VCC ≤ 5.5V
A15	TWL		—	15	ms	WRAL mode, 4.5V ≤ VCC ≤ 5.5V
A16	—	Endurance	1,000,000	—	cycles	+25°C, VCC = 5.0V (**Note 2**)

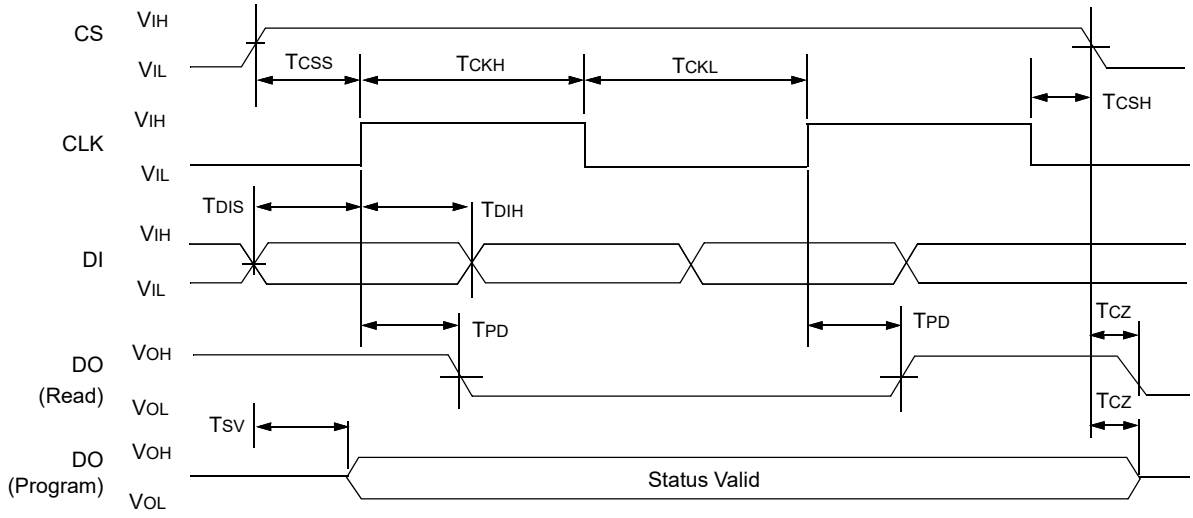
Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but ensured by characterization.

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FIGURE 1-1: SYNCHRONOUS DATA TIMING



Note: TSV is relative to CS.

TABLE 1-3: INSTRUCTION SET FOR X16 ORGANIZATION (93XX76B OR 93XX76C WITH ORG = 1)

Instruction	SB	Opcode	Address										Data In	Data Out	Req. CLK Cycles
READ	1	10	X	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D15-D0	29
EWEN	1	00	1	1	x	x	x	x	x	x	x	x	—	High-Z	13
ERASE	1	11	X	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	13
ERAL	1	00	1	0	X	X	X	X	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	13
WRITE	1	01	X	A8	A7	A6	A5	A4	A3	A2	A1	A0	D15-D0	(RDY/$\overline{\text{BSY}}$)	29
WRAL	1	00	0	1	x	x	x	x	x	x	x	x	D15-D0	(RDY/$\overline{\text{BSY}}$)	29
EWDS	1	00	0	0	x	x	x	x	x	x	x	x	—	High-Z	13

TABLE 1-4: INSTRUCTION SET FOR X8 ORGANIZATION (93XX76A OR 93XX76C WITH ORG = 0)

Instruction	SB	Opcode	Address										Data In	Data Out	Req. CLK Cycles
READ	1	10	X	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D7-D0	22
EWEN	1	00	1	1	x	x	x	x	x	x	x	x	x	—	High-Z	14
ERASE	1	11	X	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	14
ERAL	1	00	1	0	x	x	x	x	x	x	x	x	x	—	(RDY/$\overline{\text{BSY}}$)	14
WRITE	1	01	X	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	D7-D0	(RDY/$\overline{\text{BSY}}$)	22
WRAL	1	00	0	1	x	x	x	x	x	x	x	x	x	D7-D0	(RDY/$\overline{\text{BSY}}$)	22
EWDS	1	00	0	0	x	x	x	x	x	x	x	x	x	—	High-Z	14

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2.0 FUNCTIONAL DESCRIPTION

When the ORG pin (93XX76C) is connected to VCC, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a High-Z state except when reading data from the device or when checking the Ready/Busy status during a programming operation. The Ready/Busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. DO will enter the High-Z state on the falling edge of CS.

2.1 Start Condition

The Start bit is detected by the device when CS and DI are both high on the first rising edge of CLK.

Before a Start condition is detected, CS, CLK and DI may change in any combination (except one that creates a Start condition), without initiating any device operation (Read, Write, Erase, EWEN, EWDS, ERAL or WRAL). As soon as CS goes high, the device exits Standby mode.

An instruction following a Start condition is executed only if the required opcode, address and data bits for any particular instruction are clocked in.

Note:	When preparing to transmit an instruction, either the CLK or DI signal must be at a logic low when CS is toggled active high.

2.2 Data In/Data Out (DI/DO)

The Data In (DI) and Data Out (DO) pins may be connected together. However, in this configuration, a bus conflict may occur during the “dummy zero” that precedes the read operation if A0 is a logic high level. Under these conditions, the voltage level observed at the DO pin is undefined and depends on the relative impedances of the DO pin and the signal source driving A0. The greater the current-sourcing capability of the driver, the higher the voltage at the DO pin. To limit this current, a resistor should be connected between the DI and DO pins.

2.3 Data Protection

All modes of operation are inhibited when VCC is below a typical voltage of 1.5V for ‘93AA’ and ‘93LC’ devices or 3.8V for ‘93C’ devices.

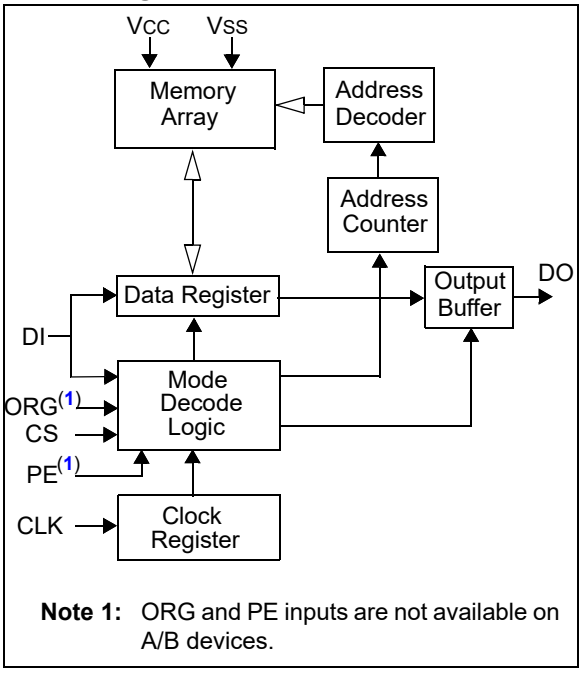
The EWEN and EWDS commands provide additional protection against accidental programming during normal operation.

Note:	For added protection, an EWDS command should be issued after every write operation, and an external 10 kΩ pull-down protection resistor should be added to the CS pin.

After power-up, the device automatically enters EWDS mode. Therefore, an EWEN instruction must be executed before the initial ERASE or WRITE instruction can be performed.

Note:	To prevent accidental writes to the array in the 93XX76C devices, set the PE pin to a logic low.

Block Diagram



Note 1: ORG and PE inputs are not available on A/B devices.

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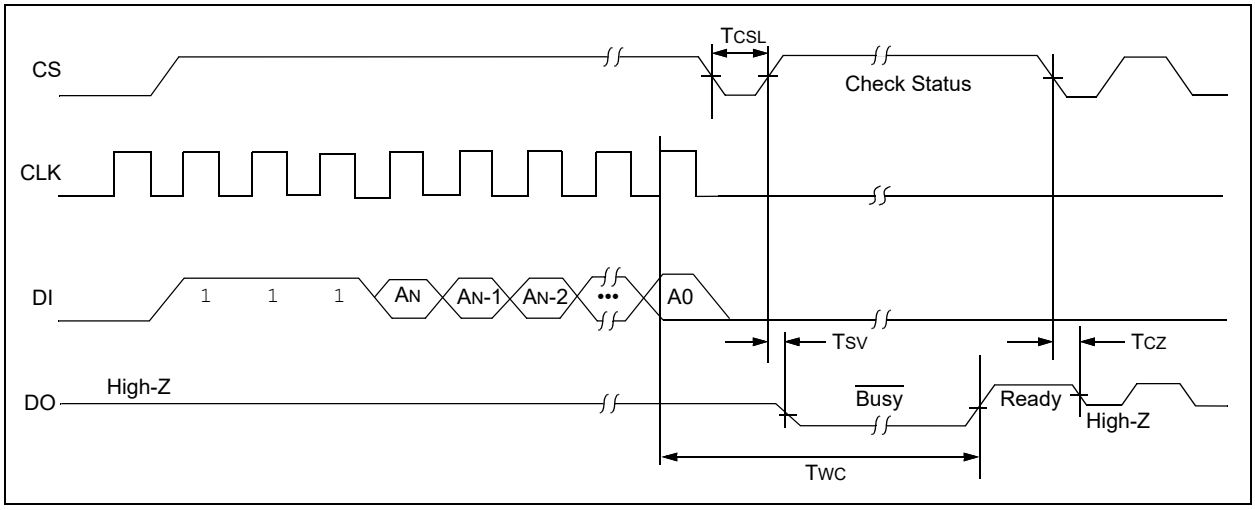
2.4 Erase

The ERASE instruction forces all data bits at the specified address to the logical '1' state. The rising edge of CLK before the last address bit initiates the write cycle.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device if CS is brought high after being held low for a minimum of 250 ns (T_{CSL}). A logical '0' on DO indicates that programming is still in progress, while a logical '1' indicates that the register at the specified address has been erased and the device is ready for another instruction.

Note:	After the Erase cycle is complete, issuing a Start bit and then driving CS low clears the Ready/$\overline{\text{Busy}}$ status on the DO pin.

FIGURE 2-1: ERASE TIMING



2.5 Erase All (ERAL)

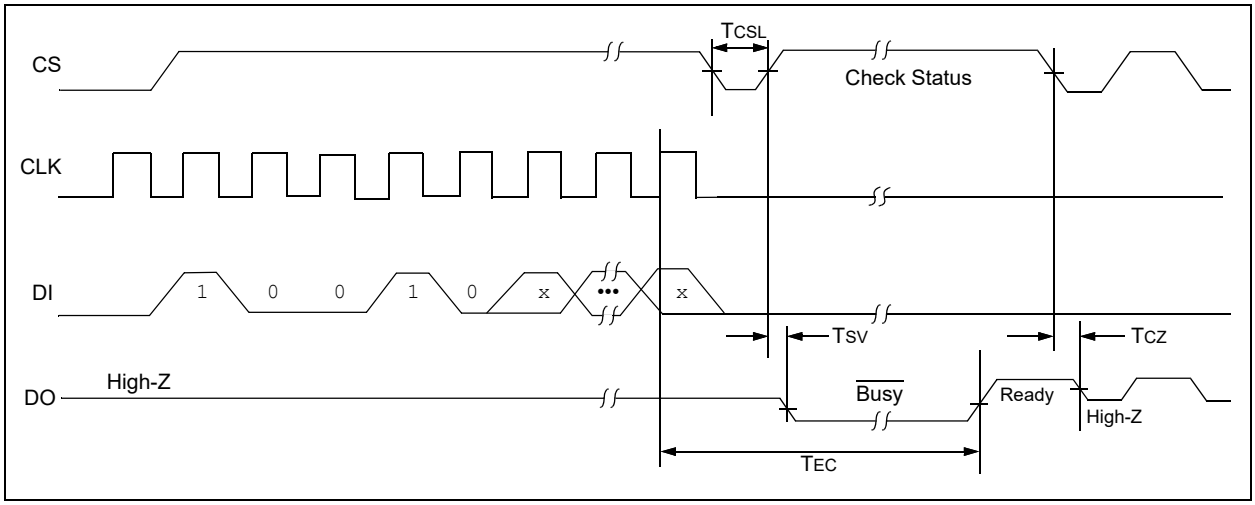
The Erase All (ERAL) instruction erases the entire memory array to the logical '1' state. The ERAL cycle is identical to the erase cycle except for the different opcode. The ERAL cycle is completely self-timed. The rising edge of CLK before the last data bit initiates the write cycle. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device if CS is brought high after being held low for a minimum of 250 ns (T_{CSL}).

Note:	After the ERAL command is complete, issuing a Start bit and then driving CS low clears the Ready/$\overline{\text{Busy}}$ status on the DO pin.

V_{CC} must be ≥ 4.5V for proper ERAL operation.

FIGURE 2-2: ERAL TIMING



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2.6 Erase/Write Disable and Enable (EWDS/EWEN)

The 93XX76A/B/C powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction.

Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or VCC is removed from the device.

To protect against accidental data disturbance, the EWDS instruction can be used to disable all erase/write functions and should be issued after all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

FIGURE 2-3: EWDS TIMING

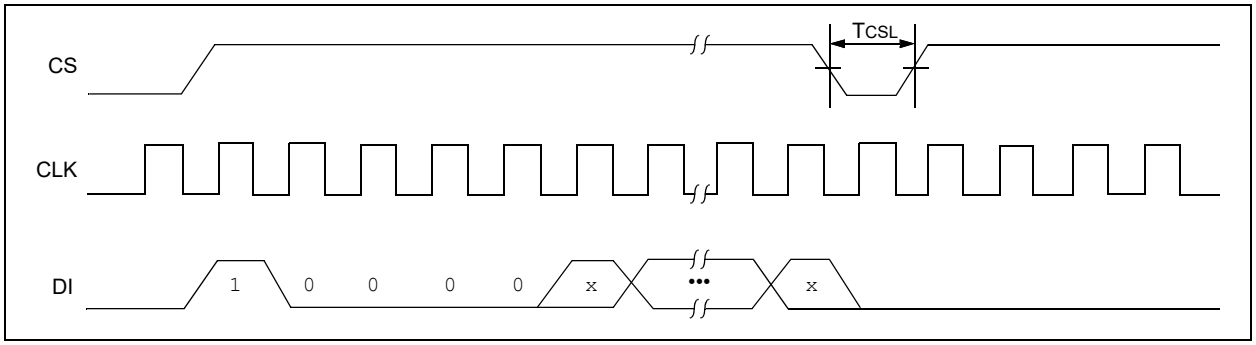
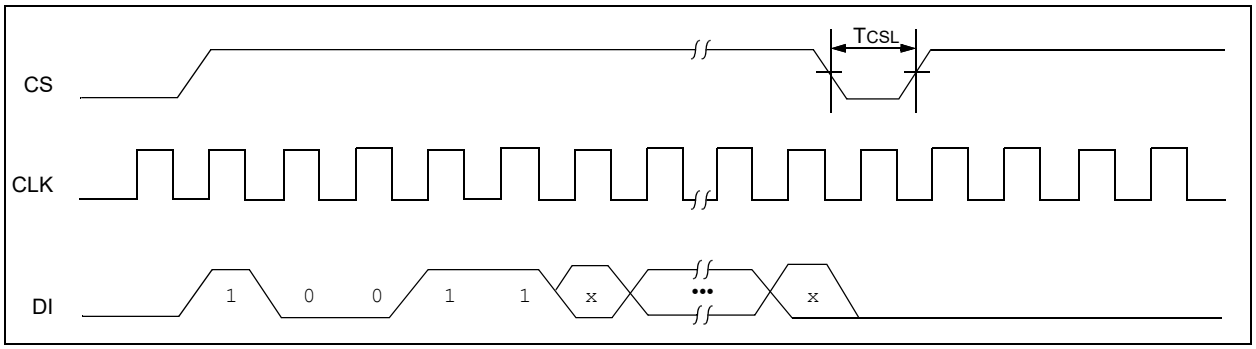


FIGURE 2-4: EWEN TIMING



2.7 Read

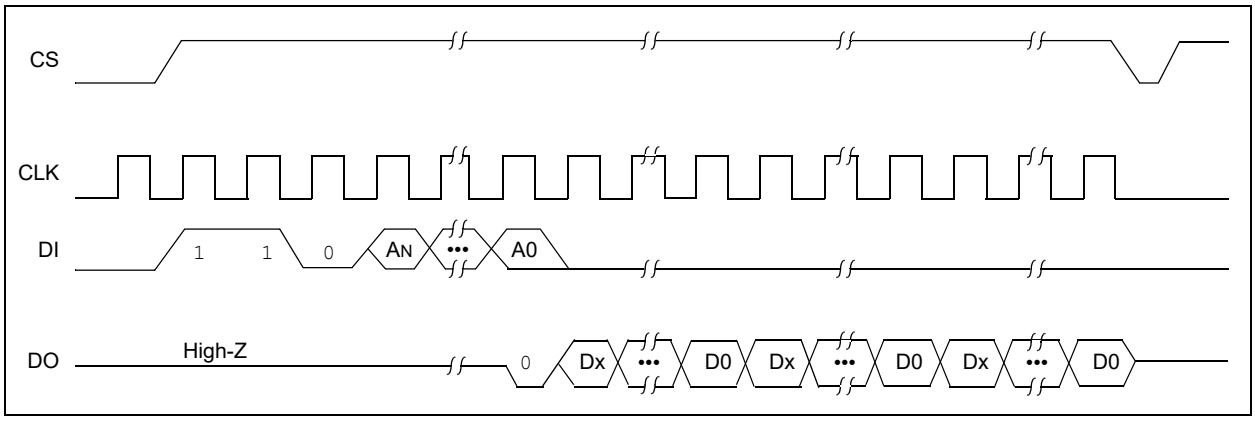
The READ instruction outputs the serial data from the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit output string (when the ORG pin is low or for A-version devices) or the 16-bit output string (when the ORG pin is high or for B-version devices).

The output data bits toggle on the rising edge of CLK and become stable after the specified time delay (TPD). Sequential reading is possible when CS is held high. The memory data automatically advances to the next register and is output sequentially.

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FIGURE 2-5: READ TIMING



2.8 Write

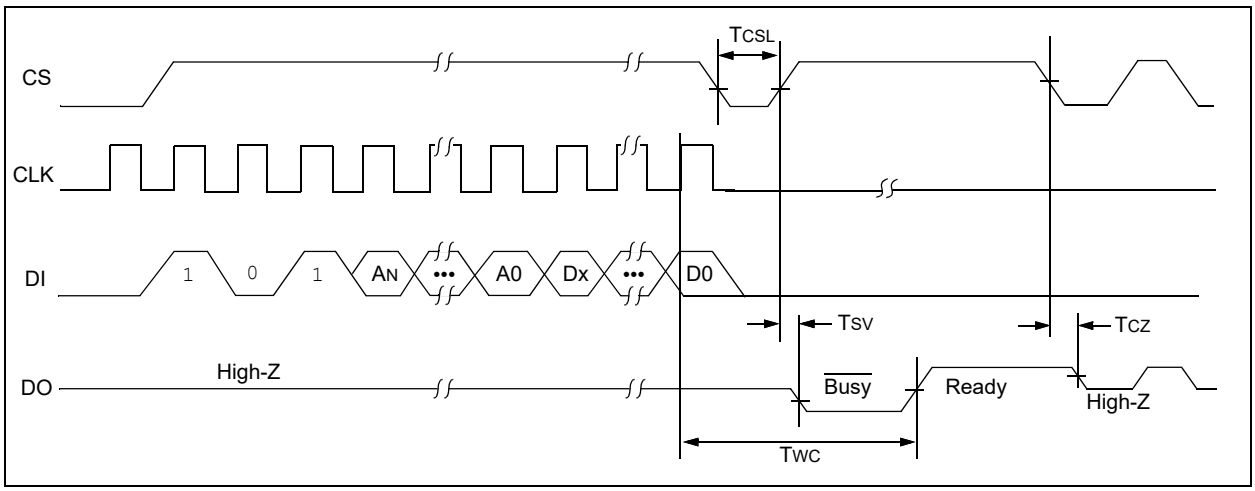
The WRITE instruction is followed by 8 bits of data (when the ORG pin is low or for A-version devices) or 16 bits of data (when the ORG pin is high or for B-version devices), which are written to the specified address. The self-timed auto-erase and programming cycle is initiated on the rising edge of CLK on the last data bit.

The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device if CS is brought high after being held low for a minimum of 250 ns (T_{CSL}). A logical '0' on DO indicates that programming is still in progress, while a logical '1' indicates that the register at the specified address has been written with the data specified and that the device is ready for another instruction.

Note:	The write sequence requires a logic high signal on the PE pin prior to the rising edge of the last data bit.

Note:	After the Write cycle is complete, issuing a Start bit and then driving CS low clears the Ready/$\overline{\text{Busy}}$ status on the DO pin.

FIGURE 2-6: WRITE TIMING



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2.9 Write All (WRAL)

The Write All (WRAL) instruction writes the entire memory array with the data specified in the command. The self-timed auto-erase and programming cycle is initiated on the rising edge of CLK on the last data bit. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command includes an automatic ERAL cycle for the device, so the WRAL instruction does not require an ERAL instruction. However, the chip must be in the EWEN status.

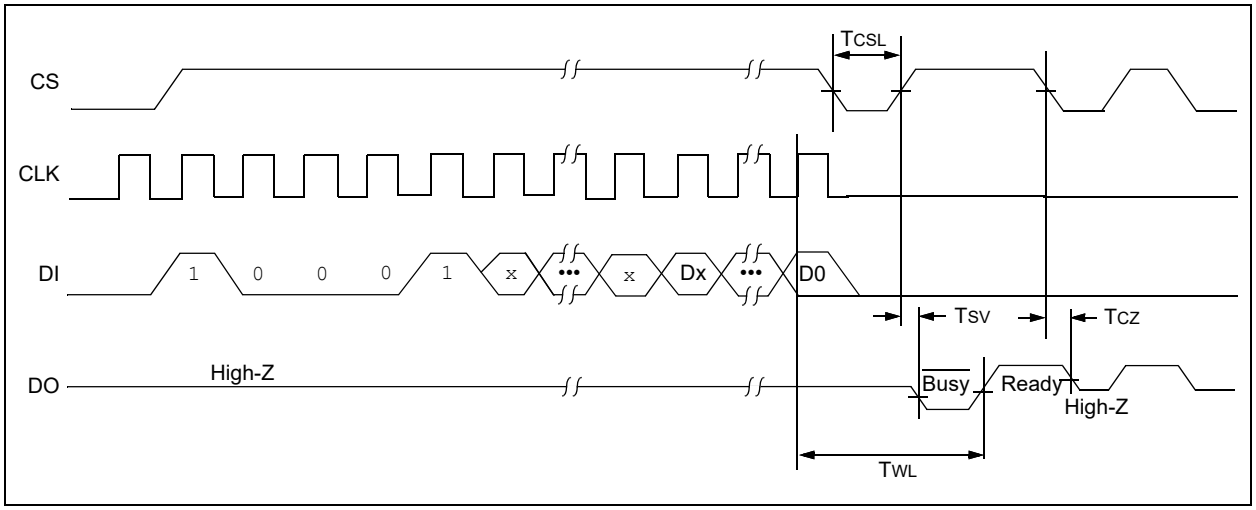
The DO pin indicates the Ready/$\overline{\text{Busy}}$ status of the device if CS is brought high after being held low for a minimum of 250 ns (TCSL).

Note:	The write sequence requires a logic high signal on the PE pin prior to the rising edge of the last data bit.

Note:	After the Write All cycle is complete, issuing a Start bit and then driving CS low clears the Ready/$\overline{\text{Busy}}$ status on the DO pin.

VCC must be ≥ 4.5V for proper WRAL operation.

FIGURE 2-7: WRAL TIMING



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3.0 PIN DESCRIPTIONS

TABLE 3-1: PIN DESCRIPTIONS

Name	DFN(1)	MSOP	PDIP	SOIC	SOT-23	TDFN(1)	TSSOP	VDFN(1)	Function
CS	1	1	1	1	5	1	1	1	Chip Select
CLK	2	2	2	2	4	2	2	2	Serial Clock
DI	3	3	3	3	3	3	3	3	Data In
DO	4	4	4	4	1	4	4	4	Data Out
VSS	5	5	5	5	2	5	5	5	Ground
ORG	6	6	6	6	—	6	6	6	Organization/ 93XX76C only
PE	7	7	7	7	—	7	7	7	Program Enable/ 93XX76C only
VCC	8	8	8	8	6	8	8	8	Power Supply

Note 1: The exposed pad on the DFN/TDFN/VDFN package may be connected to VSS or left floating.

3.1 Chip Select (CS)

A high level on the Chip Select (CS) pin selects the device, while a low level deselects the device and forces it into Standby mode. However, any programming cycle already in progress will be completed regardless of the CS input signal. If CS is driven low during a program cycle, the device enters Standby mode immediately after the programming cycle is completed.

CS must remain low for a minimum of 250 ns (TCSL) between consecutive instructions. When CS is low, the internal control logic is held in a Reset status.

3.2 Serial Clock (CLK)

The Serial Clock (CLK) synchronizes communication between the host device and the 93XX series device. Opcode, address and data bits are clocked into the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped at any point during the transmission sequence (at high or low level) and can resume at any time with respect to Clock High Time (TCKH) and Clock Low Time (TCKL). This allows the controlling host freedom in preparing opcode, address and data.

CLK is a “don’t care” signal when CS is low (device deselected). If CS is high but the Start condition has not been detected (DI = 0), the device may receive any number of clock cycles without changing its status (i.e., waiting for a Start condition).

CLK cycles are not required during the self-timed write cycle (auto erase/write cycle).

After a Start condition is detected, the specified number of clock cycles (low-to-high CLK transitions) must be provided to clock in all required opcode, address and data bits before an instruction is executed. CLK and DI then become “don’t care” inputs until a new Start condition is detected.

3.3 Data In (DI)

The Data In (DI) pin is used to clock in the Start bit, opcode, address and data synchronously with the CLK input.

3.4 Data Out (DO)

The Data Out (DO) pin is used in Read mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides Ready/$\overline{\text{Busy}}$ status information during erase and write cycles. Ready/$\overline{\text{Busy}}$ status information is available on the DO pin when CS is driven high after being held low for at least the minimum Chip Select Low Time (TCSL) and an erase or write operation has been initiated.

The Status signal is not available on the DO pin if CS is held low throughout the entire erase or write cycle. In this case, DO remains in the High-Z state. If the status is checked after the erase/write cycle, the data line will be high, indicating that the device is ready.

Note:	After a programming cycle is complete, issuing a Start bit and then driving CS low clears the Ready/$\overline{\text{Busy}}$ status on the DO pin.

3.5 Organization (ORG)

When the ORG pin is connected to VCC or logic high, the (x16) memory organization is selected. When the ORG pin is tied to VSS or logic low, the (x8) memory organization is selected. For proper operation, the ORG pin must be tied to a valid logic level.

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The 93XX76A devices are permanently configured for (x8) organization, while the 93XX76B devices are permanently configured for (x16) organization.

3.6 Program Enable (PE)

The Program Enable (PE) pin allows the user to enable or disable write access to the memory array. When the PE pin is tied to VCC, the device can be programmed. When the PE pin is tied to VSS, programming is inhibited. The pin cannot be left floating; it must be tied to VCC or VSS. The PE pin is not available on 93XX76A or 93XX76B devices. On those devices, programming is always enabled.

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4.0 PACKAGING INFORMATION

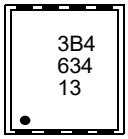
4.1 Package Marking Information

8-Lead 2x3 DFN

(Top View)

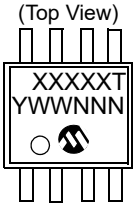


Example



8-Lead MSOP (150 mil)

(Top View)

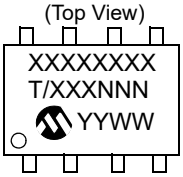


Example

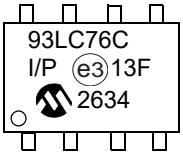


8-Lead PDIP

(Top View)

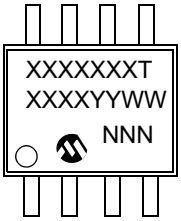


Example

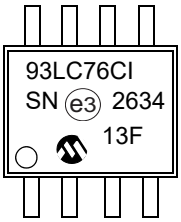


8-Lead SOIC

(Top View)

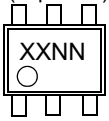


Example

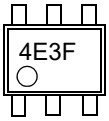


6-Lead SOT-23

(Top View)



Example



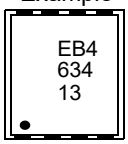
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8-Lead 2x3 TDFN

(Top View)



Example



8-Lead TSSOP

(Top View)



Example



8-Lead 2x3 VDFN

(Top View)



Example



Part Number	1st Line Marking Codes								
	DFN		MSOP	SOT-23		TDFN		TSSOP	VDFN
	I Temp.	E Temp.		I Temp.	E Temp.	I Temp.	E Temp.		E Temp.
93AA76A	—	—	3A76AT	4BNN	—	—	—	A76A	—
93AA76B	—	—	3A76BT	4LNN	—	—	—	A76B	—
93AA76C	3B1	—	3A76CT	—	—	EB1	—	A76C	—
93LC76A	—	—	3L76AT	4ENN	4FNN	—	—	L76A	—
93LC76B	—	—	3L76BT	4PNN	4RNN	—	—	L76B	—
93LC76C	3B4	—	3L76CT	—	—	EB4	EB5	L76C	AAK
93C76A	—	—	3C76AT	4HNN	4JNN	—	—	C76A	—
93C76B	—	—	3C76BT	4TNN	4UNN	—	—	C76B	—
93C76C	3B7	—	3C76CT	—	—	EB7	EB8	C76C	—

Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	RoHS-compliant JEDEC® designator for Matte Tin (Sn)

Note: For very small packages with no room for the RoHS-compliant JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

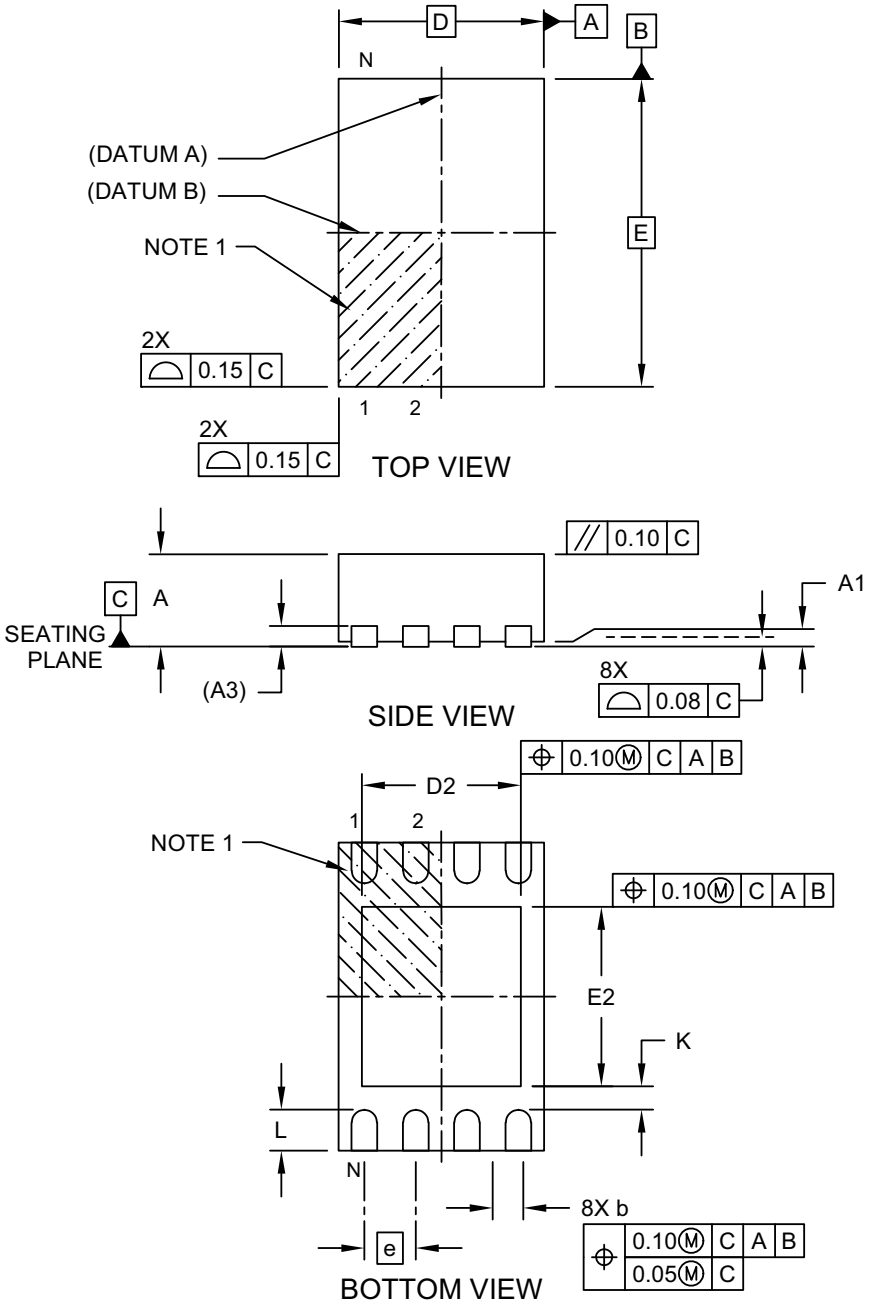
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x1 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

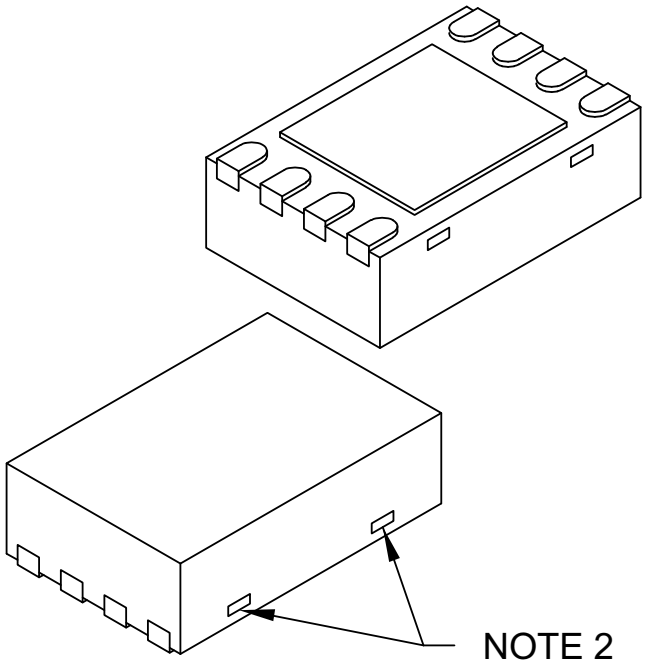


Microchip Technology Drawing C04-123 Rev E Sheet 1 of 2

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8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x1 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.30	-	1.55
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	-	1.75
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

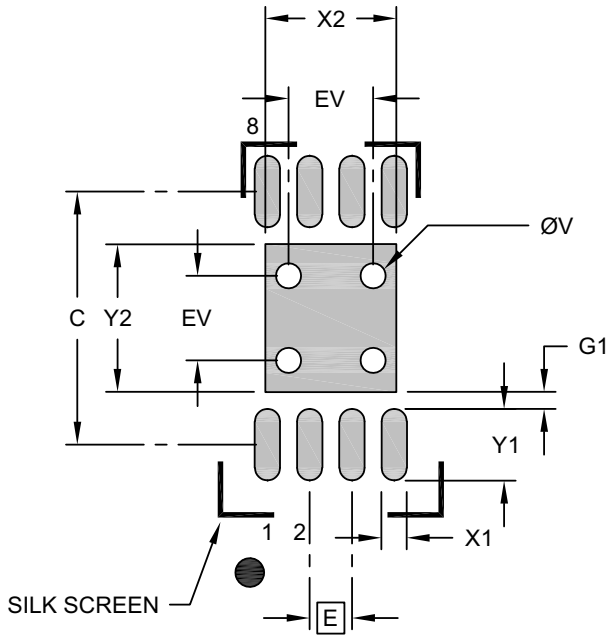
Microchip Technology Drawing C04-123 Rev E Sheet 2 of 2

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8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x1 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.55
Optional Center Pad Length	Y2			1.75
Contact Pad Spacing	C		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

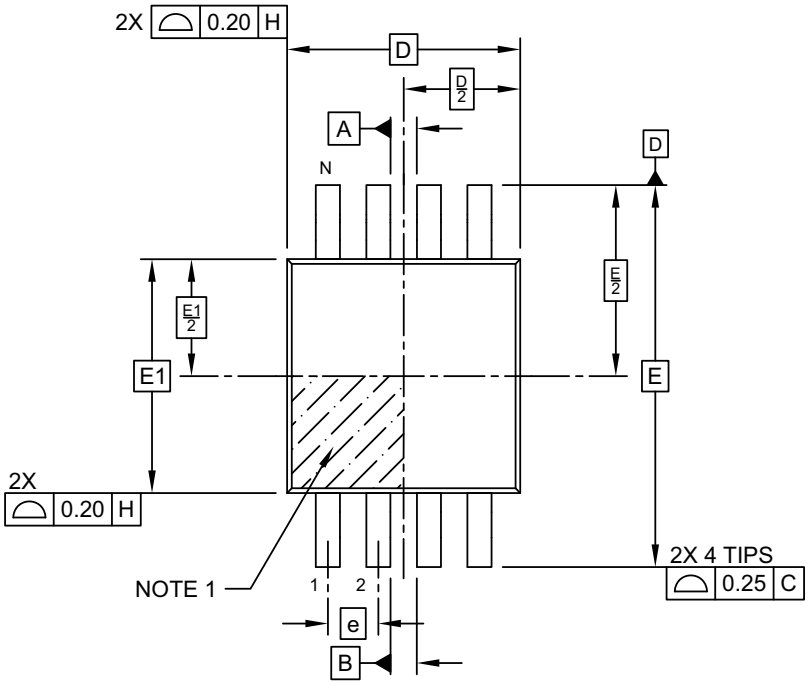
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2123 Rev E

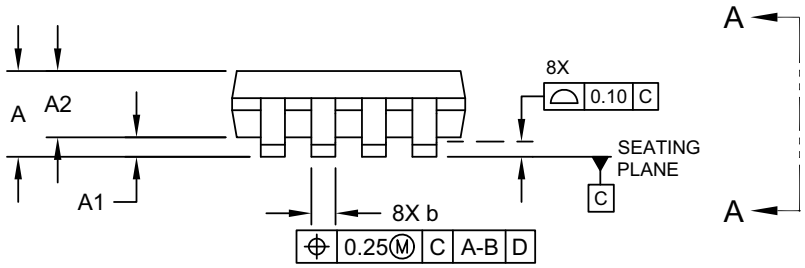
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8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

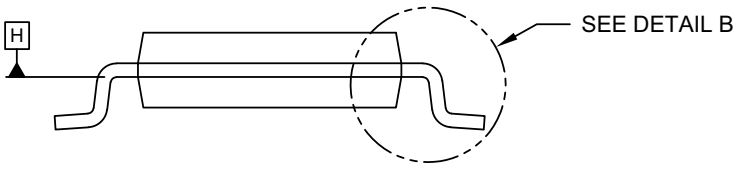
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A–A

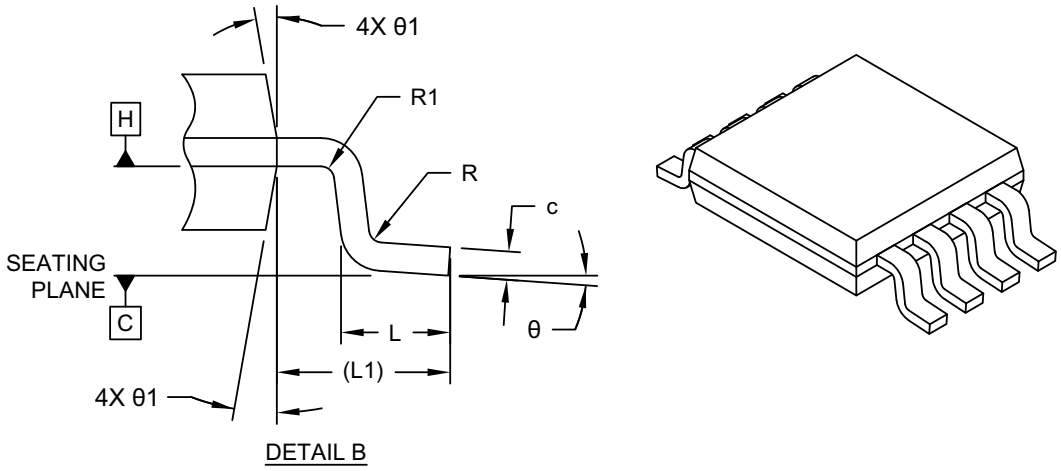
Microchip Technology Drawing C04-111-MS Rev F Sheet 1 of 2

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8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Standoff	A1	0.00	–	0.15
Molded Package Thickness	A2	0.75	0.85	0.95
Overall Length	D		3.00 BSC	
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Terminal Width	b	0.22	–	0.40
Terminal Thickness	c	0.08	–	0.23
Terminal Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

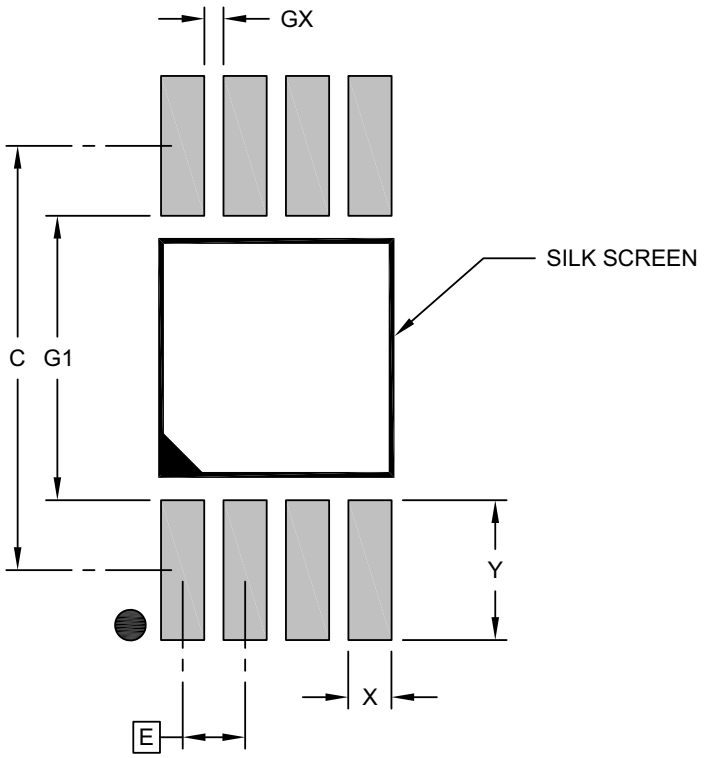
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111-MS Rev F Sheet 2 of 2

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8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Contact Pad Width (X8)	X			0.45
Contact Pad Length (X8)	Y			1.45
Contact Pad to Contact Pad (X4)	G1	2.95		
Contact Pad to Contact Pad (X6)	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

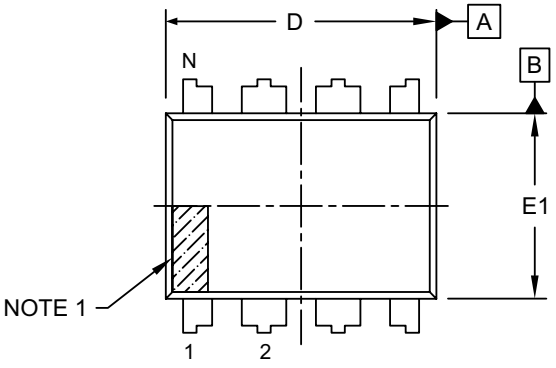
Microchip Technology Drawing C04-2111-MS Rev F

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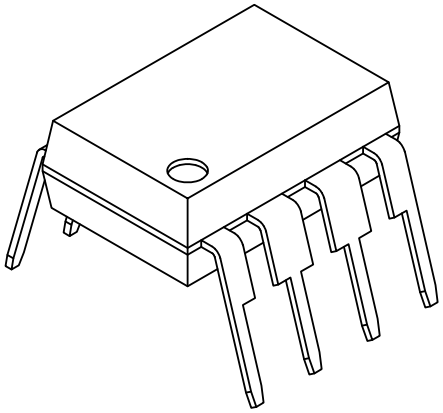
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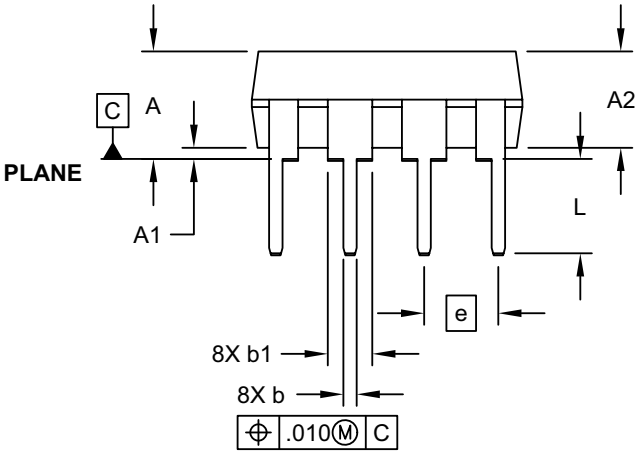
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

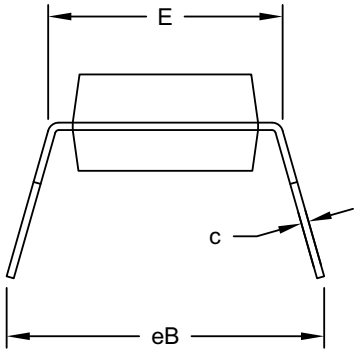


TOP VIEW





SIDE VIEW



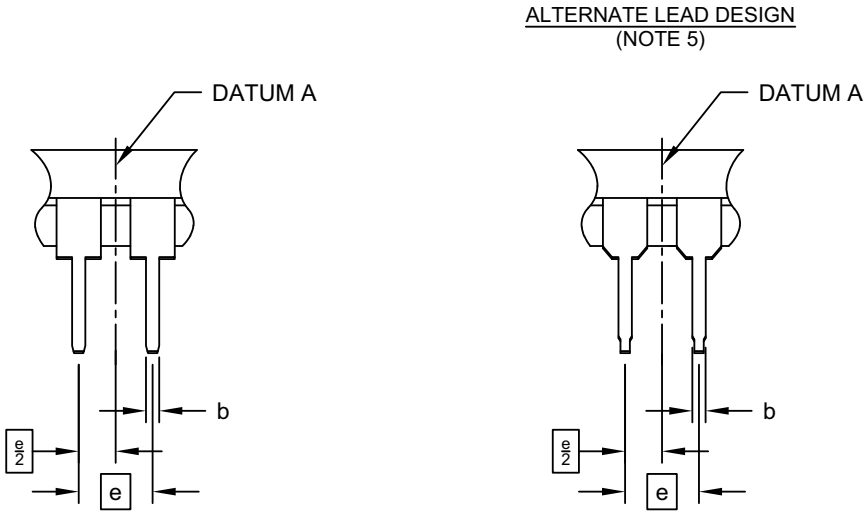
END VIEW

Microchip Technology Drawing No. C04-018-P Rev G Sheet 1 of 2

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8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

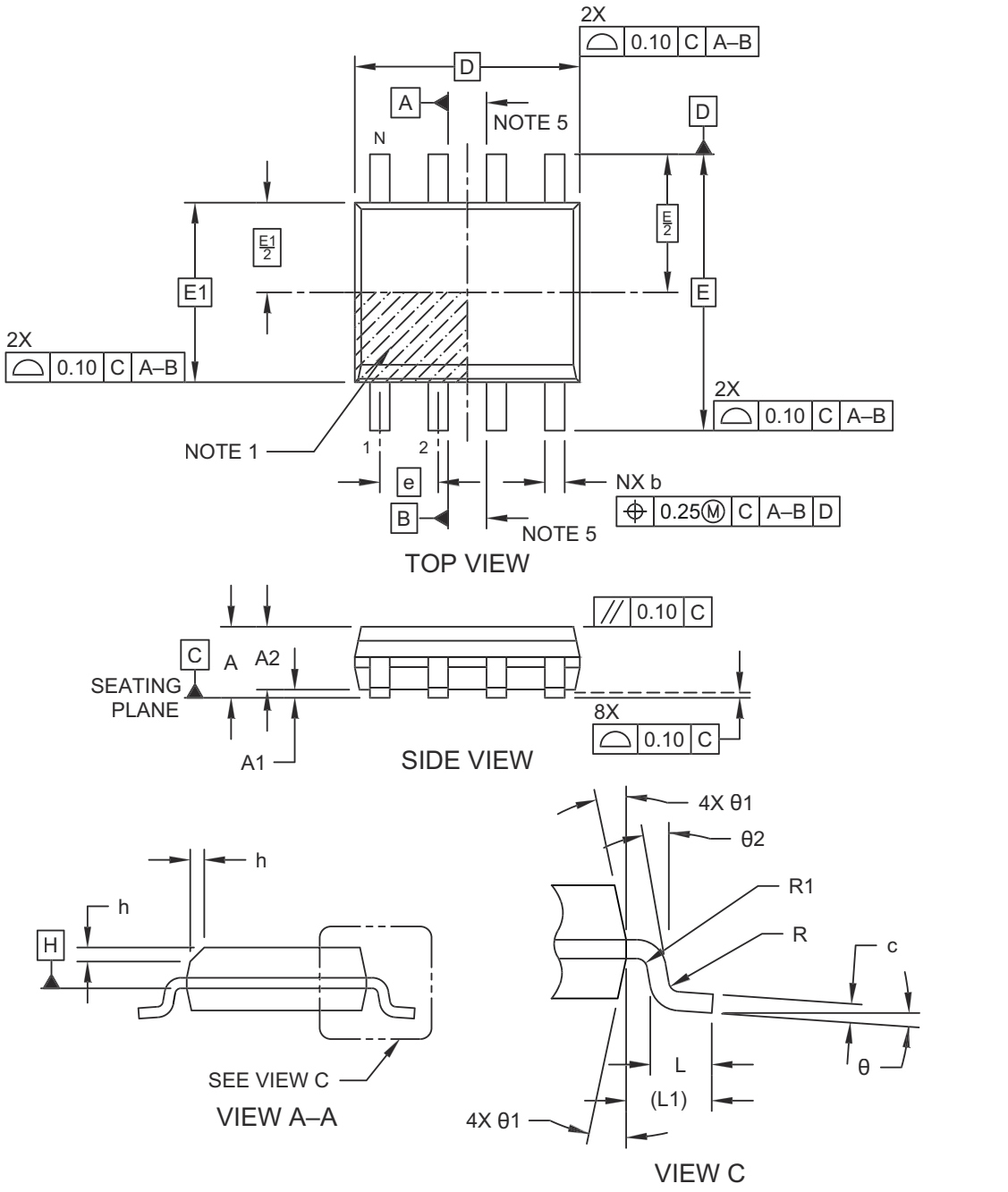
Microchip Technology Drawing No. C04-018-P Rev G Sheet 2 of 2

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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

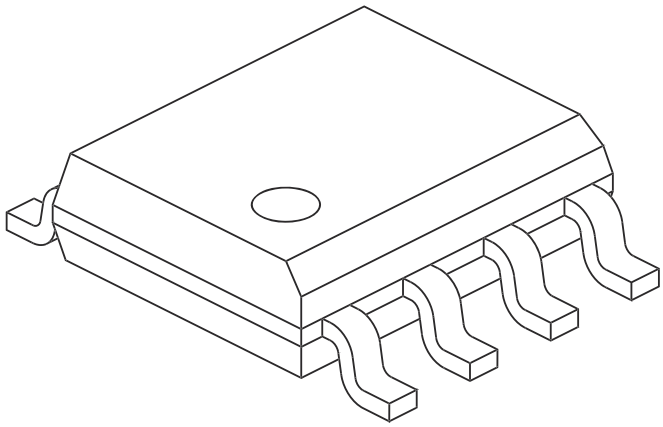


Microchip Technology Drawing No. C04-00057-SN Rev L Sheet 1 of 2

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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

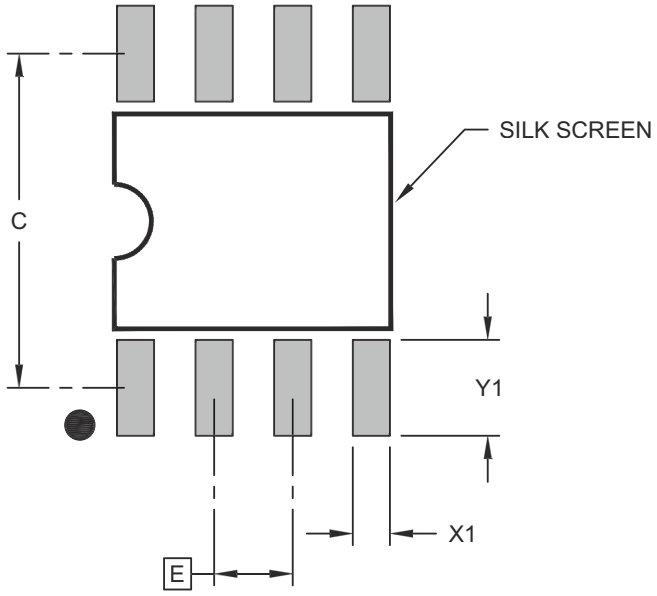
Microchip Technology Drawing No. C04-00057-SN Rev L Sheet 2 of 2

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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

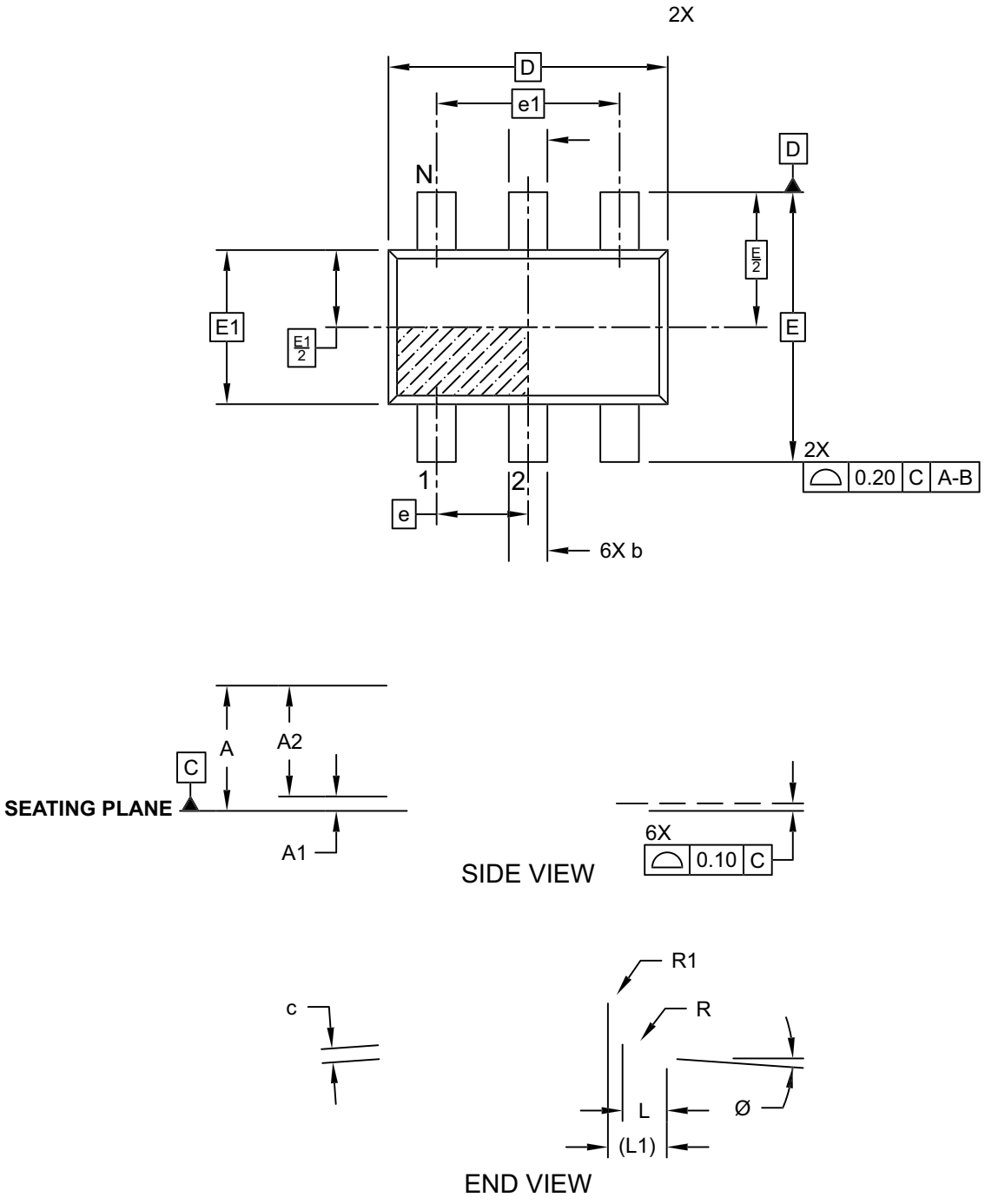
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-02057-SN Rev L

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6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



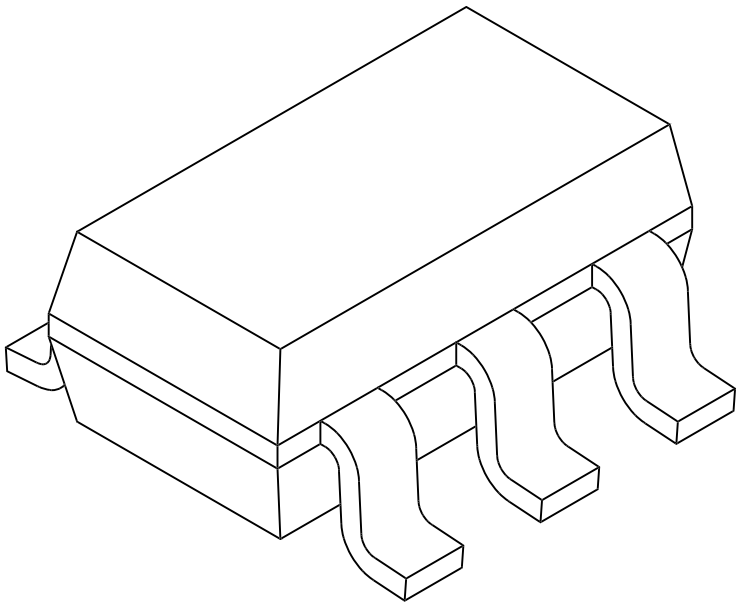
Microchip Technology Drawing C04-00028 [OT] Rev. G Sheet 1 of 2

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6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		6	
Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	1.15	1.30
Standoff	A1	0.00	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	0.45	0.60
Footprint	L1		0.60 REF	
Foot Angle	Ø	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. The theoretically exact value is shown without tolerances.

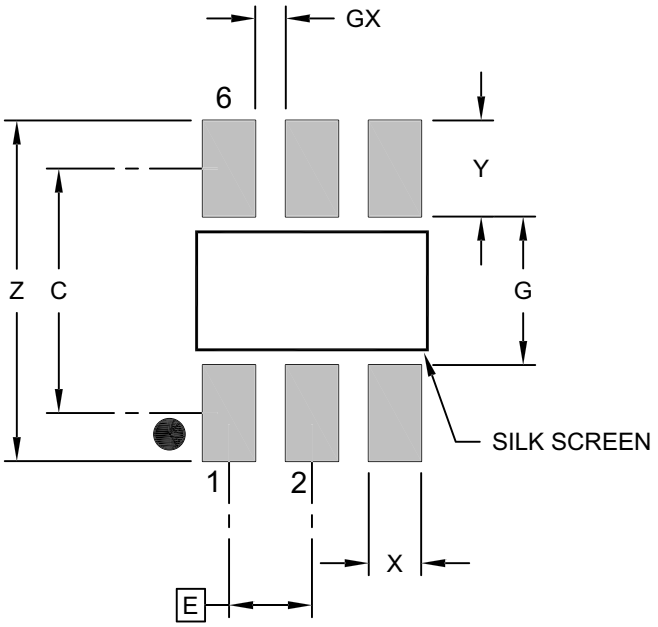
Microchip Technology Drawing C04-00028 [OT] Rev. G Sheet 2 of 2

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6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X6)	X			0.60
Contact Pad Length (X6)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. The theoretically exact value is shown without tolerances.

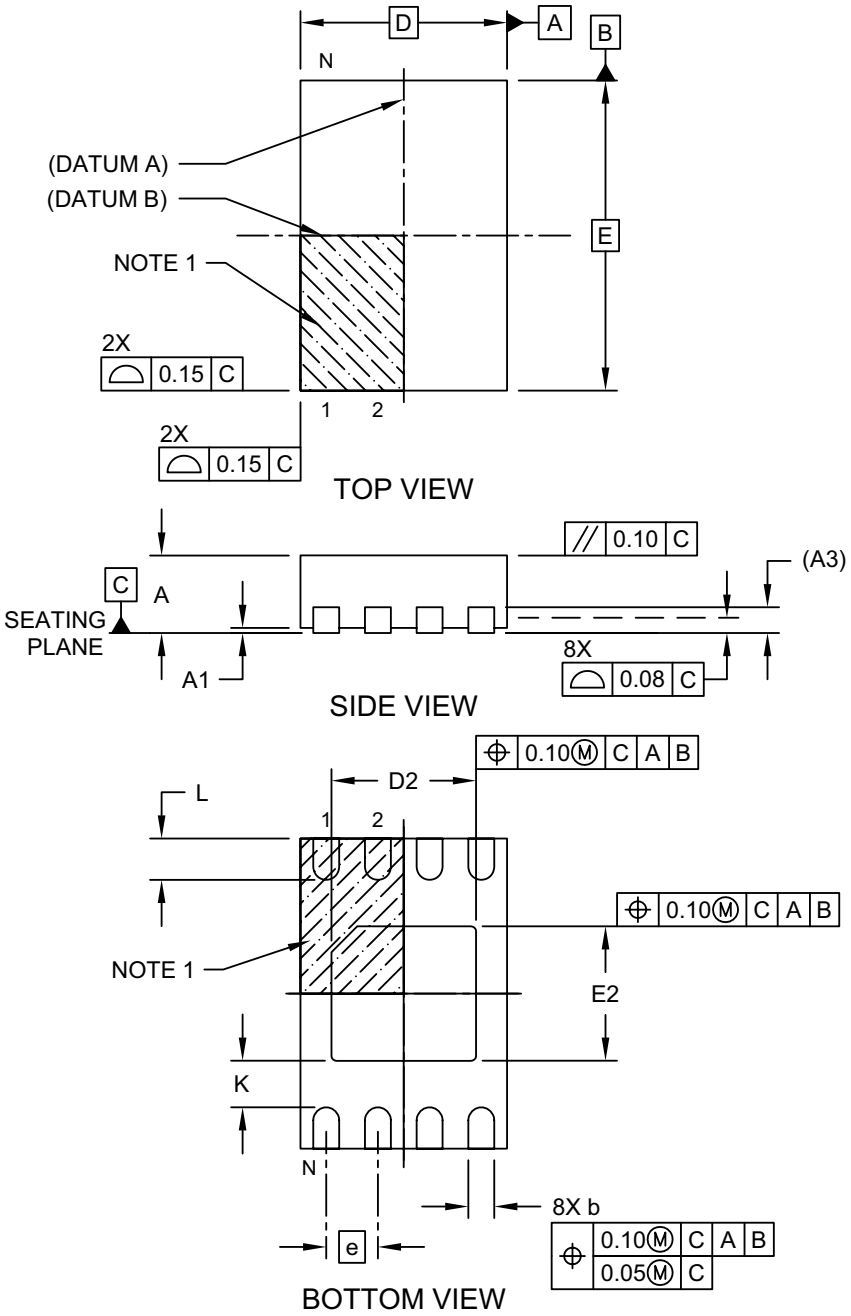
Microchip Technology Drawing No. C04-02028 [OT] Rev.G

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8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN]
With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

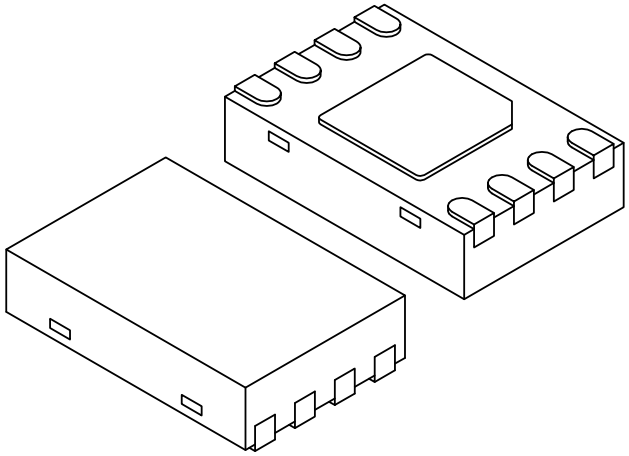


Microchip Technology Drawing No. C04-129-MN Rev E Sheet 1 of 2

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8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.35	1.40	1.45
Exposed Pad Width	E2	1.25	1.30	1.35
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

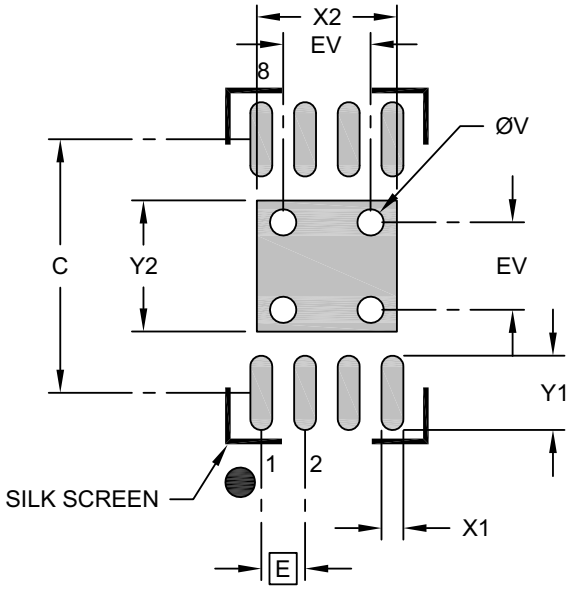
Microchip Technology Drawing No. C04-129-MN Rev E Sheet 2 of 2

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8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.50
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.25
Contact Pad Length (X8)	Y1			0.85
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

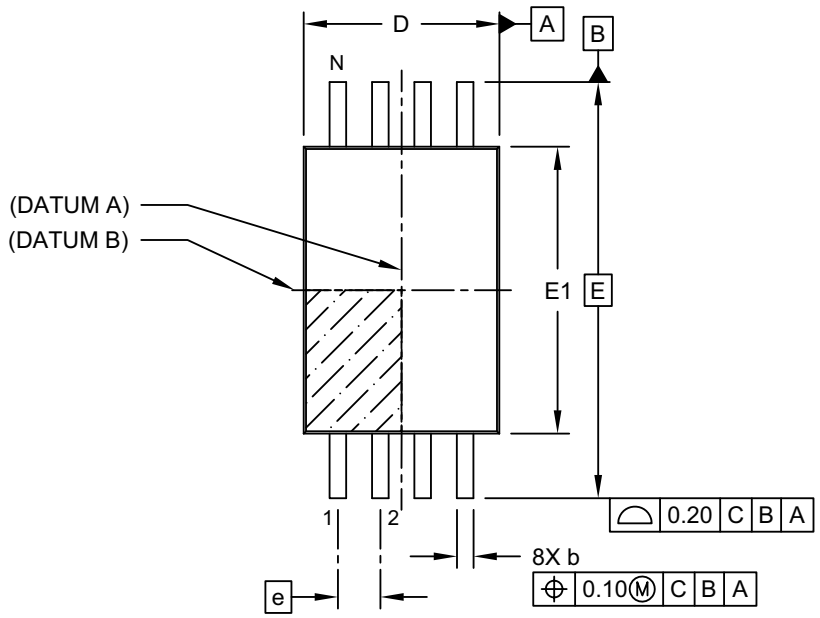
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-129-MN Rev. B

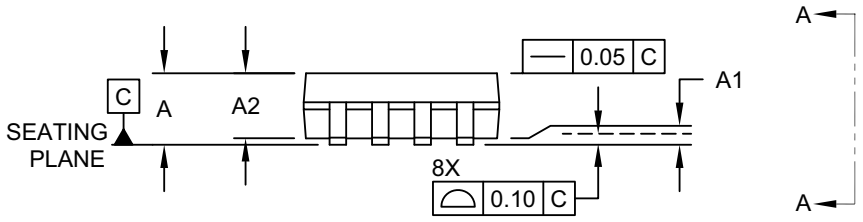
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8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

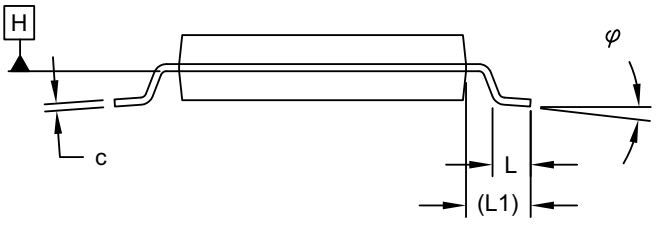
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A-A

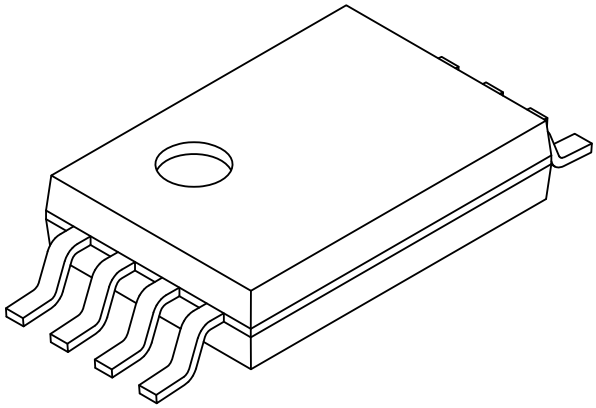
Microchip Technology Drawing C04-086 Rev C Sheet 1 of 2

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8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	-
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Overall Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Thickness	c	0.09	-	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.19	-	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

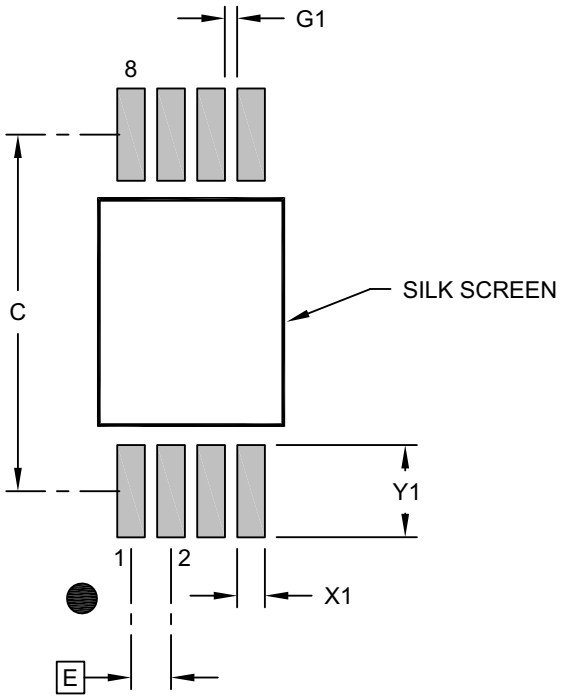
Microchip Technology Drawing C04-086 Rev C Sheet 2 of 2

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8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.80	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.50
Contact Pad to Center Pad (X6)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

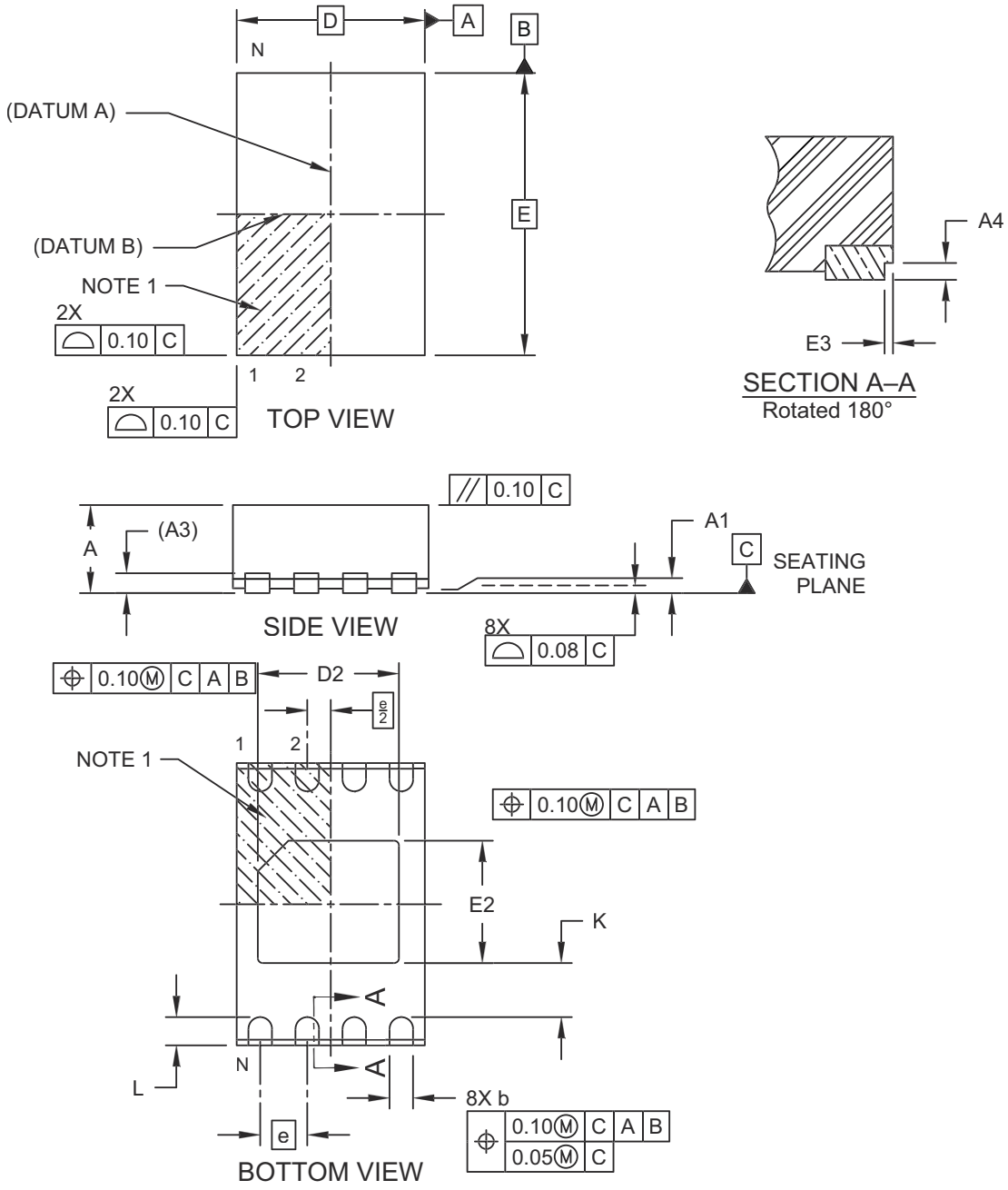
Microchip Technology Drawing C04-2086 Rev B

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8-Lead Very Thin Plastic Dual Flat, No Lead Package (MWF) - 2x3x1.0 mm Body [VDFN] 1.5x1.3 mm Exposed Pad Wettable Step Cut Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

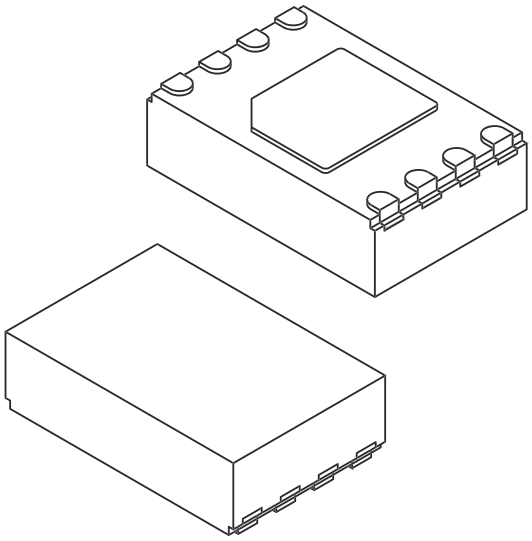


Microchip Technology Drawing C04-00598 Rev E Sheet 1 of 2

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8-Lead Very Thin Plastic Dual Flat, No Lead Package (MWF) - 2x3x1.0 mm Body [VDFN] 1.5x1.3 mm Exposed Pad Wettable Step Cut Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		008	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.40	1.50	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.20	1.30	1.40
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.25	0.35	0.45
Terminal-to-Exposed-Pad	K	0.20	–	–
Wettable Flank Step Cut Width	E3	0.035	0.06	0.085
Wettable Flank Step Cut Depth	A4	0.100	–	0.190

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

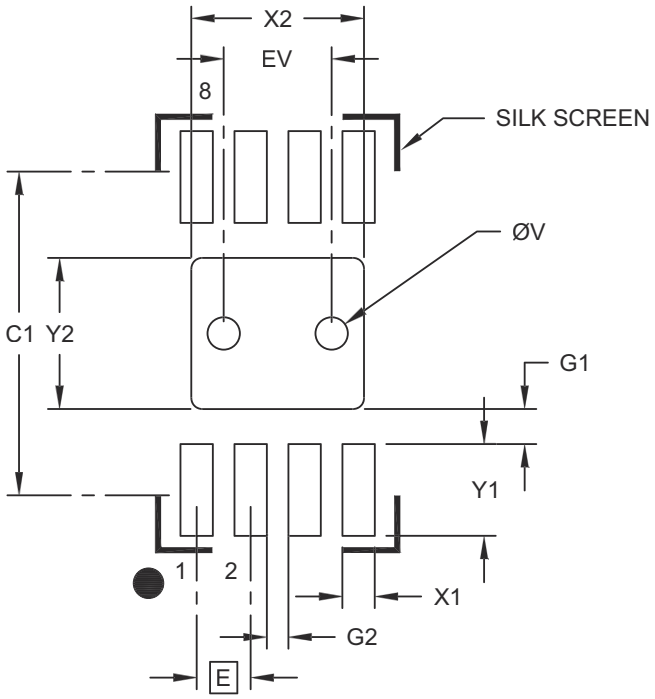
Microchip Technology Drawing C04-00598 Rev E Sheet 2 of 2

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8-Lead Very Thin Plastic Dual Flat, No Lead Package (MWF) - 2x3x1.0 mm Body [VDFN] 1.5x1.3 mm Exposed Pad Wettable Step Cut Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			1.60
Center Pad Length	Y2			1.40
Contact Pad Spacing	C1		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.33		
Contact Pad to Contact Pad (X6)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-02598 Rev E

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APPENDIX A: REVISION HISTORY

Revision O (09/2026)

Added VDFN package; Editorial updates throughout the document.

Revision N (06/2022)

Replaced terminology “Master” and “Slave” with “Host” and “Client” respectively. Updated PDIP, SOIC, TSSOP, MSOP, SOT-23, DFN and TDFN package drawings. Added Automotive Product Identification System.

Revision M (04/2012)

Revised Device Selection Table; Added Note to Package Types Diagram; Revised Marking Codes Table; Revised Product ID System.

Revision L (01/2012)

Added TDFN package.

Revision K (5/2008)

Revised Figures 2-1, 2-2, 2-6 and 2-7; Revised Package Marking Information; Replaced Package Drawings.

Revision J (10/2007)

Revised Device Selection Table; Revised Pin Function Table; Revised Package Types; Revised Table 3-1; Replaced Package Drawings; Revised Product ID System.

Revision H (11/2006)

Updated Package Drawings.

Revision G (09/2006)

Revised note in Sections 2.8 and 2.9. Replaced DFN package drawing.

Revision F (04/2005)

Added notes throughout.

Revision E (03/2005)

Added DFN package.

Revision D (02/2004)

Corrections to Device Selection Table, Table 1-1, Table 1-2, Section 2.4, Section 2.5, Section 2.8 and Section 2.9. Added note to Figure 2-7.

Revision C (12/2003)

Corrections to Section 1.0, Electrical Characteristics. Section 4.1, 6-Lead SOT-23 package to OT.

Revision B (07/2003)

Revision A (05/2003)

Initial release.

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PRODUCT IDENTIFICATION SYSTEM (NON-AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X[1]	-X	/XX
Device	Tape and Reel	Temperature Range	Package

Device:	93AA76A:	8-Kbit 1.8V Microwire Serial EEPROM (x8)	
	93AA76B:	8-Kbit 1.8V Microwire Serial EEPROM (x16)	
	93AA76C:	8-Kbit 1.8V Microwire Serial EEPROM w/ORG	
	93LC76A:	8-Kbit 2.5V Microwire Serial EEPROM (x8)	
	93LC76B:	8-Kbit 2.5V Microwire Serial EEPROM (x16)	
	93LC76C:	8-Kbit 2.5V Microwire Serial EEPROM w/ORG	
	93C76A:	8-Kbit 5.0V Microwire Serial EEPROM (x8)	
	93C76B:	8-Kbit 5.0V Microwire Serial EEPROM (x16)	
	93C76C:	8-Kbit 5.0V Microwire Serial EEPROM w/ORG	
Tape and Reel:	Blank	=	Standard pinout
	T	=	Tape and Reel[1]
Temperature Range:	I	=	-40°C to +85°C (Industrial)
	E	=	-40°C to +125°C (Extended)
Package:	MS	=	Plastic Micro Small Outline - 8-Lead (MSOP)
	OT	=	Plastic Small Outline Transistor - 6-Lead (SOT-23) (Tape and Reel only)
	P	=	Plastic Dual In-Line - 300 mil Body, 8-Lead (PDIP)
	SN	=	Plastic Small Outline - Narrow, 3.90 mm, 8-Lead (SOIC)
	ST	=	Plastic Thin Shrink Small Outline - 4.4 mm, 8-Lead (TSSOP)
	MC	=	Plastic Dual Flat, No Lead - 2x3x0.9 mm Body, 8-Lead (DFN)
	MNY[2]	=	Plastic Dual Flat, No Lead - 2x3x0.8 mm Body, 8-Lead (TDFN) (Tape and Reel only)

Examples:

a) 93AA76C-I/P: 8-Kbit, 1024x8 or 512x16, 1.8V Serial EEPROM, Industrial Temperature, PDIP package

b) 93AA76AT-I/OT: 8-Kbit, 1024x8, 1.8V Serial EEPROM, Industrial Temperature, Tape and Reel, SOT-23 package

c) 93AA76CT-I/MS: 8-Kbit, 1024x8 or 512x16, 1.8V Serial EEPROM, Industrial Temperature, Tape and Reel, MSOP package

a) 93LC76C-I/ST: 8-Kbit, 1024x8 or 512x16, 2.5V Serial EEPROM, Industrial Temperature, TSSOP package

b) 93LC76BT-I/OT: 8-Kbit, 512x16, 2.5V Serial EEPROM, Industrial Temperature, Tape and Reel, SOT-23 package

c) 93LC76CT-E/MNY: 8-Kbit, 1024x8 or 512x16, 2.5V Serial EEPROM, Extended Temperature, Tape and Reel, TDFN package

a) 93C76C-I/MS: 8-Kbit, 1024x8 or 512x16, 5.0V Serial EEPROM, Industrial Temperature, MSOP package

b) 93C76AT-I/OT: 8-Kbit, 1024x8, 5.0V Serial EEPROM, Industrial Temperature, Tape and Reel, SOT-23 package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: "Y" indicates a Nickel Palladium Gold (NiPdAu) finish.

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PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office..

PART NO.	X[1]	-X	/XX	XXX[2,3,4]
Device	Tape and Reel	Temperature Range	Package	Variant

Device:	93AA76A:	8-Kbit 1.8V Microwire Serial EEPROM (x8)	
	93AA76B:	8-Kbit 1.8V Microwire Serial EEPROM (x16)	
	93AA76C:	8-Kbit 1.8V Microwire Serial EEPROM w/ORG	
	93LC76A:	8-Kbit 2.5V Microwire Serial EEPROM (x8)	
	93LC76B:	8-Kbit 2.5V Microwire Serial EEPROM (x16)	
	93LC76C:	8-Kbit 2.5V Microwire Serial EEPROM w/ORG	
	93C76A:	8-Kbit 5.0V Microwire Serial EEPROM (x8)	
	93C76B:	8-Kbit 5.0V Microwire Serial EEPROM (x16)	
	93C76C:	8-Kbit 5.0V Microwire Serial EEPROM w/ORG	
Tape and Reel:	Blank =	Standard pinout	
	T =	Tape and Reel[1]	
Temperature Range:	I =	-40°C to +85°C (AEC-Q100 Grade 3)	
	E =	-40°C to +125°C (AEC-Q100 Grade 1)	
Package:	MS =	Plastic Micro Small Outline - 8-Lead (MSOP)	
	OT =	Plastic Small Outline Transistor - 6-Lead (SOT-23) (Tape and Reel only)	
	SN =	Plastic Small Outline - Narrow, 3.90 mm, 8-Lead (SOIC)	
	ST =	Plastic Thin Shrink Small Outline - 4.4 mm, 8-Lead (TSSOP)	
	MWF =	Very Thin Plastic Dual Flat, No Lead Package – 2x3x1.0 mm, 8-Lead (VDFN) (Tape and Reel only)	
Variant[2,3]:	15KVAO =	Standard Automotive, 15K Process[4]	
	15KVXX =	Customer-Specific Automotive, 15K Process[4]	
	36KVAO =	Standard Automotive, 36K Process	
	36KVXX =	Customer-Specific Automotive, 36K Process	

Examples:

a) 93LC76CT-E/MWF36KVAO: 8-Kbit, 2048x8 or 1024x16, 2.5V Serial EEPROM, Tape and Reel, Automotive Grade 1, VDFN package

b) 93LC76CT-E/SN36KVAO: 8-Kbit, 2048x8 or 1024x16, 2.5V Serial EEPROM, Tape and Reel, Automotive Grade 1, SOIC package

c) 93LC76CT-E/ST36KVAO: 8-Kbit, 2048x8 or 1024x16, 2.5V Serial EEPROM, Tape and Reel, Automotive Grade 1, TSSOP package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: The VAO/VXX automotive variants have been designed, manufactured, tested and qualified in accordance with AEC-Q100 requirements for automotive applications.

3: For customers requesting a PPAP, a customer-specific part number will be generated and provided. A PPAP is not provided for VAO part numbers.

4: Not recommended for new designs.

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