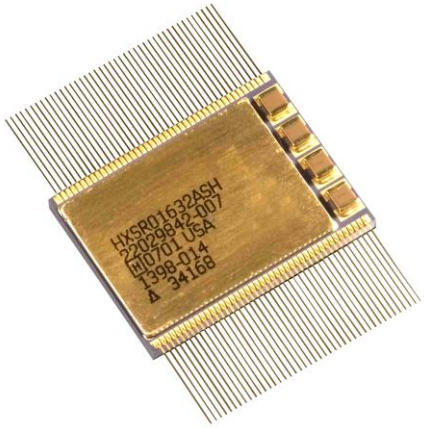
Honeywell

HXSR01632
512K x 32 STATIC RAM



The monolithic, radiation hardened 16M bit Static Random Access Memory (SRAM) in a 512k x 32 configuration is a high performance 524,288 word x 32 bit SRAM fabricated with Honeywell's 150nm silicon-on-insulator CMOS (S150) technology. It is designed for use in low voltage systems operating in radiation sensitive environments. The RAM operates over the full military temperature range and requires a core supply voltage of 1.8V +/- 0.15V and an I/O supply voltage of 3.3V ± 0.3V or 2.5V ± 0.2V.

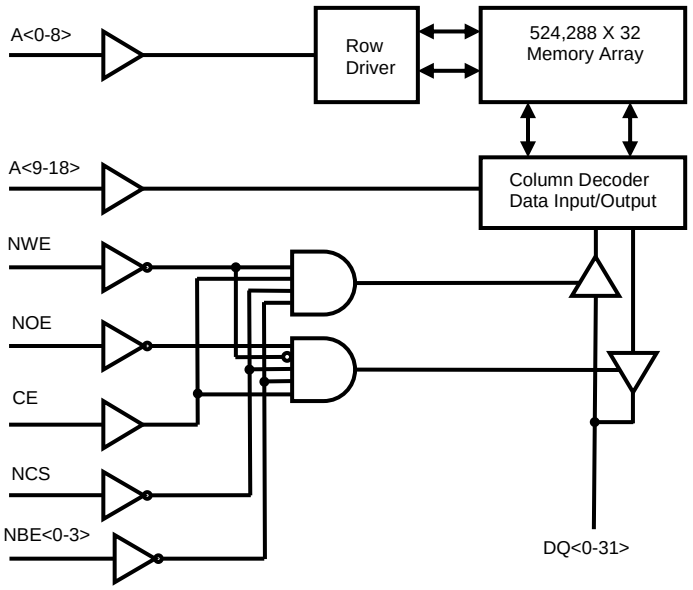
Honeywell's state-of-the-art S150 technology is radiation hardened through the use of advanced and proprietary design, layout and process hardening techniques. There is no internal EDAC implemented.

It is a low power process with a minimum drawn feature size of 150 nm. It consumes less than 300mW typical power at 40MHz operation. The SRAM is fully asynchronous with a typical access time of 13 ns at 3.3V. A seven transistor (7T) memory cell is used for superior single event upset hardening, while four layer metal power busing and the low collection volume SOI substrate provide improved dose rate hardening.

FEATURES

- Fabricated on S150 Silicon On Insulator (SOI) CMOS
- 150 nm Process (Leff = 110 nm)
- Read Cycle Times
  - Typical ≤13 ns
  - Worst case ≤ 20 ns
- Write Cycle Times
  - Typical ≤ 9 ns
  - Worst case ≤ 12 ns
- Asynchronous Operation
- CMOS Compatible I/O
- Total Dose ≥1X10^{6} rad(Si)
- Soft Error Rate
  - Heavy Ion ≤1x10^{-12} Upsets/bit-day
  - Proton ≤2x10^{-12} Upsets/bit-day
- Neutron ≥ 1x10^{14} cm^{-2}
- Dose Rate Upset ≥1x10^{10} rad(Si)/s
- Dose Rate Survivability
  - ≥1x10^{12} rad(Si)/s
- No Latchup
- Core Power Supply
  - 1.8 V ± 0.15 V
- I/O Power Supply
  - 3.3 V ± 0.3 V
  - 2.5 V ± 0.2 V
- Operating Range is
  - -55°C to +125°C
- 86-Lead Flat Pack Package

FUNCTIONAL DIAGRAM



86 LEAD FLAT PACK PINOUT

Note 1: Pin 1 and Pin 86 shall be connected to VSS on the circuit board.

HXSR01632 Top View Note 1

Cathode	1	86	Anode
VSS	2	85	VSS
VDD	3	84	VDD
A0	4	83	VDD
A1	5	82	A18
A2	6	81	A17
A3	7	80	A16
A4	8	79	A15
VSS	9	78	VSS
VDD2	10	77	VDD2
DQ0	11	76	DQ31
DQ1	12	75	DQ30
DQ2	13	74	DQ29
DQ3	14	73	DQ28
DQ4	15	72	DQ27
DQ5	16	71	DQ26
VSS	17	70	VSS
VDD2	18	69	VDD2
NBE0	19	68	NBE3
NCS	20	67	NOE
DQ6	21	66	DQ25
DQ7	22	65	DQ24
DQ8	23	64	DQ23
DQ9	24	63	DQ22
NWE	25	62	CE
NBE1	26	61	NBE2
VDD2	27	60	VDD2
VSS	28	59	VSS
DQ10	29	58	DQ21
DQ11	30	57	DQ20
DQ12	31	56	DQ19
DQ13	32	55	DQ18
DQ14	33	54	DQ17
DQ15	34	53	DQ16
VDD2	35	52	VDD2
VSS	36	51	VSS
A5	37	50	A14
A6	38	49	A13
A7	39	48	A12
A8	40	47	A11
A9	41	46	A10
VDD	42	45	VDD
VSS	43	44	VSS

SIGNAL DEFINITIONS

A (0-18)	Address input signals. Used to select a particular 32 bit word within the memory array.
DQ (0-31)	Bi-directional data signals. These function as data outputs during a read operation and as data inputs during a write operation.
NCS	Negative Chip Select input signal. Setting to a low level allows normal read or write operation. When at a high level, it sets the SRAM to a precharge condition and holds the data output drivers in a high impedance state. If the NCS signal is not used it must be connected to VSS.
NWE	Negative Write Enable input signal. Setting to a low level activates a write operation and holds the data output drivers in a high impedance state. When at a high level it allows normal read operation.
NOE	Negative Output Enable input signal. Setting to a high level holds the data output drivers in a high impedance state. When at a low level, the data output driver state is defined by NCS, NBE, CE and NWE. If this signal is not used, it must be connected to VSS.
CE	Chip Enable input signal. When set to a high level, the SRAM is in normal read or write operation. When at a low level, it defaults the SRAM to a pre-charge condition and holds the data output drivers in a high impedance state. If the CE signal is not used, it must be connected to VDD2.
NBE (0-3)	Not Byte Enable input signal. When set to a low level, enables a read or write operation on a specific byte within the 32 bit (4 byte) word. When at a high level, the write operation of a specific byte is disabled and during a read operation the 8 data outputs of the specific byte are held in a high impedance state.
VDD	SRAM Core operating voltage (typical 1.8V)
VDD2	I/O Operating voltage (typical 3.3V OR 2.5V)
Cathode and Anode	These signals are used for manufacturing test only. They shall be connected to VSS.

TRUTH TABLE

CE	NCS	NWE	NOE	NBE				Mode	DQ			
				0	1	2	3		0-7	8-15	16-23	24-31
L	X	X	X	X	X	X	X	Disable	Hi-Z	Hi-Z	Hi-Z	Hi-Z
X	H	X	X	X	X	X	X	De-select	Hi-Z	Hi-Z	Hi-Z	Hi-Z
H	L	H	L	L	H	H	H	Read	DO	Hi-Z	Hi-Z	Hi-Z
H	L	H	L	H	L	H	H	Read	Hi-Z	DO	Hi-Z	Hi-Z
H	L	H	L	H	H	L	H	Read	Hi-Z	Hi-Z	DO	Hi-Z
H	L	H	L	H	H	H	L	Read	Hi-Z	Hi-Z	Hi-Z	DO
H	L	H	L	L	L	L	L	Read	DO	DO	DO	DO
H	L	L	H	L	H	H	H	Write	DI	X	X	X
H	L	L	H	H	L	H	H	Write	X	DI	X	X
H	L	L	H	H	H	L	H	Write	X	X	DI	X
H	L	L	H	H	H	H	L	Write	X	X	X	DI
H	L	L	H	L	L	L	L	Write	DI	DI	DI	DI

X: VI = VIH or VIL,
NOE = VIH: High Z output state maintained for NCS = X, CE = X, NWE = X, NBE = X

RADIATION CHARACTERISTICS

Total Ionizing Radiation Dose

The SRAM will meet all stated functional and electrical specifications after the specified total ionizing radiation dose. All electrical and timing performance parameters will remain within specifications, post rebound (based on extrapolation), after an operational period of 15 years. Total dose hardness is assured by wafer level testing of process monitor transistors and RAM product using 10 KeV X-ray. Parameter correlations have been made between 10 KeV X-rays applied at dose rates of $1x10^5$ to $5x10^5$ rad(SiO_2)/min at T= 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

Transient Pulse Ionizing Radiation

The SRAM is capable of writing, reading, and retaining stored data during and after exposure to a transient ionizing radiation pulse, up to the specified transient dose rate upset specification, when applied under recommended operating conditions. It is recommended to provide external power supply decoupling capacitors to maintain VDD and VDD2 voltage levels during transient events. The SRAM will meet any functional or electrical specification after exposure to a radiation pulse up to the transient dose rate survivability specification, when applied under recommended operating conditions. Note that the current conducted during the pulse by the RAM inputs, outputs, and power supply may significantly exceed the normal operating levels. The application design must accommodate these effects.

Neutron Radiation

The SRAM will meet any functional or timing specification after exposure to the specified neutron fluence under recommended operating or storage conditions. This assumes an equivalent neutron energy of 1 MeV.

Soft Error Rate

The SRAM is capable of meeting the specified Soft Error Rate (SER), under recommended operating conditions. The specification applies to both heavy ion and proton. This heavy ion hardness level is defined by the Adams 90% worst case cosmic ray environment for geosynchronous orbits.

Latchup

The SRAM will not latch up due to any of the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with the SOI substrate material provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures. Sufficient transistor body tie connections to the p- and n-channel substrates are made to ensure no source/drain snapback occurs.

RADIATION-HARDNESS RATINGS (1)

Parameter	Limits	Units	Test Conditions
Total Dose	≥1X10^{6}	rad(Si)	T_A=25°C, VDD2=3.6V, VDD=1.95V
Transient Dose Rate Upset	≥1X10^{10}	rad(Si)/s	Pulse width = 50 ns,X-ray, VDD2 = 3.0V, VDD=1.65V, T_C=25°C
Transient Dose Rate Survivability	≥1X10^{12}	rad(Si)/s	Pulse width = 50 ns,X-ray, VDD2 = 3.6V, VDD=1.95V, T_A=25°C
Soft Error Rate Heavy Ion Proton	<1X10^{-12} <2X10^{-12}	Upsets/bit-day	VDD2=3.0V, VDD=1.65V, T_C= 25 and 125°C, Adams 90% worst case environment
Neutron Fluence	≥1X10^{14}	N/cm^2	1MeV equivalent energy, Unbiased, T_A=25°C

(1) Device will not latch up due to any of the specified radiation exposure conditions.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter		Rating Min	Rating Max	Units
VDD	Supply Voltage (core) (2)		-0.5	2.4	Volts
VDD2	Supply Voltage (I/O) (2)		-0.5	4.4	Volts
VPIN	Voltage on Any Pin (2)		-0.5	VDD2+0.5	Volts
IOUT	Average Output Current			15	mA
PD	Maximum Power Dissipation (3)			2.5	W
VPROT	Electrostatic Discharge Protection Voltage (4)		2000		V
TSTORE	Storage Temperature		-65	150	°C
TSOLDER	Soldering Temperature (5)			270	°C
TJ	Maximum Junction Temperature			175	°C
PJC	Package Thermal Resistance (Junction-to-Case)	86 Pin FP		2.0	°C/W

(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to VSS.
(3) RAM power dissipation including output driver power dissipation due to external loading must not exceed this specification.
(4) Class 2 electrostatic discharge (ESD) input protection voltage per MIL-STD-883, Method 3015
(5) Maximum soldering temp of 270°C can be maintained for no more than 5 seconds.

RECOMMENDED OPERATING CONDITIONS (1)

Symbol	Parameter	Description Min	Description Typ	Description Max	Units
VDD	Supply Voltage (core)	1.65	1.80	1.95	Volts
VDD2	Supply Voltage (I/O)	3.0 2.3	3.3 2.5	3.6 2.7	Volts Volts
TC	External Package Temperature	-55	25	125	°C
VPIN	Voltage on Any Pin	-0.3		VDD2+0.3	Volts
VDD2/VDD Ramp Time	Supply Voltages Ramp Time			1.0	Second
V_{DDD}/ V_{DD} PDT (2)	Power Supply Power Down Time	5			msec

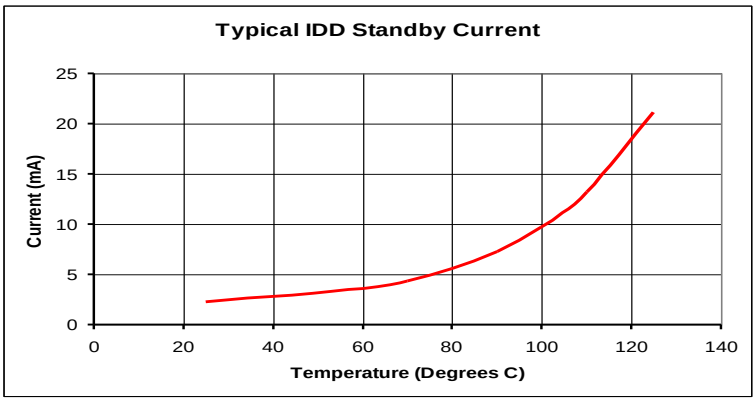
(1) Voltages referenced to Vss.
(2) Power Supplies must be turned off for power down time before turned back on.

DC ELECTRICAL CHARACTERISTICS (1)

Symbol	Parameter	Min	Max		Units	Test Conditions
			IDD	IDD2		
IDDSB (4)	Static Supply Current					
	TA=25°C		5 (5)	0.3	mA	VDD=max, Iout=0mA, Inputs Stable
	TA=85°C		9 (6)	0.3	mA	
	TA=125°C		30	0.3		
IDDOP1	Dynamic Supply Current – Deselected		0.1	0.2	mA	VDD=max, Iout=0mA, F=1MHz, NCS=VIH (3)
IDDOP3	Operating Current - Disabled		2	5	mA	VDD=max, Iout=0mA, F=40MHz, NCS=VIH (3)
IDDOPW	Dynamic Supply Current, Selected (Write)					
	1 MHz		5	0.35	mA	VDD2 and VDD=max, Iout=0mA, NCS=VIL (1) (2) (3)
	2 MHz		10	0.7	mA	
	10 MHz		50	3.5	mA	
	25 MHz		125	8.7	mA	
	40 MHz		200	14	mA	
IDDOPR	Dynamic Supply Current, Selected (Read)					
	1 MHz		2	0.2	mA	VDD2 and VDD=max, Iout=0mA, NCS=VIL (1) (3)
	2 MHz		4	0.4	mA	
	10 MHz		20	2	mA	
	25 MHz		50	5	mA	
	40 MHz		80	8	mA	
IDR	Data Retention Current TA=25°C		2	0.20	mA	VDD=1V, VDD2=2V
	(6) TA=125°C		20	0.20		

Symbol	Parameter	Min	Max	Units	Test Conditions
II	Input Leakage Current	-5	5	µA	
IOZ	Output Leakage Current	-10	10	µA	Output = high Z
VIL	Low-Level Input Voltage		0.25xVDD2	V	VDD2=3.0V to 3.6V
VIH	High-Level Input Voltage	0.75xVDD2		V	VDD2=3.0V to 3.6V
VOL	Low-Level Output Voltage		0.4	V	VDD2=3.0V, IOL = 10mA
VOH	High-Level Output Voltage	2.7		V	VDD2=3.0V, IOH = 5mA

(1) Worst case operating conditions: VDD2=2.3V to 3.6V, VDD=1.65V to 1.95V, -55°C to +125°C. Post-radiation performance guaranteed at 25°C per MIL-STD-883 method 1019 up to 1MRad(Si) total dose.
(2) All inputs switching. DC average current.
(3) All dynamic operating mode current measurements (IDDOPx) exclude standby mode current (IDDSB)
(4) See graph below for typical static current values.
(5) For applications with maximum dose rates <1 Rad(Si)/s this value applies post total dose. For applications with maximum dose rates from 1 to 300Rad(Si)/s the 125^{O}C limit applies post total dose at 25^{O}C.
(6) This is an estimated maximum for reference and is not a pass/fail criteria.



CAPACITANCE (1)

Symbol	Parameter	Worst Case (1)		Units	Test Conditions
		Min	Max		
CA	Address Input Capacitance		7	pF	VIN=VDD or VSS, f=1 MHz
CC	NCS, NOE, NWE Input Capacitance		15	pF	VIN=VDD or VSS, f=1 MHz
CD	Data I/O, NBE Capacitance		7	pF	VIN=VDD or VSS, f=1 MHz

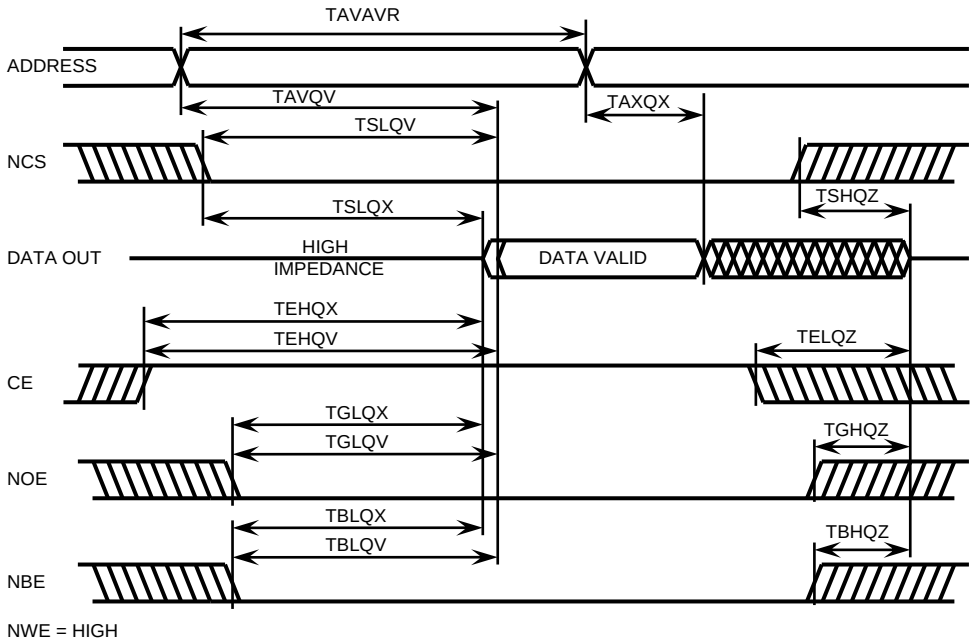
(1) This parameter is tested during initial qualification only.

READ CYCLE AC TIMING CHARACTERISTICS (1)(2)

Symbol	Parameter	VDD2 = 3.3V or 2.5V		Units
		Min	Max	
TAVAVR	Read Cycle Time (3)	20, 22		ns
TAVQV	Address Access Time (3)		20, 22	ns
TAXQX	Address Change to Output Invalid Time	4		ns
TSLQV	Chip Select Access Time (3)		20, 22	ns
TSLQX	Chip Select Output Enable Time	0		ns
TSHQZ	Chip Select Output Disable Time		4	ns
TEHQV	Chip Enable Access Time (3)		20, 22	ns
TEHQX	Chip Enable Output Enable Time	0		ns
TELQZ	Chip Enable Output Disable Time		4	ns
TBLQV	Byte Enable Access Time		6	ns
TBLQX	Byte Enable Output Enable Time	0		ns
TBHQZ	Byte Enable Output Disable Time		4	ns
TGLQV	Output Enable Access Time		6	ns
TGLQX	Output Enable Output Enable Time	0		ns
TGHQZ	Output Enable Output Disable Time		4	ns

(1) Test conditions: VIL/VIH=0V/Vdd. Reference Tester Equivalent Load Circuit and Tester AC Timing Characteristics diagrams. Capacitive output loading C_L=5 pF for TSHQZ and TGHQZ.
(2) Worst case operating conditions: VDD2=2.3V to 3.6V, VDD=1.65V to 1.95V, TA=-55°C to 125°C, post total dose at 25°C.
(3) Values shown for 3.3V and 2.5V VDD2, respectively.

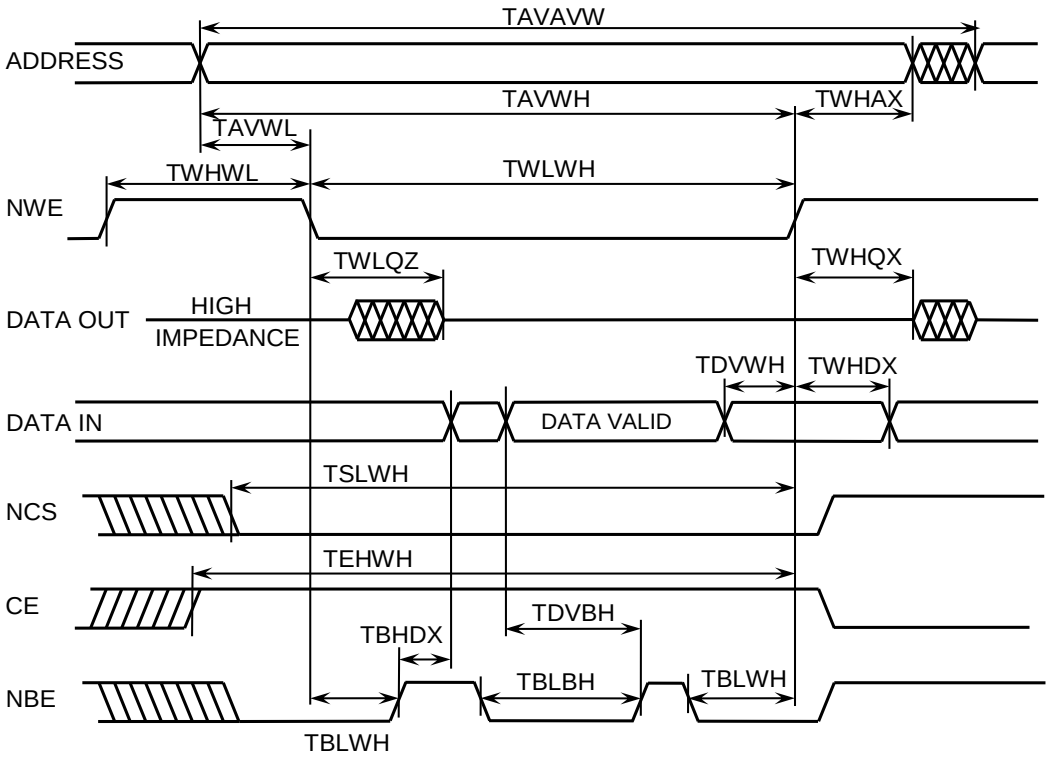
READ CYCLE TIMING



WRITE CYCLE AC TIMING CHARACTERISTICS (1)

Symbol	Parameter	VDD2 = 3.3V or 2.5V		
		Min	Max	Units
TAVAVW	Write Cycle Time (2)	12		ns
TWLWH	Write Enable Write Pulse Width	7		ns
TSLWH	Chip Select to End of Write Time	10		ns
TEHWH	Chip Enable to End of Write Time	10		ns
TDVWH	Data Valid to End of Write Time	6		ns
TAVWH	Address Valid to End of Write Time	12		ns
TWHDX	Data Hold after End of Write Time	0		ns
TAVWL	Address Valid Setup to Start of Write Time	0		ns
TWHAX	Address Valid Hold after End of Write Time	0		ns
TWLQZ	Write Enable to Output Disable Time		4	ns
TWHQX	Write Disable to Output Enable Time	0		ns
TWHWL	Write Disable to Write Enable Pulse Width (3)	5		ns
TBLWH	Byte Enable to End of Write Time	10		ns
TBLBH	Byte Enable Pulse Width	8		ns
TBLWH	Byte Enable to End of Write Time	8		ns
TWLBH	Write Enable to End of Byte Enable	8		ns
TDVBH	Data Valid to End of Byte Enable	8		ns
TBHDX	Data Hold Time after End of Byte Enable	0		ns

(1) Test conditions: VIL/VIH=0V/Vdd. Reference Tester Equivalent Load Circuit and Tester AC Timing Characteristics diagrams. Capacitive output loading C_L=5 pF for TWLQZ. Worst case operating conditions: VDD2=2.3V to 3.6V, VDD=1.65V to 1.95V, -55°C to 125°C, post total dose 25°C
(2) TAVAVW = TWLWH + TWHWL
(3) Guaranteed but not tested.



DYNAMIC ELECTRICAL OPERATION

Asynchronous Operation

The RAM is asynchronous in operation. Read and Write cycles are controlled by NWE, NCS, CE, NBE(0-3) and Address signals.

NBE(0-3) is used to control which of the 4 bytes is written to or read from. These can be used independently. When set to a low level, the signals enable a normal read or write operation. When at a high level, the write operation of a specific byte is disabled and during a read operation, the 8 data outputs of the specific byte are held in a high impedance state.

Read Operation

To perform a valid read operation, NCS, NBE(0-3) and NOE must be low and NWE and CE must be high. The output drivers can be controlled independently by the NOE signal. Although not required, it is recommended to delay NOE slightly relative to the address and other control lines at the beginning of the read cycle. This is done to minimize the potential for coupling noise from the outputs back into the inputs since up to 32 outputs can switch when NOE is activated.

It is important to have the address bus free of noise and glitches, which can cause inadvertent, read operations. The control and address signals should have rising and falling edges that are fast (<5 ns) and have good signal integrity (free of noise, ringing or steps associated reflections).

The read mode can be controlled via two different control signals: CE and NCS. Both modes of control are similar, except the signals are of opposite polarity.

To control a read cycle with NCS, all addresses must be valid prior to or coincident with the enabling NCS edge transition. Address edge transitions can occur later than the specified setup times to NCS; however, the valid data access time will be delayed. Any address edge transition, which occurs during the time when NCS is low, will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TSHQZ time following a disabling NCS edge transition.

For an address activated read cycle, NCS must be valid prior to or coincident with the address edge transition(s). Any amount of toggling or skew between address edge transitions is permissible; however, data outputs will become valid TAVQV time following the latest occurring address edge transition. The minimum address activated read cycle time is TAVAVR. When the RAM is operated at the minimum address activated read cycle time, the data outputs will remain valid on the RAM I/O until TAXQX time following the next sequential address transition.

To perform consecutive read operations, NCS is required to be held continuously low, and the toggling of the addresses will start the new read cycle.

Write Operation

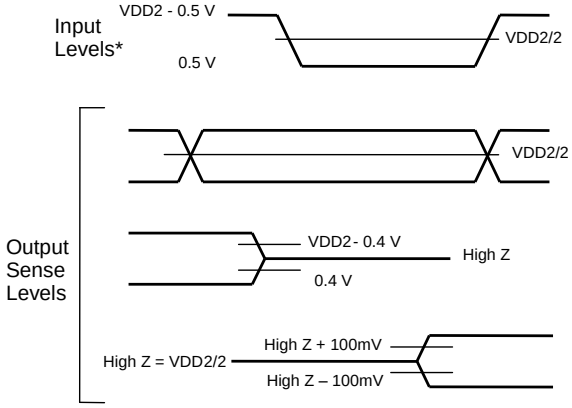
To perform a write operation, NWE, NCS and NBE(0-3) must be low and CE must be high.

The write mode can be controlled via three different control signals: NWE, CE and NCS. All modes of control are similar. Only the NWE controlled mode is shown in the table and diagram on the previous page for simplicity; however, each mode of control provides the same write cycle timing characteristics. Thus, some of the parameter names referenced below are not shown in the write cycle table or diagram, but indicate which control pin is in control as it switches high or low. To write data into the RAM, NWE and NCS must be held low for at least TWLWH/TSLWH/TEHWH time. Any amount of edge skew between the signals can be tolerated, and any one of the control signals can initiate or terminate the write operation. The DATA IN must be valid TDVWH time prior to switching high.

Consecutive write cycles can be performed by toggling one of the control signals while the other remains in their “write” state (NWE or NCS held continuously low). At least one of the control signals must transition to the opposite state between consecutive write operations.

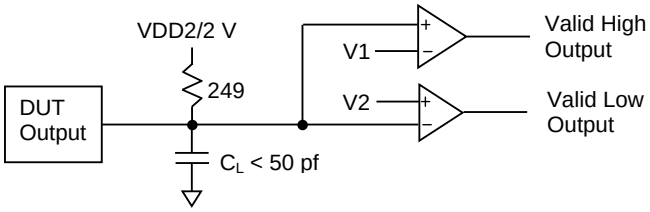
For consecutive write operations, write pulses (NWE) must be separated by the minimum specified TWHWL/TSHSL time. Address inputs must be valid at least TAVWL time before the enabling NWE/NCS edge transition, and must remain valid during the entire write time. A valid data overlap of write pulse width time of TDVWH, and an address valid to end of write time of TAVWH also must be provided for during the write operation. Hold times for address inputs and data inputs with respect to the disabling NWE/NCS edge transition must be a minimum of TWHAX time and TWHDX time, respectively. The minimum write cycle time is TAVAVW.

TESTER AC TIMING CHARACTERISTICS



* Input rise and fall times < 5 ns

TESTER EQUIVALENT LOAD CIRCUIT



RELIABILITY

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered thousands of QML parts since first becoming QML qualified in 1990.

Using this proven approach Honeywell will assure the reliability of the SRAMs manufactured with the S150 process technology. This approach includes adhering to Honeywell's General Manufacturing Standards for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDB, hot carriers, negative bias temperature instability, radiation)
- Utilizing a structured and controlled design process
- A statistically controlled wafer fabrication process with a continuous defect reduction process
- Individual wafer lot acceptance through process monitor testing (includes radiation testing)
- The use of characterized and qualified packages
- A thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

QUALIFICATION AND SCREENING

The S150 technology was qualified by Honeywell after meeting the criteria of the General Manufacturing Standards and is QML Qualified. This approval is the culmination of years of development and requires a considerable amount of testing, documentation, and review.
The test flow includes screening units with the defined flow (Class V and Q equivalent) and the appropriate periodic or lot conformance testing (Groups B, C, D, and E). Both the S150 process and the SRAM products are subject to period or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests, respectively.

Group A	General Electrical Tests
Group B	Mechanical - Dimensions, bond strength, solvents, die shear, solderability, Lead Integrity, seal, acceleration
Group C	Life Tests - 1000 hours at 125C or equivalent
Group D	Package related mechanical tests - Shock, Vibration, Accel, salt, seal, lead finish adhesion, lid torque, thermal shock, moisture resistance
Group E	Radiation Tests

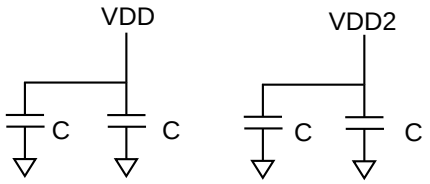
Honeywell delivers products that are tested to meet your requirements Products can be screened to several levels including Engineering Models and Flight Units. EMs are available with limited screening for prototype development and evaluation testing.

PACKAGING

The 512K x 32 SRAM is offered in an 86-lead flat pack. This package is constructed of multi-layer ceramic (Al2O3) and contains internal power and ground planes. The package lid material is Kovar and the finish is in accordance with the requirements of MIL-PRF-38535. The finished, packaged part weighs 6.6 grams.

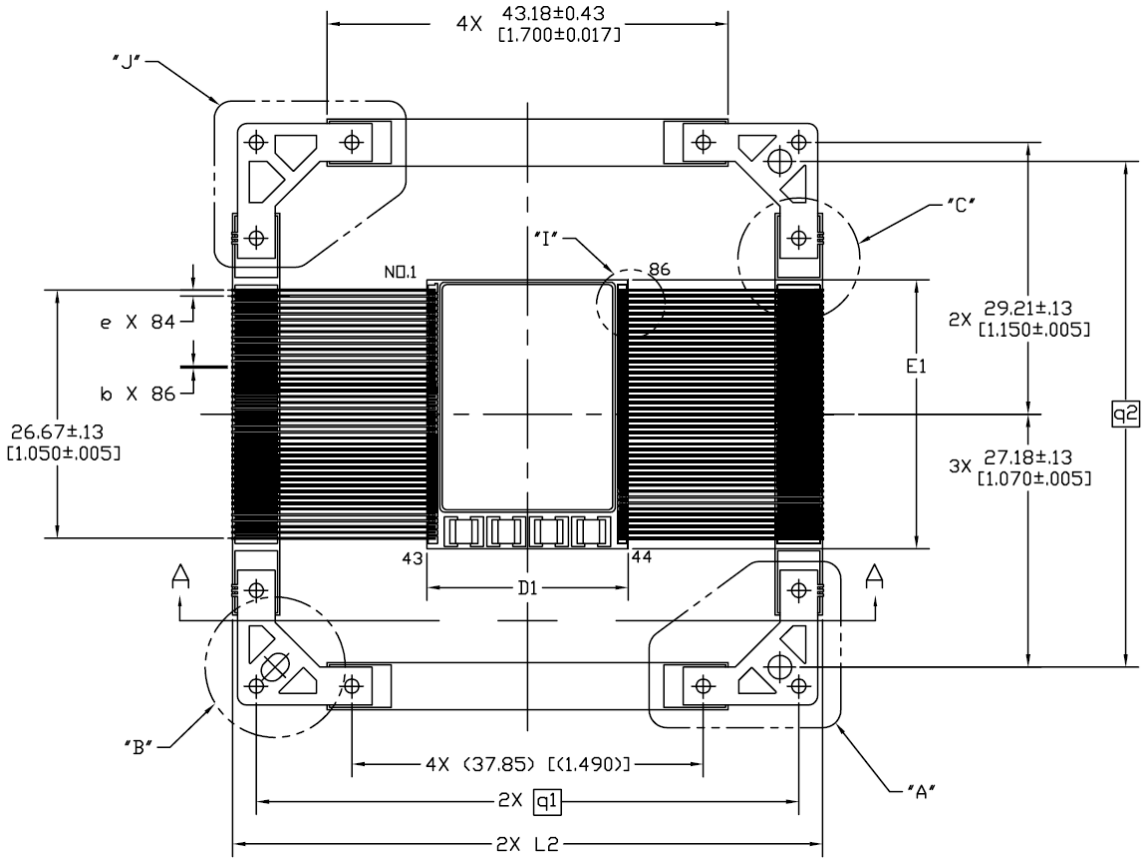
VDD AND VDD2 CAPACITORS

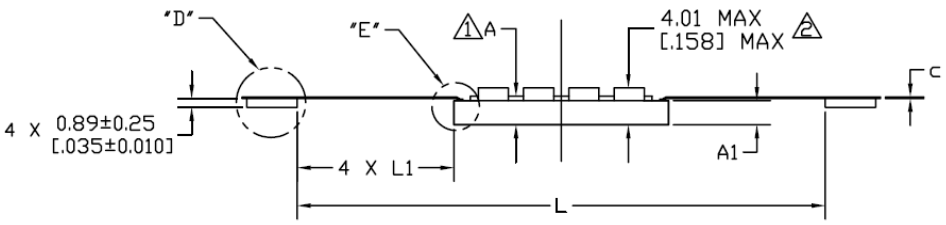
The SRAM has four external capacitors as power supply decoupling on VDD and VDD2. These are adhered to the package using epoxy (conductive on capacitor leads and non-conductive on the body) during assembly.



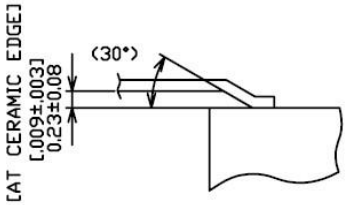
C = 0.1µF ± 10%

PACKAGE OUTLINE

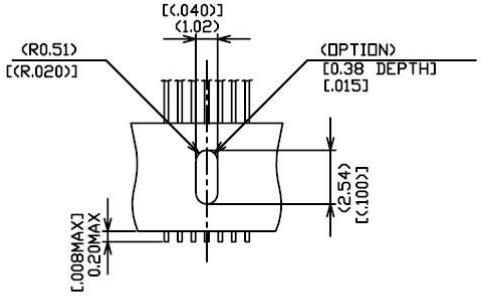




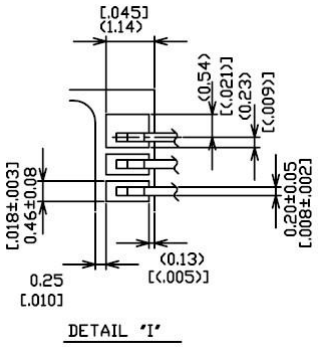
SECTION A-A



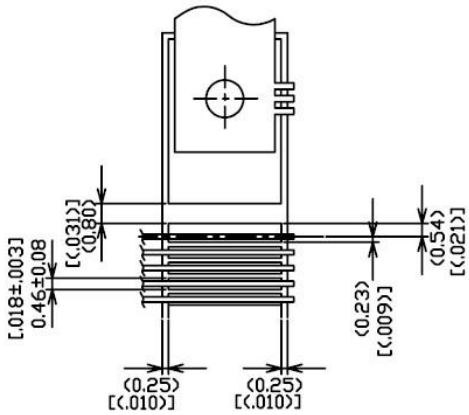
DETAIL "E"



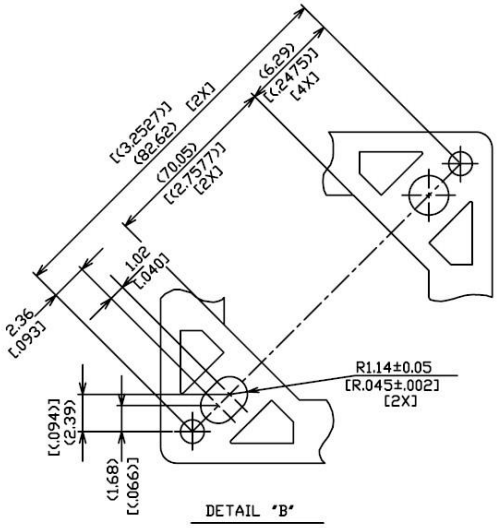
DETAIL "D"
(BOTTOM VIEW)



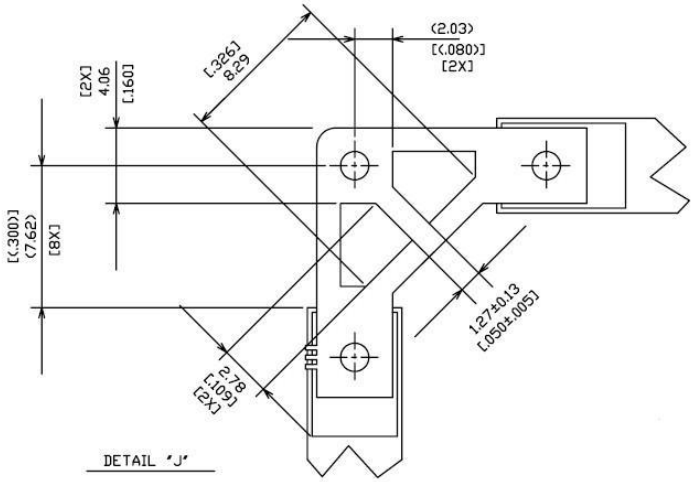
DETAIL "I"



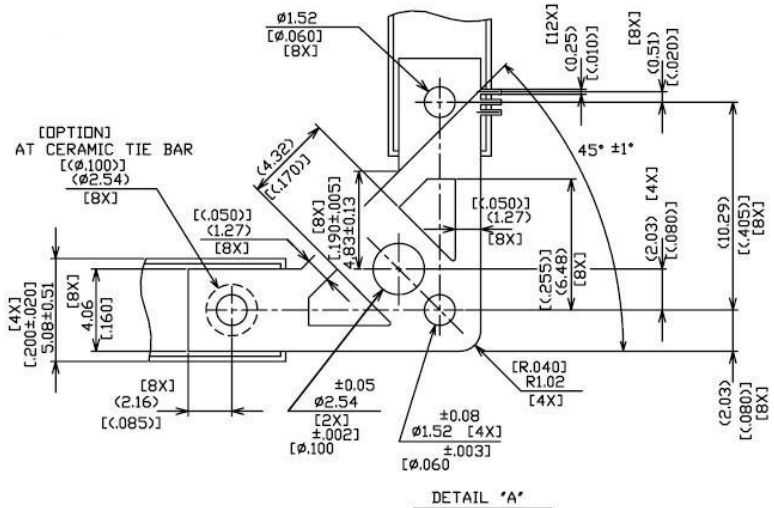
DETAIL "C"



DETAIL "B"



DETAIL "J"

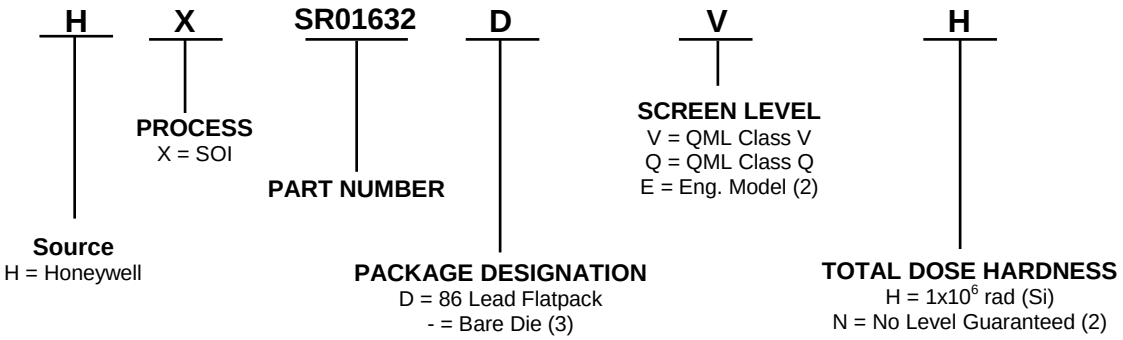


DETAIL "A"

SYMBOL	COMMON DIMENSIONS (MILLIMETERS)			COMMON DIMENSIONS (INCHES)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.59	2.87	3.15	.102	.113	.124
A1	2.19	2.44	2.69	.086	.096	.106
b	0.15	0.20	025	.006	.008	.010
c	0.125	0.15	0.20	.005	.006	.008
D1	21.47	21.67	21.87	.845	.853	.861
e	.585	.635	.685	.023	.025	.027
E1	28.63	28.91	29.19	1.127	1.138	1.149
L	52.83	---	---	2.080	---	---
L1	---	15.835	---	---	.623	---
L2	62.99	63.50	64.01	2.480	2.500	2.520
q1	58.29	58.42	58.55	2.295	2.300	2.305
q2	54.23	54.36	54.49	2.135	2.140	2.145

HXSR01632

ORDERING INFORMATION (1)



(1) Orders may be faxed to 763-954-2051. Please contact our Customer Service Representative at 1-763-954-2474 for further information.
(2) Engineering Device Description: Parameters are tested -55°C to 125°C, 24 hour burn-in, no radiation guaranteed.
(3) Bare die do not receive any reliability screening.

STANDARD MICROCIRCUIT DRAWING

The QML Certified SRAM can also be ordered under the SMD drawing 5692-08203.

FIND OUT MORE

For more information about Honeywell's family of radiation hardened products and technology, visit www.honeywell.com/radhard.

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