LatticeXP2 Standard Evaluation Board

User's Guide

February 2010
Revision: EB29_01.5

Introduction

The LatticeXP2™ Standard Evaluation Board provides a convenient platform to evaluate, test and debug user designs. The board features a LatticeXP2-17 FPGA in a 484 fpBGA package. The LatticeXP2 I/Os are connected to a rich variety of interfaces described later in this document.

This document (including the schematics in the appendix) describes LatticeXP2 Standard Evaluation Boards marked as Rev 000. This marking can be seen on the etching on the back of the printed circuit board, under the Lattice Semiconductor logo.

The LatticeXP2 is a third-generation non-volatile FPGA device. It combines a Look-up Table (LUT) based FPGA fabric with Flash Non-volatile cells in a flexiFLASH™ architecture. The flexiFLASH approach provides benefits such as instant-on, small footprint, on chip storage with FlashBAK™ embedded block memories and Serial TAG memory and design security. The LatticeXP2 also supports live updates with TransFR™, 128-bit AES Encryption and Dual-Boot technologies. The LatticeXP2 devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O and enhanced sysDSP™ blocks.

For a full description of the LatticeXP2 FPGA, see the Lattice website for data sheets, technical notes, technology summaries and more: www.latticesemi.com/products/xp2.

Some common uses for the LatticeXP2 Standard Evaluation Board include:

- A Single Board Computer system
- An analog-to-digital, and digital-to-analog mixed signal source/sink
- A platform for evaluating the Input/Output (I/O) characteristics of the FPGA

Features

Key features of the LatticeXP2 Standard Evaluation Board include:

- LatticeXP2 FPGA 484-pin fine pitch Ball Grid Array device (LFXP2-17E-6F484C)
- Single printed circuit board solution
- Eight LEDs for visual feedback
- Seven-segment LED
- Eight-position switch input
- General purpose push buttons
- SRAM memory for microprocessor applications
- Compact Flash connector for adding peripherals
- RS232 DB9 Female connector
- LCD connector with backlight and contrast controls
- IEEE 1149.1 JTAG programming/boundary-scan interface
- Built-in USB download for use with ispVM® software
- Built-in power supply operating from a 5V DC input
- Power supply manager for testing supply sequencing
- Selectable voltage for bank 6 I/O
- Replaceable oscillator for reference clocks
- SMA connectors to LatticeXP2 clock input/general purpose I/O pins
- 100mil center-center test point grid

Other items included with this board:

- USB Cable (for programming)
- AC adapter (5V DC output, international AC input)

Additional Resources

Additional resources for this board can be downloaded from the web at www.latticesemi.com/boards. Navigate to the appropriate evaluation board to find items such as; updated documentation, software, sample designs and demos, and more. We will continue to add resources to this web page. If you wish to be notified when additional resources are available, click the **subscribe to page updates** icon at the top-right of the screen.

General Description

The heart of the board is the LatticeXP2 non-volatile FPGA. The board provides several different interconnections and support devices that permit it to be used for a variety of purposes. The SRAM, RS232, and CF connector are useful for microprocessor evaluation functions. The CF connector is also useful for expansion purposes. It provides the ability to add storage, or communication capabilities to the board.

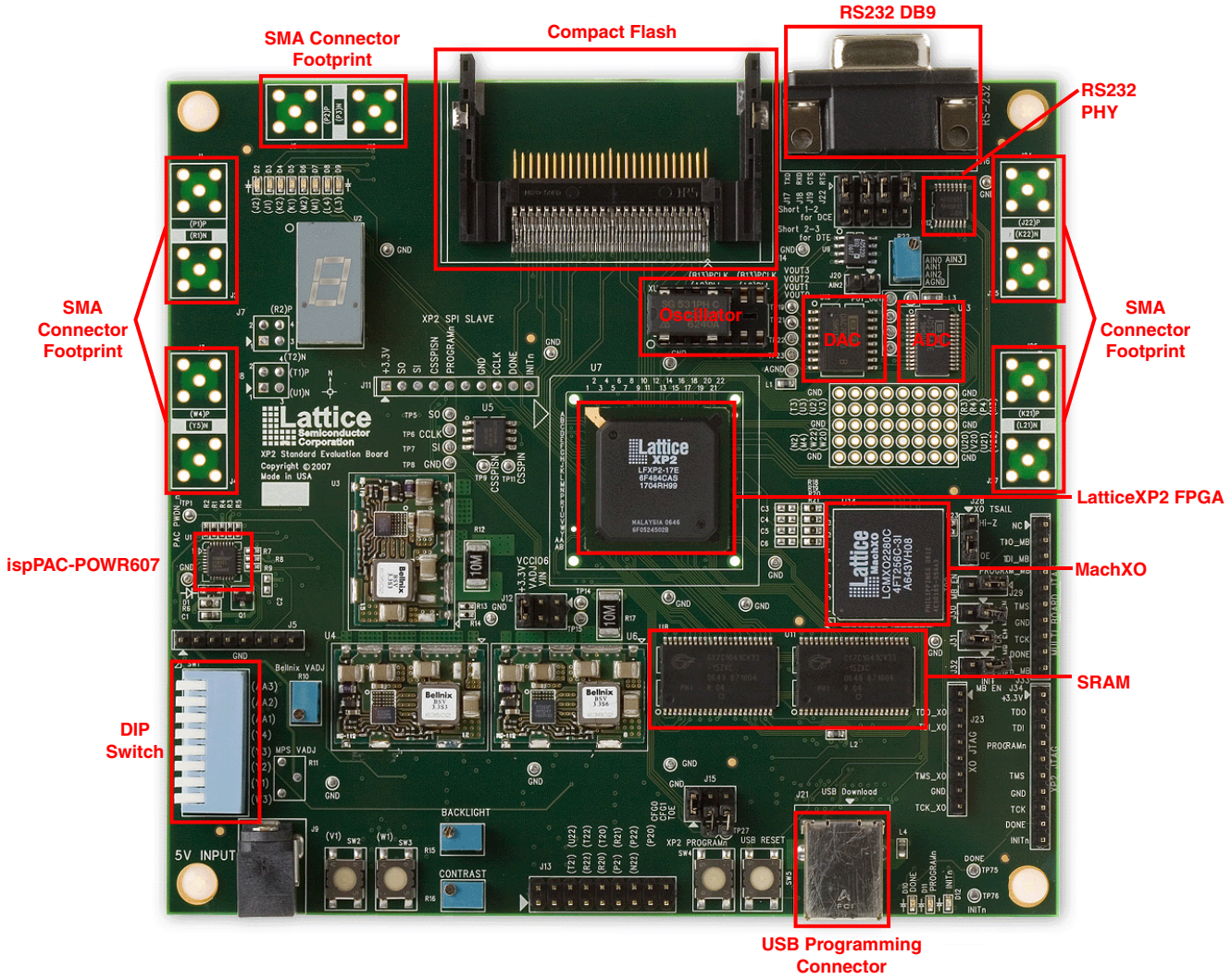
Other features on the board are useful for evaluation of the LatticeXP2 FPGA or development of more complex solutions. The A/D, D/A, and digital potentiometer are helpful for mixed signal applications. SMA connections can be used for the evaluation of high-speed differential signals, and protocols. (*Note: the SMA connectors are not populated by default, but SMA connector footprints are available*). The SPI memory showcases the failsafe capabilities of the LatticeXP2.

The board also acts as a showcase for the small, cost effective ispPAC®-POWR607 Power Manager device. The ispPAC-POWR607 is a programmable device useful for safely managing the power supply system on the board. It can be used to sequence and monitor the voltages on the LatticeXP2 Standard Evaluation Board.

Functional Description

The LatticeXP2 Standard Evaluation Board is comprised of several primary functional blocks as shown in Figure 1. In the descriptions below, locations of components and board features are described relative to a compass symbol placed adjacent to the Lattice Semiconductor Corp. logo. For example, the 8-position DIP switch is on the southwest corner of the board, and the RS232 DB9 connector is on the northeast corner of the board.

Figure 1. LatticeXP2 Standard Evaluation Board



Power Supply

The LatticeXP2 Standard Evaluation Board features a single coaxial input connector to apply power. The coaxial connector is located at the southwest side of the board. A 5V DC source must be applied to power the board.

The 5V input voltage is used to power the ispPAC-POWR607 Power Manager device (U1). The input voltage is regulated down with a zener diode and a transistor. The Power Manager uses this supply rail to boot and run a power up sequence. While the LatticeXP2 does not require any specific order for the voltage rails to be applied, the Power Manager can be used to try a wide variety of sequence options.

The Power Manager controls the enable inputs of three Bellnix BSV-m DC/DC converters. The Bellnix BSV-m is a point-of-load power supply. Each point-of-load supply is placed physically near the DC load. In this case the DC load of interest is the LatticeXP2 FPGA. There are three Bellnix converters on the LatticeXP2 Standard Evaluation Board. One supplies the LatticeXP2 core voltage, which is 1.2V. Another supplies the VCCAUX, VCCIO1/2/3/4/5/7, and all other 3.3V logic on the board. The third converter is adjustable from 1.1V to 2.5V and can be used to power VCCIO6.

The ispPAC-POWR607 is pre-programmed to initialize the power system in a specific order. The order is arbitrary, and is not a power-sequencing guideline for the LatticeXP2. The ispPAC-POWR607 starts by turning on the 1.2V core voltage. It does not turn on any other supply on the board until the 1.2V supply reaches a programmed thresh-

old. Once the 1.2V supply rail is stable, the Power Manager turns on the 3.3V rail. Once again it waits for the 3.3V supply rail to stabilize before performing any other action.

The Power Manager, having detected both the 1.2V and 3.3V supplies as stable, turns on the adjustable supply. Since the adjustable supply is not critical to the operation of the board the Power Manager does not wait for it to stabilize.

After the board is fully powered, the ispPAC-POWR607 monitors for power-down requests – pin IN1 for a high-going transition. When IN1 is pulled above V^{th} the Power Manager de-asserts the enable pins on all of the DC conversion devices, effectively powering the board down. The Power Manager continues to monitor the IN1 input, and when it is pulled below V^{th} it restarts the board in the same order as described earlier.

U3, U4, and U6, once enabled by the ispPAC-POWR607, supply all power to the board. Adjacent to U3 and U6 are current sense resistors. These are intended to permit the measurement of the current flowing from each of the power supplies. The current sense resistors are 10mOhm in value.

Table 1. LatticeXP2 Current Sense Resistors

Resistor	Voltage Supply
R12	Vcore
R17	VCCAUX, VCCIO 1/2/3/4/5/7

The LatticeXP2 Standard Evaluation Board also permits the voltage on VCCIO6 to be changed. Using a jumper on J12 controls the voltage applied to VCCIO6. The voltages that can be supplied are shown in Table 2.

Table 2. LatticeXP2 IO Voltage Selection

Jumper Block J12	VCCIO6 Voltage
1-2	User input from TP14/TP15
3-4	VAdj from U4 (1.1V-2.5V). Use R10 to adjust the output.
5-6	3.3V

Programmability

There are three programmable devices on the board. Of primary interest for the FPGA user is the LatticeXP2. However, the ispPAC-POWR607 Power Manager, and the MachXO™2280 are also important to the overall operation of the board.

USB Download Cable

The evaluation board has a download cable built in. The components for the built-in download cable are located in the southeast corner of the board. The built-in cable consists of a USB Type-B connector, a USB microcontroller, and a MachXO device.

To use the built-in download cable, simply connect a standard USB cable (included) from J21 to your PC (with ispVM System installed). The USB Hub on the PC will detect the addition of the USB Function making the built-in cable available for use with Lattice's ispVM System software.

The USB cable is connected in parallel to J34. J34 is a 1x10 100mil header that is provided for use with an external Lattice download cable (available separately). A Lattice parallel port or USB download cable can be attached to the board using J34.

Use of the built-in cable must be mutually exclusive to use of an external download cable. When using an external download cable the jumper on J28 must be moved to shunt pins 1-2. This tri-states the MachXO device, preventing it from interfering with the external download cable.

Note: The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD® Cable or USB cable. Always connect an ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeXP2 FPGA and render the board inoperable.

LatticeXP2 JTAG Access

The default configuration of the LatticeXP2 Standard Evaluation Board connects the built-in JTAG cable/J34 to only access the LatticeXP2 FPGA. The serial output from the USB cable/J34 is routed directly to the serial input of the LatticeXP2 FPGA. The serial output from the LatticeXP2 is routed to J29. A jumper on J29 directs the serial output of the LatticeXP2 back to the USB cable/J34. This is the factory default configuration and is expected to be the primary JTAG mode for most users.

The board can also be configured to access the LatticeXP2 FPGA, and a chained evaluation board. A 1x10 cable (not supplied) can be connected locally to J33 and the opposite end of the cable can be attached to another system that has a JTAG chain.

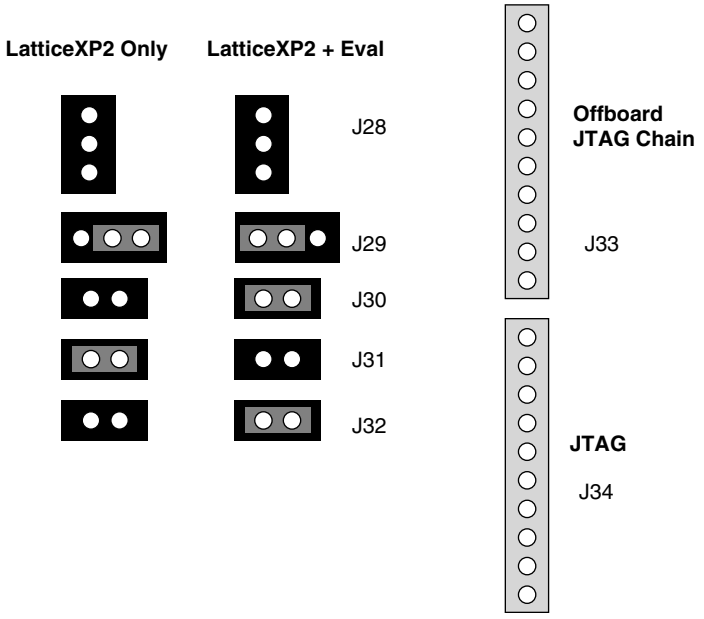
Chaining the LatticeXP2 Standard Evaluation Board with another board is accomplished by changing the routing of the TDI/TDO/TMS/TCK I/Os. Jumpers J29, J30, J31, and J32 determine how the TDI/TDO chain and TMS pins behave.

Table 3. LatticeXP2 Single/Multi-Board Configuration

Jumper Block	LatticeXP2 Board Only	LatticeXP2 Board Plus Off-board JTAG Chain
J29	1-2	2-3
J30	Open	1-2
J31	1-2 (1K pull-down resistor on TCK)	1-2 (off-board chain does not pull TCK to GND). Open (off-board chain pulls TCK to GND).
J32	Open	1-2

J31, when shorted, adds a pull-down resistor to the TCK signal. Only one chained evaluation board should have a pull-down on TCK.

Figure 2. Single/Multi-Board Jumpers



The JTAG port is used for programming the LatticeXP2 and can also be used for programming the off-chip SPI PROM. The LatticeXP2 FPGA has several modes it can use to get configuration data. Available sources for configuration data are:

- JTAG programming
- On-chip Flash PROM (with automatic failsafe)
- Off-chip SPI PROM (LatticeXP2 fetches configuration data)
- Off-chip SPI interface (LatticeXP2 receives configuration data from a master)

The JTAG interface to the LatticeXP2 provides several methods to program the LatticeXP2 and devices attached to the LatticeXP2. JTAG programming can be used to program the LatticeXP2 in SRAM mode (volatile). It can also be used to program the on-chip LatticeXP2 Flash memory (non-volatile). It also provides the ability to program an attached SPI PROM (U5). The SPI PROM is used for storing failsafe configuration data.

ispPAC-POWR607 JTAG Access
The ispPAC-POWR607 Power Manager comes from the factory with a default power sequence. It may be desired for evaluation purposes to try other power sequences. Connector J5 is the access point for the ispPAC-POWR607 JTAG I/O. See the Power Supplies and Supply Control section below for the details of using the ispPAC-POWR607.

SPI Slave Connection
The LatticeXP2 has configuration pins that define how the device will find a non-volatile bitstream to configure itself. In most cases the configuration pins will be set to have the LatticeXP2 act as a master device and actively read data from its internal Flash or from the attached SPI PROM.

The LatticeXP2 can also be configured to act as a slave device, and accept bitstream data from an external master. The master can be connected to either the JTAG port, or it can be connected to the SPI interface. The LatticeXP2 Standard Evaluation Board provides a 1x10 header, J11, that permits an off-chip SPI master to program the LatticeXP2 FPGA.

MachXO JTAG Connection
The MachXO's primary function is to be the USB download cable interface for the LatticeXP2. However, the MachXO is a PLD, and has some connections to the LatticeXP2. It is possible, therefore, to use the LatticeXP2 and the MachXO together. The MachXO can be reprogrammed with custom logic using connector J23. The factory program for the MachXO is available on-line to restore the device if needed.

LatticeXP2 and Support Interfaces

The LatticeXP2 Standard Evaluation Board provides a variety of support features for evaluating the performance and functionality of the LatticeXP2 FPGA. A FPGA can be used for a large number of different applications. The LatticeXP2 Standard Evaluation Board attempts to balance the ability to test I/O and the ability to use interesting/common logic functions.

The evaluation board has features designed to make it easier to locate resources on the board and resources connected to the FPGA.

- Devices are numbered in a consistent fashion. Each device starts at reference designator '1' in the northwest corner of the board (i.e. R1, C1, U1, L1...). The component number increases by one in a columnar fashion (i.e. southward). When the south edge of the board is reached, the count resumes slightly east, and at the north side of the board. Thus, the highest numbered components will always be in the southeast corner of the board. This same numbering sequence is applied to the secondary side of the printed-circuit board.
- Adjacent to most of the switch inputs, LED outputs, SMA connectors, and test points is the alphanumeric position of the pin on the LatticeXP2 FPGA. For example: next to the SMA connector J1, in the silkscreen, is the designator (P1). Thus LatticeXP2 (U7) pin P1 is connected to the center post of J1.
- SMA connectors have an open white rectangle area near them denoting the positive side of a matched pair. The negative side of the matched pair has a solid filled white rectangular area.

Push-Buttons and Status LEDs

There are four push-buttons and three LEDs on the south edge of the evaluation board. Switch SW2 and SW3, the westernmost, are routed to generic LatticeXP2 I/Os. One of these buttons typically acts as a reset switch, providing a reset pulse to logic inside the LatticeXP2.

SW4, which is near the USB connector, is tied to the LatticeXP2's PROGRAMn input. Pressing this switch will cause the LatticeXP2 to reprogram itself, as long as CFG0 is set to V_{IL}.

SW5 is adjacent to SW4 and is the reset button for the built-in USB download cable. Pressing this button will cause the USB cable to re-enumerate with the USB hub.

In the southeast corner of the board are three status LEDs. These indicate the state of the LatticeXP2's Done, INITn, and PROGRAMn I/O pins. During normal operation the Done and the INITn LEDs will illuminate.

Global Output Enable

The LatticeXP2 has a global output enable control. The GOE is routed to J15, and the factory default setting on J15 is to enable the LatticeXP2 outputs. The jumper on J15 can be moved from the default setting (open) to disable (tri-state) all of the LatticeXP2 I/Os.

Table 4. Global Output Enable

Jumper Block J15	Output Enable State
Shunt	Outputs disabled (tri-state)
Open*	Outputs enabled

Prototype Grid

The board provides a small 100mil center-center prototype area. The prototype area has a set of plated through-holes in a 5x8 pattern. There are a total of 16 I/O pins connected in the prototype area. The topmost row is a series of eight horizontal plated through-holes connected to the ground plane. South of this row is a row of plated through-holes connected to the LatticeXP2 device. The rows alternate GND/signal/GND/signal/GND from north to south.

Some of the plated through-holes are connected to LatticeXP2 Bank 6. It is possible to modify the I/O voltage on Bank 6 using J12.

Table 5. Testpoint Connections

Bank #	LatticeXP2 I/O	Bank #	LatticeXP2 I/O
6	T3	6	U3
6	U2	6	V3
6	R3	6	R4
6	P4	6	M3
6	N2	6	M4
3	W22	3	W20
3	U20	3	V20
3	U21	3	V22

LED Displays

In the northwest corner of the board is a set of eight green 0603 form factor LEDs. These LEDs are connected to IO pins dedicated to driving the LEDs. Table 6 shows the LatticeXP2 I/O pins that control each LED. The LEDs illuminate when the corresponding I/O is driven to V_{OL}.

Table 6. LED Pin Assignments

LED	LatticeXP2 I/O
D2	J2
D3	J1
D4	K2
D5	K1
D6	M2
D7	M1
D8	L4
D9	L3

In addition to the discrete chip LEDs there is a single 7-segment display. Like the discrete LEDs, a V_{OL} level will cause a segment to illuminate. The segment order is defined in the Lumex LDS-A304RI Data Sheet.

Table 7. 7-Segment LED Pin Assignments

Segment	LatticeXP2 I/O
A	J4
B	H4
C	F4
D	E4
E	E3
F	H3
G	G3
DP	F3

Switches

The evaluation board provides a set of eight simple toggle switches at the southwest edge of the board. The silk-screen calls out the alphanumeric location of the I/O on the FPGA. The switch, when in the up position, is pulled to VCCIO6 through a 10K resistor. When in the down position, the switch is tied to ground.

Table 8. SW1 Switch Pin Assignments

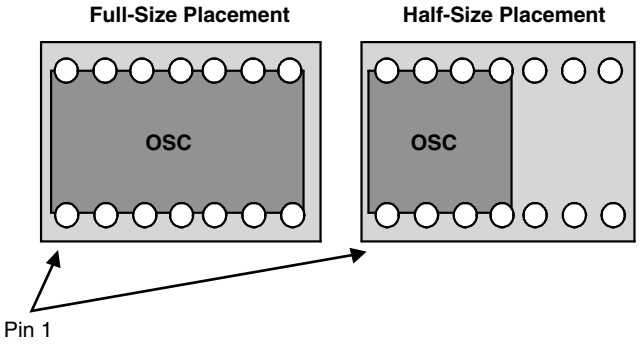
Switches	LatticeXP2 I/O
SW1-0	AA3
SW1-1	AA2
SW1-2	AA1
SW1-3	Y4
SW1-4	Y3
SW1-5	Y2
SW1-6	Y1
SW1-7	W3

Oscillator and Clock Inputs

FPGA designs are almost without exception created with logic synchronous to some reference frequency. The LatticeXP2 Standard Evaluation Board provides a built-in oscillator that provides a reference frequency for synchronous FPGA logic. Reference frequencies can be applied to other LatticeXP2 clock inputs as well.

The LatticeXP2 board provides a low-voltage (3.3V) DIP oscillator. The oscillator is installed in a 14-pin DIP socket. The socket permits the use of either a half-size or full-size DIP oscillator.

Figure 3. Oscillator Positions



The output from the oscillator is routed to two series resistors. One of the series resistors is connected to a primary clock input pin. The other resistor is connected to a PLL input pin. It is important to mention that DIP socket pin 8 is shorted to pin 11, so it is not possible to input two different clock frequencies from the socket. In order to provide a frequency on the primary clock input that is different from the PLL clock input it is necessary to remove one of the two series termination resistors, and add a temporary modification to inject an electrically isolated clock signal.

Differential/50 Ohm Input/Output

The LatticeXP2 Standard Evaluation Board provides connections to differential I/O pins. The circuit board traces for these connections are nominally 50-ohm impedance. Some of the differential I/O pins are inputs to primary or PLL clock drivers. If the built-in oscillator in socket XU1 does not provide the right kind of input clock the SMA connectors listed in Table 9 can be used to provide additional reference clock frequencies.

Table 9. Differential/50 Ohm Trace Pin Assignments

Connector Pair	LatticeXP2 I/O		Clock Input
J1	P1		N
J2	R1		N
J3	Physical connection	T1	Y (P)
	Silkscreen text	W4	
J4	Physical connection	U1	Y (N)
	Silkscreen text	Y5	
J6	P2		N
J10	P3		N
J7	T2 (3) / R2 (4)		N
J8	Physical connection	Y5 (3) / W4 (4)	N
	Silkscreen text	U1 (3) / T1 (4)	
J24	J22		Y (P)
J25	K22		Y (N)
J26	K21		Y (P)
J27	L21		Y (N)

Power Supplies and Supply Control

The LatticeXP2 Standard Evaluation Board operates from a 5V DC input voltage. The input voltage is supplied via J9, a coaxial DC input jack. The following components operate using the 5V input:

- ispPAC-POWR607 Power Manager
- Bellnix DC/DC converters

- LCD Display, contrast and backlight controls

ispPAC-POWR607

The ispPAC-POWR607 is a low-cost power management chip that is used on the LatticeXP2 Standard Evaluation Board to turn on the DC/DC converters in a controlled sequence. The LatticeXP2 FPGA does not require voltages to be applied in a predefined sequence. The ispPAC-POWR607 permits testing any startup sequence.

The ispPAC-POWR607 operates over a much looser DC input range than most 3.3V logic. It is capable of running from an input supply less than 3.96V and greater than 2.64V. This allows the DC regulation from the 5V input to be performed with loose tolerances and inexpensive components.

The evaluation board uses a zener diode and a transistor to regulate the 5V input. The ispPAC-POWR607 is the first device on the board to have a stable supply voltage. Using this stable supply voltage it is able to turn on other supplies in a controlled sequence. The sequence is reprogrammable. Reprogramming is done using Lattice Semiconductor's PAC Designer® software, available from www.latticesemi.com/pac-designer. The source code for the factory default program is available on the Lattice web site at www.latticesemi.com/boards. Navigate to the appropriate page for this board and choose "Design Files" from the list of available resources.

The ispPAC-POWR607 sequence programmed from the factory starts by enabling the 1.2V DC converter. The Power Manager waits for the 1.2V supply rail to reach 95% of its threshold voltage before turning on any other supply. The next voltage supply to be enabled is the 3.3V rail. Once again the Power Manager waits for this rail to reach 95% threshold. When the 3.3V rail reaches threshold, the adjustable voltage rail is enabled, but the Power Manager does not wait for it to reach a specified threshold since this rail is an auxiliary supply rail. The next step is for the Power Manager to monitor the PWDN/IN1 input pin. When this pin goes to V_{IH} the Power Manager disables all of the DC/DC converters.

When the IN1 pin returns to V_{IL} the Power Manager starts over as if power had just been applied.

Table 10. ispPAC-POWR607 to LatticeXP2 General Purpose Connections

ispPAC-POWR607 Pin	LatticeXP2 I/O
28	V19
26	P19
23	R19
22	M19
20	M20

Bellnix DC/DC Converters

The 5V rail also supplies power to Bellnix DC/DC converters. The Bellnix converters are point of load (POL) DC supplies. The supplies are mounted close to the LatticeXP2 FPGA in order to increase response time during periods of high current demand.

U3 is solely dedicated to supplying the LatticeXP2 FPGA's core voltage. The 1.2V passes through R12, a 10mOhm current sense resistor. The resistor permits voltage drop measurements to be used to determine how much power is being used by the LatticeXP2.

U5 is an adjustable supply with a range from 1.1V through 2.5V. The voltage from this supply is only routed to J12. J12 is used to configure the I/O voltage used by Bank 6.

U6 is a fixed 3.3V supply. It provides 3.3V to all of the ICs on the board, as well as the LatticeXP2's VCCAUX and VCCIO banks (except Bank 6). The 3.3V provided to VCCAUX and VCCIO pass through R17, a 10 mOhm current sense resistor. This allows for a voltage drop measurement to be taken indicating the amount of current being drawn by the LatticeXP2.

LCD Connector

Connector J13 is a 2x9 100mil center-center header designed to allow the use of LCD displays. The connector provides 5V directly from the DC input (J9). It also has adjustable backlight (R15) and contrast (R16) potentiometer controls. The connector is designed for use with LCD displays such as the Lumex LCM-S02002DSF or LCM-S02002DSR. *Note: Recent Lumex specifications show a 16-pin interface, which corresponds to pins 2-18 on the J13 LCD Connector.*

Table 11. LCD Connections

LCD Pin #	LCD Function		LatticeXP2 I/O
6	RS		U22
7	RW	Physical Connection	T21
		Silkscreen Text	R22
8	E		T22
9	D0	Physical Connection	R22
		Silkscreen Text	R20
10	D1		T20
11	D2	Physical Connection	R20
		Silkscreen Text	P21
12	D3		R21
13	D4	Physical Connection	P21
		Silkscreen Text	N22
14	D5		P22
15	D6	Physical Connection	N22
		Silkscreen Text	—
16	D7		P20

RS232 Interface

The evaluation board provides a RS232 connection for interfacing to equipment with RS232 ports. The RS232 connector is a female DB9 connector, and can be found in the northeast corner of the board. Four 1x3 jumpers are provided on the board to permit reconfiguration of the RX/TX/RTS/CTS connections.

Table 12. RS232 DB9 Pin Assignments

RS232 Signal	Connector	Pin 1-2	Pin 2-3
RX	J18	J16-3	J16-2
TX	J17	J16-2	J16-3
CTS	J19	J16-7	J16-8
RTS	J22	J16-8	J16-7

The LatticeXP2 FPGA is connected to the RS232 DB9 connector using a Max 3232 buffer chip. This buffer permits the LatticeXP2 3.3V I/O pins to be interfaced to the 12V RS232 signaling standard. The LatticeXP2 I/O pins that connect to the RS232 buffer listed in Table 13.

Table 13. LatticeXP2 to RS232 Pin Assignments

RS232 Signal	LatticeXP2 I/O
RX	C21
TX	B22
CTS	B21
RTS	C22

Compact Flash Connector

Connector J14 provides the evaluation board with the ability to interface to 3.3V Type II Compact Flash devices. The FPGA can be programmed to use the various different Compact Flash protocols.

Table 14. Compact Flash Pin Assignments

Connector Pin	LatticeXP2 I/O	Connector Pin	LatticeXP2 I/O
CF0	B12	CF23	D6
CF1	A12	CF24	C6
CF2	A11	CF25	A5
CF3	B11	CF26	C5
CF4	D11	CF27	A4
CF5	C11	CF28	C4
CF6	A10	CF29	A3
CF7	B10	CF30	B3
CF8	E10	CF31	B2
CF9	A9	CF32	B1
CF10	B9	CF33	C3
CF11	D9	CF34	C2
CF12	C9	CF35	C1
CF13	A8	CF36	D4
CF14	B8	CF37	D3
CF15	D8	CF38	D1
CF16	C8	CF39	E1
CF17	A7	CF40	F2
CF18	B7	CF41	F1
CF19	F7	CF42	G2
CF20	C7	CF43	G1
CF21	A6	CF44	H2
CF22	B6	CF45	H1

Mixed Signal Support

The LatticeXP2 Standard Evaluation Board also provides access to some mixed signal interface chips. There are four primary components dedicated to performing mixed signal functions on the evaluation board. These components are:

- 12-bit Analog to Digital Converter
- 12-bit Digital to Analog Converter
- 128-position Digital Potentiometer
- 25K ohm Discrete Potentiometer

The mixed signal devices are all powered from the 3.3V supply. The digital power for these devices comes directly from the 3.3V plane layer. The analog power is supplied via a smaller independent 3.3V plane. The independent plane is supplied from the 3.3V digital plane, but it is filtered with a ferrite bead.

Analog to Digital Converter

The board includes a Burr Brown ADS7842 4 Channel Parallel Sampling Analog to Digital converter.

The analog inputs of the device are connected to four test points. One of these test points is also connected to a 25K ohm discrete potentiometer. The potentiometer permits the input voltage level to vary between 0V to 3.3V at one of the A/D inputs. The remaining three inputs are not connected to any passive or active components. These test points can be used to inject signals meeting your own test requirements.

The digital I/O side of the device connects directly to the LatticeXP2 FPGA. Twelve of the I/O are the data-bus pins, and seven are used to access the internal registers.

Table 15. A/D Connections

A/D Function	LatticeXP2 I/O	A/D Function	LatticeXP2 I/O
AD0	A17	AD10	C19
AD1	B16	AD11	D19
AD2	A16	A0	C20
AD3	B15	A1	A21
AD4	A15	CLK	B20
AD5	C16	BUSYn	A20
AD6	C17	WRn	A19
AD7	D17	CSn	A18
AD8	C18	RDn	B17
AD9	D18		

Digital to Analog Converter

The board also includes a Burr Brown DAC7617 12-bit Serial Input Digital to Analog converter.

The digital interface of the converter is a six-wire control set. Changes to the analog outputs are performed using serial data. A change to an internal register requires 16 clock cycles.

The analog outputs from the D/A are connected directly to individual test points. There is no other logic connected to the analog outputs.

The AIN2 input pin controls the range of the analog outputs. AIN2 is connected to a test-point adjacent to the A/D converter described in the section above. AIN2 is also accessible via J20 pin 2. J20 is a 1x2 pin header that allows the output of the digital potentiometer to be connected to the D/A VREFH input. In order for the digital potentiometer to supply the reference voltage to the D/A converter, J20 must have pins 1-2 shunted. Regardless of the VREFH source voltage, the D/A is able to output a voltage between VREFL (GND) and VREFH (AIN2) in a +/- 1/4096th increment.

Table 16. D/A Connections

Digital to Analog Function	LatticeXP2 I/O
Serial Data In	C12
Clock	D12
Chip Select	A13
Load All	A14
Load Register	C14
Reset	D14

Digital Potentiometer

The evaluation board also provides a 10K ohm digital potentiometer. The potentiometer can be set to one of 128 positions between 0 ohm and 10K ohm. The potentiometer output voltage, which is present on J20 pin 1, can vary from 0V to 3.3V. The potentiometer will be at the midpoint resistance at power up.

Operation of the potentiometer is very simple. Whenever the CS is asserted (V_{IL}) and a clock transition occurs, the output voltage will change up/down by 1/128th. When the UP direction is requested, the output voltage will increase.

Table 17. Digital Potentiometer Connections

POT Function	LatticeXP2 I/O
CLK	D15
Up/Down_n	C15
CS_n	B14

SRAM

The evaluation board provides a quantity of asynchronous SRAM. The memory is organized as 256Kx32 providing 1Mbyte of storage. Asynchronous SRAMs provide a simple electrical and control interface eliminating the need for more complex memory control systems.

Table 18. SRAM Connections

SRAM Function	LatticeXP2 I/O	SRAM Function	LatticeXP2 I/O	SRAM Function	LatticeXP2 I/O
A0	W9	BE2	AA17	D14	AB6
A1	AB10	BE3	AB17	D15	AB5
A2	AA10	CE0	AB2	D16	W14
A3	Y11	CE1	Y14	D17	Y15
A4	W11	WE	Y12	D18	W15
A5	W12	OE	AB12	D19	Y16
A6	AA13	D0	V6	D20	Y17
A7	AA14	D1	W5	D21	W17
A8	AA15	D2	Y6	D22	Y18
A9	AA16	D3	W6	D23	W18
A10	AB16	D4	Y7	D24	Y22
A11	AB15	D5	Y8	D25	AA22
A12	AB14	D6	W8	D26	Y21
A13	AB13	D7	Y9	D27	AA21
A14	AA12	D8	AB9	D28	AA20
A15	AA11	D9	AA8	D29	AB20
A16	AB11	D10	AB8	D30	AB19
A17	AA9	D11	AA7	D31	AB18
BE0	AB4	D12	AB7		
BE1	AB3	D13	AA6		

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
LatticeXP2 Standard Evaluation Board	LFXP2-17E-L-EV	

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
May 2007	01.0	Initial release.
October 2007	01.1	Updated schematic diagrams. Note: The schematic diagrams on previous versions of this document contained erroneous reference designators for the board components.
January 2008	01.2	Updated Differential/50 Ohm Trace Pin Assignments table.
		Updated LCD Connections table.
February 2008	01.3	Updated 7-Segment LED Pin Assignments table.
May 2008	01.4	Corrected LatticeXP2 FPGA part number in the Features list.
February 2010	01.5	Updated SRAM Connections table.

Appendix A. Schematics

Figure 4. LatticeXP2 Standard Evaluation Board

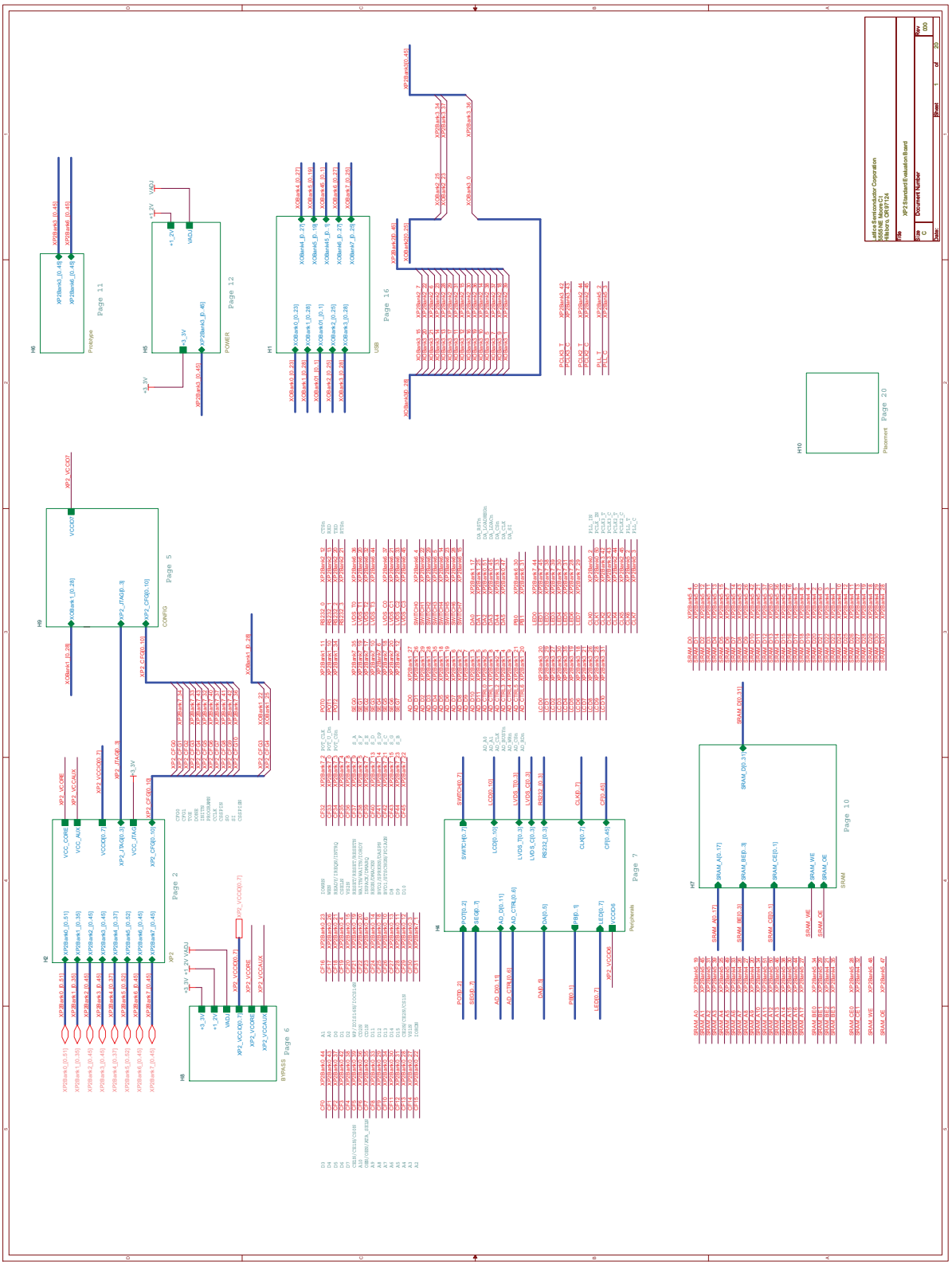


Figure 5. LatticeXP2 Power and Configuration

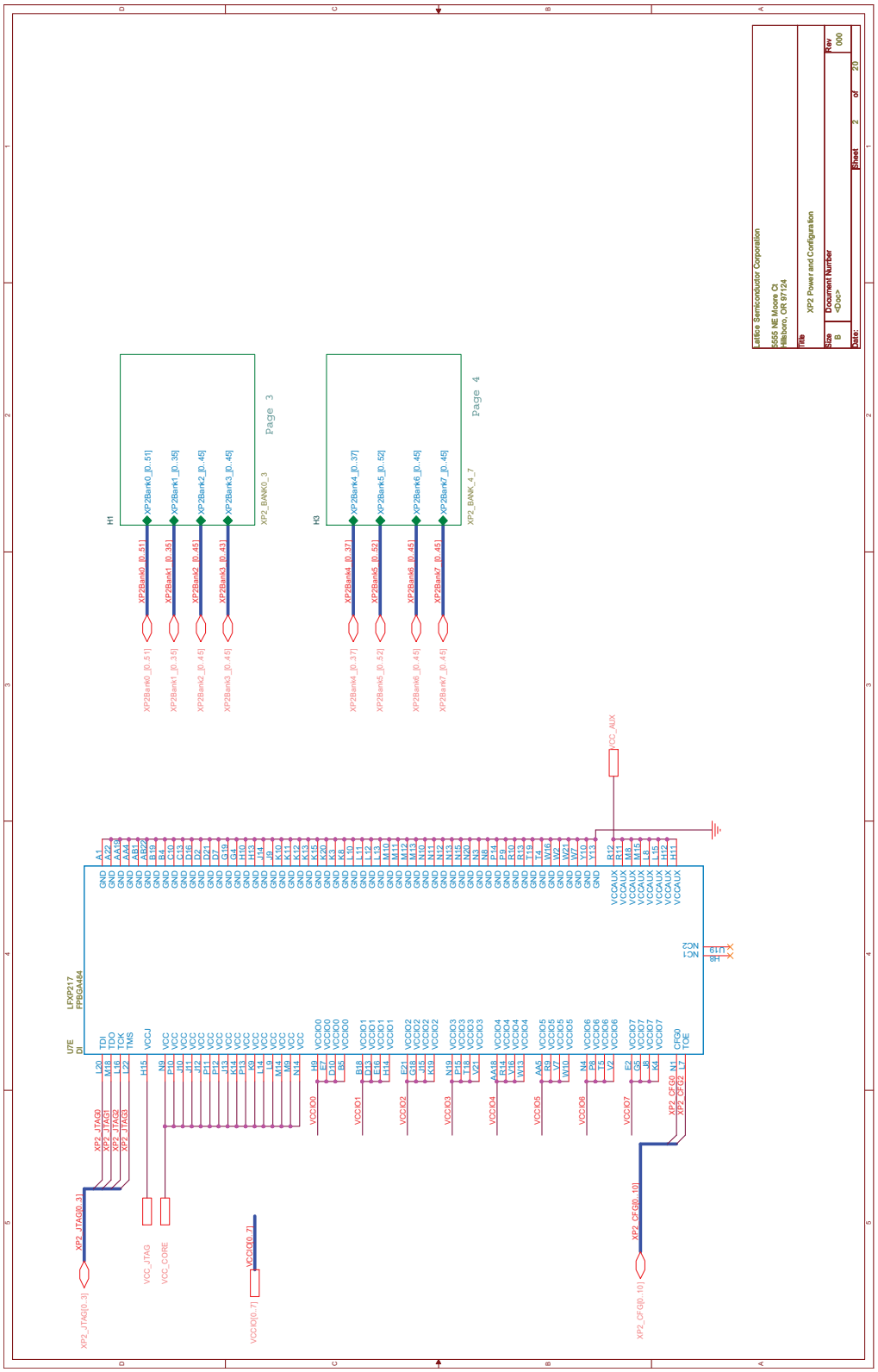


Figure 6. LatticeXP2 Banks 0 to 3

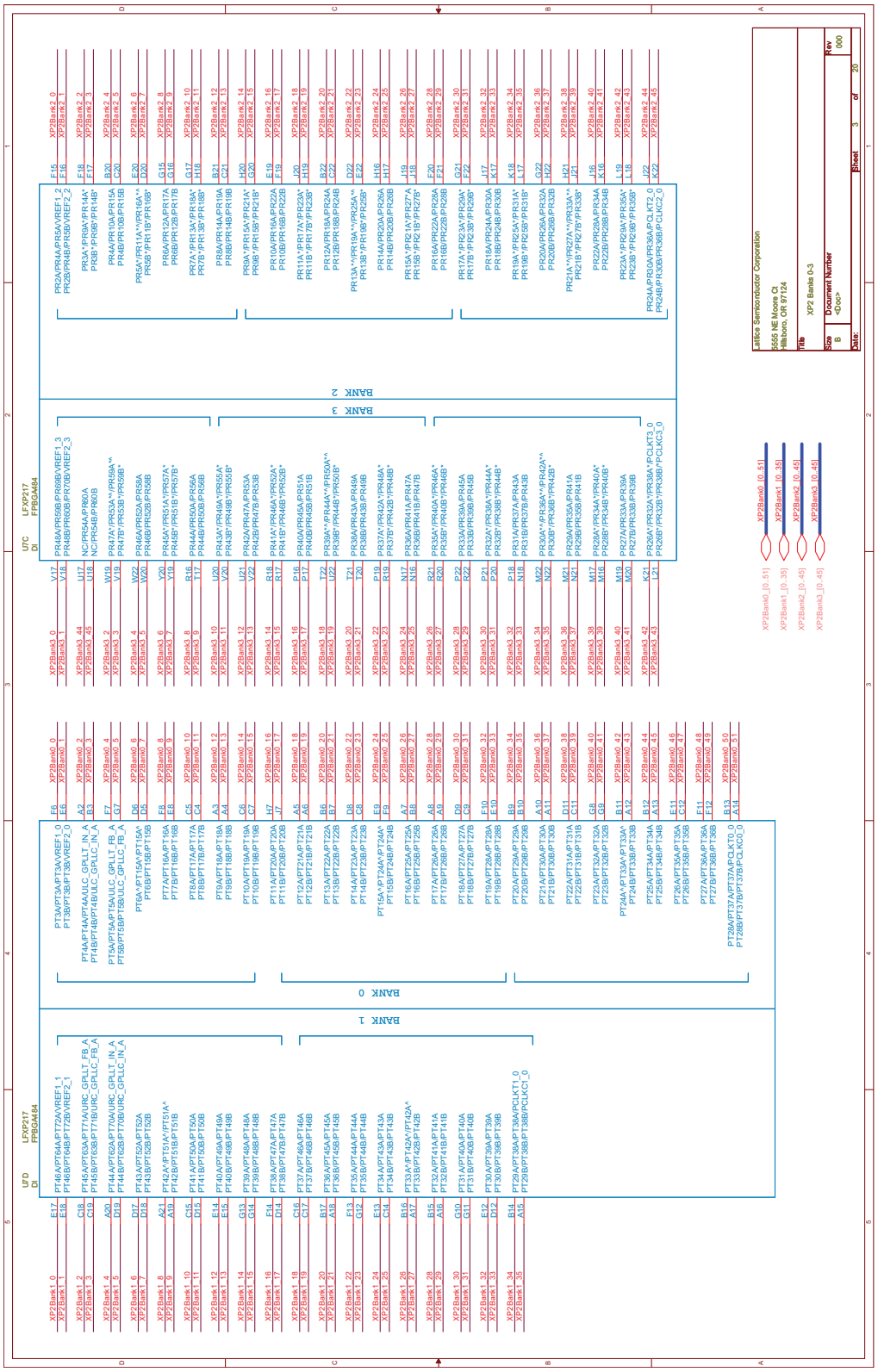


Figure 7. LatticeXP2 Banks 4 to 7

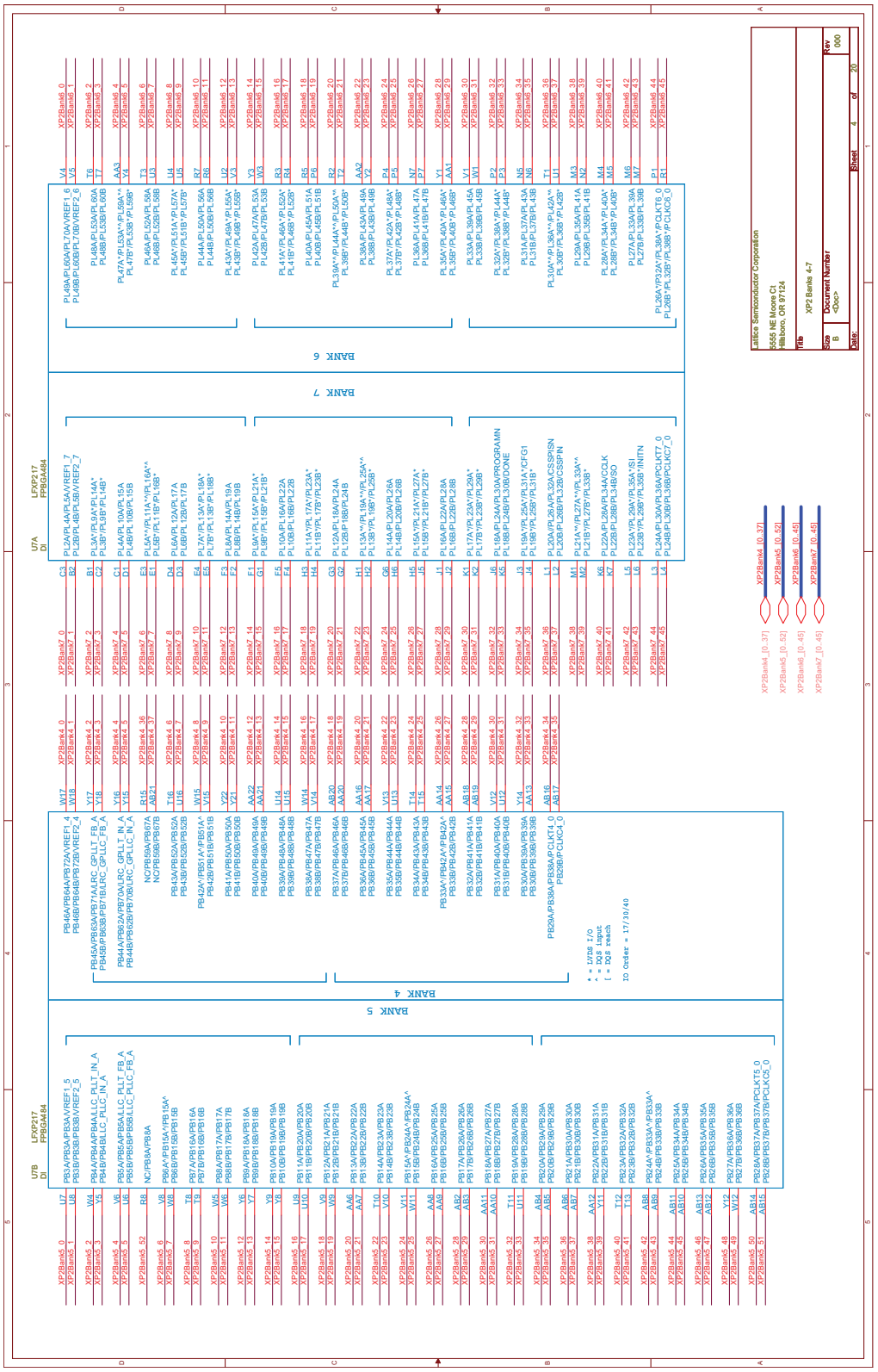


Figure 8. LatticeXP2 Programming Interfaces

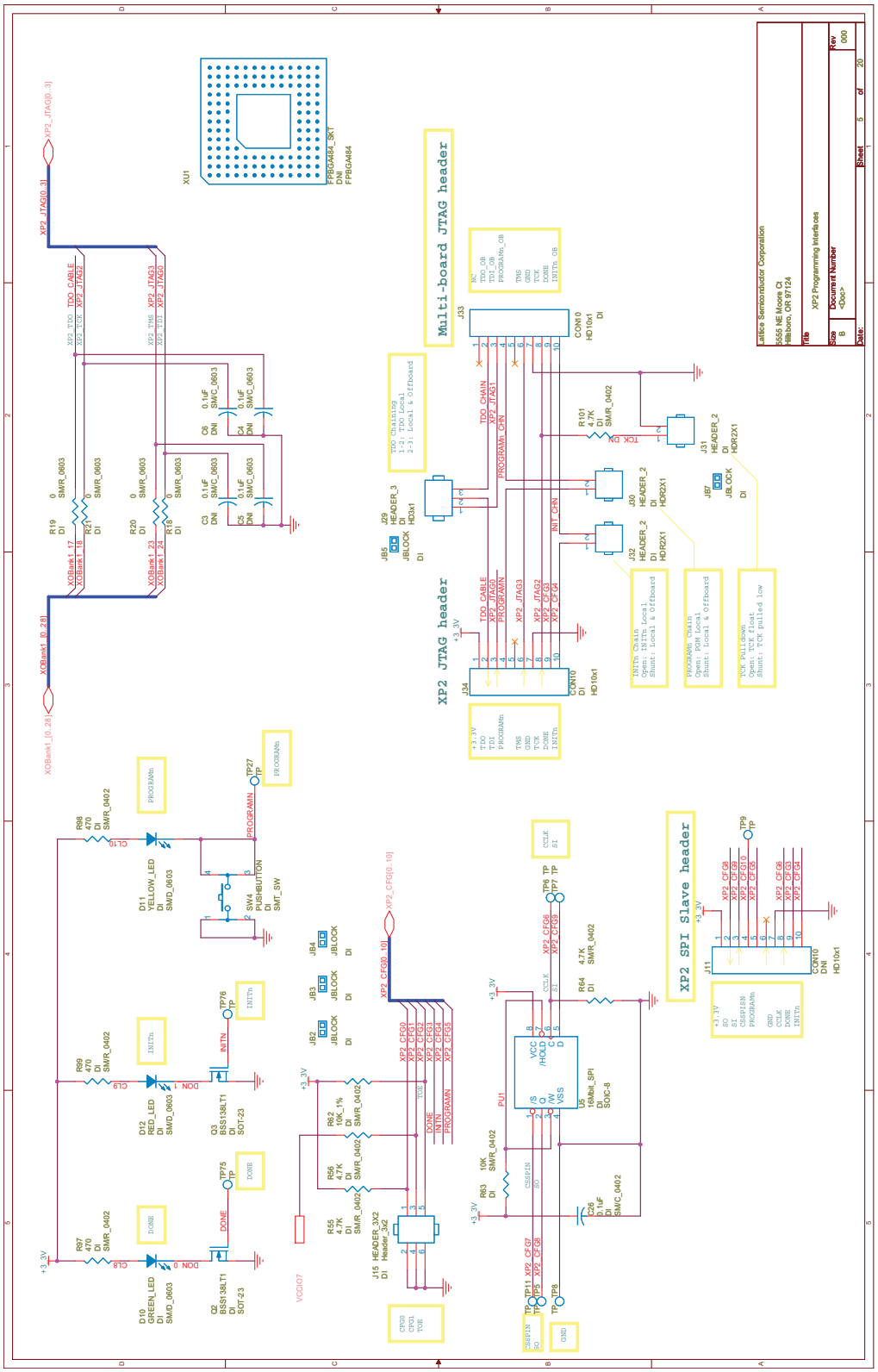


Figure 9. LatticeXP2 Bypass Capacitors

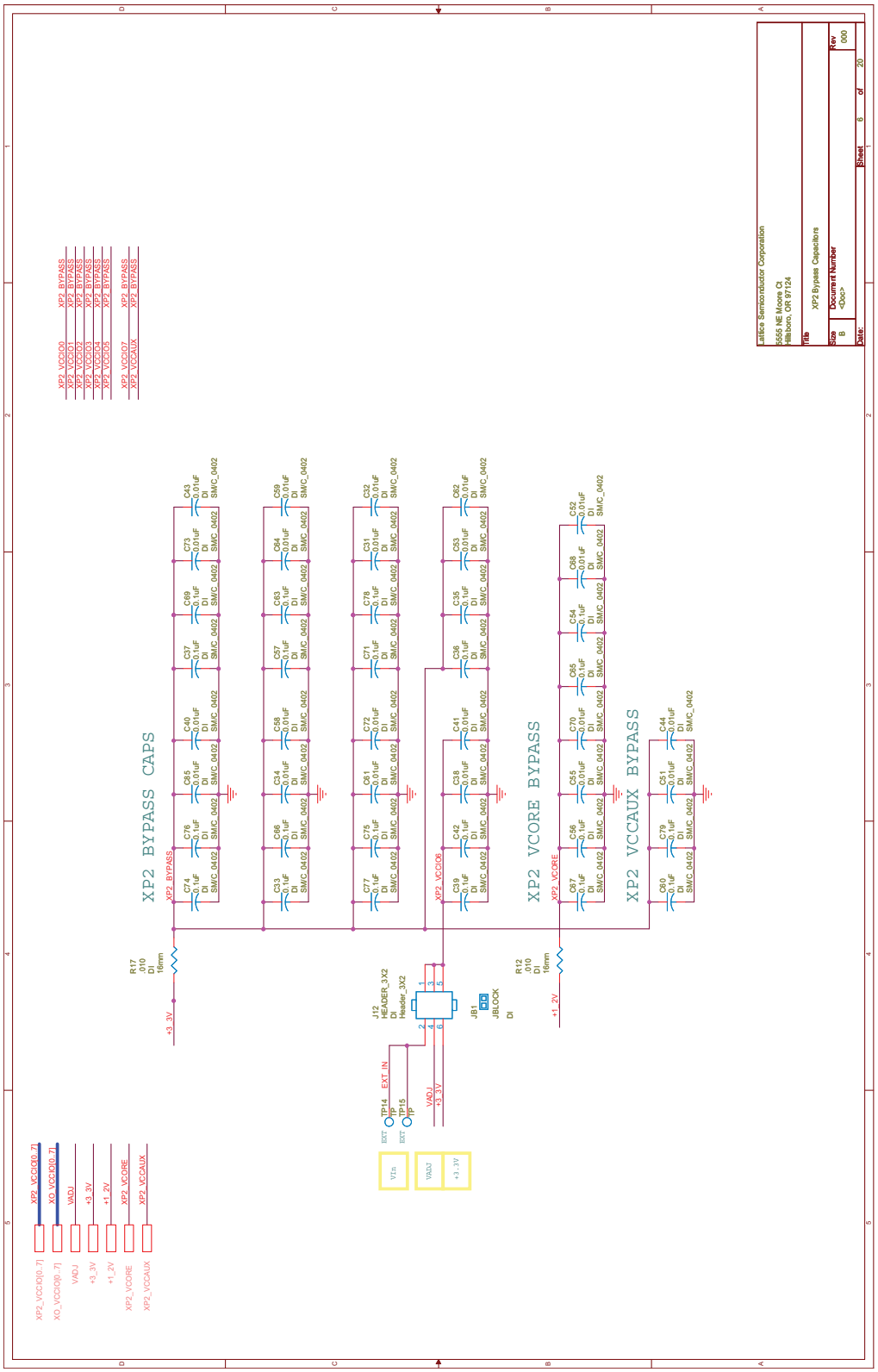


Figure 10. Peripherals and Clock Inputs

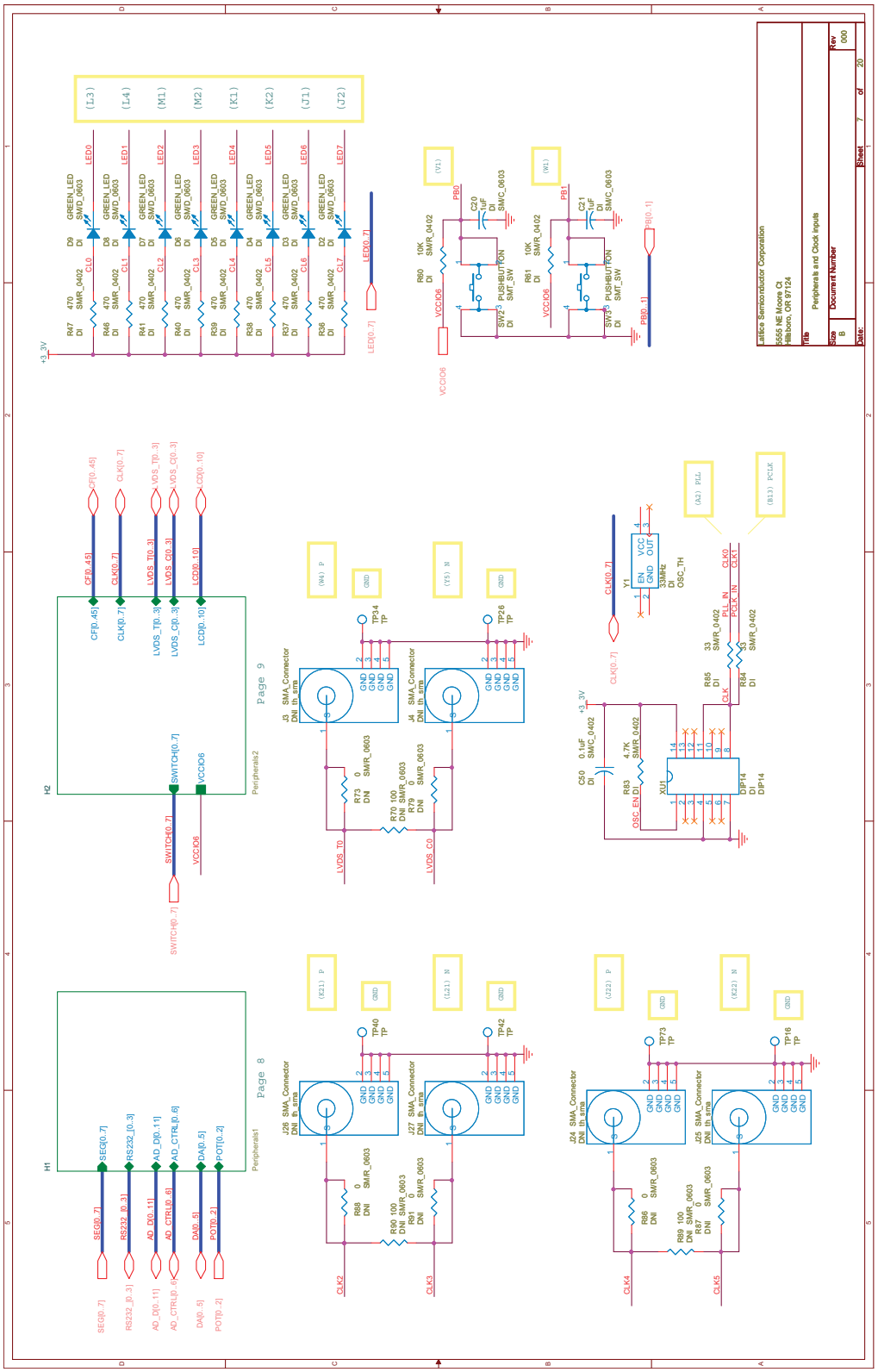


Figure 11. D/A, A/D, 7-Segment and RS232

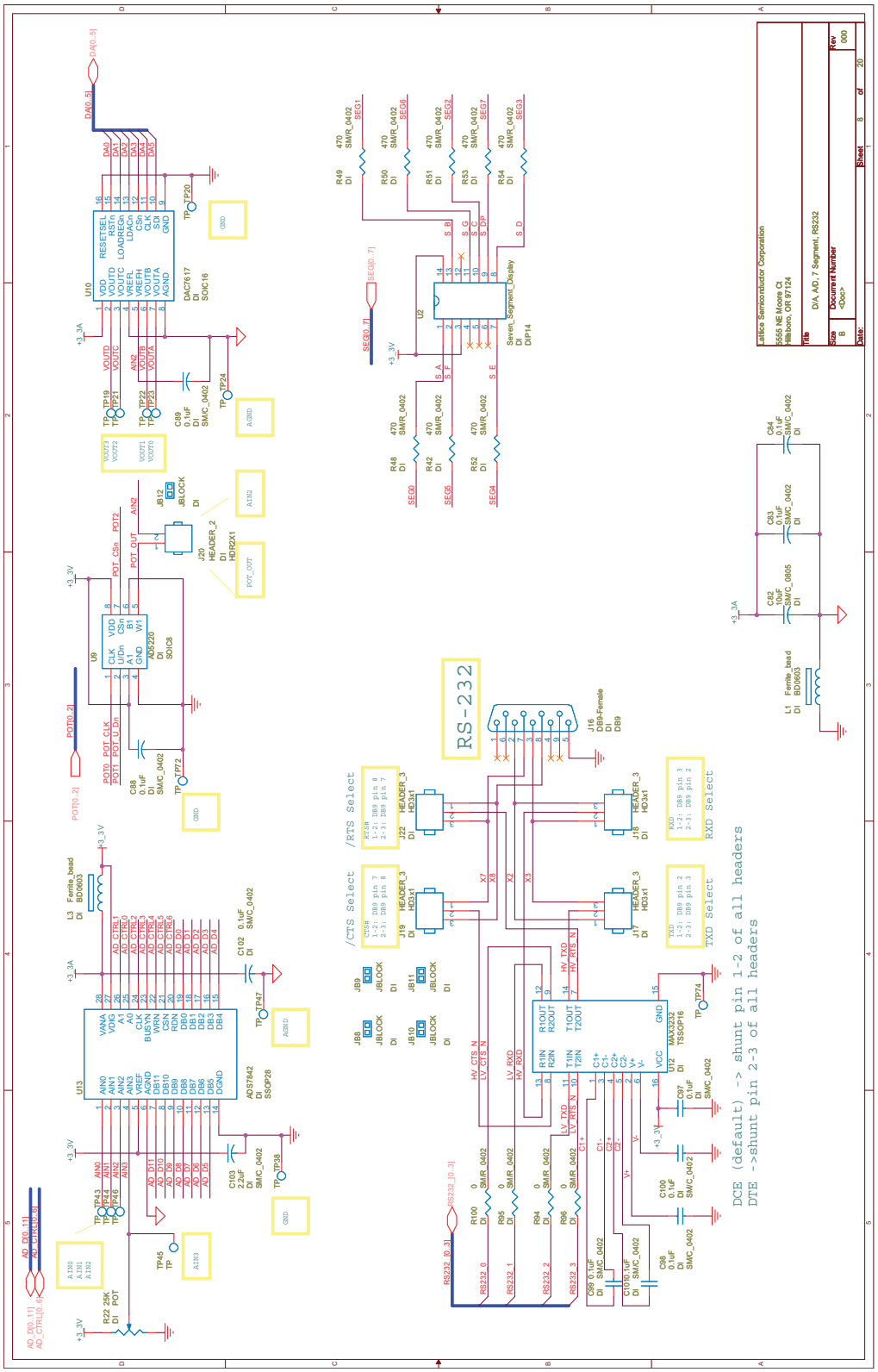


Figure 12. Compact Flash, LVDS, Switches and LCD

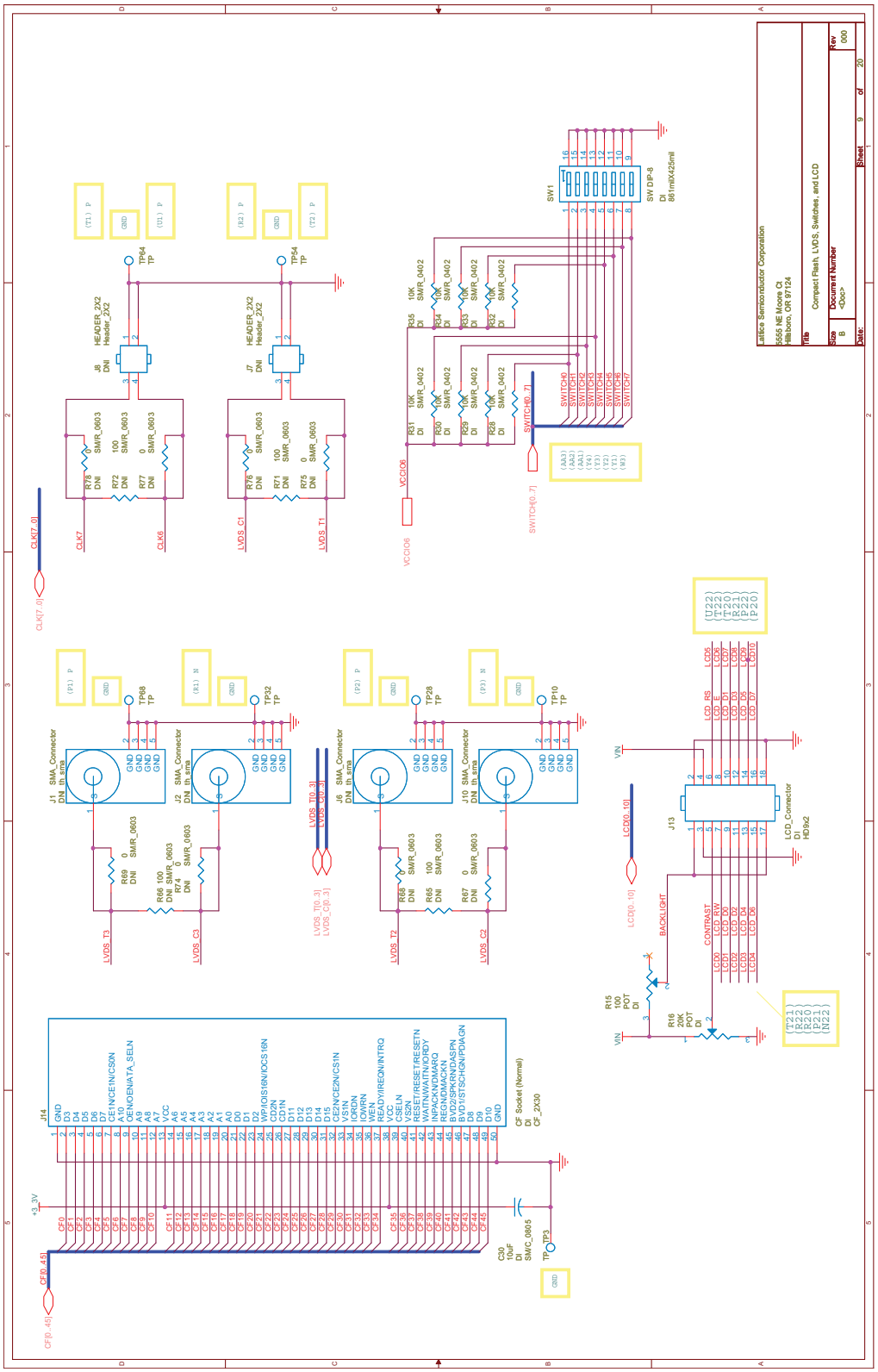


Figure 13. Asynchronous SRAM

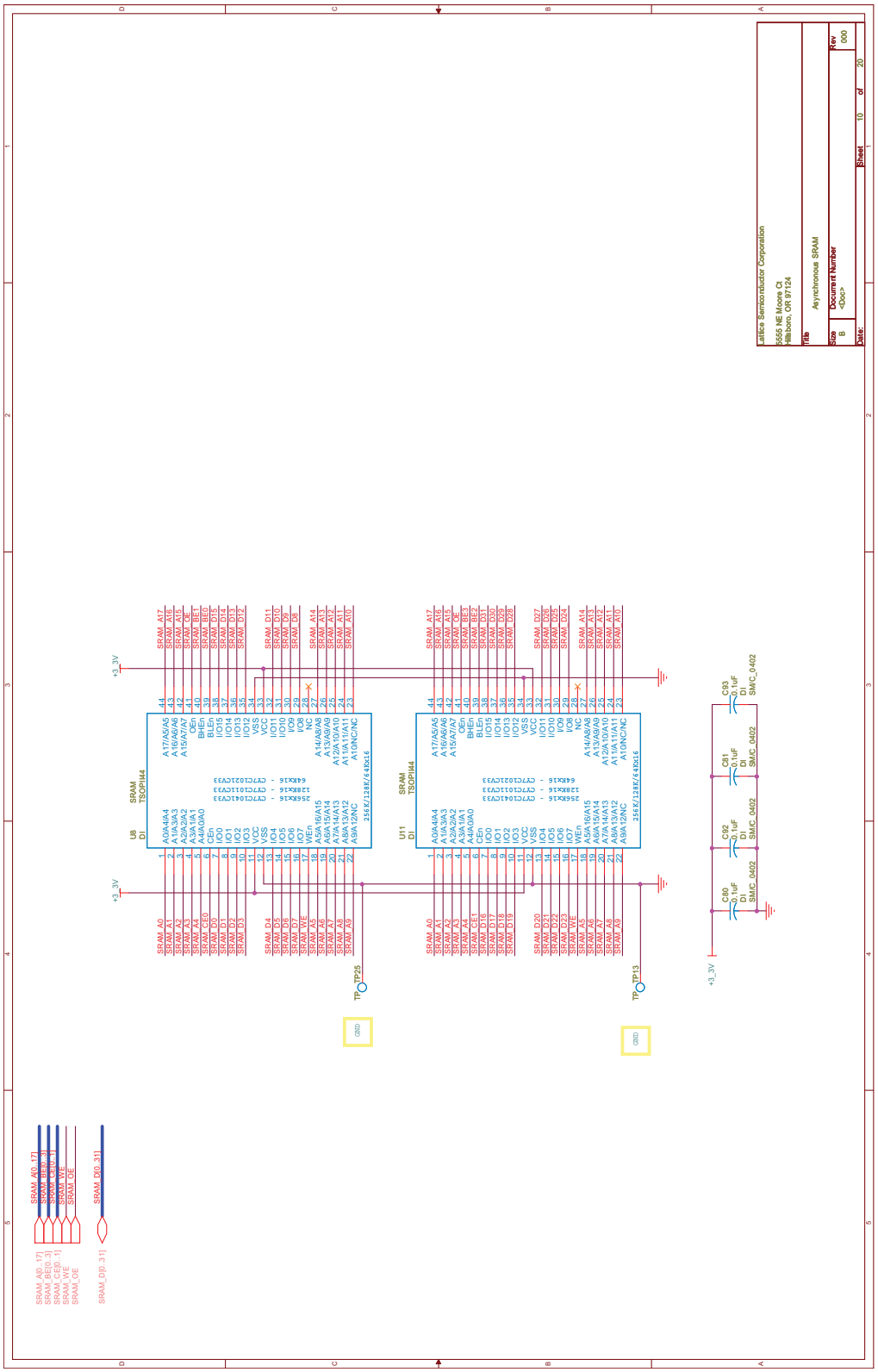


Figure 14. Prototype Grid

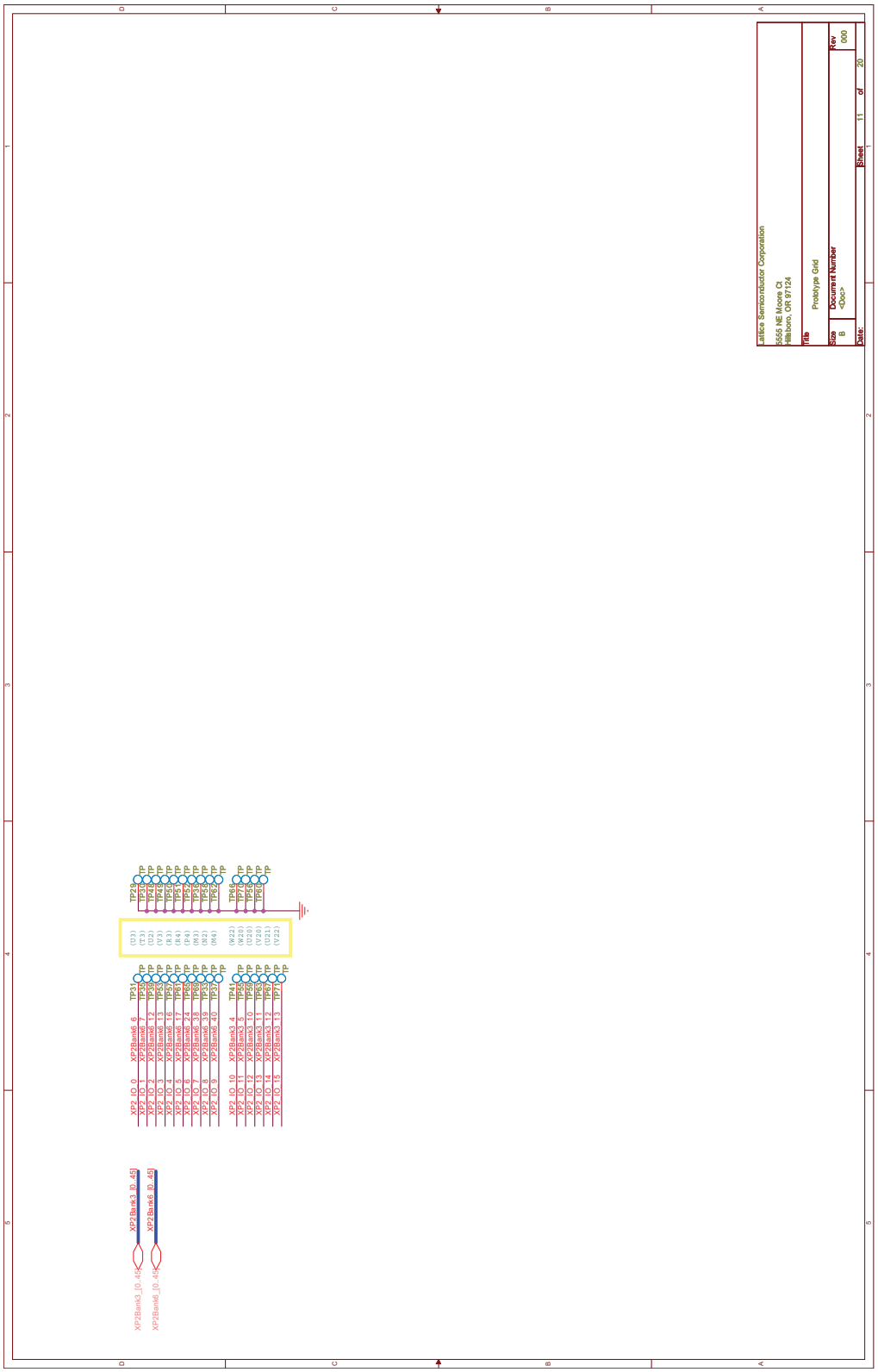


Figure 15. Power Manager

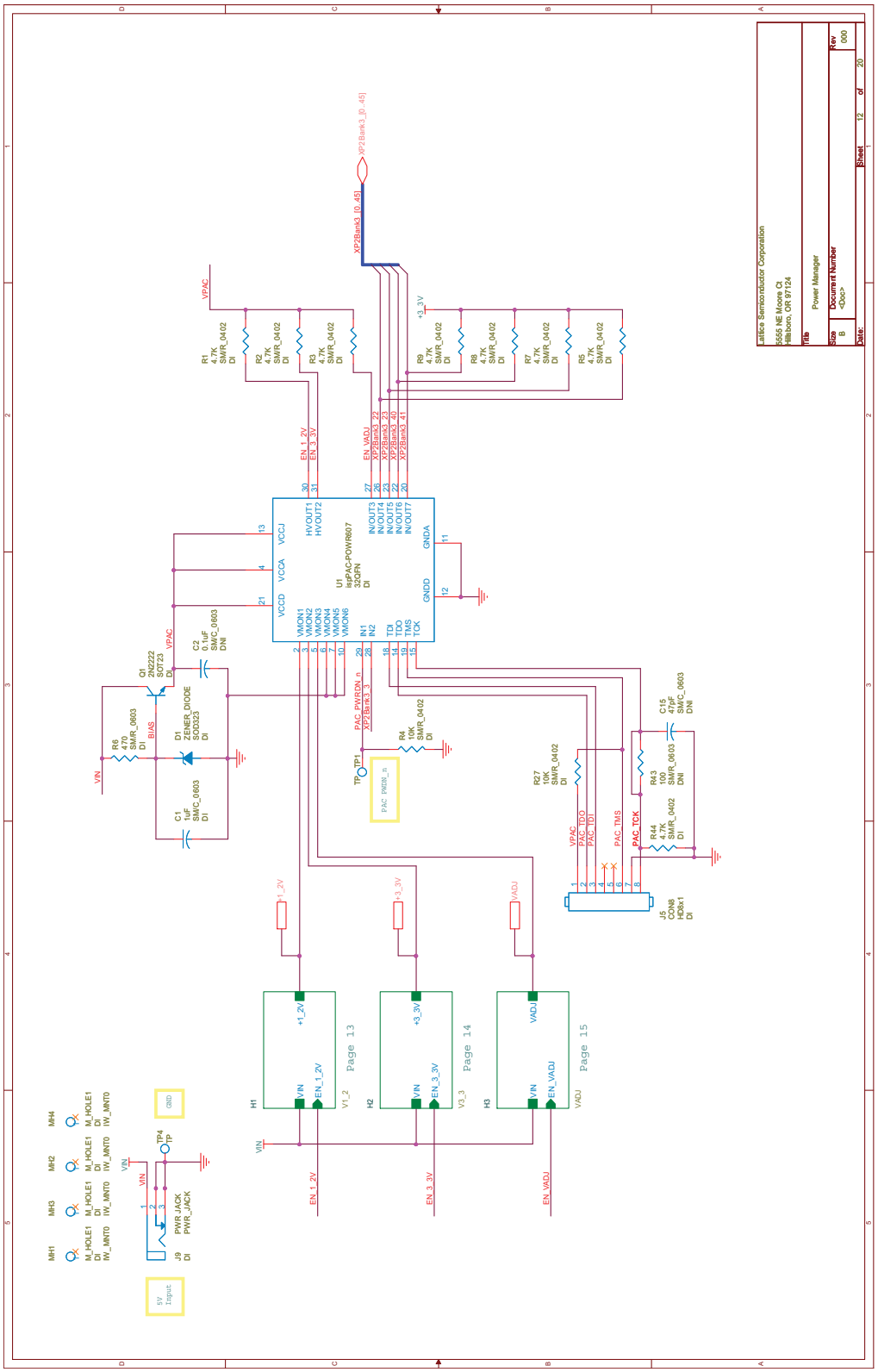


Figure 16. 1.2V Core Supply

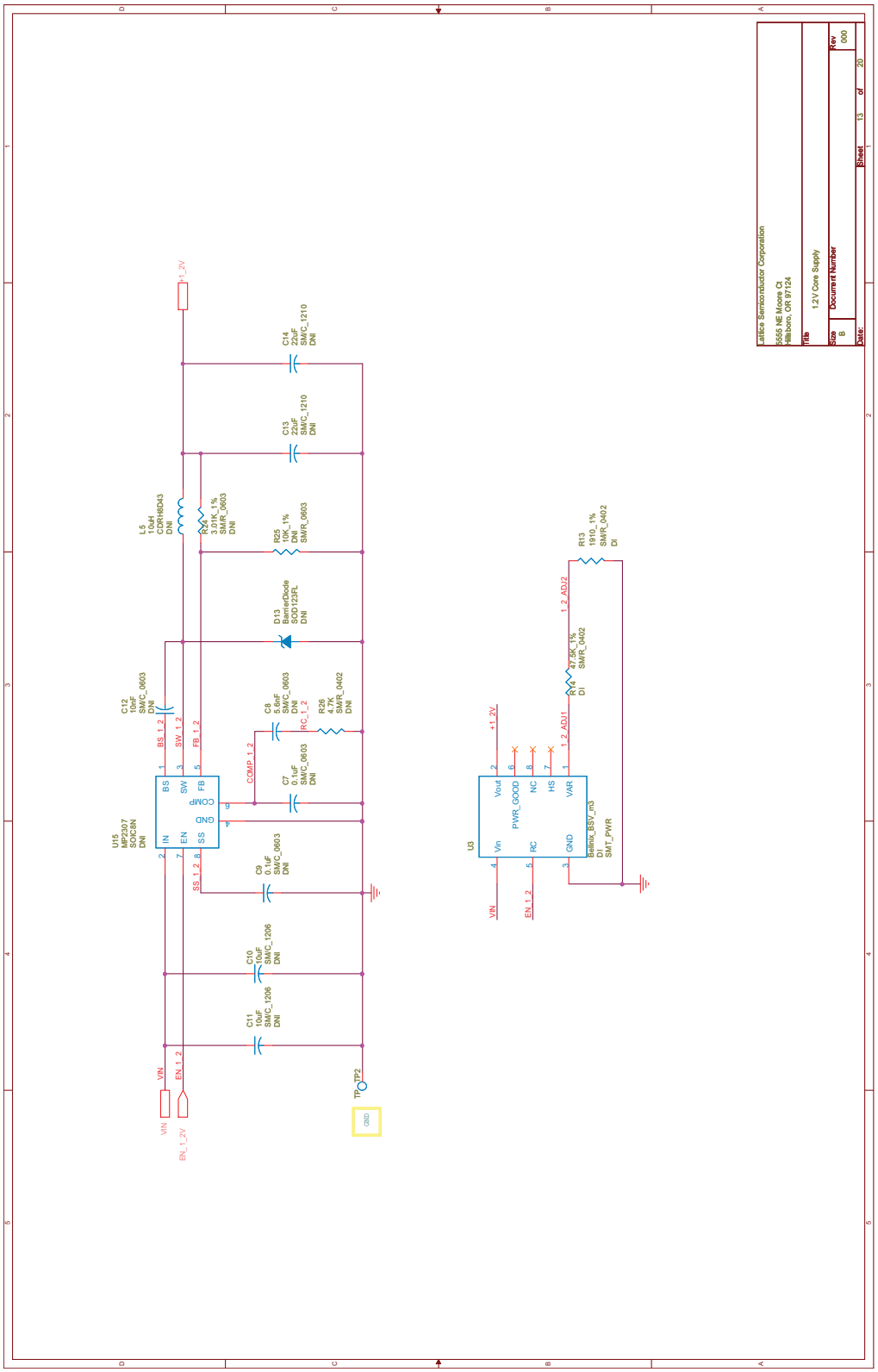


Figure 17. 3.3V Power Converter

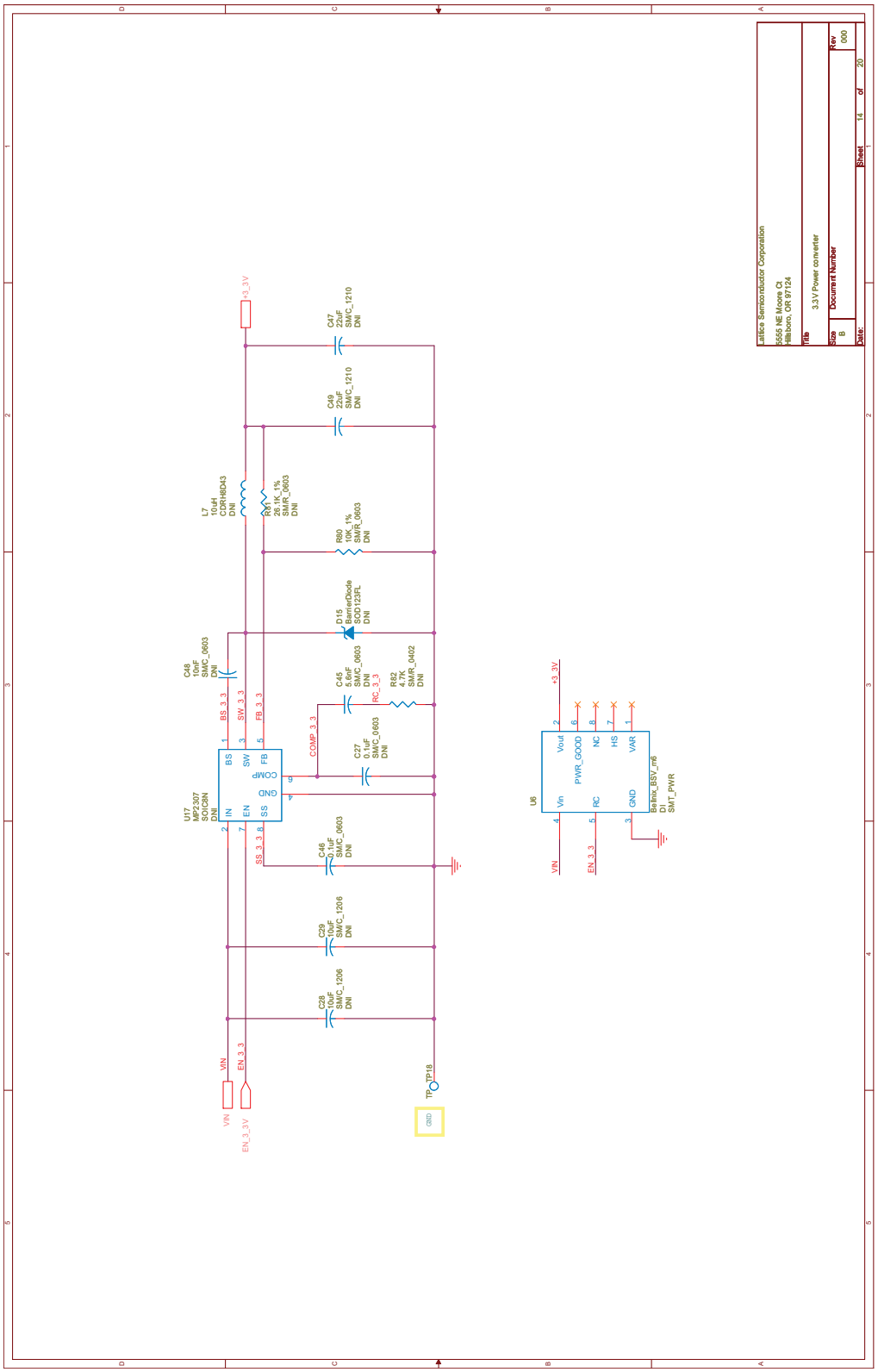


Figure 18. Adjustable Power Supply

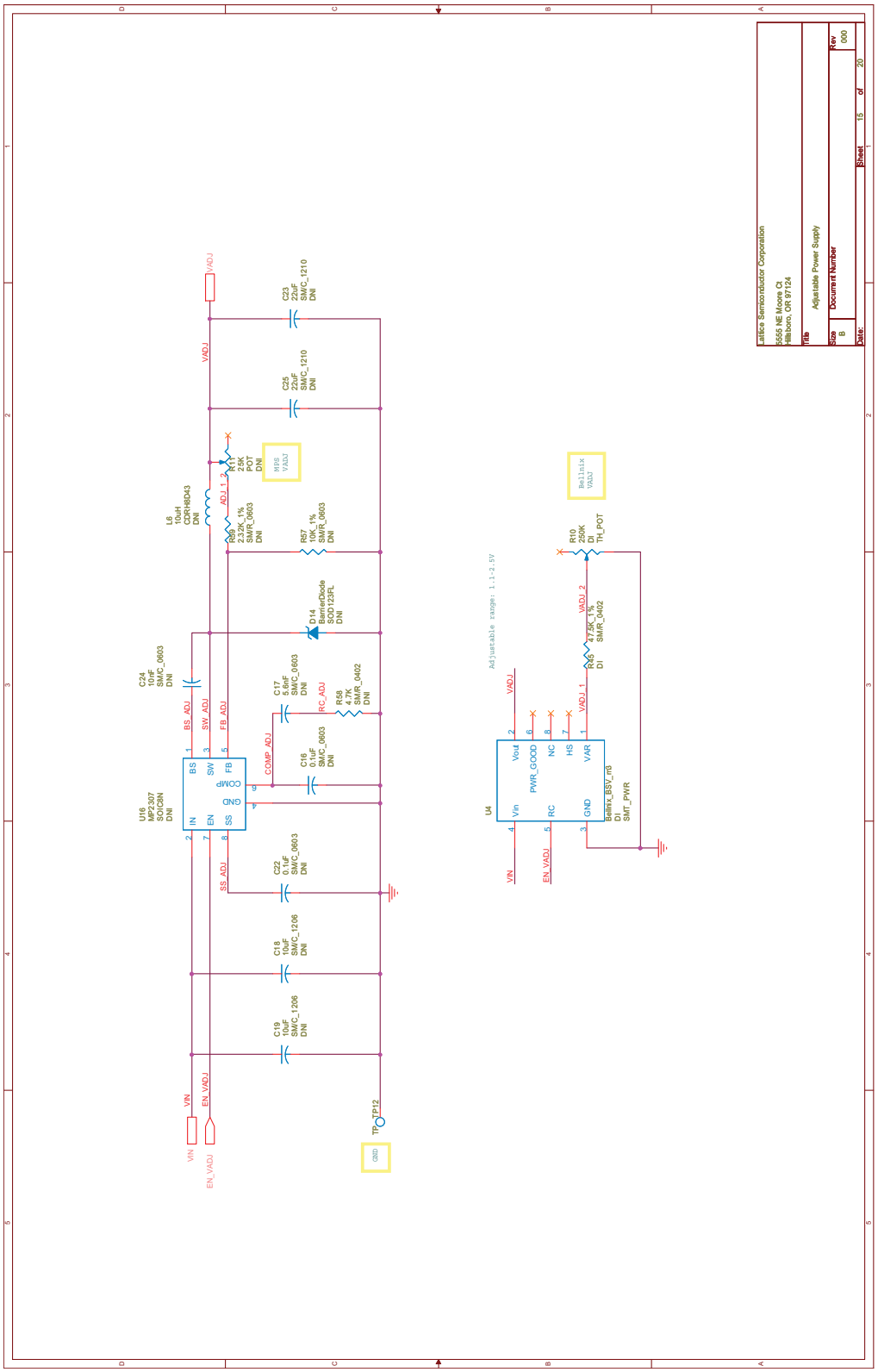


Figure 19. USB Download PHY

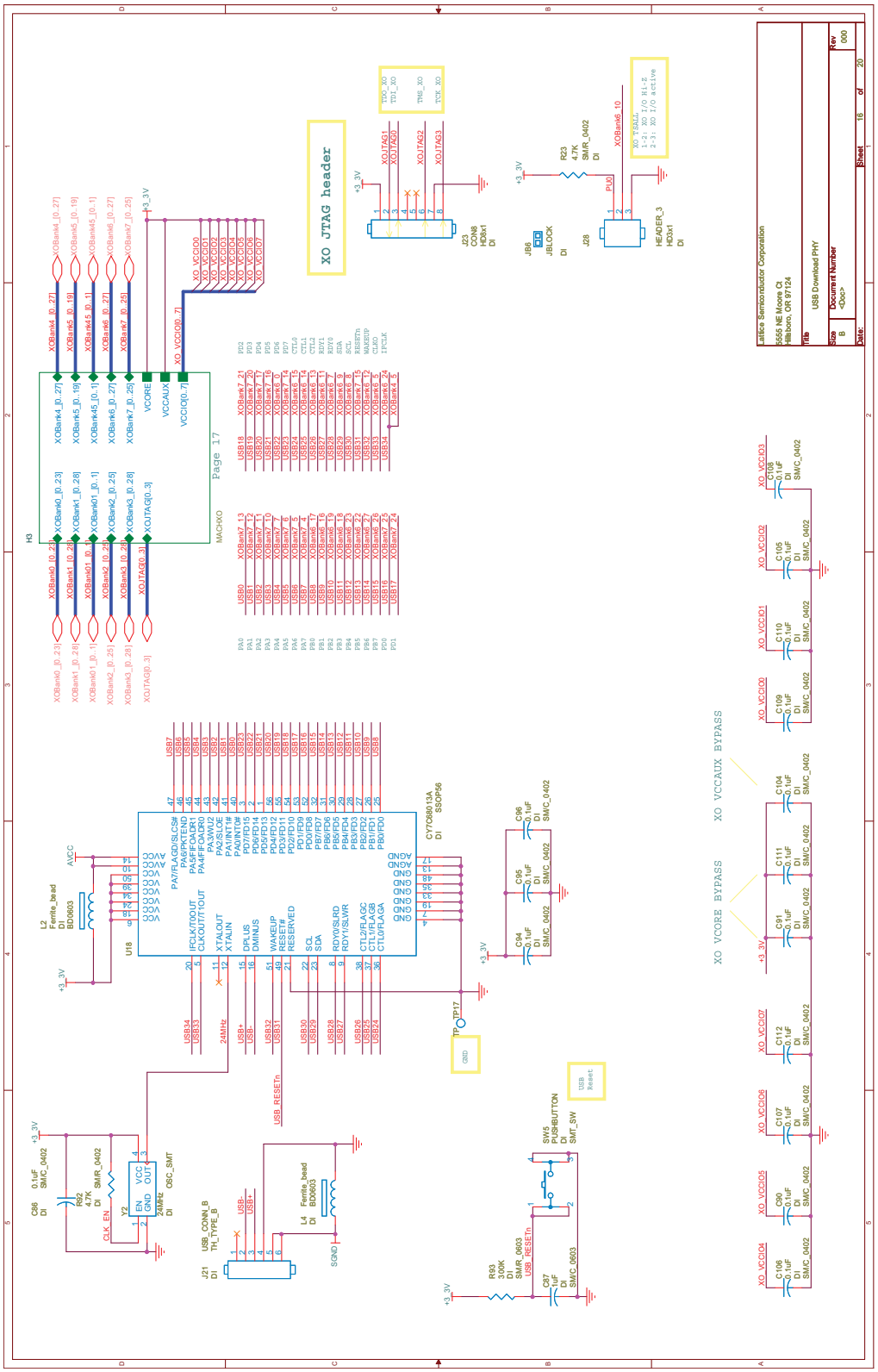


Figure 20. MachXO Power

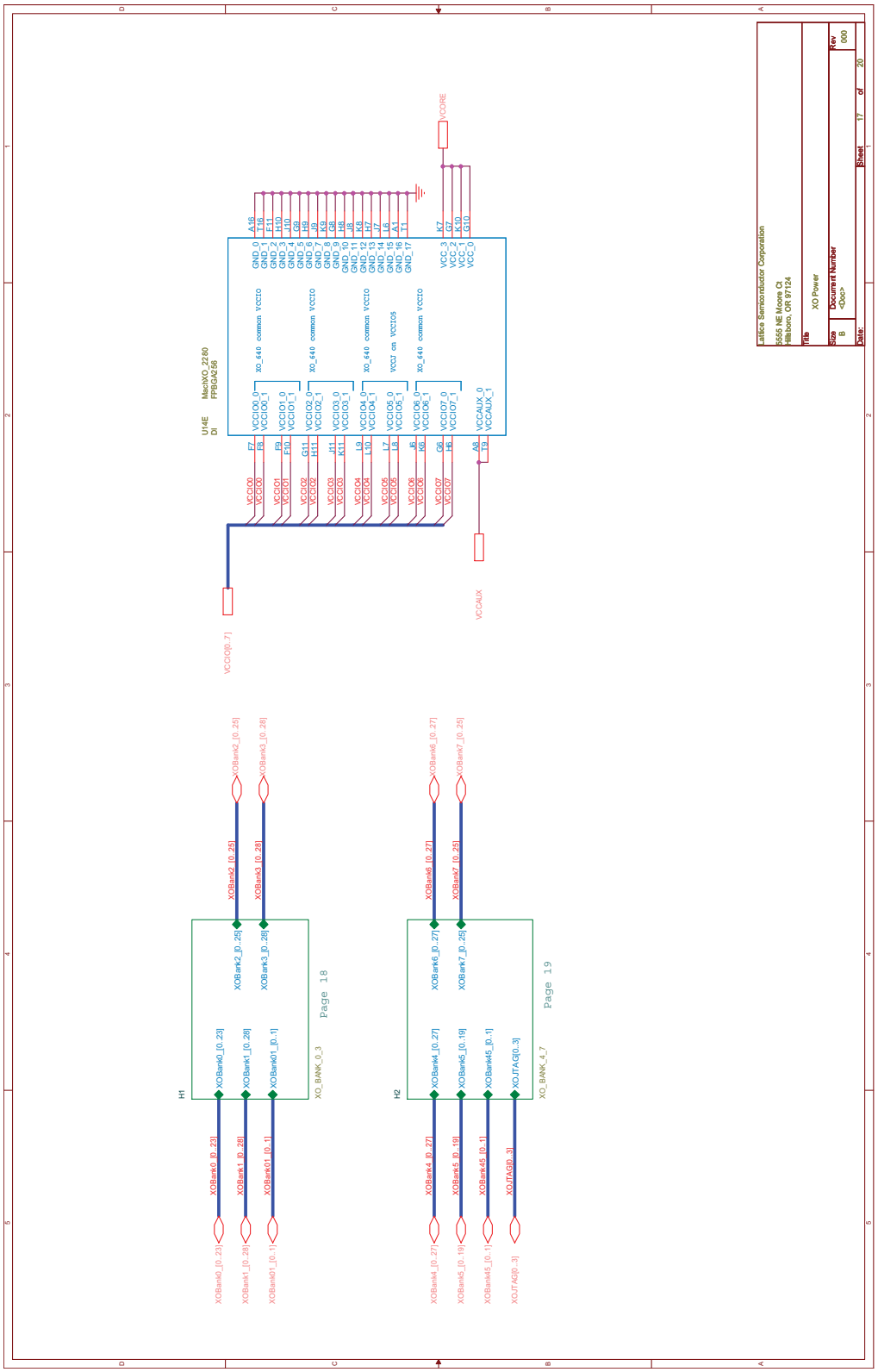


Figure 21. MachXO Banks 0 to 3

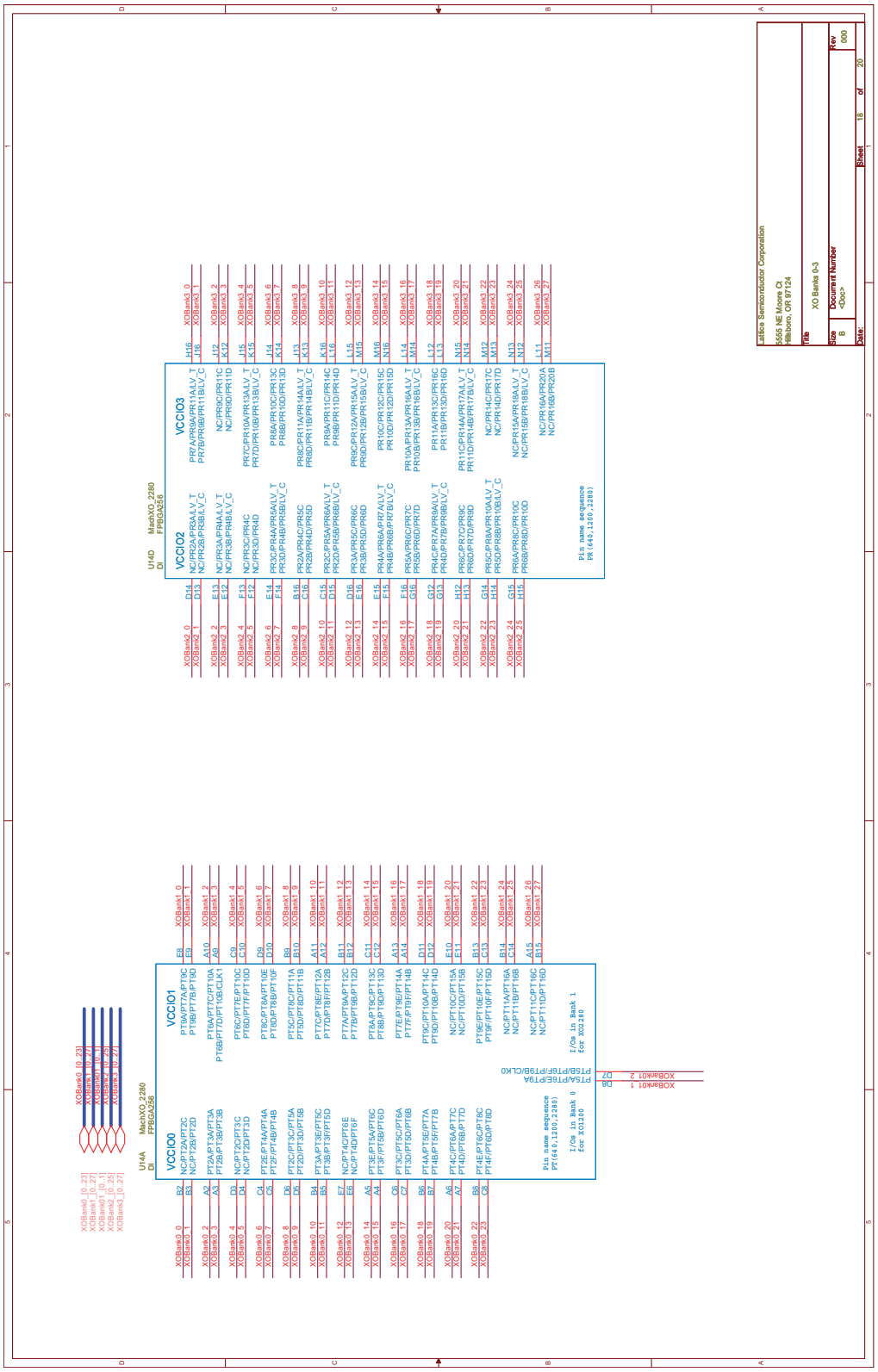


Figure 22. MachXO Banks 4 to 7

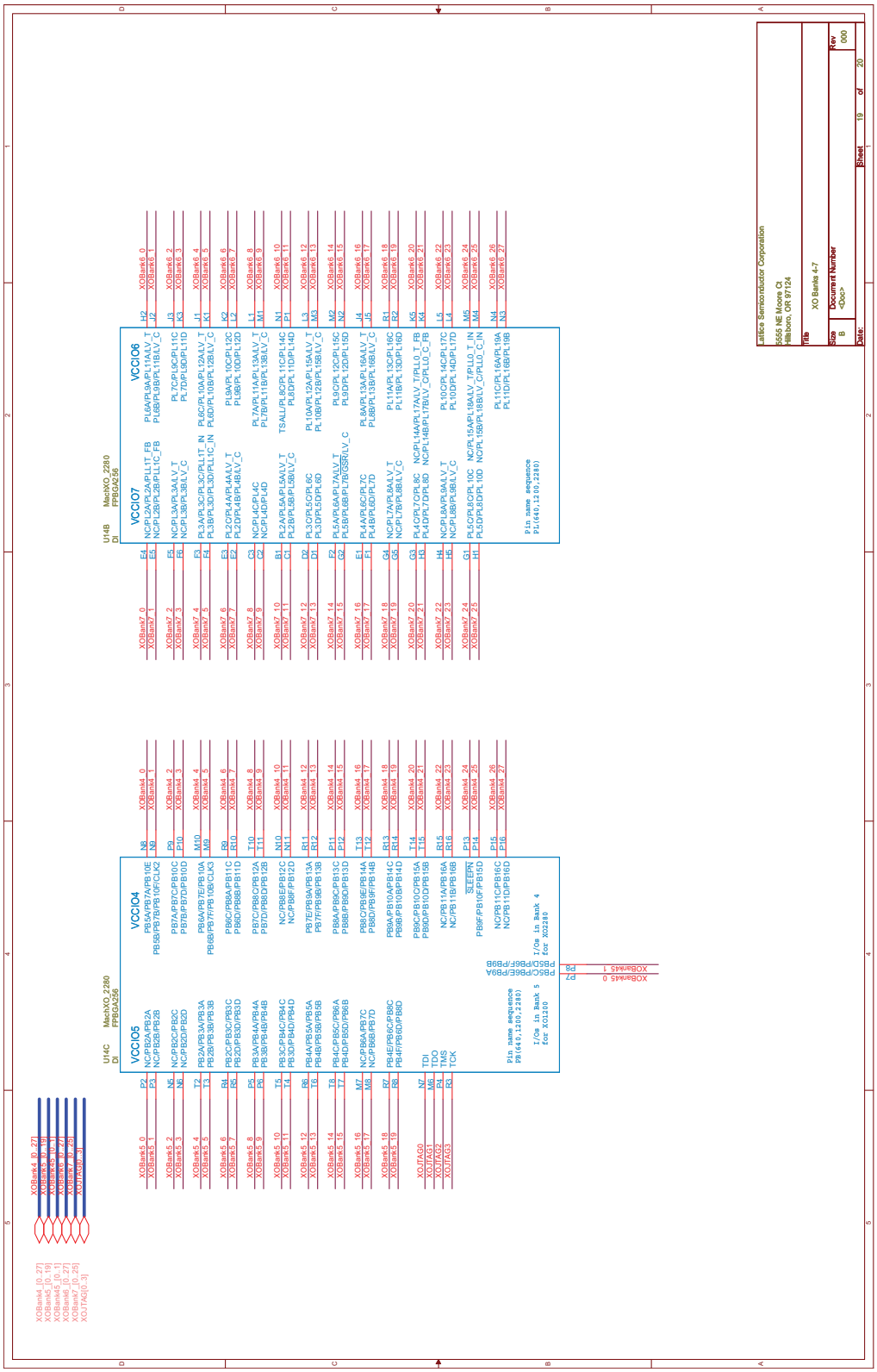


Figure 23. Placement Proposal