Wide-temperature SO-DIMM

DDR4 3200

Datasheet

Products	Product Description
TS2GSH64V2B-I-ARW	16GB DDR4 3200 SO-DIMM 2Rx8 IND 1Gx8 CL22 1.2V

Datasheet version

0.1

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Revision History

Revision No.	History	Released Date	Editor by
0.1	First version	2020/07/28	RD

Transcend Features

Part Name	Capacity	Organization	Rank	Height	DIMM type	Note
TS2GSH64V2B-I-ARW	16GB	1Gx8	2	30.00mm	SO-DIMM	Anti-sulfur

FEATURES

- Operating Temperature : -40°C to +85°C
- RoHS compliant products.
- JEDEC standard 1.2V ± 0.06V power supply
- VDDQ=1.2V ± 0.06V
- Clock Freq: 1600MHz for 3200Mb/s/Pin.
- Programmable CAS Latency: 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 22, 24
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1 clock
- Programmable /CAS Write Latency (CWL) = 16, 20(DDR4-3200)
- 8 bit pre-fetch
- Burst Length: 4, 8
- Bi-directional Differential Data-Strobe
- On Die Termination with ODT pin
- Serial presence detect with EEPROM
- Asynchronous reset
- 30 u" PCB golden finger thickness
- Embedded Anti-sulfur resistor

Table of Content

1. Introduction

1.1 General Feature Information

Hardware Feature

- **Operating Temperature : -40°C to +85°C**
- **RoHS compliant products.**
- **JEDEC standard 1.2V ± 0.06V power supply**
- **VDDQ=1.2V ± 0.06V**
- **Clock Freq: 1600MHz for 3200Mb/s/Pin.**
- **Programmable CAS Latency: 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 22, 24**
- **Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1 clock**
- **Programmable /CAS Write Latency (CWL) = 16, 20(DDR4-3200)**
- **8 bit pre-fetch**
- **Burst Length: 4, 8**
- **Bi-directional Differential Data-Strobe**
- **On Die Termination with ODT pin**
- **Serial presence detect with EEPROM**
- **Asynchronous reset**
- **30 u" PCB golden finger thickness**
- **Embedded Anti-sulfur resistor**

1.2 Product List

DIMM Type	Part Name	Capacity
SO-DIMM	TS2GSH64V2B-I-ARW	16GB

1.3 Ordering Information

TS2GSH64V2B-I-ARW

1 2 3 4 567 8

1 – Transcend

2 – DRAM module capacity = 2GB x 8

3 – SO-DIMM

4 – Module memory bus width

5 – Operation voltage 1.2V

6 – 3200

7 – 1Gx8

8 – Wide-temperature operation from -40°C to +85°C

2. Product Specifications

2.1 Interface and Compliance

- DDR4 3200 wide-temperature SODIMM (Small Outline) with 64 Bits data width
- Non-ECC Unbuffered Memory
- RoHS Compliance
- CE, FCC and BSMI Compliance

2.2 Supply Voltage

[Table 1] Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on VDD relative to Vss	VDD	-0.3 ~ 1.5	V	1)
Voltage on VDDQ pin relative to Vss	VDDQ	-0.3 ~ 1.5	V	1)
Voltage on VPP pin relative to Vss	VPP	-0.3 ~ 3.0	V	3)
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.5	V	1)
Storage temperature	TSTG	-55~+100	C	1), 2)

Note:

1) Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2) Storage Temperature is the ambient temperature.

3) VPP must be equal or greater than VDD/VDDQ at all times.

[Table 2] Recommended AC & DC Operating Conditions

Parameter	Symbol	Rating			Unit	Note
		Min	Typ.	Max		
Supply voltage	VDD	1.14	1.2	1.26	V	1), 2)
Supply voltage for Output	VDDQ	1.14	1.2	1.26	V	1), 2)
Wordline supply voltage	VPP	2.375	2.5	2.75	V	3)

Note:

1) Under all conditions VDDQ must be less than or equal to VDD.

2) VDDQ tracks with VDD, AC parameters are measured with VDD and VDDQ tied together.

3) DC bandwidth is limited to 20MHz

2.3 IDD Specification Parameters and Table

[Table 3] IDD Specification Parameters – 16GB, 2G x 64 Module (2 Rank x 8)

Parameters	Symbol	TS2GSH64V2B-I		Unit
		IDD Max.	IPP Max.	
Operating One bank Active-Precharge current	IDD0	408	56	mA
Operating One bank Active-read-Precharge current	IDD1	432	56	mA

Precharge power-down current	IDD2P	208	48	mA
Precharge quiet standby current	IDD2Q	320	64	mA
Precharge standby current	IDD2N	320	48	mA
Active power - down current	IDD3P	336	64	mA
Active standby current	IDD3N	480	64	mA
Operating burst read current	IDD4R	1072	56	mA
Operating burst write current	IDD4W	1008	56	mA
Burst refresh current	IDD5	2000	224	mA
Self refresh current	IDD6	336	80	mA
Operating bank interleave read current	IDD7	1424	112	mA

Note:

1) IDD values are for full operating range of Voltage and Temperature

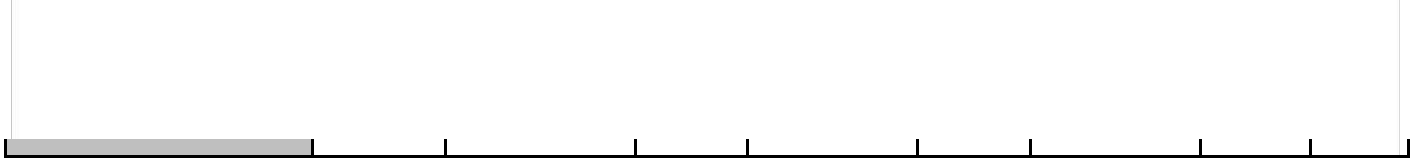
2) Module IDD was calculated on the specific brand DRAM component IDD and can be differently measured according to DQ loading capacitor.

2.4 Timing Parameters and Specifications

[Table 4] Timing Parameters and Specifications

Speed		DDR4-2133		DDR4-2400		DDR4-2666		Unit
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	
Average Clock Period	tCK (avg)	0.937	<1.071	0.833	<0.937	0.750	<0.833	ns
Average high pulse width	tCH (avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK (avg)
Average low pulse width	tCL (avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK (avg)
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS (base)	80	-	62	-	55	-	ps
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	180	-	162	-	145	-	ps
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH (base)	105	-	87	-	80	-	ps
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	180	-	162	-	145	-	ps
Control and Address Input pulse width for each input	tIPW	460	-	410	-	385	-	ps
CAS_n to CAS_n command delay for same bank group	tCCD_L	Max (5nCK,5.625ns)	-	Max (5nCK,5ns)	-	Max (5nCK,5ns)	-	nCK
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S (2K)	Max (4nCK,5.3ns)	-	Max (4nCK,5.3ns)	-	Max (4nCK,5.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S (1K)	Max (4nCK,3.7ns)	-	Max (4nCK,3.3ns)	-	Max (4nCK,3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different	tRRD_S (1/2K)	Max (4nCK,3.7ns)	-	Max (4nCK,3.3ns)	-	Max (4nCK,3ns)	-	nCK

bank group for 1/2KB page size								
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L (2K)	Max (4nCK,6.4ns)	-	Max (4nCK,6.4ns)	-	Max (4nCK,6.4ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L (1K)	Max (4nCK,5.3ns)	-	Max (4nCK,4.9ns)	-	Max (4nCK,4.9ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L (1/2K)	Max (4nCK,5.3ns)	-	Max (4nCK,4.9ns)	-	Max (4nCK,4.9ns)	-	nCK
Four activate window for 2KB page size	tFAW_2K	Max (28nCK,30ns)	-	Max (28nCK,30ns)	-	Max (28nCK,30ns)	-	ns
Four activate window for 1KB page size	tFAW_1K	Max (20nCK,21ns)	-	Max (20nCK,21ns)	-	Max (20nCK,21ns)	-	ns
Four activate window for 1/2KB page size	tFAW_1/2K	Max (16nCK,15ns)	-	Max (16nCK,13ns)	-	Max (16nCK,12ns)	-	ns
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	Max (2nCK,2.5ns)	-	Max (2nCK,2.5ns)	-	Max (2nCK,2.5ns)	-	ns
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	Max (4nCK,7.5ns)	-	Max (4nCK,7.5ns)	-	Max (4nCK,7.5ns)	-	
Internal READ Command to PRECHARGE Command delay	tRTP	Max (4nCK,7.5ns)	-	Max (4nCK,7.5ns)	-	Max (4nCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	15	-	15	-	ns
DLL locking time	tDLLK	768	-	768	-	854	-	nCK
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))						nCK
CS_n to Command Address Latency	tCAL	Max (3nCK,3.748ns)	-	Max (3nCK,3.748ns)	-	Max (3nCK,3.748ns)	-	nCK
DQS_t, DQS_c to DQ skew, per group, per ac- cess	tDQSQ	-	0.16	-	0.17	-	0.18	tCK(avg)/ 2
DQ output hold per group, per access from DQS_t,DQS_c	tQH	0.76	-	0.74	-	0.74	-	tCK(avg)/ 2
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-390	180	-330	175	-310	170	ps
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	180	-	175	-	170	ps
DQS_t, DQS_c differential READ Pre-amble (1 clock preamble)	tRPRE	0.9	-	0.9	-	0.9	-	tCK
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	-	0.33	-	0.33	-	tCK
DQS_t, DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	tCK
DQS_t, DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	tCK
DQS_t, DQS_c differential WRITE Pre-amble (1 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	tCK
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	tCK
DQS_t and DQS_c		-360	180	-330	175	-310	170	ps



erenced from RL-1)								
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	180	-	175	-	170	ps
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	tCK
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	tCK
DQS_t, DQS_c rising edge to CK_t, CK_c ris-ing edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	tCK
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	tCK
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	nCK
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	nCK
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	nCK
Exit Reset from CKE HIGH to a valid com-mand	tXPR	Max (5nCK,tRFC(min) +10ns)	-	Max (5nCK,tRFC(min)+10ns)	-	Max (5nCK,tRFC(min)+10ns)	-	nCK
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10 ns	-	tRFC(min)+10 ns	-	nCK
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1n CK	-	tCKE(min)+1n CK	-	nCK
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	Max(4nCK,6ns)	-	Max (4nCK,6ns)	-	Max (4nCK,6ns)	-	nCK
CKE minimum pulse width	tCKE	Max(3nCK,5ns)	-	Max (3nCK,5ns)	-	Max (3nCK,5ns)	-	nCK
Asynchronous RTT turn-on delay (Power- Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	ns
Asynchronous RTT turn-off delay (Power- Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	ns
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK (avg)
tRFC1 (min)	2Gb	160	-	160	-	160	-	ns
	4Gb	260	-	260	-	260	-	ns
	8Gb	350	-	350	-	350	-	ns
	16Gb	550	-	550	-	550	-	ns
tRFC2 (min)	2Gb	110	-	110	-	110	-	ns
	4Gb	160	-	160	-	160	-	ns
	8Gb	260	-	260	-	260	-	ns
	16Gb	350	-	350	-	350	-	ns
tRFC4 (min)	2Gb	90	-	90	-	90	-	ns

	4Gb	110	-	110	-	110	-	ns
	8Gb	160	-	160	-	160	-	ns
	16Gb	260	-	260	-	260	-	ns

Speed		DDR4-2933		DDR4-3200		Unit
Parameter	Symbol	MIN	MAX	MIN	MAX	
Average Clock Period	tCK(avg)	0.682	<0.750	0.625	<0.682	ns
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	tCK(avg)
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	tCK(avg)
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	48	-	40	-	ps
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	138	-	130	-	ps
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	73	-	65	-	ps
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	138	-	130	-	ps
Control and Address Input pulse width for each input	tIPW	365	-	340	-	ps
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 5 ns)	-	max(5 nCK, 5 ns)	-	nCK
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK, 2.7ns)	-	Max(4nCK, 2.5ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/ 2K)	Max(4nCK, 2.7ns)	-	Max(4nCK, 2.5ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	nCK
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,30ns)	-	Max (28nCK,30ns)	-	ns
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 21ns)	-	Max(20nCK, 21ns)	-	ns
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 10.875ns)	-	Max(16nCK, 10ns)	-	ns
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	ax (2nCK, 2.5ns)	-	max (2nCK, 2.5ns)	-	ns

Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	
Internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	15	-	ns
DLL locking time	tDLLK	1024	-	1024	-	nCK
Mode Register Set command cycle time	tMRD	8	-	8	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))				nCK
CS_n to Command Address Latency	tCAL	Max(3 nCK, 3.748 ns)	-	Max(3 nCK, 3.748 ns)	-	nCK
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.19	-	0.20	tCK(avg) /2
DQ output hold time per group, per access from DQS_t,DQS_c	tQH	0.72	-	0.70	-	tCK(avg) /2
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-280	165	-250	160	ps
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	165	-	160	ps
DQS_t, DQS_c differential READ Preamble (1 clock preamble)	tRPRE	0.9	NOTE 44	0.9	NOTE 44	tCK
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	NOTE 45	0.33	NOTE 45	tCK
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	tCK
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	tCK
DQS_t, DQS_c differential WRITE Preamble (1 clock preamble)	tWPRE	0.9	-	0.9	-	tCK
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	tCK
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-280	165	-250	160	ps
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	165	-	160	ps
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	tCK
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	tCK
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	tCK
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	tCK
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	tCK
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	nCK
Normal operation Full calibration time	tZQoper	512	-	512	-	nCK
Normal operation Short calibration time	tZQCS	128	-	128	-	nCK
		max (5nCK,tRFC(		max (5nCK,tRFC(		

valid command	tXPR	min)+10ns)	-	min)+10ns)	-	nCK

Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10 ns	-	tRFC(min)+10 ns	-	nCK
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	nCK
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+ 1nCK	-	tCKE(min)+ 1nCK	-	nCK
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	nCK
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	nCK
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	ns
RTT dynamic change skew	tADC	0.26	0.74	0.26	0.74	tCK(avg)
tRFC1 (min)	2Gb	160	-	160	-	ns
	4Gb	260	-	260	-	ns
	8Gb	350	-	350	-	ns
	16Gb	550 (default)	-	550 (default)	-	ns
		450 (optional-1)	-	450 (optional-1)		ns
		350 (optional-2)	-	350 (optional-2)		ns
tRFC2 (min)	2Gb	110	-	110	-	ns
	4Gb	160	-	160	-	ns
	8Gb	260	-	260	-	ns
	16Gb	350 (default)	-	350 (default)	-	ns
		350 (optional-1)	-	350 (optional-1)		ns
		260 (optional-2)	-	260 (optional-2)		ns
tRFC4 (min)	2Gb	90	-	90	-	ns
	4Gb	110	-	110	-	ns
	8Gb	160	-	160	-	ns
	16Gb	260 (default)	-	260 (default)	-	ns
		260 (optional-1)	-	260 (optional-1)		ns
		160 (optional-2)	-	160 (optional-2)		ns

2.5 Serial Presence Detect Specification

[Table 5] Serial Presence Detect Specification

TS2GSH64V2B-I Serial Presence Detect			
Byte No.	Description	Value	Hex Value
0	Number of Serial PD Bytes Written / SPD Device Size	SPD bytes used: 512 bytes SPD bytes total: 512 bytes	24
1	SPD Revision	Revision 1.2	12
2	DRAM Device Type	DDR4 SDRAM	0C
3	Module Type	SO-DIMM	03
4	SDRAM Density and Banks	8 Gb, 16 banks	85
5	SDRAM Addressing	Row: 16, Column: 10	21
6	Primary SDRAM Package Type	Monolithic Single die Not specified	00
7	SDRAM Optional Features	Unlimited MAC	08
8	SDRAM Thermal and Refresh Options	Reserved	00
9	Other SDRAM Optional Features	Post package repair supported Soft PPR supported	60
10	Secondary SDRAM Package Type	-	00
11	Module Nominal Voltage, VDD	1.2V	03
12	Module Organization	2 Ranks x 8 bits	09
13	Module Memory Bus Width	Non-ECC, 64 bits	03
14	Module Thermal Sensor	Not incorporated	00
15	Extended Module Type	Reserved	00
16	Reserved	-	00
17	Timebases	MTB = 125 ps FTB = 1 ps	00
18	SDRAM Minimum Cycle Time (tCKAVGmin)	0.625 ns	05
19	SDRAM Maximum Cycle Time (tCKAVGmax)	1.625 ns	0D
20-23	CAS Latencies Supported	10 11 12 13 14 15 16 17 18 19 20 22 24	F8 BF 02 00
24	Minimum CAS Latency Time (tAAmin)	13.75 ns	6E
25	Minimum RAS to CAS Delay Time (tRCDmin)	13.75 ns	6E
26	Minimum Row Precharge Delay Time (tRPmin)	13.75 ns	6E
27	Upper Nibbles for tRASmin and tRCmin	See bytes 28, 29	11
28	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	32 ns	00
29	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	45.75 ns	6E
30-31	Minimum Refresh Recovery Delay Time (tRFC1min)	350 ns	F0 0A
32-33	Minimum Refresh Recovery Delay Time (tRFC2min)	260 ns	20 08

34-35	Minimum Refresh Recovery Delay Time (tRFC4min)	160 ns	00 05
36-37	Minimum Four Activate Window Delay Time (tFAWmin)	21 ns	00 A8
38	Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group	2.5 ns	14
39	Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group	5 ns	28
40	Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group	5 ns	28
41-42	Minimum Write Recovery Time(tWRmin)	15 ns	00 78
43	Upper Nibbles for tWTRmin	See bytes 44, 45	00
44	Minimum Write to Read Time(tWTR_Smin), different bank group	2.5 ns	14
45	Minimum Write to Read Time(tWTR_Lmin), same bank group	7.5 ns	3C
46-59	Reserved	-	00
60	Connector to SDRAM Bit Mapping	1302	0B
61	Connector to SDRAM Bit Mapping	5746	2B
62	Connector to SDRAM Bit Mapping	1320	0C
63	Connector to SDRAM Bit Mapping	5746	2B
64	Connector to SDRAM Bit Mapping	5746	2B
65	Connector to SDRAM Bit Mapping	1302	0B
66	Connector to SDRAM Bit Mapping	3120	16
67	Connector to SDRAM Bit Mapping	7564	36
68	Connector to SDRAM Bit Mapping	-	00
69	Connector to SDRAM Bit Mapping	-	00
70	Connector to SDRAM Bit Mapping	3102	15
71	Connector to SDRAM Bit Mapping	5764	2C
72	Connector to SDRAM Bit Mapping	1302	0B
73	Connector to SDRAM Bit Mapping	7546	35
74	Connector to SDRAM Bit Mapping	3120	16
75	Connector to SDRAM Bit Mapping	7564	36
76	Connector to SDRAM Bit Mapping	3120	16
77	Connector to SDRAM Bit Mapping	7564	36
78-116	Reserved	-	00
117	Fine Offset for Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group	0 ps	00
118	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group	-100 ps	9C
119	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group	0 ps	00
120	Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin)	0 ps	00

121	Fine Offset for Minimum Row Precharge Delay Time (tRPmin)	0 ps	00
122	Fine Offset for Minimum RAS to CAS Delay Time (tRCDmin)	0 ps	00
123	Fine Offset for Minimum CAS Latency Time (tAAmin)	0 ps	00
124	Fine Offset for SDRAM Maximum Cycle Time (tCKAVGmax)	-25 ps	E7
125	Fine Offset for SDRAM Minimum Cycle Time (tCKAVGmin)	0 ps	00
126-127	CRC for Base Configuration Section	CRC for bytes 0-125	99 49
128	Raw Card Extension, Module Nominal Height	29 < Height ⩽ 30 mm	0F
129	Module Maximum Thickness	1 < Front ⩽ 2 mm 1 < Back ⩽ 2 mm	11
130	Reference Raw Card Used	R/C E1	24
131	Address Mapping from Edge Connector to DRAM	Mirrored	01
132-253	Reserved	-	00
254-255	Cyclical Redundancy Code (CRC) for SPD Block 1	CRC for bytes 128-253	55 23
256-319	Reserved	-	00
320-321	Module Manufacturers ID Code	Transcend Information	01 4F
322	Module Manufacturing Location	Taipei	54
323-324	Module Manufacturing Date	Year, Week	Variable
325-328	Module Serial Number	By Manufacturer	Variable
329-348	Module Part Number	TS2GSH64V2B-I	1)
349	Module Revision Code	-	00
350-351	DRAM Manufacturer ID Code	By Manufacturer	Variable
352	DRAM Stepping	Stepping information not provided	Variable
353-381	Manufacturer Specific Data	By Manufacturer	Variable
382-383	Reserved	-	00
384-511	End User Programmable	By Manufacturer	Variable

Note:

1) The detail Model Part Number is listed as below.

Byte	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343
PN	T	S	2	G	S	H	6	4	V	2	B	-	I		
Hex	54	53	32	47	53	48	36	34	56	32	42	2D	49	20	20

Byte	344	345	346	347	348
PN					
Hex	20	20	20	20	20

2.6 AC & DC INPUT MEASUREMENT LEVELS

2.6.1 Single-ended AC & DC input levels for Command and Address

[Table 6] Single-ended AC & DC input levels for Command and Address

Parameter	Symbol	DDR4-2133/2400		DDR4-2666/2933/3200		Unit	Note
		Min	Max	Min	Max		
I/O Reference Voltage	VREFCA(DC)	0.49*VDDQ	0.51*VDDQ	0.49*VDDQ	0.51*VDDQ	V	1), 2)
DC Input Logic High	VIH(DC)	VREF+0.075	VDD	VREF+0.065	VDD	V	
DC Input Logic Low	VIL(DC)	VSS	VREF-0.075	VSS	VREF-0.065	V	
AC Input Logic High	VIH(AC)	VREF+0.1	Note 1	VREF+0.09	Note 1	V	
AC Input Logic Low	VIL(AC)	Note 1	VREF-0.1	Note 1	VREF-0.09	V	

Note:

1) The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference: approx. ± 12mV)

2) For reference: approx. VDD/2 ± 12mV

2.6.2 Differential AC and DC Input Levels

[Table 7] Differential AC and DC Input Levels

Parameter	Symbol	DDR4-2133		DDR4-2400/2666		Unit	Note
		Min	Max	Min	Max		
differential input high DC	VIHdiff(DC)	+0.150	NOTE 3	+0.135	NOTE 3	V	1
differential input low DC	VILdiff(DC)	NOTE 3	-0.150	NOTE 3	-0.135	V	1
differential input high AC	VIHdiff(AC)	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	V	2
differential input low AC	VILdiff(AC)	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	NOTE 3	2 x (V_{IL}(AC) -V_{REF})	V	2
Parameter	Symbol	DDR4-2933		DDR4-3200		Unit	Note
		Min	Max	Min	Max		
differential input high DC	VIHdiff(DC)	+0.125	NOTE 3	+0.110	NOTE 3	V	1
differential input low DC	VILdiff(DC)	NOTE 3	-0.125	NOTE 3	-0.110	V	1
differential input high AC	VIHdiff(AC)	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	V	2
differential input low AC	VILdiff(AC)	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	NOTE 3	2 x (V_{IL}(AC) -V_{REF})	V	2

Note:

1) Used to define a differential signal slew-rate.

2) For CK_t - CK_c use VIH.CA/VIL.CA(AC) of ADD/CMD and VREFCA;

3) These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits (VIH.CA(DC) max, VIL.CA(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

2.6.3 Single-ended AC & DC output levels

[Table 8] Single-ended AC & DC output levels

Parameter	Symbol	DDR4-2133/2400/2666/2933/3200	Unit	Note
DC output high measurement level	VOH(DC)	1.1 x VDDQ	V	
DC output mid measurement level	VOM(DC)	0.8 x VDDQ	V	
DC output low measurement level	VOL(DC)	0.5 x VDDQ	V	

AC output high measurement level	VOH(AC)	(0.7 + 0.15) x VDDQ	V	1)
AC output low measurement level	VOL(AC)	(0.7 - 0.15) x VDDQ	V	1)

Note:

1) The swing of ± 0.15 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ.

2.6.4 Differential AC & DC output levels

[Table 9] Single-ended AC & DC output levels

Parameter	Symbol	DDR4-2133/2400/2666/2933/3200	Unit	Note
AC differential output high measurement level	VOHdiff(AC)	+0.3 x VDDQ	V	1)
AC differential output low measurement level	VOLdiff(AC)	-0.3 x VDDQ	V	1)

Note:

1) The swing of ± 0.3 × VDDQ is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ at each of the differential outputs.

2.7 SPD EEPROM Operating Conditions

[Table 10] SPD EEPROM operating conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{CC1}	1.7	3.6	V
Supply voltage	V_{CC2}	2.2	3.6	V
Input low voltage: logic 0; all inputs	V_{IL}	-0.5	V_{CC} x 0.3	V
Input high voltage: logic 1; all inputs	V_{IH}	V_{CC} x 0.7	V_{CC} + 0.5	V
Output low voltage: 3mA sink current V_{CC} > 2V	V_{OL}		0.4	V
Input leakage current: (SCL, SDA) V_{IN} = V_{CC} or V_{SS}	I_{LI}		+/- 5	uA
Output leakage current: V_{OUT} = V_{CC} or V_{SS}	I_{LO}		+/- 5	uA

2.8Environment Specifications

[Table 11] Operating Temperature condition

Symbol	Parameter	Rating	Unit	Note
T_{OPER}	Operating Temperature	-40 to 85	C	1),2)
H_{OPER}	Operating Humidity (relative)	10 to 90	%	
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	3)

Note:

1) Operating Temperature is the ambient temperature.

2) At -40 ~ 85 C, operation temperature range is the temperature which all DRAM specification will be supported.

3) Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2.9 System Reliability

[Table 12] Telcordia SR332 issue 4 MTBF Specifications

Parameter	TS2GSH64V2B-I-ARW
MTBF	3,000,000 hours

Note:

1) The calculation is based on 25 C.

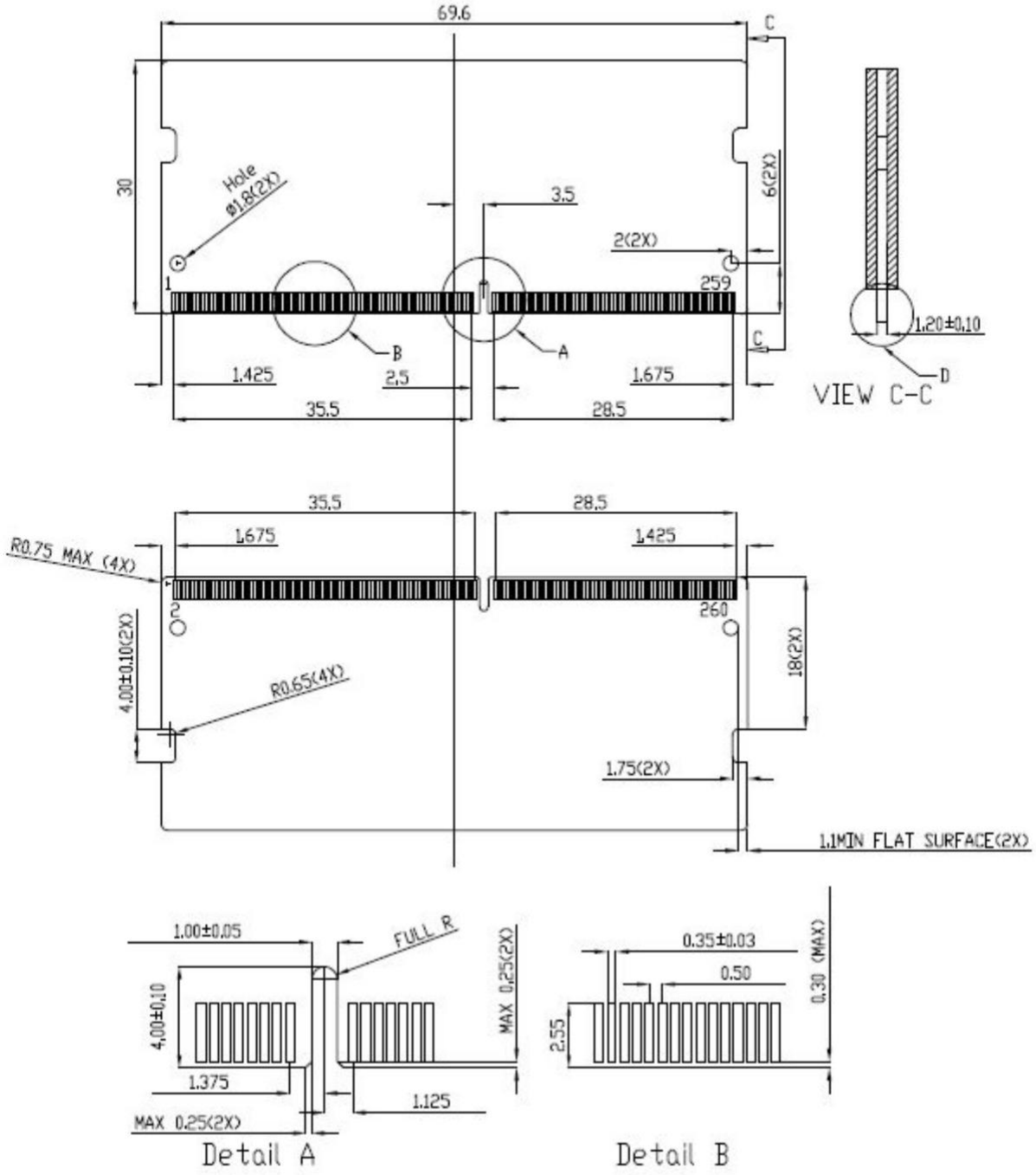
[Table 13] Warranty

Parameter	TS2GSH64V2B-I-ARW
Warranty	Limited Lifetime Warranty

3 Mechanical Specification

The figure below illustrates the Transcend DDR4 wide-temperature SO-DIMM. [Table 14] Physical Dimensions and Weight

Model	Thickness (mm)	Length (mm)	Height (mm)	Weight (gram)
TS2GSH64V2B-I	Max3.7	69.60 0.15	30.00 0.15	NA



4 Pin Assignments

4.1 Pin Assignments

[Table 15] Pin Assignments

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VSS	89	VSS	177	DQS4_c	02	VSS	90	VSS	178	DM4_n, DBI4_n,NC
03	DQ5	91	CB1/NC	179	DQS4_t	04	DQ4	92	CB0/NC	180	VSS
05	VSS	93	VSS	181	VSS	06	VSS	94	VSS	182	DQ39
07	DQ1	95	DQS8_c	183	DQ38	08	DQ0	96	DM8_n, DBI_n,NC	184	VSS
09	VSS	97	DQS8_t	185	VSS	10	VSS	98	VSS	186	DQ35
11	DQS0_c	99	VSS	187	DQ34	12	DM0_n, DBI0_n,NC	100	CB6/NC	188	VSS
13	DQS0_t	101	CB2/NC	189	VSS	14	VSS	102	VSS	190	DQ45
15	VSS	103	VSS	191	DQ44	16	DQ6	104	CB7/NC	192	VSS
17	DQ7	105	CB3/NC	193	VSS	18	VSS	106	VSS	194	DQ41
19	VSS	107	VSS	195	DQ40	20	DQ2	108	RESET_n	196	VSS
21	DQ3	109	CKE0	197	VSS	22	VSS	110	CKE1	198	DQS5_c
23	VSS	111	VDD	199	DM5_n, DBI5_n,NC	24	DQ12	112	VDD	200	DQS5_t
25	DQ13	113	BG1	201	VSS	26	VSS	114	ACT_n	202	VSS
27	VSS	115	BG0	203	DQ46	28	DQ8	116	ALERT_n	204	DQ47
29	DQ9	117	VDD	205	VSS	30	VSS	118	VDD	206	VSS
31	VSS	119	A12	207	DQ42	32	DQS1_c	120	A11	208	DQ43
33	DM1_n, DBI_n,NC	121	A9	209	VSS	34	DQS1_t	122	A7	210	VSS
35	VSS	123	VDD	211	DQ52	36	VSS	124	VDD	212	DQ53
37	DQ15	125	A8	213	VSS	38	DQ14	126	A5	214	VSS
39	VSS	127	A6	215	DQ49	40	VSS	128	A4	216	DQ48
41	DQ10	129	VDD	217	VSS	42	DQ11	130	VDD	218	VSS
43	VSS	131	A3	219	DQS6_c	44	VSS	132	A2	220	DM6_n, DBI6_n,NC
45	DQ21	133	A1	221	DQS6_t	46	DQ20	134	EVENT_n	222	VSS
47	VSS	135	VDD	223	VSS	48	VSS	136	VDD	224	DQ54
49	DQ17	137	CK0_t	225	DQ55	50	DQ16	138	CK1_t	226	VSS
51	VSS	139	CK0_c	227	VSS	52	VSS	140	CK1_c	228	DQ50
53	DQS2_c	141	VDD	229	DQ51	54	DM2_n/ DBI2_n,NC	142	VDD	230	VSS
55	DQS2_t	143	PARITY	231	VSS	56	VSS	144	A0	232	DQ60
57	VSS	145	BA1	233	DQ61	58	DQ22	146	A10/AP	234	VSS
59	DQ23	147	VDD	235	VSS	60	VSS	148	VDD	236	DQ57

61	VSS	149	CS0_n	237	DQ56	62	DQ18	150	BA0	238	VSS
63	DQ19	151	WE_n/ A14	239	VSS	64	VSS	152	RAS_n/ A16	240	DQS7_c
65	VSS	153	VDD	241	DM7_n,DBI 7_n,NC	66	DQ28	154	VDD	242	DQS7_t
67	DQ29	155	ODT0	243	VSS	68	VSS	156	CAS_n/ A15	244	VSS
69	VSS	157	CS1_n	245	DQ62	70	DQ24	158	A13	246	DQ63
71	DQ25	159	VDD	247	VSS	72	VSS	160	VDD	248	VSS
73	VSS	161	ODT1	249	DQ58	74	DQS3_c	162	C0, CS2_n,NC	250	DQ59
75	DM3_n, DBI3_n,NC	163	VDD	251	VSS	76	DQS3_t	164	VREFCA	252	VSS
77	VSS	165	C1, CS3_n, NC	253	SCL	78	VSS	166	SA2	254	SDA
79	DQ30	167	VSS	255	VDDSPD	80	DQ31	168	VSS	256	SA0
81	VSS	169	DQ37	257	VPP	82	VSS	170	DQ36	258	VTT
83	DQ26	171	VSS	259	VPP	84	DQ27	172	VSS	260	SA1
85	VSS	173	DQ33	-	-	86	VSS	174	DQ32	-	-
87	CB5/NC	175	VSS	-	-	88	CB4/NC	176	VSS	-	-

Note:

1) DM0_n–DM8_n,DBI0_n-DBI8_n:x8-based x72 DIMMs

2) CB0–CB7:DIMM ECC check bits

3) EVENT_n:only supports ECC SO-DIMMs (x72)

4.2Pin Description

[Table 16] Pin Description

Pin Name	Description
A0–A15	SDRAM address bus
BA0, BA1	SDRAM bank select
BG0, BG1	SDRAM bank group select
RAS_n	SDRAM row address strobe
CAS_n	SDRAM column address strobe
WE_n	SDRAM write enable
CS0_n, CS1_n CS2_n, CS3_n	DIMM Rank Select Lines
CKE0, CKE1	SDRAM clock enable lines
ODT0, ODT1	SDRAM on-die termination control lines
ACT_n	SDRAM activate
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits

Pin Name	Description
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)
PARITY	SDRAM parity input
VDD	SDRAM I/O and core power supply
VREFCA	SDRAM command/address reference supply
VSS	Power supply return (ground)
VDDSPD	Serial SPD positive power supply
SCL	I^2C serial bus clock for
SDA	I^2C serial bus data line for
SA0–SA	I^2C slave address select for
ALERT_n	SDRAM ALERT_n
VPP	SDRAM Supply

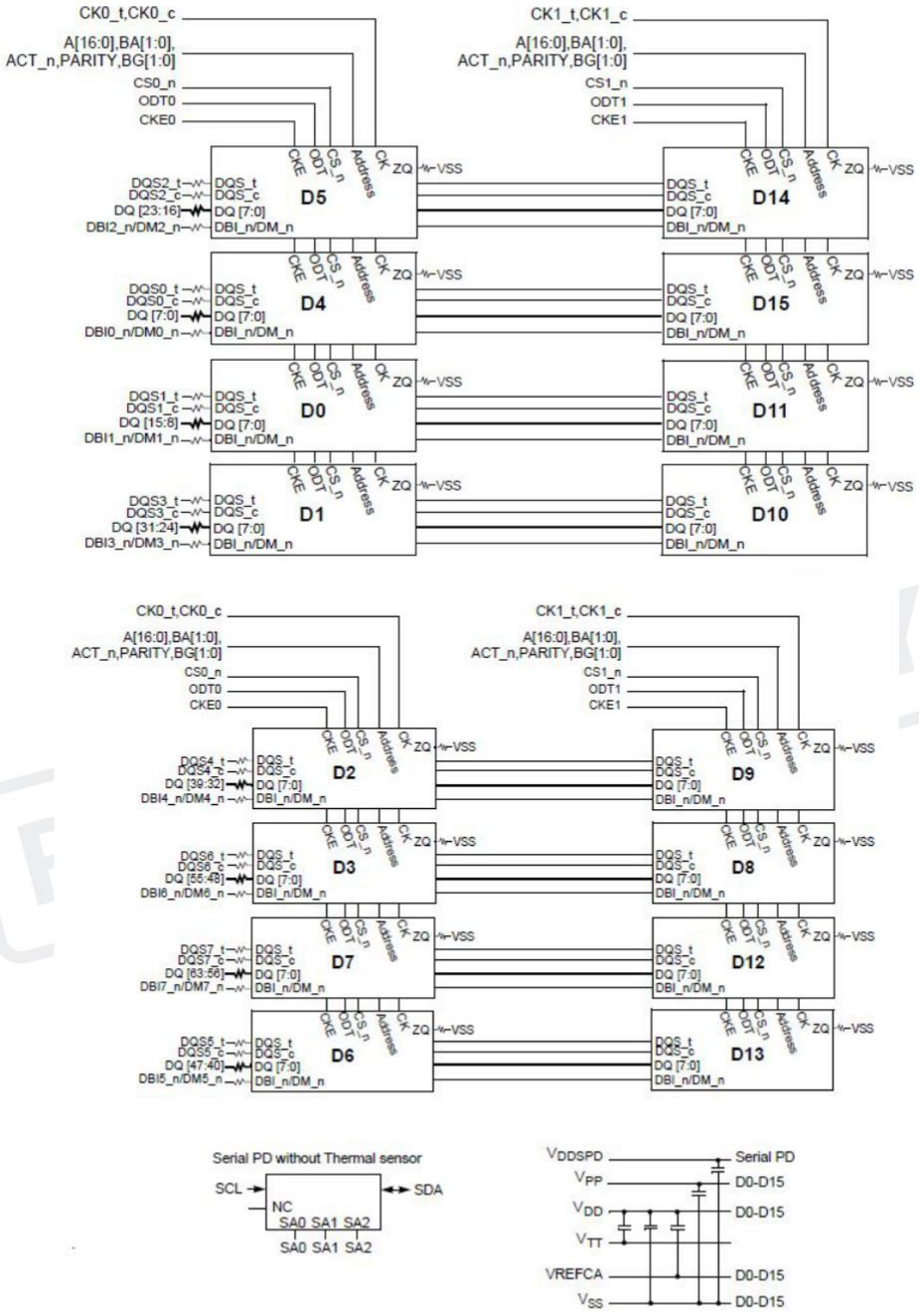
DM_n/DBI_n/	Input data mask and data bus inversion
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)

RESET_n	Set DRAMs to a Known State
EVENT_n	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use
NC	No Connection
NF	No function
C0,C1	Chip ID lines for 3DS components

5 Block Diagram

5.1 Block Diagram

16GB, 2G x 64 Module (2 Rank x 8) TS2GSH64V2B-I



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