

**TOSHIBA**

TOSHIBA Original CMOS 32-Bit Microcontroller

**TLCS-900/H1 Series**

**TMP92CF30FG**

**TOSHIBA CORPORATION**

Semiconductor Company

## Preface

Thank you very much for making use of Toshiba microcomputer LSIs.  
Before use this LSI, refer the section, "Notes and Restrictions".

## CMOS 32-Bit Microcontroller TMP92CF30FG

### 1. Outline and Features

The TMP92CF30 is a high-speed advanced 32-bit microcontroller developed for controlling equipment which processes mass data.

The TMP92CF30FG is housed in a 176-pin QFP package.

- (1) CPU: 32-bit CPU (High-speed 900/H1 CPU)
  - Compatible with TLCS-900/L1 instruction code
  - 16 Mbytes of linear address space
  - General-purpose register and register banks
  - Micro DMA: 8channels (62.5 ns/4 bytes at  $f_{SYS} = 80$  MHz, best case)
- (2) Minimum instruction execution time : 12.5 ns (at  $f_{SYS} = 80$  MHz)
- (3) Internal RAM: 144 Kbytes (can be used for program and data)  
Internal ROM: None
- (4) External memory expansion
  - Expandable up to 2.1 Gbytes (shared program/data area)
  - Can simultaneously support 8-, 16- and 32-bit width external data buses  
..... Dynamic data bus sizing
  - Separate bus system
- (5) Memory controller
  - Chip select output: 4 channels
  - One channel in 4 channels is enabled detailed AC enable setting
- (6) 8-bit timers: 8 channels
- (7) 16-bit timer/event counter: 2 channels
- (8) General-purpose serial interface: 2 channels
  - UART/synchronous mode: 2 channels
  - IrDA ver.1.0 (115.2 kbps) selectable
- (9) Serial bus interface: 1 channel
  - I<sup>2</sup>C standard mode only
- (10) USB (universal serial bus) controller: 1 channel
  - Full-speed (12 Mbps) (Low-speed is not supported.)
  - Endpoint 0: Control 64 bytes × 1 FIFO  
Endpoint 1: BULK (output) 64 bytes × 2 FIFOs  
Endpoint 2: BULK (input) 64 bytes × 2 FIFOs  
Endpoint 3: Interrupt (input) 8 bytes × 1 FIFO
  - Descriptor RAM: 384 bytes

- (11) I<sup>2</sup>S (Inter-IC Sound) interface: 1 channel
  - I<sup>2</sup>S bus mode selectable (Master, transmission only)
  - Data Format is supported Left/Right Justify
  - 128-byte FIFO buffer (64 bytes × 2)
- (12) SDRAM controller: 1 channel
  - Supports 16-Mbit, 64-Mbit, 128-Mbit, 256-Mbit and 512-Mbit SDR (Single-data-rate) SDRAM
  - Possible to execute instruction on SDRAM
- (13) Timer for real-time clock (RTC)
  - Based on TC8521A
- (14) Key-on wakeup (Interrupt key input)
- (15) 10-bit A/D converter (Built in Sample Hold circuit): 6 channels
- (16) Touch screen interface
  - Built-in Switch of Low-resistor, and available to reduce external components for shift change row/column
- (17) Watchdog timer
- (18) Melody/alarm generator
  - Melody: Output of a clock 4 to 5461-Hz clock
  - Alarm: Output of 8 kinds of alarm pattern
  - 5 kinds of interval interrupt
- (19) MMU
  - Expandable up to 2.1 Gbytes (3 local area/8 bank method)
  - Independent bank for each program, read data, write data, source and destination of DMAC (Odd channel/Even channel)
- (20) Interrupts: 58 interrupts
  - 9 CPU interrupts: Software interrupt instruction and illegal instruction
  - 39 internal interrupts: Seven selectable priority levels
  - 10 external interrupts: Seven selectable priority levels (include key and  $\overline{\text{NMI}}$  interrupt)  
(8-edge selectable)
- (21) DMAC function: 6 channels
  - High-speed data transfer enable by controlling which convert micro DMA function and this function
- (22) Input/Output ports: 98 pins (Except Data bus (16bit), Address bus (24bit) and  $\overline{\text{RD}}$  pin)
- (23) NAND Flash interface: 2 channels
  - Direct NAND flash connection capability
  - Supports SLC type and MLC type
  - Supports Data Bus 8/16 bit, Page Size 512/2048 bytes
  - Built-in Reed Solomon calculation circuits which enabled correct 4-address, and detect error more than 5-address

## (24) SPI controller: 1 channel

- Supports SPI mode of SD card and MMC card
- Built-in FIFO buffer of 32 bytes to each Input/Output

## (25) Product/Sum calculation: 1 channel

- Supports calculation  $32 \times 32 + 64 = 64$  bits,  $64 - 32 \times 32 = 64$  bits and  $32 \times 32 - 64 = 64$  bits
- I/O method
- Supports Signed calculations

## (26) Standby function

- Three Halt modes: IDLE2 (programmable), IDLE1, STOP
- Each pin status programmable for standby mode

## (27) Clock controller

- Two blocks of clock doubler (PLL) supplies 48 MHz for USB and 80 MHz for CPU from 10 MHz
- Clock gear function: Selectable high-frequency clock  $f_c$  to  $f_c/16$
- Clock for Timer ( $f_s = 32.768$  kHz)

## (28) Operating voltage:

- 2 power supplies (Internal power supply (1.4 to 1.6 V), External power supply (3.0 to 3.6 V))

## (29) Package

- 176-pin LQFP: LQFP176-P-2020-0.40F

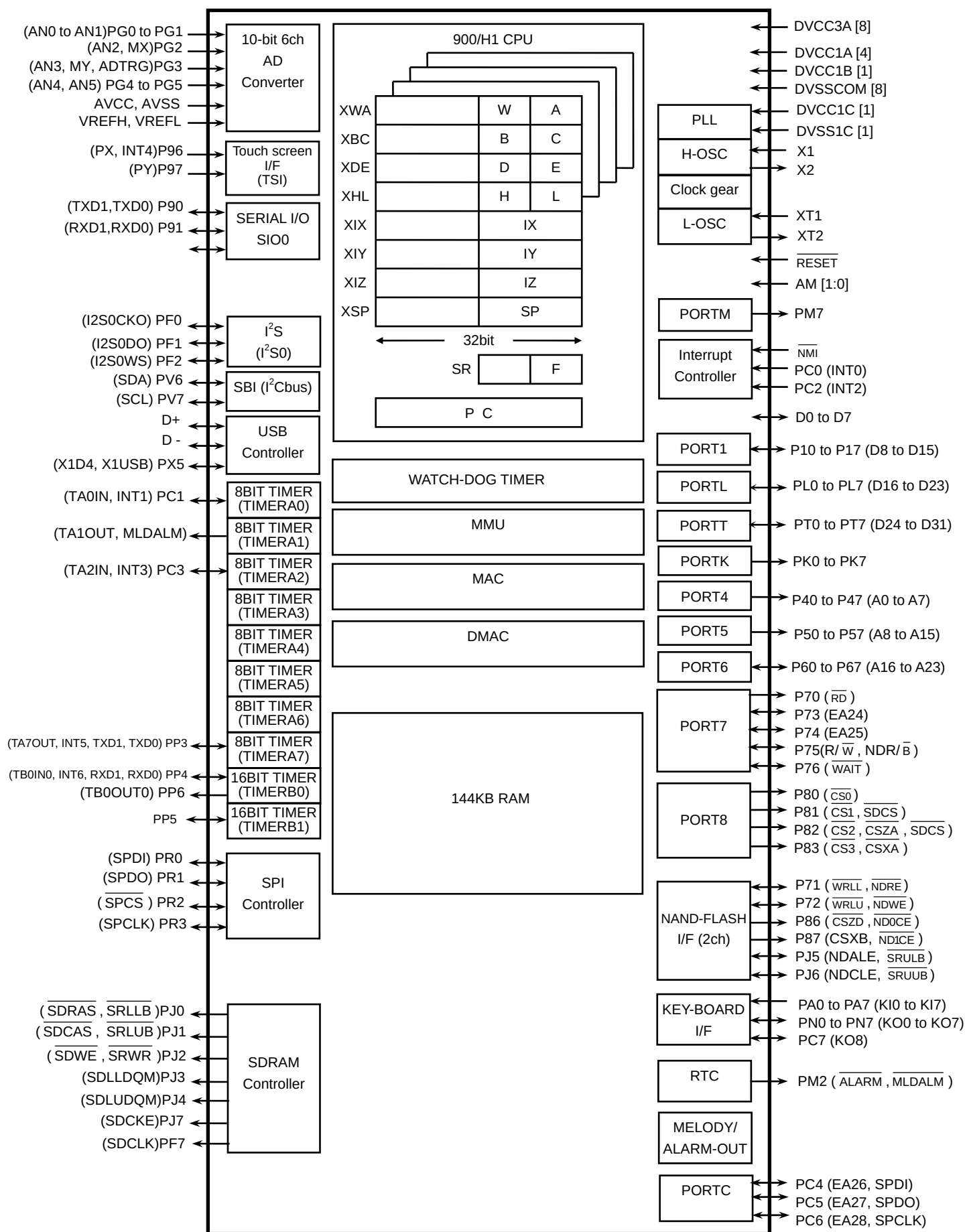


Figure 1.1 Block Diagram of TMP92CF30

## 2. Pin Assignment and Pin Functions

The assignment of input/output pins for TMP92CF30, their names and functions are as follows:

### 2.1 Pin Assignment Diagram (Top View)

Figure 2.1.1 shows the pin assignment of the TMP92CF30.

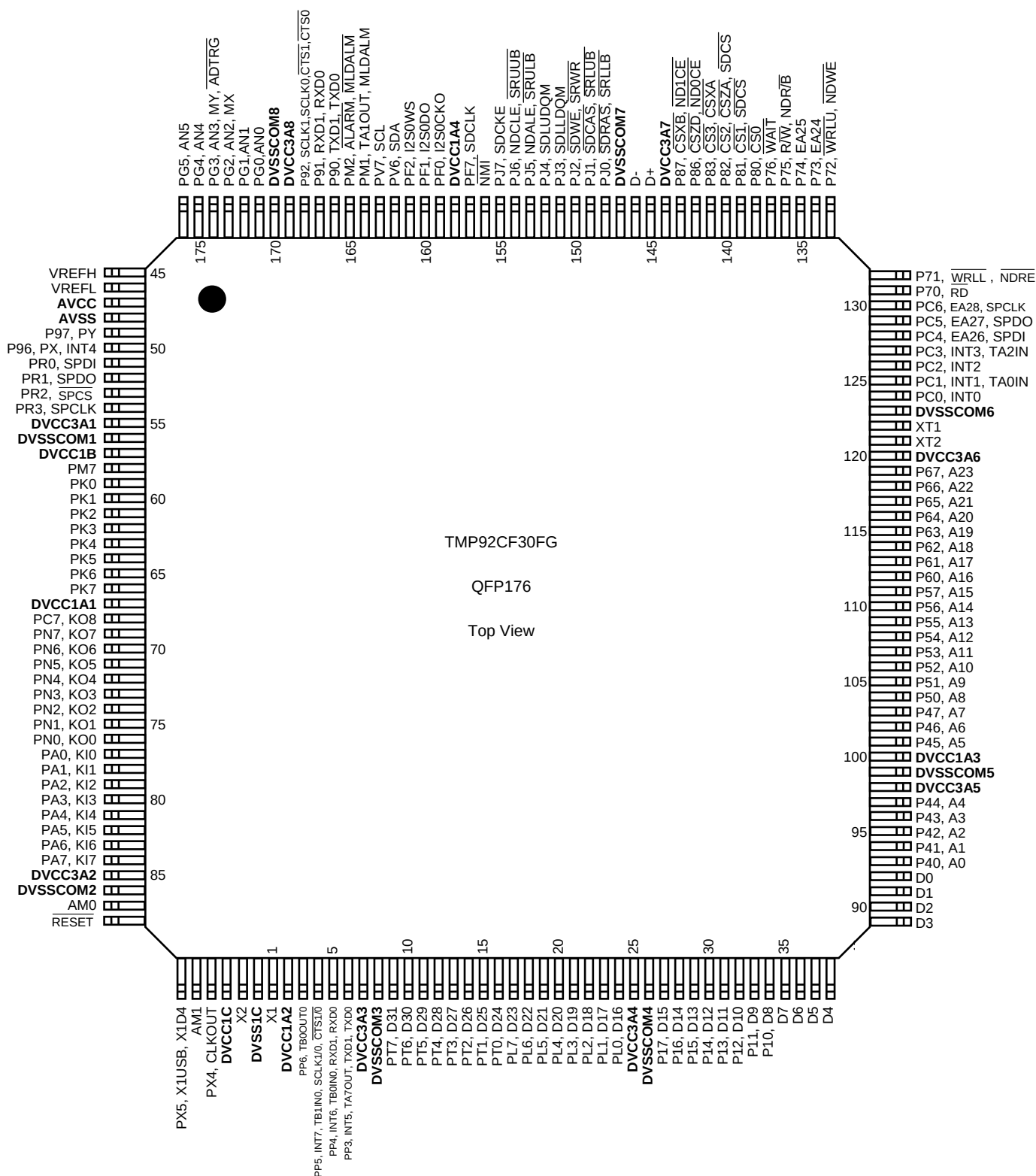


Figure 2.1.1 Pin assignment diagram (P-FBGA228)

## 2.2 Pin names and Functions

The names of the input/output pins and their functions are described below.

Table 2.2.1 Pin names and functions (1/6)

| Pin name                                                          | Number of Pins | I/O                                  | Functions                                                                                                                                                                                                                                                                    |
|-------------------------------------------------------------------|----------------|--------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D0 to D7                                                          | 8              | I/O                                  | Data: Data bus D0 to D7                                                                                                                                                                                                                                                      |
| P10 to P17<br>D8 to D15                                           | 8              | I/O<br>I/O                           | Port 1: I/O port input or output specifiable in units of bits<br>Data: Data bus D8 to D15                                                                                                                                                                                    |
| P40 to P47<br>A0 to A7                                            | 8              | Output<br>Output                     | Port 4: Output port<br>Address: Address bus A0 to A7                                                                                                                                                                                                                         |
| P50 to P57<br>A8 to A15                                           | 8              | Output<br>Output                     | Port 5: Output port<br>Address: Address bus A8 to A15                                                                                                                                                                                                                        |
| P60 to P67<br>A16 to A23                                          | 8              | I/O<br>Output                        | Port 6: I/O port input or output specifiable in units of bits<br>Address: Address bus A16 to A23                                                                                                                                                                             |
| P70<br>$\overline{RD}$                                            | 1              | Output<br>Output                     | Port 70: Output port<br>Read: Outputs strobe signal to read external memory                                                                                                                                                                                                  |
| P71<br>$\overline{WRLL}$<br>$\overline{NDRE}$                     | 1              | I/O<br>Output<br>Output              | Port 71: Output port<br>Write: Outputs strobe signal for writing data on pins D0 to D7<br>NAND Flash read: Outputs strobe signal to read external NAND-Flash                                                                                                                 |
| P72<br>$\overline{WRLU}$<br>$\overline{NDWE}$                     | 1              | I/O<br>Output<br>Output              | Port 72: I/O port<br>Write: Outputs strobe signal for writing data on pins D8 to D15<br>NAND Flash write: Write enable for NAND Flash                                                                                                                                        |
| P73<br>EA24                                                       | 1              | I/O<br>Output                        | Port 73: I/O port<br>Expanded address 24                                                                                                                                                                                                                                     |
| P74<br>EA25                                                       | 1              | I/O<br>Output                        | Port 74: I/O port<br>Expanded address 25                                                                                                                                                                                                                                     |
| P75<br>$R/\overline{W}$<br>$\overline{NDR}/\overline{B}$          | 1              | I/O<br>Output<br>Input               | Port 75: I/O port<br>Read/Write: "High" represents read or dummy cycle; "Low" represents write cycle<br>NAND Flash Ready(1) / Busy(0) input                                                                                                                                  |
| P76<br>$\overline{WAIT}$                                          | 1              | I/O<br>Input                         | Port 76: I/O port<br>Wait: Signal used to request CPU bus wait                                                                                                                                                                                                               |
| P80<br>$\overline{CS0}$                                           | 1              | Output<br>Output                     | Port 80: Output port<br>Chip select 0: Outputs "Low" when address is within specified address area                                                                                                                                                                           |
| P81<br>$\overline{CS1}$<br>$\overline{SDCS}$                      | 1              | Output<br>Output<br>Output           | Port 81: Output port<br>Chip select 1: Outputs "Low" when address is within specified address area<br>Chip select for SDRAM: Outputs "Low" when the address is within SDRAM address area                                                                                     |
| P82<br>$\overline{CS2}$<br>$\overline{CSZA}$<br>$\overline{SDCS}$ | 1              | Output<br>Output<br>Output<br>Output | Port 82: Output port<br>Chip select 2: Outputs "Low" when address is within specified address area<br>Expanded address ZA: Outputs "Low" when address is within specified address area<br>Chip select for SDRAM: Outputs "Low" when the address is within SDRAM address area |
| P83<br>$\overline{CS3}$<br>$\overline{CSXA}$                      | 1              | Output<br>Output<br>Output           | Port 83: Output port<br>Chip select 3: Outputs "Low" when address is within specified address area<br>Expanded address XA: Outputs "Low" when address is within specified address area                                                                                       |



Table 2.2.1 Pin names and functions (2/6)

| Pin name                                            | Number of Pins | I/O                                 | Functions                                                                                                                                                                                                  |
|-----------------------------------------------------|----------------|-------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| P86<br><u>CSZD</u><br><u>ND0CE</u>                  | 1              | Output<br>Output<br>Output          | Port 86: Output port<br>Expanded address ZD: Outputs "Low" when address is within specified address area<br>Chip select for NAND Flash 0: Outputs "Low" when NAND Flash 0 is enable                        |
| P87<br><u>CSXB</u><br><u>ND1CE</u>                  | 1              | Output<br>Output<br>Output          | Port 87: Output port<br>Expanded address XB: Outputs "Low" when address is within specified address area<br>Chip select for NAND Flash 1: Outputs "Low" when NAND Flash 1 is enable                        |
| P90<br>TXD0<br>TXD1                                 | 1              | I/O<br>Output<br>Output             | Port 90: I/O port<br>Transmit data for serial 0: programmable Open-drain output<br>Transmit data for serial 1: programmable Open-drain output                                                              |
| P91<br>RXD0<br>RXD1                                 | 1              | I/O<br>Input<br>Input               | Port 91: I/O port (Schmitt-input)<br>Receive data for serial 0<br>Receive data for serial 1                                                                                                                |
| P92<br>SCLK0<br><u>CTS0</u><br>SCLK0<br><u>CTS0</u> | 1              | I/O<br>I/O<br>Input<br>I/O<br>Input | Port 92: I/O port (Schmitt-input)<br>Clock I/O for serial 0<br>Enable to send data for serial 0 (Clear to send)<br>Clock I/O for serial 1<br>Enable to send data for serial 1 (Clear to send)              |
| P96<br>INT4<br>PX                                   | 1              | Input<br>Input<br>Output            | Port 96: Input port (schmitt-input, with pull-up resistor)<br>Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge<br>X-Plus: Pin connected to X+ pin for Touch Screen I/F |
| P97<br>PY                                           | 1              | Input<br>Output                     | Port 97: Input port (schmitt input)<br>Y-Plus: Pin connected to Y+ pin for Touch Screen I/F                                                                                                                |
| PA0 to PA7<br>KI0 to KI7                            | 8              | Input<br>Input                      | Port A0 to A7: Input port<br>Key input 0 to 7: Pin used for key on wake-up 0 to 7 (Schmitt-input, with pull-up resistor)                                                                                   |
| PC0<br>INT0                                         | 1              | I/O<br>Input                        | Port C0: I/O port (Schmitt-input)<br>Interrupt request pin 0: Interrupt request pin with programmable rising/falling edge                                                                                  |
| PC1<br>INT1<br>TA0IN                                | 1              | I/O<br>Input<br>Input               | Port C1: I/O port (Schmitt-input)<br>Interrupt request pin 1: Interrupt request pin with programmable rising/falling edge<br>Timer A0 input: Input pin for 8 bit timer 0                                   |
| PC2<br>INT2                                         | 1              | I/O<br>Input                        | Port C2: I/O port (Schmitt-input)<br>Interrupt request pin 2: Interrupt request pin with programmable rising/falling edge                                                                                  |
| PC3<br>INT3<br>TA2IN                                | 1              | I/O<br>Input<br>Input               | Port C3: I/O port (Schmitt-input)<br>Interrupt request pin 3: Interrupt request pin with programmable rising/falling edge<br>Timer A2 input: Input pin for 8 bit timer 2                                   |
| PC4<br>EA26<br>SPDI                                 | 1              | I/O<br>Output<br>Input              | Port C4: I/O port<br>Expanded address 26<br>Data input pin for SD card                                                                                                                                     |
| PC5<br>EA27<br>SPDO                                 | 1              | I/O<br>Output<br>Output             | Port C5: I/O port<br>Expanded address 27<br>Data output pin for SD card                                                                                                                                    |
| PC6<br>EA28<br>SPCLK                                | 1              | I/O<br>Output<br>Output             | Port C6: I/O port<br>Expanded address 28<br>Clock output pin for SD card                                                                                                                                   |
| PC7<br>KO8                                          | 1              | I/O<br>Output                       | Port C7: I/O port<br>Key output 8: Key scan strobe pin (programmable Open-drain output)                                                                                                                    |

Table 2.2.1 Pin names and functions (3/6)

| Pin name                  | Number of Pins | I/O                               | Functions                                                                                                                                                                    |
|---------------------------|----------------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PF0<br>I2S0CKO            | 1              | I/O<br>Output                     | Port F0: I/O port<br>Outputs clock for I <sup>2</sup> S0                                                                                                                     |
| PF1<br>I2S0DO             | 1              | I/O<br>Output                     | Port F1: I/O port<br>Outputs data for I <sup>2</sup> S0                                                                                                                      |
| PF2<br>I2S0WS             | 1              | I/O<br>Output                     | Port F2: I/O port<br>Outputs word select signal for I <sup>2</sup> S0                                                                                                        |
| PF7<br>SDCLK              | 1              | Output<br>Output                  | Port F7: Output port<br>Clock for SDRAM                                                                                                                                      |
| PG0 to PG1<br>AN0 to AN1  | 2              | Input<br>Input                    | Port G0 to G1: Input port<br>Analog input pin 0 to 1: Input pin for AD converter                                                                                             |
| PG2<br>AN2<br>MX          | 1              | Input<br>Input<br>Output          | Port G2: Input port<br>Analog input pin 2: Input pin for AD converter<br>X-Minus: Pin connected to X- pin for Touch Screen I/F                                               |
| PG3<br>AN3<br>MY<br>ADTRG | 1              | Input<br>Input<br>Output<br>Input | Port G3: Input port<br>Analog input pin 3: Input pin for A/D converter<br>Y-Minus: Pin connected to Y- pin for Touch Screen I/F<br>A/D Trigger: Request signal for A/D start |
| PG4 to PG5<br>AN4 to AN5  | 2              | Input<br>Input                    | Port G4 to G5: Input port<br>Analog input pin 4 to 5: Input pin for A/D converter                                                                                            |
| PJ0<br>SDRAS<br>SRLLB     | 1              | Output<br>Output<br>Output        | Port J0: Output port<br>Outputs strobe signal for SDRAM row address<br>Data enable signal for D0 to D7 for SRAM                                                              |
| PJ1<br>SDCAS<br>SRLUB     | 1              | Output<br>Output<br>Output        | Port J1: Output port<br>Outputs strobe signal for SDRAM column address<br>Data enable signal for D8 to D15 for SRAM                                                          |
| PJ2<br>SDWE<br>SRWR       | 1              | Output<br>Output<br>Output        | Port J2: Output port<br>Outputs write enable signal for SDRAM<br>Write enable for SRAM: Outputs strobe signal to write data                                                  |
| PJ3<br>SDLLDQM            | 1              | Output<br>Output                  | Port J3: Output port<br>Data enable signal for D0 to D7 for SDRAM                                                                                                            |
| PJ4<br>SDLUDQM            | 1              | Output<br>Output                  | Port J4: Output port<br>Data enable signal for D8 to D15 for SDRAM                                                                                                           |
| PJ5<br>NDALE<br>SDULB     | 1              | I/O<br>Output<br>Output           | Port J5: I/O port<br>Address latch enable signal for NAND Flash<br>Data enable signal for D16 to D23 for SDRAM                                                               |
| PJ6<br>NDCLE<br>SDUUB     | 1              | I/O<br>Output<br>Output           | Port J6: I/O port<br>Command latch enable signal for NAND Flash<br>Data enable signal for D24 to D31 for SDRAM                                                               |
| PJ7<br>SDCKE              | 1              | Output<br>Output                  | Port J7: Output port<br>Clock enable signal for SDRAM                                                                                                                        |

Table 2.2.1 Pin names and functions (4/6)

| Pin name                                                | Number of Pins | I/O                                                   | Functions                                                                                                                                                                                                                                                                                                                             |
|---------------------------------------------------------|----------------|-------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PK0 to PK7                                              | 8              | Output                                                | Port K0 to PK7: Output port                                                                                                                                                                                                                                                                                                           |
| PL0 to PL7<br>D16 to D23                                | 8              | I/O<br>Output                                         | Port L0 to L7: I/O port<br>Data bus D16 to D23                                                                                                                                                                                                                                                                                        |
| PM1<br>TA1OUT<br>MLDALM                                 | 1              | Output<br>Output<br>Output                            | Port M1: Output port<br>Timer A1 output: Output pin for 8 bit timer 1<br>Melody / Alarm output pin                                                                                                                                                                                                                                    |
| PM2<br>ALARM<br>MLDALM                                  | 1              | Output<br>Output<br>Output                            | Port M2: Output port<br>Alarm output from RTC<br>Melody / Alarm output pin (inverted)                                                                                                                                                                                                                                                 |
| PM7                                                     | 1              | Output                                                | Port M7: Output port                                                                                                                                                                                                                                                                                                                  |
| PN0 to PN7<br>K00 to K07                                | 8              | I/O<br>Output                                         | Port N: I/O port<br>Key output 0 to 7: Key scan strobe pin (programmable Open-drain output)                                                                                                                                                                                                                                           |
| PP3<br>INT5<br>TA7OUT<br>TXD0<br>TXD1                   | 1              | I/O<br>Input<br>Output<br>Output<br>Output            | Port P3: I/O port (Schmitt-input)<br>Interrupt request pin 5: Interrupt request pin with programmable rising/falling edge<br>Timer A7 output: Output pin for 8 bit timer 7<br>Transmit data for serial 0: programmable Open-drain output<br>Transmit data for serial 1: programmable Open-drain output                                |
| PP4<br>INT6<br>TB0IN0<br>RXD0<br>RXD1                   | 1              | I/O<br>Input<br>Input<br>Input<br>Input               | Port P4: I/O port (Schmitt-input)<br>Interrupt request pin 6: Interrupt request pin with programmable rising/falling edge<br>Timer B0 input: Input pin for 16 bit timer 0<br>Receive data for serial 0<br>Receive data for serial 1                                                                                                   |
| PP5<br>INT7<br>TB1IN0<br>SCLK0<br>CTS0<br>SCLK1<br>CTS1 | 1              | I/O<br>Input<br>Input<br>I/O<br>Input<br>I/O<br>Input | Port P5: I/O port (Schmitt-input)<br>Interrupt request pin 7: Interrupt request pin with programmable rising/falling edge<br>Timer B1 input: Input pin for 16 bit timer 1<br>Clock I/O for serial 0<br>Enable to send data for serial 0 (Clear to send)<br>Clock I/O for serial 1<br>Enable to send data for serial 1 (Clear to send) |
| PP6<br>TB0OUT0                                          | 1              | Output<br>Output                                      | Port P6: I/O port<br>Timer B0 output: Output pin for 16 bit timer 0                                                                                                                                                                                                                                                                   |

Table 2.2.1 Pin names and functions (5/6)

| Pin name                        | Number of Pins | I/O                    | Functions                                                               |
|---------------------------------|----------------|------------------------|-------------------------------------------------------------------------|
| PR0<br>SPDI                     | 1              | I/O<br>Input           | Port R0: I/O port<br>Data input pin for SD card                         |
| PR1<br>SPDO                     | 1              | I/O<br>Output          | Port R1: I/O port<br>Data output pin for SD card                        |
| PR2<br>$\overline{\text{SPCS}}$ | 1              | I/O<br>Output          | Port R2: I/O port<br>Chip select signal for SD card                     |
| PR3<br>SPCLK                    | 1              | I/O<br>Output          | Port R3: I/O port<br>Clock output pin for SD card                       |
| PT0 to PT7<br>D24 to D31        | 8              | I/O<br>I/O             | Port T0 to T7: I/O port<br>Data: Data bus D24 to D31                    |
| PV6<br>SDA                      | 1              | I/O<br>I/O             | Port V6: I/O port<br>Send/receive data at I <sup>2</sup> C mode         |
| PV7<br>SCL                      | 1              | I/O<br>I/O             | Port V7: I/O port<br>Input/output clock at I <sup>2</sup> C mode        |
| PX4<br>CLKOUT                   | 1              | Output<br>Output       | Port X4: Output port<br>Internal clock output pin                       |
| PX5<br>X1USB<br>X1D4            | 1              | I/O<br>Input<br>Output | Port X5: I/O port<br>Clock input pin for USB<br>Direct clock output pin |

Table 2.2.1 Pin names and functions (6/6)

| Pin name                | Number of Pins | I/O   | Functions                                                                                                                                                                                                                                               |
|-------------------------|----------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D+, D-                  | 2              | I/O   | USB-data connecting pin<br>Connect pull-up(DVCC3A) or pull-down resistor to both pins to avoid through current when USB is not in use.                                                                                                                  |
| $\overline{\text{NMI}}$ | 1              | Input | Non-maskable interrupt pin.                                                                                                                                                                                                                             |
| AM1, AM0                | 2              | Input | Operation mode;<br>Fix to AM1 = "0", AM0 = "1" for 16 bit external bus starting<br>Fix to AM1 = "1", AM0 = "0" for 32 bit external bus starting<br>Fix to AM1 = "1", AM0 = "1" is prohibited to set<br>Fix to AM1 = "0", AM0 = "0" is prohibited to set |
| X1/X2                   | 2              | I/O   | High-frequency oscillator circuit connection pin                                                                                                                                                                                                        |
| XT1/XT2                 | 2              | I/O   | Low-frequency oscillator circuit connection pin                                                                                                                                                                                                         |
| RESET                   | 1              | Input | Reset: Initialize TMP92CF30 (Schmitt-input , with pull-up resistor)                                                                                                                                                                                     |
| VREFH                   | 1              | Input | Pin for reference voltage input to AD converter(H)                                                                                                                                                                                                      |
| VREFL                   | 1              | Input | Pin for reference voltage input to AD converter(L)                                                                                                                                                                                                      |
| AVCC                    | 1              | –     | Power supply pin for AD converter                                                                                                                                                                                                                       |
| AVSS                    | 1              | –     | GND pin for AD converter (0V)                                                                                                                                                                                                                           |
| DVCC3A                  | 8              | –     | Power supply pin for peripheral I/O-A (All DVCC3A pins should be connected to the power supply pin )                                                                                                                                                    |
| DVCC1A                  | 4              | –     | Power supply pin for internal logic-A (All DVCC1A pins should be connected to the power supply pin )                                                                                                                                                    |
| DVCC1B                  | 1              | –     | Power supply pin for internal logic-B (Keep the voltage DVCC1A level )                                                                                                                                                                                  |
| DVSSCOM                 | 8              | –     | GND pin (0V) (All DVSS pins should be connected to GND(0V))                                                                                                                                                                                             |
| DVCC1C                  | 1              | –     | Power supply pin for High speed oscillator (Keep the voltage DVCC1A level )                                                                                                                                                                             |
| DVSS1C                  | 1              | –     | GND pin (0V) (DVSS1C pin should be connected to GND(0V))                                                                                                                                                                                                |

Table 2.2.2 shows the range of operational voltage for power supply pins.

Table 2.2.2 the range of operational voltage for power supply pins

| Power supply pin | Range of operational voltage |
|------------------|------------------------------|
| DVCC1A           | 1.4V~1.6V                    |
| DVCC1B           |                              |
| DVCC1C           |                              |
| DVCC3A           | 3.0V~3.6V                    |
| AVCC             |                              |

### 3. Operation

This section describes the basic components, functions and operation of the TMP92CF30.

#### 3.1 CPU

The TMP92CF30 contains an advanced high-speed 32-bit CPU (TLCS-900/H1 CPU)

##### 3.1.1 CPU Outline

The TLCS-900/H1 CPU is a high-speed, high-performance CPU based on the TLCS-900/L1 CPU. The TLCS-900/H1 CPU has an expanded 32-bit internal data bus to process Instructions more quickly.

The following is an outline of the CPU:

Table 3.1.1 Outline of TMP92CF30

| Parameter                               | TMP92CF30                                                   |                                                         |
|-----------------------------------------|-------------------------------------------------------------|---------------------------------------------------------|
| Width of CPU Address Bus                | 24-bit                                                      |                                                         |
| Width of CPU Data Bus                   | 32-bit                                                      |                                                         |
| Internal Operating Frequency            | Max 80 MHz                                                  |                                                         |
| Minimum Bus Cycle                       | 1-clock access (12.5ns at 80 MHz)                           |                                                         |
| Internal RAM                            | 32-bit 2-1-1-1 clock access                                 |                                                         |
| Internal I/O                            | 8-bit,<br>2-clock access                                    | INTC,SDRAMC,<br>MEMC,TSI,PORT                           |
|                                         | 16-bit,<br>2-clock access                                   | MMU,USB,<br>NDFC,SPIC,DMAC                              |
|                                         | 32-bit,<br>2-clock access                                   | I <sup>2</sup> S                                        |
|                                         | 32-bit,<br>1-clock access                                   | MAC                                                     |
|                                         | 8-bit,<br>5 to 6-clock access                               | TMRA,TMRB,<br>SIO,RTC,<br>MLD/ALM, SBI<br>CGEAR,ADC,WDT |
| External memory<br>(SRAM, MASKROM etc.) | 8/16-bit 2-clock access<br>(waits can be inserted)          |                                                         |
| External memory<br>(SDRAM)              | 16-bit 1-clock access                                       |                                                         |
| External memory<br>(NAND FLASH)         | 8/16-bit 2-clock access<br>(waits can be inserted)          |                                                         |
| Minimum Instruction<br>Execution Cycle  | 1-clock (12.5ns at 80 MHz)                                  |                                                         |
| Conditional Jump                        | 2-clock (25.0ns at 80 MHz)                                  |                                                         |
| Instruction Queue Buffer                | 12-byte                                                     |                                                         |
| Instruction Set                         | Compatible with TLCS-900/L1<br>(LDX instruction is deleted) |                                                         |
| Micro DMA                               | 8-channel                                                   |                                                         |
| Hardware DMA                            | 6-channel                                                   |                                                         |

### 3.1.2 Reset Operation

When resetting the TMP92CF30 microcontroller, ensure that the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then hold the  $\overline{\text{RESET}}$  input Low for at least 20 system clocks (32 $\mu$ s at X1=10MHz).

At reset, since the clock doublers (PLL0) is bypassed and the clock-gear is set to 1/16, the system clock operates at 625 kHz(X1=10MHz).

When the Reset has been accepted, the CPU performs the following. CPU internal registers do not change when the Reset is released.

- Sets the Stack Pointer (XSP) to 00000000H.
- Sets bits <IFF2:0> of the Status Register (SR) to “111” (thereby setting the Interrupt Level Mask Register to level 7).
- Clears bits <RFP1:0> of the Status Register to “00” (thereby selecting Register Bank 0).

When the Reset is released, the CPU starts executing instructions according to the Program Counter settings.

- Sets the Program Counter (PC) as follows in accordance with the Reset Vector stored at address FFFF00H~FFFF02H:

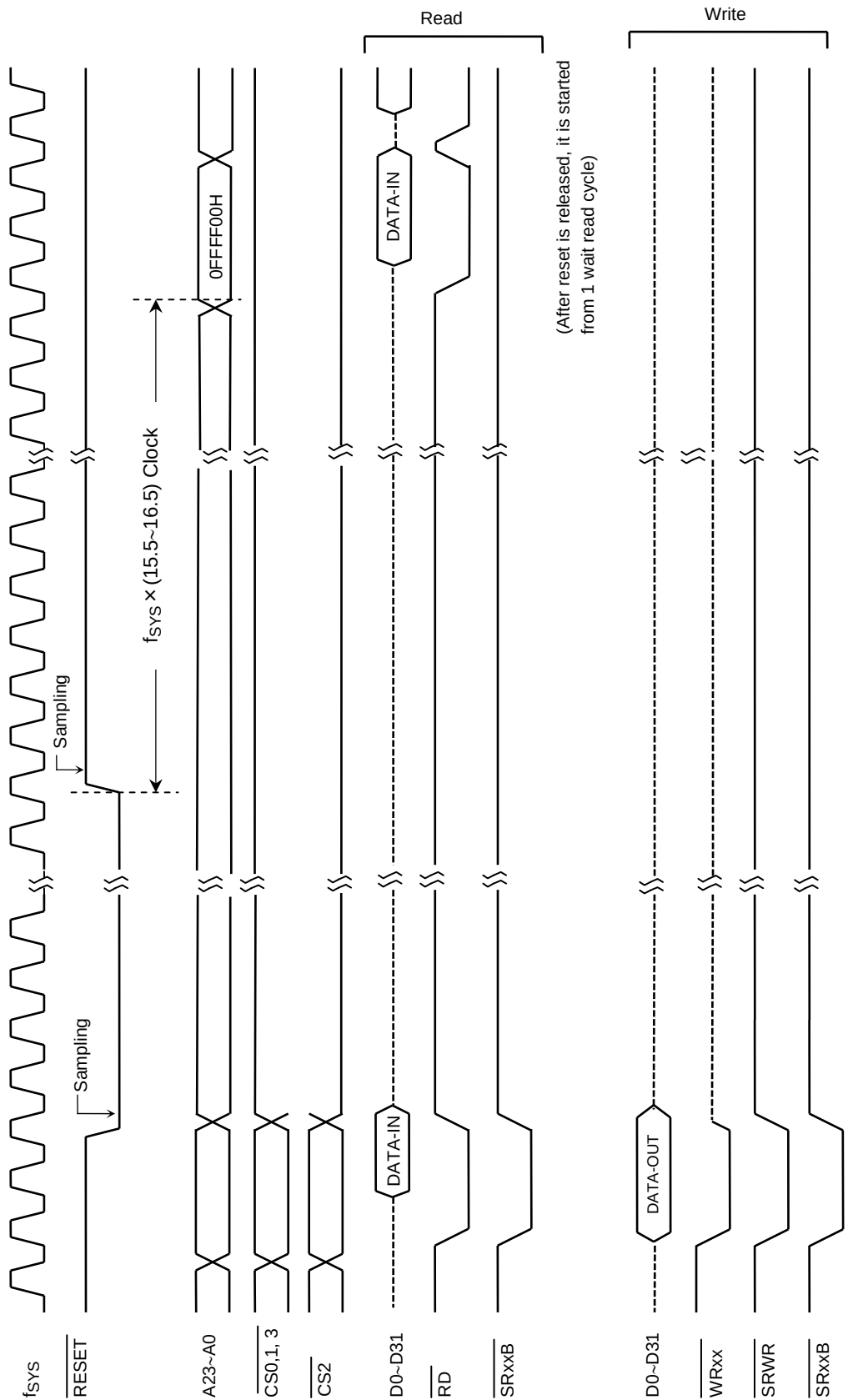
|           |   |                          |
|-----------|---|--------------------------|
| PC<7:0>   | ← | data in location FFFF00H |
| PC<15:8>  | ← | data in location FFFF01H |
| PC<23:16> | ← | data in location FFFF02H |

When the Reset is accepted, the CPU sets internal I/O, ports and other pins as follows.

- Initializes the internal I/O registers as table of “Special Function Register” in Section 5.

Note: This LSI builds in RAM internally. However, the data in internal RAM may not be held by Reset operation. After reset, initialize the data in internal RAM.

Figure 3.1.1 shows reset timing chart. Figure 3.1.2 shows the example of order of supplying power and the timing of releasing reset.



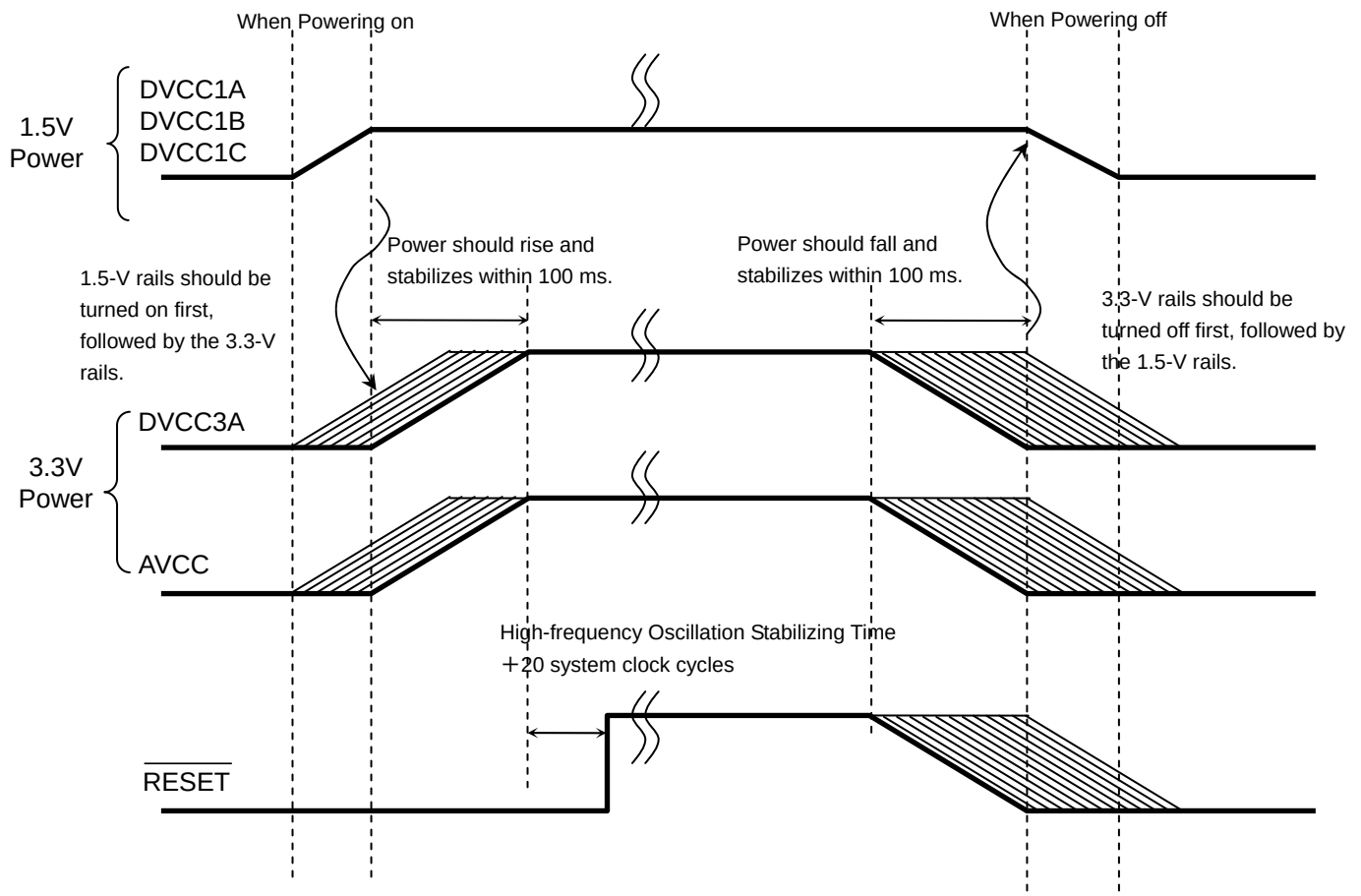
----- : High-Z

Note: This is a timing chart of the 32 bit external bus start mode

Figure 3.1.1 TMP92CF30 Reset timing chart



This LSI has the restriction for the order of supplying power. Be sure to supply external 3.3V power with 1.5V power is supplied.



Note1: Although it is possible to turn on or off the 1.5-V and 3.3-V power supply rails simultaneously, it may cause external pins to temporarily become unstable. Therefore, if there is any possibility that this would affect peripheral devices connected with the TMP92CF30, external power supplies should be turned on or off while the internal power supplies are stable, as indicated by the heavy lines in the diagram above.

Note2: In the power-on sequence, the 3.3-V power supply rails must not be turned on before the ones of 1.5-V. In the power-off sequence, the 3.3-V power supply rails must not be turned off after the ones of 1.5-V.

Figure 3.1.2 Power on Reset Timing Example

### 3.1.3 Setting of AM0 and AM1

Set AM1 and AM0 pins as shown in Table 3.1.2 according to system usage.

Table 3.1.2 Operation Mode Setup Table

| Mode Setup input pin                                                              |     |     | Operation Mode               |
|-----------------------------------------------------------------------------------|-----|-----|------------------------------|
| RESET                                                                             | AM1 | AM0 |                              |
|  | 0   | 1   | 16-bit external bus starting |
|                                                                                   | 1   | 0   | 32-bit external bus starting |
|                                                                                   | 1   | 1   | Test mode (Prohibit to set)  |
|                                                                                   | 0   | 0   | Test mode (Prohibit to set)  |

## 3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP92CF30.

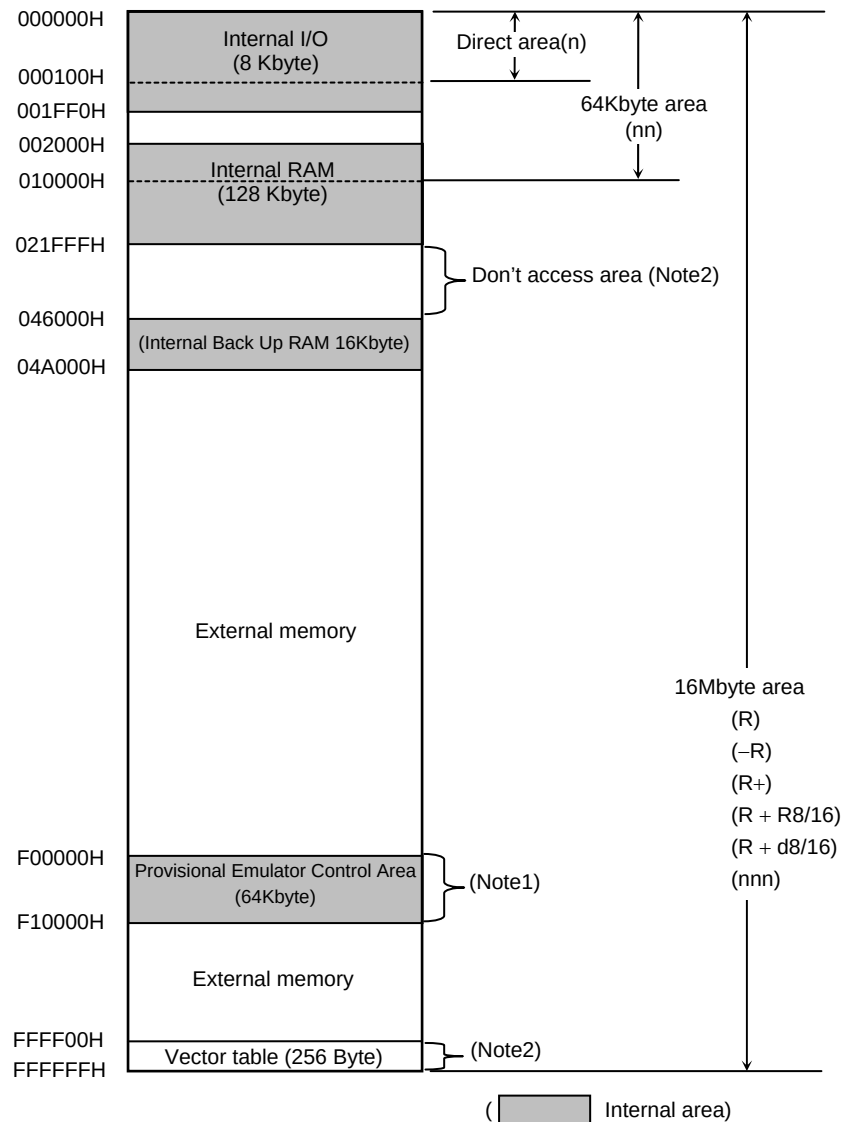


Figure 3.2.1 Memory Map

Note1: If using an emulator, an optional 64 Kbytes of the 16M bytes area is used for emulator control. Therefore, if using an emulator, this area cannot be used.

Note2: Do not use the 144K byte area (022000H to 045FFFH) and the last 16-byte area (FFFFF0H to FFFFFFFH). This area is reserved as internal area.

### 3.3 Differences between the TMP92CZ26A/CF26A and the TMP92CF30

The TMP92CF30 is a lower pin-count version of the TMP92CF26A with fewer functions (there are some added functions).

Sections 3.3.1 through 3.3.13 describe the functions that are deleted or newly added to the TMP92CF30. There are no major differences in AC/DC characteristics. For details, refer to the chapter “Electrical Characteristics”.

#### 3.3.1 DSU Circuit Deleted

The TMP92CF30 does not support the DSU function, which is available in the TMP92CZ26A/CF26A.

The development environment is offered with the TMP92CF26AXBG. (The DSU function is used and a pin conversion is required.) Therefore, functions that are modified or newly added to the TMP92CF30 cannot be debugged with development tools. (Please use the actual device or a ROM emulator to debug the TMP92CF30.)

#### 3.3.2 Internal I/O Functions Deleted and Modified

##### **[Deleted function]**

The TMP92CF30 has only one I<sup>2</sup>S channel (Channel 0), whereas the TMP92CZ26A/CF26A has Channels 0 and 1. When using the TMP92CF30, therefore, do not access the addresses where special-function registers for this deleted function have been mapped. For details, see the Table of Special Function Registers (SFRs).

##### **[Modified function 1]**

The SIO channel (SIO1) is newly added to the TMP92CF30 with its control registers. For details, see Table 3.3.1.

##### **[Modified function 2]**

There are some modifications to the port control method (multiplexed pin settings) and associated registers. If an ICE using the TMP92CF26A is used for development and debugging modified and added registers cannot be debugged. For details, see Table 3.3.1.

### 3.3.3 Port Pins Deleted

In the TMP92CF30, the following port pins are deleted as opposed to the TMP92CZ26A/CF26A.

And TMP92CF30 support the external 32bit bus function except for access to SDRAM.

Added: External 32bit bus function added. (However, if an ICE using the TMP92CF26A is used to development and debugging, it is possible only to operate by 16 bit bus mode.)

Deleted:

- $\overline{\text{DBGE}}$ : Debug enable pin (The DSU function is not available.)
- Port 8: P84 ( $\overline{\text{CSZB}}$ ), P85 ( $\overline{\text{CSZC}}$ )
- Port F: PF3 (I2S1CKO), PF4 (I2S1DO), PF5 (I2SWS)
- Port P: PP7 (TB1OUT0), PP2 (TA5OUT), PP1 (TA3OUT)
- Port U: PU0 to PU7 (LD16 to LD23)
- Port V: PV0, PV1, PV2, PV3, PV4
- Port W: PW0 to PW7
- Port X: PX7
- Port Z: PZ0 to PZ7

### 3.3.4 Maximum Memory Size Accessible with the MMU Function Reduced

With the deletion of the P84 ( $\overline{\text{CSZB}}$ ) and P85 ( $\overline{\text{CSZC}}$ ) pins, the maximum memory size that can be expanded with the MMU function is reduced, resulting in a reduced number of usable banks. In the TMP92CZ26A/CF26A the total expandable memory size is 3.1 Gbytes, which is reduced to 2.1 Gbytes in the TMP92CF30. Accordingly, the number of banks in the Z area is reduced from 512 banks to 256 banks.

If an ICE using the TMP92CF26A is used for development and debugging, be careful about registers and banks which are available in the TMP92CF26A but do not exist in the TMP92CF30. For details, see the chapter on the MMU function.

### 3.3.5 One of the I<sup>2</sup>S Channels Deleted and I<sup>2</sup>S Function Modified

#### [Deleted function]

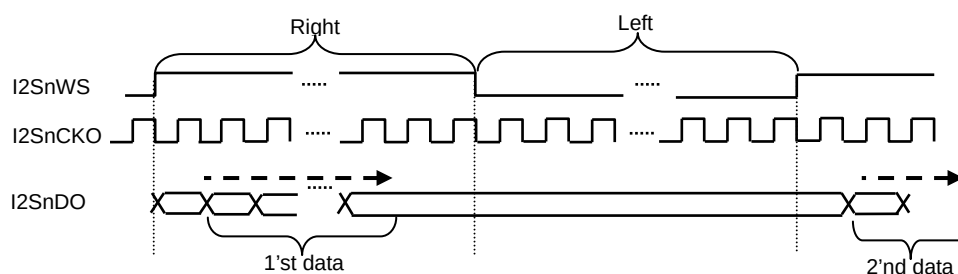
The TMP92CF30 has only one I<sup>2</sup>S channel (Channel 0), whereas the TMP92CZ26A/CF26A has Channels 0 and 1.

#### [Modified function]

The monophonic data output format of the I<sup>2</sup>S function is modified as shown below.

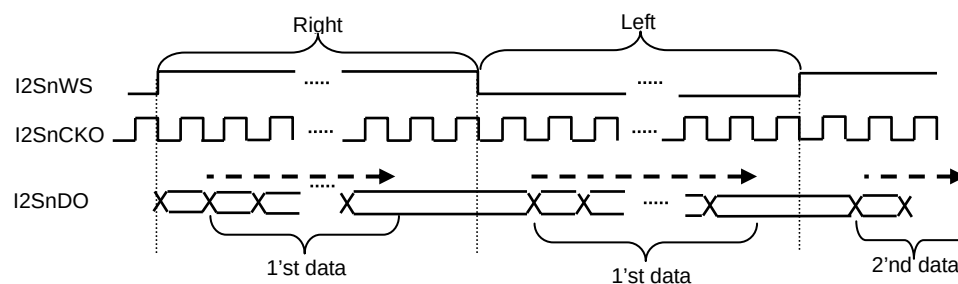
#### TMP92CZ26A/CF26A monophonic data output (I<sup>2</sup>S format)

Data is output from either right or left channel.



#### TMP92CF30 monophonic data output (I<sup>2</sup>S format)

Identical data is output from both right and left channels.



If an ICE using the TMP92CF26A is used for development, data is output from only one channel in monophonic mode. For details, see the chapter on the I<sup>2</sup>S Interface.

### 3.3.6 $\overline{\text{NMI}}$ Pin Added

In the TMP92CF30, the  $\overline{\text{TEST}}$  pin is newly added. This pin must always be fixed to high level.

TMP92CF30 is added the external 32bit bus function. The newly added the external 32bit bus function cannot be supported development tools using TMP92CF26A.

Please use  $\overline{\text{NMI}}$  pin for BREAK function etc, if ROM emulator is used for development.

### 3.3.7 Port L Function Added

Port L is an output-only port in the TMP92CZ26A/CF26A, whereas the TMP92CF30 allows Port L to be used as an input or output. In the TMP92CF30, Port L is set as an input immediately after a system reset. If an ICE using the TMP92CF26A is used for development and debugging, this new function cannot be used.

### 3.3.8 X1D4 Pin Added

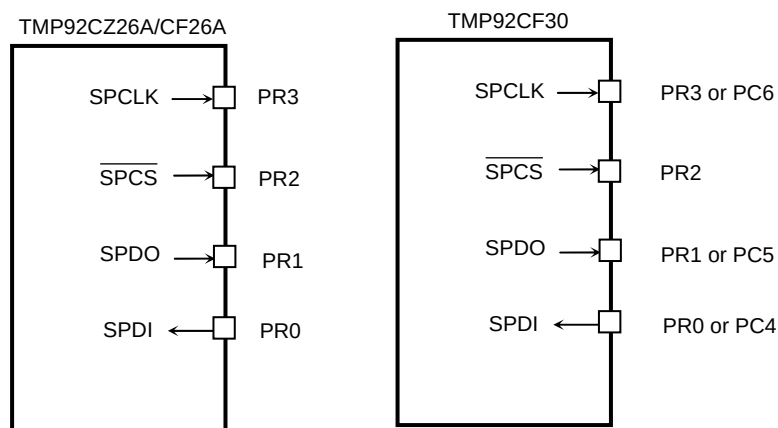
In the TMP92CF30, a new Port PX5 function is added for outputting a clock that is 1/1, 1/2, 1/4 or 1/8 of the oscillation frequency of the X1 and X2 pins. If an ICE using the TMP92CF26A is used for development and debugging, this function cannot be used.

### 3.3.9 SPI Controller Function Added

In the TMP92CZ26A/CF26A, the SPI control signals are multiplexed with Port PR. In the TMP92CF30, the SPI control signals are multiplexed with Port PR and Port PC (excluding the  $\overline{\text{SPCS}}$  signal). If an ICE using the TMP92CF26A is used for development and debugging, registers associated with the following new functions cannot be debugged.

- Output the SPCLK signal from the PC6 pin
- Output the SPDO signal from the PC5 pin
- Input the SPDI signal from the PC4 pin

For details, refer to the chapter on the SPI controller.



### 3.3.10 LCD Controller Functions Added and Deleted

#### [Deleted function]

The TMP92CF30 does not support the LCD controller, which is available in the TMP92CZ26A/CF26A.

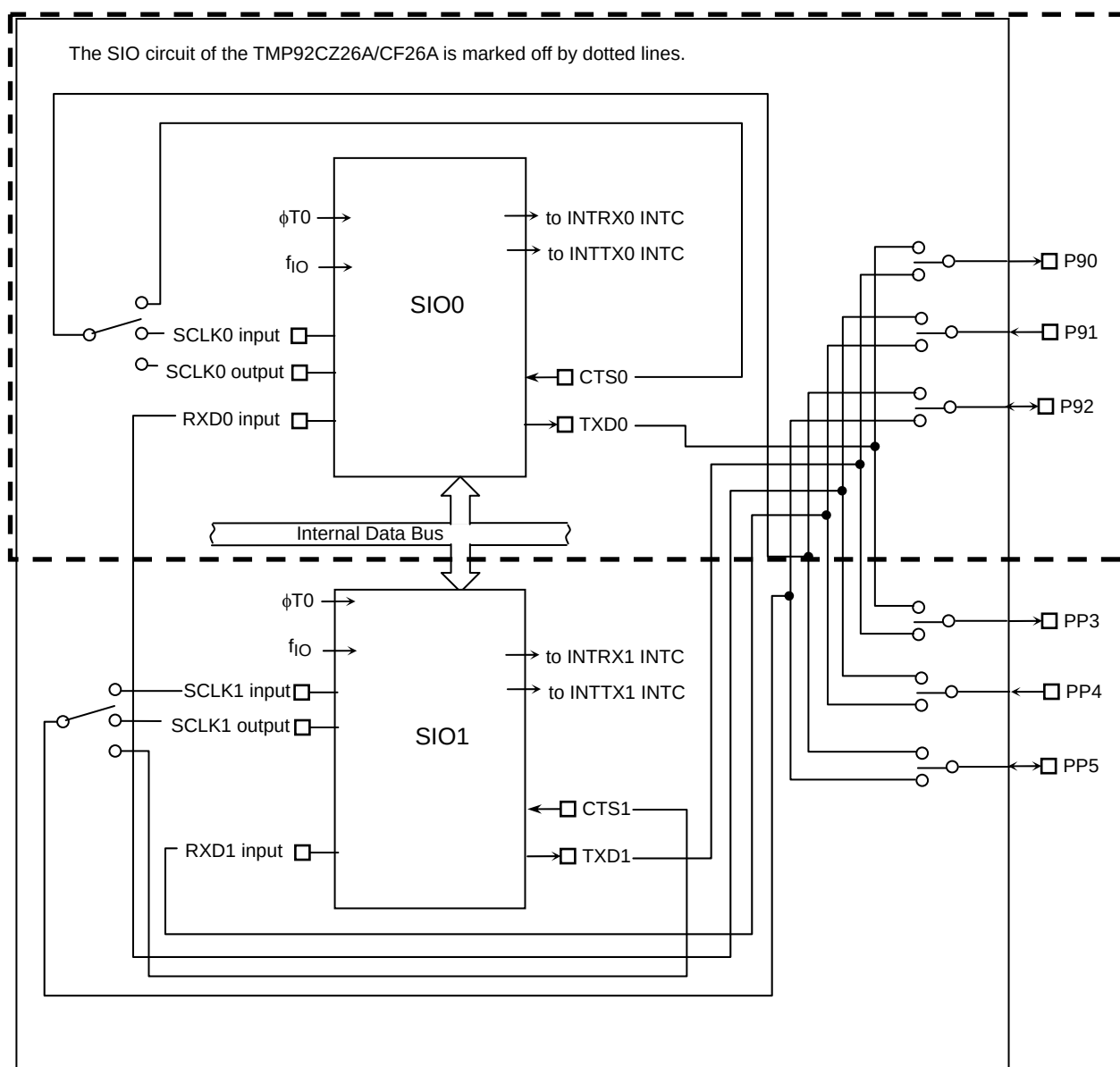
### 3.3.11 SIO Channel Added and SIO Function Modified

#### [Added function]

In the TMP92CZ26A/CF26A only one SIO channel is available, whereas the TMP92CF30 has two SIO channels. However, if an ICE using the TMP92CF26A is used for development and debugging, the newly added Channel 1 cannot be debugged.

#### [Modified function]

Each of the two SIO channels can be connected to the P90, P91 and P92 pins or the PP3, PP4 and PP5 pins. However, if an ICE using the TMP92CF26A is used for development and debugging, this modified port switching function cannot be debugged.





### 3.3.12 Interrupt Sources Deleted and Modified

#### [Deleted function]

As the number of I<sup>2</sup>S channels is reduced from two channels to one channel, the corresponding interrupt vector is deleted.

#### [Modified function]

As the number of SIO channels is increased from one channel to two channels, the interrupt vectors for SIO1 serial receive end and SIO1 serial transmission end are added in the TMP92CF30. However, if an ICE using the TMP92CF26A is used to development and debugging, this modified interrupt function cannot be debugged.

TMP92CF30 Interrupt Vectors and Micro DMA/HDMA Start Vectors

| Default Priority | Type         | Interrupt Source/Micro DMA Request Source | Vector Value | Vector Reference Address | Micro DMA /HDMA Start Vector |
|------------------|--------------|-------------------------------------------|--------------|--------------------------|------------------------------|
| 1                | Non maskable | Reset or [SWI0] instruction               | 0000H        | FFFF00H                  |                              |
| 2                |              | [SWI1] instruction                        | 0004H        | FFFF04H                  |                              |
| (Omitted)        |              | (Omitted)                                 |              |                          |                              |
| 40               |              | INTI2S0: I <sup>2</sup> S (Channel 0)     | 009CH        | FFFF9CH                  | 27H                          |
| 41               |              | <b>(Reserved)</b>                         | —            | —                        | —                            |
| 42               |              | INTADM: AD monitor function               | 00A4H        | FFFFA4H                  | 29H                          |
| 43               |              | INTSBI: SBI                               | 00A8H        | FFFFA8H                  | 2AH                          |
| 44               |              | INTSPIRX: SPIC receive                    | 00ACH        | FFFFACH                  | 2BH                          |
| 45               |              | INTSPITX: SPIC transmission               | 00B0H        | FFFFB0H                  | 2CH                          |
| 46               |              | INTRSC: NAND Flash controller             | 00B4H        | FFFFB4H                  | 2DH                          |
| 47               |              | INTRDY: NAND Flash controller             | 00B8H        | FFFFB8H                  | 2EH                          |
| 48               |              | INTUSB: USB                               | 00BCH        | FFFFBCH                  | 2FH                          |
| 49               |              | <b>INTRX1: Serial receive end</b>         | <b>00C0H</b> | <b>FFFC0H</b>            | <b>30H</b>                   |
| 50               |              | <b>INTTX1: Serial transmission end</b>    | <b>00C4H</b> | <b>FFFC4H</b>            | <b>31H</b>                   |

### 3.3.13 Pull-Up Control Port for USB Boot Modified

The TMP92CF30 does not support the Boot ROM function, which is available in the TMP92CZ26A/CF26A.

Table 3.3.1 summarizes the differences between the TMP92CZ26A and the TMP92CF30. For details, refer to the chapter on each functional block.

Table 3.3.1 Differences between the TMP92CZ26A and the TMP92CF30

| Item                      | TMP92CZ26A                                                                                                             | TMP92CF30                                                                         | Note                                                                                                                  |     |
|---------------------------|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|-----|
| RAM                       | 288 KB                                                                                                                 | 144 KB                                                                            |                                                                                                                       |     |
| ROM                       | 8 KB (BOOT)                                                                                                            | None                                                                              |                                                                                                                       |     |
| Package                   | FBGA228-P-1515-0.80A                                                                                                   | LQFP176-P-2020-0.40F                                                              |                                                                                                                       |     |
| Pin count                 | 228                                                                                                                    | 176                                                                               |                                                                                                                       |     |
| External data bus         | to 16 bit                                                                                                              | to 32 bit                                                                         | This function cannot be debugged with development tools.                                                              |     |
| DSU                       | Supports                                                                                                               | Not supports                                                                      | Development tools using the TMP92CZ26 are offered.<br>10 pins are deleted: $\overline{\text{DBGE}}$ , PZ0 to PZ7, PU7 | -10 |
| I <sup>2</sup> S          | 2 channels                                                                                                             | 1 channel                                                                         | Channel 1 are deleted<br>3 pins are deleted: PF3 (I2S1CKO, X1D4), PF4 (I2S1DO), PF5 (I2S1WS)                          | -3  |
| 8-bit timer               | 8 channels                                                                                                             | 8 channels                                                                        | 2 pins deleted: PP1(TA3OUT), PP2 (T5OUT)                                                                              | -2  |
| SIO                       | 1 channel                                                                                                              | 2 channels                                                                        | The newly added channel cannot be debugged with development tools.                                                    |     |
| 16-bit timer              | 2 channels                                                                                                             | 2 channels                                                                        | 1 pin is deleted: PP7(TB1OUT0)                                                                                        | -1  |
| LCDC                      | TFT 16M colors                                                                                                         | None                                                                              | These pins useable as data bus pins.                                                                                  | -7  |
| General-purpose port pins | P84/ $\overline{\text{CSZB}}$<br>P85/ $\overline{\text{CSZC}}$<br>PV0<br>PV1<br>PV2<br>PV3<br>PV4<br>PX7<br>PW0 to PW7 | Deleted<br>Deleted<br>Deleted<br>Deleted<br>Deleted<br>Deleted<br>Deleted         | 15 port pins are deleted                                                                                              | -16 |
| Power supply pins         | DVCC3A 12<br>DVCC3B 1<br>DVCC1A 5<br>DVCC1B 1<br>DVCC1C 1<br>DVCC1S 1<br>DVSSCOM 12                                    | DVCC3A 8<br>DVCC3B 0<br>DVCC1A 4<br>DVCC1B 1<br>DVCC1C 1<br>DVCC1S 1<br>DVSSCOM 8 | 10 power supply pins deleted                                                                                          | -10 |
| Dummy                     | 4 pins                                                                                                                 | None                                                                              | 4 dummy pins are deleted                                                                                              | -4  |
| $\overline{\text{NMI}}$   | Not supports                                                                                                           | Adds                                                                              | The TEST pin is added                                                                                                 | +1  |
| TOTAL                     |                                                                                                                        |                                                                                   | 228-pin BGA → 176-pin QFP<br>(A total of 52 pins are deleted)                                                         | -52 |

#### Other Specification Changes

|                                                          |                                                                                                                                                                                                                  |
|----------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| The number of SIO channels is increased to two channels. | In the TMPCZ26A/CF26A only one SIO channel is available, whereas the TMP92CF30 has two SIO channels. However, the added SIO function cannot be debugged with development tools.                                  |
| The X1D4 pin is added.                                   | The X1D4 pin can be used to output x1, x1/2, x1/4 or x1/8 of the external clock according to the CPU state (in NORMAL, IDLE1 and IDLE2 modes). However, this function cannot be debugged with development tools. |
| SPI output can be made from either of two pins.          | As in the case of the TMP92CZ26A/CF26A, the TMP92CF30 has only one SPI channel, but the output pin can be selected from two pins. However, this new function cannot be debugged with development tools.          |

### 3.4 Clock Function and Standby Function

The TMP92CF30 contains (1) clock gear, (2) clock doubler (PLL), (3) standby controller and (4) noise reduction circuits. They are used for low-power, low-noise systems.

This chapter is organized as follows:

3.4.1 Block diagram of system clock

3.4.2 SFR

3.4.3 System clock controller

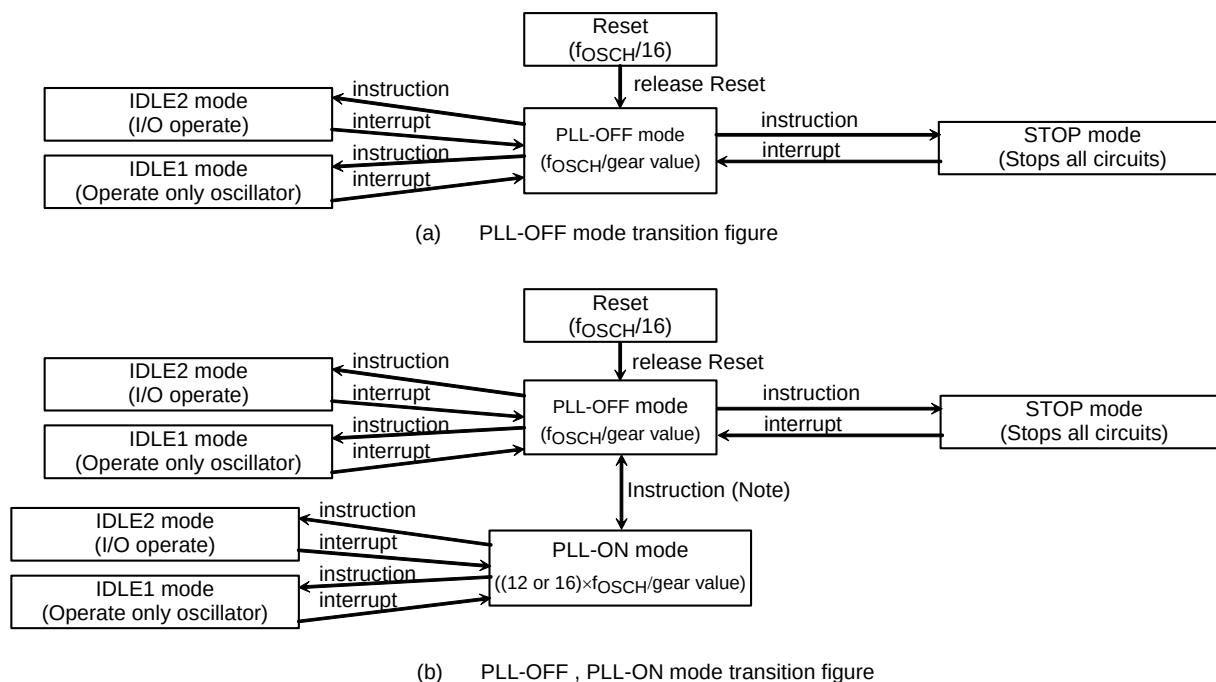
3.4.4 Clock doubler (PLL)

3.4.5 Noise reduction circuits

3.4.6 Standby controller

The clock operating modes are as follows: (a) PLL-OFF Mode (X1, X2 pins only),  
(b) PLL-ON Mode (X1, X2, and PLL).

Figure 3.4.1 shows a transition figure.



Note 1: When shifting from PLL-ON mode to PLL-OFF mode, execute the following setting in the same order.

- (1) Change CPU clock (Set "0" to PLLCR0<FCSEL>)
- (2) Stop PLL circuit (Set "0" to PLLCR1<PLLON>)

Note 2: It is not possible to shift from PLL-ON mode to STOP mode directly.

PLL-OFF mode should be set once before shifting to STOP mode.

Figure 3.4.1 System clock block diagram

The clock frequency input from the X1 and X2 pins is called  $f_{OSCH}$  and the clock frequency input from the XT1 and XT2 pins is called  $f_s$ . The clock frequency selected by SYSCR1<GEAR2:0> is called the system clock  $f_{SYS}$ . And one cycle of  $f_{SYS}$  is defined to as one state.

## 3.4.1 Block diagram of system clock

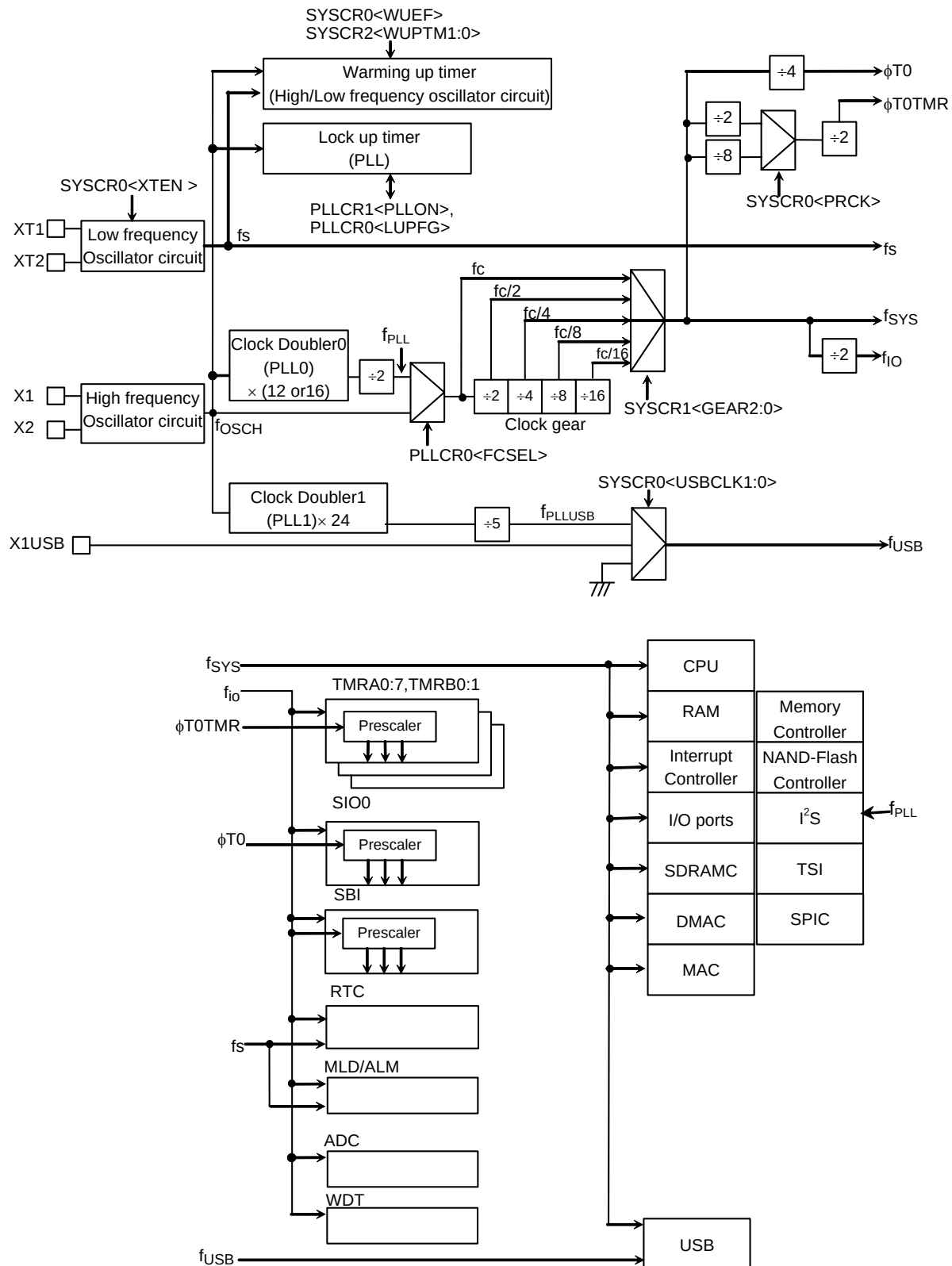


Figure 3.4.2 Block Diagram of System clock

TMP92CF30 has two PLL circuits: one is for CPU (PLL0) and the other for USB (PLL1). Each PLL can be controlled independently. Frequency of external oscillator is 6 to 10MHz.

Don't connect oscillator more than 10MHz. When clock is input by using external oscillator, range of input frequency is 6 to 10MHz.

Don't input the clock over 10MHz.

Table 3.4.1 Setting example for  $f_{OSCH}$

|                                                        | High frequency:<br>$f_{OSCH}$ | System<br>clock:<br>$f_{SYS}$ | System<br>clock:<br>$f_{SYS}$ | USB<br>clock:<br>$f_{USB}$ |
|--------------------------------------------------------|-------------------------------|-------------------------------|-------------------------------|----------------------------|
| (a) USB in use, with PLL<br>(PLL0 ON/PLL1 ON)          | 10.0 MHz                      | Max 80 MHz                    | Max 60 MHz                    | 48 MHz                     |
| (b) USB not in use, with PLL<br>(PLL0 ON/PLL1 OFF)     | Max 10.0 MHz                  | Max 80 MHz                    | Max 60 MHz                    | –                          |
| (c) USB not in use, without PLL<br>(PLL0 OFF/PLL1 OFF) | Max 10.0 MHz                  | Max 10 MHz                    | Max 10 MHz                    | –                          |

Note: When using USB, the high-frequency oscillator should be 10.0 MHz.

## 3.4.2 SFR

|                   |             |                     |                                                                              |                                                                                                                                                               |         |                                                                                |                                                                                                                                                                |       |                                                                                  |
|-------------------|-------------|---------------------|------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|--------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|----------------------------------------------------------------------------------|
| SYSCR0<br>(10E0H) |             | 7                   | 6                                                                            | 5                                                                                                                                                             | 4       | 3                                                                              | 2                                                                                                                                                              | 1     | 0                                                                                |
|                   | bit Symbol  |                     | XTEN                                                                         | USBCLK1                                                                                                                                                       | USBCLK0 |                                                                                | WUEF                                                                                                                                                           |       | PRCK                                                                             |
|                   | Read/write  |                     | R/W                                                                          |                                                                                                                                                               |         |                                                                                | R/W                                                                                                                                                            |       | R/W                                                                              |
|                   | Reset State |                     | 1                                                                            | 0                                                                                                                                                             | 0       |                                                                                | 0                                                                                                                                                              |       | 0                                                                                |
|                   | Function    |                     | Low<br>-frequency<br>oscillator<br>circuit (fs)<br>0: Stop<br>1: Oscillation | Select the clock of<br>USB(f <sub>USB</sub> )<br>00: Disable<br>01: Reserved<br>10: X1USB<br>11: f <sub>PLLUSB</sub>                                          |         |                                                                                | Warm-up<br>Timer<br>0: Write<br>Don't care<br>Note3<br>1: Write<br>start timer<br>0: Read<br>end<br>warm-up<br>1: Read<br>do not end<br>warm-up                |       | Select<br>Prescaler<br>clock<br>0: f <sub>SYS</sub> /2<br>1: f <sub>SYS</sub> /8 |
| SYSCR1<br>(10E1H) |             | 7                   | 6                                                                            | 5                                                                                                                                                             | 4       | 3                                                                              | 2                                                                                                                                                              | 1     | 0                                                                                |
|                   | bit Symbol  |                     |                                                                              |                                                                                                                                                               |         |                                                                                | GEAR2                                                                                                                                                          | GEAR1 | GEAR0                                                                            |
|                   | Read/write  |                     |                                                                              |                                                                                                                                                               |         |                                                                                | R/W                                                                                                                                                            |       |                                                                                  |
|                   | Reset State |                     |                                                                              |                                                                                                                                                               |         |                                                                                | 1                                                                                                                                                              | 0     | 0                                                                                |
|                   | Function    |                     |                                                                              |                                                                                                                                                               |         |                                                                                | Select gear value of high frequency<br>(fc)<br>000: fc<br>001: fc/2<br>010: fc/4<br>011: fc/8<br>100: fc/16<br>101: Reserved<br>110: Reserved<br>111: Reserved |       |                                                                                  |
| SYSCR2<br>(10E2H) |             | 7                   | 6                                                                            | 5                                                                                                                                                             | 4       | 3                                                                              | 2                                                                                                                                                              | 1     | 0                                                                                |
|                   | bit Symbol  | –                   | CKOSEL                                                                       | WUPTM1                                                                                                                                                        | WUPTM0  | HALTM1                                                                         | HALTM0                                                                                                                                                         |       |                                                                                  |
|                   | Read/write  |                     | R/W                                                                          |                                                                                                                                                               |         |                                                                                |                                                                                                                                                                |       |                                                                                  |
|                   | Reset State | 0                   | 0                                                                            | 1                                                                                                                                                             | 0       | 1                                                                              | 1                                                                                                                                                              |       |                                                                                  |
|                   | Function    | Always<br>write “0” | Select<br>CLKOUT<br>0: f <sub>SYS</sub><br>1: f <sub>S</sub>                 | Warm-Up Timer<br>00: Reserved<br>01: 2 <sup>9</sup> /inputted frequency<br>10: 2 <sup>14</sup> /inputted frequency<br>11: 2 <sup>16</sup> /inputted frequency |         | HALT mode<br>00: Reserved<br>01: STOP mode<br>10: IDLE1 mode<br>11: IDLE2 mode |                                                                                                                                                                |       |                                                                                  |

Note1: The unassigned registers, SYSCR0<bit7><bit3><bit1>, SYSCR1<bit7:3> and SYSCR2<bit1:0> are read as undefined value.

Note2: Low frequency oscillator circuit is enabled on reset.

Note3: Do not write SYSCR0 resiter during warming up. Because the warm-up end flag doesn't become enable if write “0” to SYSCR0<WUEF> bit during warming up.  
(A read-modify–write operation cannot be performed for SYSCR0 register during warming up.)

Figure 3.4.3 SFR for system clock

|                   |             | 7                                                                                                                                                                                                                                      | 6 | 5 | 4 | 3                    | 2                    | 1                                                      | 0                                                      |
|-------------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|---|---|----------------------|----------------------|--------------------------------------------------------|--------------------------------------------------------|
| EMCCR0<br>(10E3H) | Bit symbol  | PROTECT                                                                                                                                                                                                                                |   |   |   | –                    | EXTIN                | DRVOSCH                                                | DRVOSCL                                                |
|                   | Read/Write  | R                                                                                                                                                                                                                                      |   |   |   | R/W                  |                      |                                                        |                                                        |
|                   | Reset State | 0                                                                                                                                                                                                                                      |   |   |   | 0                    | 0                    | 1                                                      | 1                                                      |
|                   | Function    | Protect<br>flag<br>0: OFF<br>1: ON                                                                                                                                                                                                     |   |   |   | Always<br>write “0”. | 1: External<br>clock | fc oscillator<br>drive ability<br>1: NORMAL<br>0: WEAK | fs oscillator<br>drive ability<br>1: NORMAL<br>0: WEAK |
| EMCCR1<br>(10E4H) | Bit symbol  | <div>Switch the protect ON/OFF by writing the following to 1<sup>st</sup>-KEY,2<sup>nd</sup>-KEY<br/>1<sup>st</sup>-KEY: write in sequence EMCCR1=5AH,EMCCR2=A5H<br/>2<sup>nd</sup>-KEY: write in sequence EMCCR1=A5H,EMCCR2=5AH</div> |   |   |   |                      |                      |                                                        |                                                        |
|                   | Read/Write  |                                                                                                                                                                                                                                        |   |   |   |                      |                      |                                                        |                                                        |
|                   | Reset State |                                                                                                                                                                                                                                        |   |   |   |                      |                      |                                                        |                                                        |
|                   | Function    |                                                                                                                                                                                                                                        |   |   |   |                      |                      |                                                        |                                                        |
| EMCCR2<br>(10E5H) | Bit symbol  |                                                                                                                                                                                                                                        |   |   |   |                      |                      |                                                        |                                                        |
|                   | Read/Write  |                                                                                                                                                                                                                                        |   |   |   |                      |                      |                                                        |                                                        |
|                   | Reset State |                                                                                                                                                                                                                                        |   |   |   |                      |                      |                                                        |                                                        |
|                   | Function    |                                                                                                                                                                                                                                        |   |   |   |                      |                      |                                                        |                                                        |

Note1: When restarting the oscillator in the stop oscillation state (e.g. Restarting the oscillator in STOP mode), set EMCCR0<DRVOSCH>, <DRVOSCL> = “1”.

Note2: Do not write EMCCR0<EXTIN> = “1” when using external resonator.

Figure 3.4.4 SFR for system clock



|                   | 7           | 6                                                                 | 5                                                       | 4 | 3 | 2 | 1 | 0 |
|-------------------|-------------|-------------------------------------------------------------------|---------------------------------------------------------|---|---|---|---|---|
| PLLCR0<br>(10E8H) | bit symbol  | FCSEL                                                             | LUPFG                                                   |   |   |   |   |   |
|                   | Read/Write  | R/W                                                               | R                                                       |   |   |   |   |   |
|                   | Reset State | 0                                                                 | 0                                                       |   |   |   |   |   |
|                   | Function    | Select<br>fc-clock<br>0: f <sub>OSCH</sub><br>1: f <sub>PLL</sub> | Lock-up<br>timer<br>Status flag<br>0: not end<br>1: end |   |   |   |   |   |

Note: Ensure that the logic of PLLCR0<LUPFG> is different from 900/L1's DFM.

|                   | 7           | 6                                  | 5                                  | 4                                                                                                  | 3 | 2 | 1 | 0                                                  |
|-------------------|-------------|------------------------------------|------------------------------------|----------------------------------------------------------------------------------------------------|---|---|---|----------------------------------------------------|
| PLLCR1<br>(10E9H) | bit symbol  | PLL0                               | PLL1                               | LUPSEL                                                                                             |   |   |   | PLLTIMES                                           |
|                   | Read/Write  | R/W                                |                                    |                                                                                                    |   |   |   | R/W                                                |
|                   | Reset State | 0                                  | 0                                  | 0                                                                                                  |   |   |   | 0                                                  |
|                   | Function    | PLL0 for<br>CPU<br>0: Off<br>1: On | PLL1 for<br>USB<br>0: Off<br>1: On | Select<br>stage of<br>Lock up<br>counter<br>0: 12 stage<br>(for PLL0)<br>1: 13 stage<br>(for PLL1) |   |   |   | Select the<br>number of<br>PLL<br>0: ×12<br>1: ×16 |

Figure 3.4.5 SFR for PLL

|                 |                       |                                                     |      |      |      |      |      |      |      |
|-----------------|-----------------------|-----------------------------------------------------|------|------|------|------|------|------|------|
| PxDR<br>(xxxxH) |                       | 7                                                   | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|                 | bit symbol            | Px7D                                                | Px6D | Px5D | Px4D | Px3D | Px2D | Px1D | Px0D |
|                 | Read/Write            | R/W                                                 |      |      |      |      |      |      |      |
|                 | System<br>Reset State | 1                                                   | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
|                 | Hot Reset<br>State    | –                                                   | –    | –    | –    | –    | –    | –    | –    |
|                 | Function              | Output/Input buffer drive-register for standby-mode |      |      |      |      |      |      |      |

(Purpose and using)

- This register is used to set each pin-status at stand-by mode.
- All ports have registers of the format shown above. (“x” indicates the port name.)
- For each register, refer to 3.7 Function of Ports.
- Before “HALT” instruction is executed, set each register pin-status. They will be effective after the CPU has executes the “HALT” instruction.
- This is the case regardless of stand-by modes (IDLE2, IDLE1 or STOP).

The Output/Input buffer control table is shown below.

| OE | PxnD | Output buffer | Input buffer |
|----|------|---------------|--------------|
| 0  | 0    | OFF           | OFF          |
| 0  | 1    | OFF           | ON           |
| 1  | 0    | OFF           | OFF          |
| 1  | 1    | ON            | OFF          |

Note1: OE denotes an output enable signal before stand-by mode. Basically, PxCR is used as OE.

Note2: “n” in PxnD denotes the bit number of PORTx.

Figure 3.4.6 SFR for Drive register

### 3.4.3 System clock controller

The system clock controller generates the system clock signal ( $f_{SYS}$ ) for the CPU core and internal I/O.

SYSCR0<XEN> and SYSCR0<XTEN> control enabling and disabling of each oscillator. SYSCR1<GEAR2:0> sets the high frequency clock gear to either 1, 2, 4, 8 or 16 ( $f_c$ ,  $f_c/2$ ,  $f_c/4$ ,  $f_c/8$ ,  $f_c/16$ ). These functions can reduce the power consumption of the equipment in which the device is installed.

The combination of settings <XEN> = "1", <SYSCK> = "0" and <GEAR2:0> = "100" will be PLL-OFF mode and cause the system clock ( $f_{SYS}$ ) to be set to  $f_c/16$  after reset.

For example,  $f_{SYS}$  is set to 625 kHz when the 10MHz oscillator is connected to the X1 and X2 pins.

#### (1) Clock gear controller

$f_{SYS}$  is set according to the contents of the Clock Gear Select Register SYSCR1<GEAR2:0> to either  $f_c$ ,  $f_c/2$ ,  $f_c/4$ ,  $f_c/8$  or  $f_c/16$ . Using the clock gear to select a lower value of  $f_{SYS}$  reduces power consumption.

(Example)

Changing clock gear

SYSCR1 EQU 10E1H

```
LD    (SYSCR1),XXXXX001B    ;  Changes system clock  $f_{SYS}$  to  $f_c/2$ 
LD    (DUMMY),00H           ;  Dummy instruction
```

X: don't care

(High-speed clock gear changing)

To change the clock gear, write the register value to the SYSCR1<GEAR2:0> register. It is necessary for the warming up time to elapse before the change occurs after writing the register value.

There is the possibility that the instruction following the clock gear changing instruction is executed by the clock gear before changing. To execute the instruction following the clock gear switching instruction by the clock gear after changing, input the dummy instruction as follows (instruction to execute the write cycle).

(Example)

SYSCR1 EQU 10E1H

```
LD    (SYSCR1),XXXXX010B    ;  Changes  $f_{SYS}$  to  $f_c/4$ 
LD    (DUMMY),00H           ;  Dummy instruction
```

Instruction to be executed after clock gear changed

### 3.4.4 Clock doubler (PLL)

PLL0 outputs the  $f_{PLL}$  clock signal, which is 12 or 16 times as fast as  $f_{OSCH}$ . A low-speed frequency oscillator can be used as external oscillator, even though the internal clock is high-frequency.

Since Reset initializes PLL0 to stop status, so setting to PLLCR0 and PLLCR1-register is needed before use.

As with an oscillator, this circuit requires time to stabilize. This is called the lock-up time and it is measured by a 12-stage binary counter. Lock-up time is about 0.41ms at  $f_{OSCH} = 10\text{MHz}$ .

PLL (PLL1) which is special for USB is built in. Lock-up time is about 0.82ms at  $f_{OSCH} = 10\text{MHz}$  measured by 13-stage binary counter.

Note1: Input frequency range for PLL

The input frequency range (High frequency oscillation) for PLL is as follows:

$f_{OSCH} = X \text{ to } X \text{ MHz}$  ( $V_{CC} = 1.4 \text{ to } 1.6\text{V}$ )

Note2: PLLCR0<LUPFG>

The logic of PLLCR0<LUPFG> is different from 900/L1's DFM.

Exercise care in determining the end of lock-up time.

Note3: PLLCR1<PLL0>, PLLCR1<PLL1>

It is not possible to turn ON both PLL0 and PLL1 simultaneously.

If turning ON simultaneously, one PLL should be turn ON after finishing the lock up of the other PLL.

Table 3.4.2 shows the frequency of  $f_{SYS}$  when using PLL and clock gear at  $f_{OSCH} = 10\text{MHz}$ .

Table 3.4.2 The frequency of  $f_{SYS}$  at  $f_{OSCH} = 10\text{MHz}$

| $f_{OSCH}$ | $f_{PLL}$          | Frequency of $f_{SYS}$ |       |        |         |         |
|------------|--------------------|------------------------|-------|--------|---------|---------|
|            |                    | fc                     | fc/2  | fc/4   | fc/8    | fc/16   |
| 10MHz      | $f_{OSCH}$ 10MHz   | 10MHz                  | 5MHz  | 2.5MHz | 1.25MHz | 625kHz  |
|            | $\times 12$ 120MHz | 60MHz                  | 30MHz | 15MHz  | 7.5MHz  | 3.75MHz |
|            | $\times 16$ 160MHz | 80MHz                  | 40MHz | 20MHz  | 10MHz   | 5MHz    |

The following is an example of settings for PLL0-starting and PLL0 stopping.

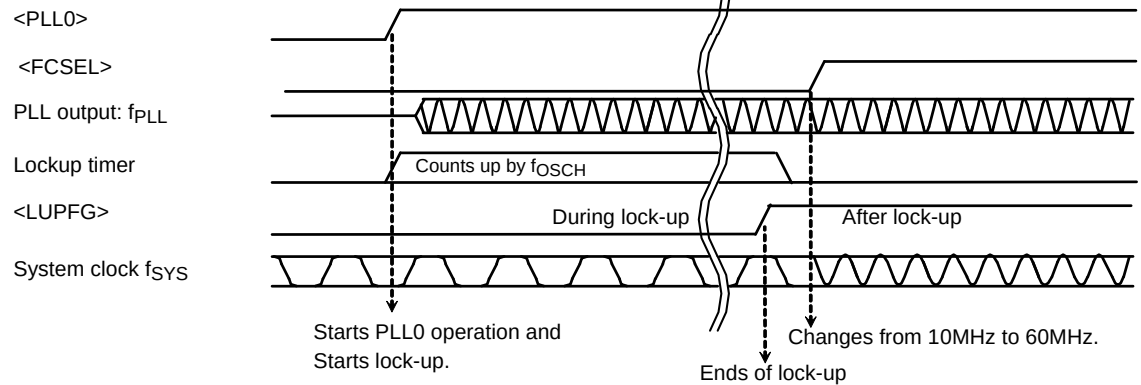
(Example-1) PLL0-starting

```

PLLCR0 EQU 10E8H
PLLCR1 EQU 10E9H
LD (PLLCR1),1XXXXXXXXB ; Enables PLL0 operation and starts lock up.
LUP: BIT 5,(PLLCR0) ; Detects end of lock-up
JR Z,LUP ;
LD (PLLCR0),X1XXXXXXXXB ; Changes fc from 10 MHz to 60 MHz.

```

X: Don't care



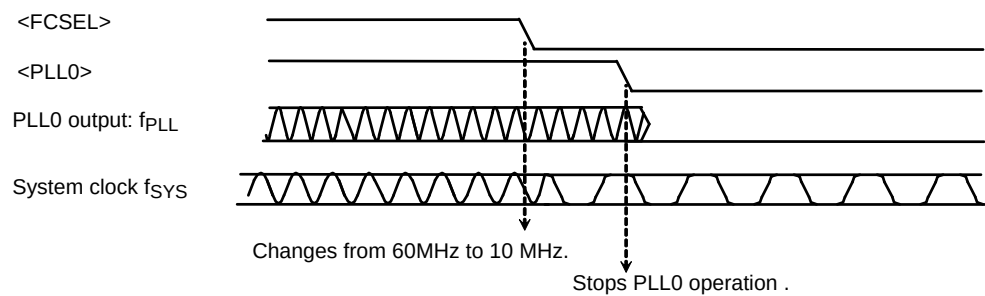
(Example-2) PLL0-stopping

```

PLLCR0 EQU 10E8H
PLLCR1 EQU 10E9H
LD (PLLCR0),X0XXXXXXXXB ; Changes fc from 60 MHz to 10 MHz.
LD (PLLCR1),0XXXXXXXXB ; Stop PLL

```

X: Don't care



Note: PLL1 operates as well.

**Limitations on the use of PLL0**

1. When stopping PLL operation during PLL0 use, execute the following settings in the same order.

```
LD    (PLLCR0),0XXXXXXXXB    ; Change the clock fPLL to fOSCH
LD    (PLLCR1),0XXXXXXXXB    ; Stop PLL0
```

X: Don't care

2. When shifting to STOP mode during PLL use, execute the following settings in the same order.

```
LD    (SYSCR2),XXXX01XXB    ; Set the STOP mode
LD    (PLLCR0), 0XXXXXXXXB    ; Change the system clock fPLL to fOSCH
LD    (PLLCR1), 0XXXXXXXXB    ; Stop PLL0
HALT                                     ; Shift to STOP mode
```

X: Don't care

Examples of settings are shown below:

- (1) Start Up / Change Control

(OK) High frequency oscillator operation mode(f<sub>OSCH</sub>)→PLL0 start up

→ PLL0 use mode (f<sub>PLL</sub>)

```
LUP: LD    (PLLCR1), 1XXXXXXXXB    ; PLL0 start up / lock up start
      BIT    5,(PLLCR0)            ;
      JR     Z,LUP                  ; Check for lock up end flag
      LD    (PLLCR0), X1XXXXXXXXB    ; Change the system clock fOSCH to fPLL
```

X: Don't care

- (2) Change / Stop Control

(OK) PLL0 use mode (f<sub>PLL</sub>)→ High frequency oscillator operation mode(f<sub>OSCH</sub>)

→ PLL0 Stop

```
LD    (PLLCR0),0XXXXXXXXB    ; Change the system clock fPLL to fOSCH
LD    (PLLCR1),0XXXXXXXXB    ; Stop PLL0
```

X: Don't care

(OK) PLL0 use mode (f<sub>PLL</sub>) → Set the STOP mode

→High frequency oscillator operation mode (f<sub>OSCH</sub>) → PLL stop

→ HALT(High frequency oscillator stop)

```
LD    (SYSCR2),XXXX01XXB    ; Set the STOP mode
                                   (This command can be executed before use of PLL0)
LD    (PLLCR0),0XXXXXXXXB    ; Change the system clock fPLL to fOSCH
LD    (PLLCR1),0XXXXXXXXB    ; Stop PLL0
HALT                                     ; Shift to STOP mode
```

X: Don't care

(NG) PLL0 use mode (f<sub>PLL</sub>) → Set the STOP mode

→ HALT(High frequency oscillator stop)

```
LD    (SYSCR2),XXXX01XXB    ; Set the STOP mode
                                   (This command can be executed before use of PLL0)
HALT                                     ; Shift to STOP mode
```

X: Don't care

### 3.4.5 Noise reduction circuits

Noise reduction circuits are built in, allowing implementation of the following features.

- (1) Reduced drivability for high-frequency oscillator circuit
- (2) Reduced drivability for low-frequency oscillator circuit
- (3) Single drive for high-frequency oscillator circuit
- (4) Runaway prevention using SFR protection register

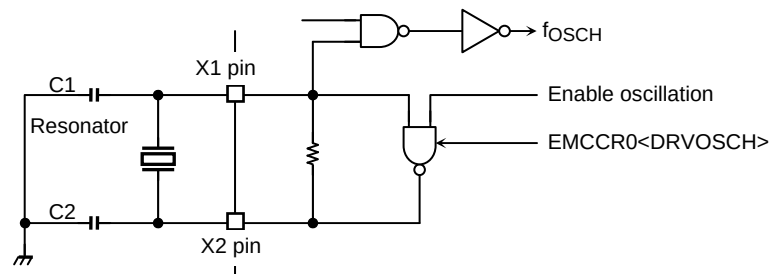
These are set in EMCCR0 to EMCCR2 registers.

- (1) Reduced drivability for high-frequency oscillator circuit

(Purpose)

Reduces noise and power for oscillator when a resonator is used.

(Clock diagram)



(Setting method)

The drivability of the oscillator is reduced by writing "0" to EMCCR0<DRVOSCH> register. At reset, <DRVOSCH> is initialized to "1" and the oscillator starts oscillation by normal-drivability when the power-supply is on.

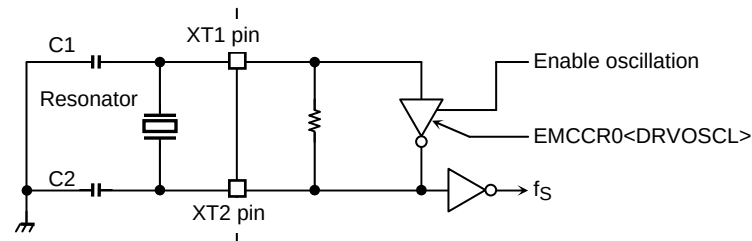
Note: This function (EMCCR0<DRVODCH>= "0") is available when  $f_{OSCH}$  = 6 to 10MHz.

## (2) Reduced drivability for low-frequency oscillator circuit

(Purpose)

Reduces noise and power for oscillator when a resonator is used.

(Block diagram)



(Setting method)

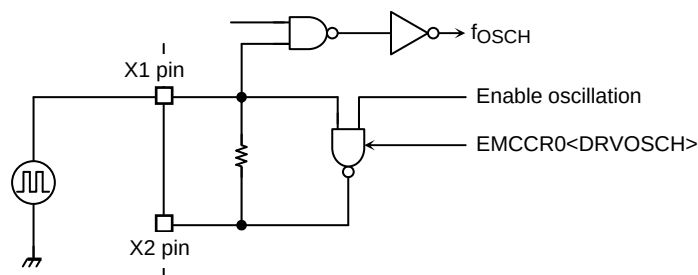
The drivability of the oscillator is reduced by writing “0” to the EMCCR0<DRVOSCL> register. At Reset, <DRVOSCL> is initialized to “1”.

## (3) Single drive for high-frequency oscillator circuit

(Purpose)

Remove the need for twin-drives and protect prevent operational errors caused by noise input to X2 pin when an external-oscillator is used.

(Block diagram)



(Setting method)

The oscillator is disabled and starts operation as buffer by writing “1” to EMCCR0<EXTIN> register. X2 pin’s output is always “1”.

At reset, <EXTIN> is initialized to “0”.

Note: Do not write EMCCR0<EXTIN> = “1” when using external resonator.

## (4) Runaway prevention using SFR protection register

## (Purpose)

Prevention of program runaway caused by introduction of noise.

Write operations to a specified SFR are prohibited so that the program is protected from runaway caused by stopping of the clock or by changes to the memory control register (Memory controller, MMU) which prevent fetch operations.

Runaway error handling is also facilitated by INTP0 interruption.

## Specified SFR list

- |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <ol style="list-style-type: none"> <li>1. Memory controller<br/>B0CSL/H, B1CSL/H, B2CSL/H, B3CSL/H, BECSL/H<br/>MSAR0, MSAR1, MSAR2, MSAR3,<br/>MAMR0, MAMR1, MAMR2, MAMR3, PMEMCR,<br/>MEMCR0, CSTMGCR, WRTMGCR, RDTMGCR0<br/>RDTMGCR1, BROMCR</li> <li>2. MMU<br/>LOCALPX/PY/PZ, LOCALX/LY/LZ,<br/>LOCALRX/RY/RZ, LOCALWX/WY/WZ,<br/>LOCALESX/ESY/ESZ, LOCALEDX/EDY/EDZ,<br/>LOCALOSX/OSY/OSZ, LOCALODX/ODY/ODZ</li> <li>3. Clock gear<br/>SYSCR0, SYSCR1, SYSCR2, EMCCR0</li> <li>4. PLL<br/>PLLCR0, PLLCR1</li> </ol> |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## (Operation explanation)

Execute and release of protection (write operation to specified SFR) becomes possible by setting up a double key to EMCCR1 and EMCCR2 registers.

## (Double key)

1<sup>st</sup>-KEY: writes in sequence, 5AH at EMCCR1 and A5H at EMCCR2

2<sup>nd</sup>-KEY: writes in sequence, A5H at EMCCR1 and 5AH at EMCCR2

Protection state can be confirmed by reading EMCCR0<PROTECT>.

At reset, protection becomes OFF.

INTP0 interruption also occurs when a write operation to the specified SFR is executed with protection in the ON state.



### 3.4.6 Standby controller

#### (1) HALT Modes and Port Drive register

When the HALT instruction is executed, the operating mode switches to IDLE2, IDLE1 or STOP Mode, depending on the contents of the SYSCR2<HALTM1:0> register and each pin-status is set according to the PxDR register, as shown below.

| PxDR<br>(xxxxH) |                       | 7                                                   | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|-----------------|-----------------------|-----------------------------------------------------|------|------|------|------|------|------|------|
|                 | bit symbol            | Px7D                                                | Px6D | Px5D | Px4D | Px3D | Px2D | Px1D | Px0D |
|                 | Read/Write            | R/W                                                 |      |      |      |      |      |      |      |
|                 | System<br>Reset State | 1                                                   | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
|                 | Hot Reset<br>State    | –                                                   | –    | –    | –    | –    | –    | –    | –    |
|                 | Function              | Output/Input buffer drive-register for standby-mode |      |      |      |      |      |      |      |

(Purpose and using)

- This register is used to set each pin-status at stand-by mode.
- All ports have this registers of the format shown above (“x” indicates the port-name.)
- For each register, refer to 3.7 Function of Ports.
- Before “HALT” instruction is executed, set each register pin-status. They will be effective after the CPU has executed the “HALT” instruction.
- This is the case regardless of stand-by mode (IDLE2, IDLE1 or STOP).

The Output/Input-buffer control table is shown below.

| OE | PxnD | Output buffer | Input buffer |
|----|------|---------------|--------------|
| 0  | 0    | OFF           | OFF          |
| 0  | 1    | OFF           | ON           |
| 1  | 0    | OFF           | OFF          |
| 1  | 1    | ON            | OFF          |

Note1: OE denotes an output enable signal before stand-by mode. Basically, PxCR is used as OE.

Note2: “n” in PxnD denotes the bit number of PORTx.

The subsequent actions performed in each mode are as follows:

a.IDLE2: Only the CPU halts.

The internal I/O is available to select operation during IDLE2 mode by setting the following register.

Table 3.4.3 shows the registers setting operation during IDLE2 mode.

Table 3.4.3 SFR setting operation during IDLE2 mode

| Internal I/O  | SFR             |
|---------------|-----------------|
| TMRA01        | TA01RUN<I2TA01> |
| TMRA23        | TA23RUN<I2TA23> |
| TMRA45        | TA45RUN<I2TA45> |
| TMRA67        | TA67RUN<I2TA67> |
| TMRB0         | TB0RUN<I2TB0>   |
| TMRB1         | TB1RUN<I2TB1>   |
| SIO0          | SC0MOD1<I2S0>   |
| SBI           | SBIBR0<I2SBI>   |
| A/D converter | ADMOD1<I2AD>    |
| WDT           | WDMOD<I2WDT>    |

b.IDLE1: Only the oscillator, RTC (real-time clock), and MLD continue to operate.

c. STOP: All internal circuits stop operating.

The operation of each of the different Halt Modes is described in Table 3.4.4.

Table 3.4.4 I/O operation during Halt Modes

| HALT Mode         |                                                                                | IDLE2                                  | IDLE1   | STOP |
|-------------------|--------------------------------------------------------------------------------|----------------------------------------|---------|------|
| SYSCR2 <HALTM1:0> |                                                                                | 11                                     | 10      | 01   |
| Block             | CPU, MAC                                                                       | Stop                                   |         |      |
|                   | I/O ports                                                                      | Depends on PxDR register setting       |         |      |
|                   | TMRA, TMRB                                                                     | Available to select<br>Operation block | Stop    |      |
|                   | SIO, SBI                                                                       |                                        |         |      |
|                   | A/D converter                                                                  |                                        |         |      |
|                   | WDT                                                                            |                                        |         |      |
|                   | I <sup>2</sup> S, SDRAMC,<br>Interrupt controller,<br>SPIC, DMAC, NDFC,<br>USB | Operate                                | Operate |      |
|                   | RTC, MLD                                                                       |                                        |         |      |

## (2) How to release the Halt mode

These HALT states can be released by resetting or requesting an interrupt. The halt release sources are determined by the combination of the states of the interrupt mask register <IFF2:0> and the halt modes. The details for releasing the HALT status are shown in Table 3.4.5.

- Release by interrupt requesting

The HALT mode release method depends on the status of the enabled interrupt. When the interrupt request level set before executing the “HALT” instruction exceeds the value of the interrupt mask register, the interrupt is processed depending on its status after the HALT mode is released, and the CPU status executing the instruction that follows the HALT instruction. When the interrupt request level set before executing the HALT instruction is less than the value of the interrupt mask register, HALT mode release is not executed. (in non-maskable interrupts, interrupt processing is processed after releasing the halt mode regardless of the value of the mask register.) However only for NMI, INT0 to INT5, INT6, INT7 (asynchronous interrupt), INTKEY, INTRTC, INTALM interrupts, even if the interrupt request level set before executing the “HALT” instruction is less than the value of the interrupt mask register, HALT mode release is executed. In this case, the interrupt is processed, and the CPU starts executing the instruction following the HALT instruction, but the interrupt request flag is held at “1”.

- Release by resetting

Release of all halt statuses is executed by resetting.

When the STOP mode is released by RESET, it is necessary to allow enough resetting time for operation of the oscillator to stabilize.

When releasing the halt mode by resetting, the internal RAM data keeps the state before the “HALT” instruction is executed. However the other settings contents are initialized. (Releasing due to interrupts keeps the state before the “HALT” instruction is executed.)

Table 3.4.5 Source of Halt state clearance and Halt clearance operation

| Status of Received Interrupt   |           | Interrupt Enabled<br>(interrupt level) $\geq$ (interrupt mask)                                                                                                                         |                           |                 | Interrupt Disabled<br>(interrupt level) $<$ (interrupt mask) |                 |                 |
|--------------------------------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|-----------------|--------------------------------------------------------------|-----------------|-----------------|
| HALT mode                      |           | IDLE2                                                                                                                                                                                  | IDLE1                     | STOP            | IDLE2                                                        | IDLE1           | STOP            |
| Source of Halt state clearance | Interrupt | INTWDT                                                                                                                                                                                 | ⊙                         | ×               | ×                                                            | —               | —               |
|                                |           | NMI                                                                                                                                                                                    | ⊙                         | ×               | ⊙ <sup>*1</sup>                                              | ○               | ○ <sup>*1</sup> |
|                                |           | INT0 to INT5 (Note1)                                                                                                                                                                   | ⊙                         | ⊙               | ⊙ <sup>*1</sup>                                              | ○               | ○ <sup>*1</sup> |
|                                |           | INTKEY                                                                                                                                                                                 | ⊙                         | ⊙ <sup>*2</sup> | ×                                                            | ○ <sup>*2</sup> | ×               |
|                                |           | INTUSB                                                                                                                                                                                 | ⊙                         | ⊙ <sup>*2</sup> | ×                                                            | ○ <sup>*2</sup> | ×               |
|                                |           | INT6 to INT7(PORT) (Note1)                                                                                                                                                             | ⊙                         | ⊙               | ⊙ <sup>*1</sup>                                              | ○               | ○ <sup>*1</sup> |
|                                |           | INT6 to INT7(TMRB)                                                                                                                                                                     | ⊙                         | ×               | ×                                                            | ×               | ×               |
|                                |           | INTALM, INTRTC                                                                                                                                                                         | ⊙                         | ⊙               | ×                                                            | ○               | ×               |
|                                |           | INTTA0 to INTTA7, INTTP0<br>INTTB00 to INTTB01,<br>INTTB10 to INTTB11<br>INTRX,INTTX, INTSBI<br>INTI2S0<br>INTAD, INTADHP<br>INTSPIRX,INTSPITX<br>INTRSC, INTRDY<br>INTDMA0 to INTDMA5 | ⊙                         | ×               | ×                                                            | ×               | ×               |
|                                |           | RESET                                                                                                                                                                                  | Reset initializes the LSI |                 |                                                              |                 |                 |

⊙: After clearing the Halt mode, CPU starts interrupt processing.

○: After clearing the Halt mode, CPU resumes executing starting from instruction following the HALT instruction.

×: Cannot be used to release the halt mode.

—: The priority level (interrupt request level) of non-maskable interrupts is fixed to 7, the highest priority level. This combination is not available.

\*1: Release of the HALT mode is executed after warm-up time has elapsed.

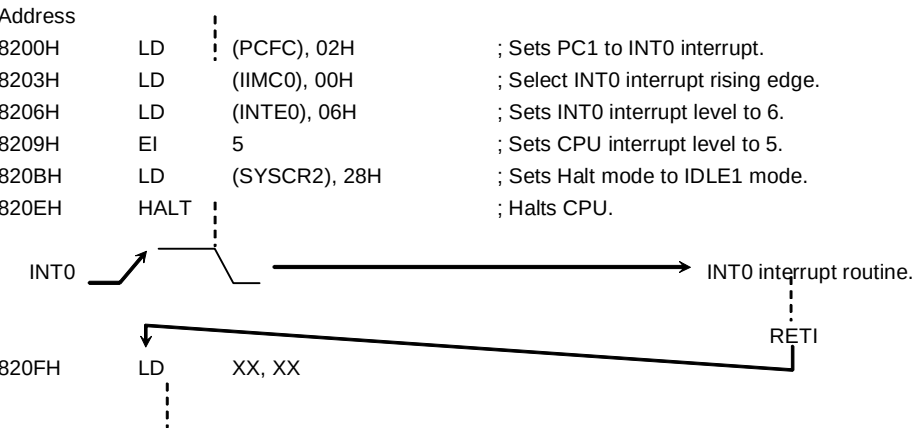
\*2: 6 interrupts of all 24 INTUSB sources can release Halt state from IDLE1 mode, allowing for the construction of low power dissipation systems. However, the method of use is limited as below.

- Shift to IDLE1 mode:  
Execute Halt instruction when the flag of INT\_SUS or INT\_CLKSTOP is "1" ( SUSPEND state )
- Release from IDLE1 mode:  
Release Halt state by INT\_RESUME or INT\_CLKON request (release SUSPEND request)  
Release Halt state by INT\_URST\_STR or INT\_URST\_END request (RESET request)

Note: When the Halt mode is cleared by an INT0 interrupt of the level mode in the interrupt enabled status, hold level H until starting interrupt processing. If level L is set before holding level L, interrupt processing is correctly started.

(Example - releasing IDLE1 Mode)

An INT0 interrupt clears the Halt state when the device is in IDLE1 Mode.



## (3) Operation

## a. IDLE2 Mode

In IDLE2 Mode, only specific internal I/O operations, as designated by the IDLE2 Setting Register, can take place. Instruction execution by the CPU stops.

Figure 3.4.7 illustrates an example of the timing for clearance of the IDLE2 Mode Halt state by an interrupt.

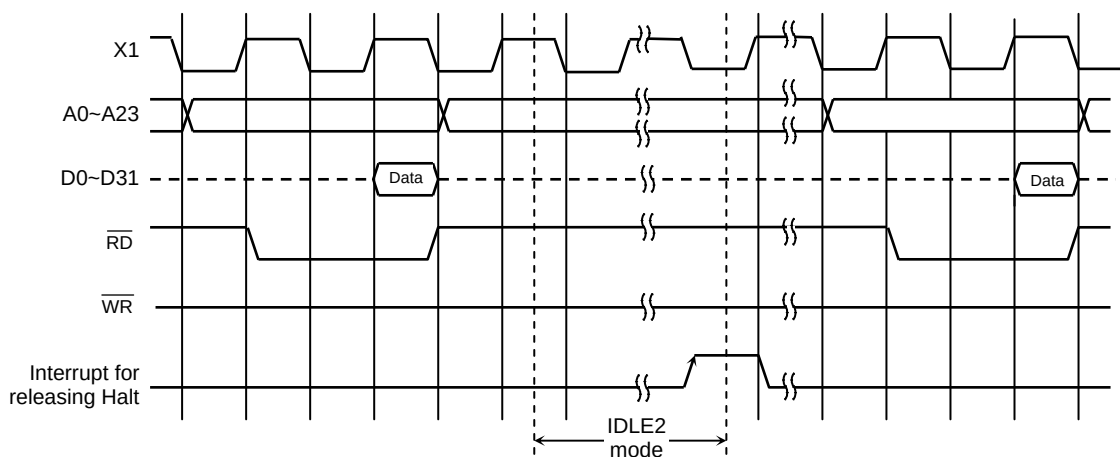


Figure 3.4.7 Timing chart for IDLE2 Mode Halt state cleared by interrupt

## b. IDLE1 Mode

In IDLE1 Mode, only the internal oscillator and the RTC and MLD continue to operate. The system clock stops.

In the Halt state, the interrupt request is sampled asynchronously with the system clock; however, clearance of the Halt state (i.e. restart of operation) is synchronous with it.

Figure 3.4.8 illustrates the timing for clearance of the IDLE1 Mode Halt state by an interrupt.

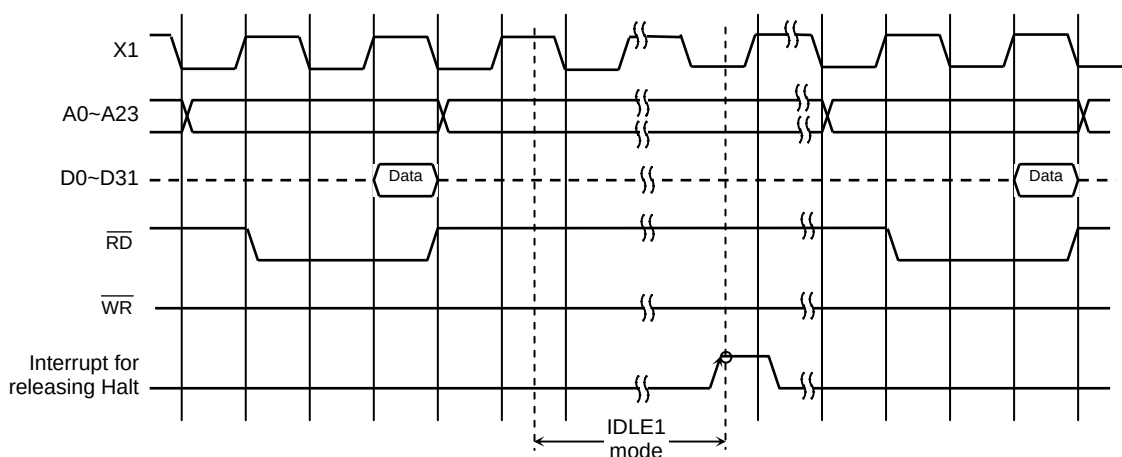


Figure 3.4.8 Timing chart for IDLE1 Mode Halt state cleared by interrupt

c. STOP Mode

When STOP Mode is selected, all internal circuits stop, including the internal oscillator.

After STOP Mode has been cleared system clock output starts when the warm-up time has elapsed, in order to allow oscillation to stabilize.

Figure 3.4.9 illustrates the timing for clearance of the STOP Mode Halt state by an interrupt.

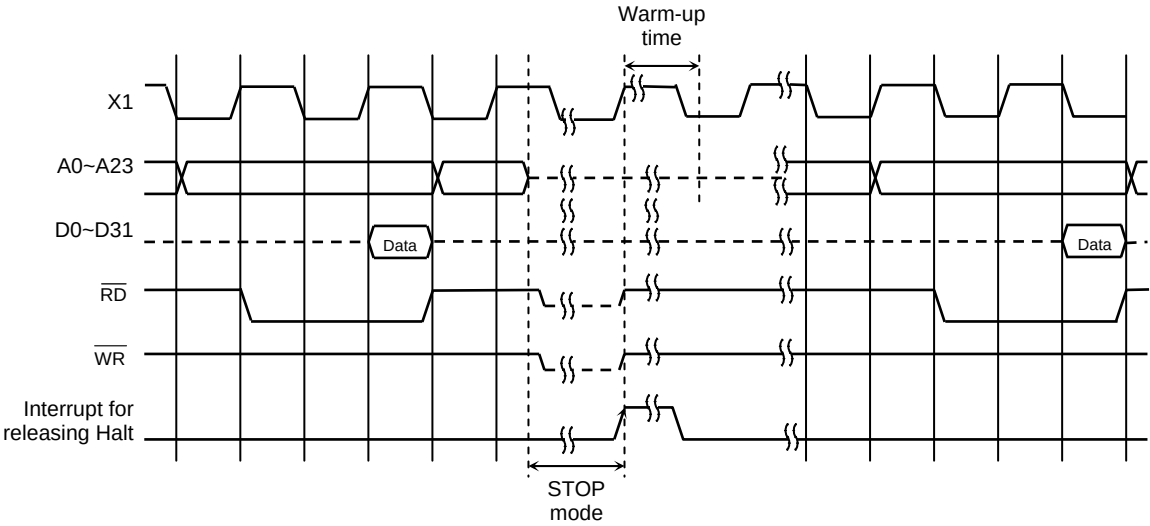


Figure 3.4.9 Timing chart for STOP Mode Halt state cleared by interrupt

Table 3.4.6 Example of warming-up time after releasing STOP-mode

at  $f_{OSCH} = 10\text{ MHz}$

| SYSCR2<WUPTM1:0>   |                 |                 |
|--------------------|-----------------|-----------------|
| 01 ( $2^8$ )       | 10 ( $2^{14}$ ) | 11 ( $2^{16}$ ) |
| 25.6 $\mu\text{s}$ | 1.6384 ms       | 6.5536 ms       |

Table 3.4.7 Input Buffer State Table

| Port Name  | Input Function Name      | Input Buffer State |                           |                         |                             |                         |                           |                         |  |  |  |
|------------|--------------------------|--------------------|---------------------------|-------------------------|-----------------------------|-------------------------|---------------------------|-------------------------|--|--|--|
|            |                          | During Reset       | When the CPU is operating |                         | In HALT mode (IDLE2/1/STOP) |                         |                           |                         |  |  |  |
|            |                          |                    | When Used as function Pin | When Used as Input port | <PxDR>=1                    |                         | <PxDR>=0                  |                         |  |  |  |
|            |                          |                    |                           |                         | When Used as function Pin   | When Used as Input port | When Used as function Pin | When Used as Input port |  |  |  |
| D0-D7      | D0-D7                    | OFF                | ON upon external read     | —                       | OFF                         | —                       | OFF                       | —                       |  |  |  |
| P10-P17    | D8-D15                   | OFF                |                           | ON                      | —                           | ON                      | —                         | OFF                     |  |  |  |
| P60-P67    | —                        | OFF                | —                         |                         | —                           |                         |                           |                         |  |  |  |
| P71-P74    | —                        | ON                 | —                         |                         | —                           |                         |                           |                         |  |  |  |
| P75        | NDR/ $\overline{B}$      |                    | ON                        |                         | ON                          |                         | OFF                       |                         |  |  |  |
| P76        | $\overline{WAIT}$        |                    | —                         |                         | —                           |                         | —                         |                         |  |  |  |
| P90        | —                        |                    | —                         |                         | —                           |                         | —                         |                         |  |  |  |
| P91        | RXD0                     |                    | ON                        |                         | ON                          |                         | OFF                       |                         |  |  |  |
| P92        | $\overline{CTS0}$ ,SCLK0 |                    | —                         |                         | —                           |                         | —                         |                         |  |  |  |
| P96 *1     | INT4                     |                    | ON                        |                         | ON                          |                         | OFF                       |                         |  |  |  |
| P97        | —                        |                    | —                         |                         | —                           |                         | —                         |                         |  |  |  |
| PA0-PA7 *1 | KI0-KI7                  |                    | ON                        |                         | ON                          |                         | OFF                       |                         |  |  |  |
| PC0        | INT0                     |                    |                           |                         |                             |                         |                           |                         |  |  |  |
| PC1        | INT1,TA0IN               |                    |                           |                         |                             |                         |                           |                         |  |  |  |
| PC2        | INT2                     |                    |                           |                         |                             |                         |                           |                         |  |  |  |
| PC3        | INT3,TA2IN               |                    |                           |                         |                             |                         |                           |                         |  |  |  |
| PC4-PC7    | —                        |                    | —                         |                         | —                           |                         | —                         |                         |  |  |  |
| PF0-PF2    | —                        |                    | —                         |                         | —                           |                         | —                         |                         |  |  |  |
| PG0-PG2    | —                        | OFF                | —                         | ON upon port read       | —                           | OFF                     | —                         |                         |  |  |  |
| PG4,PG5 *2 | —                        |                    | ON                        |                         | ON                          |                         | ON                        |                         |  |  |  |
| PG3 *2     | $\overline{ADTRG}$       | ON                 | ON                        | ON                      | ON                          | ON                      | ON                        |                         |  |  |  |
| PJ5-PJ6    | —                        |                    | —                         |                         | —                           |                         | —                         |                         |  |  |  |
| PL0-PL7    | D16-D23                  |                    | ON upon external read     |                         | OFF                         |                         | OFF                       |                         |  |  |  |
| PN0-PN7    | —                        |                    | —                         |                         | —                           |                         | —                         |                         |  |  |  |
| PP3        | INT5                     |                    | ON                        |                         | ON                          |                         | OFF                       |                         |  |  |  |
| PP4        | INT6,TB0IN0              |                    |                           |                         |                             |                         |                           |                         |  |  |  |
| PP5        | INT7,TB1IN0              |                    |                           |                         |                             |                         |                           |                         |  |  |  |
| PR0        | SPDI                     |                    |                           |                         |                             |                         |                           |                         |  |  |  |
| PR1-PR3    | —                        |                    | —                         |                         | —                           |                         | —                         |                         |  |  |  |
| PT0-PT7    | D24-D31                  |                    | ON upon external read     |                         | OFF                         |                         | OFF                       |                         |  |  |  |
| PV6-PV7    | SDA, SCL                 |                    | ON                        |                         | ON                          |                         | ON                        | OFF                     |  |  |  |
| PX5        | X1USB                    |                    |                           |                         |                             |                         |                           |                         |  |  |  |
| D+, D-     | —                        | Always ON          |                           |                         |                             |                         |                           |                         |  |  |  |
| RESET      | —                        |                    |                           |                         |                             |                         |                           |                         |  |  |  |
| AM0,AM1    | —                        |                    |                           |                         |                             |                         |                           |                         |  |  |  |
| NMI        | —                        |                    |                           |                         |                             |                         |                           |                         |  |  |  |
| X1,XT1     | —                        |                    |                           |                         |                             |                         |                           |                         |  |  |  |
|            |                          |                    |                           |                         | IDLE2/DLE1: ON              |                         |                           |                         |  |  |  |

ON: The buffer is always turned on. A current flows through the input buffer if the input pin is not driven.

OFF: The buffer is always turned off.

— : Not applicable

\*1: Port having a pull-up/pull-down resistor.

\*2: AIN input does not cause a current to flow through the buffer.

Table 3.4.8 Output buffer State Table (1/2)

| Port Name | Output Function Name | Output Buffer State |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
|-----------|----------------------|---------------------|---------------------------|--------------------------|-----------------------------|--------------------------|---------------------------|--------------------------|-----|----|-----|-----|--|--|--|--|
|           |                      | During Reset        | When the CPU is operating |                          | In HALT mode (IDLE2/1/STOP) |                          |                           |                          |     |    |     |     |  |  |  |  |
|           |                      |                     |                           |                          | <PxDR> = 1                  |                          | <PxDR> = 0                |                          |     |    |     |     |  |  |  |  |
|           |                      |                     | When Used as function Pin | When Used as Output port | When Used as function Pin   | When Used as Output port | When Used as function Pin | When Used as Output port |     |    |     |     |  |  |  |  |
| D0-7      | D0-D7                | OFF                 | ON upon external write    | –                        | OFF                         | –                        | OFF                       | –                        |     |    |     |     |  |  |  |  |
| P10-17    | D8-D15               | OFF                 |                           | ON                       | ON                          |                          |                           |                          |     |    |     |     |  |  |  |  |
| P40-P47   | A0-A7                | ON                  | ON                        | ON                       | ON                          | ON                       |                           | OFF                      | OFF |    |     |     |  |  |  |  |
| P50-P57   | A8-A15               |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| P60-67    | A16-A23              |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| P70       | RD                   |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| P71       | WRLL , NDRE          |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| P72       | WRLU , NDWE          | OFF                 | –                         | –                        | –                           | –                        | OFF                       | OFF                      |     |    |     |     |  |  |  |  |
| P73       | EA24                 |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| P74       | EA25                 |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| P75       | R/ w                 |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| P76       | –                    |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| P80       | CS0                  | ON                  | ON                        | ON                       | ON                          | ON                       | OFF                       | OFF                      |     |    |     |     |  |  |  |  |
| P81       | CS1 , SDCS           |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| P82       | CS2 , CSZA SDCS      |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| P83       | CS3 , CSXA           |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| P84       | CSZB                 |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| P85       | CSZC                 |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| P86       | CSZD , ND0CE         |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| P87       | CSXB , NDICE         |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| P90       | TXD0                 | OFF                 | –                         | –                        | –                           | –                        | OFF                       | –                        |     |    |     |     |  |  |  |  |
| P91       | –                    |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| P92       | SCLK0                |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| P96       | PX                   | OFF                 | ON                        | –                        | ON                          | –                        | OFF                       | –                        |     |    |     |     |  |  |  |  |
| P97       | PY                   |                     | –                         |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| PC0-PC3   | –                    |                     | –                         | ON                       | ON                          | ON                       | ON                        | OFF                      | OFF |    |     |     |  |  |  |  |
| PC4       | EA26                 |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| PC5       | EA27                 |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| PC6       | EA28                 |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| PC7       | KO8                  |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| PF0       | I2S0CKO              |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| PF1       | I2S0DO               |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| PF2       | I2S0WS               |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| PF7       | SDCLK                | ON                  | ON                        | ON                       | ON                          | OFF                      | OFF                       |                          |     |    |     |     |  |  |  |  |
| PG2       | MX                   | OFF                 |                           |                          |                             |                          |                           | –                        | –   | –  | –   |     |  |  |  |  |
| PG3       | MY                   |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| PJ0       | SDRAS , SRLLB        | ON                  |                           |                          |                             |                          |                           | ON                       | ON  | ON | OFF | OFF |  |  |  |  |
| PJ1       | SDCAS , SRLUB        |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| PJ2       | SDWE , SRWR          |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| PJ3       | SDLLDQM              |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| PJ4       | SDLUDQM              |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| PJ5       | NDALE, SRULB         | OFF                 |                           |                          |                             |                          |                           | ON                       | ON  | ON | OFF | OFF |  |  |  |  |
| PJ6       | NDCLE, SRUUB         |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| PJ7       | SDCKE                | ON                  |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| PK0-PK7   | –                    | OFF                 |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |
| PL0-PL7   | D16-D23              |                     |                           |                          |                             |                          |                           |                          |     |    |     |     |  |  |  |  |



Table 3.4.9 Output buffer state table (2/2)

| Port Name | Output Function Name | Output Buffer State |                                |                          |                             |                          |                                  |                          |     |     |   |   |
|-----------|----------------------|---------------------|--------------------------------|--------------------------|-----------------------------|--------------------------|----------------------------------|--------------------------|-----|-----|---|---|
|           |                      | During Reset        | When the CPU is operating      |                          | In HALT mode (IDLE2/1/STOP) |                          |                                  |                          |     |     |   |   |
|           |                      |                     |                                |                          | <PxDR>=1                    |                          | <PxDR>=0                         |                          |     |     |   |   |
|           |                      |                     | When Used as function Pin      | When Used as Output port | When Used as function Pin   | When Used as Output port | When Used as function Pin        | When Used as Output port |     |     |   |   |
| PM1       | MLDALM,TA1OUT        | ON                  | ON                             | ON                       | ON                          | ON                       | OFF                              | OFF                      |     |     |   |   |
| PM2       | MLDALM , ALARM       |                     |                                |                          |                             |                          |                                  |                          |     |     |   |   |
| PM7       | —                    |                     |                                |                          |                             |                          |                                  |                          |     |     |   |   |
| PN0-PN7   | KO0-KO7              | OFF                 |                                |                          |                             |                          |                                  |                          | —   | —   | — | — |
| PP3       | TA7OUT               |                     |                                |                          |                             |                          |                                  |                          |     |     |   |   |
| PP4-PP5   | —                    |                     | ON                             |                          | ON                          |                          | ON                               |                          | ON  | OFF |   |   |
| PP6       | TB0OUT0              |                     |                                |                          |                             |                          |                                  |                          |     |     |   |   |
| PP7       | TB1OUT0              | OFF                 |                                |                          | —                           |                          | —                                |                          | —   | —   |   |   |
| PR0       | —                    |                     |                                |                          |                             |                          |                                  |                          |     |     |   |   |
| PR1       | SPDO                 |                     | ON                             |                          | ON                          |                          | ON                               |                          | OFF |     |   |   |
| PR2       | SPCS                 |                     |                                |                          |                             |                          |                                  |                          |     |     |   |   |
| PR3       | SPCLK                |                     |                                |                          |                             |                          |                                  |                          |     |     |   |   |
| PT0-PT7   | D24-D31              |                     |                                |                          |                             |                          |                                  |                          |     |     |   |   |
| PV6       | SDA                  | OFF                 | ON                             |                          | ON                          |                          | ON                               |                          | OFF |     |   |   |
| PV7       | SCL                  |                     |                                |                          |                             |                          |                                  |                          |     |     |   |   |
| PX4       | CLKOUT               | ON                  | ON                             |                          | ON                          |                          | ON                               |                          | OFF |     |   |   |
| PX5       | —                    | OFF                 | —                              |                          | —                           |                          | —                                |                          | —   |     |   |   |
| D+, D–    | —                    | OFF                 | ON/OF depend on USBC operation |                          |                             |                          |                                  |                          |     |     |   |   |
| X2        | —                    | Always ON           |                                |                          |                             |                          | IDLE2/1:ON,<br>STOP: output "H"  |                          |     |     |   |   |
| XT2       | —                    |                     |                                |                          |                             |                          | IDLE2/1:ON,<br>STOP: output "HZ" |                          |     |     |   |   |

ON: The buffer is always turned on. When the bus is released, however, output buffers for some pins are turned off.

OFF: The buffer is always turned off.

— : Not applicable

\*1: Port having a pull-up/pull-down resistor.

### 3.5 Interrupts

Interrupts are controlled by the CPU Interrupt Mask Register <IFF2:0> (bits 12 to 14 of the Status Register) and by the built-in interrupt controller.

TMP92CF30 has a total of 58 interrupts divided into the following five types:

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>Interrupts generated by CPU: 9 sources</p> <ul style="list-style-type: none"> <li>• Software interrupts: 8 sources</li> <li>• Illegal Instruction interrupt: 1 source</li> </ul> <p>Internal interrupts: 39 sources</p> <ul style="list-style-type: none"> <li>• Internal I/O interrupts: 31 sources</li> <li>• Micro DMA Transfer End interrupts /HDMA Transfer End interrupts: 6 sources</li> <li>• Micro DMA Transfer End interrupts: 2 source</li> </ul> <p>External interrupts: 10 sources</p> <ul style="list-style-type: none"> <li>• Interrupts on external pins (NMI, INT0 to INT7, INTKEY)</li> </ul> |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

A fixed individual interrupt vector number is assigned to each interrupt source. Any one of six levels of priority can also be assigned to each maskable interrupt. Non-maskable interrupts have a fixed priority level of 7, the highest level.

When an interrupt is generated, the interrupt controller sends the priority of that interrupt to the CPU. When more than one interrupt is generated simultaneously, the interrupt controller sends the priority value of the interrupt with the highest priority to the CPU. (The highest priority level is 7, the level used for non-maskable interrupts.)

The CPU compares the interrupt priority level which it receives with the value held in the CPU interrupt mask register <IFF2:0>. If the priority level of the interrupt is greater than or equal to the value in the interrupt mask register, the CPU accepts the interrupt.

However, software interrupts and illegal instruction interrupts generated by the CPU, and are processed irrespective of the value in <IFF2:0>.

The value in the interrupt mask register <IFF2:0> can be changed using the EI instruction (EI num sets <IFF2:0> to num). For example, the command EI3 enables the acceptance of all non-maskable interrupts and of maskable interrupts whose priority level, as set in the interrupt controller, is 3 or higher. The commands EI and EI0 enable the acceptance of all non-maskable interrupts and of maskable interrupts with a priority level of 1 or above (hence both are equivalent to the command EI1).

The DI instruction (Sets <IFF2:0> to 7) is exactly equivalent to the EI7 instruction. The DI instruction is used to disable all maskable interrupts (since the priority level for maskable interrupts ranges from 0 to 6). The EI instruction takes effect as soon as it is executed.

In addition to the general-purpose interrupt processing mode described above, there is also a micro DMA processing mode that can transfer data to internal/external memory and built-in I/O, and HDMA processing mode. In micro DMA mode the CPU, and in HDMA mode the DMA controller automatically transfers data in 1byte, 2byte or 4byte blocks. HDMA mode allows transfer faster than Micro DMA mode.

In addition, the TMP92CF30 also has a software start function in which micro DMA and HDMA processing is requested in software rather than by an interrupt. Figure 3.5.1 is a flowchart showing overall interrupts processing.

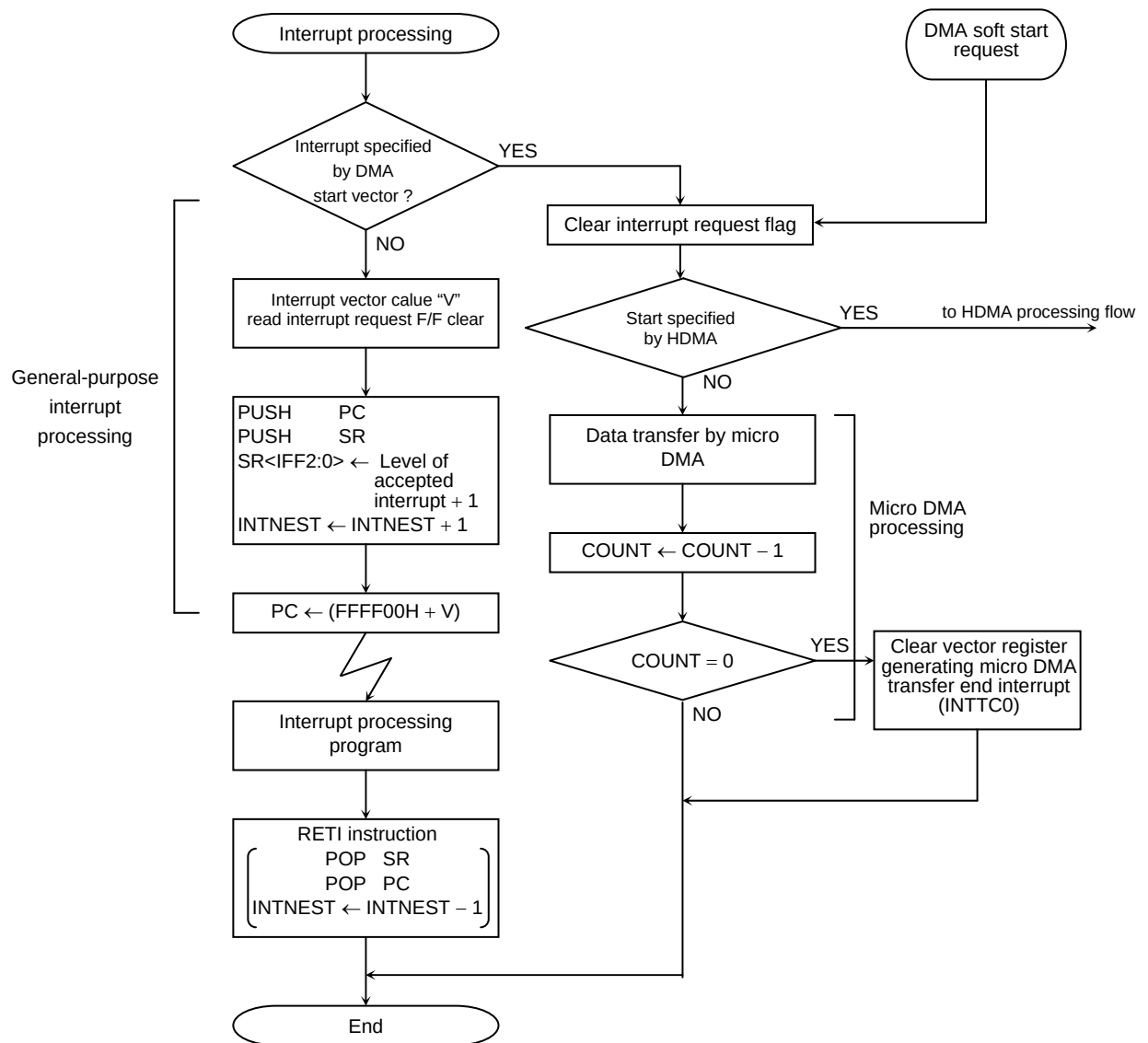


Figure 3.5.1 Interrupt processing Sequence

### 3.5.1 General-purpose Interrupt Processing

When the CPU accepts an interrupt, it usually performs the following sequence of operations. However, in the case of software interrupts and illegal instruction interrupts generated by the CPU, the CPU skips steps (1) and (3), and executes only steps (2), (4), and (5).

- (1) The CPU reads the interrupt vector from the interrupt controller. When more than one interrupt with the same priority level has been generated simultaneously, the interrupt controller generates an interrupt vector in accordance with the default priority and clears the interrupt requests. (The default priority is determined as follows: The smaller the vector value, the higher the priority.)
- (2) The CPU pushes the program counter (PC) and status register (SR) onto the top of the stack (Pointed to by XSP).
- (3) The CPU sets the value of the CPU's interrupt mask register <IFF2:0> to the priority level for the accepted interrupt plus 1. However, if the priority level for the accepted interrupt is 7, the register's value is set to 7.
- (4) The CPU increments the interrupt nesting counter INTNEST by 1.
- (5) The CPU jumps to the address given by adding the contents of address FFFF00H + the interrupt vector, then starts the interrupt processing routine.

On completion of interrupt processing, the RETI instruction is used to return control to the main routine. RETI restores the contents of the program counter and the status register from the stack and decrements the interrupt nesting counter INTNEST by 1.

Non-maskable interrupts cannot be disabled by a user program. Maskable interrupts, however, can be enabled or disabled by a user program. A program can set the priority level for each interrupt source. (A priority level setting of 0 or 7 will disable an interrupt request.) If an interrupt request is received for an interrupt with a priority level equal to or greater than the value set in the CPU interrupt mask register <IFF2:0>, the CPU will accept the interrupt. The CPU interrupt mask register <IFF2:0> is then set to the value of the priority level for the accepted interrupt plus 1.

If during interrupt processing, an interrupt is generated with a higher priority than the interrupt currently being processed, or if, during the processing of a non-maskable interrupt processing, a non-maskable interrupt request is generated from another source, the CPU will suspend the routine which it is currently executing and accept the new interrupt. When processing of the new interrupt has been completed, the CPU will resume processing of the suspended interrupt.

If the CPU receives another interrupt request while performing processing steps (1) to (5), the new interrupt will be sampled immediately after execution of the first instruction of its interrupt processing routine. Specifying DI as the start instruction disables nesting of maskable interrupts.

A reset initializes the interrupt mask register <IFF2:0> to "111", disabling all maskable interrupts.

Table 3.5.1 shows the TMP92CF30 interrupt vectors and micro DMA start vectors. FFFF00H to FFFFFFFH (256 bytes) is designated as the interrupt vector area.

Table 3.5.1 TMP92CF30 Interrupt Vectors and Micro DMA/HDMA Start Vectors

| Default Priority | Type         | Interrupt Source and Source of Micro DMA Request | Vector Value | Address Refer to Vector | Micro DMA /HDMA Start Vector |
|------------------|--------------|--------------------------------------------------|--------------|-------------------------|------------------------------|
| 1                | Non maskable | Reset or [SWI0] instruction                      | 0000H        | FFFF00H                 |                              |
| 2                |              | [SWI1] instruction                               | 0004H        | FFFF04H                 |                              |
| 3                |              | Illegal instruction or [SWI2] instruction        | 0008H        | FFFF08H                 |                              |
| 4                |              | [SWI3] instruction                               | 000CH        | FFFF0CH                 |                              |
| 5                |              | [SWI4] instruction                               | 0010H        | FFFF10H                 |                              |
| 6                |              | [SWI5] instruction                               | 0014H        | FFFF14H                 |                              |
| 7                |              | [SWI6] instruction                               | 0018H        | FFFF18H                 |                              |
| 8                |              | [SWI7] instruction                               | 001CH        | FFFF1CH                 |                              |
| 9                |              | NMI: NMI pin input                               | 0020H        | FFFF20H                 |                              |
| 10               |              | INTWD: Watchdog timer                            | 0024H        | FFFF24H                 |                              |
| –                | Maskable     | Micro DMA (Note 2)                               | –            | –                       | –                            |
| 11               |              | INT0: INT0 pin input                             | 0028H        | FFFF28H                 | 0AH(Note 1)                  |
| 12               |              | INT1: INT1 pin input                             | 002CH        | FFFF2CH                 | 0BH                          |
| 13               |              | INT2: INT2 pin input                             | 0030H        | FFFF30H                 | 0CH                          |
| 14               |              | INT3: INT3 pin input                             | 0034H        | FFFF34H                 | 0DH                          |
| 15               |              | INT4: INT4 pin input (TSI)                       | 0038H        | FFFF38H                 | 0EH                          |
| 16               |              | INTALM: ALM (8192Hz, 512Hz, 64Hz, 2Hz, 1Hz)      | 003CH        | FFFF3CH                 | 0FH                          |
| 17               |              | INTTA4: 8-bit timer 4                            | 0040H        | FFFF40H                 | 10H                          |
| 18               |              | INTTA5: 8-bit timer 5                            | 0044H        | FFFF44H                 | 11H                          |
| 19               |              | INTTA6: 8-bit timer 6                            | 0048H        | FFFF48H                 | 12H                          |
| 20               |              | INTTA7: 8-bit timer 7                            | 004CH        | FFFF4CH                 | 13H                          |
| 21               |              | INTP0: Protect 0 (Write to SFR)                  | 0050H        | FFFF50H                 | 14H                          |
| 22               |              | (Reserved)                                       | 0054H        | FFFF54H                 | 15H                          |
| 23               |              | INTTA0: 0                                        | 0058H        | FFFF58H                 | 16H                          |
| 24               |              | INTTA1: 8-bit timer 1                            | 005CH        | FFFF5CH                 | 17H                          |
| 25               |              | INTTA2: 8-bit timer 2                            | 0060H        | FFFF60H                 | 18H                          |
| 26               |              | INTTA3: 8-bit timer 3                            | 0064H        | FFFF64H                 | 19H                          |
| 27               |              | INTTB0: 16-bit timer 0                           | 0068H        | FFFF68H                 | 1AH                          |
| 28               |              | INTTB1: 16-bit timer 0                           | 006CH        | FFFF6CH                 | 1BH                          |
| 29               |              | INTKEY: Key wakeup                               | 0070H        | FFFF70H                 | 1CH                          |
| 30               |              | INTRTC: RTC (Alarm interrupt)                    | 0074H        | FFFF74H                 | 1DH                          |
| 31               |              | (Reserved)                                       | 0078H        | FFFF78H                 | 1EH                          |
| 32               |              | (Reserved)                                       | 007CH        | FFFF7CH                 | 1FH                          |
| 33               |              | INTRX0: Serial receive end                       | 0080H        | FFFF80H                 | 20H (Note 1)                 |
| 34               |              | INTTX0: Serial transmission end                  | 0084H        | FFFF84H                 | 21H                          |
| 35               |              | INTTB10: 16-bit timer 1                          | 0088H        | FFFF88H                 | 22H                          |
| 36               |              | INTTB11: 16-bit timer 1                          | 008CH        | FFFF8CH                 | 23H                          |
| 37               |              | INT5: INT5 pin input                             | 0090H        | FFFF90H                 | 24H                          |
| 38               |              | INT6: INT6 pin input                             | 0094H        | FFFF94H                 | 25H                          |
| 39               |              | INT7: INT7 pin input                             | 0098H        | FFFF98H                 | 26H                          |
| 40               |              | INTI2S0: I <sup>2</sup> S (Channel 0)            | 009CH        | FFFF9CH                 | 27H                          |
| 41               |              | (Reserved)                                       | 00A0H        | FFFA0H                  | 28H                          |
| 42               |              | INTADM: AD Monitor function                      | 00A4H        | FFFA4H                  | 29H                          |
| 43               |              | INTSBI: SBI                                      | 00A8H        | FFFA8H                  | 2AH                          |
| 44               |              | INTSPIRX: SPIC receive                           | 00ACH        | FFFACH                  | 2BH                          |
| 45               |              | INTSPITX: SPIC transmission                      | 00B0H        | FFFB0H                  | 2CH                          |
| 46               |              | INTRSC: NAND Flash controller                    | 00B4H        | FFFB4H                  | 2DH                          |
| 47               |              | INTRDY: NAND Flash controller                    | 00B8H        | FFFB8H                  | 2EH                          |
| 48               |              | INTUSB: USB                                      | 00BCH        | FFFBCH                  | 2FH                          |
| 49               |              | INTRX1: Serial receive end                       | 00C0H        | FFFC0H                  | 30H                          |
| 50               |              | INTTX1: Serial transmission end                  | 00C4H        | FFFC4H                  | 31H                          |

| Default Priority | Type     | Interrupt Source and Source of Micro DMA Request | Vector Value | Address Refer to Vector | Micro DMA /HDMA Start Vector |
|------------------|----------|--------------------------------------------------|--------------|-------------------------|------------------------------|
| 51               | Maskable | INTADHP: AD most priority conversion end         | 00C8H        | FFFFC8H                 | 32H                          |
| 52               |          | INTAD: AD conversion end                         | 00CCH        | FFFFCCH                 | 33H                          |
| 53               |          | INTTC0/INTDMA0: Micro DMA0 /HDMA0 end            | 00D0H        | FFFFD0H                 | 34H                          |
| 54               |          | INTTC1/INTDMA1: Micro DMA1 /HDMA1 end            | 00D4H        | FFFFD4H                 | 35H                          |
| 55               |          | INTTC2/INTDMA2: Micro DMA2 /HDMA2 end            | 00D8H        | FFFFD8H                 | 36H                          |
| 56               |          | INTTC3/INTDMA3: Micro DMA3 /HDMA3 end            | 00DCH        | FFFFDCH                 | 37H                          |
| 57               |          | INTTC4/INTDMA4: Micro DMA4 /HDMA4 end            | 00E0H        | FFFFE0H                 | 38H                          |
| 58               |          | INTTC5/INTDMA5: Micro DMA5 /HDMA5 end            | 00E4H        | FFFFE4H                 | 39H                          |
| 59               |          | INTTC6 : Micro DMA6 end                          | 00E8H        | FFFFE8H                 | 3AH                          |
| 60               |          | INTTC7 : Micro DMA7 end                          | 00ECH        | FFFFECH                 | 3BH                          |
| –                |          | (Reserved)                                       | 00F0H        | FFFFF0H                 | –                            |
| to               |          |                                                  | :            | :                       | to                           |
| –                |          |                                                  | 00FCH        | FFFFFCH                 | –                            |

Note 1: When initiating micro DMA/HDMA , set at edge detect mode.

Note 2 : Micro DMA default priority.

Micro DMA initiation takes priority over other maskable interrupt.

### 3.5.2 Micro DMA processing

In addition to general-purpose interrupt processing, the TMP92CF30 also includes a micro DMA function and HDMA function. This section explains about Micro DMA function. For the HDMA function, please refer 3.7 DMA controller.

Micro DMA processing for interrupt requests set by micro DMA is performed at the highest priority level for maskable interrupts (Level 6), regardless of the priority level of the interrupt source.

Because the micro DMA function is implemented through the CPU, when the CPU is placed in a stand-by state (IDLE2, IDLE1, STOP) by a HALT instruction, the requirement of the micro DMA will be ignored (Pending).

Micro DMA supports 8 channels and can be transferred continuously by specifying the micro DMA burst function as below.

Note: When using the micro DMA transfer end interrupt, always write "1" to bit 7 of SIMC register.

### (1) Micro DMA operation

When an interrupt request is generated by an interrupt source that specified by the micro DMA /HDMA start vector register, and Micro DMA start is specified by DMA selection register, the micro DMA triggers a micro DMA request to the CPU at interrupt priority level 6 and starts processing the request. When IFF = 7, Micro DMA request cannot be accepted.

The 8 micro DMA channels allow micro DMA processing to be set for up to 8 types of interrupt at once.

When micro DMA is accepted, the interrupt request flip-flop assigned to that channel is cleared. Data in one-byte, two-byte or four-byte blocks is automatically transferred at once from the transfer source address to the transfer destination address set in the control register, and the transfer counter is decremented by "1". If the value of the counter after it has been decremented is not "0", DMA processing ends with no change in the value of the micro DMA start vector register. If the value of the decremented counter is "0", a micro DMA transfer end interrupt (INTTC0 to INTTC7) is sent from the CPU to the interrupt controller.

In addition, the micro DMA /HDMA start vector register is cleared to "0", the next micro DMA operation is disabled and micro DMA processing terminates.

If an interrupt request is triggered for the interrupt source in use during the interval between the time at which the micro DMA /HDMA start vector is cleared and the next setting, general-purpose interrupt processing is performed at the interrupt level set. Therefore, if the interrupt is only being used to initiate micro DMA /HDMA (and not as a general-purpose interrupt), the interrupt level should first be set to 0 (i.e, interrupt requests should be disabled).

If micro DMA and general-purpose interrupts are being used together as described above, the level of the interrupt which is being used to initiate micro DMA processing should first be set to a lower value than all the other interrupt levels. (Note1) In this case, edge-triggered interrupts are the only kinds of general interrupts which can be accepted.

Note1: If the priority level of micro DMA is set higher than that of other interrupts, CPU operates as follows.

In case INTxxx interrupt is generated first and then INTyyy interrupt is generated between checking "Interrupt specified by micro DMA start vector" (in the Figure 3.5.1) and reading interrupt vector with setting below. The vector shifts to that of INTyyy at the time.

This is because the priority level of INTyyy is higher than that of INTxxx.

In the interrupt routine, CPU reads the vector of INTyyy because cheking of micro DMA has finished. And INTyyy is generated regardless of transfer counter of micro DMA.

INTxxx: level 1 without micro DMA

INTyyy: level 6 with micro DMA

If micro DMA requests are set simultaneously for more than one channel, priority is not based on the interrupt priority level but on the channel number: The lower the channel number, the higher the priority (Channel 0 thus has the highest priority and channel 7 the lowest).

Note2: Don't start any micro DMAs by one interrupt. If any micro DMA are set by it, micro DMA that channel number is biggest (priority is lowest) is not started. (Because interrupt flag is cleared by micro DMA that priority is highest)



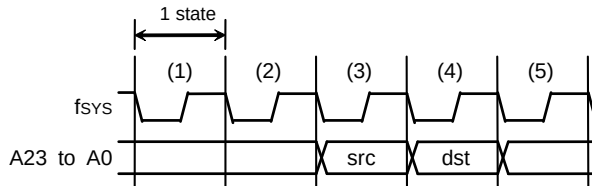
Although the control registers used for setting the transfer source and transfer destination addresses are 32 bits wide, this type of register can only output 24-bit addresses. Accordingly, micro DMA can only access 16 Mbytes (The upper 8 bits of a 32-bit address are not valid).

Three micro DMA transfer modes are supported: 1byte transfer, 2byte (One word) transfers and 4byte transfers. After a transfer in any mode, the transfer source and transfer destination addresses will either be incremented or decremented, or will remain unchanged. This simplifies the transfer of data from memory to memory, from I/O to memory, from memory to I/O, and from I/O to I/O. For details of the various transfer modes, see section 3.5.2 (4) “Detailed description of the transfer mode register”.

Since a transfer counter is a 16-bit counter, up to 65536 micro DMA processing operations can be performed per interrupt source (Provided that the transfer counter for the source is initially set to 0000H).

Micro DMA processing can be initiated by any one of 47 different interrupts – the 46 interrupts shown in the micro DMA start vectors in Table 3.5.1 and a micro DMA soft start.

Figure 3.5.2 shows a 2-byte transfer carried out using a micro DMA cycle in Transfer Destination Address INC Mode (micro DMA transfers are the same in every mode except Counter Mode). (The conditions for this cycle are as follows: both source and destination memory are internal-RAM and multiple of 4 numbered source and destination addresses).



Note: In fact, src and dst address are not outputted to A23-A0 pins because they are internal RAM address.

Figure 3.5.2 Timing for micro DMA cycle

States (1) and (2): Instruction fetch cycle (Prefetches the next instruction code)

State (3): Micro DMA read cycle.

State (4): Micro DMA writes cycle.

State (5): (The same as in state (1), (2).)

(2) Soft start function

The TMP92CF30 can initiate micro DMA/HDMA either with an interrupt or by using the micro DMA /HDMA soft start function, in which micro DMA or HDMA is initiated by a Write cycle which writes to the register DMAR.

Writing “1” to each bit of DMAR register causes micro DMA or HDMA to be performed once (If write “0” to each bit, micro DMA doesn’t operate). On completion of the transfer, the bits of DMAR for the completed channel are automatically cleared to “0”.

When writing again “1” to it, soft start can execute continuously until the DMA transfer counter (DMACn) or HDMA transfer counter B (HDMACBn) become “0”.

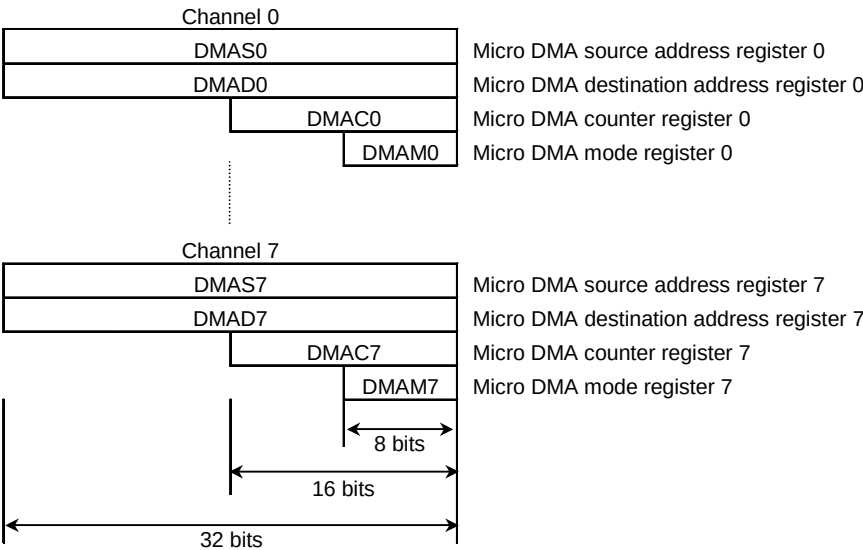
When a burst is specified by the register DMAB, data is transferred continuously from the initiation of micro DMA until the value in the micro DMA transfer counter is “0”. If execute soft start during micro DMA transfer by interrupt source, micro DMA transfer counter doesn’t change. Don’t use Read-modify-write instruction to avoid writign to other bits by mistake.

- Note1: If it is started by software, don't set any channels to start in same time.
- Note2: If be started sequentially, restart it after confirming micro DMA of all channels is completed (all micro DMA are set to “0”).

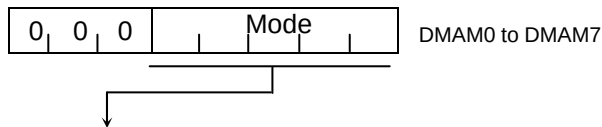
| Symbol | Name        | Address                | 7            | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|--------|-------------|------------------------|--------------|-------|-------|-------|-------|-------|-------|-------|
| DMAR   | DMA Request | 109H<br>(Prohibit RMW) | DREQ7        | DREQ6 | DREQ5 | DREQ4 | DREQ3 | DREQ2 | DREQ1 | DREQ0 |
|        |             |                        | R/W          |       |       |       |       |       |       |       |
|        |             |                        | 0            | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
|        |             |                        | 1: Start DMA |       |       |       |       |       |       |       |

(3) Transfer control registers

The transfer source address and the transfer destination address are set in the following registers. An instruction of the form LDC cr,r can be used to set these registers.



## (4) Detailed description of the transfer mode register



| DMAMn[4:0] | Mode Description                                                                                                                | Execution Time |
|------------|---------------------------------------------------------------------------------------------------------------------------------|----------------|
| 0 0 0 z z  | Destination INC mode<br>(DMADn +) $\leftarrow$ (DMASn)<br>DMACn $\leftarrow$ DMACn - 1<br>If DMACn = 0 then INTTCn              | 5 states       |
| 0 0 1 z z  | Destination DEC mode<br>(DMADn -) $\leftarrow$ (DMASn)<br>DMACn $\leftarrow$ DMACn - 1<br>If DMACn = 0 then INTTCn              | 5 states       |
| 0 1 0 z z  | Source INC mode<br>(DMADn) $\leftarrow$ (DMASn +)<br>DMACn $\leftarrow$ DMACn - 1<br>If DMACn = 0 then INTTCn                   | 5 states       |
| 0 1 1 z z  | Source DEC mode<br>(DMADn) $\leftarrow$ (DMASn -)<br>DMACn $\leftarrow$ DMACn - 1<br>If DMACn = 0 then INTTCn                   | 5 states       |
| 1 0 0 z z  | Source and destination INC mode<br>(DMADn +) $\leftarrow$ (DMASn +)<br>DMACn $\leftarrow$ DMACn - 1<br>If DMACn = 0 then INTTCn | 6 states       |
| 1 0 1 z z  | Source and destination DEC mode<br>(DMADn -) $\leftarrow$ (DMASn -)<br>DMACn $\leftarrow$ DMACn - 1<br>If DMACn = 0 then INTTCn | 6 states       |
| 1 1 0 z z  | Destination and fixed mode<br>(DMADn) $\leftarrow$ (DMASn)<br>DMACn $\leftarrow$ DMACn - 1<br>If DMACn = 0 then INTTCn          | 5 states       |
| 1 1 1 0 0  | Counter mode<br>DMASn $\leftarrow$ DMASn + 1<br>DMACn $\leftarrow$ DMACn - 1<br>If DMACn = 0 then INTTCn                        | 5 states       |

ZZ:

- 00 = 1-byte transfer
- 01 = 2-byte transfer
- 10 = 4-byte transfer
- 11 = Reserved

Note 1: n stands for the micro DMA channel number (0 to 7).

DMADn+/DMASn+: Post increment (Register value is incremented after transfer).

DMADn-/DMASn-: Post decrement (Register value is decremented after transfer).

"I/O" signifies fixed memory addresses; "memory" signifies incremented or decremented memory addresses.

Note 2: The transfer mode register should not be set to any value other than those listed above.

Note 3: The execution state number shows number of best case (1-state memory access).

### 3.5.3 Interrupt Controller Operation

The block diagram in Figure 3.5.3 shows the interrupt circuits. The left-hand side of the diagram shows the interrupt controller circuit. The right-hand side shows the CPU interrupt request signal circuit and the halt release circuit.

For each of the 59 interrupts channels there is an interrupt request flag (consisting of a flip-flop), an interrupt priority setting register and a micro DMA /HDMA start vector register. The interrupt request flag latches interrupt requests from the peripherals.

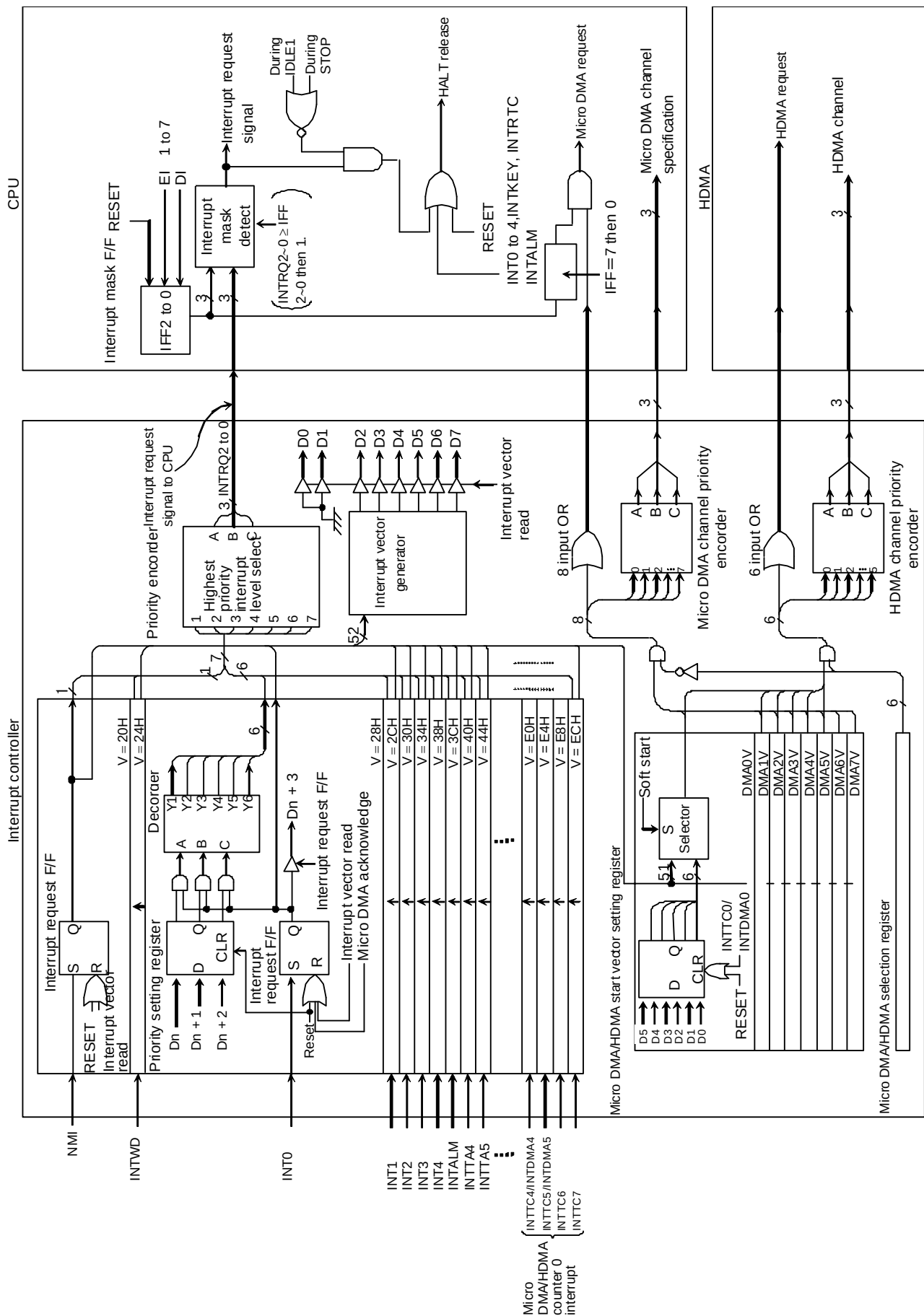
The flag is cleared to “0” in the following cases: when a reset occurs, when the CPU reads the channel vector of an interrupt it has received, when the CPU receives a micro DMA request (when micro DMA is set), when the CPU receives a HDMA request (when HDMA is set), when a micro DMA burst transfer is terminated, and when an instruction that clears the interrupt for that channel is executed (by writing a micro DMA start vector to the INTCLR register).

An interrupt priority can be set independently for each interrupt source by writing the priority to the interrupt priority setting register (e.g., INTE0 or INTE12). Six interrupt priorities levels (1 to 6) are provided. Setting an interrupt source's priority level to 0 (or 7) disables interrupt requests from that source.

If more than one interrupt request with a given priority level are generated simultaneously, the default priority (The interrupt with the lowest priority or, in other words, the interrupt with the lowest vector value) is used to determine which interrupt request is accepted first. The 3rd and 7th bits of the interrupt priority setting register indicate the state of the interrupt request flag and thus whether an interrupt request for a given channel has occurred.

If several interrupts are generated simultaneously, the interrupt controller sends the interrupt request for the interrupt with the highest priority and the interrupt's vector address to the CPU. The CPU compares the mask value set in <IFF2:0> of the status register (SR) with the priority level of the requested interrupt; if the latter is higher, the interrupt is accepted. Then the CPU sets SR<IFF2:0> to the priority level of the accepted interrupt + 1. Hence, during processing of the accepted interrupt, new interrupt requests with a priority value equal to or higher than the value set in SR<IFF2:0> (e.g., interrupts with a priority higher than the interrupt being processed) will be accepted. When interrupt processing has been completed (e.g., after execution of a RETI instruction), the CPU restores to SR<IFF2:0> the priority value which was saved on the stack before the interrupt was generated.

The interrupt controller also includes eight registers which are used to store the micro DMA /HDMA start vector. Writing the start vector of the interrupt source for the micro DMA or /HDMA processing (See Table 3.5.1), enables the corresponding interrupt to be processed by micro DMA or HDMA processing. The values must be set in the micro DMA parameter registers (e.g., DMAS and DMAD) or HDMA parameter registers (e.g., HDMAS, and HDMAD) prior to micro DMA or HDMA processing.



## (1) Interrupt priority setting registers

| Symbol   | Name                   | Address | 7                 | 6      | 5      | 4      | 3              | 2      | 1      | 0      |
|----------|------------------------|---------|-------------------|--------|--------|--------|----------------|--------|--------|--------|
| INTE0    | INT0 enable            | F0H     | –                 |        |        |        | INT0           |        |        |        |
|          |                        |         | –                 | –      | –      | –      | I0C            | I0M2   | I0M1   | I0M0   |
|          |                        |         | –                 | –      |        |        | R              | R/W    |        |        |
|          |                        |         | Always write “0”. |        |        |        | 0              | 0      | 0      | 0      |
| INTE12   | INT1 & INT2 enable     | D0H     | INT2              |        |        |        | INT1           |        |        |        |
|          |                        |         | I2C               | I2M2   | I2M1   | I2M0   | I1C            | I1M2   | I1M1   | I1M0   |
|          |                        |         | R                 | R/W    |        |        | R              | R/W    |        |        |
|          |                        |         | 0                 | 0      | 0      | 0      | 0              | 0      | 0      | 0      |
| INTE34   | INT3 & INT4 enable     | D1H     | INT4              |        |        |        | INT3           |        |        |        |
|          |                        |         | I4C               | I4M2   | I4M1   | I4M0   | I3C            | I3M2   | I3M1   | I3M0   |
|          |                        |         | R                 | R/W    |        |        | R              | R/W    |        |        |
|          |                        |         | 0                 | 0      | 0      | 0      | 0              | 0      | 0      | 0      |
| INTE56   | INT5 & INT6 enable     | D2H     | INT6              |        |        |        | INT5           |        |        |        |
|          |                        |         | I6C               | I6M2   | I6M1   | I6M0   | I5C            | I5M2   | I5M1   | I5M0   |
|          |                        |         | R                 | R/W    |        |        | R              | R/W    |        |        |
|          |                        |         | 0                 | 0      | 0      | 0      | 0              | 0      | 0      | 0      |
| INTE7    | INT7 enable            | D3H     | –                 |        |        |        | INT7           |        |        |        |
|          |                        |         | –                 | –      | –      | –      | I7C            | I7M2   | I7M1   | I7M0   |
|          |                        |         | –                 | –      |        |        | R              | R/W    |        |        |
|          |                        |         | Always write “0”. |        |        |        | 0              | 0      | 0      | 0      |
| INTETA01 | INTTA0 & INTTA1 enable | D4H     | INTTA1 (TMRA1)    |        |        |        | INTTA0 (TMRA0) |        |        |        |
|          |                        |         | ITA1C             | ITA1M2 | ITA1M1 | ITA1M0 | ITA0C          | ITA0M2 | ITA0M1 | ITA0M0 |
|          |                        |         | R                 | R/W    |        |        | R              | R/W    |        |        |
|          |                        |         | 0                 | 0      | 0      | 0      | 0              | 0      | 0      | 0      |
| INTETA23 | INTTA2 & INTTA3 enable | D5H     | INTTA3 (TMRA3)    |        |        |        | INTTA2 (TMRA2) |        |        |        |
|          |                        |         | ITA3C             | ITA3M2 | ITA3M1 | ITA3M0 | ITA2C          | ITA2M2 | ITA2M1 | ITA2M0 |
|          |                        |         | R                 | R/W    |        |        | R              | R/W    |        |        |
|          |                        |         | 0                 | 0      | 0      | 0      | 0              | 0      | 0      | 0      |
| INTETA45 | INTTA4 & INTTA5 enable | D6H     | INTTA5 (TMRA5)    |        |        |        | INTTA4 (TMRA4) |        |        |        |
|          |                        |         | ITA5C             | ITA5M2 | ITA5M1 | ITA5M0 | ITA4C          | ITA4M2 | ITA4M1 | ITA4M0 |
|          |                        |         | R                 | R/W    |        |        | R              | R/W    |        |        |
|          |                        |         | 0                 | 0      | 0      | 0      | 0              | 0      | 0      | 0      |
| INTETA67 | INTTA6 & INTTA7 enable | D7H     | INTTA7 (TMRA7)    |        |        |        | INTTA6 (TMRA6) |        |        |        |
|          |                        |         | ITA7C             | ITA7M2 | ITA7M1 | ITA7M0 | ITA6C          | ITA6M2 | ITA6M1 | ITA6M0 |
|          |                        |         | R                 | R/W    |        |        | R              | R/W    |        |        |
|          |                        |         | 0                 | 0      | 0      | 0      | 0              | 0      | 0      | 0      |

Interrupt request flag

| lxxM2 | lxxM1 | lxxM0 | Function (Write)                   |
|-------|-------|-------|------------------------------------|
| 0     | 0     | 0     | Disables interrupt requests        |
| 0     | 0     | 1     | Sets interrupt priority level to 1 |
| 0     | 1     | 0     | Sets interrupt priority level to 2 |
| 0     | 1     | 1     | Sets interrupt priority level to 3 |
| 1     | 0     | 0     | Sets interrupt priority level to 4 |
| 1     | 0     | 1     | Sets interrupt priority level to 5 |
| 1     | 1     | 0     | Sets interrupt priority level to 6 |
| 1     | 1     | 1     | Disables interrupt requests        |

| Symbol     | Name                     | Address | 7                 | 6       | 5       | 4       | 3               | 2       | 1       | 0       |
|------------|--------------------------|---------|-------------------|---------|---------|---------|-----------------|---------|---------|---------|
| INTETB0    | INTTB00 & INTTB01 enable | D8H     | INTTB01 (TMRB0)   |         |         |         | INTTB00 (TMRB0) |         |         |         |
|            |                          |         | ITB01C            | ITB01M2 | ITB01M1 | ITB01M0 | ITB00C          | ITB00M2 | ITB00M1 | ITB00M0 |
|            |                          |         | R                 | R/W     |         |         | R               | R/W     |         |         |
|            |                          |         | 0                 | 0       | 0       | 0       | 0               | 0       | 0       | 0       |
| INTETB1    | INTTB10 & INTTB11 enable | D9H     | INTTB11 (TMRB1)   |         |         |         | INTTB10 (TMRB1) |         |         |         |
|            |                          |         | ITB11C            | ITB11M2 | ITB11M1 | ITB11M0 | ITB10C          | ITB10M2 | ITB10M1 | ITB10M0 |
|            |                          |         | R                 | R/W     |         |         | R               | R/W     |         |         |
|            |                          |         | 0                 | 0       | 0       | 0       | 0               | 0       | 0       | 0       |
| INTES0     | INTRX0 & INTTX0 enable   | DBH     | INTTX0            |         |         |         | INTRX0          |         |         |         |
|            |                          |         | ITX0C             | ITX0M2  | ITX0M1  | ITX0M0  | IRX0C           | IRX0M2  | IRX0M1  | IRX0M0  |
|            |                          |         | R                 | R/W     |         |         | R               | R/W     |         |         |
|            |                          |         | 0                 | 0       | 0       | 0       | 0               | 0       | 0       | 0       |
| INTES1     | INTRX1 & INTTX1 enable   | DCH     | INTTX1            |         |         |         | INTRX1          |         |         |         |
|            |                          |         | ITX1C             | ITX1M2  | ITX1M1  | ITX1M0  | IRX1C           | IRX1M2  | IRX1M1  | IRX1M0  |
|            |                          |         | R                 | R/W     |         |         | R               | R/W     |         |         |
|            |                          |         | 0                 | 0       | 0       | 0       | 0               | 0       | 0       | 0       |
| INTESBIADM | INTSBI & INTADM enable   | E0H     | INTADM            |         |         |         | INTSBI          |         |         |         |
|            |                          |         | IADM0C            | IADMM2  | IADMM1  | IADMM0  | ISBI0C          | ISBIM2  | ISBIM1  | ISBIM0  |
|            |                          |         | R                 | R/W     |         |         | R               | R/W     |         |         |
|            |                          |         | 0                 | 0       | 0       | 0       | 0               | 0       | 0       | 0       |
| INTESPI    | INTSPI enable            | E1H     | INTSPITX          |         |         |         | INTSPIRX        |         |         |         |
|            |                          |         | ISPITC            | ISPITM2 | ISPITM1 | ISPITM0 | ISPIRC          | ISPIRM2 | ISPIRM1 | ISPIRM0 |
|            |                          |         | R                 | R/W     |         |         | R               | R/W     |         |         |
|            |                          |         | 0                 | 0       | 0       | 0       | 0               | 0       | 0       | 0       |
| INTEUSB    | INTUSB enable            | E3H     | –                 |         |         |         | INTUSB          |         |         |         |
|            |                          |         | –                 | –       | –       | –       | IUSBC           | IUSBM2  | IUSBM1  | IUSBM0  |
|            |                          |         | –                 | –       |         |         | R               | R/W     |         |         |
|            |                          |         | Always write “0”. |         |         |         | 0               | 0       | 0       | 0       |
| INTEALM    | INTALM enable            | E5H     | –                 |         |         |         | INTALM          |         |         |         |
|            |                          |         | –                 | –       | –       | –       | IALMC           | IALMM2  | IALMM1  | IALMM0  |
|            |                          |         | –                 | –       |         |         | R               | R/W     |         |         |
|            |                          |         | Always write “0”. |         |         |         | 0               | 0       | 0       | 0       |
| INTERTC    | INTRTC enable            | E8H     | –                 |         |         |         | INTRTC          |         |         |         |
|            |                          |         | –                 | –       | –       | –       | IRC             | IRM2    | IRM1    | IRM0    |
|            |                          |         | –                 | –       |         |         | R               | R/W     |         |         |
|            |                          |         | Always write “0”. |         |         |         | 0               | 0       | 0       | 0       |

Interrupt request flag

| lxxM2 | lxxM1 | lxxM0 | Function (Write)                   |
|-------|-------|-------|------------------------------------|
| 0     | 0     | 0     | Disables interrupt requests        |
| 0     | 0     | 1     | Sets interrupt priority level to 1 |
| 0     | 1     | 0     | Sets interrupt priority level to 2 |
| 0     | 1     | 1     | Sets interrupt priority level to 3 |
| 1     | 0     | 0     | Sets interrupt priority level to 4 |
| 1     | 0     | 1     | Sets interrupt priority level to 5 |
| 1     | 1     | 0     | Sets interrupt priority level to 6 |
| 1     | 1     | 1     | Disables interrupt requests        |

| Symbol   | Name                   | Address | 7                 | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
|----------|------------------------|---------|-------------------|---------|---------|---------|---------|---------|---------|---------|
| INTEKEY  | INTKEY enable          | E9H     | –                 |         |         |         | INTKEY  |         |         |         |
|          |                        |         | –                 | –       | –       | –       | IKC     | IKM2    | IKM1    | IKM0    |
|          |                        |         | –                 | –       |         |         | R       | R/W     |         |         |
|          |                        |         | Always write “0”. |         |         |         | 0       | 0       | 0       | 0       |
| INTEI2S0 | INTI2S0 enable         | EBH     | –                 |         |         |         | INTI2S0 |         |         |         |
|          |                        |         | –                 | –       | –       | –       | I I2S0C | II2S0M2 | II2S0M1 | II2S0M0 |
|          |                        |         | –                 | –       |         |         | R/W     | R/W     |         |         |
|          |                        |         | Always write “0”. |         |         |         | 0       | 0       | 0       | 0       |
| INTENDFC | INTRSC & INTRDY enable | ECH     | INTRSC            |         |         |         | INTRDY  |         |         |         |
|          |                        |         | IRSCC             | IRSCM2  | IRSCM1  | IRSCM0  | IRDYC   | IRDYM2  | IRDYM1  | IRDYM0  |
|          |                        |         | R                 | R/W     |         |         | R       | R/W     |         |         |
|          |                        |         | 0                 | 0       | 0       | 0       | 0       | 0       | 0       | 0       |
| INTEP0   | INTP0 enable           | EEH     | –                 |         |         |         | INTP0   |         |         |         |
|          |                        |         | –                 | –       | –       | –       | IPOC    | IP0M2   | IP0M1   | IP0M0   |
|          |                        |         | –                 | –       |         |         | R       | R/W     |         |         |
|          |                        |         | Always write “0”. |         |         |         | 0       | 0       | 0       |         |
| 0INTEAD  | INTAD & INTADHP enable | EFH     | INTADHP           |         |         |         | INTAD   |         |         |         |
|          |                        |         | IADHPC            | IADHPM2 | IADHPM1 | IADHPM0 | IADC    | IADM2   | IADM1   | IADM0   |
|          |                        |         | R                 | R/W     |         |         | R/W     | R/W     |         |         |
|          |                        |         | 0                 | 0       | 0       | 0       | 0       | 0       | 0       | 0       |

Interrupt request flag

| lxxM2 | lxxM1 | lxxM0 | Function (Write)                   |
|-------|-------|-------|------------------------------------|
| 0     | 0     | 0     | Disables interrupt requests        |
| 0     | 0     | 1     | Sets interrupt priority level to 1 |
| 0     | 1     | 0     | Sets interrupt priority level to 2 |
| 0     | 1     | 1     | Sets interrupt priority level to 3 |
| 1     | 0     | 0     | Sets interrupt priority level to 4 |
| 1     | 0     | 1     | Sets interrupt priority level to 5 |
| 1     | 1     | 0     | Sets interrupt priority level to 6 |
| 1     | 1     | 1     | Disables interrupt requests        |



| Symbol                | Name                                         | Address | 7                | 6                  | 5                  | 4                  | 3                | 2                  | 1                  | 0                  |
|-----------------------|----------------------------------------------|---------|------------------|--------------------|--------------------|--------------------|------------------|--------------------|--------------------|--------------------|
| INTETC01<br>/INTDMA01 | INTTC0/INTDMA0 &<br>INTTC1/INTDMA1<br>enable | F1H     | INTTC1/INTDMA1   |                    |                    |                    | INTTC0/INTDMA0   |                    |                    |                    |
|                       |                                              |         | ITC1C<br>/IDMA1C | ITC1M2<br>/IDMA1M2 | ITC1M1<br>/IDMA1M1 | ITC1M0<br>/IDMA1M0 | ITC0C<br>/IDMA0C | ITC0M2<br>/IDMA0M2 | ITC0M1<br>/IDMA0M1 | ITC0M0<br>/IDMA0M0 |
|                       |                                              |         | R                | R/W                |                    |                    | R                | R/W                |                    |                    |
|                       |                                              |         | 0                | 0                  | 0                  | 0                  | 0                | 0                  | 0                  | 0                  |
| INTETC23<br>/INTDMA23 | INTTC2/INTDMA2 &<br>INTTC3/INTDMA3<br>enable | F2H     | INTTC3/INTDMA3   |                    |                    |                    | INTTC2/INTDMA2   |                    |                    |                    |
|                       |                                              |         | ITC3C<br>/IDMA3C | ITC3M2<br>/IDMA3M2 | ITC3M1<br>/IDMA3M1 | ITC3M0<br>/IDMA3M0 | ITC2C<br>/IDMA2C | ITC2M2<br>/IDMA2M2 | ITC2M1<br>/IDMA2M1 | ITC2M0<br>/IDMA2M0 |
|                       |                                              |         | R                | R/W                |                    |                    | R                | R/W                |                    |                    |
|                       |                                              |         | 0                | 0                  | 0                  | 0                  | 0                | 0                  | 0                  | 0                  |
| INTETC45<br>/INTDMA45 | INTTC4/INTDMA4 &<br>INTTC5/INTDMA5<br>enable | F3H     | INTTC5/INTDMA5   |                    |                    |                    | INTTC4/INTDMA4   |                    |                    |                    |
|                       |                                              |         | ITC5C<br>/IDMA5C | ITC5M2<br>/IDMA5M2 | ITC5M1<br>/IDMA5M1 | ITC5M0<br>/IDMA5M0 | ITC4C<br>/IDMA4C | ITC4M2<br>/IDMA4M2 | ITC4M1<br>/IDMA4M1 | ITC4M0<br>/IDMA4M0 |
|                       |                                              |         | R                | R/W                |                    |                    | R                | R/W                |                    |                    |
|                       |                                              |         | 0                | 0                  | 0                  | 0                  | 0                | 0                  | 0                  | 0                  |
| INTETC67              | INTTC6 & INTTC7<br>enable                    | F4H     | INTTC7 (DMA7)    |                    |                    |                    | INTTC6 (DMA6)    |                    |                    |                    |
|                       |                                              |         | ITC7C            | ITC7M2             | ITC7M1             | ITC7M0             | ITC6C            | ITC6M2             | ITC6M1             | ITC6M0             |
|                       |                                              |         | R                | R/W                |                    |                    | R                | R/W                |                    |                    |
|                       |                                              |         | 0                | 0                  | 0                  | 0                  | 0                | 0                  | 0                  | 0                  |
| INTWDT/NMI            | INTWD & NMI<br>Flag<br>enable                | F7H     | NMI              |                    |                    |                    | INTWD            |                    |                    |                    |
|                       |                                              |         | ITCNMI           | –                  | –                  | –                  | ITCWD            | –                  | –                  | –                  |
|                       |                                              |         | R                | –                  |                    |                    | R                | –                  |                    |                    |
|                       |                                              |         | 0                | –                  | –                  | –                  | 0                | –                  | –                  | –                  |

Interrupt request flag

| lxxM2 | lxxM1 | lxxM0 | Function (Write)                   |
|-------|-------|-------|------------------------------------|
| 0     | 0     | 0     | Disables interrupt requests        |
| 0     | 0     | 1     | Sets interrupt priority level to 1 |
| 0     | 1     | 0     | Sets interrupt priority level to 2 |
| 0     | 1     | 1     | Sets interrupt priority level to 3 |
| 1     | 0     | 0     | Sets interrupt priority level to 4 |
| 1     | 0     | 1     | Sets interrupt priority level to 5 |
| 1     | 1     | 0     | Sets interrupt priority level to 6 |
| 1     | 1     | 1     | Disables interrupt requests        |

## (2) External interrupt control

| Symbol | Name                           | Address               | 7                                   | 6                                   | 5                                   | 4                                   | 3                                   | 2                                   | 1                                     | 0                                                           |
|--------|--------------------------------|-----------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|---------------------------------------|-------------------------------------------------------------|
| IIMC0  | Interrupt input mode control 0 | F6H<br>(Prohibit RMW) | I5EDGE                              | I4EDGE                              | I3EDGE                              | I2EDGE                              | I1EDGE                              | I0EDGE                              | I0LE                                  | NMIREE                                                      |
|        |                                |                       | W                                   |                                     |                                     |                                     |                                     |                                     | R/W                                   | R/W                                                         |
|        |                                |                       | 0                                   | 0                                   | 0                                   | 0                                   | 0                                   | 0                                   | 0                                     | 0                                                           |
|        |                                |                       | INT5EDGE<br>0: Rising<br>1: Falling | INT4EDGE<br>0: Rising<br>1: Falling | INT3EDGE<br>0: Rising<br>1: Falling | INT2EDGE<br>0: Rising<br>1: Falling | INT1EDGE<br>0: Rising<br>1: Falling | INT0EDGE<br>0: Rising<br>1: Falling | INT0<br>0: Edge mode<br>1: Level mode | NMI EDGE<br>0: Falling<br>1: Both edge (Falling and Rising) |
| IIMC1  | Interrupt input mode control 1 | FAH<br>(Prohibit RMW) |                                     |                                     |                                     |                                     |                                     |                                     | I7EDGE                                | I6EDGE                                                      |
|        |                                |                       |                                     |                                     |                                     |                                     |                                     |                                     | W                                     |                                                             |
|        |                                |                       |                                     |                                     |                                     |                                     |                                     |                                     | 0                                     | 0                                                           |
|        |                                |                       |                                     |                                     |                                     |                                     |                                     |                                     | INT7EDGE<br>0: Rising<br>1: Falling   | INT6EDGE<br>0: Rising<br>1: Falling                         |

Note 1: Disable INT0 request before changing INT0 pin mode from level sense to edge sense. (change <I0LE> from "1" to "0")

DI

LD (IIMC0), XXXXXX0-B ; Switches from level to edge.

LD (INTCLR), 0AH ; Clears interrupt request flag.

NOP

; Wait EI execution

NOP

NOP

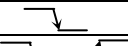
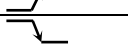
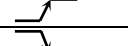
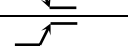
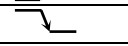
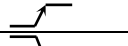
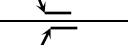
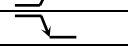
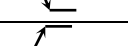
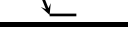
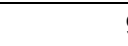
EI

X: Don't care, -: No change

Note 2: See electrical characteristics in section 4 for external interrupt input pulse width.

Note 3: In port setting, if 16 bit timer input is selected and capture control is executed, INT6 and INT7 don't depend on IIMC1 register setting. INT6 and INT7 operate by setting TBnMOD<TBnCPM1:0>.

## Settings of External Interrupt Pin Function

| Interrupt | Pin Name                | Mode                                                                                                     | Setting Method           |
|-----------|-------------------------|----------------------------------------------------------------------------------------------------------|--------------------------|
| NMI       | $\overline{\text{NMI}}$ |  Falling edge         | <NMIREE>= "0"            |
|           |                         |  Falling /Rising edge | <NMIREE>= "1"            |
| INT0      | PC0                     |  Rising edge          | <I0LE> = 0, <I0EDGE> = 0 |
|           |                         |  Falling edge         | <I0LE> = 0, <I0EDGE> = 1 |
|           |                         |  High level           | <I0LE> = 1               |
| INT1      | PC1                     |  Rising edge          | <I1EDGE> = 0             |
|           |                         |  Falling edge         | <I1EDGE> = 0             |
| INT2      | PC2                     |  Rising edge          | <I2EDGE> = 0             |
|           |                         |  Falling edge         | <I2EDGE> = 1             |
| INT3      | PC3                     |  Rising edge          | <I3EDGE> = 0             |
|           |                         |  Falling edge         | <I3EDGE> = 1             |
| INT4      | P96                     |  Rising edge          | <I4EDGE> = 0             |
|           |                         |  Falling edge         | <I4EDGE> = 1             |
| INT5      | PP3                     |  Rising edge          | <I5EDGE> = 0             |
|           |                         |  Falling edge         | <I5EDGE> = 1             |
| INT6      | PP4                     |  Rising edge          | <I6EDGE> = 0             |
|           |                         |  Falling edge         | <I6EDGE> = 1             |
| INT7      | PP5                     |  Rising edge          | <I7EDGE> = 0             |
|           |                         |  Falling edge         | <I7EDGE> = 1             |

(3) SIO receive interrupt control

| Symbol | Name                       | Address               | 7                          | 6                | 5 | 4 | 3 | 2 | 1                                               | 0                                               |
|--------|----------------------------|-----------------------|----------------------------|------------------|---|---|---|---|-------------------------------------------------|-------------------------------------------------|
| SIMC   | SIO interrupt mode control | F5H<br>(Prohibit RMW) | –                          | –                |   |   |   |   | IR1LE                                           | IR0LE                                           |
|        |                            |                       | W                          |                  |   |   |   |   | W                                               |                                                 |
|        |                            |                       | 0                          | 0                |   |   |   |   | 1                                               | 1                                               |
|        |                            |                       | Always write “0”<br>(Note) | Always write “0” |   |   |   |   | 0:INTRX1<br>edge mode<br>1:INTRX1<br>level mode | 0:INTRX0<br>edge mode<br>1:INTRX0<br>level mode |

Note: When using the micro DMA transfer end interrupt, always write “1”.

INTRX edge enable

|   |                   |
|---|-------------------|
| 0 | Edge detect INTRX |
| 1 | “H” level INTRX   |



## (4) Interrupt request flag clear register

The interrupt request flag is cleared by writing the appropriate micro DMA /HDMA start vector, as given in Table 3.5.1 to the register INTCLR.

For example, to clear the interrupt flag INT0, perform the following register operation after execution of the DI instruction.

INTCLR      ←      0AH                      ; Clears interrupt request flag INT0.

| Symbol | Name                    | Address               | 7                | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|--------|-------------------------|-----------------------|------------------|-------|-------|-------|-------|-------|-------|-------|
| INTCLR | Interrupt clear control | F8H<br>(Prohibit RMW) | CLRV7            | CLRV6 | CLRV5 | CLRV4 | CLRV3 | CLRV2 | CLRV1 | CLRV0 |
|        |                         |                       | W                |       |       |       |       |       |       |       |
|        |                         |                       | 0                | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
|        |                         |                       | Interrupt vector |       |       |       |       |       |       |       |

## (5) Micro DMA start vector registers

These registers assign micro DMA/HDMA processing to sets which source corresponds to DMA. The interrupt source whose micro DMA /HDMA start vector value matches the vector set in one of these registers is designated as the micro DMA /HDMA start source.

When the micro DMA transfer counter (DMACn) or HDMA transfer counter B (HDMACBn) value reaches “0”, the micro DMA /HDMA transfer end interrupt corresponding to the channel is sent to the interrupt controller, the micro DMA /HDMA start vector register is cleared, and the micro DMA /HDMA start source for the channel is cleared. Therefore, in order for micro DMA /HDMA processing to continue, the micro DMA /HDMA start vector register must be set again during processing of the micro DMA /HDMA transfer end interrupt.

If the same vector is set in the micro DMA /HDMA start vector registers of more than one channel, the lowest numbered channel takes priority.

Accordingly, if the same vector is set in the micro DMA /HDMA start vector registers for two different channels, the interrupt generated on the lower-numbered channel is executed until micro DMA /HDMA transfer is complete. If the micro DMA /HDMA start vector for this channel has not been set in the channel's micro DMA /HDMA start vector register again, micro DMA /HDMA transfer for the higher-numbered channel will be commenced. (This process is known as micro DMA /HDMA chaining.)

| Symbol | Name              | Address | 7 | 6 | 5                 | 4      | 3      | 2      | 1      | 0      |
|--------|-------------------|---------|---|---|-------------------|--------|--------|--------|--------|--------|
| DMA0V  | DMA0 start vector | 100H    |   |   | DMA0V5            | DMA0V4 | DMA0V3 | DMA0V2 | DMA0V1 | DMA0V0 |
|        |                   |         |   |   | R/W               |        |        |        |        |        |
|        |                   |         |   |   | 0                 | 0      | 0      | 0      | 0      | 0      |
|        |                   |         |   |   | DMA0 start vector |        |        |        |        |        |
| DMA1V  | DMA1 start vector | 101H    |   |   | DMA1V5            | DMA1V4 | DMA1V3 | DMA1V2 | DMA1V1 | DMA1V0 |
|        |                   |         |   |   | R/W               |        |        |        |        |        |
|        |                   |         |   |   | 0                 | 0      | 0      | 0      | 0      | 0      |
|        |                   |         |   |   | DMA1 start vector |        |        |        |        |        |
| DMA2V  | DMA2 start vector | 102H    |   |   | DMA2V5            | DMA2V4 | DMA2V3 | DMA2V2 | DMA2V1 | DMA2V0 |
|        |                   |         |   |   | R/W               |        |        |        |        |        |
|        |                   |         |   |   | 0                 | 0      | 0      | 0      | 0      | 0      |
|        |                   |         |   |   | DMA2 start vector |        |        |        |        |        |
| DMA3V  | DMA3 start vector | 103H    |   |   | DMA3V5            | DMA3V4 | DMA3V3 | DMA3V2 | DMA3V1 | DMA3V0 |
|        |                   |         |   |   | R/W               |        |        |        |        |        |
|        |                   |         |   |   | 0                 | 0      | 0      | 0      | 0      | 0      |
|        |                   |         |   |   | DMA3 start vector |        |        |        |        |        |
| DMA4V  | DMA4 start vector | 104H    |   |   | DMA4V5            | DMA4V4 | DMA4V3 | DMA4V2 | DMA4V1 | DMA4V0 |
|        |                   |         |   |   | R/W               |        |        |        |        |        |
|        |                   |         |   |   | 0                 | 0      | 0      | 0      | 0      | 0      |
|        |                   |         |   |   | DMA4 start vector |        |        |        |        |        |
| DMA5V  | DMA5 start vector | 105H    |   |   | DMA5V5            | DMA5V4 | DMA5V3 | DMA5V2 | DMA5V1 | DMA5V0 |
|        |                   |         |   |   | R/W               |        |        |        |        |        |
|        |                   |         |   |   | 0                 | 0      | 0      | 0      | 0      | 0      |
|        |                   |         |   |   | DMA5 start vector |        |        |        |        |        |
| DMA6V  | DMA6 start vector | 106H    |   |   | DMA6V5            | DMA6V4 | DMA6V3 | DMA6V2 | DMA6V1 | DMA6V0 |
|        |                   |         |   |   | R/W               |        |        |        |        |        |
|        |                   |         |   |   | 0                 | 0      | 0      | 0      | 0      | 0      |
|        |                   |         |   |   | DMA6 start vector |        |        |        |        |        |
| DMA7V  | DMA7 start vector | 107H    |   |   | DMA7V5            | DMA7V4 | DMA7V3 | DMA7V2 | DMA7V1 | DMA7V0 |
|        |                   |         |   |   | R/W               |        |        |        |        |        |
|        |                   |         |   |   | 0                 | 0      | 0      | 0      | 0      | 0      |
|        |                   |         |   |   | DMA7 start vector |        |        |        |        |        |

## (6) Micro DMA/HDMA select register

This register selectable that is started either Micro DMA or HDMA processing.

Micro DMA /HDMA start vector register (DMA<sub>n</sub>V) shared with both functions. When interrupt which match with vector value that is set to DMA/HDMA start vector register generated, use this register.

| Symbol | NAME                  | Address | 7 | 6 | 5                       | 4                       | 3                       | 2                       | 1                       | 0                       |
|--------|-----------------------|---------|---|---|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| DMASEL | Micro DMA/HDMA select | 10AH    |   |   | DMASEL5                 | DMASEL4                 | DMASEL3                 | DMASEL2                 | DMASEL1                 | DMASEL0                 |
|        |                       |         |   |   | R/W                     |                         |                         |                         |                         |                         |
|        |                       |         |   |   | 0                       | 0                       | 0                       | 0                       | 0                       | 0                       |
|        |                       |         |   |   | 0:Micro DMA5<br>1:HDMA5 | 0:Micro DMA4<br>1:HDMA4 | 0:Micro DMA3<br>1:HDMA3 | 0:Micro DMA2<br>1:HDMA2 | 0:Micro DMA1<br>1:HDMA1 | 0:Micro DMA0<br>1:HDMA0 |

## (7) Specification of a micro DMA burst

Specifying the micro DMA burst function causes micro DMA transfer, once started, to continue until the value in the transfer counter register reaches “0”. Setting any of the bits in the register DMAB which correspond to a micro DMA channel (as shown below) to “1” specifies that any micro DMA transfer on that channel will be a burst transfer.

| Symbol | Name      | Address | 7                            | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|--------|-----------|---------|------------------------------|-------|-------|-------|-------|-------|-------|-------|
| DMAB   | DMA burst | 108H    | DBST7                        | DBST6 | DBST5 | DBST4 | DBST3 | DBST2 | DBST1 | DBST0 |
|        |           |         | R/W                          |       |       |       |       |       |       |       |
|        |           |         | 0                            | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
|        |           |         | 1: DMA request on Burst mode |       |       |       |       |       |       |       |

## (8) Notes

The instruction execution unit and the bus interface unit in this CPU operate independently. Therefore, if immediately before an interrupt is generated, the CPU fetches an instruction which clears the corresponding interrupt request flag, the CPU may execute this instruction in between accepting the interrupt and reading the interrupt vector. In this case, the CPU will read the default vector 0004H and jump to interrupt vector address FFFF04H.

To avoid this, an instruction which clears an interrupt request flag should always be preceded by a DI instruction. And in the case of setting an interrupt enable again by EI instruction after the execution of clearing instruction, execute EI instruction after clearing and more than 3-instructions (e.g., "NOP" × 3 times). If placed EI instruction without waiting NOP instruction after execution of clearing instruction, interrupt will be enable before request flag is cleared.

In the case of changing the value of the interrupt mask register <IFF2:0> by execution of POP SR instruction, disable an interrupt by DI instruction before execution of POP SR instruction.

In addition, please note that the following two circuits are exceptional and demand special attention.

|                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| INT0 level mode | <p>In level mode INT0 is not an edge-triggered interrupt. Hence, in level mode the interrupt request flip-flop for INT0 does not function. The peripheral interrupt request passes through the S input of the flip-flop and becomes the Q output. If the interrupt input mode is changed from edge mode to level mode, the interrupt request flag is cleared automatically.</p> <p>If the CPU enters the interrupt response sequence as a result of INT0 going from 0 to 1, INT0 must then be held at 1 until the interrupt response sequence has been completed. If INT0 is set to level mode so as to release a halt state, INT0 must be held at 1 from the time INT0 changes from 0 to 1 until the halt state is released. (Hence, it is necessary to ensure that input noise is not interpreted as a 0, causing INT0 to revert to 0 before the halt state has been released.)</p> <p>When the mode changes from level mode to edge mode, interrupt request flags which were set in level mode will not be cleared. Interrupt request flags must be cleared using the following sequence.</p> <pre> DI LD (IIMC0), 00H    ; Switches from level to edge. LD (INTCLR), 0AH   ; Clears interrupt request flag. NOP                ; Wait EI execution NOP NOP EI </pre> |
| INTRX           | <p>In level mode (The register SIMC&lt;IRxLE&gt; set to "1"), the interrupt request flip-flop can only be cleared by a reset or by reading the serial channel receive buffer. It cannot be cleared by writing INTCLR register.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

Note: The following instructions or pin input state changes are equivalent to instructions which clear the interrupt request flag.

INT0: Instructions which switch to level mode after an interrupt request has been generated in edge mode.

The pin input changes from high to low after an interrupt request has been generated in level mode. ("H" → "L")

INTRX: Instructions which read the receive buffer.

### 3.6 DMAC (DMA Controller)

The TMP92CF30 incorporates a DMA controller (DMAC) having six channels. This DMAC can realize data transfer faster than the micro DMA function by the 900/H1 CPU.

The DMAC has the following features:

- 1) Six independent channels of DMA
- 2) Two types of transfer start requests

Hardware request (using an interrupt source connected with the INTC) or software request can be selected for each channel.
- 3) Various source/destination combinations

The combination of transfer source and destination can be selected for each channel from the following four types: memory to memory, memory to I/O, I/O to memory, I/O to I/O.
- 4) Transfer address mode

Only the dual address mode is supported.
- 5) Dual-count mechanism and DMA end interrupt

Two count registers are provided to execute multiple DMA transfers by one DMA request and to generate multiple DMA requests at a time. The DMA end interrupt (INTDMA0 to INTDMA5) is also provided so that a general-purpose interrupt routine can be used to prepare for the next processing.
- 6) Priorities among DMA channels (the same as the micro DMA acceptance specifications of the INTC)

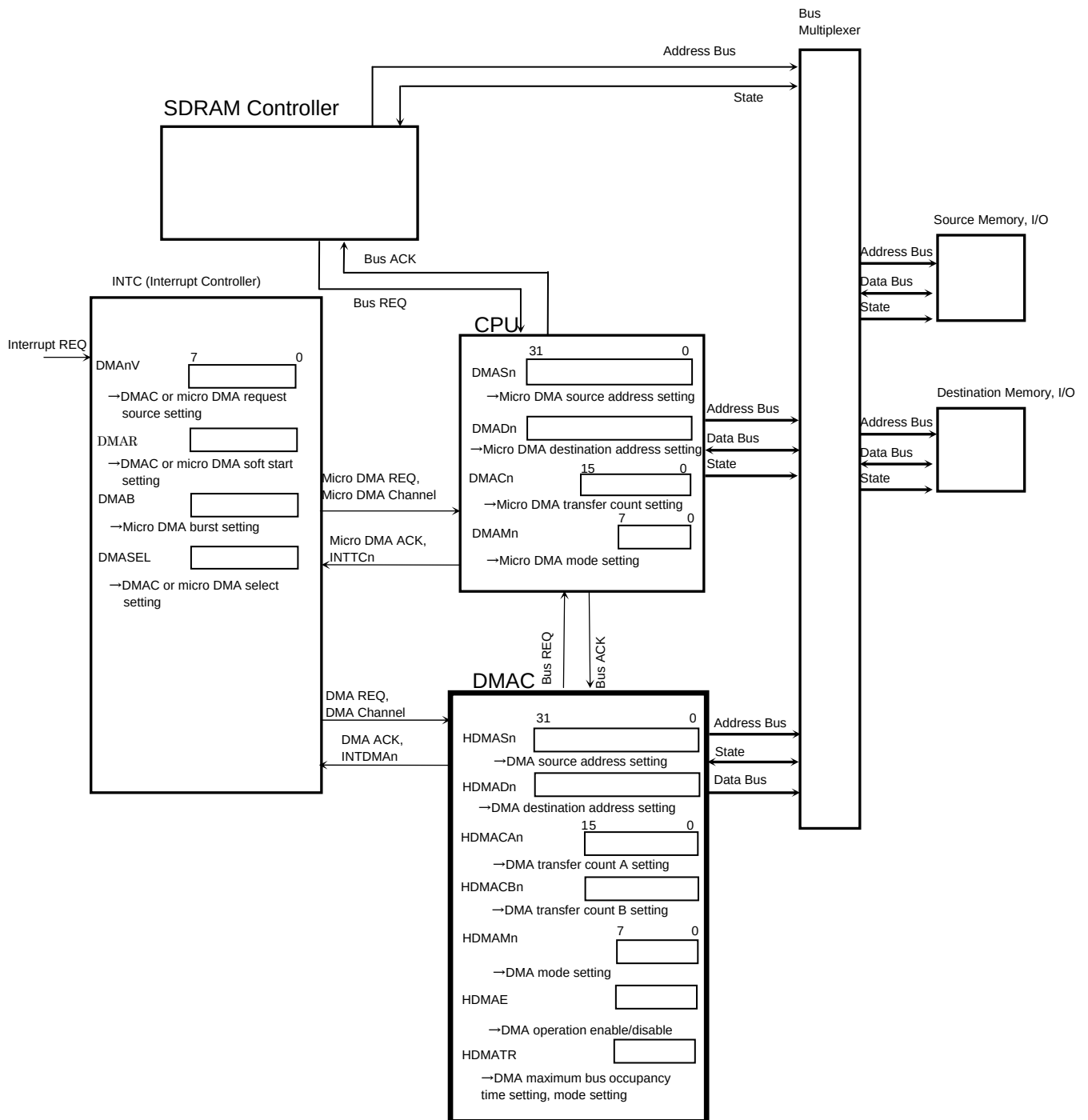
DMA requests are basically accepted in the order in which they are asserted. If more than one request is asserted simultaneously or it looks as if two requests were asserted simultaneously because one of the requests has been put on hold while other processing was being performed, the smaller-numbered channel is given a higher priority.
- 7) DMAC bus occupancy limiting function

The DMAC incorporates a special timer for limiting its bus occupancy time to avoid excessive interference with the CPU operation.
- 8) The DMAC can be used in HALT (IDLE2) mode.



## 3.6.1 Block Diagram

Figure 3.6.1 shows an overall block diagram for the DMAC.



Note: "n" denotes a channel number. Micro DMA has eight channels (0 to 7) and DMA has six channels (0 to 5).

Figure 3.6.1 Overall Block Diagram

## 3.6.2 SFRs

The DMAC has the following SFRs. These registers are connected to the CPU via a 16-bit data bus.

## (1) HDMASn (DMA Transfer Source Address Setting Register)

The HDMASn register is used to set the DMA transfer source address. When the source address is updated by DMA execution, HDMASn is also updated.

HDMAS0 to HDMAS5 have the same configuration.

Although the bus sizing function is supported, the address alignment function is not supported. Therefore, specify an even-numbered address for transferring 2 bytes and an address that is an integral multiple of 4 for transferring 4 bytes.

| HDMASn Register   |                                             |        |        |        |        |        |        |        |
|-------------------|---------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
|                   | 7                                           | 6      | 5      | 4      | 3      | 2      | 1      | 0      |
| HDMASn bit Symbol | DnSA7                                       | DnSA6  | DnSA5  | DnSA4  | DnSA3  | DnSA2  | DnSA1  | DnSA0  |
| Read/Write        | R/W                                         |        |        |        |        |        |        |        |
| Reset State       | 0                                           | 0      | 0      | 0      | 0      | 0      | 0      | 0      |
| Function          | Source address [7:0] for DMA <sub>n</sub>   |        |        |        |        |        |        |        |
|                   | 15                                          | 14     | 13     | 12     | 11     | 10     | 9      | 8      |
| HDMASn bit Symbol | DnSA15                                      | DnSA14 | DnSA13 | DnSA12 | DnSA11 | DnSA10 | DnSA9  | DnSA8  |
| Read/Write        | R/W                                         |        |        |        |        |        |        |        |
| Reset State       | 0                                           | 0      | 0      | 0      | 0      | 0      | 0      | 0      |
| Function          | Source address [15:8] for DMA <sub>n</sub>  |        |        |        |        |        |        |        |
|                   | 23                                          | 22     | 21     | 20     | 19     | 18     | 17     | 16     |
| HDMASn bit Symbol | DnSA23                                      | DnSA22 | DnSA21 | DnSA20 | DnSA19 | DnSA18 | DnSA17 | DnSA16 |
| Read/Write        | R/W                                         |        |        |        |        |        |        |        |
| Reset State       | 0                                           | 0      | 0      | 0      | 0      | 0      | 0      | 0      |
| Function          | Source address [23:16] for DMA <sub>n</sub> |        |        |        |        |        |        |        |

|           | Source address [23:16] | Source address [15:8] | Source address [7:0] |
|-----------|------------------------|-----------------------|----------------------|
| Channel 0 | (0902H)                | (0901H)               | HDMAS0 (0900H)       |
| Channel 1 | (0912H)                | (0911H)               | HDMAS1 (0910H)       |
| Channel 2 | (0922H)                | (0921H)               | HDMAS2 (0920H)       |
| Channel 3 | (0932H)                | (0931H)               | HDMAS3 (0930H)       |
| Channel 4 | (0942H)                | (0941H)               | HDMAS4 (0940H)       |
| Channel 5 | (0952H)                | (0951H)               | HDMAS5 (0950H)       |

Note: Read-modify-write instructions can be used on all these registers.

Figure3.6.2 HDMASn Register

## (2) HDMADn (DMA Transfer Destination Address Setting Register)

The HDMADn register is used to set the DMA transfer destination address. When the destination address is updated by DMA execution, HDMADn is also updated.

HDMAD0 to HDMAD5 have the same configuration.

Although the bus sizing function is supported, the address alignment function is not supported. Therefore, specify an even-numbered address for transferring 2 bytes and an address that is an integral multiple of 4 for transferring 4 bytes.

HDMADn Register

|        |             |                                      |        |        |        |        |        |        |        |
|--------|-------------|--------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| HDMADn | <div></div> | 7                                    | 6      | 5      | 4      | 3      | 2      | 1      | 0      |
|        | bit Symbol  | DnDA7                                | DnDA6  | DnDA5  | DnDA4  | DnDA3  | DnDA2  | DnDA1  | DnDA0  |
|        | Read/Write  | R/W                                  |        |        |        |        |        |        |        |
|        | Reset State | 0                                    | 0      | 0      | 0      | 0      | 0      | 0      | 0      |
|        | Function    | Destination address [7:0] for DMAn   |        |        |        |        |        |        |        |
|        | <div></div> | 15                                   | 14     | 13     | 12     | 11     | 10     | 9      | 8      |
|        | bit Symbol  | DnDA15                               | DnDA14 | DnDA13 | DnDA12 | DnDA11 | DnDA10 | DnDA9  | DnDA8  |
|        | Read/Write  | R/W                                  |        |        |        |        |        |        |        |
|        | Reset State | 0                                    | 0      | 0      | 0      | 0      | 0      | 0      | 0      |
|        | Function    | Destination address [15:8] for DMAn  |        |        |        |        |        |        |        |
|        | <div></div> | 23                                   | 22     | 21     | 20     | 19     | 18     | 17     | 16     |
|        | bit Symbol  | DnDA23                               | DnDA22 | DnDA21 | DnDA20 | DnDA19 | DnDA18 | DnDA17 | DnDA16 |
|        | Read/Write  | R/W                                  |        |        |        |        |        |        |        |
|        | Reset State | 0                                    | 0      | 0      | 0      | 0      | 0      | 0      | 0      |
|        | Function    | Destination address [23:16] for DMAn |        |        |        |        |        |        |        |

|           | Destination address<br>[23:16] | Destination address<br>[15:8] | Destination address<br>[7:0] |
|-----------|--------------------------------|-------------------------------|------------------------------|
| Channel 0 | (0906H)                        | (0905H)                       | HDMAD0<br>(0904H)            |
| Channel 1 | (0916H)                        | (0915H)                       | HDMAD1<br>(0914H)            |
| Channel 2 | (0926H)                        | (0925H)                       | HDMAD2<br>(0924H)            |
| Channel 3 | (0936H)                        | (0935H)                       | HDMAD3<br>(0934H)            |
| Channel 4 | (0946H)                        | (0945H)                       | HDMAD4<br>(0944H)            |
| Channel 5 | (0956H)                        | (0955H)                       | HDMAD5<br>(0954H)            |

Note: Read-modify-write instructions can be used on all these registers.

Figure3.6.3 HDMADn Register

## (3) HDMACAn (DMA Transfer Count A Setting Register)

The HDMACAn register is used to set the number of times a DMA transfer is to be performed by one DMA request. HDMACAn contains 16 bits and can specify up to 65536 transfers (0001H = one transfer, FFFFH = 65535 transfers, 0000H = 65536 transfers). Even when the transfer count A is updated by DMA execution, HDMACAn is not updated.

HDMACA0 to HDMACA5 have the same configuration.

HDMACAn Register

|         |             |                                  |        |        |        |        |        |       |       |
|---------|-------------|----------------------------------|--------|--------|--------|--------|--------|-------|-------|
| HDMACAn |             | 7                                | 6      | 5      | 4      | 3      | 2      | 1     | 0     |
|         | bit Symbol  | DnCA7                            | DnCA6  | DnCA5  | DnCA4  | DnCA3  | DnCA2  | DnCA1 | DnCA0 |
|         | Read/Write  | R/W                              |        |        |        |        |        |       |       |
|         | Reset State | 0                                | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|         | Function    | Transfer count A [7:0] for DMAn  |        |        |        |        |        |       |       |
|         |             | 15                               | 14     | 13     | 12     | 11     | 10     | 9     | 8     |
|         | bit Symbol  | DnCA15                           | DnCA14 | DnCA13 | DnCA12 | DnCA11 | DnCA10 | DnCA9 | DnCA8 |
|         | Read/Write  | R/W                              |        |        |        |        |        |       |       |
|         | Reset State | 0                                | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|         | Function    | Transfer count A [15:8] for DMAn |        |        |        |        |        |       |       |

|           |                            |                           |
|-----------|----------------------------|---------------------------|
|           | Transfer count A<br>[15:8] | Transfer count A<br>[7:0] |
| Channel 0 | (0909H)                    | HDMACA0<br>(0908H)        |
| Channel 1 | (0919H)                    | HDMACA1<br>(0918H)        |
| Channel 2 | (0929H)                    | HDMACA2<br>(0928H)        |
| Channel 3 | (0939H)                    | HDMACA3<br>(0938H)        |
| Channel 4 | (0949H)                    | HDMACA4<br>(0948H)        |
| Channel 5 | (0959H)                    | HDMACA5<br>(0958H)        |

Note: Read-modify-write instructions can be used on all these registers.

Figure3.6.4 HDMACAn Register

## (4) HDMACBn (DMA Transfer Count B Setting Register)

The HDMACBn register is used to set the number of times a DMA request is to be made. HDMACBn contains 16 bits and can specify up to 65536 requests (0001H = one request, FFFFH = 65535 requests, 0000H = 65536 requests). When the transfer count B is updated by DMA execution, HDMACBn is also updated.

HDMACB0 to HDMACB5 have the same configuration.

HDMACBn Register

|         |             |                                              |        |        |        |        |        |       |       |
|---------|-------------|----------------------------------------------|--------|--------|--------|--------|--------|-------|-------|
| HDMACBn |             | 7                                            | 6      | 5      | 4      | 3      | 2      | 1     | 0     |
|         | bit Symbol  | DnCB7                                        | DnCB6  | DnCB5  | DnCB4  | DnCB3  | DnCB2  | DnCB1 | DnCB0 |
|         | Read/Write  | R/W                                          |        |        |        |        |        |       |       |
|         | Reset State | 0                                            | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|         | Function    | Transfer count B [7:0] for DMA <sub>n</sub>  |        |        |        |        |        |       |       |
|         |             | 15                                           | 14     | 13     | 12     | 11     | 10     | 9     | 8     |
|         | bit Symbol  | DnCB15                                       | DnCB14 | DnCB13 | DnCB12 | DnCB11 | DnCB10 | DnCB9 | DnCB8 |
|         | Read/Write  | R/W                                          |        |        |        |        |        |       |       |
|         | Reset State | 0                                            | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|         | Function    | Transfer count B [15:8] for DMA <sub>n</sub> |        |        |        |        |        |       |       |

|           |                            |                           |
|-----------|----------------------------|---------------------------|
|           | Transfer count B<br>[15:8] | Transfer count B<br>[7:0] |
| Channel 0 | (090BH)                    | HDMACB0<br>(090AH)        |
| Channel 1 | (091BH)                    | HDMACB1<br>(091AH)        |
| Channel 2 | (092BH)                    | HDMACB2<br>(092AH)        |
| Channel 3 | (093BH)                    | HDMACB3<br>(093AH)        |
| Channel 4 | (094BH)                    | HDMACB4<br>(094AH)        |
| Channel 5 | (095BH)                    | HDMACB5<br>(095AH)        |

Note: Read-modify-write instructions can be used on all these registers.

Figure3.6.5 HDMACBn Register

## (5) HDMAMn (DMA Transfer Mode Setting Register)

The HDMAMn register is used to set the DMA transfer mode.

HDMAM0 to HDMAM5 have the same configuration.

| HDMAMn Register |             |   |   |                                           |      |      |                    |      |
|-----------------|-------------|---|---|-------------------------------------------|------|------|--------------------|------|
| HDMAMn          | 7           | 6 | 5 | 4                                         | 3    | 2    | 1                  | 0    |
|                 | bit Symbol  |   |   | DnM4                                      | DnM3 | DnM2 | DnM1               | DnM0 |
|                 | Read/Write  |   |   | R/W                                       |      |      |                    |      |
|                 | Reset State |   |   | 0                                         | 0    | 0    | 0                  | 0    |
| Function        |             |   |   | DMA transfer mode                         |      |      | Transfer data size |      |
|                 |             |   |   | 000: Destination INC (I/O → MEM)          |      |      | 00: 1 byte         |      |
|                 |             |   |   | 001: Destination DEC (I/O → MEM)          |      |      | 01: 2 bytes        |      |
|                 |             |   |   | 010: Source INC (MEM → I/O)               |      |      | 10: 4 bytes        |      |
|                 |             |   |   | 011: Source DEC (MEM → I/O)               |      |      | 11: Reserved       |      |
|                 |             |   |   | 100: Source/destination INC (MEM → MEM)   |      |      |                    |      |
|                 |             |   |   | 101: Source/destination DEC (MEM → MEM)   |      |      |                    |      |
|                 |             |   |   | 110: Source/destination fixed (I/O → I/O) |      |      |                    |      |
|                 |             |   |   | 111: Reserved                             |      |      | (Note 2)           |      |

|           | Transfer mode [7:0] |
|-----------|---------------------|
| Channel 0 | HDMAM0 (090CH)      |
| Channel 1 | HDMAM1 (091CH)      |
| Channel 2 | HDMAM2 (092CH)      |
| Channel 3 | HDMAM3 (093CH)      |
| Channel 4 | HDMAM4 (094CH)      |
| Channel 5 | HDMAM5 (095CH)      |

Note 1: Read-modify-write instructions can be used on all these registers.

Note 2: INC: Post-increment

Dec: Post-decrement

I/O: Fixed memory address

MEM: Memory address to be incremented or decremented

Figure3.6.6 HDMAMn Register

## (6) HDMAE (DMA Operation Enable Register)

The HDMAE register is used to enable or disable the DMAC operation.

Bits 0 to 5 correspond to channels 0 to 5. Unused channels should be set to "0".

| HDMAE Register   |             |   |                                                  |       |       |       |       |       |
|------------------|-------------|---|--------------------------------------------------|-------|-------|-------|-------|-------|
|                  | 7           | 6 | 5                                                | 4     | 3     | 2     | 1     | 0     |
| HDMAE<br>(097EH) | bit Symbol  |   | DMAE5                                            | DMAE4 | DMAE3 | DMAE2 | DMAE1 | DMAE0 |
|                  | Read/Write  |   | R/W                                              |       |       |       |       |       |
|                  | Reset State |   | 0                                                | 0     | 0     | 0     | 0     | 0     |
|                  | Function    |   | DMA channel operation<br>0: Disable<br>1: Enable |       |       |       |       |       |

Note: Read-modify-write instructions can be used on this register.

Figure3.6.7 HDMAE Register

## (7) HDMATR (DMA Maximum Bus Occupancy Time Setting Register)

The HDMATR register is used to set the maximum duration of time the DMAC can occupy the bus. The TMP92CF30 does not have priority levels for bus arbitration. Therefore, once the DMAC owns the bus, other masters must wait until the DMAC completes its transfer operation and releases the bus. This could lead to problems in the system. To avoid such a situation, the DMAC limits the duration of its bus occupancy by using this timer register. When the DMAC occupies the bus for the duration of time set in this register, it releases the bus even if the specified DMA operation has not been completed yet. After waiting for 16 states, the DMAC asserts a bus request again to execute the rest of the DMA operation.

The DMAC counts the bus occupancy time regardless of which channel is occupying the bus. To set the maximum bus occupancy time, ensure that the HDMAE register is set to "00H" and set HDMATR<DMATE> to "1" and <DMATR6:0> to the desired value.

Note: In case of using S/W start with HDMA, transmission start is to set to "1" DMAR register. However DMAR register can't be used to confirm flag of transmission end. DMAR register reset to "0" when HDMA release bus occupation once with HDMATR function.

| HDMATR Register   |             |                                            |                                                                                                                                                                                  |        |        |        |        |        |
|-------------------|-------------|--------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|--------|--------|--------|
|                   | 7           | 6                                          | 5                                                                                                                                                                                | 4      | 3      | 2      | 1      | 0      |
| HDMATR<br>(097FH) | bit Symbol  | DMATE                                      | DMATR6                                                                                                                                                                           | DMATR5 | DMATR4 | DMATR3 | DMATR2 | DMATR1 |
|                   | Read/Write  | R/W                                        |                                                                                                                                                                                  |        |        |        |        |        |
|                   | Reset State | 0                                          | 0                                                                                                                                                                                | 0      | 0      | 0      | 0      | 0      |
|                   | Function    | Timer operation<br>0: Disable<br>1: Enable | Maximum bus occupancy time setting<br>The value to be set in <DMATR6:0> should be obtained by<br>"maximum bus occupancy time / (256/f <sub>SYS</sub> )".<br>"00H" cannot be set. |        |        |        |        |        |

Note: Read-modify-write instructions can be used on this register.

Figure3.6.8 HDMATR Register

### 3.6.3 DMAC Operation Description

#### (1) Overall flowchart

Figure 3.6.9 shows a flowchart for DMAC operation when an interrupt (DMA) is requested.

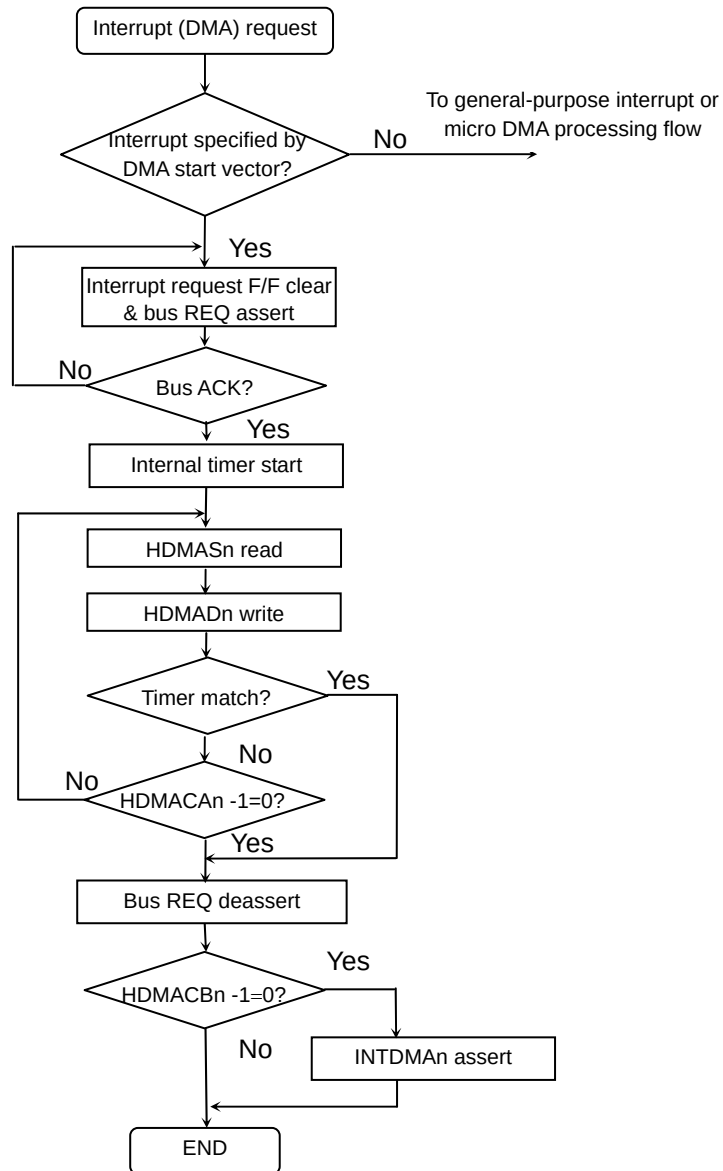


Figure 3.6.9 Overall Flowchart



## (2) Bus arbitration

The TMP92CF30 includes two controllers (DMA controller and SDRAM controller) that function as bus masters apart from the CPU. These controllers operate independently and assert a bus request as required. The controller that receives a bus acknowledgement acts as the bus master. No priorities are assigned to these two controllers, and bus requests are processed in the order in which they are asserted. Once one of the controllers owns the bus, bus requests from other controllers are put on hold until the bus is released again. While one of the controllers is occupying the bus, CPU processing including non-maskable interrupt requests is also put on hold.

## (3) Transfer source and destination memory setting

Either internal or external memory can be set as the source and destination memory or I/O to be accessed by the DMAC. Even when the MMU is used in external memory, the addresses to be accessed by the DMAC should be specified using logical addresses. The DMAC accesses the specified source and destination addresses according to the bus width and number of waits set in the memory controller and the bank settings made in the MMU.

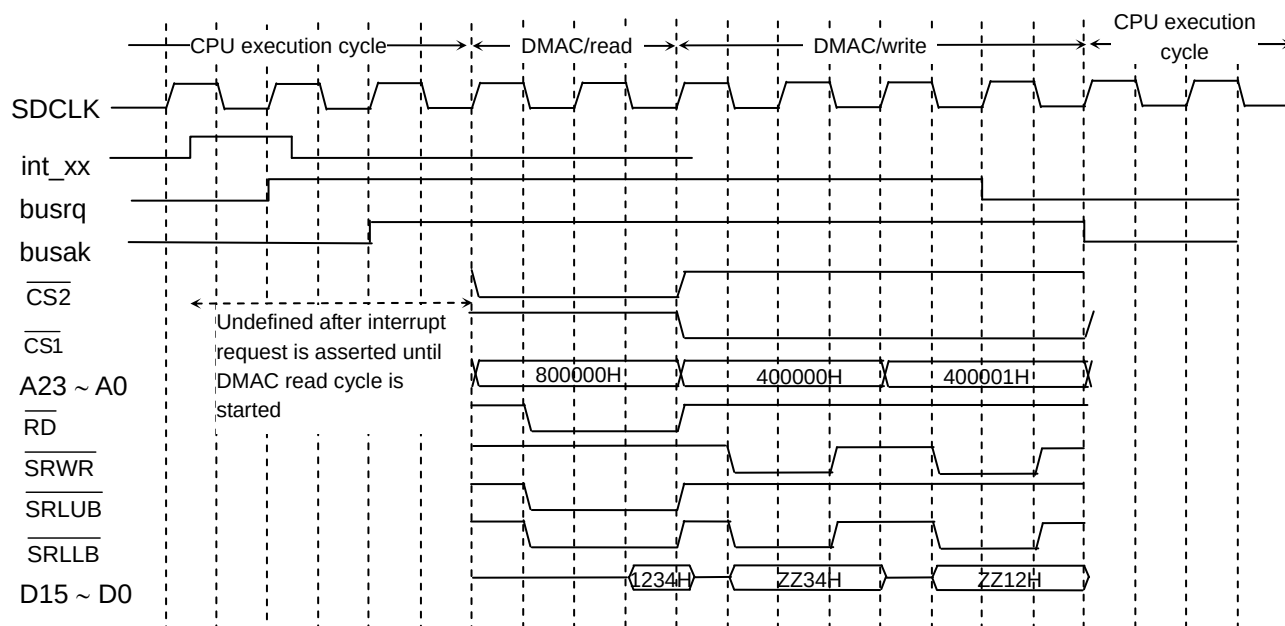
Although the bus sizing function is supported, the address alignment function is not supported. Therefore, specify an even-numbered address for transferring 2 bytes and an address that is an integral multiple of 4 for transferring 4 bytes.

Table 3.6.1 Difference point of address setting between HDMA and micro DMA

|                     | Data Length | HDMA                      | Micro DMA      |
|---------------------|-------------|---------------------------|----------------|
| Source address      | 1byte       | No restriction            | No restriction |
|                     | 2byte       | Even address              |                |
|                     | 4byte       | Address in multiples of 4 |                |
| Destination address | 1byte       | No restriction            |                |
|                     | 2byte       | Even address              |                |
|                     | 4byte       | Address in multiples of 4 |                |

## (4) Operation timing

The following diagram shows an example of operation timing for transferring 2 bytes from 16-bit memory connected with the  $\overline{\text{CS}}2$  area to 8-bit memory connected with the  $\overline{\text{CS}}1$  area.



### 3.6.4 Setting Example

This section explains how to set the DMAC using an example.

#### (1) Transferring music data from internal RAM to I<sup>2</sup>S by DMA transfer

The 32 Kbytes of data stored in the internal RAM at addresses 2000H to 9FFFH shall be transferred to FIFO-RAM via I<sup>2</sup>S. Each time an INTI2S request is asserted, 64 bytes (4 bytes x 16 times) shall be transferred to FIFO-RAM using DMAC channel 0. Since INTI2S is an FIFO empty interrupt, the first data must be set in advance. Therefore, only the first 64 bytes shall be transferred by DMA soft start. After 32 Kbytes have been transferred, the INTDMA0 interrupt routine shall be activated to prepare for the next processing.

##### (a) Main routine

| No | Instruction           | Comments                                         |
|----|-----------------------|--------------------------------------------------|
| 1  | ldl (hdmas0),2000H    | ; Source address = 2000H                         |
| 2  | ldl (hdmad0),i2sbuf   | ; Destination address = i2sbuf                   |
| 3  | ldw (hdmaca0),16      | ; Counter A = 16                                 |
| 4  | ldw (hdmacb0),512     | ; Counter B = 512 (32768/64)                     |
| 5  | ldb (hdmam0),0AH      | ; Transfer mode = source INC, 4 bytes            |
| 6  | set 0,(hdmae)         | ; Enable DMA channel 0.                          |
| 7  | ld (dmar),01H         | ; Transfer the first 64 bytes by DMA soft start. |
| 8  | nop                   | ;                                                |
| 9  | ld (dma0v),i2s_vector | ; INTI2S = DMA0                                  |
| 10 | ld (intdma01),xxH     | ; INTDMA level = x                               |
| 11 | ldw (i2sctl0),xxxxH   | ; Set operation mode for I <sup>2</sup> S.       |
| 12 | ldw (i2sctl1),xxxxH   | ; Start I <sup>2</sup> S transmission.           |
| 13 | ei xx                 | ; Enable CPU interrupts.                         |

##### (b) INTDMA0 interrupt routine

| No | Instruction   | Comments                 |
|----|---------------|--------------------------|
| 1  | res 0,(hdmae) | ; Disable DMA channel 0. |
| 2  | :             |                          |
| 3  | :             |                          |
| 4  | :             |                          |
| 5  | :             |                          |
| 6  |               |                          |
| 7  |               |                          |
| 8  |               |                          |
| 9  |               |                          |
| 10 |               |                          |
| 11 | reti          | ;                        |
|    |               |                          |

### 3.6.5 Note

In case of using S/W start with HDMA, transmission start is to set to “1” DMAR register. However DMAR register can't be used to confirm flag of transmission end. DMAR register reset to “0” when HDMA release bus occupation once with HDMATR function. We recommend to use HDMACBn register (counter value) to confirm flag of transmission end.

### 3.6.6 Considerations for Using More Than One Bus Master

In the TMP92CF30, the SDRAM controller and DMA controller may act as the bus master apart from the CPU. Therefore, care must be exercised to enable each of these functions to operate smoothly.

To facilitate explanation of DMA operation performed by each bus master, the DMA transfer operation performed by the DMA controller is defined as “HDMA” and the SDRAM auto refresh operation performed by the SDRAM controller as “ARDMA”.

The following explains various cases where two or more bus masters may operate at the same time.

#### (1) CPU + HDMA

The DMA controller performs DMA transfer (HDMA) after issuing a bus request to the CPU and getting a bus acknowledgement. The DMA controller may be active while the CPU is in HALT mode (IDLE2 mode only), in which case HDMA does not interfere with the CPU operation. However, if HDMA is started while the CPU is active, the CPU cannot execute instructions while HDMA is being performed.

Before activating the DMA controller, therefore, it is necessary to estimate the CPU stop time (defined as “t<sub>STOP</sub> (HDMA)”) based on the transfer time, transfer start interval, and number of channels to be used.

$$\text{CPU bus stop rate} = t_{\text{STOP}} (\text{HDMA})[\text{s}] / \text{HDMA start interval} [\text{s}]$$

$$\text{HDMA start interval} [\text{s}] = \text{HDMA start interrupt period} [\text{s}]$$

Note: The HDMA start interval depends on the period of the HDMA start interrupt source. However, it is also possible to start HDMA by software.

$$t_{\text{STOP}} (\text{HDMA}) [\text{s}] = (\text{Source read time} + \text{Destination write time}) \times \text{Transfer count} + \alpha$$

state/byte

| Memory Type<br>Read / Write | Internal RAM   | External SDRAM<br>16-bit bus                  | External SRAM<br>16-bit bus | External SRAM<br>8-bit bus |
|-----------------------------|----------------|-----------------------------------------------|-----------------------------|----------------------------|
| Read                        | 1 / 4 (Note 1) | Burst 1 / 2 (Note 2)<br>1 word 6 / 2 (Note 2) | 2 / 2 (Note 3)              | 2 / 1 (Note 3)             |
| Write                       | 1 / 4          | Burst 1 / 2 (Note 2)<br>1 word 3 / 2 (Note 2) | 2 / 2 (Note 3)              | 2 / 1 (Note 3)             |

Note 1: 2-1-1-1 access. Each consecutive address can be accessed in 1 state.

Note 2: The transfer speed varies depending on the combination of source and destination.

a) When the source or destination is internal RAM or internal I/O (SFR), burst access (6-1-1-1 access) is possible. Only consecutive addresses on the same page can be accessed in 1 state. Additional 4 states are needed at the end of each burst access.

b) When the source or destination is other than internal RAM or internal I/O, 1-word access is used.

Note 3: In the case of 0 waits

state/byte

| I/O Type<br>Read / Write | I <sup>2</sup> S | NANDF | USB   | SPI   |
|--------------------------|------------------|-------|-------|-------|
| Read                     | –                | 2 / 2 | 2 / 2 | 2 / 4 |
| Write                    | 2 / 4            | 2 / 2 | 2 / 2 | 2 / 4 |

## Sample 1: Calculation example for CPU + HDMA

## Conditions:

CPU operation speed ( $f_{\text{SYS}}$ ) : 60 MHz  
 I<sup>2</sup>S sampling frequency : 48 kHz (60 MHz/25/50 = 48 kHz)  
 I<sup>2</sup>S data transfer bit length : 16 bits  
 DMAC channel 0 used to transfer 5 Kbytes from internal RAM to I<sup>2</sup>S

## Calculation example:

DMAC source data read time:

Internal RAM data read time

= 1 state/4 bytes (However, the first 1 byte requires 2 states.)

DMAC destination write time:

I<sup>2</sup>S register write time = 2 states/4 bytes

## Transfer count

To transfer 5 Kbytes of data in 4-byte units, the transfer count is calculated as follows:

5 Kbytes/4 bytes = 1280 [times]

Since I<sup>2</sup>S generates an interrupt for every 64 bytes, the DMAC's counter A is set to 16 (64 bytes/4 bytes = 16 times) and counter B is set to 80.

Note: Since an interrupt is generated 80 times, the first read to internal RAM (which requires 1 additional state) occurs 80 times, requiring additional 80 states in total. In addition, from bus REQ to bus ACK, an overhead time of 2 states is also needed for each interrupt request, requiring additional 160 states in total.

$$t_{\text{STOP}}(\text{HDMA}) = (((1 + 2) \times 16) \times 80) + 80 + 160 / f_{\text{SYS}} [\text{s}] = 68 [\mu\text{s}]$$

$$\begin{aligned} \text{HDMA start interval} [\text{s}] &= 1 / \text{I}^2\text{S sampling frequency} [\text{Hz}] \times (64 / 16) \\ &= 83.33 [\text{ms}] \end{aligned}$$

$$\begin{aligned} \text{CPU bus stop rate} &= t_{\text{STOP}}(\text{HDMA}) [\text{s}] / \text{HDMA start interval} [\text{s}] \\ &= 68 [\mu\text{s}] / 83.33 [\text{ms}] = 0.08 [\%] \end{aligned}$$

### 3.7 Function of ports

The TMP92CF30 I/O port pins are shown in Table 3.7.1. In addition to functioning as general-purpose I/O ports, these pins are also used by the internal CPU and I/O functions. Table 3.7.2 lists the I/O registers and their specifications.

Table 3.7.1 Port Functions (1/2) (R: PD= with programmable pull-down resistor, U= with pull-up resistor)

| Port Name | Pin Name   | Number of Pins | I/O    | R  | I/O Setting | Pin Name for built-in function                           |
|-----------|------------|----------------|--------|----|-------------|----------------------------------------------------------|
| Port 1    | P10 to P17 | 8              | I/O    | –  | bit         | D8 to D15                                                |
| Port 4    | P40 to P47 | 8              | Output | –  | (Fixed)     | A0 to A7                                                 |
| Port 5    | P50 to P57 | 8              | Output | –  | (Fixed)     | A8 to A15                                                |
| Port 6    | P60 to P67 | 8              | I/O    | –  | bit         | A16 to A23                                               |
| Port 7    | P70        | 1              | Output | –  | (Fixed)     | $\overline{RD}$                                          |
|           | P71        | 1              | I/O    | –  | bit         | $\overline{WRL\overline{L}}$ , $\overline{NDRE}$         |
|           | P72        | 1              | I/O    | –  | bit         | $\overline{WRL\overline{U}}$ , $\overline{NDWE}$         |
|           | P73        | 1              | I/O    | –  | bit         | EA24                                                     |
|           | P74        | 1              | I/O    | –  | bit         | EA25                                                     |
|           | P75        | 1              | I/O    | –  | bit         | $R/\overline{W}$ , $\overline{NDR}/\overline{B}$         |
|           | P76        | 1              | I/O    | –  | bit         | $\overline{WAIT}$                                        |
| Port 8    | P80        | 1              | Output | –  | (Fixed)     | $\overline{CS0}$                                         |
|           | P81        | 1              | Output | –  | (Fixed)     | $\overline{CS1}$ , $\overline{SDCS}$                     |
|           | P82        | 1              | Output | –  | (Fixed)     | $\overline{CS2}$ , $\overline{CSZA}$ , $\overline{SDCS}$ |
|           | P83        | 1              | Output | –  | (Fixed)     | $\overline{CS3}$ , $\overline{CSXA}$                     |
|           | P86        | 1              | Output | –  | (Fixed)     | $\overline{CSZD}$ , $\overline{ND0CE}$                   |
|           | P87        | 1              | Output | –  | (Fixed)     | $\overline{CSXB}$ , $\overline{ND1CE}$                   |
| Port 9    | P90        | 1              | I/O    | –  | bit         | TXD0, TXD1                                               |
|           | P91        | 1              | I/O    | –  | bit         | RXD0, RXD1                                               |
|           | P92        | 1              | I/O    | –  | bit         | SCLK0, $\overline{CTS0}$ , SCLK1, $\overline{CTS1}$      |
|           | P96        | 1              | Input  | PD | (Fixed)     | INT4, PX                                                 |
|           | P97        | 1              | Input  | –  | (Fixed)     | PY                                                       |
| Port A    | PA0 to PA7 | 8              | Input  | U  | (Fixed)     | KI0 to KI7                                               |
| Port C    | PC0        | 1              | I/O    | –  | bit         | INT0                                                     |
|           | PC1        | 1              | I/O    | –  | bit         | INT1, TA0IN                                              |
|           | PC2        | 1              | I/O    | –  | bit         | INT2                                                     |
|           | PC3        | 1              | I/O    | –  | bit         | INT3, TA2IN                                              |
|           | PC4        | 1              | I/O    | –  | bit         | EA26                                                     |
|           | PC5        | 1              | I/O    | –  | bit         | EA27                                                     |
|           | PC6        | 1              | I/O    | –  | bit         | EA28                                                     |
|           | PC7        | 1              | I/O    | –  | bit         | KO8                                                      |
| Port F    | PF0        | 1              | I/O    | –  | bit         | I2S0CKO                                                  |
|           | PF1        | 1              | I/O    | –  | bit         | I2S0DO                                                   |
|           | PF2        | 1              | I/O    | –  | bit         | I2S0WS                                                   |
|           | PF7        | 1              | Output | –  | (Fixed)     | SDCLK                                                    |
| Port G    | PG0 to PG1 | 2              | Input  | –  | (Fixed)     | AN0 to AN1                                               |
|           | PG2        | 1              | Input  | –  | (Fixed)     | AN2, MX                                                  |
|           | PG3        | 1              | Input  | –  | (Fixed)     | AN3, ADTRG, MY                                           |
|           | PG4 to PG5 | 2              | Input  | –  | (Fixed)     | AN4 to AN5                                               |

Table 3.7.1 Port Functions (2/2)

| Port Name | Pin Name   | Number of Pins | I/O    | R | I/O Setting | Pin Name for built-in function                                                                     |
|-----------|------------|----------------|--------|---|-------------|----------------------------------------------------------------------------------------------------|
| Port J    | PJ0        | 1              | Output | – | (Fixed)     | $\overline{\text{SDRAS}}$ , $\text{SRLLB}$                                                         |
|           | PJ1        | 1              | Output | – | (Fixed)     | $\overline{\text{SDCAS}}$ , $\text{SRLUB}$                                                         |
|           | PJ2        | 1              | Output | – | (Fixed)     | $\overline{\text{SDWE}}$ , $\overline{\text{SRWR}}$                                                |
|           | PJ3        | 1              | Output | – | (Fixed)     | $\text{SDLLDQM}$                                                                                   |
|           | PJ4        | 1              | Output | – | (Fixed)     | $\text{SDLUDQM}$                                                                                   |
|           | PJ5        | 1              | I/O    | – | bit         | $\text{NDALE}$ , $\overline{\text{SRULB}}$                                                         |
|           | PJ6        | 1              | I/O    | – | bit         | $\text{NDCLE}$ , $\overline{\text{SRUUB}}$                                                         |
|           | PJ7        | 1              | Output | – | (Fixed)     | $\text{SDCKE}$                                                                                     |
| Port K    | PK0-PK7    | 8              | Output | – | (Fixed)     | –                                                                                                  |
| Port L    | PL0 to PL7 | 8              | I/O    | – | bit         | D16 to D23                                                                                         |
| Port M    | PM1        | 1              | Output | – | (Fixed)     | $\text{MLDALM}$ , $\text{TA1OUT}$                                                                  |
|           | PM2        | 1              | Output | – | (Fixed)     | $\overline{\text{ALARM}}$ , $\overline{\text{MLDALM}}$                                             |
|           | PM7        | 1              | Output | – | (Fixed)     | –                                                                                                  |
| Port N    | PN0 to PN7 | 8              | I/O    | – | bit         | KO0 to KO7                                                                                         |
| Port P    | PP3        | 1              | I/O    | – | bit         | $\text{INT5}$ , $\text{TA7OUT}$ , $\text{TXD0}$ , $\text{TXD1}$                                    |
|           | PP4        | 1              | I/O    | – | bit         | $\text{INT6}$ , $\text{TB0IN0}$ , $\text{RXD0}$ , $\text{RXD1}$                                    |
|           | PP5        | 1              | I/O    | – | bit         | $\text{INT7}$ , $\text{TB1IN0}$ , $\text{SCLK0}$ , $\text{CTS0}$<br>$\text{SCLK1}$ , $\text{CTS1}$ |
|           | PP6        | 1              | Output | – | (Fixed)     | $\text{TB0OUT0}$                                                                                   |
| Port R    | PR0        | 1              | I/O    | – | bit         | $\text{SPDI}$                                                                                      |
|           | PR1        | 1              | I/O    | – | bit         | $\text{SPDO}$                                                                                      |
|           | PR2        | 1              | I/O    | – | bit         | $\overline{\text{SPCS}}$                                                                           |
|           | PR3        | 1              | I/O    | – | bit         | $\text{SPCLK}$                                                                                     |
| Port T    | PT0 to PT7 | 8              | I/O    | – | bit         | D24 to D31                                                                                         |
| Port V    | PV6        | 1              | I/O    | – | bit         | $\text{SDA}$                                                                                       |
|           | PV7        | 1              | I/O    | – | bit         | $\text{SCL}$                                                                                       |
| Port X    | PX4        | 1              | Output | – | (Fixed)     | $\text{CLKOUT}$                                                                                    |
|           | PX5        | 1              | I/O    | – | bit         | $\text{X1USB}$ , $\text{X1D4}$                                                                     |

Table 3.7.2 I/O Port and Specifications (1/5)

X: Don't care

| Port   | Pin name   | Specification             | I/O register |      |      |       |
|--------|------------|---------------------------|--------------|------|------|-------|
|        |            |                           | Pn           | PnCR | PnFC | PnFC2 |
| Port 1 | P10 to P17 | Input port                | X            | 0    | 0    | None  |
|        |            | Output port               | X            | 1    |      |       |
|        |            | D8 to D15 bus             | X            | X    |      |       |
| Port 4 | P40 to P47 | Output port               | X            | None | 0    | None  |
|        |            | A0 to A7 Output           | X            | None | 1    |       |
| Port 5 | P50 to P57 | Output port               | X            | None | 0    | None  |
|        |            | A8 to A15 Output          | X            | None | 1    |       |
| Port 6 | P60 to P67 | Input port                | X            | 0    | 0    | None  |
|        |            | Output port               | X            | 1    |      |       |
|        |            | A16 to A23 Output         | X            | X    |      |       |
| Port 7 | P70 to P76 | Output port               | X            | 1    | 0    | None  |
|        | P71 to P76 | Input port                | X            | 0    | 0    |       |
|        | P70        | $\overline{RD}$ Output    | X            | None | 1    |       |
|        | P71        | $\overline{WRLL}$ Output  | 1            | 1    | 1    |       |
|        |            | $\overline{NDRE}$ Output  | 0            |      |      |       |
|        | P72        | $\overline{WRLU}$ Output  | 1            | 1    | 1    |       |
|        |            | $\overline{NDWE}$ Output  | 0            |      |      |       |
|        | P73        | EA24 Output               | X            | 1    | 1    |       |
|        | P74        | EA25 Output               | X            | 1    | 1    |       |
|        | P75        | R/ $\overline{W}$ Output  | X            | 1    | 1    |       |
|        |            | NDR/B Input               | X            | 0    | 1    |       |
|        | P76        | $\overline{WAIT}$ Input   | X            | 0    | 1    |       |
| Port 8 | P80 to P87 | Output port               | X            | None | 0    | 0     |
|        | P80        | $\overline{CS0}$ Output   | X            |      | 1    | None  |
|        | P81        | $\overline{CS1}$ Output   | X            |      | 1    | 0     |
|        |            | $\overline{SDCS}$ Output  | X            |      | X    | 1     |
|        | P82        | $\overline{CS2}$ Output   | X            |      | 1    | 0     |
|        |            | $\overline{CSZA}$ Output  | X            |      | 0    | 1     |
|        |            | $\overline{SDCS}$ Output  | X            |      | 1    | 1     |
|        | P83        | $\overline{CS3}$ Output   | X            |      | 1    | 0     |
|        |            | $\overline{CSXA}$ Output  | X            |      | X    | 1     |
|        | P86        | $\overline{CSZD}$ Output  | X            |      | 1    | 0     |
|        |            | $\overline{ND0CE}$ Output | X            |      | 1    | 1     |
|        | P87        | $\overline{CSXB}$ Output  | X            |      | 1    | 0     |
|        |            | $\overline{ND1CE}$ Output | X            |      | 1    | 1     |



Table3.7.2 I/O Port and Specifications (2/5)

X: Don't care

| Port   | Pin name   | Specification                         | I/O register |      |      |            |
|--------|------------|---------------------------------------|--------------|------|------|------------|
|        |            |                                       | Pn           | PnCR | PnFC | PnFC2      |
| Port 9 | P90, P92   | Input port                            | X            | 0    | 0    | None       |
|        | P91        | Input port, RXD0 Input                | X            | 0    | None | None       |
|        | P96        | Input port                            | X            | None | 0    | None       |
|        | P97        | Input port                            | X            | None | None | None       |
|        | P90 to P92 | Output port                           | X            | 1    | 0    | 0          |
|        | P90        | TXD0 Output                           | X            | 1    | 1    | 0          |
|        |            | TXD0 Output (Open-drain)              | X            | 1    | 1    | 1          |
|        |            | TXD1 Output                           | X            | 1    | 1    | 0          |
|        |            | TXD1 Output (Open-drain)              | X            | 1    | 1    | 1          |
|        | P92        | SCLK0 Output                          | X            | 1    | 1    | <P95F2> =0 |
|        |            | SCLK0, $\overline{\text{CTS0}}$ Input | X            | 0    | 0    | 0          |
|        |            | SCLK1 Output                          | X            | 1    | 1    | <P95F2> =1 |
|        |            | SCLK1, $\overline{\text{CTS1}}$ Input | X            | 0    | 0    | 0          |
|        | P96        | INT4 Input                            | X            | None | 1    | None       |
| Port A | PA0 to PA7 | Input port                            | X            | None | 0    | None       |
|        |            | KI0 to KI7 Input                      | X            |      | 1    | None       |
| Port C | PC0 to PC3 | Input port                            | X            | 0    | 0    | None       |
|        | PC5 to PC7 | Output port                           | X            | 1    | 0    | None       |
|        | PC4        | Input port                            | X            | 0    | 0    | X          |
|        |            | Output port                           | X            | 1    | 0    | X          |
|        | PC0        | INT0 Input                            | X            | 0    | 1    | None       |
|        | PC1        | INT1 Input                            | X            | 0    | 1    | None       |
|        |            | TA0IN Input                           | X            | 1    | 1    | None       |
|        | PC2        | INT2 Input                            | X            | 0    | 1    | None       |
|        | PC3        | INT3 Input                            | X            | 0    | 1    | None       |
|        |            | TA2IN Input                           | X            | 1    | 1    | None       |
|        | PC4        | EA26 Output                           | X            | 0    | 1    | X          |
|        |            | (PC4) SPDI Input                      | X            | 1    | 1    | 1          |
|        |            | (PR0) SPDI Input                      | X            | 1    | 1    | 0          |
|        | PC5        | EA27 Output                           | X            | 0    | 1    | None       |
|        |            | SPDO Output                           | X            | 1    | 1    | None       |
|        | PC6        | EA28 Output                           | X            | 0    | 1    | None       |
|        |            | SPCLK Output                          | X            | 1    | 1    | None       |
|        | PC7        | KO8 Output (Open-drain)               | X            | 1    | 1    | None       |
| Port F | PF0 to PF2 | Input port                            | X            | 0    | 0    | None       |
|        | PF0 to PF2 | Output port                           | X            | 1    | 0    | None       |
|        | PF7        | Output port                           | X            | None | 0    |            |
|        | PF0        | I2S0CKO Output                        | X            | X    | 1    |            |
|        | PF1        | I2S0DO Output                         | X            | X    | 1    |            |
|        | PF2        | I2S0WS Output                         | X            | X    | 1    |            |
|        | PF7        | SDCLK Output                          | X            | None | 1    |            |

Table3.7.2 I/O Port and Specifications (3/5)

X: Don't care

| Port   | Pin name        | Specification                 | I/O register |      |      |       |
|--------|-----------------|-------------------------------|--------------|------|------|-------|
|        |                 |                               | Pn           | PnCR | PnFC | PnFC2 |
| Port G | PG0 to PG5      | Input port                    | X            | None | None | None  |
|        |                 | AN0 to AN5 Input              |              |      |      |       |
|        | PG3             | ADTRG Input                   |              |      | 1    |       |
|        | PG2             | MX Output Note:               |              |      | None |       |
|        | PG3             | MY Output Note:               |              |      |      |       |
| Port J | PJ5 to PJ6      | Input port                    | X            | 0    | 0    | None  |
|        | PJ5 to PJ6      | Output port                   | X            | 1    | 0    |       |
|        | PJ0 to PJ4, PJ7 | Output port                   | X            | None | 0    |       |
|        | PJ0             | SDRAS ,SRLLB Output           | X            | None | 1    |       |
|        | PJ1             | SDCAS ,SRLUB Output           | X            |      | 1    |       |
|        | PJ2             | SDWE ,SRWR Output             | X            |      | 1    |       |
|        | PJ3             | SDLLDQM Output                | X            |      | 1    |       |
|        | PJ4             | SDLUDQM Output                | X            |      | 1    |       |
|        | PJ5             | NDALE Output                  | X            | 1    | 1    |       |
|        | PJ5             | SRUUB output                  | X            | 0    | 1    |       |
|        | PJ6             | NDCLE Output                  | X            | 1    | 1    |       |
|        | PJ6             | SRULB output                  | X            | 0    | 1    |       |
|        | PJ7             | SDCKE Output                  | X            | None | 1    |       |
| Port K | PK0 to PK7      | Output port                   | X            | None | 0    | None  |
| Port L | PL0 to PL7      | Input port                    | X            | 0    | 0    | 0     |
|        |                 | Output port                   | X            | 1    | 0    | 0     |
|        |                 | D16 to D23                    | X            | X    | X    | 1     |
| Port M | PM1, PM2, PM7   | Output port                   | X            | None | 0    | None  |
|        | PM1             | TA1OUTOutput                  | 0            |      | 1    |       |
|        |                 | MLDALM Output                 | 1            |      | 1    |       |
|        | PM2             | MLDALM Output                 | 0            |      | 1    |       |
|        |                 | ALARM Output                  | 1            |      | 1    |       |
| Port N | PN0 to PN7      | Input port                    | X            | 0    | 0    | None  |
|        |                 | Output port (CMOS Output)     | X            | 1    | 0    |       |
|        |                 | KO Output (Open-drain Output) | X            |      | 1    |       |

Note: Case of using touch screen.

Table 3.7.2 I/O Port and Specifications (4/5)

X: Don't care

| Port   | Pin name   | Specification                         | I/O register |      |      |                                     |
|--------|------------|---------------------------------------|--------------|------|------|-------------------------------------|
|        |            |                                       | Pn           | PnCR | PnFC | PnFC2                               |
| Port P | PP3 to PP5 | Input port                            | X            | 0    | 0    | <PP1F2:3F2>=0                       |
|        |            | Output port                           | X            | 1    | 0    | <PP1F2:3F2>=0                       |
|        | PP6        | Output port                           | X            | None | 0    | None                                |
|        | PP3        | INT5 input                            | X            | 0    | 1    | <PP1F2>=0                           |
|        |            | TA7OUT Output                         | X            | 1    | 1    | <PP1F2>=0                           |
|        |            | TXD0 Output                           | X            | X    | X    | <PP0F2>=0<br><PP1F2>=1<br><PP4F2>=1 |
|        |            | TXD0 Output (Open-drain)              | X            | X    | X    | <PP0F2>=1<br><PP1F2>=1<br><PP4F2>=1 |
|        |            | TXD1 Output                           | X            | X    | X    | <PP0F2>=0<br><PP1F2>=1<br><PP4F2>=0 |
|        |            | TXD1 Output (Open-drain)              | X            | X    | X    | <PP0F2>=1<br><PP1F2>=1<br><PP4F2>=0 |
|        |            |                                       |              |      |      |                                     |
|        |            |                                       |              |      |      |                                     |
|        | PP6        | INT6 Input                            | X            | 0    | 1    | <PP2F2>=0                           |
|        |            | TB0IN0 Input                          | X            | 1    | 1    | <PP2F2>=0                           |
|        |            | RXD1 (PP4/RXD1) Input                 | X            | X    | X    | <PP2F2>=1<br><PP5F2>=0              |
|        |            | RXD1(P91/RXD1) Input                  | X            | X    | X    | <PP2F2>=1<br><PP5F2>=1              |
|        | PP5        | INT7 Input                            | X            | 0    | 1    | <PP3F2>=0                           |
|        |            | TB1IN0 Input                          | X            | 1    | 1    | <PP3F2>=0                           |
|        |            | SCLK1 (PP5/SCLK1) Input<br>CTS1 Input | X            | 0    | X    | <PP3F2>=1<br><PP6F2>=0              |
|        |            | SCLK1 (P92/SCLK1) Input<br>CTS1 Input | X            | 0    | X    | <PP3F2>=1<br><PP6F2>=1              |
|        |            | SCLK0 Output                          | X            | 1    | X    | <PP3F2>=1<br><PP6F2>=1              |
|        |            | SCLK1 Output                          | X            | 1    | X    | <PP3F2>=1<br><PP6F2>=0              |
|        |            |                                       |              |      |      |                                     |
|        |            |                                       |              |      |      |                                     |
|        | PP7        | TB1OUT0 Output                        | X            | None | 1    | None                                |
| Port R | PR0 to PR3 | Input port                            | X            | 0    | 0    | None                                |
|        |            | Output port                           | X            | 1    | 0    |                                     |
|        | PR0        | SPDI_PR0 Input (to PC4)               | X            | 0    | 1    |                                     |
|        | PR1        | SPDO Output                           | X            | 1    | 1    |                                     |
|        | PR2        | SPCS Output                           | X            | 1    | 1    |                                     |
|        | PR3        | SPCLK Output                          | X            | 1    | 1    |                                     |
| Port T | PT0 to PT7 | Input port                            | X            | 0    | 0    | 0                                   |
|        |            | Output port                           | X            | 1    | 0    | 0                                   |
|        |            | D24 to D31                            | X            | X    | 1    | 1                                   |
| Port V | PV6 to PV7 | Input port                            | X            | 0    | 0    | 0                                   |
|        |            | Output port                           | X            | 1    | 0    | 0                                   |
|        |            | Output port (Open-drain)              | X            | 1    | 0    | 1                                   |
|        | PV6        | SDA I/O                               | X            | 1    | 1    | 0                                   |
|        |            | SDA I/O (Open-drain)                  | X            | 1    | 1    | 1                                   |
|        | PV7        | SCL I/O                               | X            | 1    | 1    | 0                                   |
|        |            | SCL I/O (Open-drain)                  | X            | 1    | 1    | 1                                   |
|        |            |                                       |              |      |      |                                     |

Table 3.7.2 I/O Port and Specifications (5/5)

X: Don't care

| Port   | Pin name | Specification                              | I/O register |      |      |                |
|--------|----------|--------------------------------------------|--------------|------|------|----------------|
|        |          |                                            | Pn           | PnCR | PnFC | PnFC2          |
| Port X | PX5      | Input port                                 | X            | 0    | 0    | X              |
|        | PX4      | Output port                                | X            | None | 0    | X              |
|        | PX5      | Output port                                | X            | 1    | 0    | X              |
|        | PX4      | CLKOUT Output                              | 0            | None | 1    | X              |
|        | PX5      | X1USB Input                                | X            | 0    | 1    | None           |
|        |          | X1D4 Output (Output clock = $\times 1/8$ ) | 1            | 1    | 1    | <PX5F2:4F2>=00 |
|        |          | X1D4 Output (Output clock = $\times 1/4$ ) | 1            | 1    | 1    | <PX5F2:4F2>=01 |
|        |          | X1D4 Output (Output clock = $\times 1/2$ ) | 1            | 1    | 1    | <PX5F2:4F2>=10 |
|        |          | X1D4 Output (Output clock = $\times 1/1$ ) | 1            | 1    | 1    | <PX5F2:4F2>=11 |

### 3.7.1 Port 1 (P10 to P17)

Port1 is an 8-bit general-purpose I/O port. Bits can be individually set as either inputs or outputs by control register P1CR and function register P1FC.

In addition to functioning as a general-purpose I/O port, port1 can also function as a data bus (D8 to D15).

Setting the AM1 and AM0 pins as shown below and resetting the device initialize port 1 to the following function pins:

| AM1 | AM0 | Function Setting after reset is released |
|-----|-----|------------------------------------------|
| 0   | 0   | Don't use this setting                   |
| 0   | 1   | Data bus (D8 to D15)                     |
| 1   | 0   | Data bus (D8 to D15)                     |
| 1   | 1   | Don't use this setting                   |

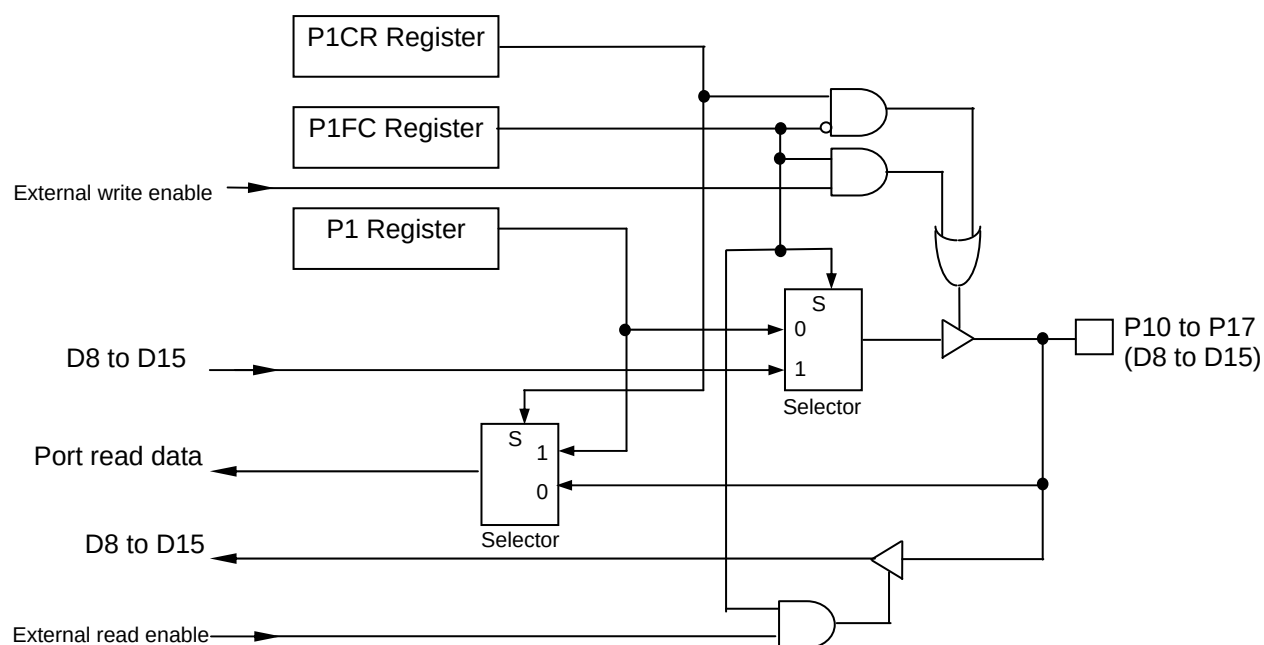


Figure 3.7.1 Port1

| Port 1 register |                    |                                                                   |     |     |     |     |     |     |     |
|-----------------|--------------------|-------------------------------------------------------------------|-----|-----|-----|-----|-----|-----|-----|
| P1<br>(0004H)   |                    | 7                                                                 | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|                 | bit Symbol         | P17                                                               | P16 | P15 | P14 | P13 | P12 | P11 | P10 |
|                 | Read/Write         | R/W                                                               |     |     |     |     |     |     |     |
|                 | System Reset State | Data from external port (Output latch register is cleared to “0”) |     |     |     |     |     |     |     |

| Port 1 Control register |                    |      |      |      |      |      |      |      |      |
|-------------------------|--------------------|------|------|------|------|------|------|------|------|
| P1CR<br>(0006H)         |                    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|                         | bit Symbol         | P17C | P16C | P15C | P14C | P13C | P12C | P11C | P10C |
|                         | Read/Write         | W    |      |      |      |      |      |      |      |
|                         | System Reset State | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| Function                | 0: Input 1: Output |      |      |      |      |      |      |      |      |

| Port 1 Function register |                    |   |   |   |   |   |   |   |                                      |
|--------------------------|--------------------|---|---|---|---|---|---|---|--------------------------------------|
| P1FC<br>(0007H)          |                    | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0                                    |
|                          | bit Symbol         |   |   |   |   |   |   |   | P1F                                  |
|                          | Read/Write         |   |   |   |   |   |   |   | W                                    |
|                          | System Reset State |   |   |   |   |   |   |   | 1                                    |
| Function                 |                    |   |   |   |   |   |   |   | 0: Port<br>1:Data bus<br>(D8 to D15) |

| Port 1 Drive register |                                                     |      |      |      |      |      |      |      |      |
|-----------------------|-----------------------------------------------------|------|------|------|------|------|------|------|------|
| P1DR<br>(0081H)       |                                                     | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|                       | bit Symbol                                          | P17D | P16D | P15D | P14D | P13D | P12D | P11D | P10D |
|                       | Read/Write                                          | R/W  |      |      |      |      |      |      |      |
|                       | System Reset State                                  | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| Function              | Input/Output buffer drive register for standby mode |      |      |      |      |      |      |      |      |

Note: A read-modify-write operation cannot be performed for P1CR, P1FC.

Figure 3.7.2 Register for Port1

### 3.7.2 Port 4 (P40 to P47)

Port4 is an 8-bit general-purpose Output ports. In addition to functioning as a general-purpose Output port, port4 can also function as an address bus (A0 to A7). Each bit can be set individually for function. Setting the AM1 and AM0 pins as shown below and resetting the device initialize port 4 to the following function pins:

| AM1 | AM0 | Function Setting after reset is released |
|-----|-----|------------------------------------------|
| 0   | 0   | Don't use this setting                   |
| 0   | 1   | Address bus (A0 to A7)                   |
| 1   | 0   | Address bus (A0 to A7)                   |
| 1   | 1   | Don't use this setting                   |

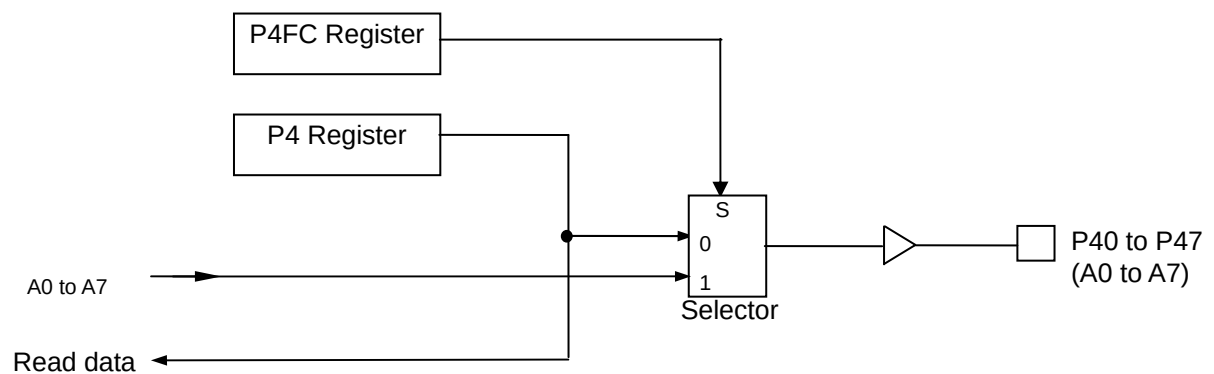


Figure 3.7.3 Port4

Port 4 register

|                    |     |     |     |     |     |     |     |     |
|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|
|                    | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| bit Symbol         | P47 | P46 | P45 | P44 | P43 | P42 | P41 | P40 |
| Read/Write         | R/W |     |     |     |     |     |     |     |
| System Reset State | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

P4  
(0010H)

Port 4 Function register

|                    |                                 |      |      |      |      |      |      |      |
|--------------------|---------------------------------|------|------|------|------|------|------|------|
|                    | 7                               | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
| bit Symbol         | P47F                            | P46F | P45F | P44F | P43F | P42F | P41F | P40F |
| Read/Write         | W                               |      |      |      |      |      |      |      |
| System Reset State | 1                               | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| Function           | 0:Port 1:Address bus (A0 to A7) |      |      |      |      |      |      |      |

P4FC  
(0013H)

Port 4 Drive register

|                    |                                                     |      |      |      |      |      |      |      |
|--------------------|-----------------------------------------------------|------|------|------|------|------|------|------|
|                    | 7                                                   | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
| bit Symbol         | P47D                                                | P46D | P45D | P44D | P43D | P42D | P41D | P40D |
| Read/Write         | R/W                                                 |      |      |      |      |      |      |      |
| System Reset State | 1                                                   | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| Function           | Input/Output buffer drive register for standby mode |      |      |      |      |      |      |      |

P4DR  
(0084H)

Note: A read-modify-write operation cannot be performed for P4FC.

Figure 3.7.4 Register for Port1



3.7.3 Port 5 (P50 to P57)

Port5 is an 8-bit general-purpose Output ports. In addition to functioning as a general-purpose I/O port, port5 can also function as an address bus (A8 to A15). Each bit can be set individually for function. Setting the AM1 and AM0 pins as shown below and resetting the device initialize port 5 to the following function pins:

| AM1 | AM0 | Function Setting after reset is released |
|-----|-----|------------------------------------------|
| 0   | 0   | Don't use this setting                   |
| 0   | 1   | Address bus (A8 ~ A15)                   |
| 1   | 0   | Address bus (A8 ~ A15)                   |
| 1   | 1   | Don't use this setting                   |

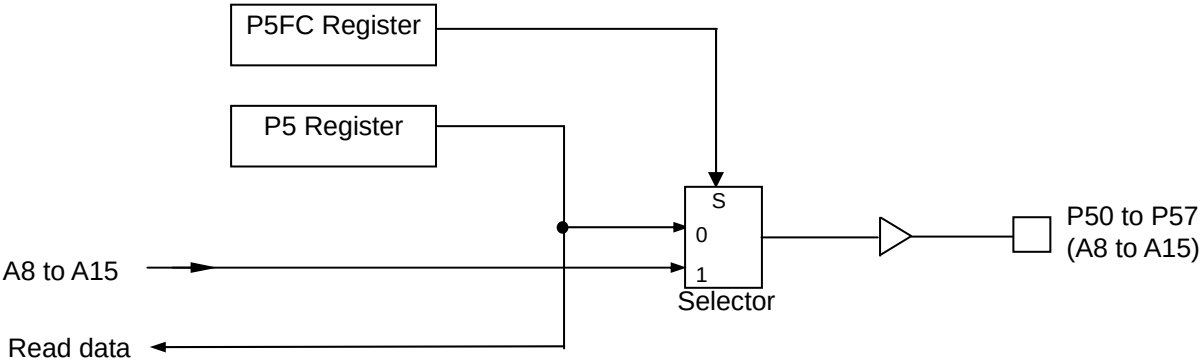


Figure 3.7.5 Port5

Port 5 register

|               |                    |     |     |     |     |     |     |     |     |
|---------------|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|
|               | 7                  | 6   | 5   | 4   | 3   | 2   | 1   | 0   |     |
| P5<br>(0014H) | bit Symbol         | P57 | P56 | P55 | P54 | P53 | P52 | P51 | P50 |
|               | Read/Write         | R/W |     |     |     |     |     |     |     |
|               | System Reset State | 0   | 0   | 0   | 0   | 0   | 0   | 0   |     |

Port 5 Function register

|                 |                    |                                  |      |      |      |      |      |      |      |
|-----------------|--------------------|----------------------------------|------|------|------|------|------|------|------|
|                 | 7                  | 6                                | 5    | 4    | 3    | 2    | 1    | 0    |      |
| P5FC<br>(0017H) | bit Symbol         | P57F                             | P56F | P55F | P54F | P53F | P52F | P51F | P50F |
|                 | Read/Write         | W                                |      |      |      |      |      |      |      |
|                 | System Reset State | 1                                | 1    | 1    | 1    | 1    | 1    | 1    |      |
|                 | Function           | 0:Port 1:Address bus (A8 to A15) |      |      |      |      |      |      |      |

Port 5 Drive register

|                 |                    |                                                     |      |      |      |      |      |      |      |
|-----------------|--------------------|-----------------------------------------------------|------|------|------|------|------|------|------|
|                 | 7                  | 6                                                   | 5    | 4    | 3    | 2    | 1    | 0    |      |
| P5DR<br>(0085H) | bit Symbol         | P57D                                                | P56D | P55D | P54D | P53D | P52D | P51D | P50D |
|                 | Read/Write         | R/W                                                 |      |      |      |      |      |      |      |
|                 | System Reset State | 1                                                   | 1    | 1    | 1    | 1    | 1    | 1    |      |
|                 | Function           | Input/Output buffer drive register for standby mode |      |      |      |      |      |      |      |

Note: A read-modify-write operation cannot be performed for P5FC.

Figure 3.7.6 Register for Port5

### 3.7.4 Port 6 (P60 to P67)

Port6 is an 8-bit general-purpose I/O ports. Bits can be individually set as either inputs or outputs and function by control register P6CR and function register P6FC.

In addition to functioning as a general-purpose I/O port, port6 can also function as an address bus (A16 to A23). Setting the AM1 and AM0 pins as shown below and resetting the device initialize port 6 to the following function pins:

| AM1 | AM0 | Function Setting after reset is released |
|-----|-----|------------------------------------------|
| 0   | 0   | Don't use this setting                   |
| 0   | 1   | Address bus(A16 ~ A23)                   |
| 1   | 0   | Address bus(A16 ~ A23)                   |
| 1   | 1   | Don't use this setting                   |

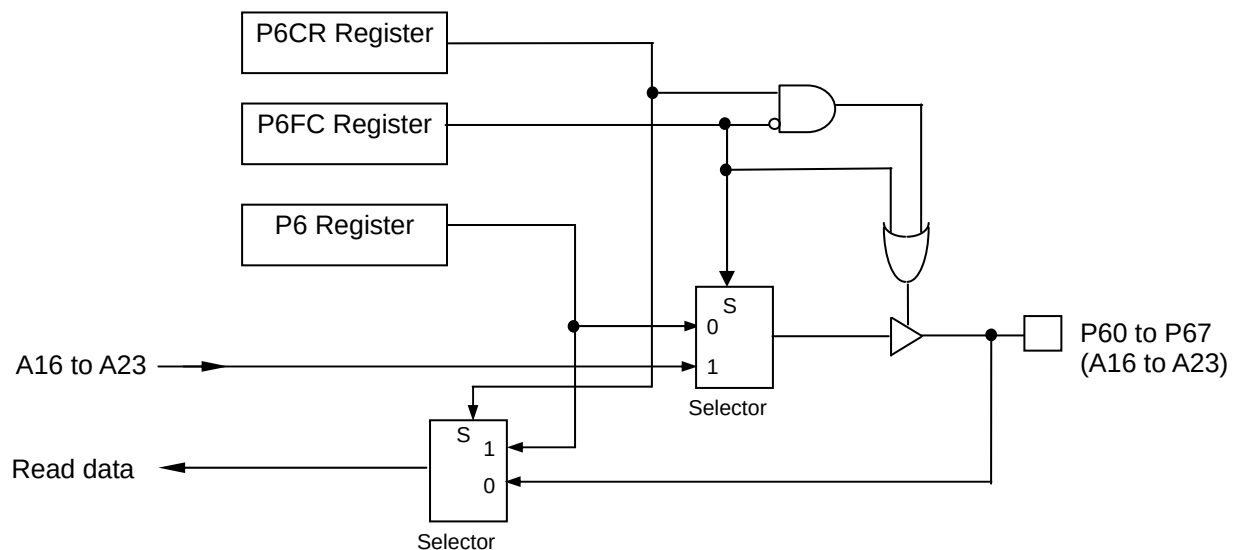


Figure 3.7.7 Port6

| Port 6 register |                       |                                                                   |     |     |     |     |     |     |     |
|-----------------|-----------------------|-------------------------------------------------------------------|-----|-----|-----|-----|-----|-----|-----|
| P6<br>(0018H)   |                       | 7                                                                 | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|                 | bit Symbol            | P67                                                               | P66 | P65 | P64 | P63 | P62 | P61 | P60 |
|                 | Read/Write            | R/W                                                               |     |     |     |     |     |     |     |
|                 | System<br>Reset State | Data from external port (Output latch register is cleared to “0”) |     |     |     |     |     |     |     |

| Port 6 Control register |                       |                  |      |      |      |      |      |      |      |
|-------------------------|-----------------------|------------------|------|------|------|------|------|------|------|
| P6CR<br>(001AH)         |                       | 7                | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|                         | bit Symbol            | P67C             | P66C | P65C | P64C | P63C | P62C | P61C | P60C |
|                         | Read/Write            | W                |      |      |      |      |      |      |      |
|                         | System<br>Reset State | 0                | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
|                         | Function              | 0:Input 1:Output |      |      |      |      |      |      |      |

| Port 6 Function register |                       |                                    |      |      |      |      |      |      |      |
|--------------------------|-----------------------|------------------------------------|------|------|------|------|------|------|------|
| P6FC<br>(001BH)          |                       | 7                                  | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|                          | bit Symbol            | P67F                               | P66F | P65F | P64F | P63F | P62F | P61F | P60F |
|                          | Read/Write            | W                                  |      |      |      |      |      |      |      |
|                          | System<br>Reset State | 1                                  | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
|                          | Function              | 0: Port 1:Address bus (A16 to A23) |      |      |      |      |      |      |      |

| Port 6 Drive buffer register |                       |                                                     |      |      |      |      |      |      |      |
|------------------------------|-----------------------|-----------------------------------------------------|------|------|------|------|------|------|------|
| P6DR<br>(0086H)              |                       | 7                                                   | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|                              | bit Symbol            | P67D                                                | P66D | P65D | P64D | P63D | P62D | P61D | P60D |
|                              | Read/Write            | R/W                                                 |      |      |      |      |      |      |      |
|                              | System<br>Reset State | 1                                                   | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
|                              | Hot Reset<br>State    | –                                                   | –    | –    | –    | –    | –    | –    | –    |
|                              | Function              | Input/Output buffer drive register for standby mode |      |      |      |      |      |      |      |

Note: A read-modify-write operation cannot be performed for P6CR, P6FC.

Figure 3.7.8 Register for Port 6

### 3.7.5 Port 7 (P70 to P76)

Port7 is a 7-bit general-purpose I/O port (P70 is used for output only). Bits can be individually set as either inputs or outputs by control register P7CR and function register P7FC.

In addition to functioning as a general-purpose I/O port, P70 to P76 pins can also function as interface-pins for external memory.

A reset initializes P70 pin to output port mode, and P71 to P76 pins to input port mode.

Setting the AM1 and AM0 pins as shown below and resetting the device initialize port 7 to the following function pins:

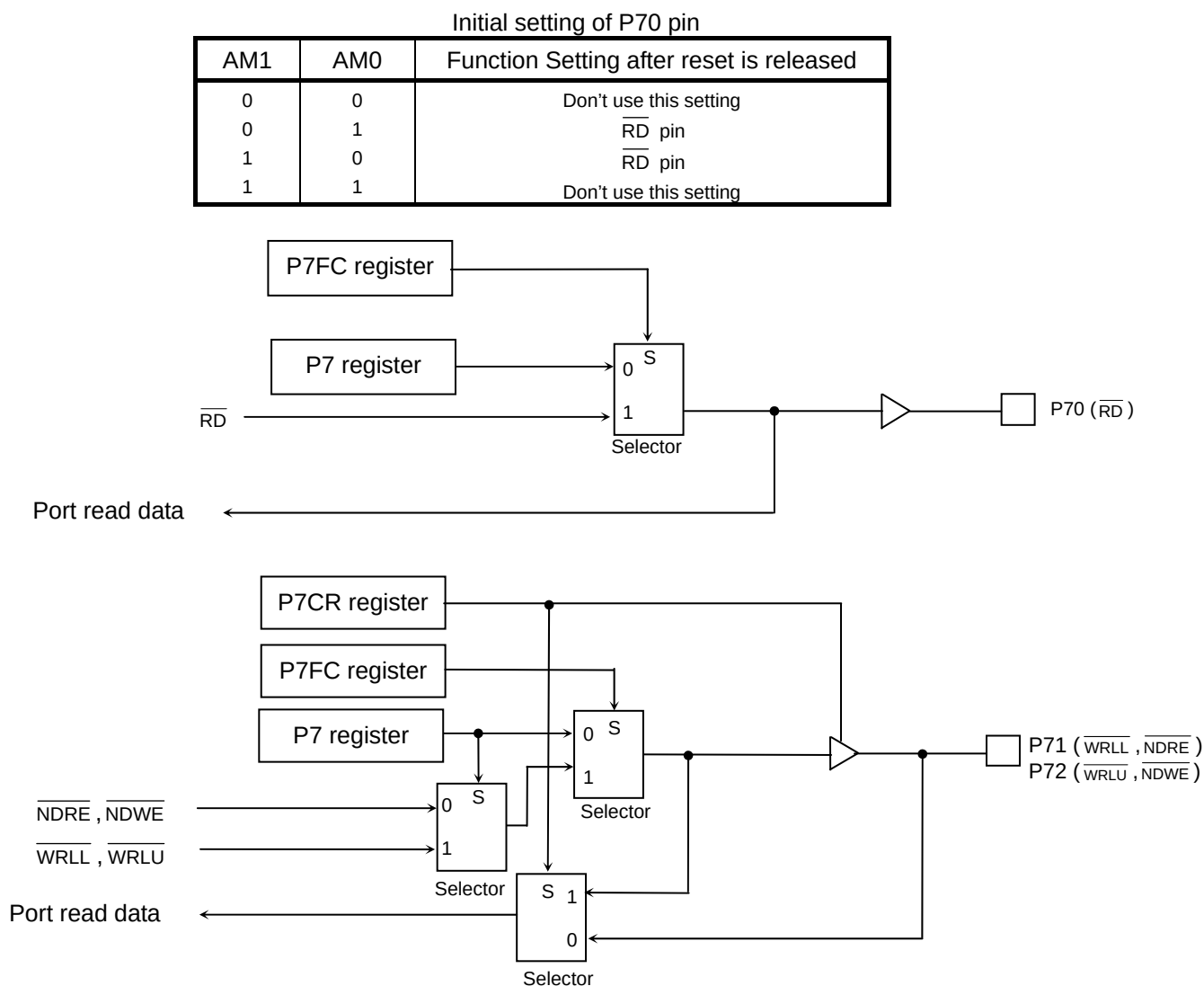
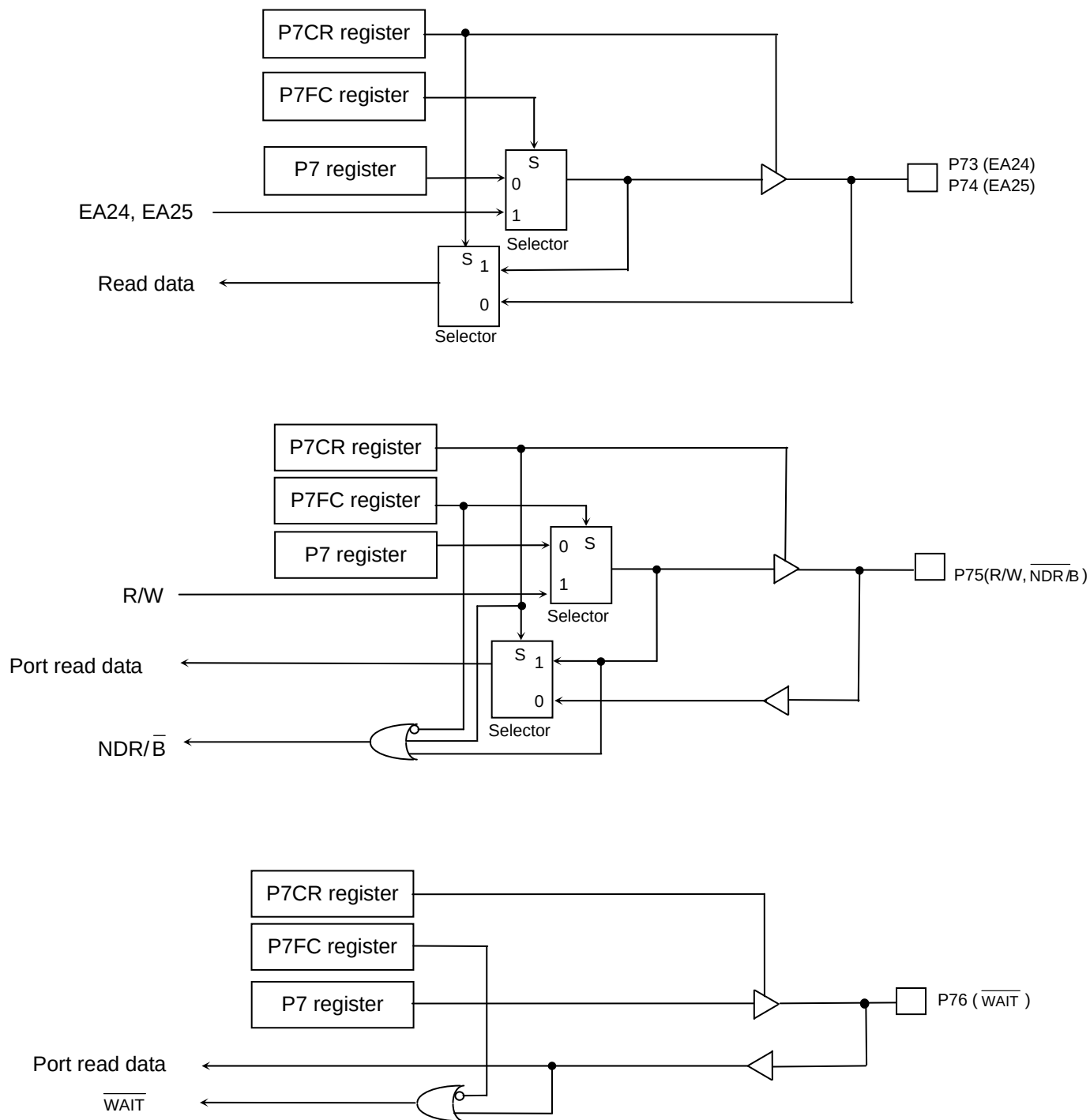


Figure 3.7.9 Port7



| Port 7 register |                    |                                                               |     |                                                                   |     |                                                               |     |     |
|-----------------|--------------------|---------------------------------------------------------------|-----|-------------------------------------------------------------------|-----|---------------------------------------------------------------|-----|-----|
|                 | 7                  | 6                                                             | 5   | 4                                                                 | 3   | 2                                                             | 1   | 0   |
| P7<br>(001CH)   | bit Symbol         | P76                                                           | P75 | P74                                                               | P73 | P72                                                           | P71 | P70 |
|                 | Read/Write         | R/W                                                           |     |                                                                   |     |                                                               |     |     |
|                 | System Reset State | Data from external port (Output latch register is set to "1") |     | Data from external port (Output latch register is cleared to "0") |     | Data from external port (Output latch register is set to "1") |     | 1   |

| Port 7 Control register |                    |                    |      |      |      |      |      |   |
|-------------------------|--------------------|--------------------|------|------|------|------|------|---|
|                         | 7                  | 6                  | 5    | 4    | 3    | 2    | 1    | 0 |
| P7CR<br>(001EH)         | bit Symbol         | P76C               | P75C | P74C | P73C | P72C | P71C |   |
|                         | Read/Write         | W                  |      |      |      |      |      |   |
|                         | System Reset State | 0                  | 0    | 0    | 0    | 0    | 0    |   |
|                         | Function           | 0: Input 1: Output |      |      |      |      |      |   |

| Port 7 Function register |                    |                   |                          |      |      |                                                                           |                                                                           |                                     |
|--------------------------|--------------------|-------------------|--------------------------|------|------|---------------------------------------------------------------------------|---------------------------------------------------------------------------|-------------------------------------|
|                          | 7                  | 6                 | 5                        | 4    | 3    | 2                                                                         | 1                                                                         | 0                                   |
| P7FC<br>(001FH)          | bit Symbol         | P76F              | P75F                     | P74F | P73F | P72F                                                                      | P71F                                                                      | P70F                                |
|                          | Read/Write         | W                 |                          |      |      |                                                                           |                                                                           |                                     |
|                          | System Reset State | 0                 | 0                        | 0    | 0    | 0                                                                         | 0                                                                         | 1                                   |
|                          | Function           | 0:Port<br>1: WAIT | Refer to following table |      |      | 0:Port<br>1: $\overline{\text{NDWE}}$ at<br><P72>=0<br>WRLU at<br><P72>=1 | 0:Port<br>1: $\overline{\text{NDRE}}$ at<br><P71>=0<br>WRLI at<br><P71>=1 | 0:Port<br>1: $\overline{\text{RD}}$ |

| Port 7 Drive register |                    |                                                     |      |      |      |      |      |      |
|-----------------------|--------------------|-----------------------------------------------------|------|------|------|------|------|------|
|                       | 7                  | 6                                                   | 5    | 4    | 3    | 2    | 1    | 0    |
| P7DR<br>(0087H)       | bit Symbol         | P76D                                                | P75D | P74D | P73D | P72D | P71D | P70D |
|                       | Read/Write         | R/W                                                 |      |      |      |      |      |      |
|                       | System Reset State | 1                                                   | 1    | 1    | 1    | 1    | 1    | 1    |
|                       | Function           | Input/Output buffer drive register for standby mode |      |      |      |      |      |      |

P73 setting

|                  | 0          | 1           |
|------------------|------------|-------------|
| <P73C><br><P73F> | Input Port | Output Port |
| 0                | Reserved   | EA24Output  |
| 1                |            |             |

P72 setting

|                  | 0          | 1                                                    |
|------------------|------------|------------------------------------------------------|
| <P72C><br><P72F> | Input Port | Output Port                                          |
| 0                | Reserved   | NDWE Output (at <P72>=0)<br>WRLU Output (at <P72>=1) |
| 1                |            |                                                      |

P71 setting

|                  | 0          | 1                                                    |
|------------------|------------|------------------------------------------------------|
| <P71C><br><P71F> | Input Port | Output Port                                          |
| 0                | Reserved   | NDRE Output (at <P71>=0)<br>WRLI Output (at <P71>=1) |
| 1                |            |                                                      |

P76 setting

|                  | 0          | 1           |
|------------------|------------|-------------|
| <P76C><br><P76F> | Input Port | Output Port |
| 0                | Input Port | Output Port |
| 1                | WAIT Input | Reserved    |

P75 setting

|                  | 0                                | 1           |
|------------------|----------------------------------|-------------|
| <P75C><br><P75F> | Input Port                       | Output Port |
| 0                | Input Port                       | Output Port |
| 1                | NDR/ $\overline{\text{E}}$ Input | R/W Output  |

P74 setting

|                  | 0          | 1           |
|------------------|------------|-------------|
| <P74C><br><P74F> | Input Port | Output Port |
| 0                | Input Port | Output Port |
| 1                | Reserved   | EA25Output  |

Note1: A read-modify-write operation cannot be performed for P7CR, P7FC.

Note2: When  $\overline{\text{NDRE}}$  and  $\overline{\text{NDWE}}$  are used, set registers in the following order to avoid outputting a negative glitch.

| Order | Register | bit2 | bit1 |
|-------|----------|------|------|
| (1)   | P7       | 0    | 0    |
| (2)   | P7FC     | 1    | 1    |
| (3)   | P7CR     | 1    | 1    |

Figure 3.7.11 Register for Port 7

### 3.7.6 Port 8 (P80 to P83, P86, P87)

Port 8 is 6-bit output ports. Resetting sets the output latch of P82 to “0” and the output latches of P80 to P81, P83, P86 and P87 to “1”.

Port 8 can also be set to function as an interface-pin for external memory using function register P8FC.

Writing “1” in the corresponding bit of P8FC and P8FC2 enables the respective functions.

Resetting P8FC to “0” and P8FC2 to “0”, sets all bits to output ports.

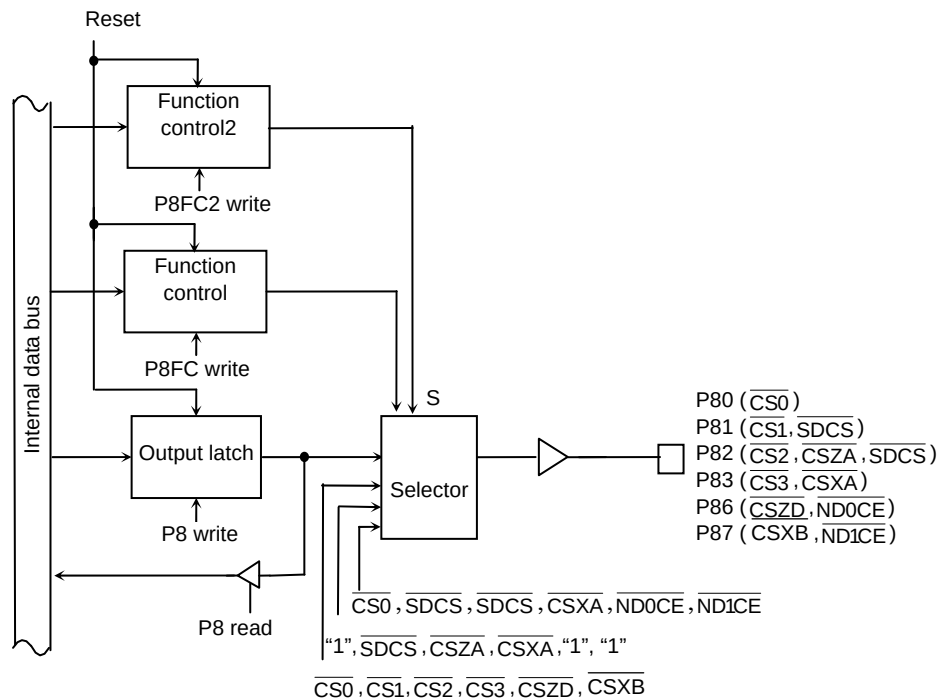


Figure 3.7.12 Port 8





### 3.7.7 Port 9 (P90 to P92, P96, P97)

P90 to P92 are 3-bit general-purpose I/O port. I/O can be set on a bit basis using the control register. Each bit can be set individually for input or output. Resetting sets P90 to P92 to input port and all bits of output latch to "1".

P96 to P97 are 2-bit general-purpose input port.

Writing "1" the corresponding bits of P9FC enables the respective functions.

Resetting resets the P9FC to "0", and sets all bits to input ports.

#### (1) Port 90 (TXD0), Port 91 (RXD0), Port 92 (SCLK0, $\overline{\text{CTS0}}$ )

Ports 90 to 92 are general-purpose I/O port. They are also function as either SIO0 or SIO1. SIO0 and SIO1 functions are also used as PP3 to PP5 pins. When selecting SIO0 function (using Port 9 or Port P), set P9FC2<P93F2, P94F2, P95F2>. And when selection SIO1 function (using Port 9 or Port P), set PPFC2<PP4F2, PP5F2, PP6F2>.

|     | SIO mode<br>(SIO0 module)               | UART, IrDA mode<br>(SIO0 module)                                       |
|-----|-----------------------------------------|------------------------------------------------------------------------|
| P90 | TXD0, TXD1<br>(Data output)             | TXD0<br>(Data output)                                                  |
| P91 | RXD0, RXD1<br>(Data input)              | RXD0<br>(Data input)                                                   |
| P92 | SCLK0, SCLK1<br>(Clock input or output) | $\overline{\text{CTS0}}$ , $\overline{\text{CTS1}}$<br>(Clear to send) |

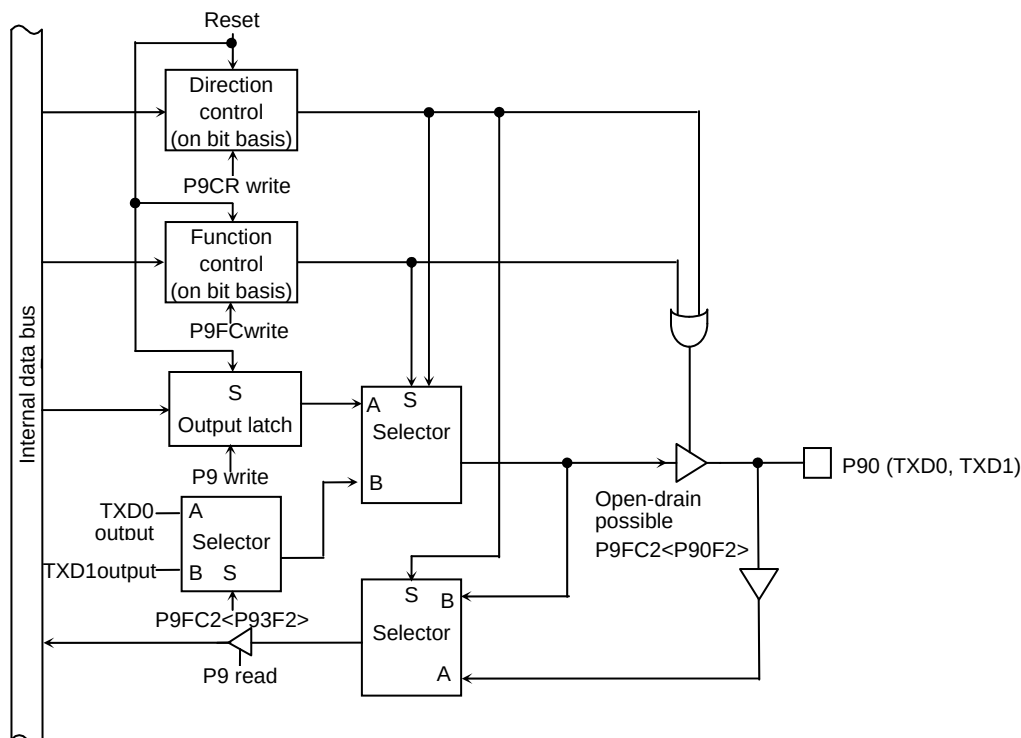


Figure 3.7.14 P90

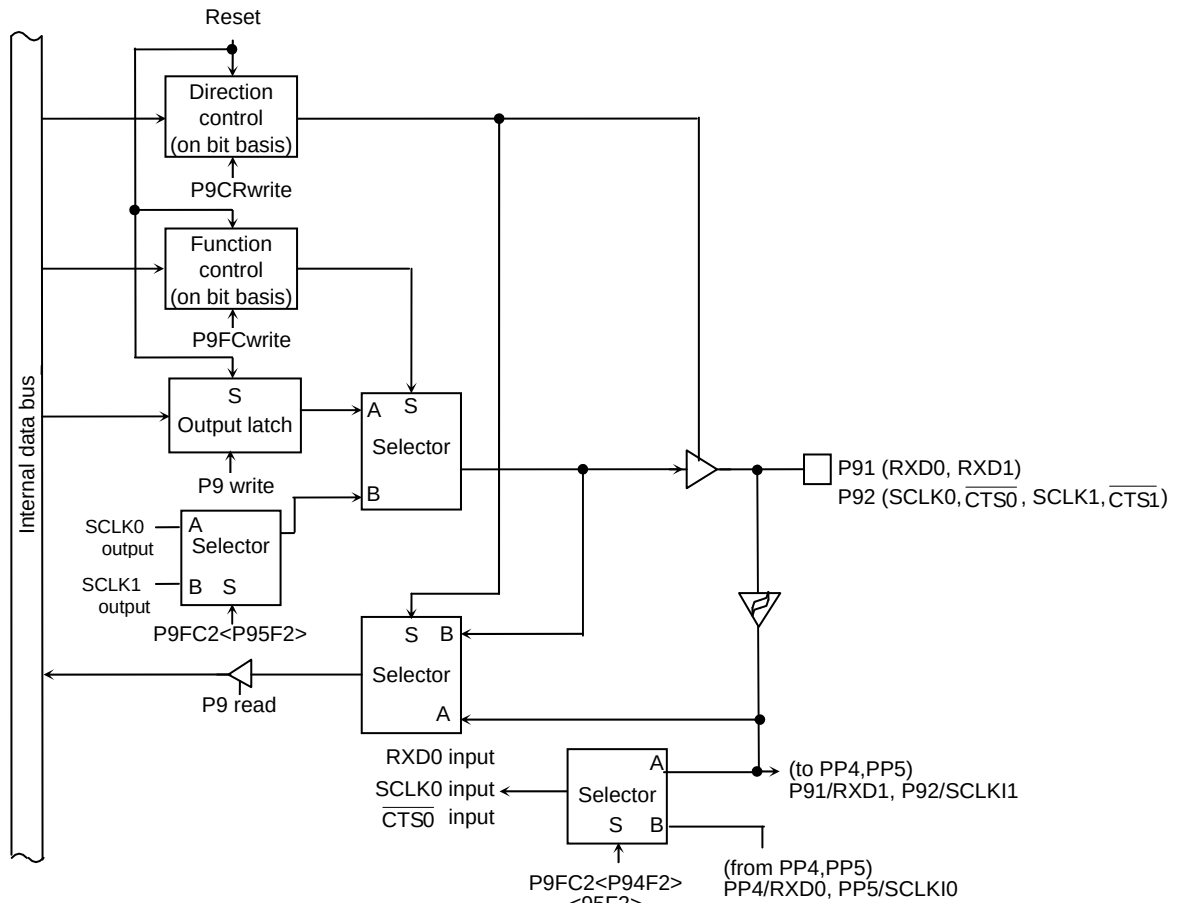


Figure 3.7.15 P91, 92

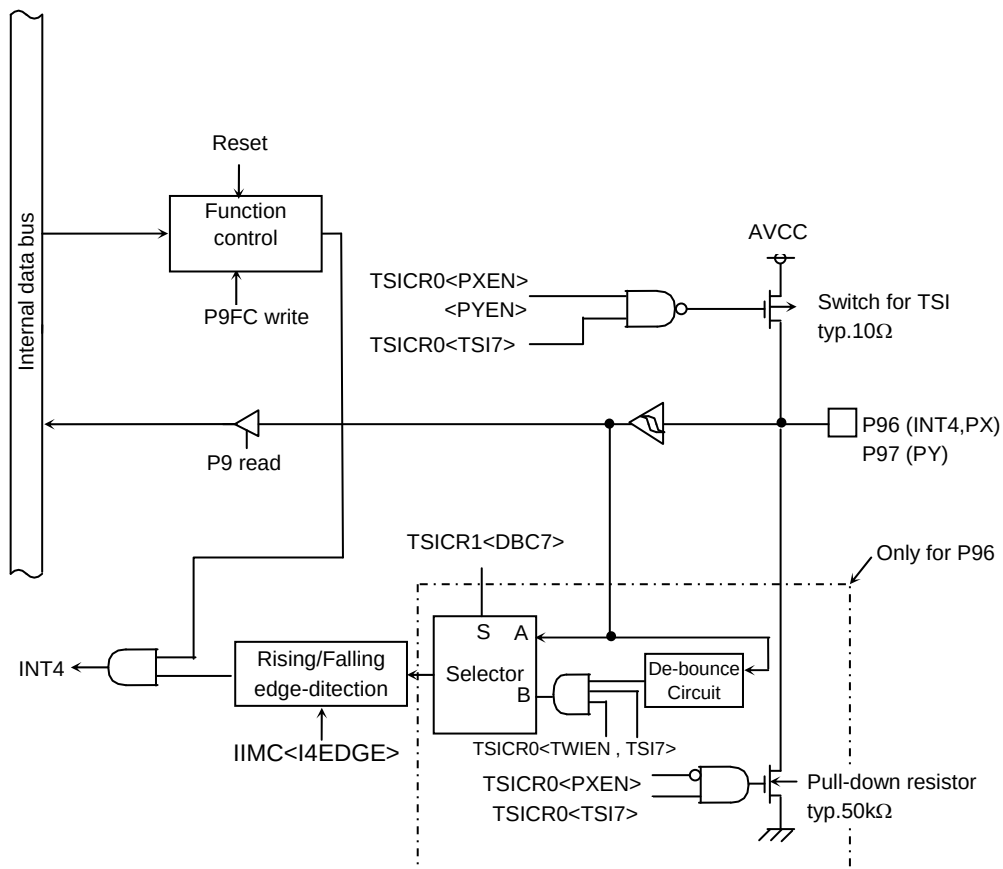


Figure 3.7.16 Port 96,97

Port 9 register

|               | 7                  | 6                       | 5   | 4 | 3 | 2                                                             | 1   | 0   |
|---------------|--------------------|-------------------------|-----|---|---|---------------------------------------------------------------|-----|-----|
| P9<br>(0024H) | bit Symbol         | P97                     | P96 |   |   | P92                                                           | P91 | P90 |
|               | Read/Write         | R                       |     |   |   | R/W                                                           |     |     |
|               | System Reset State | Data from external port |     |   |   | Data from external port (Output latch register is set to "1") |     |     |

Port 9 control register

|                 | 7                  | 6 | 5 | 4 | 3 | 2                        | 1    | 0    |
|-----------------|--------------------|---|---|---|---|--------------------------|------|------|
| P9CR<br>(0026H) | bit Symbol         |   |   |   |   | P92C                     | P91C | P90C |
|                 | Read/Write         |   |   |   |   | W                        |      |      |
|                 | System Reset State |   |   |   |   | 0                        | 0    | 0    |
|                 | Function           |   |   |   |   | Refer to following table |      |      |

Port 9 function register

|                 | 7                  | 6                        | 5 | 4 | 3 | 2                        | 1 | 0                        |
|-----------------|--------------------|--------------------------|---|---|---|--------------------------|---|--------------------------|
| P9FC<br>(0027H) | bit Symbol         | P96F                     |   |   |   | P92F                     |   | P90F                     |
|                 | Read/Write         | W                        |   |   |   | W                        |   | W                        |
|                 | System Reset State | 0                        |   |   |   | 0                        |   | 0                        |
|                 | Function           | 0: Input port<br>1: INT4 |   |   |   | Refer to following table |   | Refer to following table |

Port 9 Function registers 2

|                  | 7                  | 6                | 5                                                                                                    | 4                                      | 3                                       | 2                | 1 | 0                       |
|------------------|--------------------|------------------|------------------------------------------------------------------------------------------------------|----------------------------------------|-----------------------------------------|------------------|---|-------------------------|
| P9FC2<br>(0025H) | bit Symbol         | –                | P95F2                                                                                                | P94F2                                  | P93F2                                   | –                |   | P90F2                   |
|                  | Read/Write         | W                | W                                                                                                    | W                                      | W                                       | W                |   | W                       |
|                  | System Reset State | 0                | 0                                                                                                    | 0                                      | 0                                       | 0                |   | 0                       |
|                  | Function           | Always write "0" | P92 SCLK selection<br>0: SCLK0<br>1: SLCK1<br><br>SIO0 SCLK, CTS input selection<br>0: P92<br>1: PP5 | SIO0 RXD selection<br>0: P91<br>1: PP4 | P90 TXD selection<br>0: TXD0<br>1: TXD1 | Always write "0" |   | 0:CMOS<br>1: Open-drain |

| Port 9 drive register |                       |                                                     |      |   |   |      |      |      |
|-----------------------|-----------------------|-----------------------------------------------------|------|---|---|------|------|------|
|                       | 7                     | 6                                                   | 5    | 4 | 3 | 2    | 1    | 0    |
| P9DR<br>(0089H)       | bit Symbol            | P97D                                                | P96D |   |   | P92D | P91D | P90D |
|                       | Read/Write            | R/W                                                 |      |   |   | R/W  |      |      |
|                       | System<br>Reset State | 1                                                   | 1    |   |   | 1    | 1    | 1    |
|                       | Function              | Input/Output buffer drive register for standby mode |      |   |   |      |      |      |

P92 setting

| <div>&lt;P92C&gt;<br/>&lt;P92F&gt;</div> | 0                                                  | 1                     |
|------------------------------------------|----------------------------------------------------|-----------------------|
| 0                                        | Input port,<br>CTS0, CTS1<br>/SCLK0,SCLK1<br>Input | Output port           |
| 1                                        | Don't setting                                      | SCLK0,SCLK1<br>Output |

P91 setting

| <P91C>                            |             |
|-----------------------------------|-------------|
| 0                                 | 1           |
| Input port/<br>RXD0,RXD1<br>Input | Output port |

P90 setting

| <div>&lt;P90C&gt;<br/>&lt;P90F&gt;</div> | 0                | 1                    |
|------------------------------------------|------------------|----------------------|
| 0                                        | Input port       | Output port          |
| 1                                        | Don't<br>setting | TXD0, TXD1<br>Output |

Note 1: A read-modify-write operation cannot be performed for P9CR, P9FC and P9FC2.

Note 2: When setting P96 pin to INT4 input, set P9DR<P96D> to "0" (prohibit input), and when driving P96 pin to "0", execute HALT instruction. This setting generates INT4 inside. If don't using external interrupt in HALT condition, set like an interrupt don't generated. (e.g. change port setting)

Figure 3.7.17 Register for Port 9

### 3.7.8 Port A (PA0 to PA7)

Ports A0 to A7 are 8-bit general-purpose input ports with pull-up resistor. In addition to functioning as general-purpose I/O ports, ports A0 to A7 can also, as a Keyboard interface, operate a Key-on wake-up function. The various functions can each be enabled by writing a “1” to the corresponding bit of the Port A Function Register (PAFC).

Resetting resets all bits of the register PAFC to “0” and sets all pins to be input port.

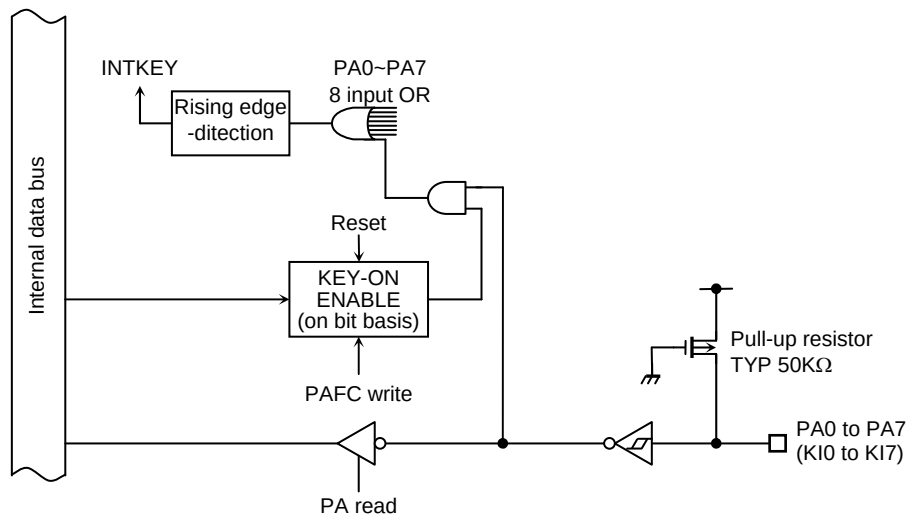


Figure 3.7.18 Port A

When PAFC = “1”, if the input of any of KI0-KI7 pins falls down, an INTKEY interrupt is generated. An INTKEY interrupt can be used to release all HALT modes.



### 3.7.9 Port C (PC0 to PC7)

PC0 to PC7 are 8-bit general-purpose I/O port. Each bit can be set individually for input or output. Resetting sets Port C to an input port. It also sets all bits of the output latch register to “1”.

In addition to functioning as a general-purpose I/O port, Port C can also function as an input pin for timers (TA0IN, TA2IN), input pin for external interruption (INT0 to INT3), Extension address function (EA26, EA27, EA28), output pin for SPI controller (SPDI, SPDO and SPCLK) and output pin for Key (KO8). These settings are mode using the function register PCFC. The edge select for external interruption is determined by the IIMC register in the interruption controller.

#### (1) PC0 (INT0), PC2 (INT2)

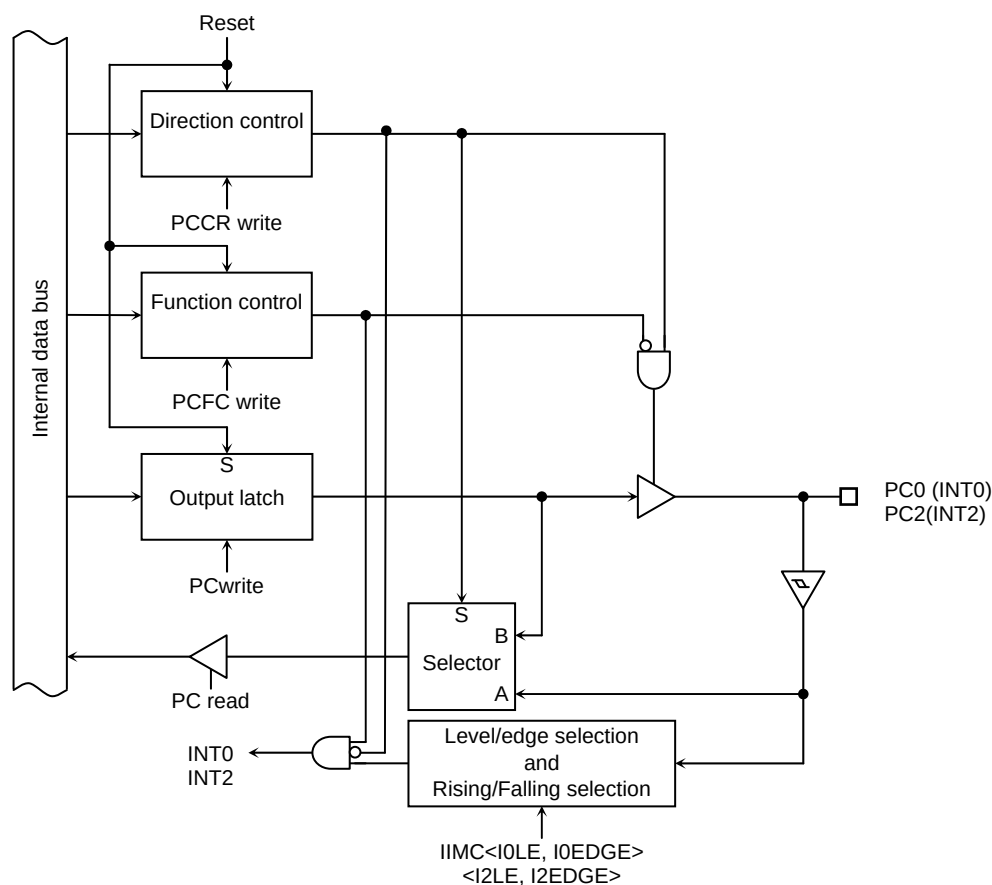


Figure 3.7.20 Port C0, C2



(2) PC1 (INT1, TA0IN), PC3 (INT3, TA2IN)

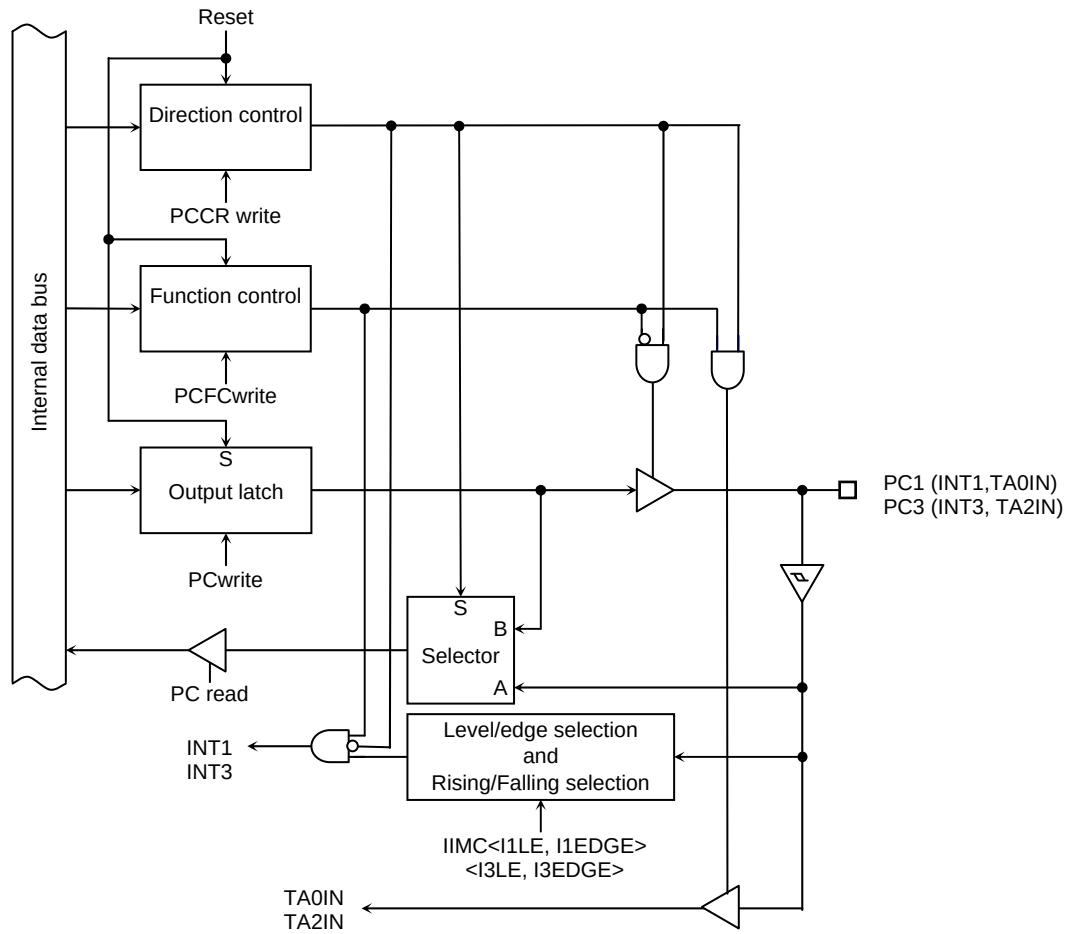


Figure 3.7.21 Port C1,C3

## (3) PC4 (EA26, SPDI)

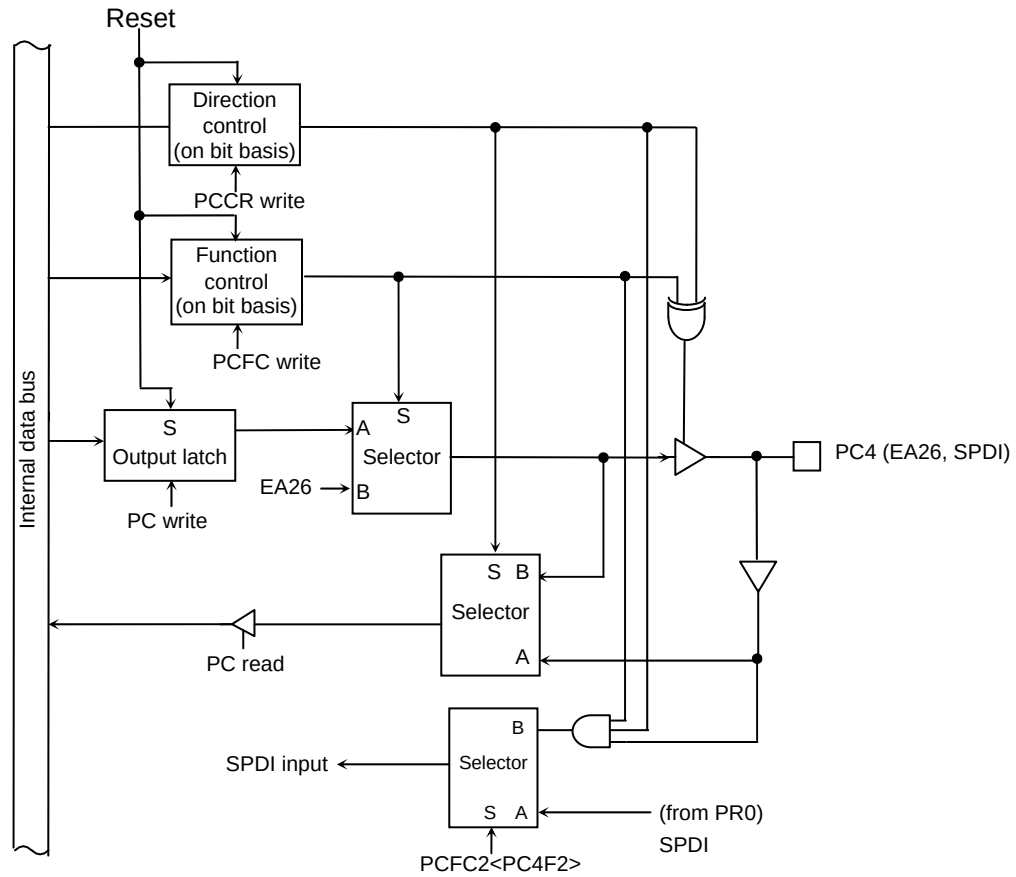


Figure 3.7.22 Port C4

## (4) PC5 (EA27), PC6 (EA28)

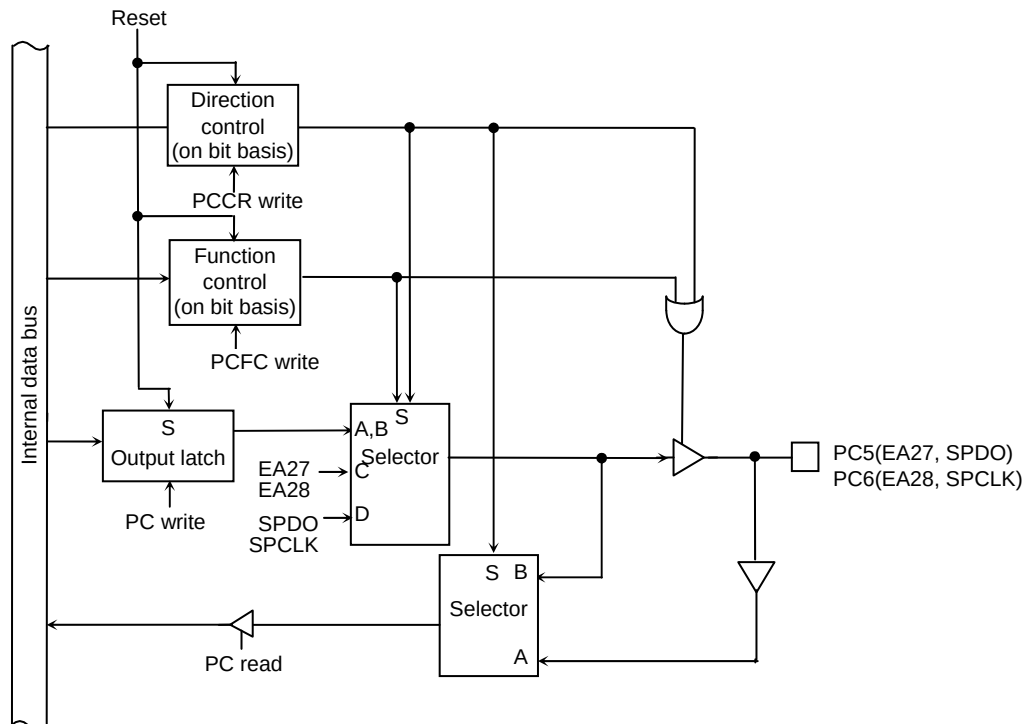


Figure 3.7.23 Port C5, C6

(5) PC7 (K08)

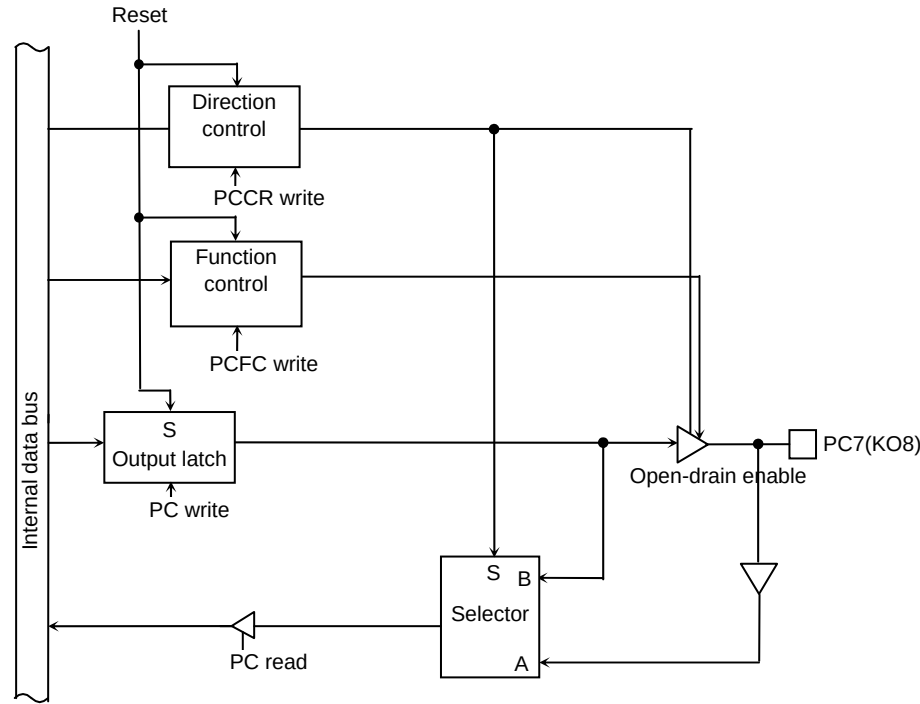


Figure 3.7.24 Port C7

Port C register

|               |                    |                                                               |     |     |     |     |     |     |     |
|---------------|--------------------|---------------------------------------------------------------|-----|-----|-----|-----|-----|-----|-----|
| PC<br>(0030H) |                    | 7                                                             | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|               | bit Symbol         | PC7                                                           | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
|               | Read/Write         | R/W                                                           |     |     |     |     |     |     |     |
|               | System Reset State | Data from external port (Output latch register is set to "1") |     |     |     |     |     |     |     |

Port C control register

|                 |                    |                    |      |      |      |      |      |      |      |
|-----------------|--------------------|--------------------|------|------|------|------|------|------|------|
| PCCR<br>(0032H) |                    | 7                  | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|                 | bit Symbol         | PC7C               | PC6C | PC5C | PC4C | PC3C | PC2C | PC1C | PC0C |
|                 | Read/Write         | W                  |      |      |      |      |      |      |      |
|                 | System Reset State | 0                  | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
|                 | Function           | 0: Input 1: Output |      |      |      |      |      |      |      |

Port C function register

|                 |                    |                          |      |      |      |      |      |      |      |
|-----------------|--------------------|--------------------------|------|------|------|------|------|------|------|
| PCFC<br>(0033H) |                    | 7                        | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|                 | bit Symbol         | PC7F                     | PC6F | PC5F | PC4F | PC3F | PC2F | PC1F | PC0F |
|                 | Read/Write         | W                        |      |      |      |      |      |      |      |
|                 | System Reset State | 0                        | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
|                 | Function           | Refer to following table |      |      |      |      |      |      |      |

Port C function register 2

|                  |                    |   |   |   |                                        |   |   |   |   |
|------------------|--------------------|---|---|---|----------------------------------------|---|---|---|---|
| PCFC2<br>(0031H) |                    | 7 | 6 | 5 | 4                                      | 3 | 2 | 1 | 0 |
|                  | bit Symbol         |   |   |   | PC4F2                                  |   |   |   |   |
|                  | Read/Write         |   |   |   | W                                      |   |   |   |   |
|                  | System Reset State |   |   |   | 0                                      |   |   |   |   |
|                  | Function           |   |   |   | SPDI pin selection<br>0: PR0<br>1: PC4 |   |   |   |   |

Port C drive register

|                    |                                                     |      |      |      |      |      |      |      |
|--------------------|-----------------------------------------------------|------|------|------|------|------|------|------|
|                    | 7                                                   | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
| bit Symbol         | PC7D                                                | PC6D | PC5D | PC4D | PC3D | PC2D | PC1D | PC0D |
| Read/Write         | R/W                                                 |      |      |      |      |      |      |      |
| System Reset State | 1                                                   | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| Function           | Input/Output buffer drive register for standby mode |      |      |      |      |      |      |      |

PC2 setting

|                  |            |               |
|------------------|------------|---------------|
| <PC2C><br><PC2F> | 0          | 1             |
| 0                | Input port | Output port   |
| 1                | INT2       | Don't setting |

PC1 setting

|                  |            |             |
|------------------|------------|-------------|
| <PC1C><br><PC1F> | 0          | 1           |
| 0                | Input port | Output port |
| 1                | INT1       | TA0IN input |

PC0 setting

|                  |            |               |
|------------------|------------|---------------|
| <PC0C><br><PC0F> | 0          | 1             |
| 0                | Input port | Output port   |
| 1                | INT0       | Don't setting |

PC5 setting

|                  |             |             |
|------------------|-------------|-------------|
| <PC5C><br><PC5F> | 0           | 1           |
| 0                | Input port  | Output port |
| 1                | EA27 output | SPDO output |

PC4 setting

|                  |             |             |
|------------------|-------------|-------------|
| <PC4C><br><PC4F> | 0           | 1           |
| 0                | Input port  | Output port |
| 1                | EA26 output | SPDI input  |

PC3 setting

|                  |            |             |
|------------------|------------|-------------|
| <PC3C><br><PC3F> | 0          | 1           |
| 0                | Input port | Output port |
| 1                | INT3       | TA2IN input |

PC7 setting

|                  |               |                        |
|------------------|---------------|------------------------|
| <PC7C><br><PC7F> | 0             | 1                      |
| 0                | Input port    | Output port            |
| 1                | Don't setting | KO8output (Open-drain) |

PC6 setting

|                  |             |              |
|------------------|-------------|--------------|
| <PC6C><br><PC6F> | 0           | 1            |
| 0                | Input port  | Output port  |
| 1                | EA28 output | SPCLK output |

Note 1: A read-modify-write operation cannot be performed for the registers PCCR, PCFC.

Note 2: When setting PC3-PC0 pins to INT3-INT0 input, set PCCR<PC3D: PC0D> to "0000"(prohibit input), and when driving PC3-PC0 pins to "0", execute HALT instruction. This setting generates INT3-INT0 inside. If don't use external interrupt in HALT condition, set like an interrupt don't generated. (e.g. change port setting)

Figure 3.7.25 Register for Port C

### 3.7.10 Port F (PF0 to PF2, PF7)

Ports F0 to F2 are 3-bit general-purpose I/O ports. Each bit can be set individually for input or output. Resetting sets PF0 to PF2 to be input ports. It also sets all bits of the output latch register to “1”. In addition to functioning as general-purpose I/O port pins, PF0 to PF2 can also function as the output for I<sup>2</sup>S0. A pin can be enabled for I/O by writing a “1” to the corresponding bit of the Port F Function Register (PFFC).

Port F7 is a 1-bit general-purpose output port. In addition to functioning as general-purpose output port, PF7 can also function as the SDCLK output. Resetting sets PF7 to be an SDCLK output port.

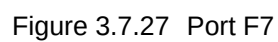
#### (1) Port F0 (I2S0CKO), Port F1 (I2S0DO), Port F2 (I2S0WS)

Ports F0 to F2 are general-purpose I/O port. They also function as either I<sup>2</sup>S. Each pin is detailed below.

|     | I <sup>2</sup> Smode<br>(I2S0Module) |
|-----|--------------------------------------|
| PF0 | I2S0CKO<br>(Clock output)            |
| PF1 | I2S0DO<br>(Data output)              |
| PF2 | I2S0WS<br>(Word-select output)       |



Port F7 is general-purpose output port. In addition to functioning as general-purpose output port, PF7 can also function as the SDCLK output.



|                 |                    |     |   |   |   |   |                                                               |     |     |
|-----------------|--------------------|-----|---|---|---|---|---------------------------------------------------------------|-----|-----|
| Port F register |                    |     |   |   |   |   |                                                               |     |     |
| PF<br>(003CH)   |                    | 7   | 6 | 5 | 4 | 3 | 2                                                             | 1   | 0   |
|                 | bit Symbol         | PF7 |   |   |   |   | PF2                                                           | PF1 | PF0 |
|                 | Read/Write         | R/W |   |   |   |   |                                                               |     |     |
|                 | System Reset State | 1   |   |   |   |   | Data from external port (Output latch register is set to “1”) |     |     |

|                         |                    |   |   |   |   |   |                          |      |      |
|-------------------------|--------------------|---|---|---|---|---|--------------------------|------|------|
| Port F control register |                    |   |   |   |   |   |                          |      |      |
| PFCR<br>(003EH)         |                    | 7 | 6 | 5 | 4 | 3 | 2                        | 1    | 0    |
|                         | bit Symbol         |   |   |   |   |   | PF2C                     | PF1C | PF0C |
|                         | Read/Write         |   |   |   |   |   | W                        |      |      |
|                         | System Reset State |   |   |   |   |   | 0                        | 0    | 0    |
|                         | Function           |   |   |   |   |   | Refer to following table |      |      |

|                          |                    |                     |   |   |   |   |                          |      |      |
|--------------------------|--------------------|---------------------|---|---|---|---|--------------------------|------|------|
| Port F function register |                    |                     |   |   |   |   |                          |      |      |
| PFFC<br>(003FH)          |                    | 7                   | 6 | 5 | 4 | 3 | 2                        | 1    | 0    |
|                          | bit Symbol         | PF7F                |   |   |   |   | PF2F                     | PF1F | PF0F |
|                          | Read/Write         | W                   |   |   |   |   | W                        |      |      |
|                          | System Reset State | 1                   |   |   |   |   | 0                        | 0    | 0    |
|                          | Function           | 0: Port<br>1: SDCLK |   |   |   |   | Refer to following table |      |      |

|                       |                    |                                                     |   |   |   |   |      |      |      |
|-----------------------|--------------------|-----------------------------------------------------|---|---|---|---|------|------|------|
| Port F drive register |                    |                                                     |   |   |   |   |      |      |      |
| PFDR<br>(008FH)       |                    | 7                                                   | 6 | 5 | 4 | 3 | 2    | 1    | 0    |
|                       | bit Symbol         | PF7D                                                |   |   |   |   | PF2D | PF1D | PF0D |
|                       | Read/Write         | R/W                                                 |   |   |   |   | R/W  |      |      |
|                       | System Reset State | 1                                                   |   |   |   |   | 1    | 1    | 1    |
|                       | Function           | Input/Output buffer drive register for standby mode |   |   |   |   |      |      |      |

|                                                                  |               |             |                                                                  |               |             |                                                                  |                |             |
|------------------------------------------------------------------|---------------|-------------|------------------------------------------------------------------|---------------|-------------|------------------------------------------------------------------|----------------|-------------|
| PF2 setting                                                      |               |             | PF1 setting                                                      |               |             | PF0 setting                                                      |                |             |
| <div><div>&lt;PF2C&gt;<br/>&lt;PF2F&gt;</div><div>01</div></div> | 0             | 1           | <div><div>&lt;PF1C&gt;<br/>&lt;PF1F&gt;</div><div>01</div></div> | 0             | 1           | <div><div>&lt;PF0C&gt;<br/>&lt;PF0F&gt;</div><div>01</div></div> | 0              | 1           |
| 0                                                                | Input port    | Output port | 0                                                                | Input port    | Output port | 0                                                                | Input port     | Output port |
| 1                                                                | I2S0WS output |             | 1                                                                | I2S0DO output |             | 1                                                                | I2S0CKO output |             |

Note: A read-modify-write operation cannot be performed for the registers PFCR, PFFC.

Figure 3.7.28 Register for Port F



### 3.7.11 Port G (PG0 to PG5)

PG0 to PG5 are 6-bit input ports and can also be used as the analog input pins for the internal AD converter. PG3 can also be used as the ADTRG pin for the AD converter.

PG2 and PG3 can also be used as the MX and MY pins for a Touch screen interface.

(PG) register is prohibited to access by byte. All the instruction (Arithmetic/Logical/

Bit operation and rotate/shift instruction) accesses by byte are prohibited. Word access is always needed.

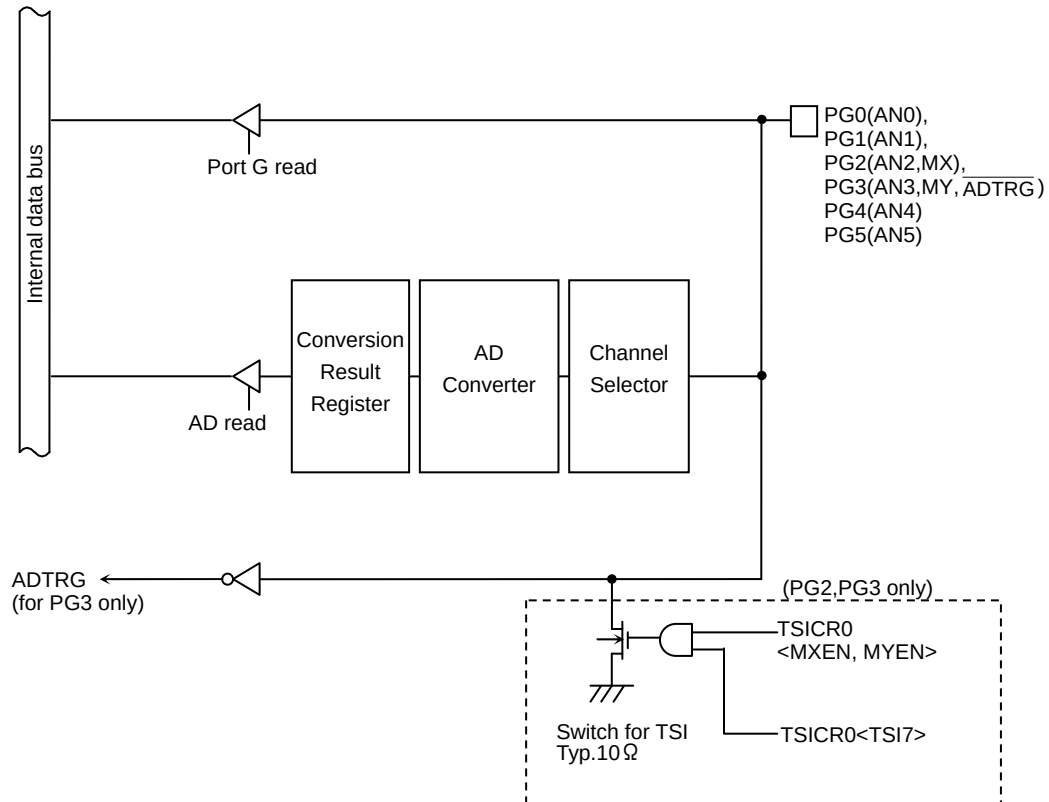


Figure 3.7.29 Port G

| Port G register |                    |   |                         |     |     |     |     |     |
|-----------------|--------------------|---|-------------------------|-----|-----|-----|-----|-----|
|                 | 7                  | 6 | 5                       | 4   | 3   | 2   | 1   | 0   |
| PG<br>(0040H)   | Bit Symbol         |   | PG5                     | PG4 | PG3 | PG2 | PG1 | PG0 |
|                 | Read/Write         |   | R                       |     |     |     |     |     |
|                 | System Reset State |   | Data from external port |     |     |     |     |     |
|                 | Hot Reset State    |   | —                       |     |     |     |     |     |

Note: The input channel selection of the AD converter and the permission of for ADTRG input are set by AD converter mode register ADMOD1.

| Port G Function register |                    |   |   |   |                                     |   |   |   |
|--------------------------|--------------------|---|---|---|-------------------------------------|---|---|---|
|                          | 7                  | 6 | 5 | 4 | 3                                   | 2 | 1 | 0 |
| PGFC<br>(0043H)          | Bit Symbol         |   |   |   | PG3F                                |   |   |   |
|                          | Read/Write         |   |   |   | W                                   |   |   |   |
|                          | System Reset State |   |   |   | 0                                   |   |   |   |
|                          | Hot Reset State    |   |   |   | —                                   |   |   |   |
|                          | Function           |   |   |   | 0: Input port<br>or AN3<br>1: ADTRG |   |   |   |

| Port G driver register |                    |   |   |   |                                                           |      |   |   |
|------------------------|--------------------|---|---|---|-----------------------------------------------------------|------|---|---|
|                        | 7                  | 6 | 5 | 4 | 3                                                         | 2    | 1 | 0 |
| PGDR<br>(0090H)        | Bit Symbol         |   |   |   | PG3D                                                      | PG2D |   |   |
|                        | Read/Write         |   |   |   | R/W                                                       |      |   |   |
|                        | System Reset State |   |   |   | 1                                                         | 1    |   |   |
|                        | Hot Reset State    |   |   |   | —                                                         | —    |   |   |
|                        | Function           |   |   |   | Input/Output buffer<br>drive register for<br>standby mode |      |   |   |

Note : A read-modify-write operation cannot be performed for the registers PGFC.

Figure 3.7.30 Register for Port G

### 3.7.12 Port J (PJ0 to PJ7)

PJ0 to PJ4 and PJ7 are 6-bit output port. Resetting sets the output latch PJ to “1”, and they output “1”. PJ5 to PJ6 are 2-bit input/output port. In addition to functioning as a port, Port J also functions as output pins for SDRAM ( $\overline{\text{SDRAS}}$ ,  $\overline{\text{SDCAS}}$ ,  $\overline{\text{SDWE}}$ ,  $\overline{\text{SDLLDQM}}$ ,  $\overline{\text{SDLUDQM}}$ , and  $\overline{\text{SDCKE}}$ ), SRAM ( $\overline{\text{SRWR}}$ ,  $\overline{\text{SRLLB}}$ ,  $\overline{\text{SRLUB}}$ ,  $\overline{\text{SRULB}}$  and  $\overline{\text{SRUUB}}$ ) and NAND-Flash(NDALE and NDCLE).

The above settings are made using the function register PJFC.

However, either SDRAM or SRAM output signal for PJ0 to PJ2 are selected automatically according to the setting of the memory controller.

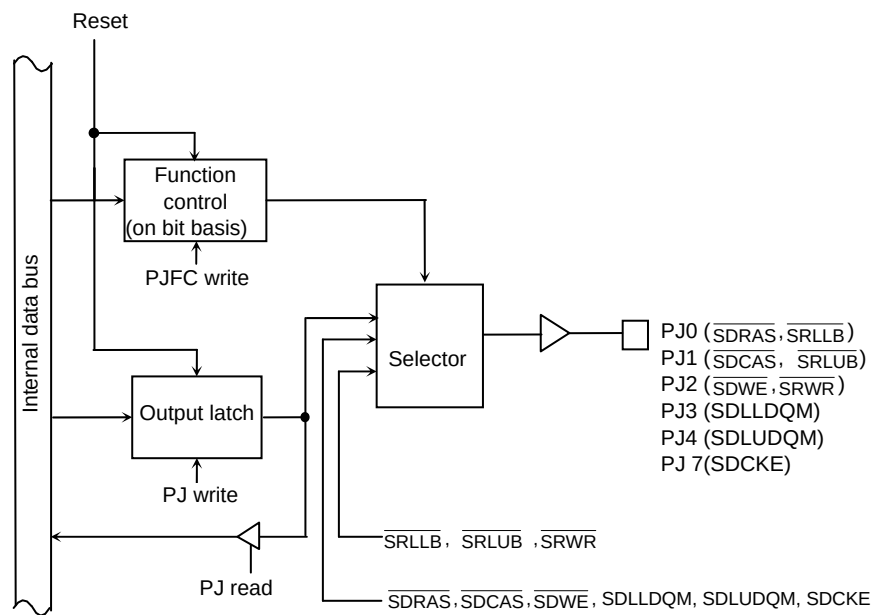


Figure 3.7.31 Port J0 to J4 and J7

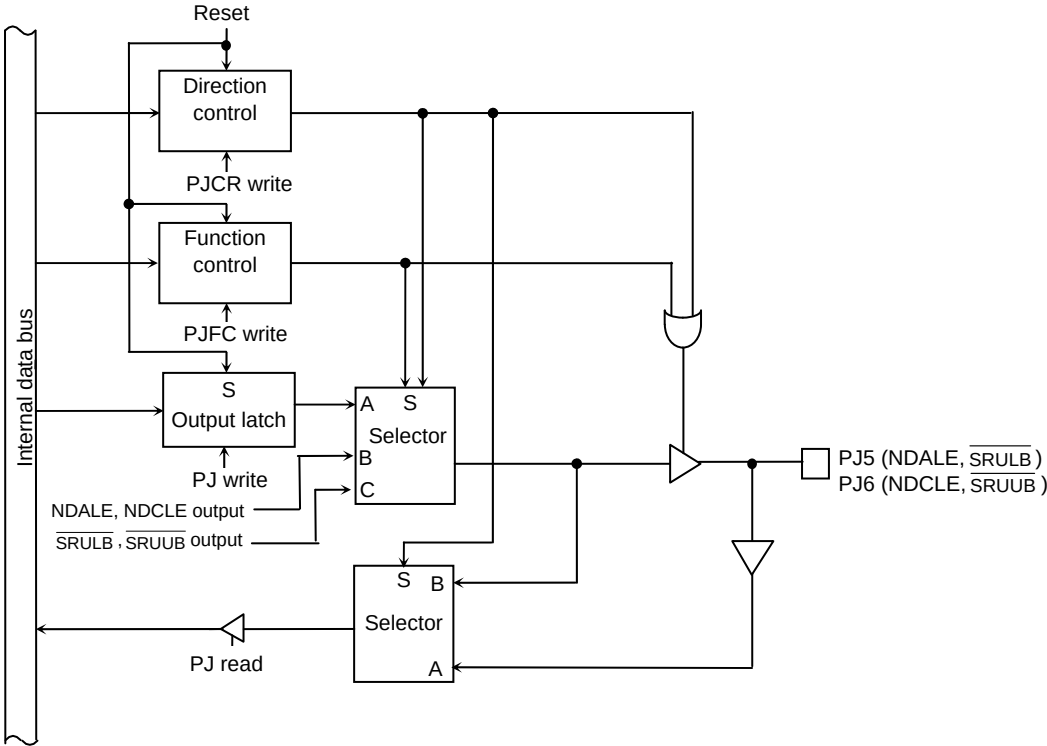


Figure 3.7.32 Port J5,J6

|                 |                    |     |                                                                  |     |     |     |     |     |     |
|-----------------|--------------------|-----|------------------------------------------------------------------|-----|-----|-----|-----|-----|-----|
| Port J register |                    |     |                                                                  |     |     |     |     |     |     |
| PJ<br>(004CH)   |                    | 7   | 6                                                                | 5   | 4   | 3   | 2   | 1   | 0   |
|                 | bit Symbol         | PJ7 | PJ6                                                              | PJ5 | PJ4 | PJ3 | PJ2 | PJ1 | PJ0 |
|                 | Read/Write         | R/W |                                                                  |     |     |     |     |     |     |
|                 | System Reset State | 1   | Data from external port<br>(Output latch register is set to “1”) |     | 1   | 1   | 1   | 1   | 1   |

|                         |                    |   |                     |      |   |   |   |   |   |
|-------------------------|--------------------|---|---------------------|------|---|---|---|---|---|
| Port J control register |                    |   |                     |      |   |   |   |   |   |
| PJCR<br>(004EH)         |                    | 7 | 6                   | 5    | 4 | 3 | 2 | 1 | 0 |
|                         | bit Symbol         |   | PJ6C                | PJ5C |   |   |   |   |   |
|                         | Read/Write         |   | W                   |      |   |   |   |   |   |
|                         | System Reset State |   | 0                   | 0    |   |   |   |   |   |
|                         | Function           |   | 0: Input, 1: Output |      |   |   |   |   |   |

|                          |                    |                     |                          |      |                       |                       |                                                                      |                                                                        |                                                                        |
|--------------------------|--------------------|---------------------|--------------------------|------|-----------------------|-----------------------|----------------------------------------------------------------------|------------------------------------------------------------------------|------------------------------------------------------------------------|
| Port J function register |                    |                     |                          |      |                       |                       |                                                                      |                                                                        |                                                                        |
| PJFC<br>(004FH)          |                    | 7                   | 6                        | 5    | 4                     | 3                     | 2                                                                    | 1                                                                      | 0                                                                      |
|                          | bit Symbol         | PJ7F                | PJ6F                     | PJ5F | PJ4F                  | PJ3F                  | PJ2F                                                                 | PJ1F                                                                   | PJ0F                                                                   |
|                          | Read/Write         | W                   |                          |      |                       |                       |                                                                      |                                                                        |                                                                        |
|                          | System Reset State | 0                   | 0                        | 0    | 0                     | 0                     | 0                                                                    | 0                                                                      | 0                                                                      |
|                          | Function           | 0: Port<br>1: SDCKE | Refer to following table |      | 0: Port<br>1: SDLUDQM | 0: Port<br>1: SDLLDQM | 0: Port<br>1: $\overline{\text{SDWE}}$ ,<br>$\overline{\text{SRWR}}$ | 0: Port<br>1: $\overline{\text{SDCAS}}$ ,<br>$\overline{\text{SRLUB}}$ | 0: Port<br>1: $\overline{\text{SDRAS}}$ ,<br>$\overline{\text{SRLLB}}$ |

|                       |                    |                                                     |      |      |      |      |      |      |      |
|-----------------------|--------------------|-----------------------------------------------------|------|------|------|------|------|------|------|
| Port J drive register |                    |                                                     |      |      |      |      |      |      |      |
| PJDR<br>(0093H)       |                    | 7                                                   | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|                       | bit Symbol         | PJ7D                                                | PJ6D | PJ5D | PJ4D | PJ3D | PJ2D | PJ1D | PJ0D |
|                       | Read/Write         | R/W                                                 |      |      |      |      |      |      |      |
|                       | System Reset State | 1                                                   | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
|                       | Function           | Input/Output buffer drive register for standby mode |      |      |      |      |      |      |      |

|             |        |              |              |  |        |              |              |
|-------------|--------|--------------|--------------|--|--------|--------------|--------------|
| PJ6 setting |        |              | PJ5 setting  |  |        |              |              |
|             | <PJ6C> | 0            | 1            |  | <PJ5C> | 0            | 1            |
|             | <PJ6F> |              |              |  | <PJ5F> |              |              |
|             | 0      | Input port   | Output port  |  | 0      | Input port   | Output port  |
|             | 1      | SRUUB output | NDCLE output |  | 1      | SRULB output | NDALE output |

Note: A read-modify-write operation cannot be performed for the registers PJCR and PJFC.

Figure 3.7.33 Register for Port J

### 3.7.13 Port K (PK0 to PK7)

PK0 to PK7 are 8-bit output ports. Resetting sets the output latch PK to “0”, and PK0 to PK7 pins output “0”.

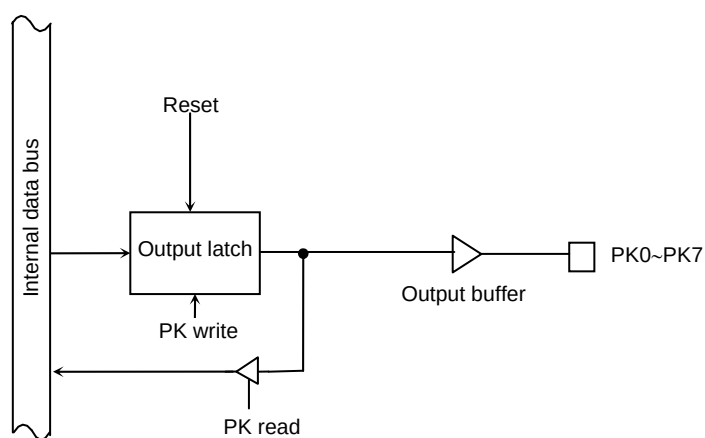


Figure 3.7.34 Port K0 to K7



### 3.7.14 Port L (PL0 to PL7)

PL0 to PL7 are 8-bit output ports. Resetting sets the output latch PL to “0”, and PL0 to PL7 pins output “0”. In addition to functioning as a general-purpose output port, port L can also function as a data bus for 32-bit memory connection (D16 to D23). Above setting is used the function register PLFC.

Setting the AM1 and AM0 pins as shown below and resetting the device initialize port 1 to the following function pins:

| AM1 | AM0 | Function Setting after reset is released |
|-----|-----|------------------------------------------|
| 0   | 0   | Don't use this setting                   |
| 0   | 1   | Input port (PL0 ~ PL7)                   |
| 1   | 0   | Data bus (D16 ~ D23)                     |
| 1   | 1   | Don't use this setting                   |

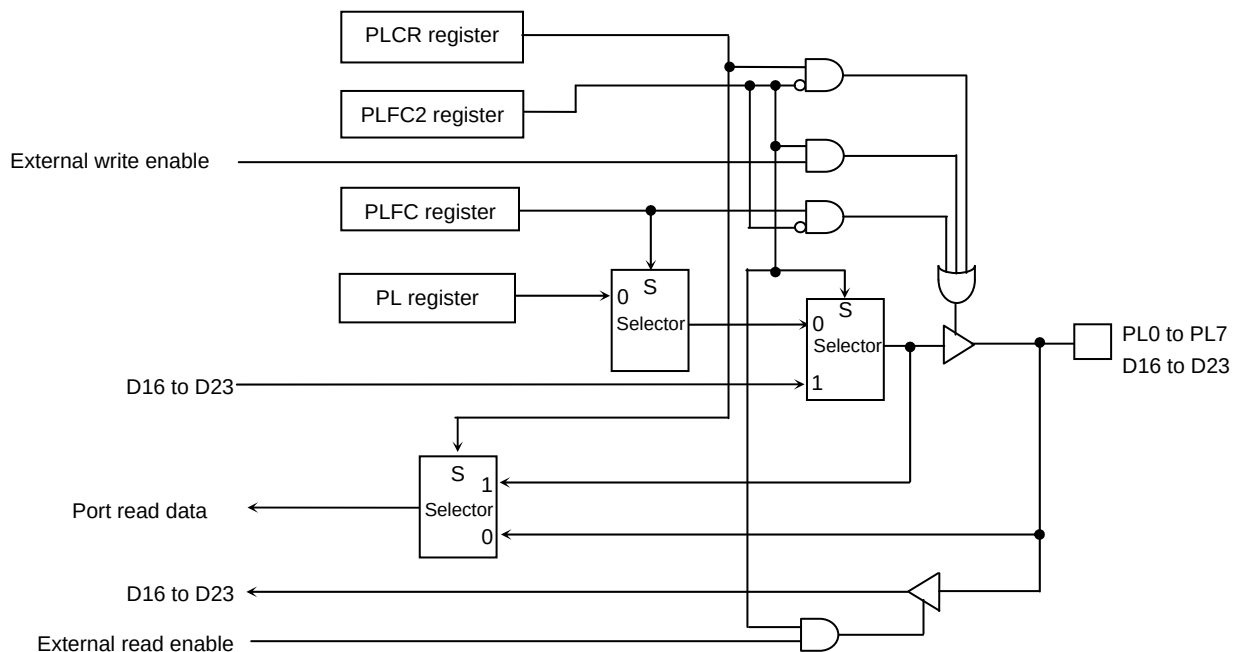


Figure 3.7.36 Port L0 to L7



| Port L register |                    |     |     |     |     |     |     |     |     |
|-----------------|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| PL<br>(0054H)   |                    | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|                 | bit Symbol         | PL7 | PL6 | PL5 | PL4 | PL3 | PL2 | PL1 | PL0 |
|                 | Read/Write         | R/W |     |     |     |     |     |     |     |
|                 | System Reset State | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

| Port L control register |                    |                       |      |      |      |      |      |      |      |
|-------------------------|--------------------|-----------------------|------|------|------|------|------|------|------|
| PLCR<br>(0056H)         |                    | 7                     | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|                         | bit Symbol         | PL7C                  | PL6C | PL5C | PL4C | PL3C | PL2C | PL1C | PL0C |
|                         | Read/Write         | W                     |      |      |      |      |      |      |      |
|                         | System Reset State | 0                     | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| Function                |                    | 0: Input    1: Output |      |      |      |      |      |      |      |

| Port L function register |                    |                             |      |      |      |      |      |      |      |
|--------------------------|--------------------|-----------------------------|------|------|------|------|------|------|------|
| PLFC<br>(0057H)          |                    | 7                           | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|                          | bit Symbol         | PL7F                        | PL6F | PL5F | PL4F | PL3F | PL2F | PL1F | PL0F |
|                          | Read/Write         | W                           |      |      |      |      |      |      |      |
|                          | System Reset State | 0                           | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| Function                 |                    | 0: Port    1: Don't setting |      |      |      |      |      |      |      |

| Port L function register 2 |                    |   |   |   |   |   |   |   |                                     |
|----------------------------|--------------------|---|---|---|---|---|---|---|-------------------------------------|
| PLFC2<br>(0055H)           |                    | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0                                   |
|                            | bit Symbol         |   |   |   |   |   |   |   | PL0F2                               |
|                            | Read/Write         |   |   |   |   |   |   |   | W                                   |
|                            | System Reset State |   |   |   |   |   |   |   | 0/1                                 |
| Function                   |                    |   |   |   |   |   |   |   | 0: Port<br>1: Data bus<br>(D16~D23) |

| Port L drive register |                    |                                                     |      |      |      |      |      |      |      |
|-----------------------|--------------------|-----------------------------------------------------|------|------|------|------|------|------|------|
| PLDR<br>(0095H)       |                    | 7                                                   | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|                       | bit Symbol         | PL7D                                                | PL6D | PL5D | PL4D | PL3D | PL2D | PL1D | PL0D |
|                       | Read/Write         | R/W                                                 |      |      |      |      |      |      |      |
|                       | System Reset State | 1                                                   | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| Function              |                    | Input/Output buffer drive register for standby mode |      |      |      |      |      |      |      |

Note: A read-modify-write operation cannot be performed for the registers PLCR, PLFC and PLFC2.

|               |               | <PL0F2>=0   |          | <PL0F2>=1 |  |
|---------------|---------------|-------------|----------|-----------|--|
| <PLnF>\<PLnC> | 0             | 1           | 0        | 1         |  |
| 0             | Input port    | Output port | Data Bus |           |  |
| 1             | Don't setting |             |          |           |  |

Figure 3.7.37 Register for Port L

### 3.7.15 Port M (PM1, PM2, PM7)

PM1, PM2 and PM7 are 3-bit output ports. Resetting sets the output latch PM to “1”, and PM1, PM2 and PM7 pins output “1”.

In addition to functioning as an output ports, port M also functions as output pin for the timers (TA1OUT), output pins for the RTC alarm ( $\overline{\text{ALARM}}$ ), and as the output pin for the melody/alarm generator (MLDALM,  $\overline{\text{MLDALM}}$ ). The above settings are made using the function register PMFC.

PM1 has two output function which MLDALM and TA1OUT, and PM2 has two output functions  $\overline{\text{ALARM}}$  and  $\overline{\text{MLDALM}}$ . These are selected using PM<PM1>, PM<PM2>.

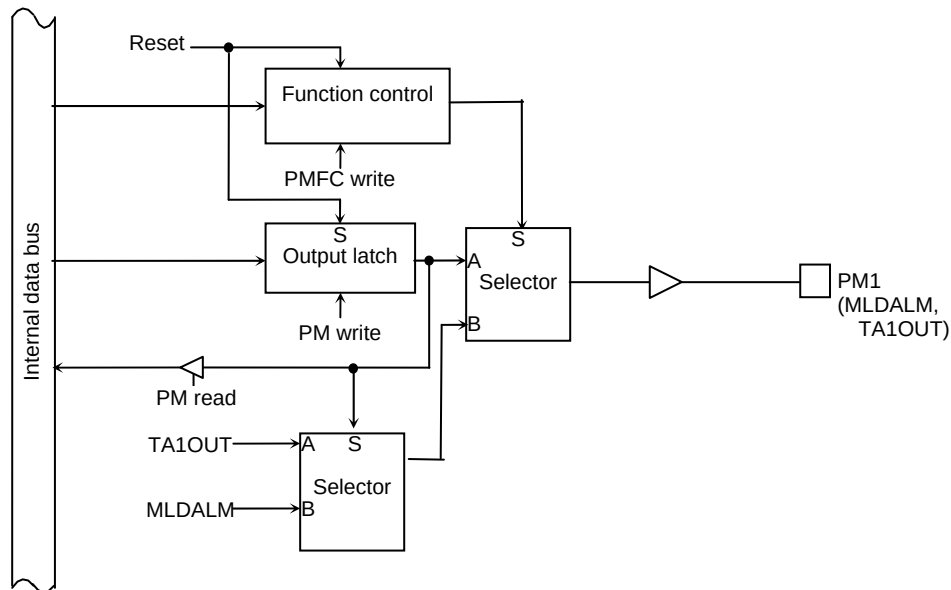


Figure 3.7.38 Port M1

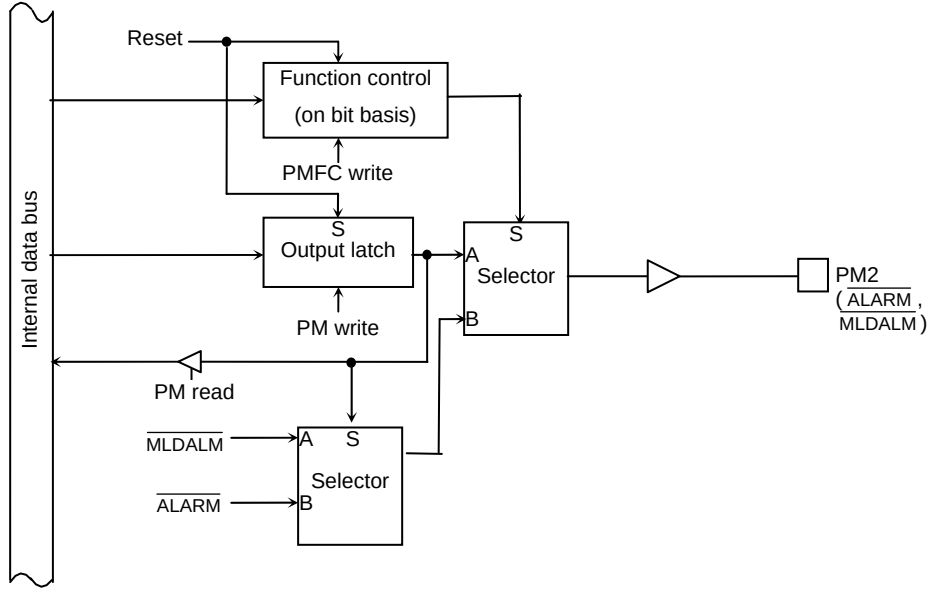


Figure 3.7.39 Port M2

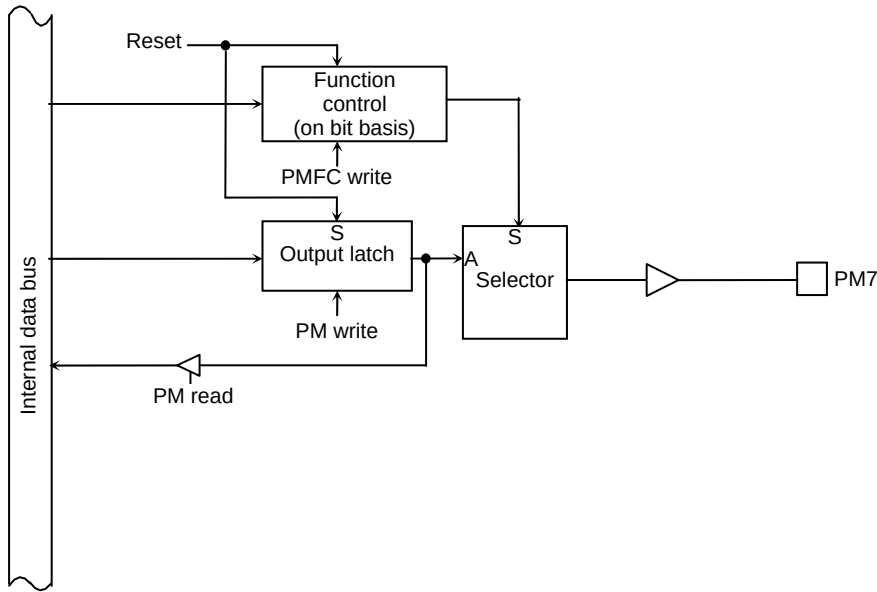


Figure 3.7.40 Port M7

| Port M register          |                    |                                                                        |   |   |   |                                                               |                                                                   |   |
|--------------------------|--------------------|------------------------------------------------------------------------|---|---|---|---------------------------------------------------------------|-------------------------------------------------------------------|---|
|                          | 7                  | 6                                                                      | 5 | 4 | 3 | 2                                                             | 1                                                                 | 0 |
| PM<br>(0058H)            | bit Symbol         | PM7                                                                    |   |   |   | PM2                                                           | PM1                                                               |   |
|                          | Read/Write         | R/W                                                                    |   |   |   | R/W                                                           |                                                                   |   |
|                          | System Reset State | 1                                                                      |   |   |   | 1                                                             | 1                                                                 |   |
| Port M function register |                    |                                                                        |   |   |   |                                                               |                                                                   |   |
|                          | 7                  | 6                                                                      | 5 | 4 | 3 | 2                                                             | 1                                                                 | 0 |
| PMFC<br>(005BH)          | bit Symbol         | PM7F                                                                   |   |   |   | PM2F                                                          | PM1F                                                              |   |
|                          | Read/Write         | W                                                                      |   |   |   | W                                                             |                                                                   |   |
|                          | System Reset State | 0                                                                      |   |   |   | 0                                                             | 0                                                                 |   |
|                          | Function           | 0: Port<br>1: Don't<br>setting                                         |   |   |   | 0: Port<br>1: ALARM at<br><PM2>=1,<br>MLDALM<br>at<br><PM2>=0 | 0: Port<br>1: MLDALM<br>at<br><PM1>=1,<br>TA1OUT<br>at<br><PM1>=0 |   |
| Port M drive register    |                    |                                                                        |   |   |   |                                                               |                                                                   |   |
|                          | 7                  | 6                                                                      | 5 | 4 | 3 | 2                                                             | 1                                                                 | 0 |
| PMDR<br>(0096H)          | bit Symbol         | PM7D                                                                   |   |   |   | PM2D                                                          | PM1D                                                              |   |
|                          | Read/Write         | R/W                                                                    |   |   |   | R/W                                                           |                                                                   |   |
|                          | System Reset State | 1                                                                      |   |   |   | 1                                                             | 1                                                                 |   |
| PMDR<br>(0096H)          | Function           | Input<br>/Output<br>buffer<br>drive<br>register for<br>standby<br>mode |   |   |   | Input/Output buffer<br>drive register for<br>standby mode     |                                                                   |   |

Note: A read-modify-write operation cannot be performed for the registers PMFC.

Figure 3.7.41 Register for Port M

### 3.7.16 Port N (PN0 to PN7)

PN0 to PN7 are 8-bit general-purpose I/O port. Each bit can be set individually for input or output. Resetting sets Port N to an input port.

In addition to functioning as a general-purpose I/O port, Port N can also function as key-board interface pin (KO0 to KO7) which can be set to open-drain output buffer.

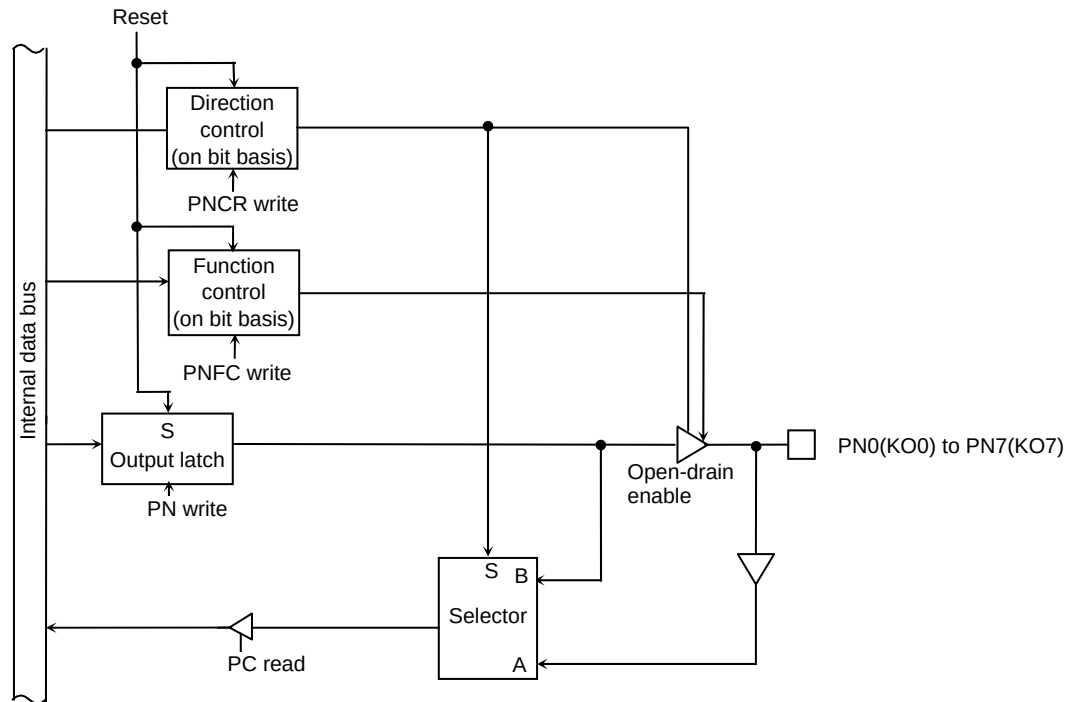


Figure 3.7.42 Port N

Port N register

|               |                    |                                                               |     |     |     |     |     |     |     |
|---------------|--------------------|---------------------------------------------------------------|-----|-----|-----|-----|-----|-----|-----|
| PN<br>(005CH) |                    | 7                                                             | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|               | bit Symbol         | PN7                                                           | PN6 | PN5 | PN4 | PN3 | PN2 | PN1 | PN0 |
|               | Read/Write         | R/W                                                           |     |     |     |     |     |     |     |
|               | System Reset State | Data from external port (Output latch register is set to “1”) |     |     |     |     |     |     |     |

Port N control register

|                 |                    |                         |      |      |      |      |      |      |      |
|-----------------|--------------------|-------------------------|------|------|------|------|------|------|------|
| PNCR<br>(005EH) |                    | 7                       | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|                 | bit Symbol         | PN7C                    | PN6C | PN5C | PN4C | PN3C | PN2C | PN1C | PN0C |
|                 | Read/Write         | W                       |      |      |      |      |      |      |      |
|                 | System Reset State | 0                       | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
|                 | Function           | 0: Input      1: Output |      |      |      |      |      |      |      |

Port N function register

|                 |                    |                                        |      |      |      |      |      |      |      |
|-----------------|--------------------|----------------------------------------|------|------|------|------|------|------|------|
| PNFC<br>(005FH) |                    | 7                                      | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|                 | bit Symbol         | PN7F                                   | PN6F | PN5F | PN4F | PN3F | PN2F | PN1F | PN0F |
|                 | Read/Write         | W                                      |      |      |      |      |      |      |      |
|                 | System Reset State | 0                                      | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
|                 | Function           | 0: CMOS output    1: Open-drain output |      |      |      |      |      |      |      |

Port N drive register

|                 |                    |                                                     |      |      |      |      |      |      |      |
|-----------------|--------------------|-----------------------------------------------------|------|------|------|------|------|------|------|
| PNDR<br>(0097H) |                    | 7                                                   | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|                 | bit Symbol         | PN7D                                                | PN6D | PN5D | PN4D | PN3D | PN2D | PN1D | PN0D |
|                 | Read/Write         | R/W                                                 |      |      |      |      |      |      |      |
|                 | System Reset State | 1                                                   | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
|                 | Function           | Input/Output buffer drive register for standby mode |      |      |      |      |      |      |      |

Note : A read-modify-write operation cannot be performed for the registers PNCR and PNFC.

Figure 3.7.43 Register for Port N

### 3.7.17 Port P (PP3 to PP7)

Ports P3 to P5 are 3-bit general-purpose I/O ports. Each bit can be set individually for input or output. Resetting sets port P3 to P5 to input port and output latch to “0”.

In addition to functioning as general-purpose I/O port, P3 to P5 can also function as an output pin for timer (TA7OUT), as an input pin for timers (TB0IN0, TB1IN0), and as an input pin for external interruption (INT5 to INT7), serial transfer SIO0 (TXD0, RXD0, SCLK0,  $\overline{\text{CTS0}}$ ), SIO1 (TXD1, RXD1, SCLK1,  $\overline{\text{CTS1}}$ ).

Port P6 is 1-bit output port. Resetting sets output latch to “0”.

In addition to functioning as an output port, PP6 and PP7 can also function as an output pin for timer (TB0OUT0).

Setting in the corresponding bits of PPCR and PPFC enables the respective functions.

The edge select for external interruption is determined by the IIMC register in the interruption controller.

In port setting, if 16 bit timer input is selected and capture control is executed, INT6 and INT7 don't depend on IIMC1 register setting. INT6 and INT7 operate by setting TBNMOD<TBNCPM1:0>.

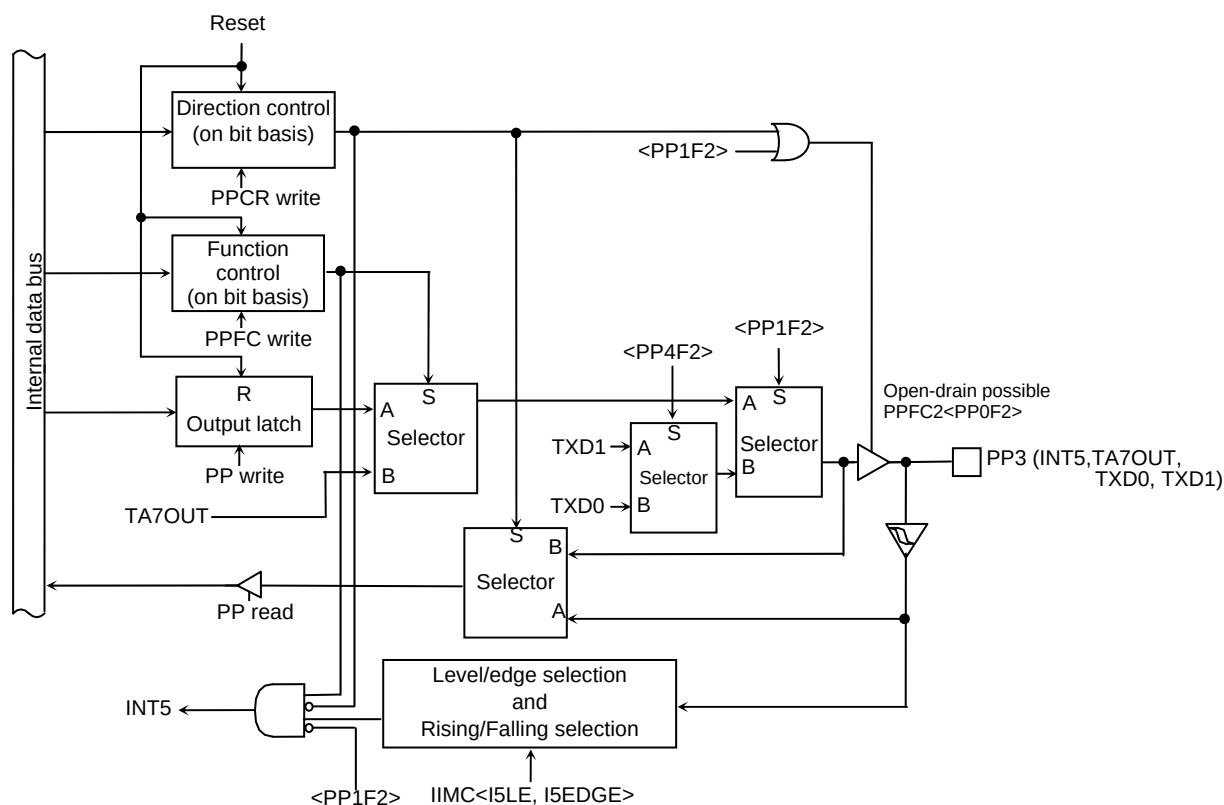


Figure 3.7.44 Port P3

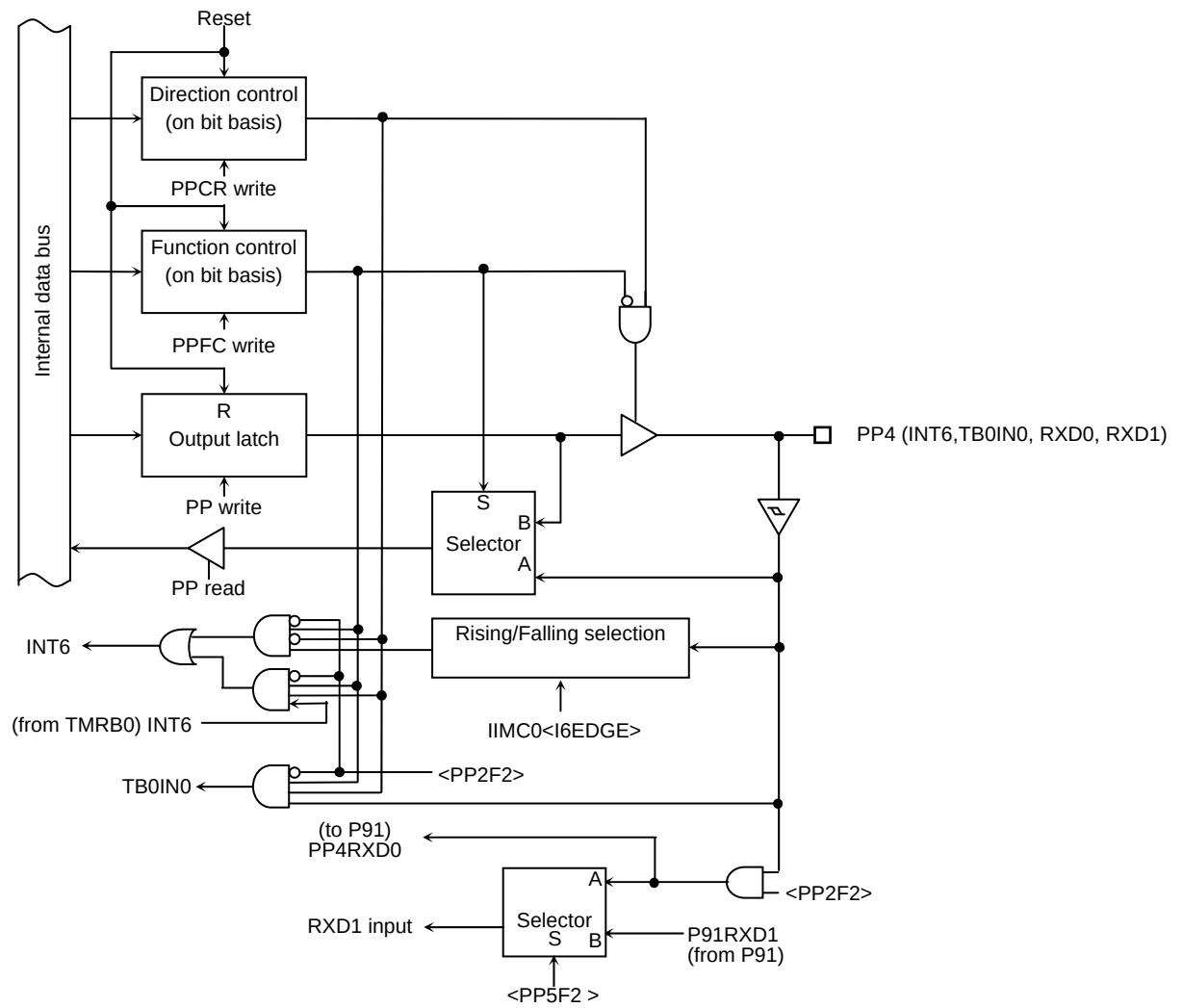


Figure 3.7.45 Port P4



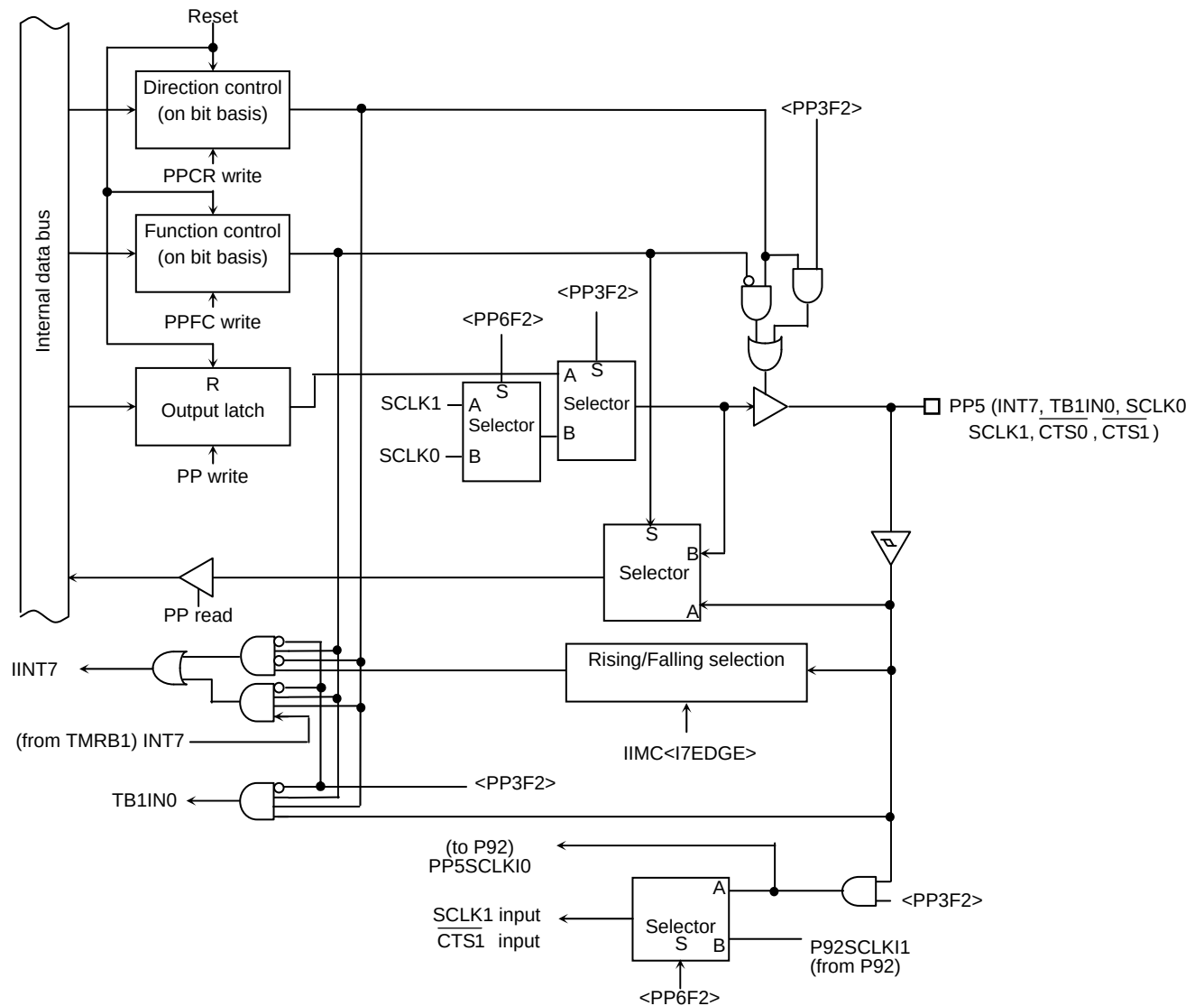


Figure 3.7.46 Port P5

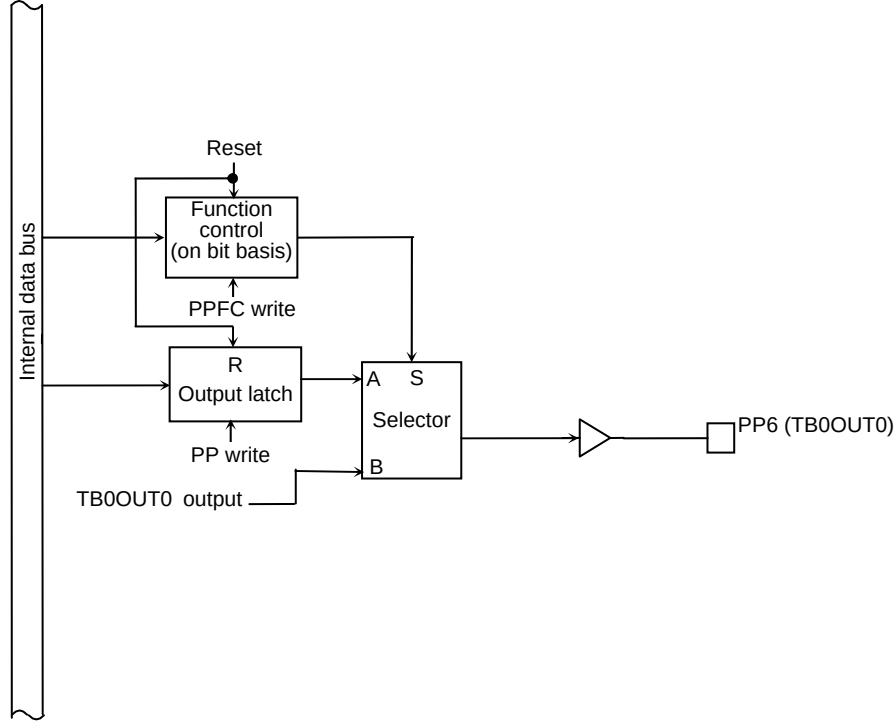


Figure 3.7.47 Port P6

Port P register

|               |                    | 7 | 6   | 5                                                                 | 4   | 3   | 2 | 1 | 0 |
|---------------|--------------------|---|-----|-------------------------------------------------------------------|-----|-----|---|---|---|
| PP<br>(0060H) | bit Symbol         |   | PP6 | PP5                                                               | PP4 | PP3 |   |   |   |
|               | Read/Write         |   | R/W |                                                                   |     |     |   |   |   |
|               | System Reset State |   | 0   | Data from external port (Output latch register is cleared to "0") |     |     |   |   |   |

Port P control register

|                 |                    | 7 | 6 | 5                  | 4    | 3    | 2 | 1 | 0 |
|-----------------|--------------------|---|---|--------------------|------|------|---|---|---|
| PPCR<br>(0062H) | bit Symbol         |   |   | PP5C               | PP4C | PP3C |   |   |   |
|                 | Read/Write         |   |   | W                  |      |      |   |   |   |
|                 | System Reset State |   |   | 0                  | 0    | 0    |   |   |   |
|                 | Function           |   |   | 0: Input 1: Output |      |      |   |   |   |

Port P function register

|                 |                    | 7 | 6                   | 5                        | 4    | 3    | 2 | 1 | 0 |
|-----------------|--------------------|---|---------------------|--------------------------|------|------|---|---|---|
| PPFC<br>(0063H) | bit Symbol         |   | PP6F                | PP5F                     | PP4F | PP3F |   |   |   |
|                 | Read/Write         |   | W                   |                          |      |      |   |   |   |
|                 | System Reset State |   | 0                   | 0                        | 0    | 0    |   |   |   |
|                 | Function           |   | 0:Port<br>1:TB0OUT0 | Refer to following table |      |      |   |   |   |

Port P drive register

|                 |                    | 7 | 6                                                   | 5    | 4    | 3    | 2 | 1 | 0 |
|-----------------|--------------------|---|-----------------------------------------------------|------|------|------|---|---|---|
| PPDR<br>(0098H) | bit Symbol         |   | PP6D                                                | PP5D | PP4D | PP3D |   |   |   |
|                 | Read/Write         |   | R/W                                                 |      |      |      |   |   |   |
|                 | System Reset State |   | 1                                                   | 1    | 1    | 1    |   |   |   |
|                 | Function           |   | Input/Output buffer drive register for standby mode |      |      |      |   |   |   |

| Port P Function register 2 |                       |                                                                                                     |                                              |                                        |                                                                                 |                                                  |                                                   |                                                  |
|----------------------------|-----------------------|-----------------------------------------------------------------------------------------------------|----------------------------------------------|----------------------------------------|---------------------------------------------------------------------------------|--------------------------------------------------|---------------------------------------------------|--------------------------------------------------|
|                            | 7                     | 6                                                                                                   | 5                                            | 4                                      | 3                                                                               | 2                                                | 1                                                 | 0                                                |
| PPFC2<br>(0061H)           | bit Symbol            | PP6F2                                                                                               | PP5F2                                        | PP4F2                                  | PP3F2                                                                           | PP2F2                                            | PP1F2                                             | PP0F2                                            |
|                            | Read/Write            | W                                                                                                   |                                              |                                        |                                                                                 |                                                  |                                                   |                                                  |
|                            | System<br>Reset State | 0                                                                                                   | 0                                            | 0                                      | 0                                                                               | 0                                                | 0                                                 | 0                                                |
|                            | Function              | PP5<br>SCLK<br>output<br>0: SCLK1<br>1: SCLK0<br><br>SIO1<br>SCLK,<br>CTS input<br>0: PP5<br>1: P92 | SIO1<br>RXD<br>selection<br>0: PP4<br>1: P91 | PP3<br>selection<br>0: TXD1<br>1: TXD0 | PP5<br>selection<br>0: Others<br>1: SCLK,<br>CTS in<br>put or<br>SCLK<br>output | PP4<br>selection<br>0: Others<br>1: RXD<br>input | PP3<br>selection<br>0: Others<br>1: TXD<br>output | PP3<br>selection<br>0: CMOS<br>1: Open<br>-drain |

PP3 setting (&lt;PP1F2&gt;=0)

| <PP3C><br><PP3F> | 0          | 1                |
|------------------|------------|------------------|
| 0                | Input port | Output port      |
| 1                | INT5 input | TA7OUT<br>output |

PP4 setting (&lt;PP2F2&gt;=0)

| <PP4C><br><PP4F> | 0          | 1               |
|------------------|------------|-----------------|
| 0                | Input port | Output port     |
| 1                | INT5 input | TB0IN0<br>input |

PP5 setting (&lt;PP3F2&gt;=0)

| <PP5C><br><PP5F> | 0          | 1               |
|------------------|------------|-----------------|
| 0                | Input port | Output port     |
| 1                | INT7 input | TB1IN0<br>input |

Note1: When setting <PP3F2, PP2F2, PP1F2> = "1", PP3~PP5 pins are set to SIO0 or SIO1 functions regardless PPCR, PPFC setting. PP3 is set to TXD, PP4 is set to RXD. PP5 is set to SCLK input or CTS input when <PP5C>=0. PP5 is set to SCLK output when <PP5C>=1.

Note2: A read-modify-write operation cannot be performed for the registers PPCR, PPFC.

Note3: When setting PP5, PP4, PP3 pins to INT7,INT6,INT5 input, set PPDR<PP5D:3D> to "0000" (prohibit input), and when driving PP5,PP4,PP3 pins to "0", execute HALT instruction. This setting generates INT7, INT6, and INT5 inside. If don't using external interrupt in HALT condition, set like an interrupt don't generated.

Figure 3.7.48 Register for Port P

### 3.7.18 Port R (R0 to R3)

Ports R0 to R3 are 4-bit general-purpose I/O ports. Each bit can be set individually for input or output. Resetting sets port R0 to R3 to input port and output latch to “0”.

In addition to functioning as general-purpose I/O port, PR0 to PR3 can also function as the SPI controller pin (SPCLK,  $\overline{\text{SPCS}}$ , SPDO and SPDI).

Setting in the corresponding bits of PFCR and PFFC enables the respective functions.

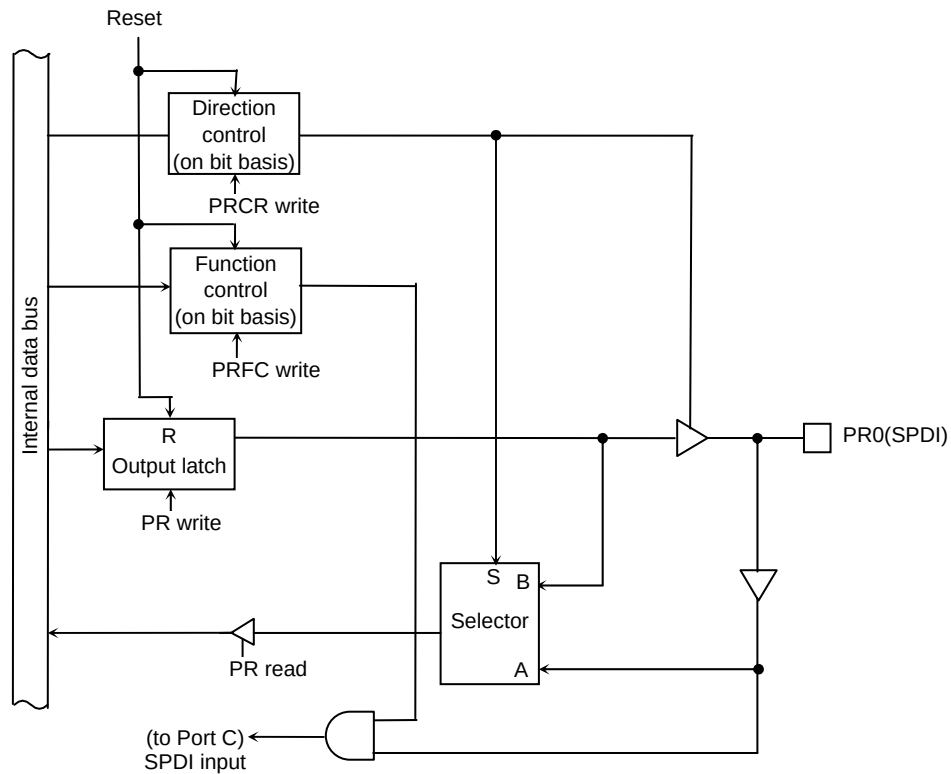


Figure 3.7.49 Port R0

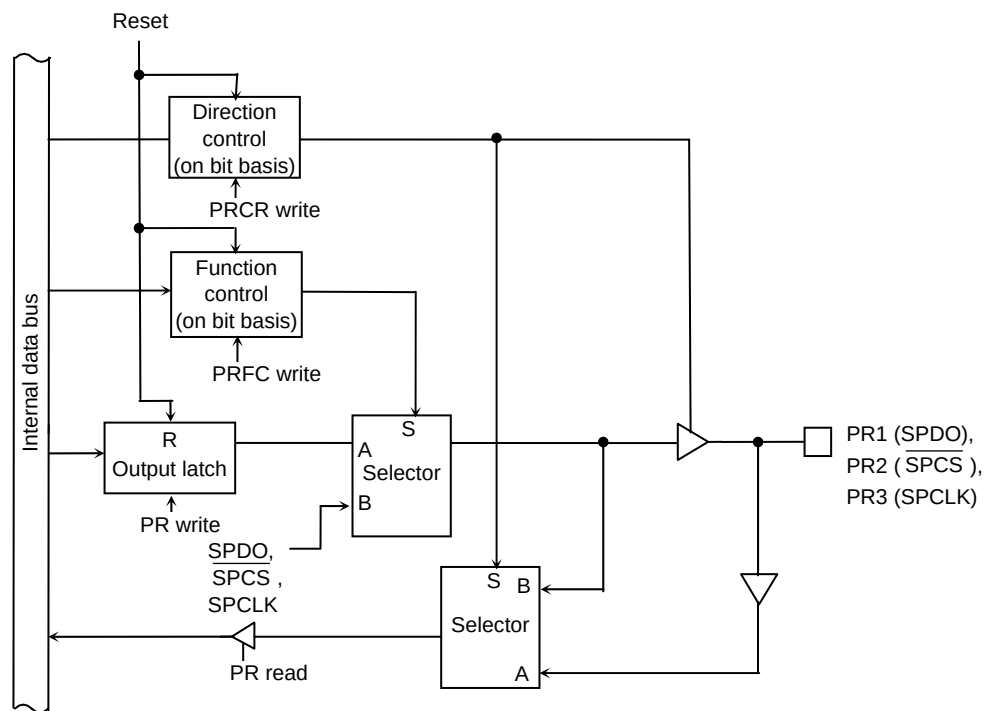


Figure 3.7.50 Port R1 to R3

| Port R register |                    |   |   |   |   |                                                                      |     |     |     |
|-----------------|--------------------|---|---|---|---|----------------------------------------------------------------------|-----|-----|-----|
| PR<br>(0064H)   |                    | 7 | 6 | 5 | 4 | 3                                                                    | 2   | 1   | 0   |
|                 | bit Symbol         |   |   |   |   | PR3                                                                  | PR2 | PR1 | PR0 |
|                 | Read/Write         |   |   |   |   | R/W                                                                  |     |     |     |
|                 | System Reset State |   |   |   |   | Data from external port<br>(Output latch register is cleared to "0") |     |     |     |

| Port R control register |                    |   |   |   |   |                     |      |      |      |
|-------------------------|--------------------|---|---|---|---|---------------------|------|------|------|
| PRCR<br>(0066H)         |                    | 7 | 6 | 5 | 4 | 3                   | 2    | 1    | 0    |
|                         | bit Symbol         |   |   |   |   | PR3C                | PR2C | PR1C | PR0C |
|                         | Read/Write         |   |   |   |   | W                   |      |      |      |
|                         | System Reset State |   |   |   |   | 0                   | 0    | 0    | 0    |
|                         | Function           |   |   |   |   | 0: Input, 1: Output |      |      |      |

| Port R function register |                    |   |   |   |   |                     |                    |                    |                    |
|--------------------------|--------------------|---|---|---|---|---------------------|--------------------|--------------------|--------------------|
| PRFC<br>(0067H)          |                    | 7 | 6 | 5 | 4 | 3                   | 2                  | 1                  | 0                  |
|                          | bit Symbol         |   |   |   |   | PR3F                | PR2F               | PR1F               | PR0F               |
|                          | Read/Write         |   |   |   |   | W                   |                    |                    |                    |
|                          | System Reset State |   |   |   |   | 0                   | 0                  | 0                  | 0                  |
|                          | Function           |   |   |   |   | 0: Port<br>1: SPCLK | 0: Port<br>1: SPCS | 0: Port<br>1: SPDO | 0: Port<br>1: SPDI |

| Port R drive register |                    |   |   |   |   |                                                        |      |      |      |
|-----------------------|--------------------|---|---|---|---|--------------------------------------------------------|------|------|------|
| PRDR<br>(0099H)       |                    | 7 | 6 | 5 | 4 | 3                                                      | 2    | 1    | 0    |
|                       | bit Symbol         |   |   |   |   | PR3D                                                   | PR2D | PR1D | PR0D |
|                       | Read/Write         |   |   |   |   | R/W                                                    |      |      |      |
|                       | System Reset State |   |   |   |   | 1                                                      | 1    | 1    | 1    |
|                       | Function           |   |   |   |   | Input/Output buffer drive register<br>for standby mode |      |      |      |

|                                                                             |            |             |                                                                             |            |             |
|-----------------------------------------------------------------------------|------------|-------------|-----------------------------------------------------------------------------|------------|-------------|
| PR1 setting                                                                 |            |             | PR0 setting                                                                 |            |             |
| <div><div>&lt;PR1C&gt;<br/>&lt;PR1F&gt;</div><div>0</div><div>1</div></div> | 0          | 1           | <div><div>&lt;PR0C&gt;<br/>&lt;PR0F&gt;</div><div>0</div><div>1</div></div> | 0          | 1           |
|                                                                             | Input port | Output port |                                                                             | Input port | Output port |
|                                                                             | Reserved   | SPDO output |                                                                             | SPDI input | Reserved    |

|                                                                             |            |              |                                                                             |            |             |
|-----------------------------------------------------------------------------|------------|--------------|-----------------------------------------------------------------------------|------------|-------------|
| PR3setting                                                                  |            |              | PR2 setting                                                                 |            |             |
| <div><div>&lt;PR3C&gt;<br/>&lt;PR3F&gt;</div><div>0</div><div>1</div></div> | 0          | 1            | <div><div>&lt;PR2C&gt;<br/>&lt;PR2F&gt;</div><div>0</div><div>1</div></div> | 0          | 1           |
|                                                                             | Input port | Output port  |                                                                             | Input port | Output port |
|                                                                             | Reserved   | SPCLK output |                                                                             | Reserved   | SPCS Output |

Note: A read-modify-write operation cannot be performed for the registers PRCR, PRFC.

Figure 3.7.51 Register for Port R

### 3.7.19 Port T (PT0 to PT7)

Ports T0 to T7 are 8-bit general-purpose I/O ports. Each bit can be set individually for input or output. Resetting sets ports T0 to T7 to input port and output latch to “0”.

In addition to functioning as general-purpose I/O port, PT0 to PT7 can also function as data bus for 32-bit memory connection (D24 to D31).

Above setting is used the control register PTCR and function register PTFC.

Setting the AM1 and AM0 pins as shown below and resetting the device initialize port 1 to the following function pins:

| AM1 | AM0 | Function Setting after reset is released |
|-----|-----|------------------------------------------|
| 0   | 0   | Don't use this setting                   |
| 0   | 1   | Input port (PT0 ~ PT7)                   |
| 1   | 0   | Data bus (D24 ~ D31)                     |
| 1   | 1   | Don't use this setting                   |

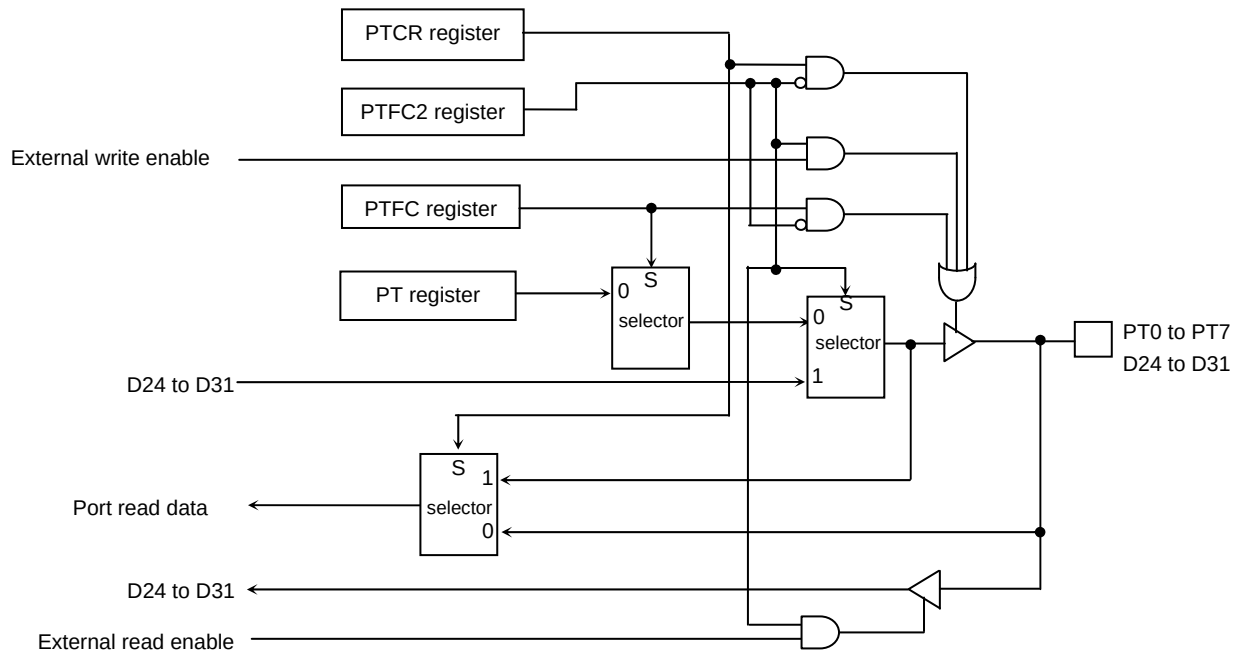


Figure 3.7.52 Port T0 to T7



| Port T register |                       |                                                                   |     |     |     |     |     |     |     |
|-----------------|-----------------------|-------------------------------------------------------------------|-----|-----|-----|-----|-----|-----|-----|
| PT<br>(00A0H)   |                       | 7                                                                 | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|                 | bit Symbol            | PT7                                                               | PT6 | PT5 | PT4 | PT3 | PT2 | PT1 | PT0 |
|                 | Read/Write            | R/W                                                               |     |     |     |     |     |     |     |
|                 | System<br>Reset State | Data from external port (Output latch register is cleared to “0”) |     |     |     |     |     |     |     |

| Port T control register |                       |                    |      |      |      |      |      |      |      |
|-------------------------|-----------------------|--------------------|------|------|------|------|------|------|------|
| PTCR<br>(00A2H)         |                       | 7                  | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|                         | bit Symbol            | PT7C               | PT6C | PT5C | PT4C | PT3C | PT2C | PT1C | PT0C |
|                         | Read/Write            | W                  |      |      |      |      |      |      |      |
|                         | System<br>Reset State | 0                  | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
|                         | Function              | 0: Input 1: Output |      |      |      |      |      |      |      |

| Port T function register |                       |                          |      |      |      |      |      |      |      |
|--------------------------|-----------------------|--------------------------|------|------|------|------|------|------|------|
| PTFC<br>(00A3H)          |                       | 7                        | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|                          | bit Symbol            | PT7F                     | PT6F | PT5F | PT4F | PT3F | PT2F | PT1F | PT0F |
|                          | Read/Write            | W                        |      |      |      |      |      |      |      |
|                          | System<br>Reset State | 0                        | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
|                          | Function              | 0: Port 1: Don't setting |      |      |      |      |      |      |      |

| Port T function register 2 |                       |   |   |   |   |   |   |   |                                      |
|----------------------------|-----------------------|---|---|---|---|---|---|---|--------------------------------------|
| PTFC2<br>(00A1H)           |                       | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0                                    |
|                            | bit Symbol            |   |   |   |   |   |   |   | PT0F2                                |
|                            | Read/Write            |   |   |   |   |   |   |   |                                      |
|                            | After<br>system reset |   |   |   |   |   |   |   | 0/1                                  |
|                            | After<br>Hot reset    |   |   |   |   |   |   |   | —                                    |
|                            | Function              |   |   |   |   |   |   |   | 0:Port<br>1:Data bus<br>(D24 to D31) |

| Port T drive register |                       |                                                     |      |      |      |      |      |      |      |
|-----------------------|-----------------------|-----------------------------------------------------|------|------|------|------|------|------|------|
| PTDR<br>(009BH)       |                       | 7                                                   | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|                       | bit Symbol            | PT7D                                                | PT6D | PT5D | PT4D | PT3D | PT2D | PT1D | PT0D |
|                       | Read/Write            | R/W                                                 |      |      |      |      |      |      |      |
|                       | System<br>Reset State | 1                                                   | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
|                       | Function              | Input/Output buffer drive register for standby mode |      |      |      |      |      |      |      |

Note: A read-modify-write operation cannot be performed for the registers PTCR, PTFC and PTFC2.

|                  |  | <PT0F2>=0     |             | <PT0F2>=1 |   |
|------------------|--|---------------|-------------|-----------|---|
| <PTnC><br><PTnF> |  | 0             | 1           | 0         | 1 |
| 0                |  | Input port    | Output port | Data Bus  |   |
| 1                |  | Don't setting |             |           |   |

Figure 3.7.53 Register for Port T

## 3.7.20 Port V (PV6, PV7)

Ports V6 and V7 are 2-bit general-purpose I/O ports. Each bit can be set individually for input or output. Resetting sets port V6 and V7 to input port and output latch to "0".

In addition to functioning as general-purpose I/O port, PV can also function as a input or output pin for SBI (SDA, SCL).

Setting in the corresponding bits of PVCR and PVFC enables the respective functions.

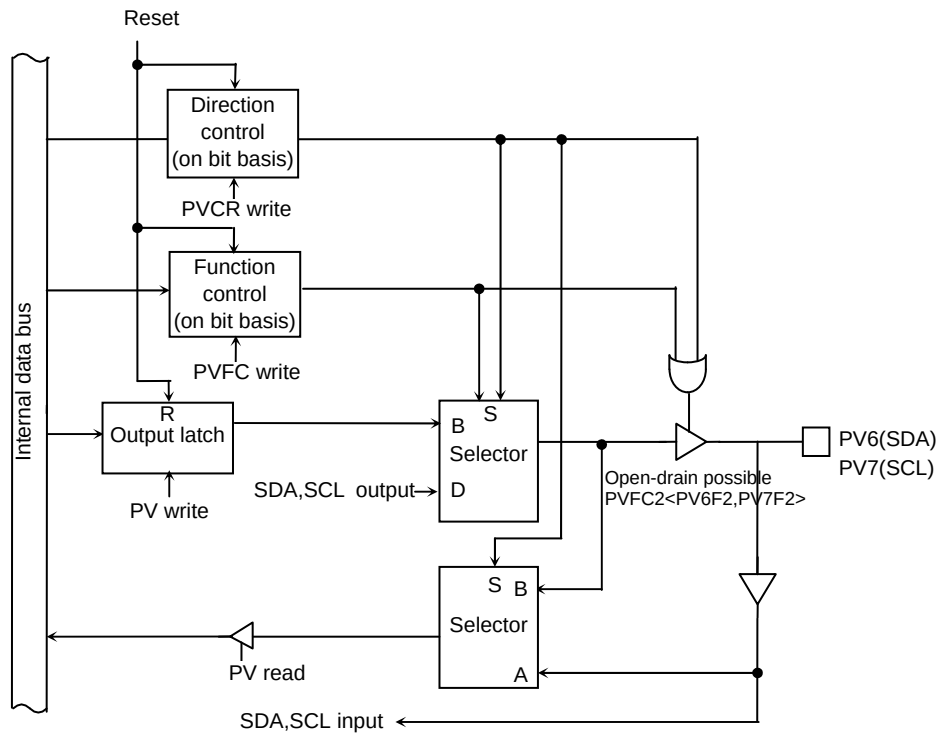


Figure 3.7.54 Port V6, V7

| Port V register |                    |                                                                   |     |   |   |   |   |   |   |
|-----------------|--------------------|-------------------------------------------------------------------|-----|---|---|---|---|---|---|
| PV<br>(00A8H)   |                    | 7                                                                 | 6   | 5 | 4 | 3 | 2 | 1 | 0 |
|                 | bit Symbol         | PV7                                                               | PV6 |   |   |   |   |   |   |
|                 | Read/Write         | R/W                                                               |     |   |   |   |   |   |   |
|                 | System Reset State | Data from external port (Output latch register is cleared to "0") |     |   |   |   |   |   |   |

| Port V control register |                    |                    |      |   |   |   |   |   |   |
|-------------------------|--------------------|--------------------|------|---|---|---|---|---|---|
| PVCR<br>(00AAH)         |                    | 7                  | 6    | 5 | 4 | 3 | 2 | 1 | 0 |
|                         | bit Symbol         | PV7C               | PV6C |   |   |   |   |   |   |
|                         | Read/Write         |                    |      |   |   |   |   |   |   |
|                         | System Reset State | 0                  | 0    |   |   |   |   |   |   |
|                         | Function           | 0: Input 1: Output |      |   |   |   |   |   |   |

| Port V function register |                    |                          |      |   |   |   |   |   |   |
|--------------------------|--------------------|--------------------------|------|---|---|---|---|---|---|
| PVFC<br>(00ABH)          |                    | 7                        | 6    | 5 | 4 | 3 | 2 | 1 | 0 |
|                          | bit Symbol         | PV7F                     | PV6F |   |   |   |   |   |   |
|                          | Read/Write         | W                        |      |   |   |   |   |   |   |
|                          | System Reset State | 0                        | 0    |   |   |   |   |   |   |
|                          | Function           | Refer to following table |      |   |   |   |   |   |   |

| Port V function register 2 |                    |                              |                              |   |   |   |   |   |   |
|----------------------------|--------------------|------------------------------|------------------------------|---|---|---|---|---|---|
| PVFC2<br>(00A9H)           |                    | 7                            | 6                            | 5 | 4 | 3 | 2 | 1 | 0 |
|                            | bit Symbol         | PV7F2                        | PV6F2                        |   |   |   |   |   |   |
|                            | Read/Write         | W                            |                              |   |   |   |   |   |   |
|                            | System Reset State | 0                            | 0                            |   |   |   |   |   |   |
|                            | Function           | 0: CMOS<br>1: Open<br>-drain | 0: CMOS<br>1: Open<br>-drain |   |   |   |   |   |   |

| Port V drive register |                    |                                                     |      |   |   |   |   |   |   |
|-----------------------|--------------------|-----------------------------------------------------|------|---|---|---|---|---|---|
| PVDR<br>(009DH)       |                    | 7                                                   | 6    | 5 | 4 | 3 | 2 | 1 | 0 |
|                       | bit Symbol         | PV7D                                                | PV6D |   |   |   |   |   |   |
|                       | Read/Write         | R/W                                                 |      |   |   |   |   |   |   |
|                       | System Reset State | 1                                                   | 1    |   |   |   |   |   |   |
|                       | Function           | Input/Output buffer drive register for standby mode |      |   |   |   |   |   |   |

| PV7 setting      |            |             | PV6 setting      |            |             |
|------------------|------------|-------------|------------------|------------|-------------|
| <PV7C><br><PV7F> | 0          | 1           | <PV6C><br><PV6F> | 0          | 1           |
| 0                | Input port | Output port | 0                | Input port | Output port |
| 1                | Reserved   | SCL I/O     | 1                | Reserved   | SDA I/O     |

Note: A read-modify-write operation cannot be performed for the registers PVCR, PVFC and PVFC2.

Figure 3.7.55 Register for Port V

### 3.7.21 Port X (PX4, PX5)

Port X5 is 1-bit general-purpose I/O ports. Each bit can be set individually for input or output. Resetting sets ports X5 to input port and output latch to “0”.

In addition to functioning as general-purpose I/O port, PX5 can also function as the USB clock input pin (X1USB) and dividing clock output of X1 and X2 oscillation clock (X1D4).

Setting in the corresponding bits of PXCR and PXFC enables the respective functions.

Port X4 is 1-bit general-purpose output port. Resetting sets output latch to “0”.

In addition to functioning as general-purpose output port, PX4 can also function as a system clock output pin (CLKOUT).

Setting in the corresponding bits of PX and PXFC enables the respective functions.

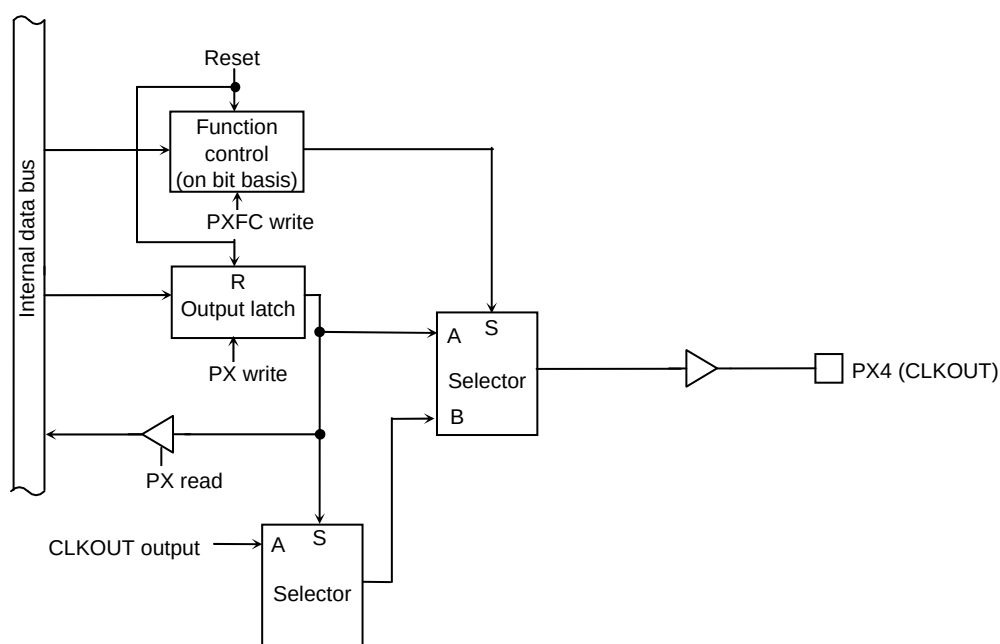


Figure 3.7.56 Port X4

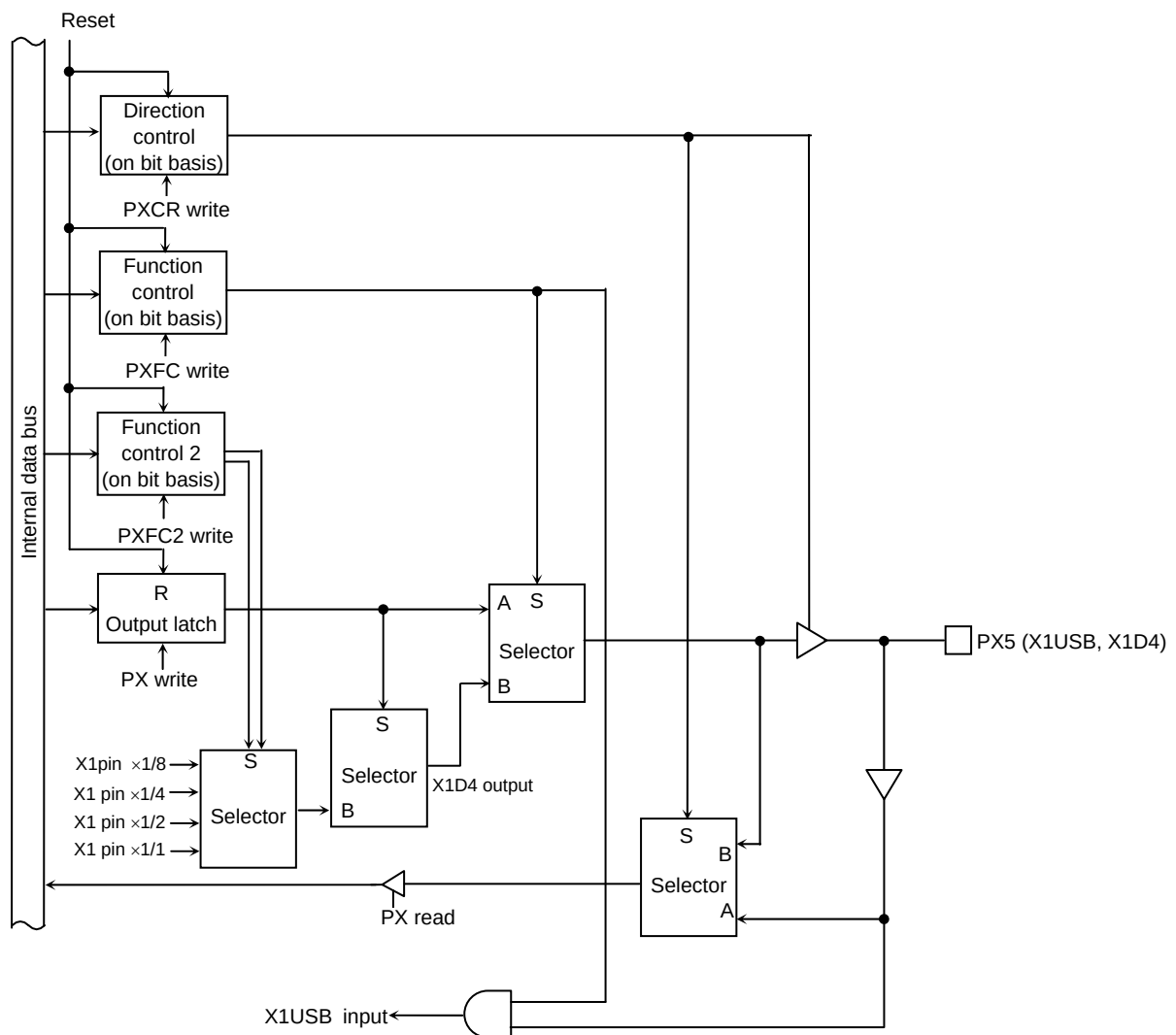


Figure 3.7.57 Port X5

Port X register

|               | 7                  | 6 | 5                                                                    | 4          | 3 | 2 | 1 | 0 |
|---------------|--------------------|---|----------------------------------------------------------------------|------------|---|---|---|---|
| PX<br>(00B0H) | bit Symbol         |   | PX5 Note3)                                                           | PX4 Note2) |   |   |   |   |
|               | Read/Write         |   | R/W                                                                  |            |   |   |   |   |
|               | System Reset State |   | Data from external port<br>(Output latch register is cleared to "0") |            |   |   |   |   |

Port X control register

|                 | 7                  | 6 | 5                     | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------------------|---|-----------------------|---|---|---|---|---|
| PXCR<br>(00B2H) | bit Symbol         |   | PX5C                  |   |   |   |   |   |
|                 | Read/Write         |   | W                     |   |   |   |   |   |
|                 | System Reset State |   | 0                     |   |   |   |   |   |
|                 | Function           |   | 0: Input<br>1: Output |   |   |   |   |   |

Port X function register

|                 | 7                  | 6 | 5                        | 4                                  | 3 | 2 | 1 | 0 |
|-----------------|--------------------|---|--------------------------|------------------------------------|---|---|---|---|
| PXFC<br>(00B3H) | bit Symbol         |   | PX5F                     | PX4F                               |   |   |   |   |
|                 | Read/Write         |   | W                        |                                    |   |   |   |   |
|                 | System Reset State |   | 0                        | 0                                  |   |   |   |   |
|                 | Function           |   | Refer to following table | 0: Port<br>1: CLKOUT<br>at <PX4>=0 |   |   |   |   |

Port X function register 2

|                  | 7                  | 6 | 5                                                                                                          | 4     | 3 | 2 | 1 | 0 |
|------------------|--------------------|---|------------------------------------------------------------------------------------------------------------|-------|---|---|---|---|
| PXFC2<br>(00B1H) | bit Symbol         |   | PX5F2                                                                                                      | PX4F2 |   |   |   |   |
|                  | Read/Write         |   | R/W                                                                                                        |       |   |   |   |   |
|                  | System Reset State |   | 0                                                                                                          | 0     |   |   |   |   |
|                  | Function           |   | X1D4 output<br>clock selection<br>00: X1 pin ×1/8<br>01: X1 pin ×1/4<br>10: X1 pin ×1/2<br>11: X1 pin ×1/1 |       |   |   |   |   |

| Port X drive register |                       |   |   |                                                           |      |   |   |   |   |
|-----------------------|-----------------------|---|---|-----------------------------------------------------------|------|---|---|---|---|
| PXDR<br>(009FH)       |                       | 7 | 6 | 5                                                         | 4    | 3 | 2 | 1 | 0 |
|                       | bit Symbol            |   |   | PXD5                                                      | PXD4 |   |   |   |   |
|                       | Read/Write            |   |   | R/W                                                       |      |   |   |   |   |
|                       | System<br>Reset State |   |   | 1                                                         | 1    |   |   |   |   |
|                       | Function              |   |   | Input/Output buffer<br>drive register<br>for standby mode |      |   |   |   |   |

Note 1: A read-modify-write operation cannot be performed for the registers PXCR, PXFC and PXFC2.

Note 2: When PX4 is used as CLKOUT output pin, PX<PX4> must be set to “0”. Refer to following PX4 setting table.

Note 3: When PX5 is used as X1D4 pin, PX<PX5> must be set to “1”. Refer to following PX5 setting table.

PX4 setting

| <PX4><br><PX4F> | 0             | 1             |
|-----------------|---------------|---------------|
|                 | 0             | Output port   |
| 1               | CLKOUT output | Don't setting |

PX5 setting

| <PX5C><br><PX5F> | 0           | 1                            |
|------------------|-------------|------------------------------|
|                  | 0           | Input port      Output port  |
| 1                | X1USB input | X1D4 output<br>at <PX5>= “1” |

Figure 3.7.58 Register for Port X

## 3.8 Memory Controller (MEMC)

### 3.8.1 Functional Overview

The TMP92CF30 has a memory controller with the following features to control four programmable address spaces:

(1) Four programmable address spaces

The MEMC can specify a start address and a block size for each of the four memory spaces (CS0 to CS3 spaces).

\* SRAM or ROM: All CS spaces (CS0 to CS3) can be assigned.

\* SDRAM: Either the CS1 or CS2 space can be assigned.

\* Page-ROM: Only the CS2 space can be assigned.

\* NAND-Flash: It is not required to setup the CS lines. However, when using NAND-Flash, set the BROMCR<CSDIS> bit to "1" to assign an external area to avoid data conflicts with CS spaces.

(2) Memory specification

The MEMC can specify the type of memory, SRAM, ROM and SDRAM to associate with the selected address spaces.

(3) Data bus width specification

The data bus width is selectable from 8, 16 and 32 bits for the respective chip select spaces. However, SDRAM and NANDF cannot use 32 bit data bus.

(4) Wait control

The number of wait states to be inserted into an external bus cycle is determined by the wait state bits of the control register and the  $\overline{\text{WAIT}}$  input pin. The number of wait states of a read cycle and that of a write cycle can be specified individually. The number of wait states can be selected from the following 15 options:

0 to 10 wait states, 12 wait states,  
16 wait states, 20 wait states  
4+N wait states (controlled by the  $\overline{\text{WAIT}}$  pin)



### 3.8.2 Control Registers and Memory Access Operations After Reset

This section describes the registers to control the memory controller, their reset states and the necessary settings after reset.

#### (1) Control Registers

The control registers of the memory controller are listed below.

- Control registers: BnCSH/BnCSL(n = 0 to 3, EX)  
Configures the basic settings of the memory controller, such as the memory type specification and the number of wait states to be inserted into a read or write cycle.
- Memory Start Address register: MSARn(n = 0 to 3)  
Specifies a start address for a selected address space.
- Memory Address Mask register: MAMR (n = 0 to 3)  
Specifies a block size for a selected address space.
- Page ROM Control register: PMEMCR  
Selects a method of accessing Page-ROM.
- Timing control registers: CSTMGCR, WRTMGCR, RDTMGCRn  
Adjust the timing of rising and falling edges of control signals.
- On-chip Boot ROM Control register: BROMCR  
Selects a method of accessing Boot-ROM.

Table 3.8.1 Control Registers

|                  |             | 7     | 6     | 5     | 4     | 3     | 2     | 1        | 0      |
|------------------|-------------|-------|-------|-------|-------|-------|-------|----------|--------|
| B0CSL<br>(0140H) | Bit Symbol  | B0WW3 | B0WW2 | B0WW1 | B0WW0 | B0WR3 | B0WR2 | B0WR1    | B0WR0  |
|                  | Read/Write  | R/W   |       |       |       |       |       |          |        |
|                  | Reset State | 0     | 0     | 1     | 0     | 0     | 0     | 1        | 0      |
| B0CSH<br>(0141H) | Bit Symbol  | B0E   |       |       | B0REC | B0OM1 | B0OM0 | B0BUS1   | B0BUS0 |
|                  | Read/Write  | R/W   |       |       | R/W   |       |       |          |        |
|                  | Reset State | 0     |       |       | 0     | 0     | 0     | 0        | 0      |
| MAMR0<br>(0142H) | Bit Symbol  | M0V20 | M0V19 | M0V18 | M0V17 | M0V16 | M0V15 | M0V14-V9 | M0V8   |
|                  | Read/Write  | R/W   |       |       |       |       |       |          |        |
|                  | Reset State | 1     | 1     | 1     | 1     | 1     | 1     | 1        | 1      |
| MSAR0<br>(0143H) | Bit Symbol  | M0S23 | M0S22 | M0S21 | M0S20 | M0S19 | M0S18 | M0S17    | M0S16  |
|                  | Read/Write  | R/W   |       |       |       |       |       |          |        |
|                  | Reset State | 1     | 1     | 1     | 1     | 1     | 1     | 1        | 1      |
| B1CSL<br>(0144H) | Bit Symbol  | B1WW3 | B1WW2 | B1WW1 | B1WW0 | B1WR3 | B1WR2 | B1WR1    | B1WR0  |
|                  | Read/Write  | R/W   |       |       |       |       |       |          |        |
|                  | Reset State | 0     | 0     | 1     | 0     | 0     | 0     | 1        | 0      |
| B1CSH<br>(0145H) | Bit Symbol  | B1E   |       |       | B1REC | B1OM1 | B1OM0 | B1BUS1   | B1BUS0 |
|                  | Read/Write  | R/W   |       |       | R/W   |       |       |          |        |
|                  | Reset State | 0     |       |       | 0     | 0     | 0     | 0        | 0      |
| MAMR1<br>(0146H) | Bit Symbol  | M1V21 | M1V20 | M1V19 | M1V18 | M1V17 | M1V16 | M1V15-V9 | M1V8   |
|                  | Read/Write  | R/W   |       |       |       |       |       |          |        |
|                  | Reset State | 1     | 1     | 1     | 1     | 1     | 1     | 1        | 1      |
| MSAR1<br>(0147H) | Bit Symbol  | M1S23 | M1S22 | M1S21 | M1S20 | M1S19 | M1S18 | M1S17    | M1S16  |
|                  | Read/Write  | R/W   |       |       |       |       |       |          |        |
|                  | Reset State | 1     | 1     | 1     | 1     | 1     | 1     | 1        | 1      |
| B2CSL<br>(0148H) | Bit Symbol  | B2WW3 | B2WW2 | B2WW1 | B2WW0 | B2WR3 | B2WR2 | B2WR1    | B2WR0  |
|                  | Read/Write  | R/W   |       |       |       |       |       |          |        |
|                  | Reset State | 0     | 0     | 1     | 0     | 0     | 0     | 1        | 0      |
| B2CSH<br>(0149H) | Bit Symbol  | B2E   | B2M   |       | B2REC | B2OM1 | B2OM0 | B2BUS1   | B2BUS0 |
|                  | Read/Write  | R/W   |       |       | R/W   |       |       |          |        |
|                  | Reset State | 1     | 0     |       | 0     | 0     | 0     | 0        | 1      |
| MAMR2<br>(014AH) | Bit Symbol  | M2V22 | M2V21 | M2V20 | M2V19 | M2V18 | M2V17 | M2V16    | M2V15  |
|                  | Read/Write  | R/W   |       |       |       |       |       |          |        |
|                  | Reset State | 1     | 1     | 1     | 1     | 1     | 1     | 1        | 1      |
| MSAR2<br>(014BH) | Bit Symbol  | M2S23 | M2S22 | M2S21 | M2S20 | M2S19 | M2S18 | M2S17    | M2S16  |
|                  | Read/Write  | R/W   |       |       |       |       |       |          |        |
|                  | Reset State | 1     | 1     | 1     | 1     | 1     | 1     | 1        | 1      |
| B3CSL<br>(014CH) | Bit Symbol  | B3WW3 | B3WW2 | B3WW1 | B3WW0 | B3WR3 | B3WR2 | B3WR1    | B3WR0  |
|                  | Read/Write  | R/W   |       |       |       |       |       |          |        |
|                  | Reset State | 0     | 0     | 1     | 0     | 0     | 0     | 1        | 0      |
| B3CSH<br>(014DH) | Bit Symbol  | B3E   |       |       | B3REC | B3OM1 | B3OM0 | B3BUS1   | B3BUS0 |
|                  | Read/Write  | R/W   |       |       | R/W   |       |       |          |        |
|                  | Reset State | 0     |       |       | 0     | 0     | 0     | 0        | 0      |
| MAMR3<br>(014EH) | Bit Symbol  | M3V22 | M3V21 | M3V20 | M3V19 | M3V18 | M3V17 | M3V16    | M3V15  |
|                  | Read/Write  | R/W   |       |       |       |       |       |          |        |
|                  | Reset State | 1     | 1     | 1     | 1     | 1     | 1     | 1        | 1      |
| MSAR3<br>(014FH) | Bit Symbol  | M3S23 | M3S22 | M3S21 | M3S20 | M3S19 | M3S18 | M3S17    | M3S16  |
|                  | Read/Write  | R/W   |       |       |       |       |       |          |        |
|                  | Reset State | 1     | 1     | 1     | 1     | 1     | 1     | 1        | 1      |

Table 3.8.2 Control Registers

|                     |             | 7       | 6       | 5       | 4       | 3       | 2       | 1       | 0                       |
|---------------------|-------------|---------|---------|---------|---------|---------|---------|---------|-------------------------|
| BEXCSL<br>(0158H)   | Bit Symbol  | BEXWW3  | BEXWW2  | BEXWW1  | BEXWW0  | BEXWR3  | BEXWR2  | BEXWR1  | BEXWR0                  |
|                     | Read/Write  | R/W     |         |         |         |         |         |         |                         |
|                     | Reset State | 0       | 0       | 1       | 0       | 0       | 0       | 1       | 0                       |
| BEXCSH<br>(0159H)   | Bit Symbol  |         |         |         | BEXREC  | BEXOM1  | BEXOM0  | BEXBUS1 | BEXBUS0                 |
|                     | Read/Write  |         |         |         | R/W     |         |         |         |                         |
|                     | Reset State |         |         |         | 0       | 0       | 0       | 0       | 0                       |
| PMEMCR<br>(0166H)   | Bit Symbol  |         |         |         | OPGE    | OPWR1   | OPWR0   | PR1     | PR0                     |
|                     | Read/Write  |         |         |         | R/W     | R/W     |         | R/W     |                         |
|                     | Reset State |         |         |         | 0       | 0       | 0       | 1       | 0                       |
| CSTMGCR<br>(0168H)  | Bit Symbol  |         |         | TACSEL1 | TACSEL0 |         |         | TAC1    | TAC0                    |
|                     | Read/Write  |         |         | R/W     |         |         |         | R/W     |                         |
|                     | Reset State |         |         | 0       | 0       |         |         | 0       | 0                       |
| WRTMGCR<br>(0169H)  | Bit Symbol  |         |         | TCWSEL1 | TCWSEL0 | TCWS1   | TCWS0   | TCWH1   | TCWH0                   |
|                     | Read/Write  |         |         | R/W     |         | R/W     |         | R/W     |                         |
|                     | Reset State |         |         | 0       | 0       | 0       | 0       | 0       | 0                       |
| RDTMGCR0<br>(016AH) | Bit Symbol  | B1TCRS1 | B1TCRS0 | B1TCRH1 | B1TCRH0 | B0TCRS1 | B0TCRS0 | B0TCRH1 | B0TCRH0                 |
|                     | Read/Write  | R/W     |         | R/W     |         | R/W     |         | R/W     |                         |
|                     | Reset State | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0                       |
| RDTMGCR1<br>(016BH) | Bit Symbol  | B3TCRS1 | B3TCRS0 | B3TCRH1 | B3TCRH0 | B2TCRS1 | B2TCRS0 | B2TCRH1 | B2TCRH0                 |
|                     | Read/Write  | R/W     |         | R/W     |         | R/W     |         | R/W     |                         |
|                     | Reset State | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0                       |
| BROMCR<br>(016CH)   | Bit Symbol  |         |         |         |         |         | CSDIS   | ROMLESS | VACE                    |
|                     | Read/Write  |         |         |         |         |         | R/W     |         |                         |
|                     | Reset State |         |         |         |         |         | 1       | 1       | 0                       |
| RAMCR<br>(016DH)    | Bit Symbol  |         |         |         |         |         |         |         | –                       |
|                     | Read/Write  |         |         |         |         |         |         |         | R/W                     |
|                     | Reset State |         |         |         |         |         |         |         | Must be written as "1". |

## (2) Memory Access Operations After Reset

After reset, external memory is accessed using the initial data bus width that is determined by the AM1 and AM0 pins. The settings of the AM1 and AM0 pins and their corresponding operation modes are as follows:

| AM1 | AM0 | Start Mode                          |
|-----|-----|-------------------------------------|
| 0   | 0   | Don't use this setting              |
| 0   | 1   | 16-bit external bus starting (Note) |
| 1   | 0   | 32-bit external bus starting (Note) |
| 1   | 1   | Don't use this setting              |

Note: The memory that is used for booting after reset must be either NOR-Flash or Masked-ROM. NAND-Flash and SDRAM cannot be used.

The values of AM1 and AM0 are effective only upon reset. The data bus width is specified by the <BnBUS1:BnBUS0> bits of the control registers at any other timing.

Upon reset, only the control registers (B2CSH and B2CSL) for the CS2 space automatically becomes effective. (The B2CSH<B2E> bit is set to 1 upon reset.) Then, the AM1 and AM0 values that specify the data bus width are loaded into the data bus width specification bits of the control register for the CS2 space. At the same time, the address range between 000000H and FFFFFFFH is defined as the CS2 space. (The B2CSH<B2M> is cleared to 0.)

Then, the address spaces are configured by MSARn and MAMRn. The BnCSH and BnCSL registers are also set up. The BnCSH<BnE> must be set to 1 to enable these settings.

3.8.3 Basic Functions and Register Settings

This section describes some of the memory controller functions, such as setting the address range for each address space, associating memory to the selected space and setting the number of wait states to be inserted.

(1) Programming chip select spaces

The address ranges of CS0 to CS3 are specified by MSAR0 to MSAR3 and MAMR0 to MAMR3.

(a) Memory Start Address registers

Figure 3.8.1 shows the Memory Start Address registers. The MSAR0 to MSAR3 specify the start addresses for the CS0 to CS3 spaces. The bits S23 to S16 specify the upper 8 bits (A23 to A16) of the start address. The lower 16 bits of the start address (A15 to A0) are assumed to be 0. Accordingly, the start address can only be a multiple of 64 Kbytes, ranging from 000000H to FF0000H. Figure 3.8.2 shows the relationship between the start addresses and the Memory Start Address register values.

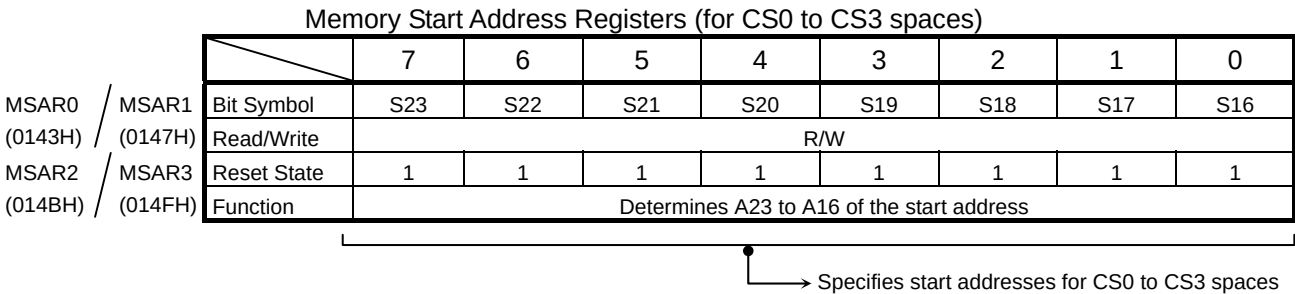


Figure 3.8.1 Memory Start Address Register

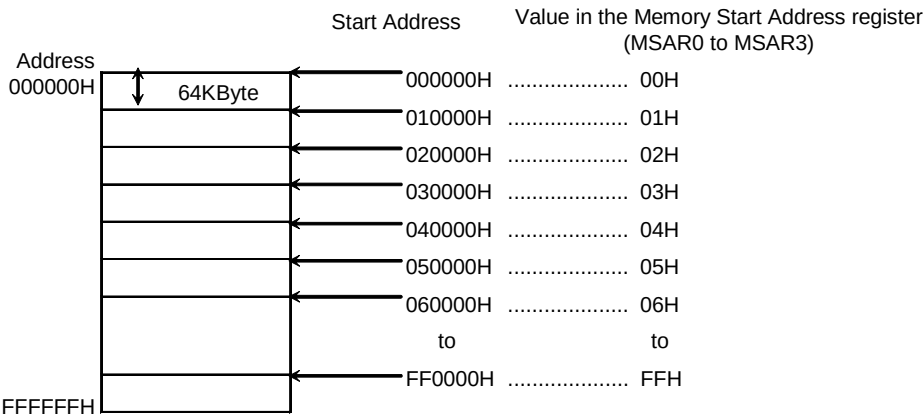


Figure 3.8.2 Relationship Between Start Addresses and the Memory Start Address Register Values

## (b) Memory Address Mask Registers

Figure 3.8.3 shows the Memory Address Mask registers. MAMR0 to MAMR3 are used to determine the sizes of the CS0 to CS3 spaces by setting particular bits in MAMR0 to MAMR3 to mask the corresponding start address bits. The address compare logic uses only the address bits that are not masked (i.e., mask bit cleared to 0) to detect an address match in the CS0 to CS3 spaces. The upper bits are always compared.

Also, the address bits that can be masked by MAMR0 to MAMR3 differ between CS0 to CS3 spaces as follows:

CS0 space: A20 to A8

CS1 space: A21 to A8

CS2 and CS3 spaces: A22 to A15

Accordingly, the block size that can be assigned to each space is also different.

Note: After reset, only the control register for the CS2 space is effective. The control register for the CS2 space has the B2M bit. If the B2M bit is cleared to 0, the address range between 000000H and FFFFFFFH is defined as the CS2 space. (The B2M bit is cleared to 0 after reset.) By setting the B2CSH<B2M> bit to 1, the start address and the block size can be arbitrarily specified, as in the other spaces.

Memory Address Mask Register (for CS0 space)

|                  |             | 7                                                                 | 6   | 5   | 4   | 3   | 2   | 1     | 0  |
|------------------|-------------|-------------------------------------------------------------------|-----|-----|-----|-----|-----|-------|----|
|                  |             | 7                                                                 | 6   | 5   | 4   | 3   | 2   | 1     | 0  |
| MAMR0<br>(0142H) | Bit Symbol  | V20                                                               | V19 | V18 | V17 | V16 | V15 | V14~9 | V8 |
|                  | Read/Write  | R/W                                                               |     |     |     |     |     |       |    |
|                  | Reset State | 1                                                                 | 1   | 1   | 1   | 1   | 1   | 1     | 1  |
|                  | Function    | CS0 block size 0: The address compare logic uses this address bit |     |     |     |     |     |       |    |

The CS0 block size can vary from 256 Bytes to 2 Mbytes

Memory Address Mask Register (for CS1 space)

|                  |             | 7                                                                 | 6   | 5   | 4   | 3   | 2   | 1     | 0  |
|------------------|-------------|-------------------------------------------------------------------|-----|-----|-----|-----|-----|-------|----|
|                  |             | 7                                                                 | 6   | 5   | 4   | 3   | 2   | 1     | 0  |
| MAMR1<br>(0146H) | Bit Symbol  | V21                                                               | V20 | V19 | V18 | V17 | V16 | V15~9 | V8 |
|                  | Read/Write  | R/W                                                               |     |     |     |     |     |       |    |
|                  | Reset State | 1                                                                 | 1   | 1   | 1   | 1   | 1   | 1     | 1  |
|                  | Function    | CS1 block size 0: The address compare logic uses this address bit |     |     |     |     |     |       |    |

The CS1 block size can vary from 256 Bytes to 4 Mbytes

Memory Address Mask Register (for CS2 and CS3 spaces)

|                                    |             | 7                                                                         | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|------------------------------------|-------------|---------------------------------------------------------------------------|-----|-----|-----|-----|-----|-----|-----|
|                                    |             | 7                                                                         | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| MAMR2 / MSAR3<br>(014AH) / (014FH) | Bit Symbol  | V22                                                                       | V21 | V20 | V19 | V18 | V17 | V16 | V15 |
|                                    | Read/Write  | R/W                                                                       |     |     |     |     |     |     |     |
|                                    | Reset State | 1                                                                         | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
|                                    | Function    | CS2 or CS3 block size 0: The address compare logic uses this address bit. |     |     |     |     |     |     |     |

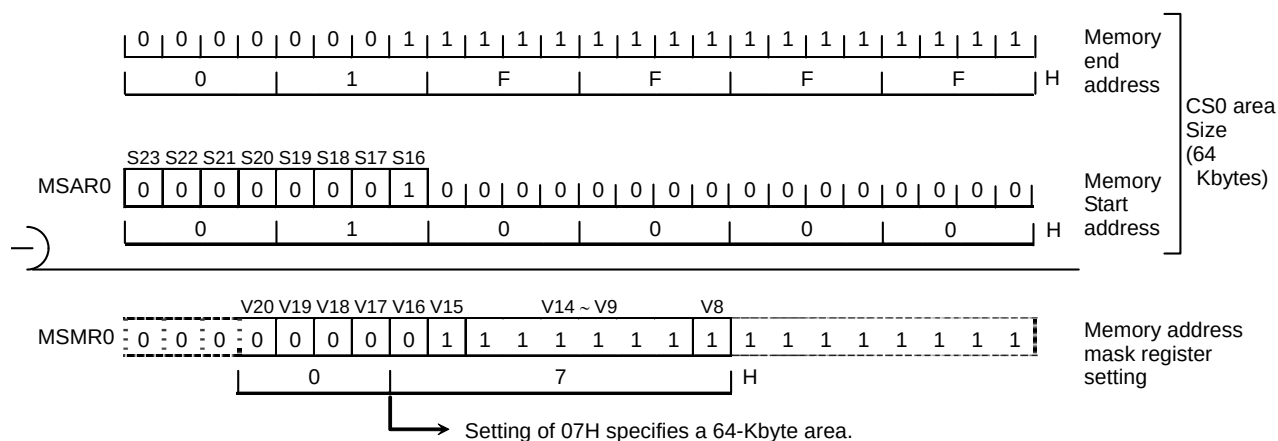
The CS2 and CS3 block sizes can vary from 32 Kbytes to 8 Mbytes

Figure 3.8.3 Memory Address Mask Registers

## (c) Setting the start addresses and address ranges

An example of specifying a 64-Kbyte address space starting from 010000H for the CS0 space:

Set 01H in the MSAR0<S23:S16> bits that corresponds to the upper 8 bits of the start address. Then, calculate the difference between the start address and the anticipated end address (01FFFFH) based on the size of the CS0 space. Bits 20 to 8 of the calculation result correspond to the mask value to be set for the CS0 space. Setting this value in the MAMR0<V20:V8> bits specifies the block size. This example sets 07H in MAMR0 to allocate a 64-Kbyte address space for the CS0 space.



## (d) Programming block sizes

Table 3.8.3 shows the relationship between CS spaces and their block sizes. The “Δ” symbol indicates the size that might not be programmable depending on the combination of the values of the Memory Start Address and Memory Address Mask registers. When specifying a block size indicated as “Δ”, set the start address register to a multiple of the desired block size starting from 000000H.

If the 16-Mbyte range is defined as CS2 space, or if two or more spaces overlap, the settings for the CS space with the smallest number overrides the settings for other spaces because of its highest priority.

Example: Defining 128 Kbyte area as the CS0 space:

## a. Valid start addresses

|         |   |            |   |                                                                   |
|---------|---|------------|---|-------------------------------------------------------------------|
| 000000H | } | 128 Kbytes | } | The desired block size can be programmed with this configuration. |
| 020000H |   | 128 Kbytes |   |                                                                   |
| 040000H |   | 128 Kbytes |   |                                                                   |
| 060000H |   | 128 Kbytes |   |                                                                   |
| :       |   |            |   |                                                                   |

## b. Invalid start addresses

|         |   |            |   |                                                                                                                                             |
|---------|---|------------|---|---------------------------------------------------------------------------------------------------------------------------------------------|
| 000000H | } | 64 Kbytes  | } | This start address is not a multiple of the desired block size. Hence, the desired block size cannot be programmed with this configuration. |
| 010000H |   | 128 Kbytes |   |                                                                                                                                             |
| 030000H |   | 128 Kbytes |   |                                                                                                                                             |
| 050000H |   | 128 Kbytes |   |                                                                                                                                             |

Table 3.8.3 Valid Block Sizes for Each CS Space

| Size<br>(Byte)<br>CS space | 256 | 512 | 32 K | 64 K | 128 K | 256 K | 512 K | 1 M | 2 M | 4 M | 8 M |
|----------------------------|-----|-----|------|------|-------|-------|-------|-----|-----|-----|-----|
| CS0                        | ○   | ○   | ○    | ○    | Δ     | Δ     | Δ     | Δ   | Δ   |     |     |
| CS1                        | ○   | ○   |      | ○    | Δ     | Δ     | Δ     | Δ   | Δ   | Δ   |     |
| CS2                        |     |     | ○    | ○    | Δ     | Δ     | Δ     | Δ   | Δ   | Δ   | Δ   |
| CS3                        |     |     | ○    | ○    | Δ     | Δ     | Δ     | Δ   | Δ   | Δ   | Δ   |

Note: The “Δ” symbol indicates the sizes that may not be programmable depending on the combination of the values of the Memory Start Address and Memory Address Mask registers.

(e) Priorities of the address spaces

When the specified address space overlaps with the on-chip memory area, the priority order of the address spaces are as follows:

|                                                                              |
|------------------------------------------------------------------------------|
| On-chip I/O > On-chip memory > CS0 space > CS1 space > CS2 space > CS3 space |
|------------------------------------------------------------------------------|

(f) Specifying the number of wait states and the bus width for the address locations outside the CS0 to CS3 spaces

The BEXCSL and BEXCSH registers specify the data bus width and number of wait states when an address outside the CS0 to CS3 spaces ( $\overline{\text{CSEX}}$  space) is accessed. These registers are always enabled for the CSEX space.



## (2) Memory specification

Setting the BnCSH<BnOM1:BnOM0> bits specifies the memory type that is associated with each address spaces. The interface signal that corresponds to the specified memory type is generated. The memory type is specified as follows:

BnCSH&lt;BnOM1:0&gt;

| BnOM1 | BnOM0 | Memory Type        |
|-------|-------|--------------------|
| 0     | 0     | SRAM/ROM (Default) |
| 0     | 1     | (Reserved)         |
| 1     | 0     | (Reserved)         |
| 1     | 1     | SDRAM              |

Note : SDRAM can be associated with the CS1 or CS2 space.

## (3) Data bus width specification

The data bus width can be specified for each address space by the BnCSH<BnBUS1:BnBUS0> bits as follows:

BnCSH&lt;BnBUS1:BnBUS0&gt;

| <BnBUS1> | <BnBUS0> | Bus Width                |
|----------|----------|--------------------------|
| 0        | 0        | 8-bit bus mode (Default) |
| 0        | 1        | 16-bit bus mode          |
| 1        | 0        | 32-bit bus mode          |
| 1        | 1        | Don't use this setting   |

Note: The data bus width for SDRAM should be defined as 16 bits by setting BnCSH<BnBUS1:BnBUS0> to 01.

As described above, the TMP92CF30 supports dynamic bus sizing, which allows the controller to transfer operands to or from the selected address spaces while automatically determining the data bus width. On which part of the data bus the data is actually placed is determined by the data size, bus width and start address. The table below provides a detailed description of the actual bus operation.

Note: If two memories with different bus widths are assigned to consecutive addresses, do not execute an instruction that accesses the addresses crossing the boundary between those memories. Otherwise, a read/write operation might not be performed correctly.

| Operand Data<br>Size (bit) | Operand Start<br>Address | Memory Bus Width<br>(bit) | CPU Address                                          | CPU Data                                             |                                  |                                  |                                                   |                                                   |
|----------------------------|--------------------------|---------------------------|------------------------------------------------------|------------------------------------------------------|----------------------------------|----------------------------------|---------------------------------------------------|---------------------------------------------------|
|                            |                          |                           |                                                      | D31 to D24                                           | D23 to D16                       | D15 to D8                        | D7 to D0                                          |                                                   |
| 8                          | 4n + 0                   | 8/16/32                   | 4n + 0                                               | xxxxx                                                | xxxxx                            | xxxxx                            | b7 to b0                                          |                                                   |
|                            | 4n + 1                   | 8                         | 4n + 1                                               | xxxxx                                                | xxxxx                            | xxxxx                            | b7 to b0                                          |                                                   |
|                            |                          | 16/32                     | 4n + 1                                               | xxxxx                                                | xxxxx                            | b7 to b0                         | xxxxx                                             |                                                   |
|                            | 4n + 2                   | 8/16                      | 4n + 2                                               | xxxxx                                                | xxxxx                            | xxxxx                            | b7 to b0                                          |                                                   |
|                            |                          | 32                        | 4n + 2                                               | xxxxx                                                | b7 to b0                         | xxxxx                            | xxxxx                                             |                                                   |
|                            | 4n + 3                   | 8                         | 4n + 3                                               | xxxxx                                                | xxxxx                            | xxxxx                            | b7 to b0                                          |                                                   |
|                            |                          | 16                        | 4n + 3                                               | xxxxx                                                | xxxxx                            | b7 to b0                         | xxxxx                                             |                                                   |
|                            |                          | 32                        | 4n + 3                                               | b7 to b0                                             | xxxxx                            | xxxxx                            | xxxxx                                             |                                                   |
| 16                         | 4n + 0                   | 8                         | (1) 4n + 0<br>(2) 4n + 1                             | xxxxx<br>xxxxx                                       | xxxxx<br>xxxxx                   | xxxxx<br>xxxxx                   | b7 to b0<br>b15 to b8                             |                                                   |
|                            |                          | 16/32                     | 4n + 0                                               | xxxxx                                                | xxxxx                            | b15 to b8                        | b7 to b0                                          |                                                   |
|                            |                          |                           |                                                      |                                                      |                                  |                                  |                                                   |                                                   |
|                            | 4n + 1                   | 8                         | (1) 4n + 1<br>(2) 4n + 2                             | xxxxx<br>xxxxx                                       | xxxxx<br>xxxxx                   | xxxxx<br>xxxxx                   | b7 to b0<br>b15 to b8                             |                                                   |
|                            |                          | 16                        | (1) 4n + 1<br>(2) 4n + 2                             | xxxxx<br>xxxxx                                       | xxxxx                            | b7 to b0                         | xxxxx                                             |                                                   |
|                            |                          | 32                        | 4n + 1                                               | xxxxx                                                | b15 to b8                        | b7 to b0                         | xxxxx                                             |                                                   |
|                            | 4n + 2                   | 8                         | (1) 4n + 2<br>(2) 4n + 1                             | xxxxx<br>xxxxx                                       | xxxxx<br>xxxxx                   | xxxxx<br>xxxxx                   | b7 to b0<br>b15 to b8                             |                                                   |
|                            |                          | 16                        | 4n + 2                                               | xxxxx                                                | xxxxx                            | b15 to b8                        | b7 to b0                                          |                                                   |
|                            |                          | 32                        | 4n + 2                                               | b15 to b8                                            | b7 to b0                         | xxxxx                            | xxxxx                                             |                                                   |
|                            | 4n + 3                   | 8                         | (1) 4n + 3<br>(2) 4n + 4                             | xxxxx<br>xxxxx                                       | xxxxx<br>xxxxx                   | xxxxx<br>xxxxx                   | b7 to b0<br>b15 to b8                             |                                                   |
|                            |                          | 16                        | (1) 4n + 3<br>(2) 4n + 4                             | xxxxx<br>xxxxx                                       | xxxxx                            | b7 to b0                         | xxxxx                                             |                                                   |
|                            |                          | 32                        | (1) 4n + 3<br>(2) 4n + 4                             | b7 to b0<br>xxxxx                                    | xxxxx<br>xxxxx                   | xxxxx<br>xxxxx                   | xxxxx<br>b15 to b8                                |                                                   |
|                            | 32                       | 4n + 0                    | 8                                                    | (1) 4n + 0<br>(2) 4n + 1<br>(3) 4n + 2<br>(4) 4n + 3 | xxxxx<br>xxxxx<br>xxxxx<br>xxxxx | xxxxx<br>xxxxx<br>xxxxx<br>xxxxx | xxxxx<br>xxxxx<br>xxxxx<br>xxxxx                  | b7 to b0<br>b15 to b8<br>b23 to b16<br>b31 to b24 |
|                            |                          |                           | 16                                                   | (1) 4n + 0<br>(2) 4n + 2                             | xxxxx<br>xxxxx                   | xxxxx<br>xxxxx                   | b15 to b8<br>b31 to b24                           | b7 to b0<br>b23 to b16                            |
|                            |                          |                           | 32                                                   | 4n + 0                                               | b31 to b24                       | b23 to b16                       | b15 to b8                                         | b7 to b0                                          |
|                            |                          | 4n + 1                    | 8                                                    | (1) 4n + 0<br>(2) 4n + 1<br>(3) 4n + 2<br>(4) 4n + 3 | xxxxx<br>xxxxx<br>xxxxx<br>xxxxx | xxxxx<br>xxxxx<br>xxxxx<br>xxxxx | xxxxx<br>xxxxx<br>xxxxx<br>xxxxx                  | b7 to b0<br>b15 to b8<br>b23 to b16<br>b31 to b24 |
| 16                         |                          |                           | (1) 4n + 1<br>(2) 4n + 2<br>(3) 4n + 4               | xxxxx<br>xxxxx<br>xxxxx                              | xxxxx<br>xxxxx<br>xxxxx          | b7 to b0<br>b23 to b16<br>xxxxx  | xxxxx<br>b15 to b8<br>b31 to b24                  |                                                   |
| 32                         |                          |                           | (1) 4n + 1<br>(2) 4n + 4                             | b23 to b16<br>xxxxx                                  | b15 to b8<br>xxxxx               | b7 to b0<br>xxxxx                | xxxxx<br>b31 to b24                               |                                                   |
| 4n + 2                     |                          | 8                         | (1) 4n + 2<br>(2) 4n + 3<br>(3) 4n + 4<br>(4) 4n + 5 | xxxxx<br>xxxxx<br>xxxxx<br>xxxxx                     | xxxxx<br>xxxxx<br>xxxxx<br>xxxxx | xxxxx<br>xxxxx<br>xxxxx<br>xxxxx | b7 to b0<br>b15 to b8<br>b23 to b16<br>b31 to b24 |                                                   |
|                            |                          | 16                        | (1) 4n + 2<br>(2) 4n + 4                             | xxxxx<br>xxxxx                                       | xxxxx<br>xxxxx                   | b15 to b8<br>b31 to b24          | b7 to b0<br>b23 to b16                            |                                                   |
|                            |                          | 32                        | (1) 4n + 2<br>(2) 4n + 4                             | b15 to b8<br>xxxxx                                   | b7 to b0<br>xxxxx                | xxxxx<br>b31 to b24              | xxxxx<br>b23 to b16                               |                                                   |
| 4n + 3                     |                          | 8                         | (1) 4n + 3<br>(2) 4n + 4<br>(3) 4n + 5<br>(4) 4n + 6 | xxxxx<br>xxxxx<br>xxxxx<br>xxxxx                     | xxxxx<br>xxxxx<br>xxxxx<br>xxxxx | xxxxx<br>xxxxx<br>xxxxx<br>xxxxx | b7 to b0<br>b15 to b8<br>b23 to b16<br>b31 to b24 |                                                   |
|                            |                          | 16                        | (1) 4n + 3<br>(2) 4n + 4<br>(3) 4n + 6               | xxxxx<br>xxxxx<br>xxxxx                              | xxxxx<br>xxxxx<br>xxxxx          | b7 to b0<br>b23 to b16<br>xxxxx  | xxxxx<br>b15 to b8<br>b31 to b24                  |                                                   |
|                            |                          | 32                        | (1) 4n + 3<br>(2) 4n + 4                             | b7 to b0<br>xxxxx                                    | xxxxx<br>b31 to b24              | xxxxx<br>b23 to b16              | xxxxx<br>b15 to b8                                |                                                   |
|                            |                          |                           |                                                      |                                                      |                                  |                                  |                                                   |                                                   |
|                            |                          |                           |                                                      |                                                      |                                  |                                  |                                                   |                                                   |
|                            |                          |                           |                                                      |                                                      |                                  |                                  |                                                   |                                                   |

xxxxx: The input data placed on the data bus indicated by this symbol is ignored during a read operation. During a write operation, the bus is in the high-impedance state, and the write strobe signal remains inactive.

## (4) Wait control

The external bus cycle completes in two states at minimum (25 ns at  $f_{SYS} = 80$  MHz) without inserting a wait state.

Setting up the BnCSL<BnWW3:BnWW0> bits specifies the number of wait states to be inserted in a write cycle, and setting the BnCSL<BnWR3:BnWR0> bits specifies the number of wait states to be inserted in a read cycle. The external bus cycle can be programmed as follows;

BnCSL&lt;BnWW&gt;/&lt;BnWR&gt;

| <BnWW3><br><BnWR3>   | <BnWW2><br><BnWR2> | <BnWW1><br><BnWR1> | <BnWW0><br><BnWR0> | Number of Wait States                                    |
|----------------------|--------------------|--------------------|--------------------|----------------------------------------------------------|
| 0                    | 0                  | 0                  | 1                  | 2 states (0 wait state), fixed wait-state mode           |
| 0                    | 0                  | 1                  | 0                  | 3 states (1 wait state), fixed wait-state mode (Default) |
| 0                    | 1                  | 0                  | 1                  | 4 states (2 wait states), fixed wait-state mode          |
| 0                    | 1                  | 1                  | 0                  | 5 states (3 wait states), fixed wait-state mode          |
| 0                    | 1                  | 1                  | 1                  | 6 states (4 wait states), fixed wait-state mode          |
| 1                    | 0                  | 0                  | 0                  | 7 states (5 wait states), fixed wait-state mode          |
| 1                    | 0                  | 0                  | 1                  | 8 states (6 wait states), fixed wait-state mode          |
| 1                    | 0                  | 1                  | 0                  | 9 states (7 wait states), fixed wait-state mode          |
| 1                    | 0                  | 1                  | 1                  | 10 states (8 wait states), fixed wait-state mode         |
| 1                    | 1                  | 0                  | 0                  | 11 states (9 wait states), fixed wait-state mode         |
| 1                    | 1                  | 0                  | 1                  | 12 states (10 wait states), fixed wait-state mode        |
| 1                    | 1                  | 1                  | 0                  | 14 states (12 wait states), fixed wait-state mode        |
| 1                    | 1                  | 1                  | 1                  | 18 states (16 wait states), fixed wait-state mode        |
| 0                    | 1                  | 0                  | 0                  | 22 states (20 wait states), fixed wait-state mode        |
| 0                    | 0                  | 1                  | 1                  | 6 states + $\overline{\text{WAIT}}$ pin input mode       |
| Other than the above |                    |                    |                    | Reserved                                                 |

Note 1: For SDRAM, the above settings are not effective. Refer to Section 3.11, SDRAM controller.

Note 2: For NAND flash memory, the above settings are not effective.

## (a) Fixed wait-state mode

The bus cycle is completed in the specified number of states. The number of states can be selected from 2 (0 wait state) through 12 (10 wait states), 14 (12 wait states), 18 (16 wait states) and 22 (20 wait states).

(b)  $\overline{\text{WAIT}}$  pin input mode

In this mode, the  $\overline{\text{WAIT}}$  signal is sampled. A wait state is continued to be inserted while the  $\overline{\text{WAIT}}$  signal is sampled active. The minimum bus cycle in this mode is six states. The bus cycle is completed if the  $\overline{\text{WAIT}}$  signal is sampled High at the rising edge of SDCLK in the sixth state. The bus cycle is extended as long as the  $\overline{\text{WAIT}}$  signal remains active after sixth state.

## (5) Recovery cycle (data hold time) control

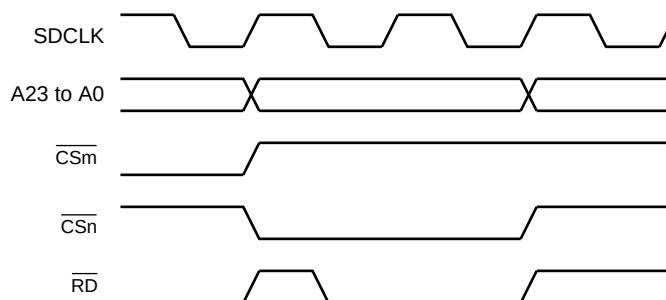
For some memory, the data hold time after when the  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  signal is asserted in a read cycle is defined by the AC specification. This may lead to data conflicts. Thus, to avoid this problem, a single dummy cycle can be inserted immediately after an access cycle for the CS<sub>m</sub> space by setting the BmCSH<BmREC> bit to 1.

This single dummy cycle is inserted when another CS space is accessed in the next bus cycle.

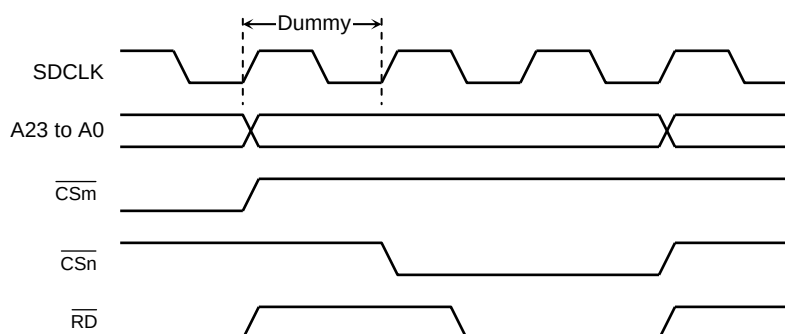
## BnCSH&lt;BnREC&gt;

|   |                                       |
|---|---------------------------------------|
| 0 | No dummy cycle is inserted (Default). |
| 1 | Dummy cycle is inserted.              |

- When no dummy cycle is inserted (0 wait state)



- When a single dummy cycle is inserted (0 wait state)



## (6) Timing adjustment function for control signals

This function allows for the timing adjustment of the rising and falling edges of the  $\overline{\text{CSn}}$ ,  $\overline{\text{CSZx}}$ ,  $\overline{\text{CSXx}}$ ,  $\text{R}/\overline{\text{W}}$ ,  $\overline{\text{RD}}$ ,  $\overline{\text{WRxx}}$ ,  $\overline{\text{SRWR}}$  and  $\overline{\text{SRxxB}}$  signals based on the setup and hold time requirements of memories.

As for the  $\overline{\text{CSn}}$ ,  $\overline{\text{CSZx}}$ ,  $\overline{\text{CSXx}}$  and  $\text{R}/\overline{\text{W}}$  signals, and also for the  $\overline{\text{WRxx}}$ ,  $\overline{\text{SRWR}}$  and  $\overline{\text{SRxxB}}$  signals (generated in a write cycle), their timing can be adjusted for only one CS space. As for the  $\overline{\text{RD}}$  and  $\overline{\text{SRxxB}}$  signals (generated in a read cycle), their timing can be adjusted individually for each of all CS spaces. As for the CS and EX spaces for which the timing adjustment is not performed, the buses connected to them operate with basic bus timing. (Refer to (7).)

This function can not be used while the  $\text{BnCSH}<\text{BnREC}>$  bit is enabled.

The control signals of SDRAM can be adjusted by setting up the SDRAM controller.

## CSTMGCR&lt;TxxSEL1:TxxSEL0&gt;, WRTMGCR&lt;TxxSEL1:TxxSEL0&gt;

|    |                                     |
|----|-------------------------------------|
| 00 | Change the bus timing for CS0 space |
| 01 | Change the bus timing for CS1 space |
| 10 | Change the bus timing for CS2 space |
| 11 | Change the bus timing for CS3 space |

## CSTMGCR&lt;TAC1:TAC0&gt;

|    |                                                    |
|----|----------------------------------------------------|
| 00 | $\text{TAC} = 0 \times 1/f_{\text{SYS}}$ (Default) |
| 01 | $\text{TAC} = 1 \times 1/f_{\text{SYS}}$           |
| 10 | $\text{TAC} = 2 \times 1/f_{\text{SYS}}$           |
| 11 | Reserved                                           |

TAC: The delay from A23-A0 to  $\overline{\text{CSn}}$ ,  $\overline{\text{CSZx}}$ ,  $\overline{\text{CSXx}}$ ,  $\text{R}/\overline{\text{W}}$ .

## WRTMGCR&lt;TCWS/H1:TCWS/H0&gt;

|    |                                                                |
|----|----------------------------------------------------------------|
| 00 | $\text{TCWS}/\text{H} = 0.5 \times 1/f_{\text{SYS}}$ (Default) |
| 01 | $\text{TCWS}/\text{H} = 1.5 \times 1/f_{\text{SYS}}$           |
| 10 | $\text{TCWS}/\text{H} = 2.5 \times 1/f_{\text{SYS}}$           |
| 11 | $\text{TCWS}/\text{H} = 3.5 \times 1/f_{\text{SYS}}$           |

TCWS: The delay from  $\overline{\text{CSn}}$  to  $\overline{\text{WRxx}}$ ,  $\overline{\text{SRWR}}$ ,  $\overline{\text{SRxxB}}$ .

TCWH: The delay from  $\overline{\text{WRxx}}$ ,  $\overline{\text{SRWR}}$ ,  $\overline{\text{SRxxB}}$  to  $\overline{\text{CSn}}$ .

## RDTMGCR0/1&lt;BnTCRH1:BnTCRH0&gt;

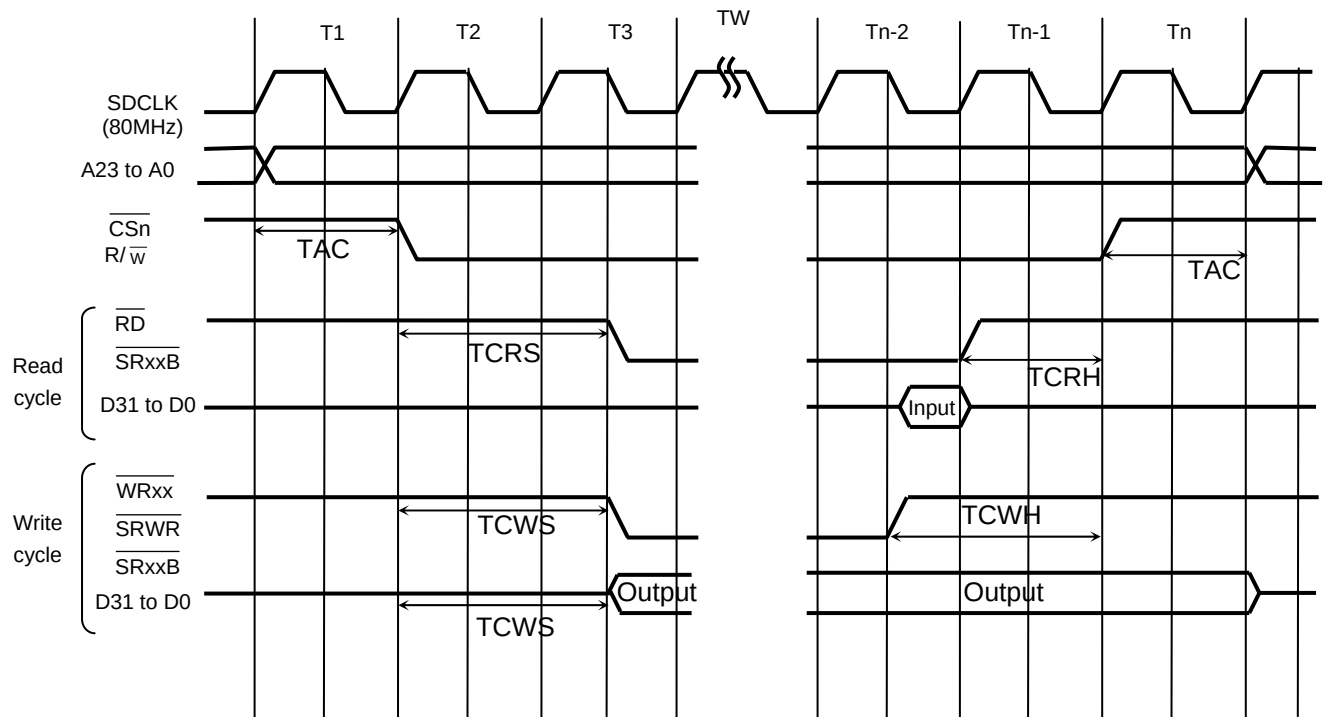
|    |                                                     |
|----|-----------------------------------------------------|
| 00 | $\text{TCRH} = 0 \times 1/f_{\text{SYS}}$ (Default) |
| 01 | $\text{TCRH} = 1 \times 1/f_{\text{SYS}}$           |
| 10 | $\text{TCRH} = 2 \times 1/f_{\text{SYS}}$           |
| 11 | $\text{TCRH} = 3 \times 1/f_{\text{SYS}}$           |

TCRH: The delay from  $\overline{\text{RD}}$ ,  $\overline{\text{SRxxB}}$  to  $\overline{\text{CSn}}$ .

RDTMGCR0/1&lt;BnTCRS1:BnTCRS0&gt;

|    |                                         |
|----|-----------------------------------------|
| 00 | $TCRS = 0.5 \times 1/f_{SYS}$ (Default) |
| 01 | $TCRS = 1.5 \times 1/f_{SYS}$           |
| 10 | $TCRS = 2.5 \times 1/f_{SYS}$           |
| 11 | $TCRS = 3.5 \times 1/f_{SYS}$           |

TCRS: The delay from CSn to RD,SRxxB.

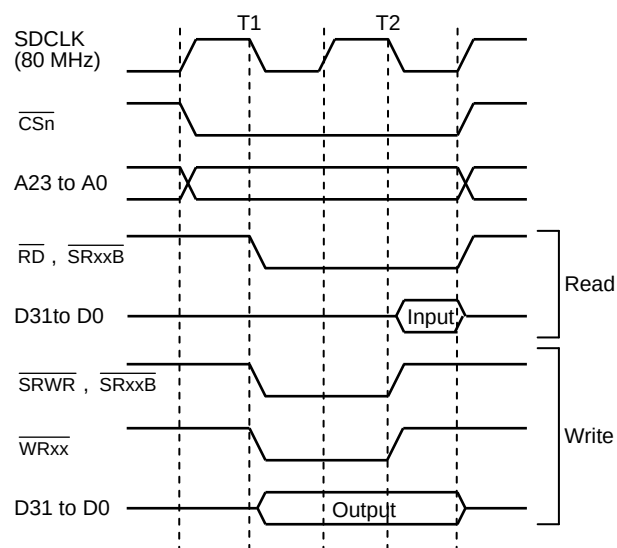


Note1: Wait states (TWs) are inserted as specified by the BnCSL register. No TW is inserted if the number of wait state is specified as zero.

Note2: Above diagram shows case of 32-bit bus access.

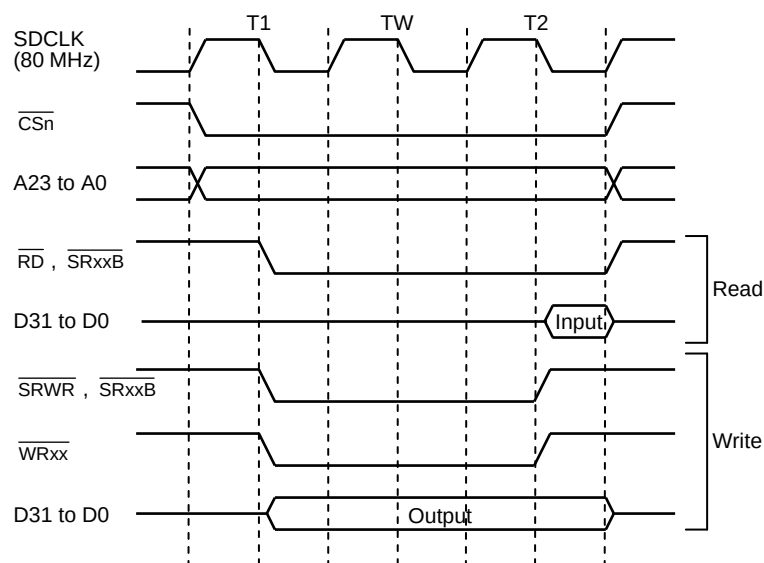
## (7) Basic bus timing

## (a) External bus read/write cycle (0 wait state)



Note: Above diagram shows case of 32-bit bus access.

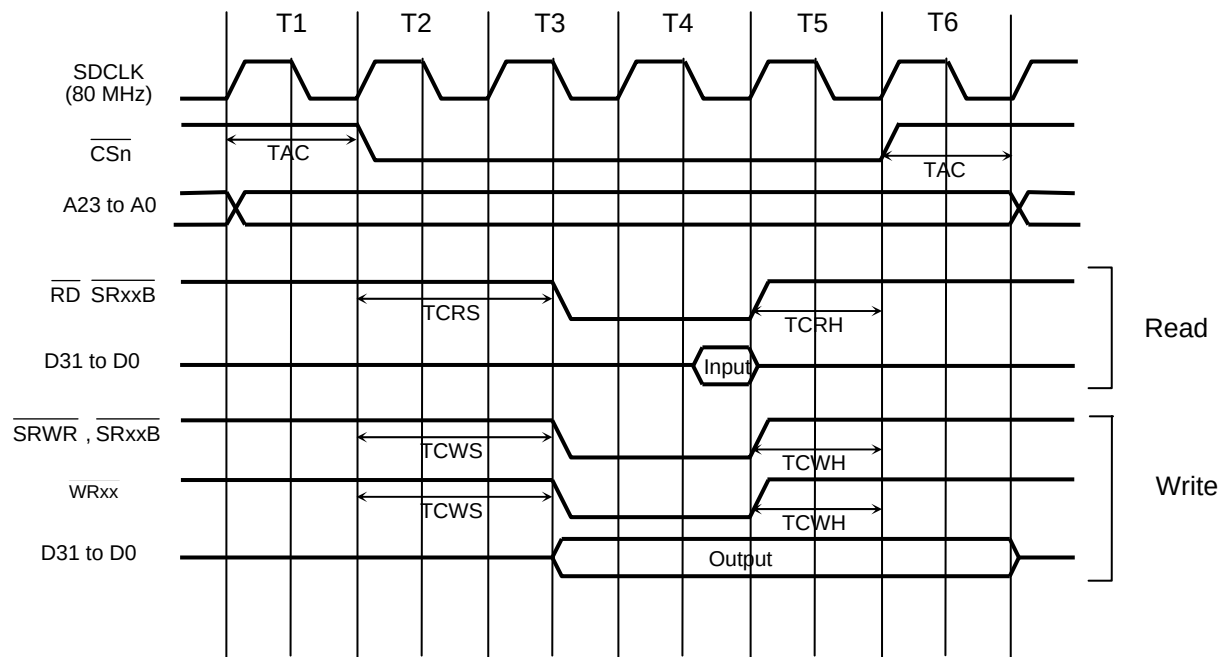
## (b) External bus read/write cycle (1 wait state)



Note: Above diagram shows case of 32-bit bus access.

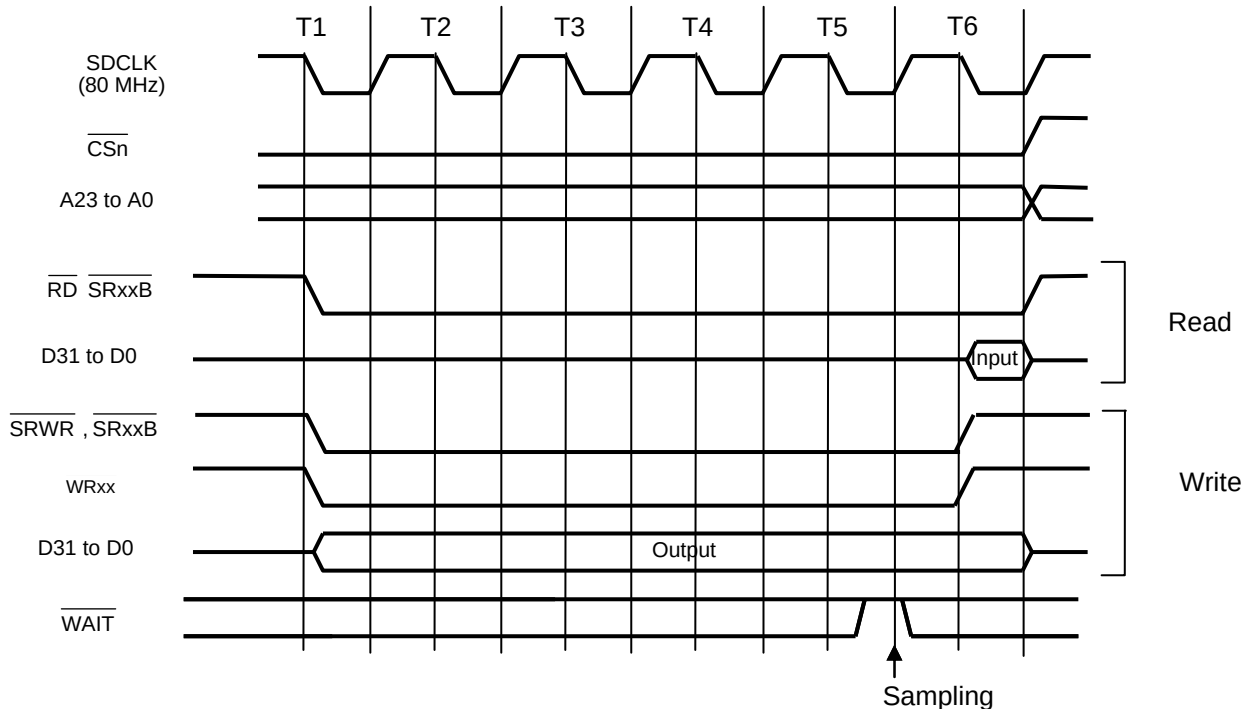
- (c) External bus read cycle (1 wait state + TAC:  $1 \times 1/f_{\text{SYS}}$  + TCRS:  $1.5 \times 1/f_{\text{SYS}}$  + TCRH:  $1 \times 1/f_{\text{SYS}}$ )

External bus write cycle (1 wait state + TAC:  $1 \times 1/f_{\text{SYS}}$  + TCWS/H:  $1.5 \times 1/f_{\text{SYS}}$ )



Note: Above diagram shows case of 32-bit bus access.

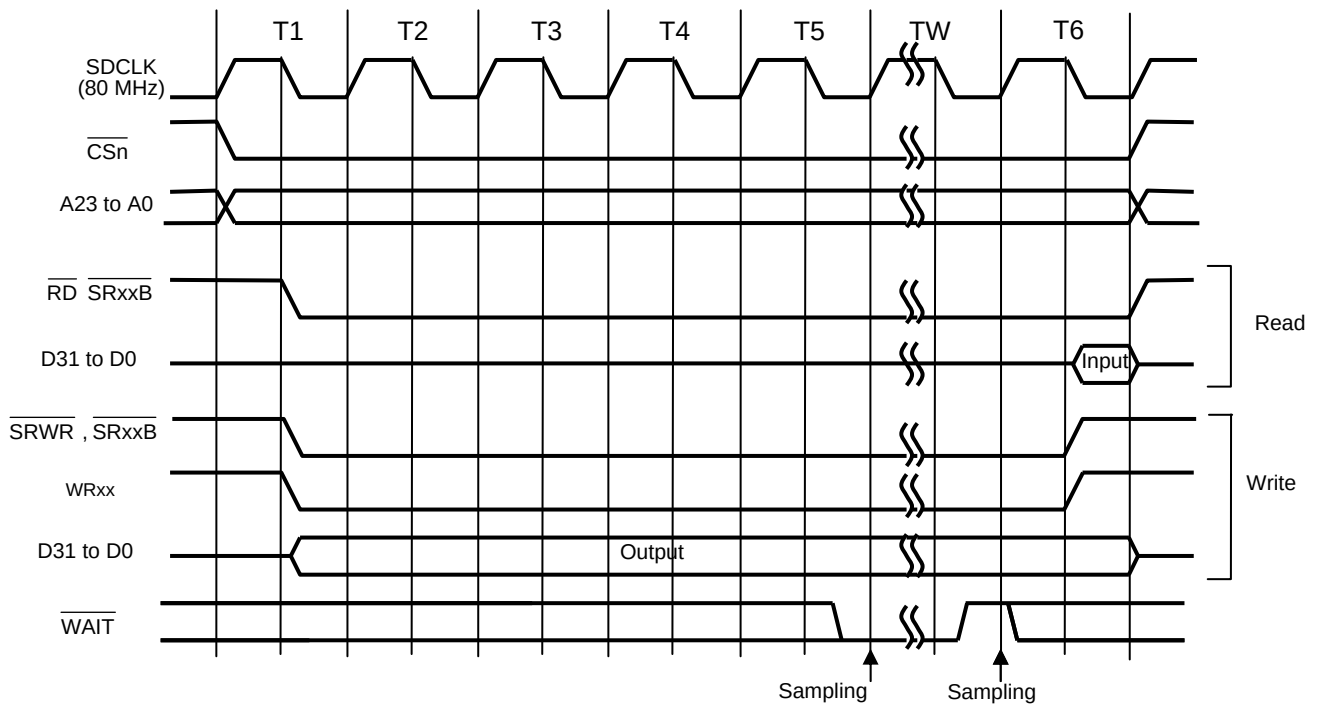
- (d) External bus read/write cycle (4 wait states +  $\overline{\text{WAIT}}$  pin input mode)



Note: Above diagram shows case of 32-bit bus access.

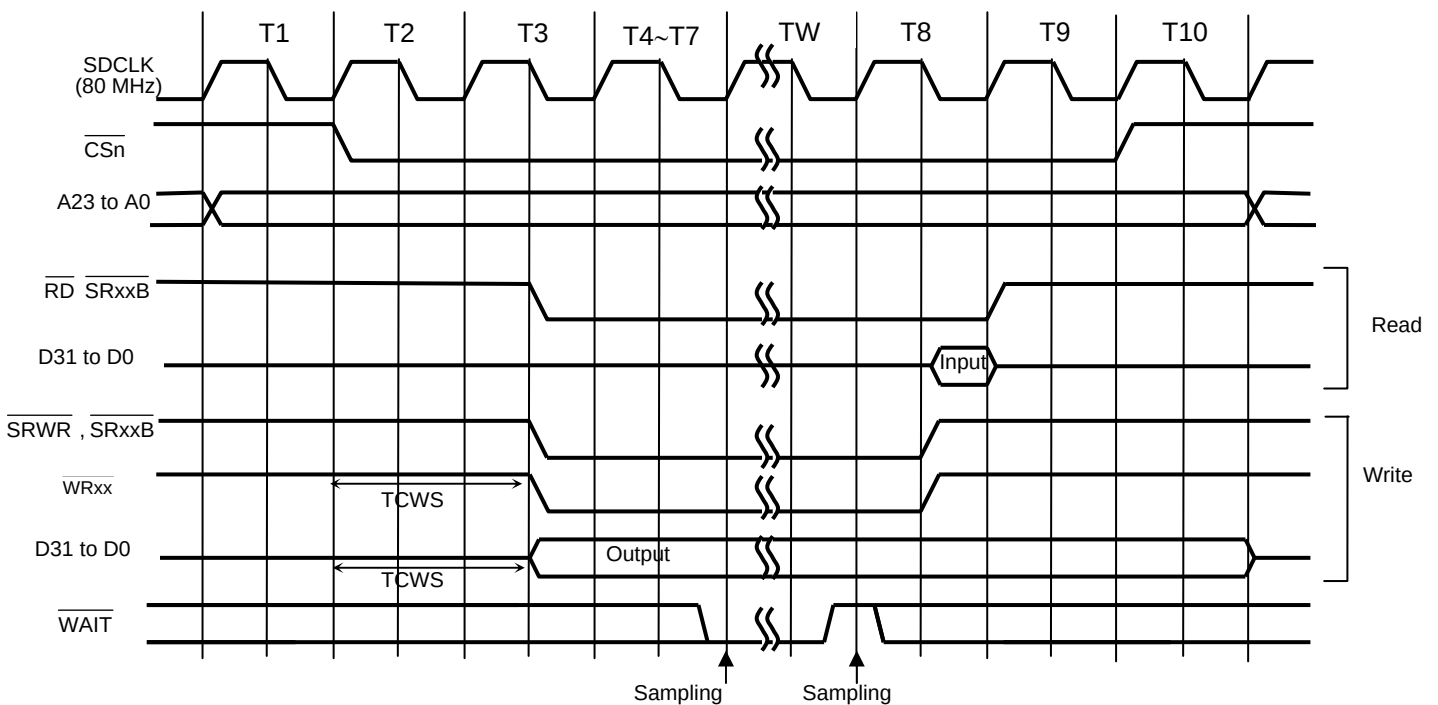


(e) External bus read/write cycle (4 wait states +  $\overline{\text{WAIT}}$  pin input mode)



Note: Above diagram shows case of 32-bit bus access.

(f) External bus read cycle (4 wait states +  $\overline{\text{WAIT}}$  pin input mode + TAC:  $1 \times 1/f_{\text{SYS}}$   
+ TCRS:  $1.5 \times 1/f_{\text{SYS}}$  + TCRH:  $1 \times 1/f_{\text{SYS}}$ )  
External bus write cycle (4 wait states +  $\overline{\text{WAIT}}$  pin input mode + TAC:  $1 \times 1/f_{\text{SYS}}$   
+ TCWS/H:  $1.5 \times 1/f_{\text{SYS}}$ )



Note: Above diagram shows case of 32-bit bus access.

## (8) External memory connections

Figure 3.8.4 shows an example of how to connect external 16-bit SRAM and 16-bit NOR flash to the TMP92CF30.

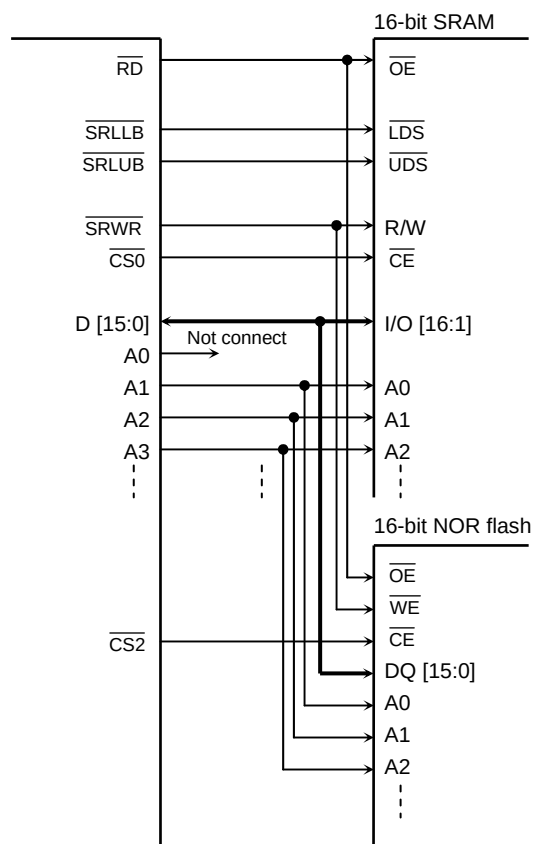


Figure 3.8.4 Example of External 16-Bit SRAM and NOR Flash Connection

### 3.8.4 Controlling the Page Mode Access to ROM

This section describes page mode access operations to ROM and the required register settings. The page mode operation to ROM is specified by PMEMCR.

#### (1) Operations and register settings

The TMP92CF30 supports page mode accesses to ROM. Only the CS2 space can be configured for this mode of access. The page mode operation to ROM is specified by the Page ROM Control register, PMEMCR.

Setting the PMEMCR<OPGE> bit to 1 sets the mode of memory access to the CS2 space to page mode.

The number of cycles required for a read cycle is specified by the PMEMCR<OPWR1:OPWR0> bits.

PMEMCR<OPWR1:OPWR0>

| <OPWR1> | <OPWR0> | Number of Cycles in Page Mode          |
|---------|---------|----------------------------------------|
| 0       | 0       | 1 cycle (n-1-1-1 mode) ( $n \geq 2$ )  |
| 0       | 1       | 2 cycles (n-2-2-2 mode) ( $n \geq 3$ ) |
| 1       | 0       | 3 cycles (n-3-3-3 mode) ( $n \geq 4$ ) |
| 1       | 1       | 4 cycles (n-4-4-4 mode) ( $n \geq 5$ ) |

Note: Specify the number of wait states (n) using the control register (BnCSL) for each address space.

The page size (the number of bytes) of ROM as seen from the CPU is determined by PMEMCR<PR1:PR0>. When the specified page boundary is reached, the controller terminates the page read operation. The first data of the next page is read in the normal mode. Then, the following data is read again in page mode.

PMEMCR<PR1:PR0>

| <PR1> | <PR0> | ROM Page Size      |
|-------|-------|--------------------|
| 0     | 0     | 64 bytes           |
| 0     | 1     | 32 bytes           |
| 1     | 0     | 16 bytes (Default) |
| 1     | 1     | 8 bytes            |

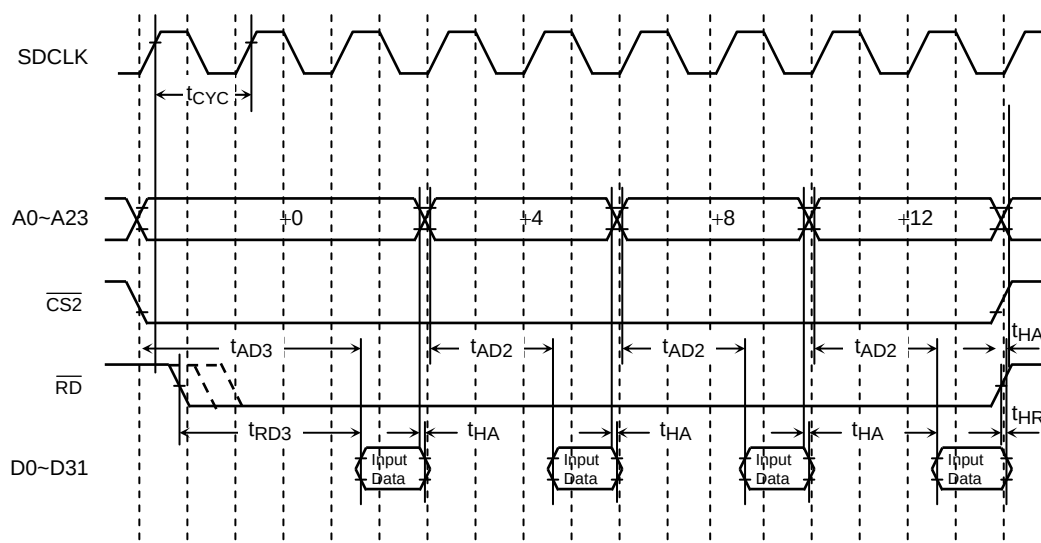


Figure 3.8.5 Page Mode Access Timing (when using a 16-byte page size)

## 3.8.5 Notes

(1) Timing for the  $\overline{CS}$  and  $\overline{RD}$  signals

If the load capacitance of the  $\overline{RD}$  (Read) signal line is greater than that of the  $\overline{CS}$  (Chip Select) signal line, the deassertion timing of the read signal is delayed, which may lead to an unintentional extension of a read cycle. Such an unintended read cycle extension, which is indicated as (a) in Figure 3.8.6, may cause a problem.

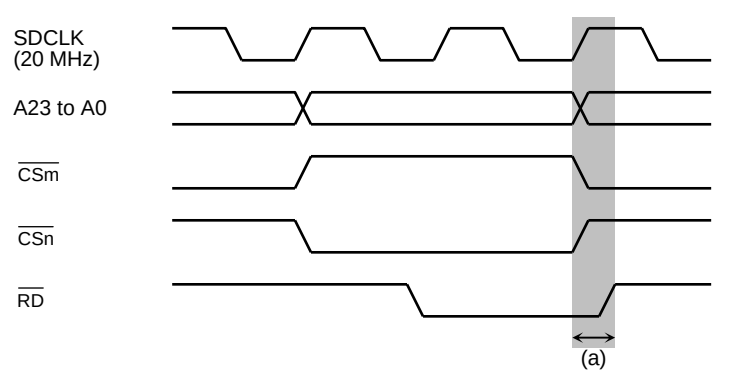


Figure 3.8.6 Read Cycle of When the Read Signal is Delayed

Example: When using an externally connected NOR flash whose commands are compatible with the standard JEDEC commands, the toggle bit may not be read correctly. If the rising edge of the read signal in the cycle immediately preceding the NOR flash access cycle does not occur in time, a read cycle may be extended unintentionally as indicated as (b) in Figure 3.8.7.

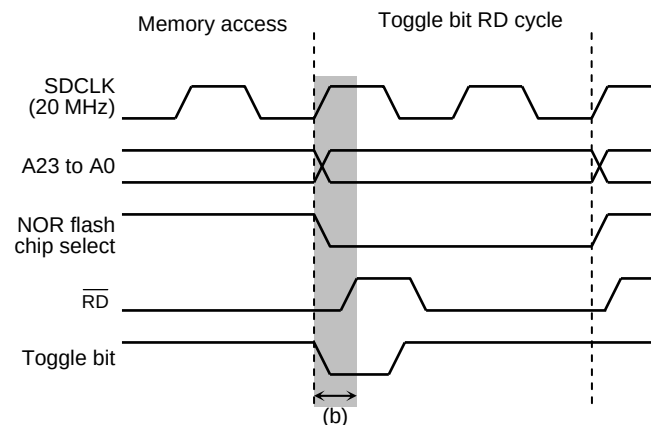


Figure 3.8.7 NOR Flash Toggle Bit Read Cycle

When the toggle bit is inverted due to this unexpected read cycle extension, the CPU cannot read the toggle bit properly and it always reads the same value from the toggle bit.

To avoid this situation, it is recommended to perform data polling or to use the timing adjustment function for the rising edge of the  $\overline{RD}$  signal (RDTMGCRn <BnTCRH1:BnTCRH0>).

## (2) Setting up the NAND flash area

Figure 3.8.8 shows a memory map for the NAND flash memory.

Since it is recommended that the CS3 space be located in the memory area from 000000H to 3FFFFFFH, the following description is provided for such condition. In this case, the NAND flash area overlaps with the CS3 space. However, the  $\overline{\text{CS3}}$  pin is not asserted by setting the BROMCR<CSDIS> bit to 1. Likewise, the  $\overline{\text{CS0}}$  through  $\overline{\text{CS3}}$  pins, the  $\overline{\text{CSXA}}$  through  $\overline{\text{CSXB}}$  pins and the  $\overline{\text{CSZA}}$  through  $\overline{\text{CSZD}}$  pins are not asserted either.

Note 1: In the above setting, 296 Kbytes out of the memory area for the CS3 (000000H to 049FFFFH) cannot be used.

Note 2: The 16-byte area (001FF0H to 001FFFFH) is predefined as NAND Flash area as shown below regardless of which CS space is selected. Therefore, the setting of the CS3 space does not affect the NAND flash area. (NAND-Flash area specification)

1. Bus width : Specified by NDFMCR1<BUSW> in the NAND Flash controller.
2. Wait control : Specified by NDFMCR<SPLW1:SPLW0> and NDFMCR<SPHW1:SPHW0> in the NAND Flash controller

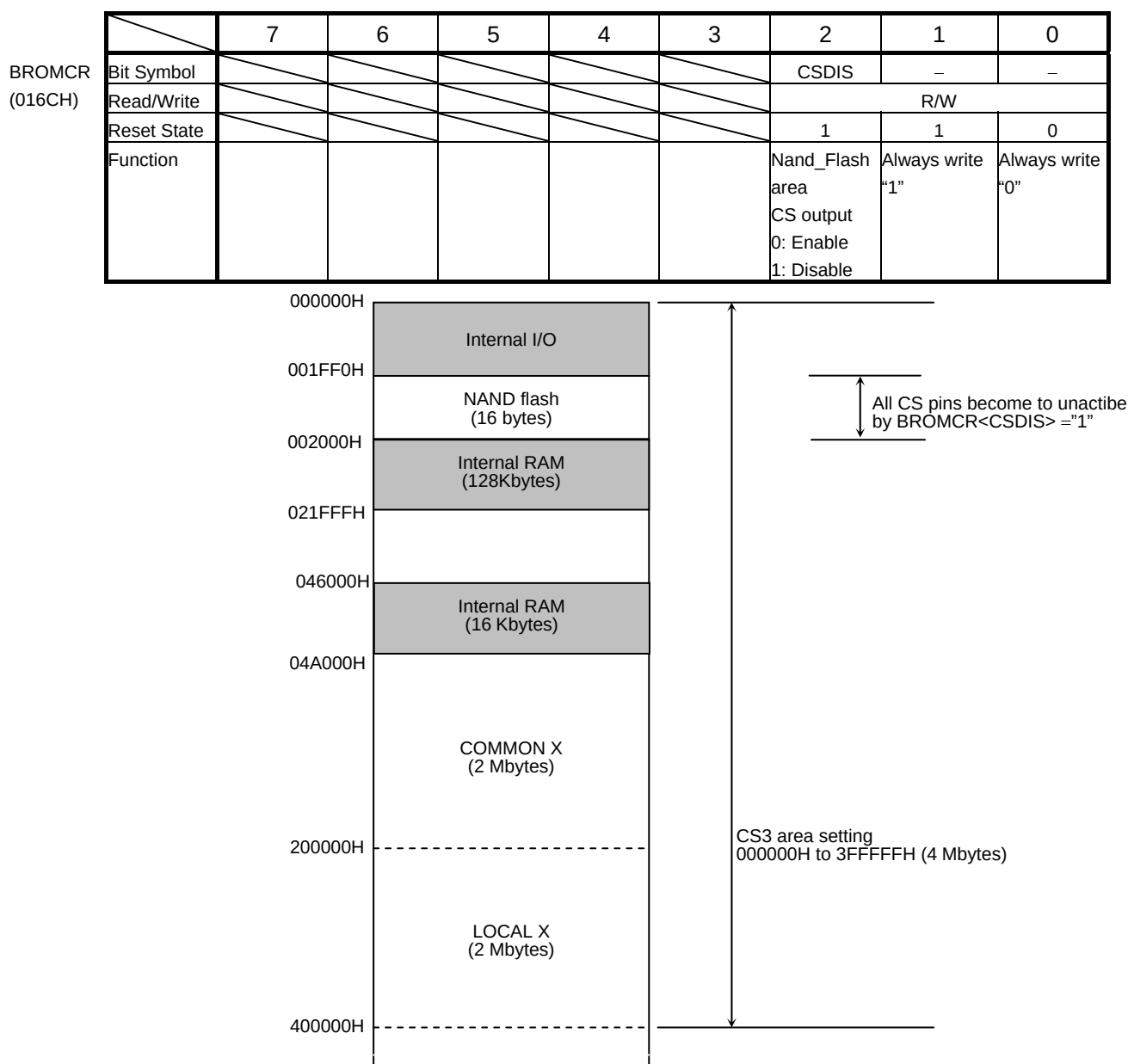


Figure 3.8.8 Recommended CS3 Space Assignment

## (3) Setting up the NAND flash area

In case of using SDRAM (SDCS) and NAND flash together, the BROMCR<CSDIS> bit cannot be used. This section provides an example of such cases.

It is recommended that the memory area from 000000H to 3FFFFFFH be assigned to the CS2 or CS1 (SDCS) space. A detailed description is provided below.

In this case, the NAND flash area overlaps with the CS2 or CS1 (SDCS) space.

So, if a program accesses NAND flash, the CS2 or CS1 space and NAND flash space are accessed at the same time, which leads to problems such as a data conflict.

To avoid this, it is recommended that the 32-Kbyte memory area from 000000H to 007FFFH be assigned to the CS0 space. (The  $\overline{CS0}$  pin is not required.)

Since the CS0 setting has higher priority over the settings of the CS2 and CS1 spaces, only NAND flash will be accessed without causing data conflicts.

Note: In this case, the 32-Kbyte memory area from 000000H to 007FFFH within the SDCS space cannot be used.

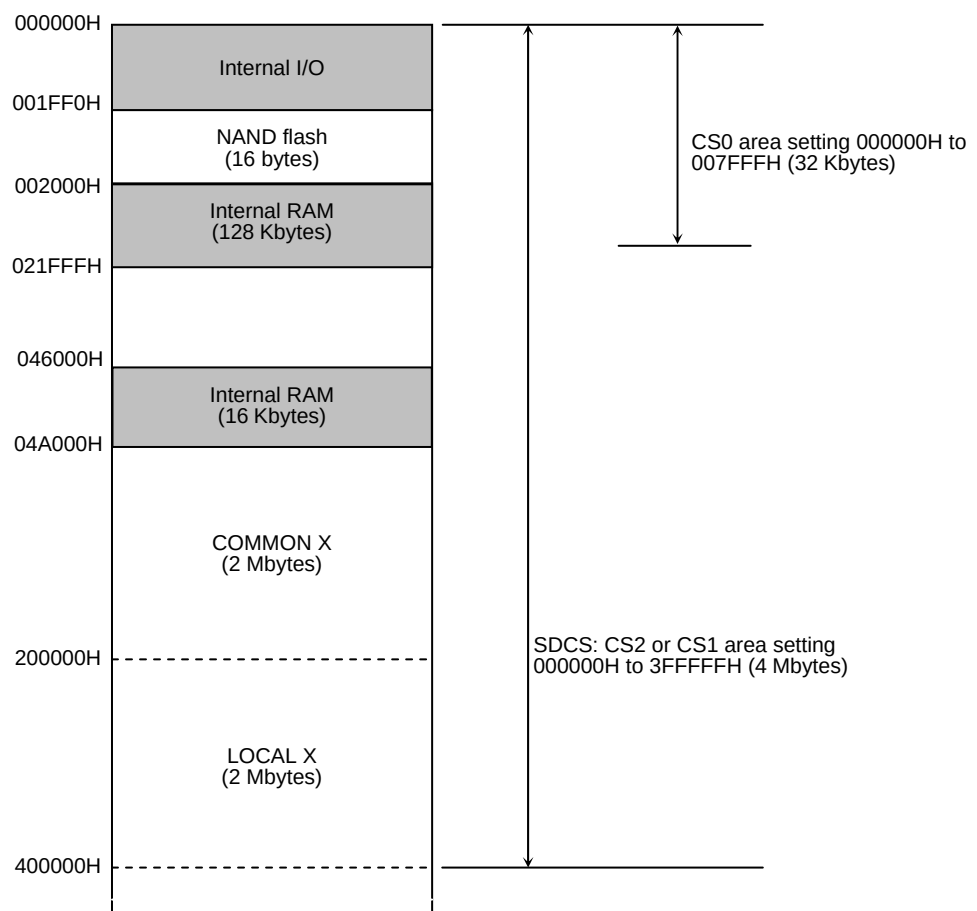


Figure 3.8.9 Recommended Assignment for the SDCS and CS0 Spaces

### 3.9 External Memory Extension (MMU)

The MMU allows for memory expansion by providing three local memory areas, the MMU function allows for the expansion of the program/data area to 2.1Gbytes.

For recommended address memory maps, refer to Figure 3.9.1.

However, when the amount of memory being used is less than 16 Mbytes, it is not necessary to configure the MMU register. For such cases, please refer to the section on the Memory controller.

A memory area which can be configured into banks is called the LOCAL area. The address range assigned to the LOCAL area is predefined and cannot be changed.

And the rest of the memory area is called the COMMON area.

Basically, a series of program routines should be stored entirely within one bank. The program execution cannot be branched between different banks of the same LOCAL area using the JP instruction. For more details, refer to the following programming examples.

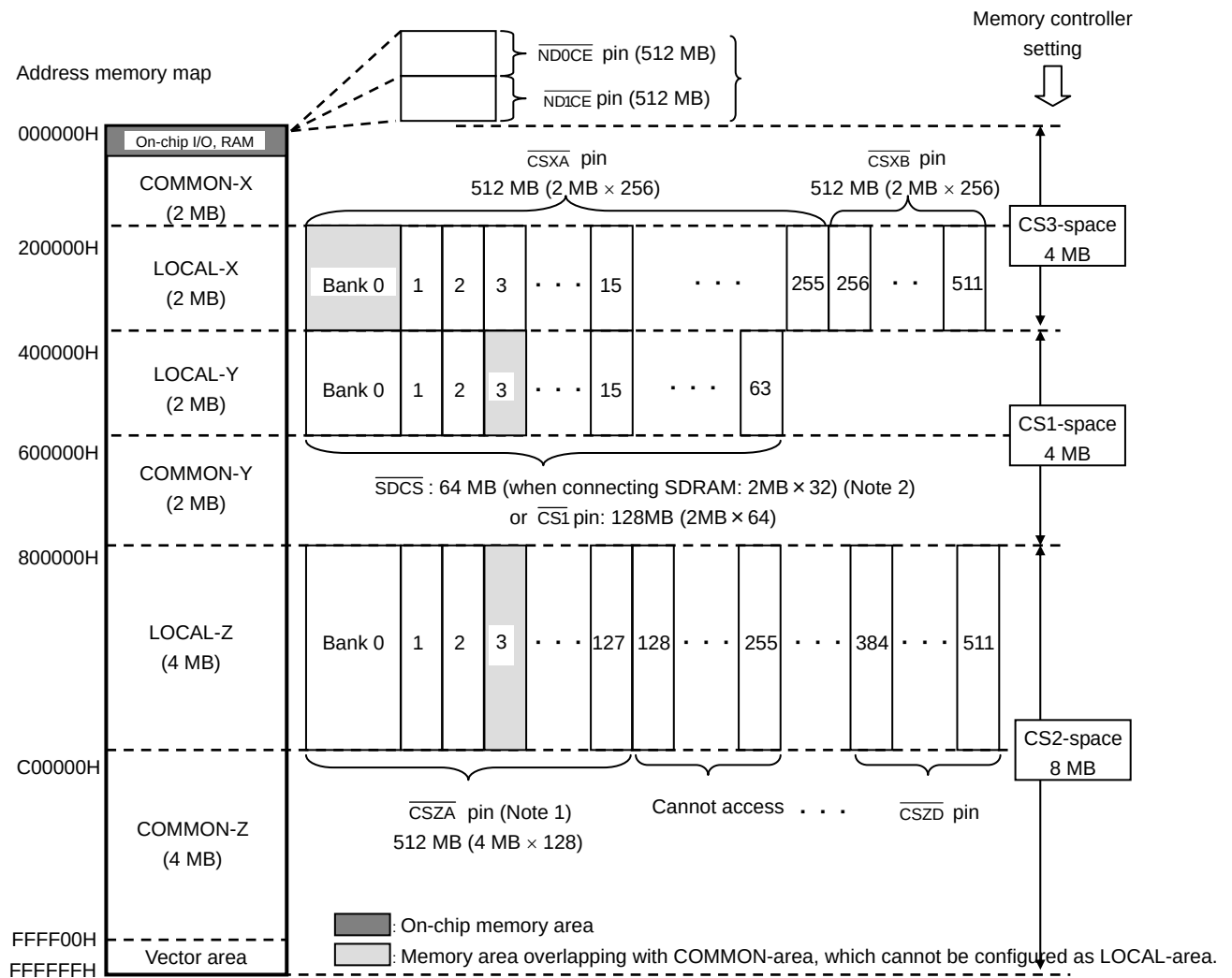
The TMP92CF30 has the following external pins for connecting external memory.

- Address bus: EA28, EA27, EA26, EA25, EA24 and A23 to A0
- Chip Select:  $\overline{\text{CS0}}$  to  $\overline{\text{CS3}}$ ,  $\overline{\text{CSXA}}$  to  $\overline{\text{CSXB}}$ ,  $\overline{\text{CSZA}}$  to  $\overline{\text{CSXD}}$ ,  $\overline{\text{SDCS}}$ ,  $\overline{\text{ND0CE}}$  and  $\overline{\text{NDICE}}$
- Data bus: D31 to D0

Note: This device is a subset microcontroller of 900H1 series microcontroller: TMP92CZ26AXBG and TMP92CF26A. The total memory size of this device was cut from 3.1GByte to 2.1G byte because number of pins was cut, and BANK of Z-area was cut from 512 banks to 256 banks.

#### 3.9.1 Recommended Memory Map

Figure 3.9.1 shows one of recommended address memory maps. This is an example of when memory is expanded to the maximum size.

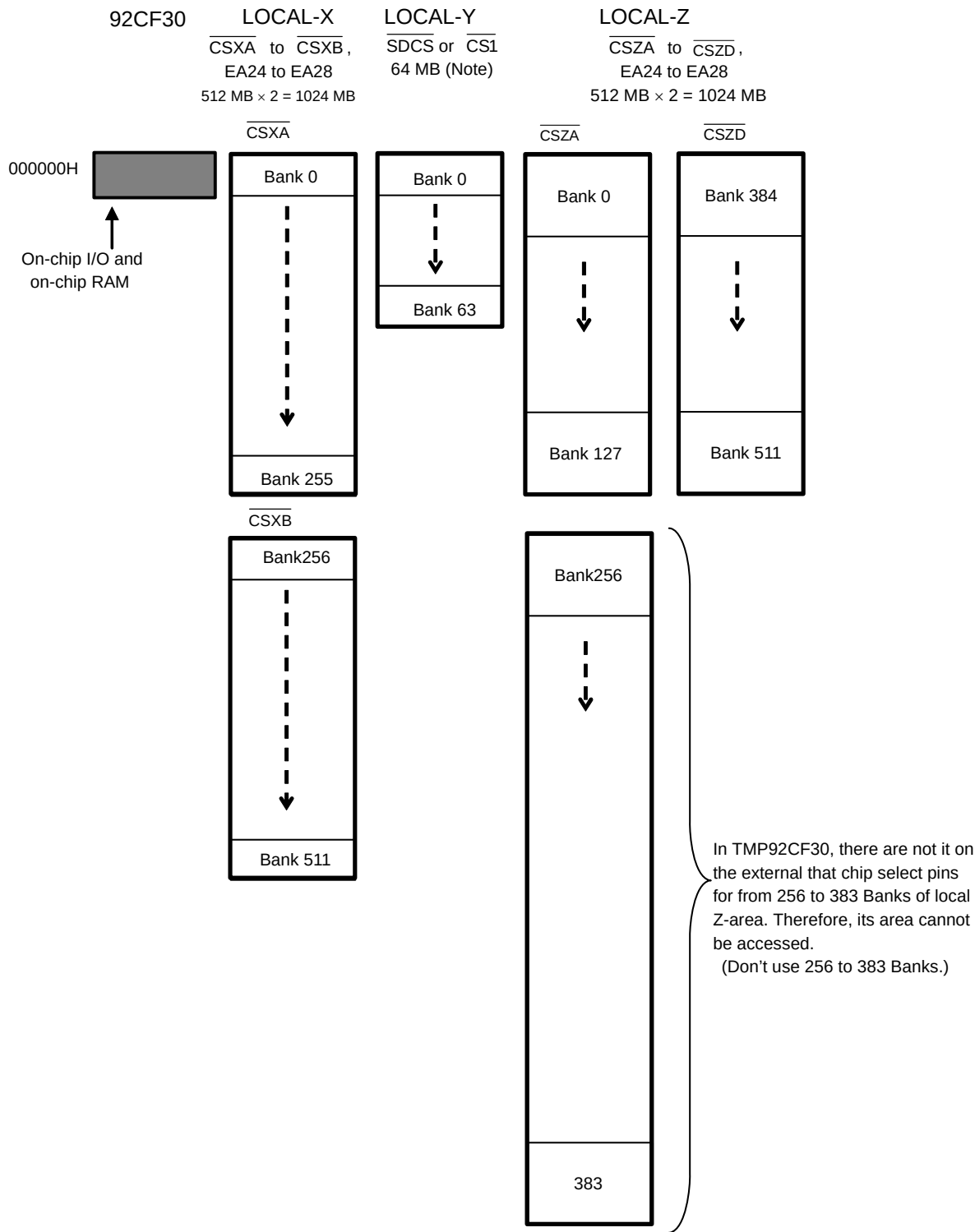


Note1: CSZA is a chip-select signal for not only bank 0 through bank 127 of the LOCAL-Z area, but also for the COMMON-Z area.

Note2: In case of connecting SDRAM to the Y-area, the maximum expanded memory size is 64 MB (2 MB × 32).

Figure 3.9.1 Recommended Memory Map for the Maximum Expansion (Logical address)





Note: In case of connecting SDRAM to the Y-area, the maximum expanded memory size is 64MB (2MB×32).

Figure 3.9.2 Recommended Memory Map for the Maximum Expansion (Physical address)

### 3.9.2 Control registers

The TMP92CF30 MMU has 21 registers. These registers are used for storing seven types of data (program, read data, write data, source data for DMA channels of odd/even number, destination-data for DMA channels of odd/even number) for each of three-LOCAL areas (LOCAL-X through LOCAL-Z). These registers allow for easy data access.

(How to use the control registers)

First, load the control registers for each LOCAL area with the desired bank number and enable/disable the specified bank. Then, configure the external pins to be used and also the Memory Controller. Then, when the CPU accesses a logical address in the LOCAL area, the MMU translates the logical address to the corresponding physical address according to the programmed bank configuration. The physical address is then placed on the external address bus pin, which enables external memory accesses. Thus, even when a program accesses the same logical address, its physical address changes depending on the bank specified by the program bank register. This enables memory accesses to the different memory banks.

Note1: When programming the bank registers, the bank area that is overlapping with the COMMON area must not be specified ( because addresses of those areas are converted to the same physical addresses).

Note2: In the LOCAL area, changing Program bank number (LOCALPX, Y or Z) is disabled. Program bank setting of each LOCAL area must change in COMMON area. (But bank setting of data-Read and data-Write can change also in LOCAL area.)

Note3: After setting values specifying the data bank number into bank registers for the read, write and DMA data (LOCALRn, LOCALWn or LOCALLn, LOCALESn, LOCALEDn, LOCALOSn, LOCALODn; the symbol "n" indicates X, Y or Z), the specified bank requires a certain setup time to be enabled. Thus, the bank cannot be accessed by an instruction immediately following the register setting instructions. In this case, insert a dummy instruction which accesses SFR or another memory area as shown in the following example.

(Example)

|     |                  |                                                       |
|-----|------------------|-------------------------------------------------------|
| ld  | xix, 200000h     | ;                                                     |
| ldw | (localrx), 8001h | ; Specify the read-data bank number                   |
| ldw | wa, (localrx)    | ; ← Inserted dummy instruction which accesses SFR     |
| ldw | wa, (xix)        | ; instruction which reads bank 1 of the LOCAL-X area. |

Note4: When the LOCAL-Z area is used, pin P82 should be assigned as the chip select signal  $\overline{\text{CSZA}}$ . In this case,  $\overline{\text{CSZA}}$  works as the chip select signal for the bank 0 through the bank 15, and also for the COMMON-Z area.

After reset, pin P82 should be properly configured following the procedure below.

|     |                          |                                                     |
|-----|--------------------------|-----------------------------------------------------|
| ldw | (localpz), 8000h         | ; Enable the banks in LOCAL-Z for program           |
| ldw | (localrz), 8000h         | ; Enable the banks in LOCAL-Z for read data         |
| ldw | (localwz), 8000h         | ; Enable the banks in LOCAL-Z for write data (*1)   |
| ld  | (P8FC), -- -- -- 0 -- B  | ; Assign P82 as the $\overline{\text{CSZA}}$ output |
| ld  | (P8FC2), -- -- -- 1 -- B |                                                     |

(\*1) This setting is not required if the COMMON-Z area is not used to store write data.

## 3.9.2.1 Program bank registers

These registers should be loaded with bank number values to specify the bank to be used as program memory. As described above, the program execution cannot be directly branched to a different bank in the same LOCAL area. The bank switching within the same LOCAL area is prohibited.

LOCAL-X Register for Program

|                    |             |                                                                                                                                            |                                                                                                                                                                                              |             |             |             |             |             |     |
|--------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-------------|-------------|-------------|-------------|-----|
| LOCALPX<br>(0880H) | <div></div> | 7                                                                                                                                          | 6                                                                                                                                                                                            | 5           | 4           | 3           | 2           | 1           | 0   |
|                    | Bit Symbol  | X7                                                                                                                                         | X6                                                                                                                                                                                           | X5          | X4          | X3          | X2          | X1          | X0  |
|                    | Read/Write  | R/W                                                                                                                                        |                                                                                                                                                                                              |             |             |             |             |             |     |
|                    | Reset State | 0                                                                                                                                          | 0                                                                                                                                                                                            | 0           | 0           | 0           | 0           | 0           | 0   |
|                    | Function    | Specify the bank number for the LOCAL-X area<br>(Since bank 0 is overlapping with the COMMON area, this filed must not be specified as 0.) |                                                                                                                                                                                              |             |             |             |             |             |     |
| (0881H)            | <div></div> | 15                                                                                                                                         | 14                                                                                                                                                                                           | 13          | 12          | 11          | 10          | 9           | 8   |
|                    | Bit Symbol  | LXE                                                                                                                                        | <div></div>                                                                                                                                                                                  | <div></div> | <div></div> | <div></div> | <div></div> | <div></div> | X8  |
|                    | Read/Write  | R/W                                                                                                                                        | <div></div>                                                                                                                                                                                  | <div></div> | <div></div> | <div></div> | <div></div> | <div></div> | R/W |
|                    | Reset State | 0                                                                                                                                          | <div></div>                                                                                                                                                                                  | <div></div> | <div></div> | <div></div> | <div></div> | <div></div> | 0   |
|                    | Function    | Bank for<br>LOCAL-X<br>0: Disable<br>1: Enable                                                                                             | Specify the bank number for the LOCAL-X area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>000000000 to 011111111 CSXA<br>100000000 to 111111111 CSXB |             |             |             |             |             |     |

LOCAL-Y Register for Program

|                    | 7           | 6                                              | 5                                                                                                                                          | 4  | 3  | 2  | 1  | 0  |
|--------------------|-------------|------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|
| LOCALPY<br>(0882H) | Bit Symbol  |                                                | Y5                                                                                                                                         | Y4 | Y3 | Y2 | Y1 | Y0 |
|                    | Read/Write  |                                                | R/W                                                                                                                                        |    |    |    |    |    |
|                    | Reset State |                                                | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0  |
|                    | Function    |                                                | Specify the bank number for the LOCAL-Y area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |    |    |    |    |    |
|                    | 15          | 14                                             | 13                                                                                                                                         | 12 | 11 | 10 | 9  | 8  |
| (0883H)            | Bit Symbol  | LYE                                            |                                                                                                                                            |    |    |    |    |    |
|                    | Read/Write  | R/W                                            |                                                                                                                                            |    |    |    |    |    |
|                    | Reset State | 0                                              |                                                                                                                                            |    |    |    |    |    |
|                    | Function    | Bank for<br>LOCAL-Y<br>0: Disable<br>1: Enable |                                                                                                                                            |    |    |    |    |    |

LOCAL-Z Register for Program

|                    |             |                                                                                                                                            |                                                                                                                                                                                                                                                                                                  |    |    |    |    |    |     |
|--------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|-----|
| LOCALPZ<br>(0884H) |             | 7                                                                                                                                          | 6                                                                                                                                                                                                                                                                                                | 5  | 4  | 3  | 2  | 1  | 0   |
|                    | Bit Symbol  | Z7                                                                                                                                         | Z6                                                                                                                                                                                                                                                                                               | Z5 | Z4 | Z3 | Z2 | Z1 | Z0  |
|                    | Read/Write  | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                                  |    |    |    |    |    |     |
|                    | Reset State | 0                                                                                                                                          | 0                                                                                                                                                                                                                                                                                                | 0  | 0  | 0  | 0  | 0  | 0   |
|                    | Function    | Specify the bank number for the LOCAL-Z area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |                                                                                                                                                                                                                                                                                                  |    |    |    |    |    |     |
| (0885H)            |             | 15                                                                                                                                         | 14                                                                                                                                                                                                                                                                                               | 13 | 12 | 11 | 10 | 9  | 8   |
|                    | Bit Symbol  | LZE                                                                                                                                        |                                                                                                                                                                                                                                                                                                  |    |    |    |    |    | Z8  |
|                    | Read/Write  | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                                  |    |    |    |    |    | R/W |
|                    | Reset State | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                                  |    |    |    |    |    | 0   |
|                    | Function    | Bank for<br>LOCAL-Z<br>0: Disable<br>1: Enable                                                                                             | Specify the bank number for the LOCAL-Z area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>00000000 to 00111111 CSZA                      10000000 to 10111111 Setting prohibited<br>01000000 to 01111111 Setting prohibited    11000000 to 11111111 CSZD |    |    |    |    |    |     |

## 3.9.2.2 Read-Data Bank Registers

These registers should be loaded with bank number values to specify the banks to be used as read-data memory. The following example shows how to specify bank 1 for storing read data in the LOCAL-X area. The instruction, “ldw wa, (xix),” reads the data from the memory location at the address xix and stores it into the wa register of the CPU. When loading the address xix into the read-data bank register, the bank is only enabled upon a data (operand) read operation for the memory location at the address xix.

(Example)

```
ld    xix, 200000h    ;
ld    (localrx), 8001h    ; Specify the read-data bank number.
ldw   wa, (localrx)    ; ← Insert a dummy instruction that accesses SFR
ldw   wa, (xix)        ; Read bank 1 of the LOCAL-X area
```

LOCAL-X Register for Read Data

|                    |             | 7                                                                                                                                          | 6                                                                                                                                                                                        | 5  | 4  | 3  | 2  | 1  | 0   |
|--------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|-----|
|                    |             | X7                                                                                                                                         | X6                                                                                                                                                                                       | X5 | X4 | X3 | X2 | X1 | X0  |
| LOCALRX<br>(0890H) | Bit Symbol  | R/W                                                                                                                                        |                                                                                                                                                                                          |    |    |    |    |    |     |
|                    | Read/Write  |                                                                                                                                            |                                                                                                                                                                                          |    |    |    |    |    |     |
|                    | Reset State | 0                                                                                                                                          | 0                                                                                                                                                                                        | 0  | 0  | 0  | 0  | 0  | 0   |
|                    | Function    | Specify the bank number for the LOCAL-X area<br>(Since bank 0 is overlapping with the COMMON area, this field must not be specified as 0.) |                                                                                                                                                                                          |    |    |    |    |    |     |
|                    |             | 15                                                                                                                                         | 14                                                                                                                                                                                       | 13 | 12 | 11 | 10 | 9  | 8   |
|                    |             | LXE                                                                                                                                        |                                                                                                                                                                                          |    |    |    |    |    | X8  |
| (0891H)            | Read/Write  | R/W                                                                                                                                        |                                                                                                                                                                                          |    |    |    |    |    | R/W |
|                    | Reset State | 0                                                                                                                                          |                                                                                                                                                                                          |    |    |    |    |    | 0   |
|                    | Function    | Bank for LOCAL-X<br>0: Disable<br>1: Enable                                                                                                | Specify the bank number for the LOCAL-X area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>00000000 to 01111111 CSXA<br>10000000 to 11111111 CSXB |    |    |    |    |    |     |
|                    |             |                                                                                                                                            |                                                                                                                                                                                          |    |    |    |    |    |     |

LOCAL-Y Register for Read Data

|                    |             | 7                                           | 6  | 5                                                                                                                                          | 4  | 3  | 2  | 1  | 0  |
|--------------------|-------------|---------------------------------------------|----|--------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|
|                    |             |                                             |    | Y5                                                                                                                                         | Y4 | Y3 | Y2 | Y1 | Y0 |
| LOCALRY<br>(0892H) | Read/Write  |                                             |    | R/W                                                                                                                                        |    |    |    |    |    |
|                    | Reset State |                                             |    | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0  |
|                    | Function    |                                             |    | Specify the bank number for the LOCAL-Y area<br>(Since bank 3 is overlapping with the COMMON area, this field must not be specified as 3.) |    |    |    |    |    |
|                    |             |                                             |    |                                                                                                                                            |    |    |    |    |    |
|                    |             | 15                                          | 14 | 13                                                                                                                                         | 12 | 11 | 10 | 9  | 8  |
|                    |             | LYE                                         |    |                                                                                                                                            |    |    |    |    |    |
| (0893H)            | Read/Write  | R/W                                         |    |                                                                                                                                            |    |    |    |    |    |
|                    | Reset State | 0                                           |    |                                                                                                                                            |    |    |    |    |    |
|                    | Function    | Bank for LOCAL-Y<br>0: Disable<br>1: Enable |    |                                                                                                                                            |    |    |    |    |    |
|                    |             |                                             |    |                                                                                                                                            |    |    |    |    |    |

| LOCAL-Z Register for Read Data |             |                                                                                                                                            |                                                                                                                                                                                                                                                                                  |    |    |    |    |       |
|--------------------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|-------|
| LOCALRZ<br>(0894H)             |             | 7                                                                                                                                          | 6                                                                                                                                                                                                                                                                                | 5  | 4  | 3  | 2  | 1 0   |
|                                | Bit Symbol  | Z7                                                                                                                                         | Z6                                                                                                                                                                                                                                                                               | Z5 | Z4 | Z3 | Z2 | Z1 Z0 |
|                                | Read/Write  | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                  |    |    |    |    |       |
|                                | Reset State | 0                                                                                                                                          | 0                                                                                                                                                                                                                                                                                | 0  | 0  | 0  | 0  | 0     |
| (0895H)                        | Function    | Specify the bank number for the LOCAL-Z area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |                                                                                                                                                                                                                                                                                  |    |    |    |    |       |
|                                |             | 15                                                                                                                                         | 14                                                                                                                                                                                                                                                                               | 13 | 12 | 11 | 10 | 9 8   |
|                                | Bit Symbol  | LZE                                                                                                                                        |                                                                                                                                                                                                                                                                                  |    |    |    |    | Z8    |
|                                | Read/Write  | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                  |    |    |    |    | R/W   |
|                                | Reset State | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                  |    |    |    |    | 0     |
|                                | Function    | Bank for<br>LOCAL-Z<br>0: Disable<br>1: Enable                                                                                             | Specify the bank number for the LOCAL-Z area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>000000000 to 001111111 CSZA 100000000 to 101111111 Setting prohibited<br>010000000 to 011111111 Setting prohibited 110000000 to 111111111 CSZD |    |    |    |    |       |

## 3.9.2.3 Write-Data Bank Registers

These registers should be loaded with bank number values to specify the banks to be used as write data memory. The following example shows how to specify bank 1 for storing write data in the LOCAL-X area. The instruction, “ldw (xix), wa,” writes the wa register value of the CPU into the memory location at the address xix. When loading the address xix into the read-data bank register, the bank is only enabled upon a data (operand) write operation for the memory location at the address xix.

(Example)

```
ld      xix, 200000h      ;
ld      (localwx), 8001h  ; Specify the write-data bank number.
ldw     wa, (localwx)     ; ← Insert a dummy instruction that accesses SFR
ldw     (xix), wa         ; Write to bank 1 of the LOCAL-X area
```

LOCAL-X Register for Write Data

|                    |             | 7                                                                                                                                                                                            | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
|--------------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|-----|
|                    |             | X7                                                                                                                                                                                           | X6 | X5 | X4 | X3 | X2 | X1 | X0  |
| LOCALWX<br>(0898H) | Bit Symbol  | R/W                                                                                                                                                                                          |    |    |    |    |    |    |     |
|                    | Read/Write  | R/W                                                                                                                                                                                          |    |    |    |    |    |    |     |
|                    | Reset State | 0                                                                                                                                                                                            | 0  | 0  | 0  | 0  | 0  | 0  | 0   |
|                    | Function    | Specify the bank number for the LOCAL-X area<br>(Since bank 0 is overlapping with the COMMON area, this field must not be specified as 0.)                                                   |    |    |    |    |    |    |     |
|                    |             | 15                                                                                                                                                                                           | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
|                    |             | LXE                                                                                                                                                                                          |    |    |    |    |    |    | X8  |
| (0899H)            | Read/Write  | R/W                                                                                                                                                                                          |    |    |    |    |    |    | R/W |
|                    | Reset State | 0                                                                                                                                                                                            |    |    |    |    |    |    | 0   |
|                    | Function    | Specify the bank number for the LOCAL-X area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>000000000 to 011111111 CSXA<br>100000000 to 111111111 CSXB |    |    |    |    |    |    |     |
|                    |             | Bank for LOCAL-X<br>0: Disable<br>1: Enable                                                                                                                                                  |    |    |    |    |    |    |     |

LOCAL-Y Register for Write Data

|                    |             | 7                                           | 6  | 5                                                                                                                                          | 4  | 3  | 2  | 1  | 0  |
|--------------------|-------------|---------------------------------------------|----|--------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|
|                    |             |                                             |    | Y5                                                                                                                                         | Y4 | Y3 | Y2 | Y1 | Y0 |
| LOCALWY<br>(089AH) | Read/Write  |                                             |    | R/W                                                                                                                                        |    |    |    |    |    |
|                    | Reset State |                                             |    | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0  |
|                    | Function    |                                             |    | Specify the bank number for the LOCAL-Y area<br>(Since bank 3 is overlapping with the COMMON area, this field must not be specified as 3.) |    |    |    |    |    |
|                    |             | 15                                          | 14 | 13                                                                                                                                         | 12 | 11 | 10 | 9  | 8  |
|                    |             | LYE                                         |    |                                                                                                                                            |    |    |    |    |    |
| (089BH)            | Read/Write  | R/W                                         |    |                                                                                                                                            |    |    |    |    |    |
|                    | Reset State | 0                                           |    |                                                                                                                                            |    |    |    |    |    |
|                    | Function    | Bank for LOCAL-Y<br>0: Disable<br>1: Enable |    |                                                                                                                                            |    |    |    |    |    |
|                    |             |                                             |    |                                                                                                                                            |    |    |    |    |    |

LOCAL-Z Register for Write Data

|                    |             |                                                                                                                                            |                                                                                |                    |                        |                    |    |    |     |
|--------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------|--------------------|------------------------|--------------------|----|----|-----|
| LOCALWZ<br>(089CH) |             | 7                                                                                                                                          | 6                                                                              | 5                  | 4                      | 3                  | 2  | 1  | 0   |
|                    | Bit Symbol  | Z7                                                                                                                                         | Z6                                                                             | Z5                 | Z4                     | Z3                 | Z2 | Z1 | Z0  |
|                    | Read/Write  | R/W                                                                                                                                        |                                                                                |                    |                        |                    |    |    |     |
|                    | Reset State | 0                                                                                                                                          | 0                                                                              | 0                  | 0                      | 0                  | 0  | 0  | 0   |
|                    | Function    | Specify the bank number for the LOCAL-Z area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |                                                                                |                    |                        |                    |    |    |     |
| (089DH)            |             | 15                                                                                                                                         | 14                                                                             | 13                 | 12                     | 11                 | 10 | 9  | 8   |
|                    | Bit Symbol  | LZE                                                                                                                                        |                                                                                |                    |                        |                    |    |    | Z8  |
|                    | Read/Write  | R/W                                                                                                                                        |                                                                                |                    |                        |                    |    |    | R/W |
|                    | Reset State | 0                                                                                                                                          |                                                                                |                    |                        |                    |    |    | 0   |
|                    | Function    | Bank for<br>LOCAL-Z                                                                                                                        | Specify the bank number for the LOCAL-Z area                                   |                    |                        |                    |    |    |     |
|                    |             |                                                                                                                                            | Settings of the X8 through X0 bits and their corresponding chip select signals |                    |                        |                    |    |    |     |
|                    |             | 0: Disable                                                                                                                                 | 000000000 to 001111111                                                         | CSZA               | 100000000 to 101111111 | Setting prohibited |    |    |     |
|                    |             | 1: Enable                                                                                                                                  | 010000000 to 011111111                                                         | Setting prohibited | 110000000 to 111111111 | CSZD               |    |    |     |

### 3.9.2.4 DMA-Function Bank Registers

The TMP92CF30 supports not only the read and write operations of the CPU, but also the high-speed data transfer by enabling the internal DMAC to become the bus master. (Please refer to Section 3.7, “DMA Controller”).

These registers are provided specially for the DMA operation, separately from the bank registers for the CPU. Regardless of the settings of the bank registers for program, read and write data of the CPU, the banks to be used as source address memory and destination address memory are specified individually during DMA operations.

The DMAC of the TMP92CF30 supports six channels, and the bank control is performed by dividing those channels into 2 groups. The DMA channels with the even-channel number, 0, 2 and 4, are classified into the E-group (ES and ED groups); while the channels with the odd-channel number, 1 and 3, are classified into the O-group (OS and OD groups). These registers cannot specify bank numbers for each channel, but specifies one bank number for all the channels in the same group.

The following example shows how to specify bank 1 for storing DMA-source addresses in the LOCAL-X area, and also specify bank 2 for storing DMA-destination addresses in the LOCAL-Y area. If the DMA operation for channel 0 is initiated Assume that the source and destination addresses specified by the DMA operation, which is described in Section 3.7, are set into the LOCAL-X and LOCAL-Y areas, respectively. Then, if the DMA operation for channel 0 is initiated, bank 1 in the LOCAL-X area is configured as the source address memory, and bank 2 in the LOCAL-Y area is configured as the destination address memory.

(Example)

|     |                   |                                                     |
|-----|-------------------|-----------------------------------------------------|
| ldw | (localex), 8001h  | ; Specify DMA-source bank number for channel 0      |
| ldw | (localedy), 8002h | ; Specify DMA-destination bank number for channel 0 |

DMA operation for channel 0 is started



LOCAL-X Register for the E-group DMA Source

|                     |             |                                                                                                                                            |                                                                                                                                                                                          |    |    |    |    |    |    |
|---------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|
| LOCALESX<br>(08A0H) | Bit Symbol  | 7                                                                                                                                          | 6                                                                                                                                                                                        | 5  | 4  | 3  | 2  | 1  | 0  |
|                     | Read/Write  | X7                                                                                                                                         | X6                                                                                                                                                                                       | X5 | X4 | X3 | X2 | X1 | X0 |
|                     | Reset State | 0                                                                                                                                          | 0                                                                                                                                                                                        | 0  | 0  | 0  | 0  | 0  | 0  |
|                     | Function    | Specify the bank number for the LOCAL-X area<br>(Since bank 0 is overlapping with the COMMON area, this filed must not be specified as 0.) |                                                                                                                                                                                          |    |    |    |    |    |    |
| (08A1H)             | Bit Symbol  | 15                                                                                                                                         | 14                                                                                                                                                                                       | 13 | 12 | 11 | 10 | 9  | 8  |
|                     | Read/Write  | LXE                                                                                                                                        |                                                                                                                                                                                          |    |    |    |    |    | X8 |
|                     | Reset State | 0                                                                                                                                          |                                                                                                                                                                                          |    |    |    |    |    | 0  |
|                     | Function    | Bank for LOCAL-X<br>0: Disable<br>1: Enable                                                                                                | Specify the bank number for the LOCAL-X area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>00000000 to 01111111 CSXA<br>10000000 to 11111111 CSXB |    |    |    |    |    |    |

LOCAL-Y Register for the E-group DMA Source

|                     |             |                                             |    |                                                                                                                                            |    |    |    |    |    |
|---------------------|-------------|---------------------------------------------|----|--------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|
| LOCALESY<br>(08A2H) | Bit Symbol  | 7                                           | 6  | 5                                                                                                                                          | 4  | 3  | 2  | 1  | 0  |
|                     | Read/Write  |                                             |    | Y5                                                                                                                                         | Y4 | Y3 | Y2 | Y1 | Y0 |
|                     | Reset State |                                             |    | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0  |
|                     | Function    |                                             |    | Specify the bank number for the LOCAL-Y area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |    |    |    |    |    |
| (08A3H)             | Bit Symbol  | 15                                          | 14 | 13                                                                                                                                         | 12 | 11 | 10 | 9  | 8  |
|                     | Read/Write  | LYE                                         |    |                                                                                                                                            |    |    |    |    |    |
|                     | Reset State | 0                                           |    |                                                                                                                                            |    |    |    |    |    |
|                     | Function    | Bank for LOCAL-Y<br>0: Disable<br>1: Enable |    |                                                                                                                                            |    |    |    |    |    |

LOCAL-Z Register for the E-group DMA Source

|                     |             |                                                                                                                                           |                                                                                                                                                                                                                                                                                |    |    |    |    |    |    |
|---------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|
| LOCALESZ<br>(08A4H) | Bit Symbol  | 7                                                                                                                                         | 6                                                                                                                                                                                                                                                                              | 5  | 4  | 3  | 2  | 1  | 0  |
|                     | Read/Write  | Z7                                                                                                                                        | Z6                                                                                                                                                                                                                                                                             | Z5 | Z4 | Z3 | Z2 | Z1 | Z0 |
|                     | Reset State | 0                                                                                                                                         | 0                                                                                                                                                                                                                                                                              | 0  | 0  | 0  | 0  | 0  | 0  |
|                     | Function    | Specify the bank number for the LOCAL-Z area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3) |                                                                                                                                                                                                                                                                                |    |    |    |    |    |    |
| (08A5H)             | Bit Symbol  | 15                                                                                                                                        | 14                                                                                                                                                                                                                                                                             | 13 | 12 | 11 | 10 | 9  | 8  |
|                     | Read/Write  | LZE                                                                                                                                       |                                                                                                                                                                                                                                                                                |    |    |    |    |    | Z8 |
|                     | Reset State | 0                                                                                                                                         |                                                                                                                                                                                                                                                                                |    |    |    |    |    | 0  |
|                     | Function    | BANK for LOCAL-Z<br>0: Disable<br>1: Enable                                                                                               | Specify the bank number for the LOCAL-Z area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>00000000 to 00111111 CSZA<br>01000000 to 01111111 Setting prohibited<br>10000000 to 10111111 Setting prohibited<br>11000000 to 11111111 CSZD |    |    |    |    |    |    |

LOCAL-X Register for the E-group DMA Destination

|                     |             |                                                                                                                                            |                                                                                                                                                                                          |    |    |    |    |    |    |
|---------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|
| LOCALEDX<br>(08A8H) | Bit Symbol  | 7                                                                                                                                          | 6                                                                                                                                                                                        | 5  | 4  | 3  | 2  | 1  | 0  |
|                     | Read/Write  | X7                                                                                                                                         | X6                                                                                                                                                                                       | X5 | X4 | X3 | X2 | X1 | X0 |
|                     | Reset State | 0                                                                                                                                          | 0                                                                                                                                                                                        | 0  | 0  | 0  | 0  | 0  | 0  |
|                     | Function    | Specify the bank number for the LOCAL-X area<br>(Since bank 0 is overlapping with the COMMON area, this filed must not be specified as 0.) |                                                                                                                                                                                          |    |    |    |    |    |    |
| (08A9H)             | Bit Symbol  | 15                                                                                                                                         | 14                                                                                                                                                                                       | 13 | 12 | 11 | 10 | 9  | 8  |
|                     | Read/Write  | LXE                                                                                                                                        |                                                                                                                                                                                          |    |    |    |    |    | X8 |
|                     | Reset State | 0                                                                                                                                          |                                                                                                                                                                                          |    |    |    |    |    | 0  |
|                     | Function    | Bank for<br>LOCAL-X<br>0: Disable<br>1: Enable                                                                                             | Specify the bank number for the LOCAL-X area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>00000000 to 01111111 CSXA<br>10000000 to 11111111 CSXB |    |    |    |    |    |    |

LOCAL-Y Register for the E-group DMA Destination

|                     |            |                                                |    |                                                                                                                                            |    |    |    |    |    |
|---------------------|------------|------------------------------------------------|----|--------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|
| LOCALEDY<br>(08AAH) | Bit Symbol | 7                                              | 6  | 5                                                                                                                                          | 4  | 3  | 2  | 1  | 0  |
|                     | Read/Write |                                                |    | Y5                                                                                                                                         | Y4 | Y3 | Y2 | Y1 | Y0 |
|                     | Reset      |                                                |    | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0  |
|                     | Function   |                                                |    | Specify the bank number for the LOCAL-Y area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |    |    |    |    |    |
| (08ABH)             | Bit Symbol | 15                                             | 14 | 13                                                                                                                                         | 12 | 11 | 10 | 9  | 8  |
|                     | Read/Write | LYE                                            |    |                                                                                                                                            |    |    |    |    |    |
|                     | Reset      | 0                                              |    |                                                                                                                                            |    |    |    |    |    |
|                     | Function   | Bank for<br>LOCAL-Y<br>0: Disable<br>1: Enable |    |                                                                                                                                            |    |    |    |    |    |

LOCAL-Z Register for the E-group DMA Destination

|                     |             |                                                                                                                                            |                                                                                                                                                                                                                                                                                    |    |    |    |    |    |    |
|---------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|
| LOCALEDZ<br>(08ACH) | Bit Symbol  | 7                                                                                                                                          | 6                                                                                                                                                                                                                                                                                  | 5  | 4  | 3  | 2  | 1  | 0  |
|                     | Read/Write  | Z7                                                                                                                                         | Z6                                                                                                                                                                                                                                                                                 | Z5 | Z4 | Z3 | Z2 | Z1 | Z0 |
|                     | Reset State | 0                                                                                                                                          | 0                                                                                                                                                                                                                                                                                  | 0  | 0  | 0  | 0  | 0  | 0  |
|                     | Function    | Specify the bank number for the LOCAL-Z area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |                                                                                                                                                                                                                                                                                    |    |    |    |    |    |    |
| (08ADH)             | Bit Symbol  | 15                                                                                                                                         | 14                                                                                                                                                                                                                                                                                 | 13 | 12 | 11 | 10 | 9  | 8  |
|                     | Read/Write  | LZE                                                                                                                                        |                                                                                                                                                                                                                                                                                    |    |    |    |    |    | Z8 |
|                     | Reset State | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                    |    |    |    |    |    | 0  |
|                     | Function    | Bank for<br>LOCAL-Z<br>0: Disable<br>1: Enable                                                                                             | Specify the bank number for the LOCAL-Z area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>00000000 to 00111111 CSZA      10000000 to 10111111 Setting prohibited<br>01000000 to 01111111 Setting prohibited      11000000 to 11111111 CSZD |    |    |    |    |    |    |

LOCAL-X Register for the O-group DMA Source

|                     |             |                                                                                                                                            |                                                                                                                                                                                          |    |    |    |    |    |     |
|---------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|-----|
| LOCALOSX<br>(08B0H) |             | 7                                                                                                                                          | 6                                                                                                                                                                                        | 5  | 4  | 3  | 2  | 1  | 0   |
|                     | Bit Symbol  | X7                                                                                                                                         | X6                                                                                                                                                                                       | X5 | X4 | X3 | X2 | X1 | X0  |
|                     | Read/Write  | R/W                                                                                                                                        |                                                                                                                                                                                          |    |    |    |    |    |     |
|                     | Reset State | 0                                                                                                                                          | 0                                                                                                                                                                                        | 0  | 0  | 0  | 0  | 0  | 0   |
| (08B1H)             | Function    | Specify the bank number for the LOCAL-X area<br>(Since bank 0 is overlapping with the COMMON area, this filed must not be specified as 0.) |                                                                                                                                                                                          |    |    |    |    |    |     |
|                     |             | 15                                                                                                                                         | 14                                                                                                                                                                                       | 13 | 12 | 11 | 10 | 9  | 8   |
|                     | Bit Symbol  | LXE                                                                                                                                        |                                                                                                                                                                                          |    |    |    |    |    | X8  |
|                     | Read/Write  | R/W                                                                                                                                        |                                                                                                                                                                                          |    |    |    |    |    | R/W |
|                     | Reset State | 0                                                                                                                                          |                                                                                                                                                                                          |    |    |    |    |    | 0   |
|                     | Function    | Bank for<br>LOCAL-X<br>0: Disable<br>1: Enable                                                                                             | Specify the bank number for the LOCAL-X area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>00000000 to 01111111 CSXA<br>10000000 to 11111111 CSXB |    |    |    |    |    |     |

LOCAL-Y Register for the O-group DMA Source

|                     |             |                                                |    |                                                                                                                                            |    |    |    |    |    |
|---------------------|-------------|------------------------------------------------|----|--------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|
| LOCALOSY<br>(08B2H) |             | 7                                              | 6  | 5                                                                                                                                          | 4  | 3  | 2  | 1  | 0  |
|                     | Bit Symbol  |                                                |    | Y5                                                                                                                                         | Y4 | Y3 | Y2 | Y1 | Y0 |
|                     | Read/Write  |                                                |    | R/W                                                                                                                                        |    |    |    |    |    |
|                     | Reset State |                                                |    | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0  |
| (08B3H)             | Function    |                                                |    | Specify the bank number for the LOCAL-Y area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |    |    |    |    |    |
|                     |             | 15                                             | 14 | 13                                                                                                                                         | 12 | 11 | 10 | 9  | 8  |
|                     | Bit Symbol  | LYE                                            |    |                                                                                                                                            |    |    |    |    |    |
|                     | Read/Write  | R/W                                            |    |                                                                                                                                            |    |    |    |    |    |
|                     | Reset State | 0                                              |    |                                                                                                                                            |    |    |    |    |    |
|                     | Function    | Bank for<br>LOCAL-Y<br>0: Disable<br>1: Enable |    |                                                                                                                                            |    |    |    |    |    |

LOCAL-Z Register for the O-group DMA Source

|                     |             |                                                                                                                                            |                                                                                                                                                                                                                                                                                    |    |    |    |    |    |     |
|---------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|-----|
| LOCALOSZ<br>(08B4H) |             | 7                                                                                                                                          | 6                                                                                                                                                                                                                                                                                  | 5  | 4  | 3  | 2  | 1  | 0   |
|                     | Bit Symbol  | Z7                                                                                                                                         | Z6                                                                                                                                                                                                                                                                                 | Z5 | Z4 | Z3 | Z2 | Z1 | Z0  |
|                     | Read/Write  | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                    |    |    |    |    |    |     |
|                     | Reset State | 0                                                                                                                                          | 0                                                                                                                                                                                                                                                                                  | 0  | 0  | 0  | 0  | 0  | 0   |
| (08B5H)             | Function    | Specify the bank number for the LOCAL-Z area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |                                                                                                                                                                                                                                                                                    |    |    |    |    |    |     |
|                     |             | 15                                                                                                                                         | 14                                                                                                                                                                                                                                                                                 | 13 | 12 | 11 | 10 | 9  | 8   |
|                     | Bit Symbol  | LZE                                                                                                                                        |                                                                                                                                                                                                                                                                                    |    |    |    |    |    | Z8  |
|                     | Read/Write  | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                    |    |    |    |    |    | R/W |
|                     | Reset State | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                    |    |    |    |    |    | 0   |
|                     | Function    | Bank for<br>LOCAL-Z<br>0: Disable<br>1: Enable                                                                                             | Specify the bank number for the LOCAL-Z area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>00000000 to 00111111 CSZA      10000000 to 10111111 Setting prohibited<br>01000000 to 01111111 Setting prohibited      11000000 to 11111111 CSZD |    |    |    |    |    |     |

LOCAL-X Register for the O-group DMA Destination

|                     |             |                                                                                                                                            |                                                                                                                                                                                          |    |    |    |    |    |     |
|---------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|-----|
| LOCALODX<br>(08B8H) |             | 7                                                                                                                                          | 6                                                                                                                                                                                        | 5  | 4  | 3  | 2  | 1  | 0   |
|                     | Bit Symbol  | X7                                                                                                                                         | X6                                                                                                                                                                                       | X5 | X4 | X3 | X2 | X1 | X0  |
|                     | Read/Write  | R/W                                                                                                                                        |                                                                                                                                                                                          |    |    |    |    |    |     |
|                     | Reset State | 0                                                                                                                                          | 0                                                                                                                                                                                        | 0  | 0  | 0  | 0  | 0  | 0   |
| (08B9H)             | Function    | Specify the bank number for the LOCAL-X area<br>(Since bank 0 is overlapping with the COMMON area, this filed must not be specified as 0.) |                                                                                                                                                                                          |    |    |    |    |    |     |
|                     |             | 15                                                                                                                                         | 14                                                                                                                                                                                       | 13 | 12 | 11 | 10 | 9  | 8   |
|                     | Bit Symbol  | LXE                                                                                                                                        |                                                                                                                                                                                          |    |    |    |    |    | X8  |
|                     | Read/Write  | R/W                                                                                                                                        |                                                                                                                                                                                          |    |    |    |    |    | R/W |
|                     | Reset State | 0                                                                                                                                          |                                                                                                                                                                                          |    |    |    |    |    | 0   |
|                     | Function    | Bank for LOCAL-X<br>0: Disable<br>1: Enable                                                                                                | Specify the bank number for the LOCAL-X area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>00000000 to 01111111 CSXA<br>10000000 to 11111111 CSXB |    |    |    |    |    |     |

LOCAL-Y Register for the O-group DMA Destination

|                     |             |                                             |    |                                                                                                                                            |    |    |    |    |    |
|---------------------|-------------|---------------------------------------------|----|--------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|
| LOCALODY<br>(08BAH) |             | 7                                           | 6  | 5                                                                                                                                          | 4  | 3  | 2  | 1  | 0  |
|                     | Bit Symbol  |                                             |    | Y5                                                                                                                                         | Y4 | Y3 | Y2 | Y1 | Y0 |
|                     | Read/Write  |                                             |    | R/W                                                                                                                                        |    |    |    |    |    |
|                     | Reset State |                                             |    | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0  |
| (08BBH)             | Function    |                                             |    | Specify the bank number for the LOCAL-Y area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |    |    |    |    |    |
|                     |             | 15                                          | 14 | 13                                                                                                                                         | 12 | 11 | 10 | 9  | 8  |
|                     | Bit Symbol  | LYE                                         |    |                                                                                                                                            |    |    |    |    |    |
|                     | Read/Write  | R/W                                         |    |                                                                                                                                            |    |    |    |    |    |
|                     | Reset State | 0                                           |    |                                                                                                                                            |    |    |    |    |    |
|                     | Function    | BANK for LOCAL-Y<br>0: Disable<br>1: Enable |    |                                                                                                                                            |    |    |    |    |    |

LOCAL-Z Register for the O-group DMA Destination

|                     |             |                                                                                                                                            |                                                                                                                                                                                                                                                                                    |    |    |    |    |    |     |
|---------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|-----|
| LOCALODZ<br>(08BCH) |             | 7                                                                                                                                          | 6                                                                                                                                                                                                                                                                                  | 5  | 4  | 3  | 2  | 1  | 0   |
|                     | Bit Symbol  | Z7                                                                                                                                         | Z6                                                                                                                                                                                                                                                                                 | Z5 | Z4 | Z3 | Z2 | Z1 | Z0  |
|                     | Read/Write  | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                    |    |    |    |    |    |     |
|                     | Reset State | 0                                                                                                                                          | 0                                                                                                                                                                                                                                                                                  | 0  | 0  | 0  | 0  | 0  | 0   |
| (08BDH)             | Function    | Specify the bank number for the LOCAL-Z area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |                                                                                                                                                                                                                                                                                    |    |    |    |    |    |     |
|                     |             | 15                                                                                                                                         | 14                                                                                                                                                                                                                                                                                 | 13 | 12 | 11 | 10 | 9  | 8   |
|                     | Bit Symbol  | LZE                                                                                                                                        |                                                                                                                                                                                                                                                                                    |    |    |    |    |    | Z8  |
|                     | Read/Write  | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                    |    |    |    |    |    | R/W |
|                     | Reset State | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                    |    |    |    |    |    | 0   |
|                     | Function    | Bank for LOCAL-Z<br>0: Disable<br>1: Enable                                                                                                | Specify the bank number for the LOCAL-Z area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>00000000 to 00111111 CSZA      10000000 to 10111111 Setting prohibited<br>01000000 to 01111111 Setting prohibited      11000000 to 11111111 CSZD |    |    |    |    |    |     |

## 3.9.3 Programming example

The conditions listed in this table apply the following programming examples.

| No. | Used as       | Memory                      | Setting                                                     | MMU area          | Logical address     | Physical address    |
|-----|---------------|-----------------------------|-------------------------------------------------------------|-------------------|---------------------|---------------------|
| (a) | Main Routine  | NOR-Flash<br>(16 MB, 1 pcs) | $\overline{\text{CS}}\text{A}$ ,<br>32 bit,<br>1 wait state | COMMON-Z          | C00000H to FFFFFFFH |                     |
| (b) | Character-ROM |                             |                                                             | Bank 0 in LOCAL-Z | 800000H to BFFFFFFH | 000000H to 3FFFFFFH |
| (c) | Subroutine    | SRAM<br>(16 MB, 1 pcs)      | $\overline{\text{CS}}\text{I}$ ,<br>16 bit,<br>0 wait state | Bank 0 in LOCAL-Y | 400000H to 5FFFFFFH | 000000H to 1FFFFFFH |
| (d) | Stack-RAM     | On-chip-RAM<br>(144KB)      | –<br>(32 bit, 2-1-1-1clk)                                   | Bank 2 in LOCAL-Y | 002000H to 049FFFFH |                     |

(a) Main Routine (COMMON-Z)

| Logical Address | Physical Address | Instruction No. | Instruction         | Comment                                                               |
|-----------------|------------------|-----------------|---------------------|-----------------------------------------------------------------------|
|                 |                  | 1               | org C00000H         | ;                                                                     |
| C00000H         | <-(Same)         | 2               | ldw (mamr2),80FFH   | ; CS2 800000-FFFFFF/8MB                                               |
| C000xxH         | <-               | 3               | ldw (b2cs), C222H   | ; CS2 32-bit ROM, 1 wait state                                        |
|                 |                  | 4               | ldw (mamr1),40FFH   | ; CS1 400000-7FFFFFF/4MB                                              |
|                 |                  | 5               | ldw (b1cs), 8111H   | ; CS1 16-bit RAM, 0 wait state                                        |
|                 |                  | 5.1             | ldw (localpz),8000H | ; Enable LOCAL-Z bank for program                                     |
|                 |                  | 5.2             | ldw (localrz),8000H | ; Enable LOCAL-Z bank for read-data                                   |
|                 |                  | 6               | ld (p8fc), 02H      | ; P81: CS1                                                            |
|                 |                  | 7               | ld (p8fc2), 04H     | ; P82:                                                                |
|                 |                  | 9               | ld xsp,48000H       | ; Stack Pointer = 48000H                                              |
|                 |                  | 10              | ldw (localpy),8000H | ; Bank 0 in LOCAL-Y is configured as the program bank for subroutines |
|                 |                  | 11              | :                   | ;                                                                     |
| C000yyH         | <-               | 12              | call 400000H        | ; Call a subroutine                                                   |
|                 |                  | 13              | :                   | ;                                                                     |
|                 |                  | 14              | :                   | ;                                                                     |
|                 |                  | 15              | :                   | ;                                                                     |

- The instructions No.2 through No.8 configure external pins and the Memory Controller.
- The instruction No.9 specifies the stack pointer value. The stack pointer is herein specified to point to the memory location in on-chip RAM.
- The instruction No.10 configures the setting used for a subroutine call instruction of No.12.
- The instruction No.12 calls a subroutine. When the CPU generates the address 400000H, the MMU translates it to the physical address 000000H, which is then placed onto the external address bus: A23 to A0. Since the logical address is within the address range of the CS1 space,  $\overline{\text{CS}}\text{I}$  for SRAM is asserted at the same time. By using these instructions, the program execution of the CPU can be branched to the subroutine.

Note: This example assumes that the subroutine program is already written into SRAM.

(b) Subroutine (Bank 0 in LOCAL-Y)

| Logical address | Physical address | Instruction No. | Instruction                  | Comment                                                                 |
|-----------------|------------------|-----------------|------------------------------|-------------------------------------------------------------------------|
|                 |                  | 16              | org 400000H                  | ;                                                                       |
| 400000H         | 000000H          | 17              | ldw (localrz), 8001H         | ; Bank 0 in LOCAL-Z is configured as read-data memory for Character-RAM |
| 4000xxH         | 0000xxH          | 18              | ld xiy,800000H               | ; Index address register for reading Character-ROM                      |
|                 |                  | 19              | ld wa,(xiy)                  | ; Read Character-ROM                                                    |
|                 |                  | 20              | :                            | ;                                                                       |
|                 |                  | 21              | <del>ld (localpy), 82H</del> | ;                                                                       |
|                 |                  | 22              | :                            |                                                                         |
| 5000yyH         | 1000yyH          | 23              | ret                          | ;                                                                       |

- The instruction No.17 configures Bank 0 of the LOCAL-Z area to read data from character-ROM.
- The instructions No.18 and No.19 are used to read data from character-ROM. When the CPU generates the address 800000H, the MMU translates it to the physical address 000000H, which is then placed onto the external address bus: A23 to A0. Since the logical address is within the address range of the CS2 space,  $\overline{CSZA}$  for NOR-Flash is asserted at the same time. By using these instructions, the CPU can read data from character ROM.
- The instruction No.21 switches the program bank in the LOCAL area. Since the program bank switching within the same LOCAL area is prohibited, this is a bad example.

### 3.10 SDRAM Controller (SDRAMC)

The TMP92CF30 incorporates an SDRAM controller (SDRAMC) for accessing SDRAM that can be used as data memory, program memory, or display memory.

The SDRAMC has the following features:

(1) Supported SDRAM

Data rate type : SDR (single data rate) type only

Memory capacity : 16 / 64 / 128 / 256 / 512 Mbits

Number of banks : 2 banks / 4 banks

Data bus width : 16 bits

(This device support 32-bit data bus mode, but the accessing to SDRAM is 16-bit mode only.)

Read burst length : 1 word / full page

Write mode : Single mode / Burst mode

(2) Supported initialization sequence commands

Precharge All command

Eight Auto Refresh commands

Mode Register Set command

(3) Access mode

|                     | CPU Cycle  | HDMA Cycle                     |
|---------------------|------------|--------------------------------|
| Burst length        | 1 word     | 1 word or full page selectable |
| Addressing mode     | Sequential | Sequential                     |
| CAS latency (clock) | 2          | 2                              |
| Write mode          | Single     | Single or burst selectable     |

(4) Access cycles

- CPU access cycles

Read cycle : 1 word, 4-3-3-3 states (minimum)

Write cycle : Single, 3-2-2-2 states (minimum)

Data size : 1 byte / 1 word / 1 long-word

- HDMA access cycles

Read cycle : 1 word, 4-3-3-3 states / full page, 4-1-1-1 states (minimum)

Write cycle : Single, 3-2-2-2 states (minimum) / burst, 2-1-1-1 states (minimum)

Data size : 1 byte / 1 word / 1 long-word

(5) Auto generation of refresh cycles

- Auto Refresh is performed while the SDRAM is not being accessed.
- The Auto Refresh interval is programmable.
- The Self Refresh function is also supported.

Note: The SDRAM address area is determined by the CS1 or CS2 setting of the memory controller. However, the number of bus cycle states is controlled by the SDRAMC.

## 3.10.1 Control Registers

The SDRAMC has the following control registers.

SDRAM Access Control Register

|                  | 7           | 6                                                   | 5                | 4                                                                                                       | 3      | 2                                                                          | 1 | 0                                           |
|------------------|-------------|-----------------------------------------------------|------------------|---------------------------------------------------------------------------------------------------------|--------|----------------------------------------------------------------------------|---|---------------------------------------------|
| SDACR<br>(0250H) | Bit symbol  | SRDS                                                | –                | SMUXW1                                                                                                  | SMUXW0 | SPRE                                                                       |   | SMAC                                        |
|                  | Read/Write  | R/W                                                 |                  |                                                                                                         |        |                                                                            |   | R/W                                         |
|                  | Reset State | 1                                                   | 0                | 0                                                                                                       | 0      | 0                                                                          |   | 0                                           |
|                  | Function    | Read data shift function<br>0: Disable<br>1: Enable | Always write "0" | Address multiplex type<br>00: Type A (A9- )<br>01: Type B (A10- )<br>10: Type C (A11- )<br>11: Reserved |        | Read/Write commands<br>0: Without auto precharge<br>1: With auto precharge |   | SDRAM controller<br>0: Disable<br>1: Enable |

SDRAM Command Interval Setting Register

|                   | 7           | 6 | 5                            | 4                           | 3                           | 2                            | 1                                                                                                                           | 0     |
|-------------------|-------------|---|------------------------------|-----------------------------|-----------------------------|------------------------------|-----------------------------------------------------------------------------------------------------------------------------|-------|
| SDCISR<br>(0251H) | Bit symbol  |   | STM RD                       | STWR                        | STRP                        | STRCD                        | STRC2                                                                                                                       | STRC1 |
|                   | Read/Write  |   | R/W                          |                             |                             |                              |                                                                                                                             |       |
|                   | Reset State |   | 1                            | 1                           | 1                           | 1                            | 1                                                                                                                           | 0     |
|                   | Function    |   | TMRD<br>0: 1 CLK<br>1: 2 CLK | TWR<br>0: 1 CLK<br>1: 2 CLK | TRP<br>0: 1 CLK<br>1: 2 CLK | TRCD<br>0: 1 CLK<br>1: 2 CLK | TRC<br>000: 1 CLK      100: 5 CLK<br>001: 2 CLK      101: 6 CLK<br>010: 3 CLK      110: 7 CLK<br>011: 4 CLK      111: 8 CLK |       |

SDRAM Refresh Control Register

|                  | 7           | 6                | 5 | 4                                                          | 3                                                                                                                                                                     | 2    | 1    | 0                                       |
|------------------|-------------|------------------|---|------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|-----------------------------------------|
| SDRCR<br>(0252H) | Bit symbol  | –                |   | SSAE                                                       | SRS2                                                                                                                                                                  | SRS1 | SRS0 | SRC                                     |
|                  | Read/Write  | R/W              |   | R/W                                                        |                                                                                                                                                                       |      |      |                                         |
|                  | Reset State | 0                |   | 1                                                          | 0                                                                                                                                                                     | 0    | 0    | 0                                       |
|                  | Function    | Always write "0" |   | Self Refresh auto exit function<br>0: Disable<br>1: Enable | Refresh interval<br>000: 47 states    100: 468 states<br>001: 78 states    101: 624 states<br>010: 156 states   110: 936 states<br>011: 312 states   111: 1248 states |      |      | Auto Refresh<br>0: Disable<br>1: Enable |



| SDRAM Command Register |   |   |   |   |   |                                                                                                                                                                                                                                                                                                                          |       |       |
|------------------------|---|---|---|---|---|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|
|                        | 7 | 6 | 5 | 4 | 3 | 2                                                                                                                                                                                                                                                                                                                        | 1     | 0     |
| SDCMM<br>(0253H)       |   |   |   |   |   | SCMM2                                                                                                                                                                                                                                                                                                                    | SCMM1 | SCMM0 |
| Bit symbol             |   |   |   |   |   | R/W                                                                                                                                                                                                                                                                                                                      |       |       |
| Read/Write             |   |   |   |   |   |                                                                                                                                                                                                                                                                                                                          |       |       |
| Reset State            |   |   |   |   |   | 0                                                                                                                                                                                                                                                                                                                        | 0     | 0     |
| Function               |   |   |   |   |   | Command issue (Note 1) (Note 2)<br>000: Don't care<br>001: Initialization sequence<br>a. Precharge All command<br>b. Eight Auto Refresh commands<br>c. Mode Register Set command<br>010: Precharge All command<br>100: Reserved<br>101: Self Refresh Entry command<br>110: Self Refresh Exit command<br>Others: Reserved |       |       |

Note 1: <SCMM2:0> is automatically cleared to "000" after the specified command is issued. Before writing the next command, make sure that <SCMM2:0> is "000". In the case of the Self Refresh Entry command, however, <SCMM2:0> is not cleared to "000" by execution of this command. Thus, this register can be used as a flag for checking whether or not Self Refresh is being performed.

Note 2: The Self Refresh Exit command can only be specified while Self Refresh is being performed.

| SDRAM HDMA Burst Length Select Register |   |   |                                                                                       |           |           |           |           |           |
|-----------------------------------------|---|---|---------------------------------------------------------------------------------------|-----------|-----------|-----------|-----------|-----------|
|                                         | 7 | 6 | 5                                                                                     | 4         | 3         | 2         | 1         | 0         |
| SDBLS<br>(0254H)                        |   |   | SDBL5                                                                                 | SDBL4     | SDBLS     | SDBL2     | SDBL1     | SDBL0     |
| Bit symbol                              |   |   | R/W                                                                                   |           |           |           |           |           |
| Read/Write                              |   |   |                                                                                       |           |           |           |           |           |
| Reset State                             |   |   | 0                                                                                     | 0         | 0         | 0         | 0         | 0         |
| Function                                |   |   | For HDMA5                                                                             | For HDMA4 | For HDMA3 | For HDMA2 | For HDMA1 | For HDMA0 |
|                                         |   |   | HDMA burst length<br>0: 1 Word read / Single write<br>1: Full page read / Burst write |           |           |           |           |           |

Figure 3.10.1 Control Registers

### 3.10.2 Operation Description

#### (1) Memory access control

The SDRAMC is enabled by setting SDACR<SMAC> to “1”.

When one of the bus masters (CPU, DMAC) generates a cycle to access the SDRAM address area, the SDRAMC outputs SDRAM control signals.

Figure 3.10.2 to Figure3.10.5 shows the timing for accessing the SDRAM. The number of SDRAM access cycles is controlled by the SDRAMC and does not depend on the number of waits controlled by the memory controller.

#### (a) Command issue function

The SDRAMC issues commands as specified by the SDCMM register. The SDRAMC also issues commands automatically for each SDRAM access cycle generated by each bus master.

Table 3.10.1 shows the commands that are issued by the SDRAMC.

Table 3.10.1 Commands Issued by the SDRAMC

| Command                   | CKEn-1 | CKEn | SDxxDQM | A10 | A15-11<br>A9-0 | $\overline{\text{SDCS}}$ | $\overline{\text{SDRAS}}$ | $\overline{\text{SDCAS}}$ | $\overline{\text{SDWE}}$ |
|---------------------------|--------|------|---------|-----|----------------|--------------------------|---------------------------|---------------------------|--------------------------|
| Bank Activate             | H      | H    | H       | RA  | RA             | L                        | L                         | H                         | H                        |
| Precharge All             | H      | H    | H       | H   | X              | L                        | L                         | H                         | L                        |
| Read                      | H      | H    | L       | L   | CA             | L                        | H                         | L                         | H                        |
| Read with Auto Precharge  | H      | H    | L       | H   | CA             | L                        | H                         | L                         | H                        |
| Write                     | H      | H    | L       | L   | CA             | L                        | H                         | L                         | L                        |
| Write with Auto Precharge | H      | H    | L       | H   | CA             | L                        | H                         | L                         | L                        |
| Mode Register Set         | H      | H    | H       | L   | M              | L                        | L                         | L                         | L                        |
| Burst Stop                | H      | H    | H       | X   | X              | L                        | H                         | H                         | L                        |
| Auto Refresh              | H      | H    | H       | X   | X              | L                        | L                         | L                         | H                        |
| Self Refresh Entry        | H      | L    | H       | X   | X              | L                        | L                         | L                         | H                        |
| Self Refresh Exit         | L      | H    | H       | X   | X              | H                        | H                         | H                         | H                        |

Note 1: H = High level, L = Low level, RA = Row address, CA = Column address, M = Mode data, X = Don't care

Note 2: CKEn = CKE level in the command input cycle

CKEn-1 = CKE level in a cycle immediately before the command input cycle

## (b) Address multiplex function

In access cycles, the A0 to A15 pins output low/column multiplexed addresses. The multiplex width is set by SDACR<SMUXW1:0>. Table 3.10.2 shows the relationship between the multiplex width and low/column addresses.

Table 3.10.2 Address Multiplex

| 92CF30<br>Pin Name | SDRAM Access Cycle Address |                        |                        |                |
|--------------------|----------------------------|------------------------|------------------------|----------------|
|                    | Row Address                |                        |                        | Column Address |
|                    | Type A<br><SMUXW> = 00     | Type B<br><SMUXW> = 01 | Type C<br><SMUXW> = 10 |                |
| A0                 | A9                         | A10                    | A11                    | A1             |
| A1                 | A10                        | A11                    | A12                    | A2             |
| A2                 | A11                        | A12                    | A13                    | A3             |
| A3                 | A12                        | A13                    | A14                    | A4             |
| A4                 | A13                        | A14                    | A15                    | A5             |
| A5                 | A14                        | A15                    | A16                    | A6             |
| A6                 | A15                        | A16                    | A17                    | A7             |
| A7                 | A16                        | A17                    | A18                    | A8             |
| A8                 | A17                        | A18                    | A19                    | A9             |
| A9                 | A18                        | A19                    | A20                    | A10            |
| A10                | A19                        | A20                    | A21                    | AP *           |
| A11                | A20                        | A21                    | A22                    | Row Address    |
| A12                | A21                        | A22                    | A23                    |                |
| A13                | A22                        | A23                    | EA24                   |                |
| A14                | A23                        | EA24                   | EA25                   |                |
| A15                | EA24                       | EA25                   | EA26                   |                |

\*AP: Auto Precharge

## (c) Burst length

When the CPU accesses the SDRAM, the burst length is fixed to 1-word read/single write. The burst length can be selected for SDRAM read and write accesses by HDMA if the following conditions are satisfied:

- The HDMA transfer mode is an increment mode.
- Transfers are made between the SDRAM and internal RAM or internal I/O.

In other cases, HDMA operation can only be performed in 1-word read/single write mode. Use SDBLS<SDBL5:0> to set the burst length for each HDMA channel.

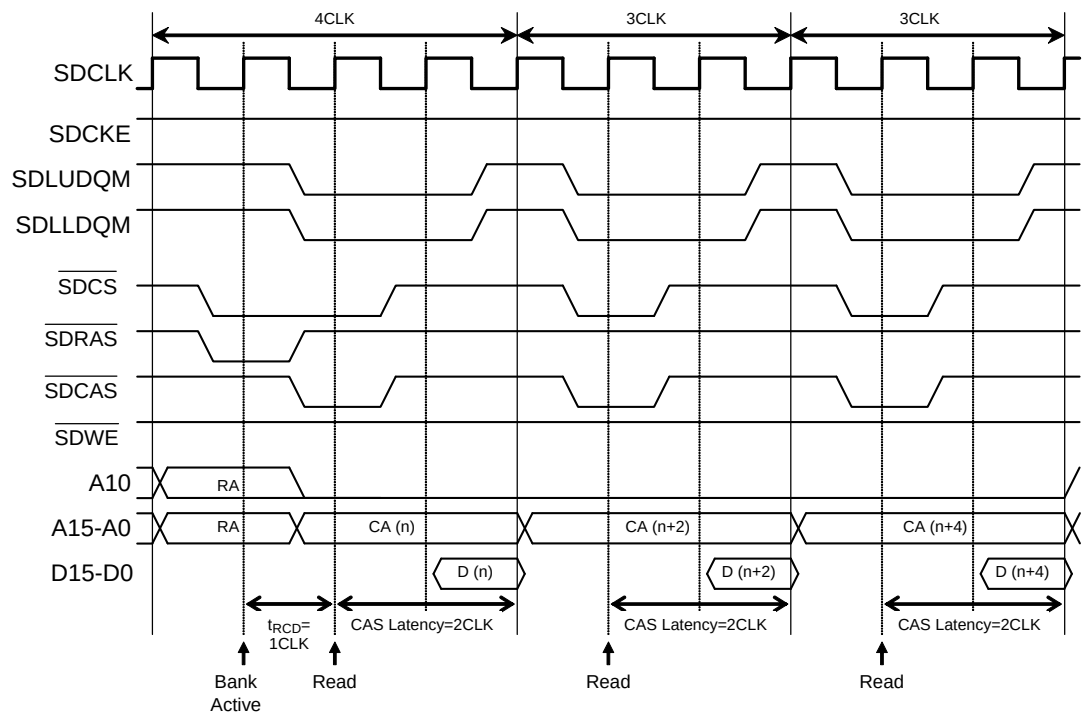


Figure 3.10.2 1-Word Read Cycle Timing

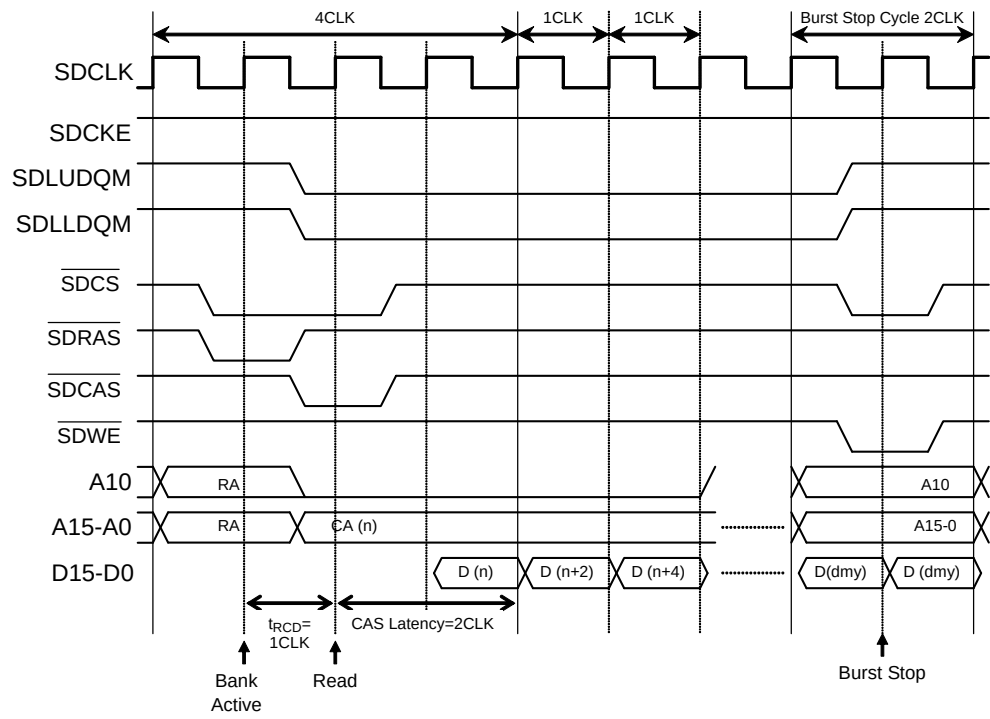


Figure 3.10.3 Full-Page Read Cycle Timing

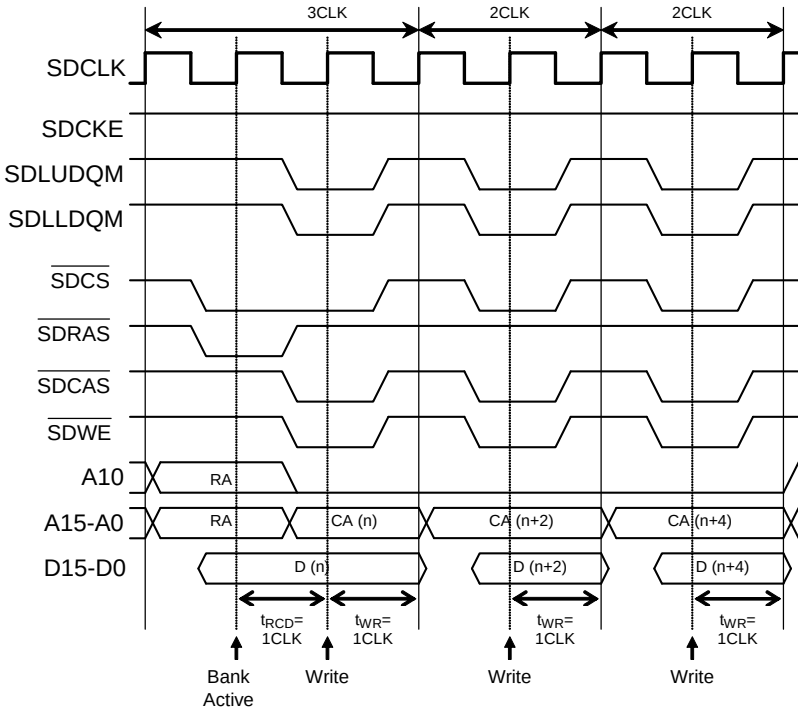


Figure 3.10.4 Single Write Cycle Timing

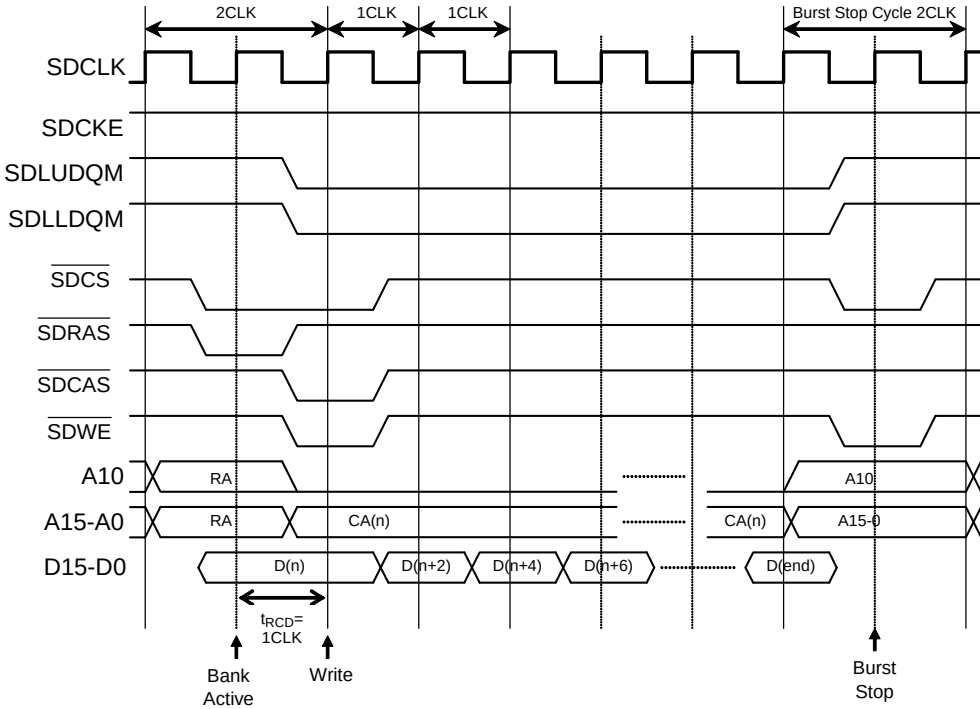


Figure 3.10.5 Burst Write Cycle Timing

## (2) Execution of instructions on SDRAM

The CPU can execute instructions that are stored in the SDRAM. However, the following operations cannot be performed.

- a) Executing the HALT instruction
- b) Changing the clock gear setting
- c) Changing the settings in the SDACR, SDCMM, and SDCISR registers

These operations, if needed, must be executed by branching to other memory such as internal RAM.

## (3) Command interval adjustment function

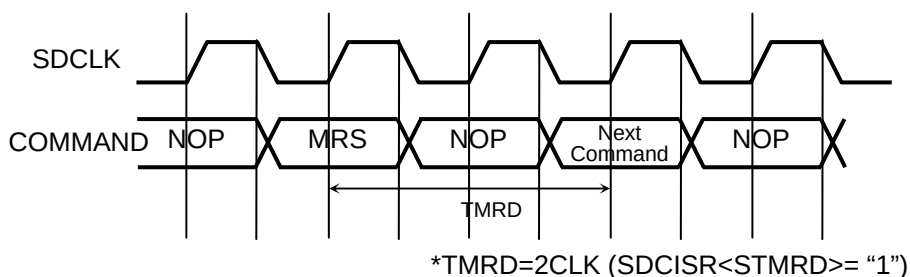
Command execution intervals can be adjusted for each command. This function enables the SDRAM to be accessed at optimum cycles even if the operation frequency is changed by clock gear.

Command intervals should be set in the SDCISR register according to the operating frequency of the TMP92CF30 and the AC specifications of the SDRAM.

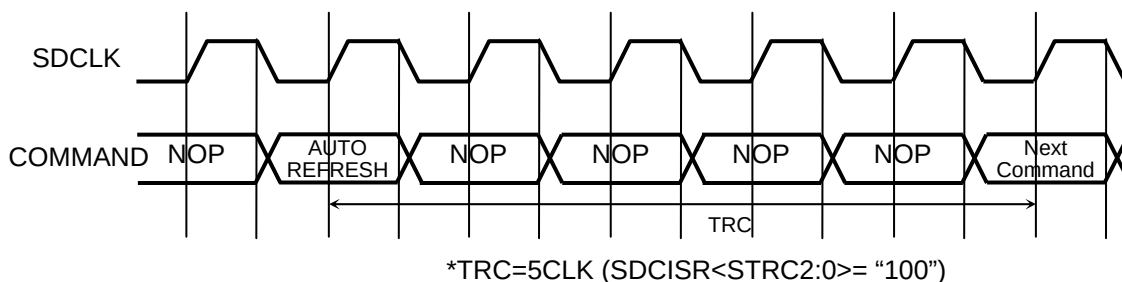
The SDCICR register must not be changed while the SDRAM is being accessed.

The timing waveforms for various cases are shown below.

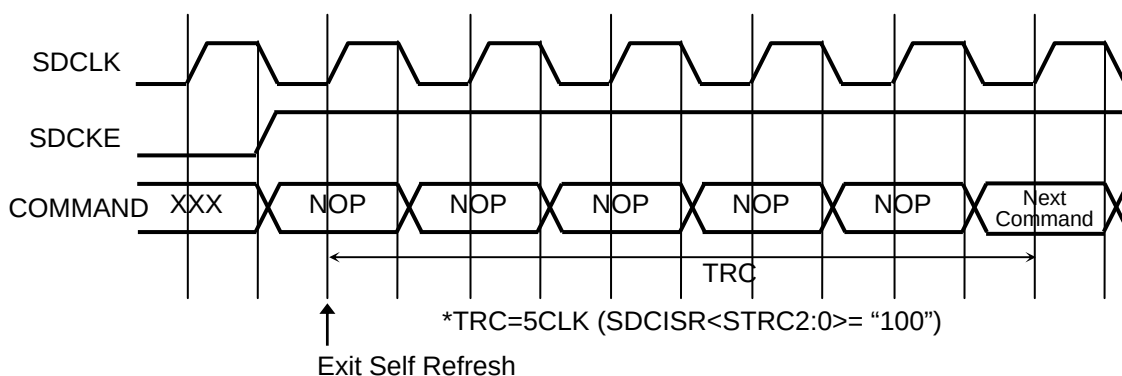
## (a) Mode Register Set command



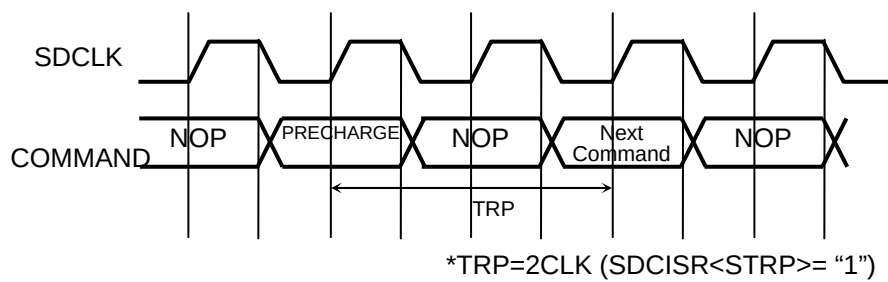
## (b) Auto Refresh command



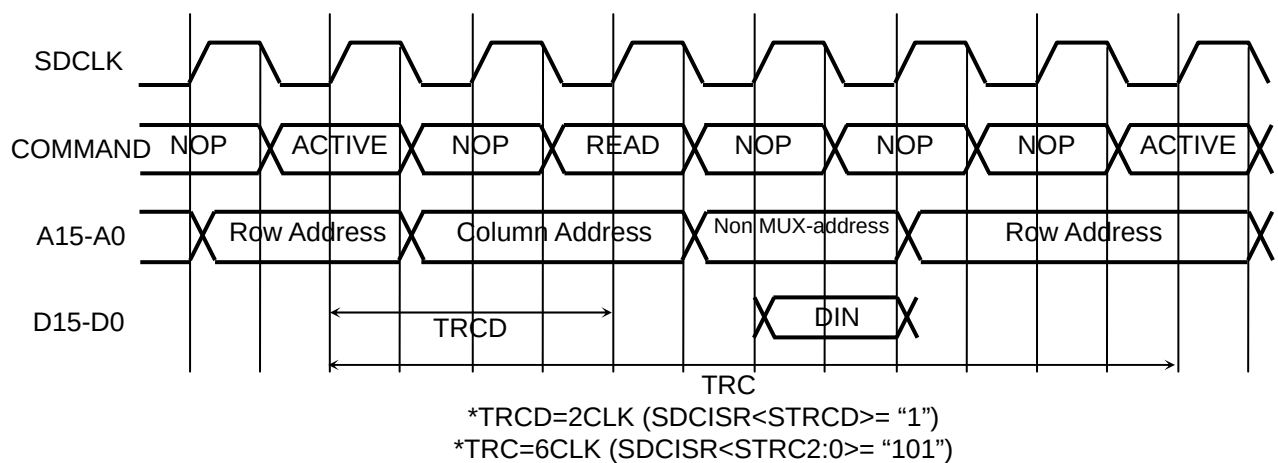
## (c) Self Refresh Exit



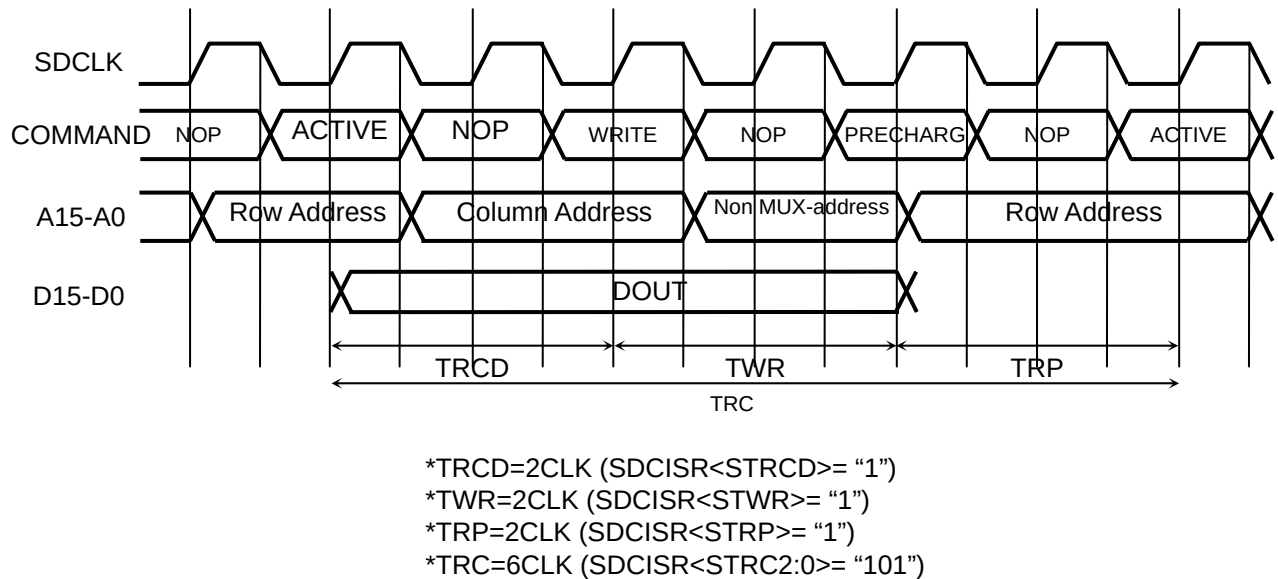
(d) Precharge command



(e) Read cycle



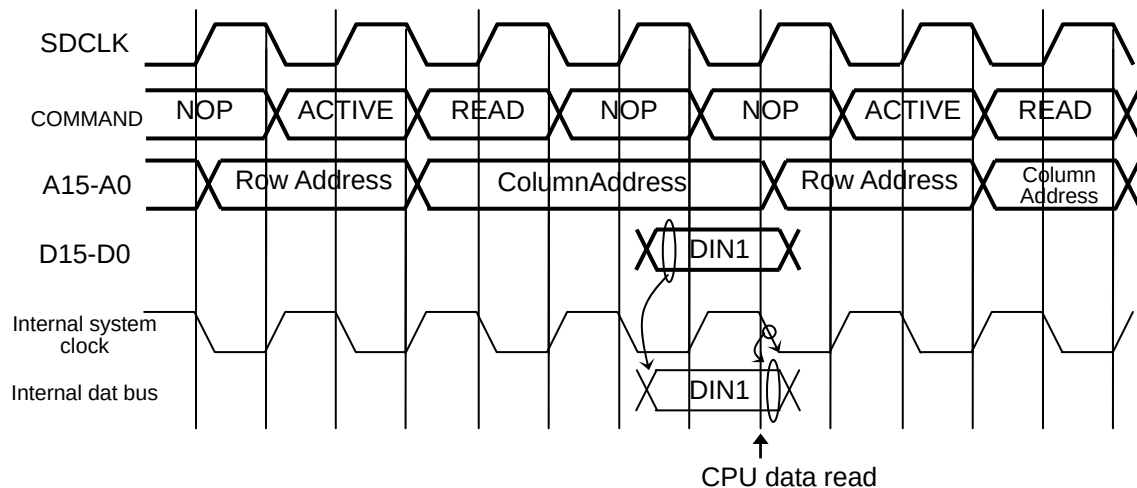
(f) Write cycle



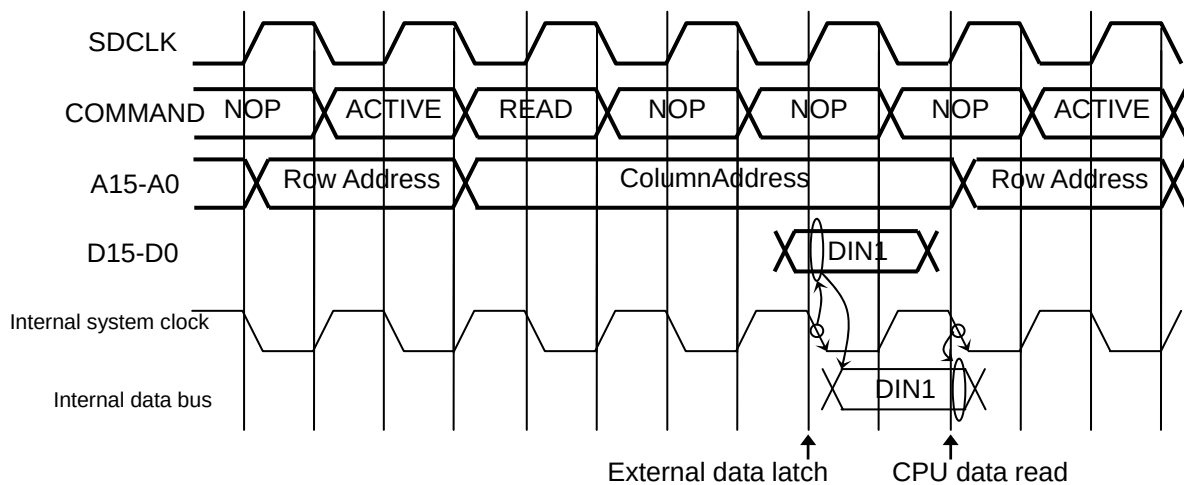
## (4) Read data shift function

If the AC specifications of the SDRAM cannot be satisfied when data is read from the SDRAM, the read data can be latched in a port circuit so that the CPU can read the data in the next state. When this read data shift function is used, the read cycle requires additional one state. The write cycle is not affected. The timing waveforms for various cases are shown below.

(a) 1-word read, the read data shift function disabled (SDACR&lt;SRCS&gt; = "0")

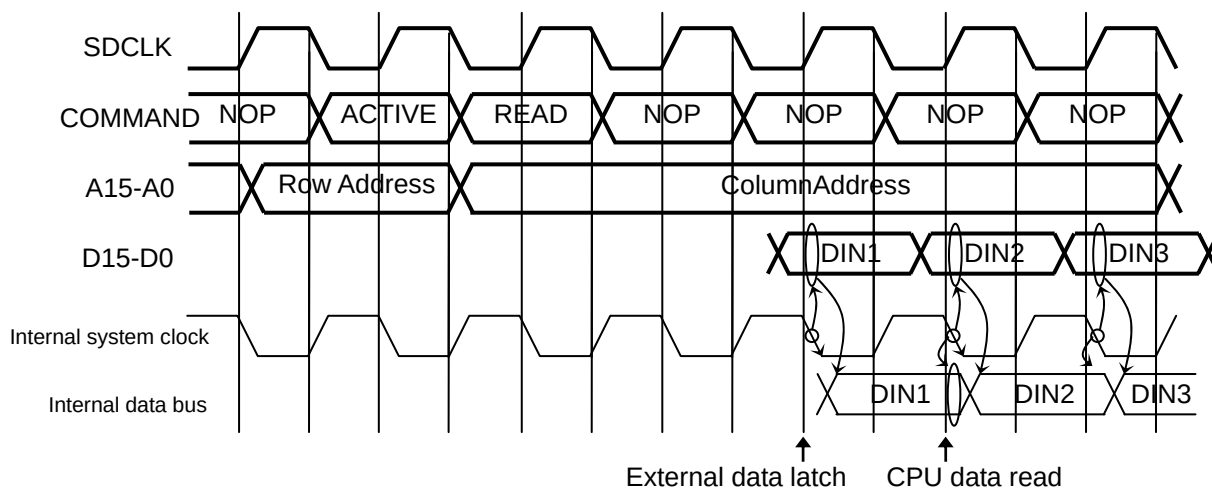


(b) 1-word read, the read data shift function enabled (SDACR&lt;SRDS&gt; = "1", &lt;SRDSCK&gt; = "0")





- (c) Full-page read, the read data shift function enabled (SDACR<SRDS> = "1", <SRDSCK> = "0")



#### (5) Read/Write commands

The Read/Write commands to be used in 1-word read/single write mode can be specified by using SDACR<SPRE>.

When SDACR<SPRE> is set to "1", the Read/Write commands are executed with Auto Precharge. When Auto Precharge is enabled, the SDRAM is automatically precharged internally at every access cycle. Thus, the SDRAM is always in a "bank idle" state while it is not being accessed. This helps reduce the power consumption of the SDRAM but at the cost of degradation in performance as the Bank Active command is needed at every access cycle.

When SDACR<SPRE> is set to "0", the Read/Write commands are executed without Auto Precharge. In this case, the SDRAM is not precharged at every access cycle and is always in a "bank active" state. This increases the power consumption of the SDRAM, but improves performance as there is no need to issue the Bank Active command at every access cycle. If an access is made to outside the SDRAM page boundaries or if the Auto Refresh command is issued, the SDRAMC automatically issues the Precharge All command.

## (6) Refresh control

The TMP92CF30 supports two kinds of refresh commands: Auto Refresh and Self Refresh.

## (a) Auto Refresh

When  $\text{SDRCR}\langle\text{SRC}\rangle$  is set to "1", the Auto Refresh command is automatically issued at intervals specified by  $\text{SDRCR}\langle\text{SRS2:0}\rangle$ . The Auto Refresh interval can be specified in a range of 47 states to 1248 states ( $0.78\ \mu\text{s}$  to  $20.8\ \mu\text{s}$  at  $f_{\text{SYS}} = 60\ \text{MHz}$ ).

The CPU operation (instruction fetch and execution) is halted while the Auto Refresh command is being executed. Figure 3.10.6 shows the Auto Refresh cycle timing, and Table 3.10.3 shows the Auto Refresh interval settings. The Auto Refresh function cannot be used in IDLE1 and STOP modes. In these modes, use the Self Refresh function to be explained next.

Note: A system reset disables the Auto Refresh function.

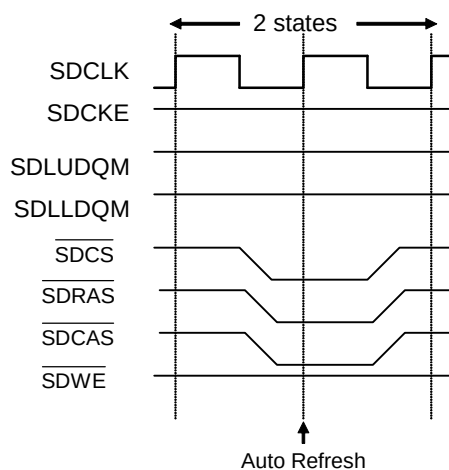


Figure 3.10.6 Auto Refresh Cycle Timing

Note1: Set the interval of Auto Refresh as below table for your reference.

Note2: Take care SDRAM specification and CPU operation speed, please.

Table 3.10.3 System clock speed & auto refresh interval

| SDRCR<SRS2:0> |      |      |                | Frequency: system clock [ MHz ]               |       |       |       |       |       |       |       |       |       |       |       |
|---------------|------|------|----------------|-----------------------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| SRS2          | SRS1 | SRS0 | interval state | 1                                             | 2     | 3     | 4     | 6     | 8     | 10    | 20    | 30    | 40    | 60    | 80    |
|               |      |      |                | Time: auto refresh interval [ $\mu\text{s}$ ] |       |       |       |       |       |       |       |       |       |       |       |
| 0             | 0    | 0    | 47             | 47.0                                          | 23.5  | 15.67 | 11.75 | 7.83  | 5.88  | 4.70  | 2.35  | 1.57  | 1.18  | 0.78  | 0.59  |
| 0             | 0    | 1    | 78             | 78.0                                          | 39.0  | 26.0  | 19.5  | 13.0  | 9.75  | 7.80  | 3.9   | 2.60  | 1.95  | 1.30  | 0.98  |
| 0             | 1    | 0    | 156            | 156.0                                         | 78.0  | 52.0  | 39.0  | 26.0  | 19.5  | 15.60 | 7.8   | 5.20  | 3.90  | 2.60  | 1.95  |
| 0             | 1    | 1    | 312            | 312.0                                         | 156.0 | 104.0 | 78.0  | 52.0  | 39.0  | 31.2  | 15.60 | 10.4  | 7.80  | 5.20  | 3.90  |
| 1             | 0    | 0    | 468            | 468.0                                         | 234.0 | 156.0 | 117.0 | 78.0  | 58.5  | 46.8  | 23.4  | 15.60 | 11.7  | 7.80  | 5.85  |
| 1             | 0    | 1    | 624            | 624.0                                         | 312.0 | 208.0 | 156.0 | 104.0 | 78.0  | 62.4  | 31.2  | 20.8  | 15.60 | 10.4  | 7.80  |
| 1             | 1    | 0    | 936            | 936.0                                         | 468.0 | 312.0 | 234.0 | 156.0 | 117.0 | 93.6  | 46.8  | 31.2  | 23.4  | 15.60 | 11.70 |
| 1             | 1    | 1    | 1248           | 1248.0                                        | 624.0 | 416.0 | 312.0 | 208.0 | 156.0 | 124.8 | 62.4  | 41.6  | 31.2  | 20.8  | 15.60 |

Note: Above gray zone is prohibited to set. SDRAM request: 4096 times per 64ms.(Refresh request: under  $15.625\ \mu\text{s}$ )

## (b) Self Refresh

The Self Refresh Entry command is issued by setting SDCMM<SCMM2:0> to “101”. Figure 3.10.7 shows the Self Refresh cycle timing. Before entering Self-refresh mode, issue the all Bank Pre-charge Command. Once Self Refresh is started, the SDRAM is refreshed internally without the need to issue the Auto Refresh command.

Note 1: When standby mode is released by a system reset, the I/O registers are initialized and the Self Refresh state is exited. Note that the Auto Refresh function is also disabled at this time.

Note 2: The SDRAM cannot be accessed while it is in the Self Refresh state.

Note 3: To execute the HALT instruction after the Self Refresh Entry command, insert at least 10 bytes of NOP or other instructions between the instruction to set SDCMM<SCMM2:0> to “101” and the HALT instruction.

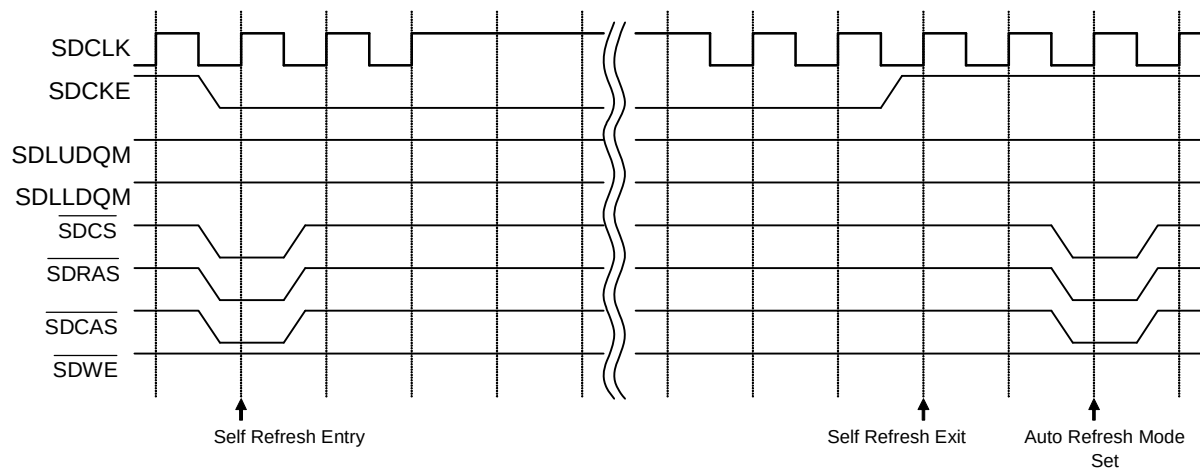


Figure 3.10.7 Self Refresh Cycle Timing

Setting Example

```

org 0x2000 ; Internal RAM
ld (sdcm),0x02 ; All Bank Precharge Command
ld (sdcm),0x05 ; Self Refresh Entry Command
NOP×10 ; Setup time
halt ;

```

The Self Refresh state can be exited by the Self Refresh Exit command. The Self Refresh Exit command is executed when SDCMM<SCMM2:0> is set to “110”. It is also executed automatically in synchronization with HALT mode release. In either of these two cases, Auto Refresh is performed immediately after the Self Refresh state is exited. Then, Auto Refresh is executed at specified intervals. Exiting the Self Refresh state clears SDCMM<SCMM2:0> to “000”.

| SDRAM Refresh Control Register |             |                  |   |                                                          |                                                                                                                                                                         |      |      |                                       |
|--------------------------------|-------------|------------------|---|----------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|---------------------------------------|
|                                | 7           | 6                | 5 | 4                                                        | 3                                                                                                                                                                       | 2    | 1    | 0                                     |
| SDRCR (0252H)                  | Bit symbol  | –                |   | SSAE                                                     | SRS2                                                                                                                                                                    | SRS1 | SRS0 | SRC                                   |
|                                | Read/Write  | R/W              |   | R/W                                                      |                                                                                                                                                                         |      |      |                                       |
|                                | Reset State | 0                |   | 1                                                        | 0                                                                                                                                                                       | 0    | 0    | 0                                     |
|                                | Function    | Always write “0” |   | Self Refresh auto exit function<br>0:Disable<br>1:Enable | Refresh interval<br>000: 47 states    100: 468 states<br>001: 78 states    101: 624 states<br>010: 156 states    110: 936 states<br>011: 312 states    111: 1248 states |      |      | Auto Refresh<br>0:Disable<br>1:Enable |

Setting SDRCR<SSAE> to “1” enables automatic execution of the Self Refresh Exit command in synchronization with HALT release.

Setting SDRCR<SSAE> to “0” disables automatic execution of the Self Refresh Exit command in synchronization with HALT release. The auto exit function should also be disabled in cases where the SDRAM operation requirements cannot be met as the operation clock frequency is reduced by clock gear down, as shown in Figure 3.10.8.

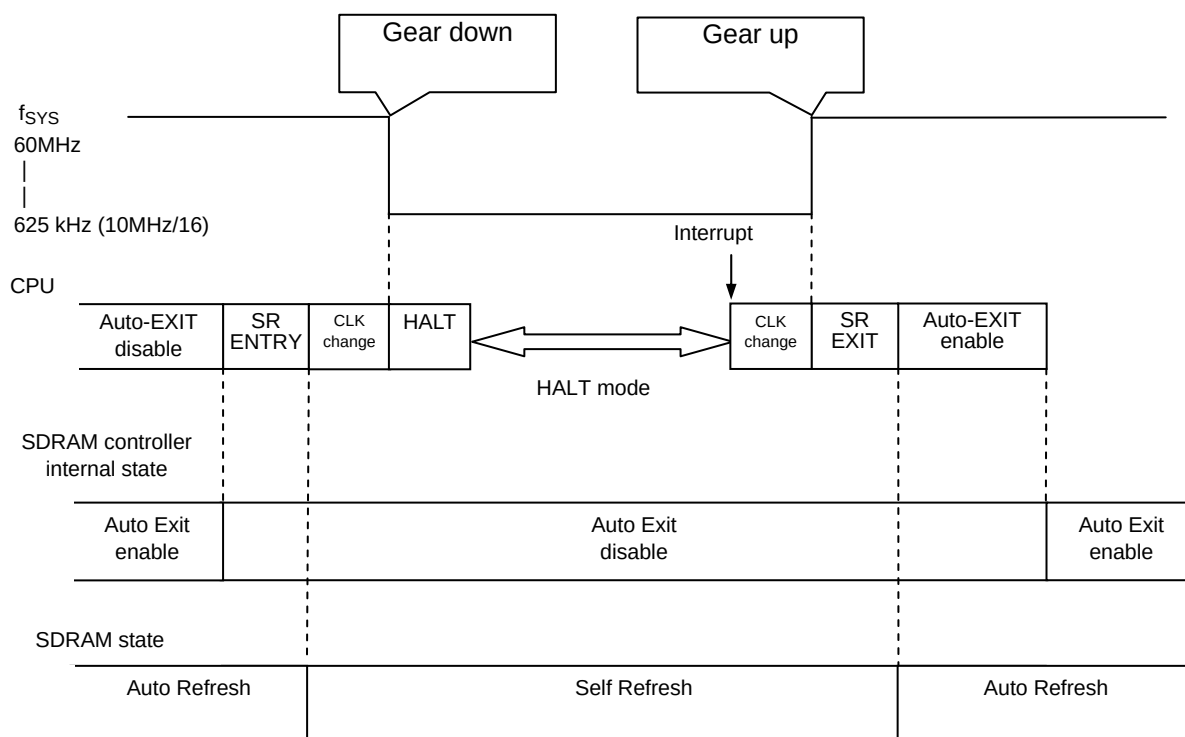


Figure 3.10.8 Execution Flow for Executing HALT Instruction after Clock Gear Down

## (7) SDRAM initialization sequence

After reset release, the following sequence of commands can be executed to initialize the SDRAM.

Precharge All command

Eight Auto Refresh commands

Mode Register Set command

The above commands are issued by setting SDCMM<SCMM2:0> to "001". While these commands are issued, the CPU operation (instruction fetch, execution) is halted. Before executing the initialization sequence, appropriate port settings must be made to enable the SDRAM control signals and address signals (A0 to A15).

After the initialization sequence is completed, SDCMM<SCMM2:0> is automatically cleared to "000".

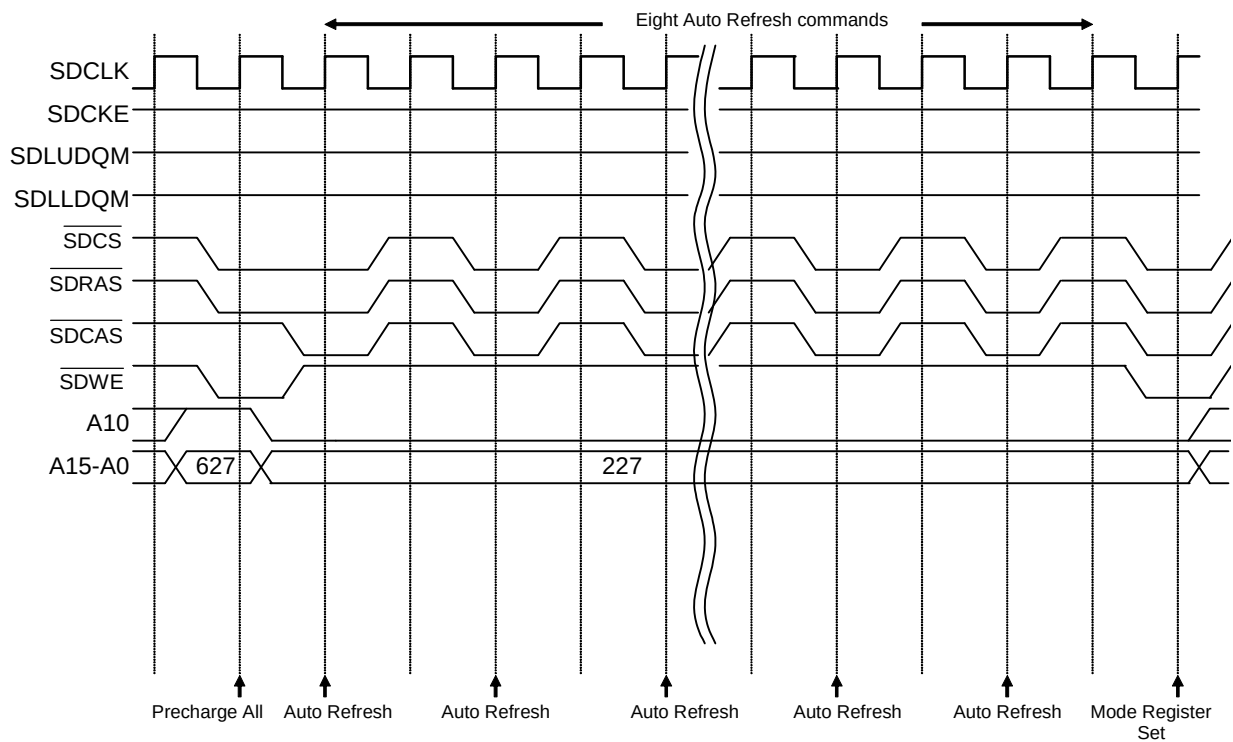


Figure3.10.9 Initialization Sequence Timing

## (8) Connection example

Figure 3.10.10 shows an example of connections between the TMP92CF30 and SDRAM.

Table 3.10.4 Pin Connections

| 92CF30<br>Pin Name | SDRAM Pin Name         |              |              |              |              |
|--------------------|------------------------|--------------|--------------|--------------|--------------|
|                    | Data Bus Width 16 bits |              |              |              |              |
|                    | 16M                    | 64M          | 128M         | 256M         | 512M         |
| A0                 | A0                     | A0           | A0           | A0           | A0           |
| A1                 | A1                     | A1           | A1           | A1           | A1           |
| A2                 | A2                     | A2           | A2           | A2           | A2           |
| A3                 | A3                     | A3           | A3           | A3           | A3           |
| A4                 | A4                     | A4           | A4           | A4           | A4           |
| A5                 | A5                     | A5           | A5           | A5           | A5           |
| A6                 | A6                     | A6           | A6           | A6           | A6           |
| A7                 | A7                     | A7           | A7           | A7           | A7           |
| A8                 | A8                     | A8           | A8           | A8           | A8           |
| A9                 | A9                     | A9           | A9           | A9           | A9           |
| A10                | A10                    | A10          | A10          | A10          | A10          |
| A11                | BS                     | A11          | A11          | A11          | A11          |
| A12                | –                      | BS0          | BS0          | A12          | A12          |
| A13                | –                      | BS1          | BS1          | BS0          | BS0          |
| A14                | –                      | –            | –            | BS1          | BS1          |
| A15                | –                      | –            | –            | –            | –            |
| SDCS               | CS                     | CS           | CS           | CS           | CS           |
| SDLUDQM            | UDQM                   | UDQM         | UDQM         | UDQM         | UDQM         |
| SDLLDQM            | LDQM                   | LDQM         | LDQM         | LDQM         | LDQM         |
| SDRAS              | RAS                    | RAS          | RAS          | RAS          | RAS          |
| SDCAS              | CAS                    | CAS          | CAS          | CAS          | CAS          |
| SDWE               | WE                     | WE           | WE           | WE           | WE           |
| SDCKE              | CKE                    | CKE          | CKE          | CKE          | CKE          |
| SDCLK              | CLK                    | CLK          | CLK          | CLK          | CLK          |
| SDACR<br><SMUXW>   | 00:<br>TypeA           | 00:<br>TypeA | 01:<br>TypeB | 01:<br>TypeB | 10:<br>TypeC |

■: Command address pin of SDRAM

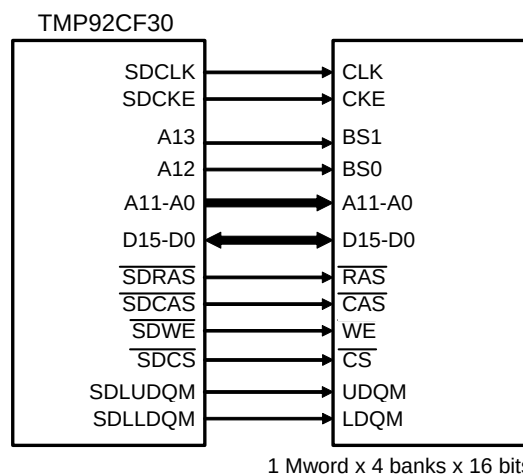


Figure 3.10.10 An Example of Connections between TMP92CF30 and SDRAM

### 3.10.3 An Example of Calculating HDMA Transfer Time

The following shows an example of calculating the HDMA transfer time when SDRAM is used as the transfer source.

- Transfer from SDRAM to internal SRAM

Conditions:

System clock ( $f_{\text{SYS}}$ ) : 60 MHz  
 SDRAM read cycle : Full page (5-1-1-1), 16-bit data bus  
 16-bit data bus  
 SDRAM Auto Refresh interval: 936 states (15.6  $\mu\text{s}$ )  
 Internal RAM write cycle : 1 state, 32-bit data bus  
 Number of bytes to transfer : 512 bytes

Calculation example:

$$\begin{aligned} \text{Transfer time} &= (\text{SDRAM read time} + \text{SRAM write time}) \times \text{transfer count} \\ &\quad + (\text{SDRAM burst start} + \text{stop time}) \\ &\quad + (\text{Precharge time} + \text{Auto Refresh time}) \times \text{Auto Refresh count} \end{aligned}$$

(a) Read/write time

$$\begin{aligned} &(\text{SDRAM read 1 state} \times 2 + \text{Internal RAM write 1 state}) \times 512 \text{ bytes}/4 \text{ bytes} \\ &= 384 \text{ states} \times 1/60 \text{ MHz} \\ &= 6.4 \mu\text{s} \end{aligned}$$

(b) Burst start/stop time

$$\begin{aligned} &\text{Start (TRCD: 2CLK) 5 states} + \text{Stop 2 states} \\ &= 7 \text{ states}/60 \text{ MHz} \\ &= 0.117 \mu\text{s} \end{aligned}$$

(c) Auto Refresh time

Based on the above (a), Auto Refresh occurs once or zero times in 384 states. It is assumed that Auto Refresh occurs once here.

$$\begin{aligned} &(\text{Precharge (TRP: 2CLK) 2 states} + \text{AREF (TRC: 5CLK) 5 states}) \times \text{AREF once} \\ &= 7 \text{ states} \times 1/60 \text{ MHz} \\ &= 0.117 \mu\text{s} \end{aligned}$$

$$\begin{aligned} \text{Total transfer time} &= (a) + (b) + (c) \\ &= 6.4 \mu\text{s} + 0.117 \mu\text{s} + 0.117 \mu\text{s} \\ &= 6.634 \mu\text{s} \end{aligned}$$

### 3.10.4 Considerations for Using the SDRAMC

This section describes the points that must be taken into account when using the SDRAMC. Please carefully read the following to ensure proper use of the SDRAMC.

#### 1) WAIT access

When SDRAM is used, the following restriction applies to memory access to other than the SDRAM.

In the external WAIT pin input setting of the memory controller, the maximum external WAIT period that can be set is limited to “Auto Refresh interval × 8190”.

#### 2) Execution of the Self Refresh Entry, Initialization Sequence, or Precharge All command before the HALT instruction

Execution of the commands issued by the SDRAMC (Self Refresh Entry, Initialization Sequence, Precharge All) requires several states after the SDCMM register is set.

Therefore, to execute the HALT instruction after one of these commands, be sure to insert at least 10 bytes of NOP or other instructions.

#### 3) Auto Refresh interval setting

When SDRAM is used, the system clock frequency must be set to satisfy the minimum operation frequency and minimum Auto Refresh interval of the SDRAM to be used.

In a system in which SDRAM is used and the clock is geared up and down, the Auto Refresh interval must be set carefully.

Before changing the Auto Refresh interval, ensure that SDRCCR<SRC> is set to “0” to disable the Auto Refresh function.

#### 4) Changing SFR settings

Before changing the settings of the SDACR<SPRE> and SDCISR registers, ensure that the SDRAMC is disabled (SDACR<SMAC> = “0”).

#### 5) Disabling the SDRAMC

Set the following procedure, when disable the SDRAMC.

```

LOOP:  LD   (SDCMM),0x02    ; Issue to All Bank Precharge
        LD   A,(SDCMM)      ; Read SDCMM
        CP   A,0x00        ; Palling it until the All Bank Precharge command is finished
        JP   NZ,LOOP        ;
        LD   (SDACR),0x00   ; Stop the SDRAM controller

```



### 3.11 NAND Flash Controller (NDFC)

#### 3.11.1 Features

The NAND Flash Controller (NDFC) is provided with dedicated pins for connecting with NAND Flash memory.

The NDFC also has an ECC calculation function for error correction and supports two types of ECC calculation methods. The ECC calculation method using Hamming codes can be used for NAND Flash memory of SLC (Single Level Cell) type and is capable of detecting a single-bit error for every 256 bytes. The ECC calculation method using Reed-Solomon codes can be used for NAND Flash memory of MLC (Multi Level Cell) type and is capable of detecting four error addresses for every 518 bytes.

Although the NDFC has two channels (channel 0, channel 1), all pins except for Chip Enable are shared between the two channels. Only the operation of channel 0 is explained here.

The NDFC has the following features:

- 1) Controls the NAND Flash memory interface through registers.
- 2) Supports 8-bit and 16-bit NAND Flash memory devices.
- 3) Supports page sizes of 512 bytes and 2048 bytes.
- 4) Supports large-capacity block sizes over 256 Kbytes.
- 5) Includes an ECC generation circuit using Hamming codes (for SLC type).
- 6) Includes a 4-address (4-byte) error detection circuit using Reed-Solomon coding/encoding techniques (for MLC type).

Note 1: The  $\overline{\text{WP}}$  (Write Protect) pin of NAND Flash is not supported. If this function is needed, prepare it on an external circuit.

Note 2: The two channels cannot be accessed simultaneously. It is necessary to switch between the two channels.

3.11.2 Block Diagram

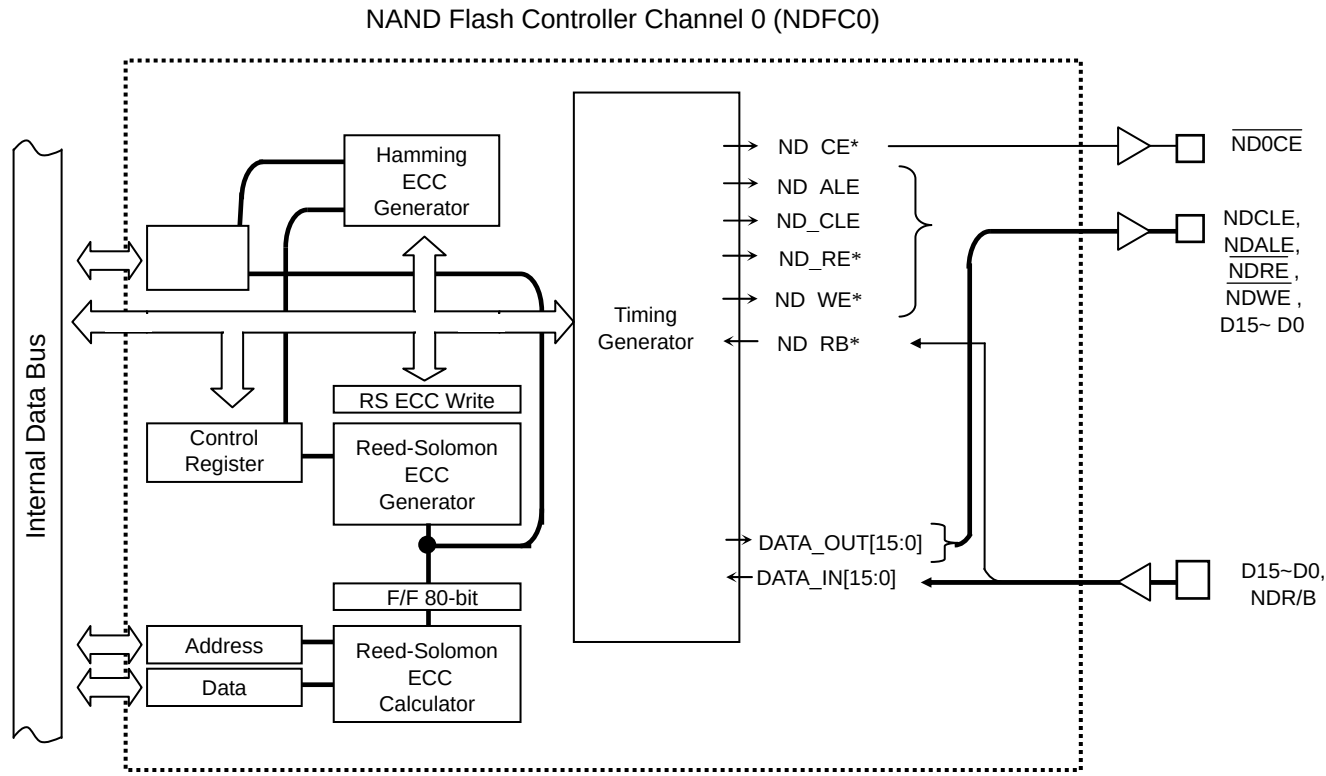


Figure 3.11.1 Block Diagram for NAND Flash Controller

### 3.11.3 Operation Description

#### 3.11.3.1 Accessing NAND Flash Memory

The NDFC accesses data on NAND Flash memory indirectly through its internal registers. This section explains the operations for accessing the NAND Flash.

Since no dedicated sequencer is provided for generating commands to the NAND Flash, the levels of the NDCLE, NDALE, and  $\overline{\text{NDCE}}$  pins must be controlled by software.

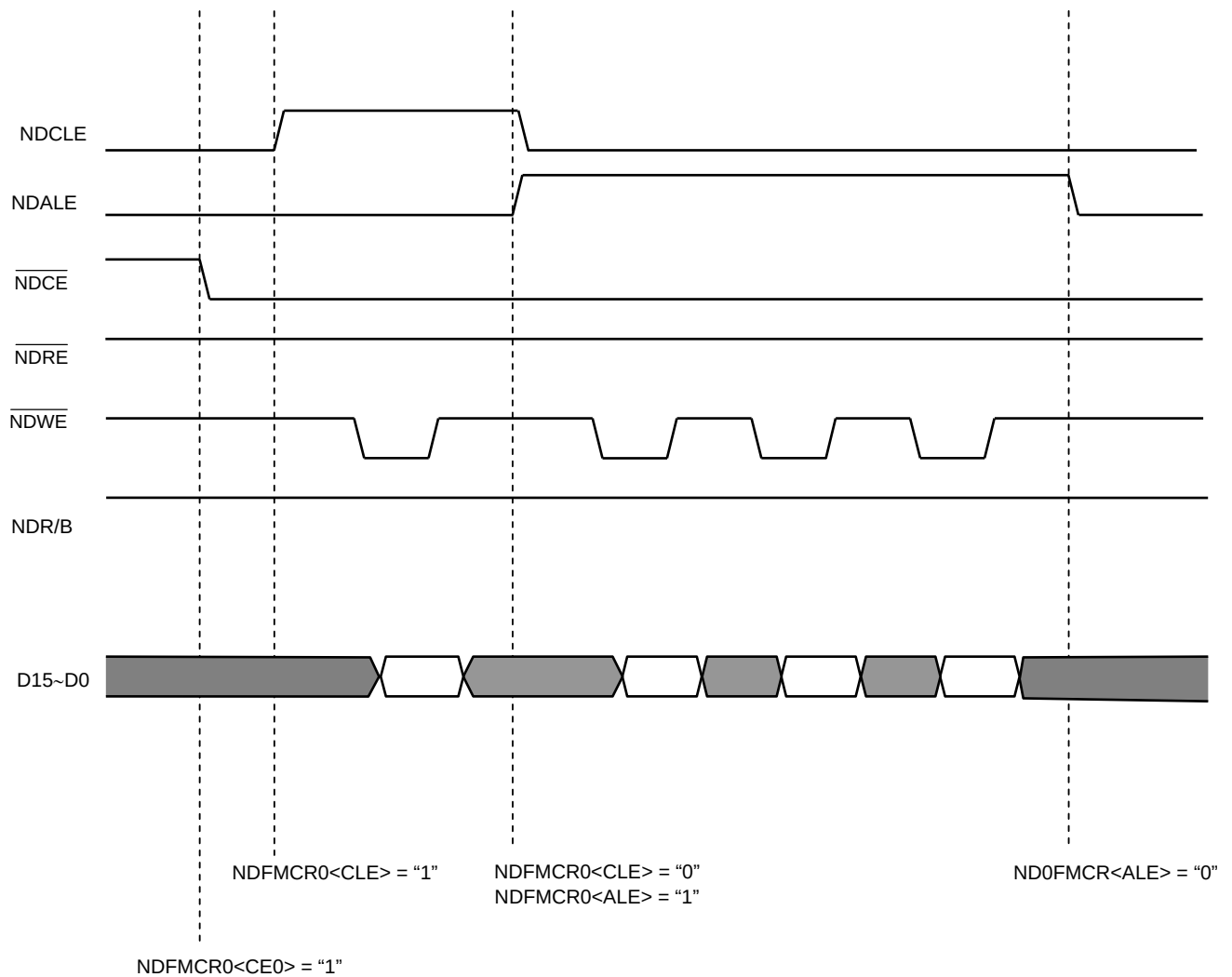


Figure3.11.2 Basic Timing for Accessing NAND Flash

The  $\overline{\text{NDRE}}$  and  $\overline{\text{NDWE}}$  signals are explained next. Write and read operations to and from the NAND Flash are performed through the ND0FDTR register. The actual write operation completes not when the ND0FDTR register is written to but when the data is written to the external NAND Flash. Likewise, the actual read operation completes not when the ND0FDTR register is read but when the data is read from the external NAND Flash.

At this time, the Low and High widths of  $\overline{\text{NDRE}}$  and  $\overline{\text{NDWE}}$  can be adjusted according to the CPU operating speed ( $f_{\text{sys}}$ ) and the access time of the NAND Flash. (For details, refer to the electrical characteristics.)

The following shows an example of accessing the NAND Flash in 6 clocks by setting  $\text{NDFMCR0} < \text{SPLW1:0} > = 2$  and  $\text{NDFMCR0} < \text{SPHW1:0} > = 2$ . (In write cycles, the data drive time also becomes longer.)

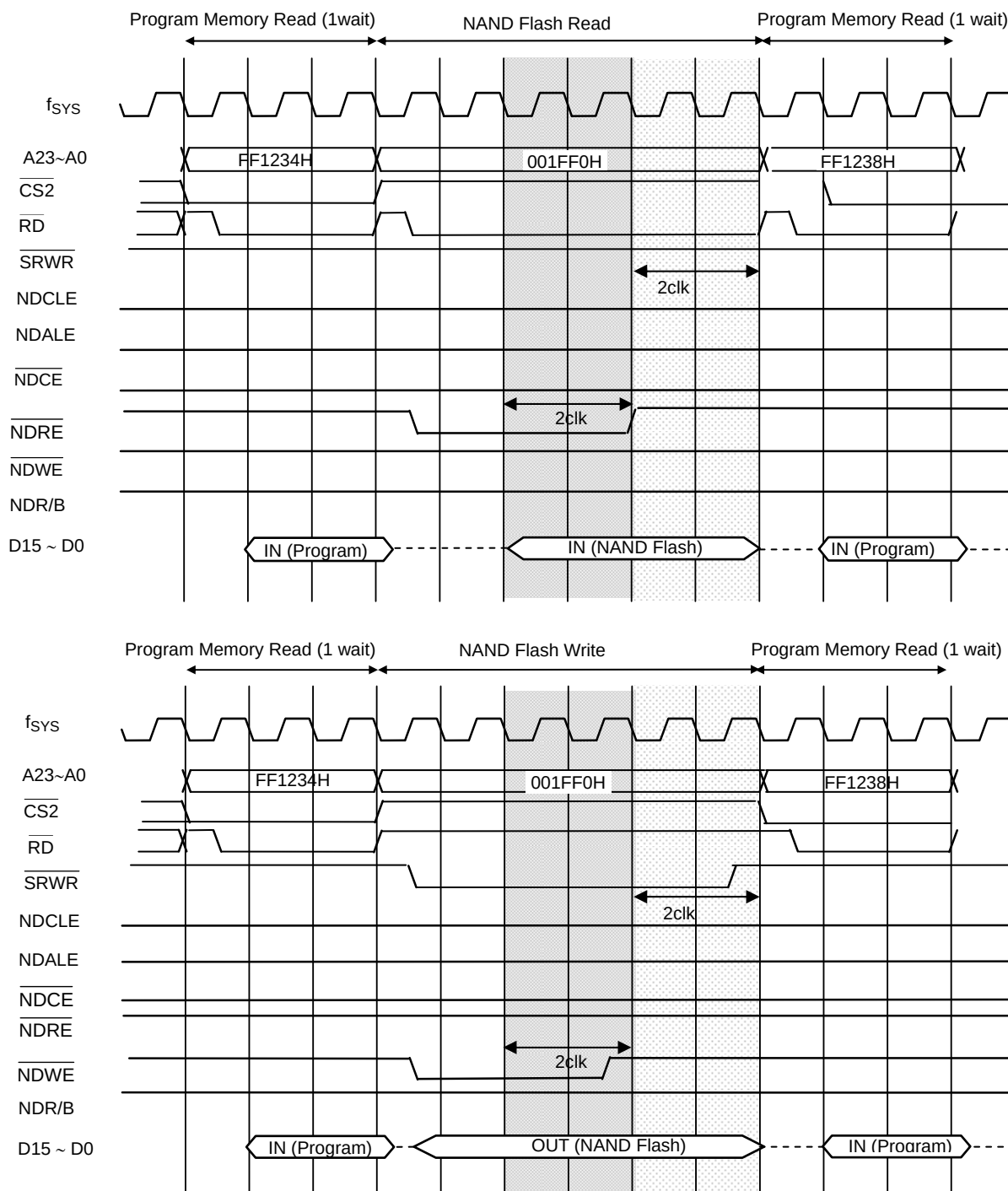


Figure3.11.3 Read/Write Access to NAND Flash

### 3.11.4 ECC Control

NAND Flash memory devices may inherently include error bits. It is therefore necessary to implement the error correction processing using ECC (Error Correction Code).

Figure3.11.4 shows a basic flowchart for ECC control.

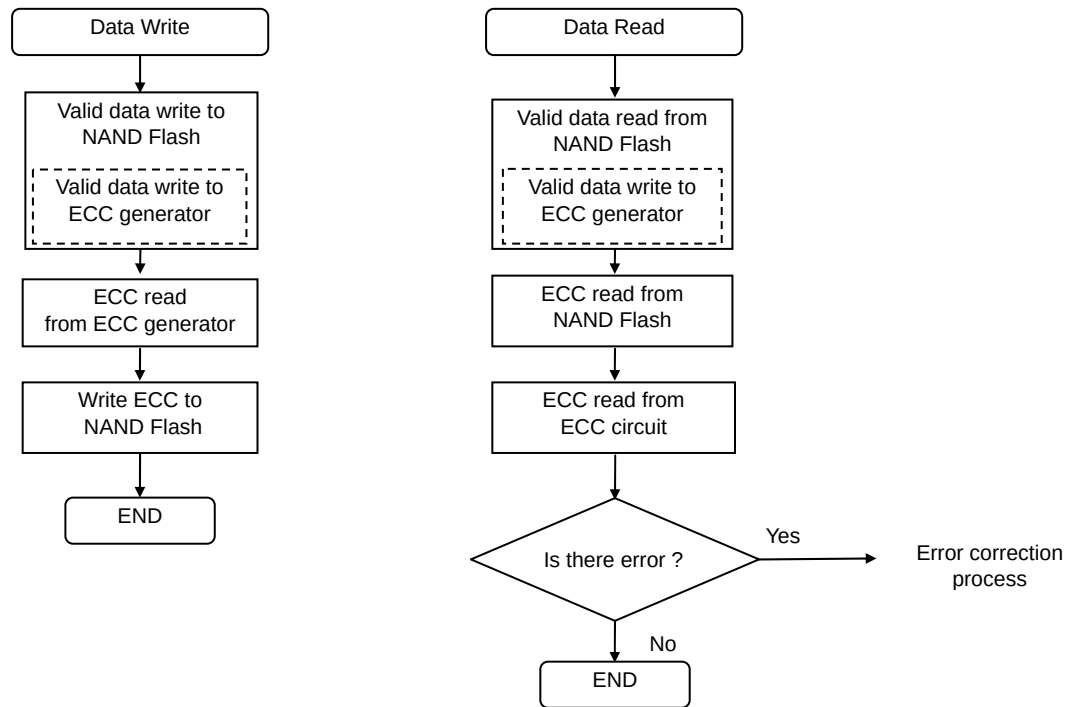


Figure3.11.4 Basic Flow of ECC Control

#### Write:

1. When data is written to the actual NAND Flash memory, the ECC generator in the NDFC simultaneously generates ECC for the written data.
2. The ECC is written to the redundant area in the NAND Flash separately from the valid data.

#### Read:

1. When data is read from the actual NAND Flash memory, the ECC generator in the NDFC simultaneously generates ECC for the read data.
2. The ECC for the written data and the ECC for the read data are compared to detect and correct error bits.

### 3.11.4.1 Differences between Hamming Codes and Reed-Solomon Codes

The NDFC includes an ECC generator supporting NAND Flash memory devices of SLC (or 2LC: two states) type and MLC (or 4LC: four states) type.

The ECC calculation using Hamming codes (supporting SLC) generates 22 bits of ECC for every 256 bytes of valid data and is capable of detecting and correcting a single-bit error for every 256 bytes. Error bit detection calculation and correction must be implemented by software. When using SmartMedia™, Hamming codes should be used.

The ECC calculation using Reed-Solomon codes (supporting MLC) generates 80 bits of ECC for every 1 byte to 518 bytes of valid data and is capable of detecting and correcting error bits at four addresses for every 518 bytes. When using Reed-Solomon codes, error bit detection calculation is supported by hardware and only error bit correction needs to be implemented by software.

The differences between Hamming codes and Reed-Solomon codes are summarized in Table 3.11.1.

Table 3.11.1 Differences between Hamming Codes and Reed-Solomon Codes

|                                      | Hamming                             | Reed-Solomon                                                    |
|--------------------------------------|-------------------------------------|-----------------------------------------------------------------|
| Maximum number of correctable errors | 1 bit                               | 4 addresses<br>(All the 8 bits at one address are correctable.) |
| Number of ECC bits                   | 22 bits/256 bytes                   | 80 bits/up to 518 bytes                                         |
| Error bit detection method           | Software                            | Hardware                                                        |
| Error bit correction method          | Software                            | Software                                                        |
| Error bit detection time             | Depends on the software to be used. | See the table below.                                            |
| Others                               | Supports SmartMedia™.               | —                                                               |

| Number of Error Bits | Reed-Solomon Error Bit Detection Time<br>(Unit: Clocks) | Notes                                                                                                                              |
|----------------------|---------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------|
| 4                    | 813 (max)                                               | These values indicate the total number of clocks for detecting error bit(s) not including the register read/write time by the CPU. |
| 3                    | 648 (max)                                               |                                                                                                                                    |
| 2                    | 358 (max)                                               |                                                                                                                                    |
| 1                    | 219 (max)                                               |                                                                                                                                    |
| 0                    | 1                                                       |                                                                                                                                    |

## 3.11.4.2 Error Correction Methods

## Hamming ECC

- The ECC generator generates 44 bits of ECC for a page containing 512 bytes of valid data. The error correction process must be performed in units of 256 bytes (22 bits of ECC). The following explains how to implement error correction on 256 bytes of valid data using 22 bits of ECC.
  - If the NAND Flash to be used has a large-capacity page size (e.g. 2048 bytes), the error correction process must be repeated several times to cover the entire page.
- 1) The calculated ECC and the ECC in the redundant area are rearranged, respectively, so that the lower 2 bytes represent line parity (LPR15:0) and the upper 1 byte (of which the upper 6 bits are valid) represents column parity (CPR7:2).
  - 2) The two rearranged ECCs are XORed.
  - 3) If the XOR result is 0 indicating an ECC match, the error correction process ends normally (no error). If the XOR result is other than 0, it is checked whether or not the error data can be corrected.
  - 4) If the XOR result contains only one ON bit, it is determined that a single-bit error exists in the ECC data itself and the error correction process terminates here (error not correctable).
  - 5) If each pair of bits 0 to 21 of the XOR result is either 01B or 10B, it is determined that the error data is correctable and error correction is performed accordingly. If the XOR result contains either 00B or 11B, it is determined that the error data is not correctable and the error correction process terminates here.

|        | An Example of Correctable XOR Result                                                                                            | An Example of Uncorrectable XOR Result                                                                                          |
|--------|---------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|
| Binary | <div> <div>10 01 10</div> 00 Column parity           <div>10 10 01 10</div> Line parity           <div>01 01 10 10</div> </div> | <div> <div>10 11 10</div> 00 Column parity           <div>10 10 01 10</div> Line parity           <div>01 01 10 10</div> </div> |

- 6) The line and bit positions of the error are detected using the line parity and column parity of the XOR result, respectively. The error bit thus detected is then inverted. This completes the error correction process.

Example: When the XOR result is 1001101010011001011010

Convert two bytes of line parity into one byte (10→1, 01→0).

Convert six bits of column parity into three bits (10→1, 01→0).

Line parity:            10 10 01 10 01 01 10 10  
                           ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓  
                           1  1  0  1  0  0  1  1 = D3H            \*Error at D3/FF H

Column parity:        10 01 10  
                           ↓ ↓ ↓  
                           1  0  1 = 5                                \*Error in bit 5

Based on the above, error correction is performed by inverting the data in bit 5 at address 212.

## Reed-Solomon ECC

- The ECC generator generates 80 bits of ECC for up to 518 bytes of valid data. If the NAND Flash to be used has a large-capacity page size (e.g. 2048 bytes), the error correction process must be repeated several times to cover the entire page.
  - Basically no calculation is needed for error correction. If error detection is performed properly, the NDFC only needs to refer to the error address and error bit. However, it may be necessary to convert the error address, as explained below.
- 1) If the error address indicated by the NDRSCAN register is in the range of 000H to 007H, this error exists in the ECC area and no correction is needed in this case.  
(It is not able to correct the error in the ECC area. However, if the error exists in the ECC area, only 4symbol (include the error in the ECC area) can correct the error to this LSI. Please be careful.)
  - 2) If the error address indicated by the NDRSCAN register is in the range of 008H to 20DH, the actual error address is obtained by subtracting this address from 20 DH.  
(If the valid data is processed as 512 byte, the actual error address is obtained by subtracting this address from 207H when the error address in the range of 008H to 207H.)

## Example 1:

NDRSCAN = 005H, NDRSCDn = 04H = 00000100B

As the error address (005H) is in the range of 000H to 007H, no correction is needed.

(Although an error exists in bit 2, no correction is needed.)

## Example 2:

NDRSCAN = 083H, NDRSCDn = 81H = 10000001B

The actual error address is obtained by subtracting 083H from 20DH. Thus, the error correction process inverts the data in bits 7 and 0 at address 18AH.

(If the valid data is 512 byte, the actual error address is obtained by subtracting 083H from 207H. Thus, the error correction process inverts the data in bits 7 and 0 at address 184H.)

Note: If the error address (after converted) is in the range of 000H to 007H, it indicates that an error bit exists in redundant area (ECC). In this case, no error correction is needed. If the number of error bits is not more than 4 symbols, Reed-Solomon codes calculate each error bit precisely even if it is the redundant area (ECC).



## 3.11.5 Description of Registers

| NAND Flash Control 0 Register                                     |             |                                                                          |                                            |                                                                           |                                                                |                                                                |                                                                              |                                                                                                     |                                                                                     |
|-------------------------------------------------------------------|-------------|--------------------------------------------------------------------------|--------------------------------------------|---------------------------------------------------------------------------|----------------------------------------------------------------|----------------------------------------------------------------|------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| NDFMCR0<br>(08C0H)                                                |             | 7                                                                        | 6                                          | 5                                                                         | 4                                                              | 3                                                              | 2                                                                            | 1                                                                                                   | 0                                                                                   |
|                                                                   | bit Symbol  | WE                                                                       | ALE                                        | CLE                                                                       | CE0                                                            | CE1                                                            | ECCE                                                                         | BUSY                                                                                                | ECCRST                                                                              |
|                                                                   | Read/Write  | R/W                                                                      |                                            |                                                                           |                                                                |                                                                |                                                                              | R                                                                                                   | W                                                                                   |
|                                                                   | Reset State | 0                                                                        | 0                                          | 0                                                                         | 0                                                              | 0                                                              | 0                                                                            | 0                                                                                                   | 0                                                                                   |
| A<br>read-modify<br>-write<br>operation<br>cannot be<br>performed | Function    | WE<br>enable<br>0: Disable<br>1: Enable                                  | ALE<br>control<br>0: "L" out<br>1: "H" out | CLE<br>control<br>0: "L" out<br>1: "H" out                                | $\overline{\text{CE0}}$<br>control<br>0: "H" out<br>1: "L" out | $\overline{\text{CE1}}$<br>control<br>0: "H" out<br>1: "L" out | ECC<br>circuit<br>control<br>0: Disable<br>1: Enable                         | NAND<br>Flash<br>state<br>1: Busy<br>0: Ready                                                       | ECC<br>reset<br>control<br>0: –<br>1: Reset<br>*Always<br>read as<br>"0".           |
|                                                                   |             |                                                                          |                                            |                                                                           |                                                                |                                                                |                                                                              |                                                                                                     |                                                                                     |
| (08C1H)                                                           |             | 15                                                                       | 14                                         | 13                                                                        | 12                                                             | 11                                                             | 10                                                                           | 9                                                                                                   | 8                                                                                   |
|                                                                   | bit Symbol  | SPLW1                                                                    | SPLW0                                      | SPHW1                                                                     | SPHW0                                                          | RSECCL                                                         | RSEDN                                                                        | RSESTA                                                                                              | RSECGW                                                                              |
|                                                                   | Read/Write  | R/W                                                                      |                                            |                                                                           |                                                                |                                                                |                                                                              | W                                                                                                   | R/W                                                                                 |
|                                                                   | Reset State | 0                                                                        | 0                                          | 0                                                                         | 0                                                              | 0                                                              | 0                                                                            | 0                                                                                                   | 0                                                                                   |
| A<br>read-modify-<br>write<br>operation<br>cannot be<br>performed | Function    | Strobe pulse width<br>(Low width of NDRE ,<br>$\overline{\text{NDWE}}$ ) |                                            | Strobe pulse width<br>(High width of NDRE ,<br>$\overline{\text{NDWE}}$ ) |                                                                | Reed-<br>Solomon<br>ECC<br>latch                               | Reed-<br>Solomon<br>operation<br>0: Encode<br>(Write)<br>1: Decode<br>(Read) | Reed-<br>Solomon<br>error<br>calculation<br>start<br>0: –<br>1: Start<br>*Always<br>read as<br>"0". | Reed-<br>Solomon<br>ECC<br>generator<br>write<br>control<br>0: Disable<br>1: Enable |
|                                                                   |             | Inserted width<br>= (fSYS) × (set value)                                 |                                            | Inserted width<br>= (fSYS) × (set value)                                  |                                                                | 0: Disable<br>1: Enable                                        |                                                                              |                                                                                                     |                                                                                     |

Figure3.11.5 NAND Flash Mode Control 0 Register

## (a) &lt;ECCRST&gt;

The <ECCRST> bit is used for both Hamming and Reed-Solomon codes.

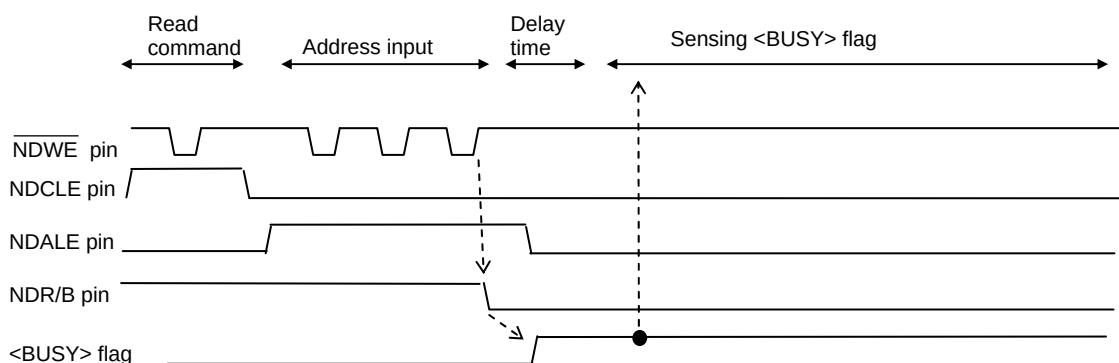
When NDFMCR1<ECCS>="0", setting this bit to "1" clears the Hamming ECC in the ECC generator. When NDFMCR1<ECCS>="1", setting this bit to "1" clears the Reed-Solomon ECC. Note that this bit is ineffective when NDFMCR0<ECCE>="0". Before writing to this bit, ensure that NDFMCR0<ECCE>="1".

## (b) &lt;BUSY&gt;

The <BUSY> bit is used for both Hamming and Reed-Solomon codes.

This bit is used to check the state of the NAND Flash memory (NDR/B pin). It is set to "1" when the NAND Flash is "busy" and to "0" when it is "ready".

Since the NDFC incorporates a noise filter of several states, a change in the NDR/B pin state is reflected on the <BUSY> flag after some delay. It is therefore necessary to insert a delay time by software (e.g. ten NOP instructions) before checking this flag.



## (c) &lt;ECCE&gt;

The <ECCE> bit is used for both Hamming and Reed-Solomon codes.

This bit is used to enable or disable the ECC generator. To reset the ECC in the ECC generator (to set <ECCRST> to “1”), the ECC generator must be enabled (<ECCE> = “1”).

## (d) &lt;CE1:0&gt;, &lt;CLE&gt;, &lt;ALE&gt;

The <CE1:0>, <CLE>, and <ALE> bits are used for both Hamming and Reed-Solomon codes to control the pins of the NAND Flash memory.

## (e) &lt;WE&gt;

The <WE> bit is used for both Hamming and Reed-Solomon codes to enable or disable write operations.

## (f) &lt;RSECGW&gt;

The <RSECGW> bit is used only for Reed-Solomon codes. When Hamming codes are used, this bit should be set to “0”.

Since valid data and ECC are processed differently, the NDFC needs to know whether valid data or ECC is to be read. This control is implemented by software using this bit.

To read valid data from the NAND Flash, set <RSECGW> to “0”. To read ECC written in the redundant area in the NAND Flash, set <RSECGW> to “1”.

Note 1: Valid data and ECC cannot be read continuously by DMA transfer. After valid data has been read, DMA transfer should be stopped once to change the <RSECGW> bit from “0” to “1” before ECC can be read.

Note 2: Immediately after ECC is read from the NAND Flash, the NAND Flash access operation or error bit calculation cannot be performed for a duration of 20 system clocks ( $f_{SYS}$ ). It is necessary to insert 20 NOP instructions or the like.

## (g) &lt;RSESTA&gt;

The <RSESTA> bit is used only for Reed-Solomon codes.

The error address and error bit position are calculated using an intermediate code generated from the ECC for written data and the ECC for read data. Setting <RSESTA> to “1” starts this calculation.

## (h) &lt;RSEDN&gt;

The <RSEDN> bit is used only for Reed-Solomon codes. When using Hamming codes, this bit should be set to “0”.

For a write operation, this bit should be set to “0” (encode) to generate ECC. The ECC read from the NDECCRDn register is written to the redundant area in the NAND Flash. For a read operation, this bit should be set to “1” (decode). In this case, valid data is read from the NAND Flash and the ECC written in the redundant area is also read to generate an intermediate code for calculating the error address and error bit position.

## (i) &lt;RSECCL&gt;

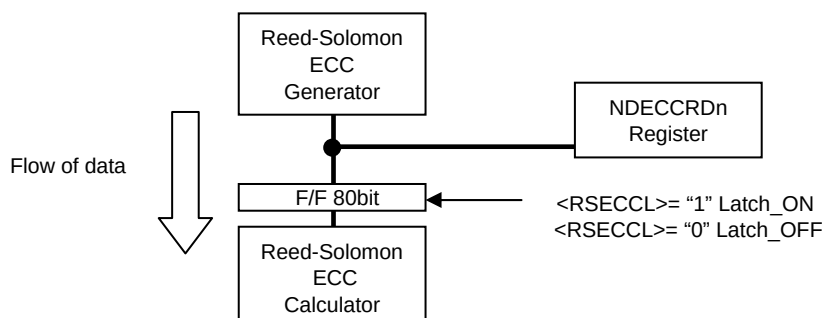
The <RSECCL> bit is used only for Reed-Solomon codes. When using Hamming codes, this bit should be set to "0".

The Reed-Solomon processing unit is comprised of two elements: an ECC generator and an ECC calculator. The latter is used to calculate the error address and error bit position.

The error address and error bit position are calculated using an intermediate code generated from the ECC for written data and the ECC for read data. At this time, no special care is needed if ECC generation and error calculation are performed serially. If these operations need to be performed parallelly, the intermediate code used for error calculation must be latched while the calculation is being performed. The <RSECCL> bit is provided to enable this latch operation.

When <RSECCL> is set to "1", the intermediate code is latched so that the ECC generator can generate the ECC for another page without problem while the ECC calculator is calculating the error address and error bit position. At this time, the ECC generator can perform both encode (write) and decode (read) operations.

When <RSECCL> is set to "0", the latch is released and the contents of the ECC calculator are updated as the data in the ECC generator is updated.



## (j) &lt;SPHW1:0&gt;

The <SPHW1:0> bits are used for both Hamming and Reed-Solomon codes.

These bits are used to specify the High width of the  $\overline{\text{NDRE}}$  and  $\overline{\text{NDWE}}$  signals. The High width to be inserted is obtained by multiplying the value set in these bits by  $f_{\text{SYS}}$ .

## (k) &lt;SPLW1:0&gt;

The <SPLW1:0> bits are used for both Hamming and Reed-Solomon codes.

These bits are used to specify the Low width of the  $\overline{\text{NDRE}}$  and  $\overline{\text{NDWE}}$  signals. The Low width to be inserted is obtained by multiplying the value set in these bits by  $f_{\text{SYS}}$ .

| NAND Flash Control 1 Register |             |                                                |                                                                   |             |             |             |                                             |                                                     |                                              |
|-------------------------------|-------------|------------------------------------------------|-------------------------------------------------------------------|-------------|-------------|-------------|---------------------------------------------|-----------------------------------------------------|----------------------------------------------|
| NDFMCR1<br>(08C2H)            | <div></div> | 7                                              | 6                                                                 | 5           | 4           | 3           | 2                                           | 1                                                   | 0                                            |
|                               | bit Symbol  | INTERDY                                        | INTRSC                                                            | <div></div> | <div></div> | <div></div> | BUSW                                        | ECCS                                                | SYSCKE                                       |
|                               | Read/Write  | R/W                                            |                                                                   | <div></div> | <div></div> | <div></div> | R/W                                         |                                                     |                                              |
|                               | Reset State | 0                                              | 0                                                                 | <div></div> | <div></div> | <div></div> | 0                                           | 0                                                   | 0                                            |
|                               | Function    | Ready interrupt<br><br>0: Disable<br>1: Enable | Reed-Solomon calculation end interrupt<br>0: Disable<br>1: Enable |             |             |             | Data bus width<br><br>0: 8-bit<br>1: 16-bit | ECC calculation<br><br>0:Hamming<br>1: Reed-Solomon | Clock control<br><br>0: Disable<br>1: Enable |
| (08C3H)                       | <div></div> | 15                                             | 14                                                                | 13          | 12          | 11          | 10                                          | 9                                                   | 8                                            |
|                               | bit Symbol  | STATE3                                         | STATE2                                                            | STATE1      | STATE0      | SEER1       | SEER0                                       | <div></div>                                         | <div></div>                                  |
|                               | Read/Write  | R                                              |                                                                   |             |             |             |                                             | <div></div>                                         | <div></div>                                  |
|                               | Reset State | 0                                              | 0                                                                 | 0           | 0           | Undefined   | Undefined                                   | <div></div>                                         | <div></div>                                  |
|                               | Function    | Status read (See the table below.)             |                                                                   |             |             |             |                                             |                                                     |                                              |

Table3.11.2 Reed-Solomon Calculation Result Status Table

| STATE<3:0> | Meaning                                                          |
|------------|------------------------------------------------------------------|
| 0000       | Calculation ended 0 (No error)                                   |
| 0001       | Calculation ended 1(5 or more symbols in error; not correctable) |
| 0010       | Calculation ended 2 (Error found)                                |
| 0011       |                                                                  |
| 0100~1111  | Calculation in progress                                          |

Note: The <STATE3:0> value becomes effective after the calculation has started.

| SEER<1:0> | Meaning         |
|-----------|-----------------|
| 00        | 1-address error |
| 01        | 2-address error |
| 10        | 3-address error |
| 11        | 4-address error |

Note: The <SEER1:0> value becomes effective after the calculation has ended.

(a) <SYSCKE>

The <SYSCKE> bit is used for both Hamming and Reed-Solomon codes.

When using the NDFC, this bit must be set to “1” to enable the system clock. When not using the NDFC, power consumption can be reduced by setting this bit to “0”.

(b) <ECCS>

The <ECCS> bit is used to select whether to use Hamming codes or Reed-Solomon codes. This bit is set to “0” for using Hamming codes and to “1” for using Reed-Solomon codes. It is also necessary to set this bit for clearing ECC.

(c) <BUSW>

The <BUSW> bit is used for both Hamming and Reed-Solomon codes.

This bit specifies the bus width of the NAND Flash to be accessed (“0” = 8 bits, “1” = 16 bits). No other setting is required in the memory controller.

## (d) &lt;INTRSC&gt;

The <INTRSC> bit is used only for Reed-Solomon codes. When using Hamming codes, this bit should be set to “0”.

This bit is used to enable or disable the interrupt to be generated when the calculation of error address and error bit position has ended.

The interrupt is enabled when this bit is set to “1” and disabled when “0”.

## (e) &lt;INTRDY&gt;

The <INTRDY> bit is used for both Hamming and Reed-Solomon codes.

This bit is used to enable or disable the interrupt to be generated when the status of the NDR/B pin of the NAND Flash changes from “busy” (0) to “ready” (1). The interrupt is enabled when this bit is set to “1” and disabled when “0”.

## (f) &lt;STATE3:0&gt;, &lt;SEER1:0&gt;

The <STATE3:0> and <SEER1:0> bits are used only for Reed-Solomon codes. When using Hamming codes, they have no meaning.

These bits are used as flags to indicate the result of error address and error bit calculation. For details, see Table3.11.2.

| NAND Flash Data Register 0 |             |                                 |           |           |           |           |           |           |           |
|----------------------------|-------------|---------------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| NDFDTR0<br>(1FF0H)         | <div></div> | 7                               | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|                            | bit Symbol  | D7                              | D6        | D5        | D4        | D3        | D2        | D1        | D0        |
|                            | Read/Write  | R/W                             |           |           |           |           |           |           |           |
|                            | Reset State | Undefined                       | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
| (1FF1H)                    | Function    | NAND Flash Data Register (7-0)  |           |           |           |           |           |           |           |
|                            | <div></div> | 15                              | 14        | 13        | 12        | 11        | 10        | 9         | 8         |
|                            | bit Symbol  | D15                             | D14       | D13       | D12       | D11       | D10       | D9        | D8        |
|                            | Read/Write  | R/W                             |           |           |           |           |           |           |           |
|                            | Reset State | Undefined                       | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
|                            | Function    | NAND Flash Data Register (15-8) |           |           |           |           |           |           |           |

| NAND Flash Data Register 1 |             |                                 |           |           |           |           |           |           |           |
|----------------------------|-------------|---------------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| NDFDTR1<br>(1FF2H)         | <div></div> | 7                               | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|                            | bit Symbol  | D7                              | D6        | D5        | D4        | D3        | D2        | D1        | D0        |
|                            | Read/Write  | R/W                             |           |           |           |           |           |           |           |
|                            | Reset State | Undefined                       | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
|                            | Function    | NAND Flash Data Register (7-0)  |           |           |           |           |           |           |           |
| (1FF3H)                    | <div></div> | 15                              | 14        | 13        | 12        | 11        | 10        | 9         | 8         |
|                            | bit Symbol  | D15                             | D14       | D13       | D12       | D11       | D10       | D9        | D8        |
|                            | Read/Write  | R/W                             |           |           |           |           |           |           |           |
|                            | Reset State | Undefined                       | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
|                            | Function    | NAND Flash Data Register (15-8) |           |           |           |           |           |           |           |

Note: Although these registers allow both read and write operations, no flip-flop is incorporated. Since write and read operations are performed in different manners, it is not possible to read out the data that has been just written.

Figure3.11.6 NAND Flash Data Registers (NDFDTR0, NDFDTR1)

Write and read operations to and from the NAND Flash memory are performed by accessing the NDFDTR0 register. When you write to this register, the data is written to the NAND Flash. When you read from this register, the data is read from the NAND Flash. The NDFDTR0 register is used for both channel 0 and channel 1.

A total of 4 bytes are provided as data registers to enable 4-byte DMA transfer. For example, 4 bytes of data can be transferred from 32-bit internal RAM to 8-bit NAND Flash memory by DMA operation by setting the destination address as NDFDTR0. (NDFDTR1 cannot be set as the destination address.) The actual DMA operation is performed by first reading 4 bytes from the internal RAM and then writing 1 byte to the NAND Flash four times from the lowest address.

To access data in the NAND Flash, be sure to access NDFDTR0 (at address 1FF0). For details, see Table3.11.3.

Table3.11.3 How to Access the NAND Flash Data Register

## Write

| Access Data Size | Example of instruction | 8-bit NAND Flash | 16-bit NAND Flash |
|------------------|------------------------|------------------|-------------------|
| 1-byte access    | ld (0x1FF0),a          | Supported        | Not supported     |
| 2-byte access    | ld (0x1FF0),wa         | Supported        | Supported         |
| 4-byte access    | ld (0x1FF0),xwa        | Supported        | Supported         |

## Read

| Access Data Size | Example of instruction | 8-bit NAND Flash | 16-bit NAND Flash |
|------------------|------------------------|------------------|-------------------|
| 1-byte access    | ld a,(0x1FF0)          | Supported        | Not supported     |
| 2-byte access    | ld wa,(0x1FF0)         | Supported        | Supported         |
| 4-byte access    | ld xwa,(0x1FF0)        | Supported        | Supported         |

NAND Flash ECC Register 0

|                     |             |                                |        |        |        |        |        |       |       |
|---------------------|-------------|--------------------------------|--------|--------|--------|--------|--------|-------|-------|
| NDECCRD0<br>(08C4H) |             | 7                              | 6      | 5      | 4      | 3      | 2      | 1     | 0     |
|                     | bit Symbol  | ECCD7                          | ECCD6  | ECCD5  | ECCD4  | ECCD3  | ECCD2  | ECCD1 | ECCD0 |
|                     | Read/Write  | R                              |        |        |        |        |        |       |       |
|                     | Reset State | 0                              | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
| (08C5H)             | Function    | NAND Flash ECC Register (7-0)  |        |        |        |        |        |       |       |
|                     |             | 15                             | 14     | 13     | 12     | 11     | 10     | 9     | 8     |
|                     | bit Symbol  | ECCD15                         | ECCD14 | ECCD13 | ECCD12 | ECCD11 | ECCD10 | ECCD9 | ECCD8 |
|                     | Read/Write  | R                              |        |        |        |        |        |       |       |
| (08C5H)             | Reset State | 0                              | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|                     | Function    | NAND Flash ECC Register (15-8) |        |        |        |        |        |       |       |

NAND Flash ECC Register 1

|                     |             |                                |        |        |        |        |        |       |       |
|---------------------|-------------|--------------------------------|--------|--------|--------|--------|--------|-------|-------|
| NDECCRD1<br>(08C6H) |             | 7                              | 6      | 5      | 4      | 3      | 2      | 1     | 0     |
|                     | bit Symbol  | ECCD7                          | ECCD6  | ECCD5  | ECCD4  | ECCD3  | ECCD2  | ECCD1 | ECCD0 |
|                     | Read/Write  | R                              |        |        |        |        |        |       |       |
|                     | Reset State | 0                              | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
| (08C7H)             | Function    | NAND Flash ECC Register (7-0)  |        |        |        |        |        |       |       |
|                     |             | 15                             | 14     | 13     | 12     | 11     | 10     | 9     | 8     |
|                     | bit Symbol  | ECCD15                         | ECCD14 | ECCD13 | ECCD12 | ECCD11 | ECCD10 | ECCD9 | ECCD8 |
|                     | Read/Write  | R                              |        |        |        |        |        |       |       |
| (08C7H)             | Reset State | 0                              | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|                     | Function    | NAND Flash ECC Register (15-8) |        |        |        |        |        |       |       |

NAND Flash ECC Register 2

|                     |             |                                |        |        |        |        |        |       |       |
|---------------------|-------------|--------------------------------|--------|--------|--------|--------|--------|-------|-------|
| NDECCRD2<br>(08C8H) |             | 7                              | 6      | 5      | 4      | 3      | 2      | 1     | 0     |
|                     | bit Symbol  | ECCD7                          | ECCD6  | ECCD5  | ECCD4  | ECCD3  | ECCD2  | ECCD1 | ECCD0 |
|                     | Read/Write  | R                              |        |        |        |        |        |       |       |
|                     | Reset State | 0                              | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
| (08C9H)             | Function    | NAND Flash ECC Register (7-0)  |        |        |        |        |        |       |       |
|                     |             | 15                             | 14     | 13     | 12     | 11     | 10     | 9     | 8     |
|                     | bit Symbol  | ECCD15                         | ECCD14 | ECCD13 | ECCD12 | ECCD11 | ECCD10 | ECCD9 | ECCD8 |
|                     | Read/Write  | R                              |        |        |        |        |        |       |       |
| (08C9H)             | Reset State | 0                              | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|                     | Function    | NAND Flash ECC Register (15-8) |        |        |        |        |        |       |       |

NAND Flash ECC Register 3

|                     |             |                                |        |        |        |        |        |       |       |
|---------------------|-------------|--------------------------------|--------|--------|--------|--------|--------|-------|-------|
| NDECCRD3<br>(08CAH) |             | 7                              | 6      | 5      | 4      | 3      | 2      | 1     | 0     |
|                     | bit Symbol  | ECCD7                          | ECCD6  | ECCD5  | ECCD4  | ECCD3  | ECCD2  | ECCD1 | ECCD0 |
|                     | Read/Write  | R                              |        |        |        |        |        |       |       |
|                     | Reset State | 0                              | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
| (08CBH)             | Function    | NAND Flash ECC Register (7-0)  |        |        |        |        |        |       |       |
|                     |             | 15                             | 14     | 13     | 12     | 11     | 10     | 9     | 8     |
|                     | bit Symbol  | ECCD15                         | ECCD14 | ECCD13 | ECCD12 | ECCD11 | ECCD10 | ECCD9 | ECCD8 |
|                     | Read/Write  | R                              |        |        |        |        |        |       |       |
| (08CBH)             | Reset State | 0                              | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|                     | Function    | NAND Flash ECC Register (15-8) |        |        |        |        |        |       |       |



| NAND Flash ECC Register 4 |             |                                |        |        |        |        |        |       |       |
|---------------------------|-------------|--------------------------------|--------|--------|--------|--------|--------|-------|-------|
| NDECCRD4<br>(08CCH)       |             | 7                              | 6      | 5      | 4      | 3      | 2      | 1     | 0     |
|                           | bit Symbol  | ECCD7                          | ECCD6  | ECCD5  | ECCD4  | ECCD3  | ECCD2  | ECCD1 | ECCD0 |
|                           | Read/Write  | R                              |        |        |        |        |        |       |       |
|                           | Reset State | 0                              | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|                           | Function    | NAND Flash ECC Register (7-0)  |        |        |        |        |        |       |       |
| (08CDH)                   |             | 15                             | 14     | 13     | 12     | 11     | 10     | 9     | 8     |
|                           | bit Symbol  | ECCD15                         | ECCD14 | ECCD13 | ECCD12 | ECCD11 | ECCD10 | ECCD9 | ECCD8 |
|                           | Read/Write  | R                              |        |        |        |        |        |       |       |
|                           | Reset State | 0                              | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|                           | Function    | NAND Flash ECC Register (15-8) |        |        |        |        |        |       |       |

Figure3.11.7 NAND Flash ECC Registers

The NAND Flash ECC register is used to read ECC generated by the ECC generator.

After valid data has been written to or read from the NAND Flash, setting NDFMCR0<ECCE> to “0” causes the corresponding ECC to be set in this register. (The ECC in this register is updated when NDFMCR0<ECCE> changes from “1” to “0”.)

When Hamming codes are used, 22 bits of ECC are generated for up to 256 bytes of valid data. In the case of Reed-Solomon codes, 80 bits of ECC are generated for up to 518 bytes of valid data. A total of 80 bits of registers are provided, arranged as five 16-bit registers. These registers must be read in 16-bit units and cannot be accessed in 32-bit units.

After ECC calculation has completed, in the case of Hamming codes, the 16-bit line parity for the first 256 bytes is stored in the NDECCRD0 register, the 6-bit column parity for the first 256 bytes in the NDECCRD1 register (<ECCE7:2>), the 16-bit line parity for the second 256 bytes in the NDECCRD2 register, and the 6-bit column parity for the second 256 bytes in the NDECCRD3 register (<ECCD7:2>). In this case, the NDECCRD4 register is not used.

In the case of Reed-Solomon codes, 80 bits of ECC are stored in the NDECCRD0, NDECCRD1, NDECCRD2, NDECCRD3 and NDECCRD4 registers.

Note: Before reading ECC from the NAND Flash ECC register, be sure to set NDFMCR0<ECCE> to “0”. The ECC in the NAND Flash ECC register is updated when NDFMCR0<ECCE> changes from “1” to “0”. Also note that when the ECC in the ECC generator is reset by NDFMCR0<ECCRST>, the contents of this register are not reset.

| Register Name | Hamming                                           | Reed-Solomon                          |
|---------------|---------------------------------------------------|---------------------------------------|
| NDECCRD0      | [15:0] Line parity<br>(for the first 256 bytes)   | [15:0]<br>Reed-Solomon ECC code 79:64 |
| NDECCRD1      | [7:2] Column parity<br>(for the first 256 bytes)  | [15:0]<br>Reed-Solomon ECC code 63:48 |
| NDECCRD2      | [15:0] Line parity<br>(for the second 256 bytes)  | [15:0]<br>Reed-Solomon ECC code 47:32 |
| NDECCRD3      | [7:2] Column parity<br>(for the second 256 bytes) | [15:0]<br>Reed-Solomon ECC code 31:16 |
| NDECCRD4      | Not in use                                        | [15:0]<br>Reed-Solomon ECC code 15:0  |

The table below shows an example of how ECC is written to the redundant area in the NAND Flash memory when using Reed-Solomon codes.

When using Hamming codes with SmartMedia™, the addresses of the redundant area are specified by the physical format of SmartMedia™. For details, refer to the SmartMedia™ Physical Format Specifications.

| Register Name | Reed-Solomon                          | NAND Flash Address                                                       |
|---------------|---------------------------------------|--------------------------------------------------------------------------|
| NDECCRD0      | [15:0]<br>Reed-Solomon ECC code 79:64 | Upper 8 bits [79:72] → address 518<br>Lower 8 bits [71:64] → address 519 |
| NDECCRD1      | [15:0]<br>Reed-Solomon ECC code 63:48 | Upper 8 bits [63:56] → address 520<br>Upper 8 bits [55:48] → address 521 |
| NDECCRD2      | [15:0]<br>Reed-Solomon ECC code 47:32 | Upper 8 bits [47:40] → address 522<br>Lower 8 bits [39:32] → address 523 |
| NDECCRD3      | [15:0]<br>Reed-Solomon ECC code 31:16 | Upper 8 bits [31:24] → address 524<br>Lower 8 bits [23:16] → address 525 |
| NDECCRD4      | [15:0]<br>Reed-Solomon ECC code 15:0  | Upper 8 bits [15:8] → address 526<br>Lower 8 bits [7:0] → address 527    |

| NAND Flash Reed-Solomon Calculation Result Address Register |             |                                                                   |       |       |       |       |       |                                                                   |       |  |
|-------------------------------------------------------------|-------------|-------------------------------------------------------------------|-------|-------|-------|-------|-------|-------------------------------------------------------------------|-------|--|
| NDRSCA0<br>(08D0H)                                          |             | 7                                                                 | 6     | 5     | 4     | 3     | 2     | 1                                                                 | 0     |  |
|                                                             | bit Symbol  | RS0A7                                                             | RS0A6 | RS0A5 | RS0A4 | RS0A3 | RS0A2 | RS0A1                                                             | RS0A0 |  |
|                                                             | Read/Write  | R                                                                 |       |       |       |       |       |                                                                   |       |  |
|                                                             | Reset State | 0                                                                 | 0     | 0     | 0     | 0     | 0     | 0                                                                 | 0     |  |
| (08D1H)                                                     | Function    | NAND Flash Reed-Solomon Calculation Result Address Register (7-0) |       |       |       |       |       |                                                                   |       |  |
|                                                             |             | 15                                                                | 14    | 13    | 12    | 11    | 10    | 9                                                                 | 8     |  |
|                                                             | bit Symbol  |                                                                   |       |       |       |       |       | RS0A9                                                             | RS0A8 |  |
|                                                             | Read/Write  |                                                                   |       |       |       |       |       | R                                                                 |       |  |
| NDRSCA1<br>(08D4H)                                          | Reset State |                                                                   |       |       |       |       |       | 0                                                                 | 0     |  |
|                                                             | Function    |                                                                   |       |       |       |       |       | NAND Flash Reed-Solomon Calculation Result Address Register (9-8) |       |  |
|                                                             |             | 7                                                                 | 6     | 5     | 4     | 3     | 2     | 1                                                                 | 0     |  |
|                                                             | bit Symbol  | RS1A7                                                             | RS1A6 | RS1A5 | RS1A4 | RS1A3 | RS1A2 | RS1A1                                                             | RS1A0 |  |
| (08D5H)                                                     | Read/Write  | R                                                                 |       |       |       |       |       |                                                                   |       |  |
|                                                             | Reset State | 0                                                                 | 0     | 0     | 0     | 0     | 0     | 0                                                                 | 0     |  |
|                                                             | Function    | NAND Flash Reed-Solomon Calculation Result Address Register (7-0) |       |       |       |       |       |                                                                   |       |  |
|                                                             |             | 15                                                                | 14    | 13    | 12    | 11    | 10    | 9                                                                 | 8     |  |
| NDRSCA2<br>(08D8H)                                          | bit Symbol  |                                                                   |       |       |       |       |       | RS1A9                                                             | RS1A8 |  |
|                                                             | Read/Write  |                                                                   |       |       |       |       |       | R                                                                 |       |  |
|                                                             | Reset State |                                                                   |       |       |       |       |       | 0                                                                 | 0     |  |
|                                                             | Function    |                                                                   |       |       |       |       |       | NAND Flash Reed-Solomon Calculation Result Address Register (9-8) |       |  |
| (08D9H)                                                     |             | 7                                                                 | 6     | 5     | 4     | 3     | 2     | 1                                                                 | 0     |  |
|                                                             | bit Symbol  | RS2A7                                                             | RS2A6 | RS2A5 | RS2A4 | RS2A3 | RS2A2 | RS2A1                                                             | RS2A0 |  |
|                                                             | Read/Write  | R                                                                 |       |       |       |       |       |                                                                   |       |  |
|                                                             | Reset State | 0                                                                 | 0     | 0     | 0     | 0     | 0     | 0                                                                 | 0     |  |
| NDRSCA3<br>(08DCH)                                          | Function    | NAND Flash Reed-Solomon Calculation Result Address Register (7-0) |       |       |       |       |       |                                                                   |       |  |
|                                                             |             | 15                                                                | 14    | 13    | 12    | 11    | 10    | 9                                                                 | 8     |  |
|                                                             | bit Symbol  |                                                                   |       |       |       |       |       | RS2A9                                                             | RS2A8 |  |
|                                                             | Read/Write  |                                                                   |       |       |       |       |       | R                                                                 |       |  |
| (08DDH)                                                     | Reset State |                                                                   |       |       |       |       |       | 0                                                                 | 0     |  |
|                                                             | Function    |                                                                   |       |       |       |       |       | NAND Flash Reed-Solomon Calculation Result Address Register (9-8) |       |  |
|                                                             |             | 7                                                                 | 6     | 5     | 4     | 3     | 2     | 1                                                                 | 0     |  |
|                                                             | bit Symbol  | RS3A7                                                             | RS3A6 | RS3A5 | RS3A4 | RS3A3 | RS3A2 | RS3A1                                                             | RS3A0 |  |
| (08DDH)                                                     | Read/Write  | R                                                                 |       |       |       |       |       |                                                                   |       |  |
|                                                             | Reset State | 0                                                                 | 0     | 0     | 0     | 0     | 0     | 0                                                                 | 0     |  |
|                                                             | Function    | NAND Flash Reed-Solomon Calculation Result Address Register (7-0) |       |       |       |       |       |                                                                   |       |  |
|                                                             |             | 15                                                                | 14    | 13    | 12    | 11    | 10    | 9                                                                 | 8     |  |
| (08DDH)                                                     | bit Symbol  |                                                                   |       |       |       |       |       | RS3A9                                                             | RS3A8 |  |
|                                                             | Read/Write  |                                                                   |       |       |       |       |       | R                                                                 |       |  |
|                                                             | Reset State |                                                                   |       |       |       |       |       | 0                                                                 | 0     |  |
|                                                             | Function    |                                                                   |       |       |       |       |       | NAND Flash Reed-Solomon Calculation Result Address Register (9-8) |       |  |

Figure3.11.8 NAND Flash Reed-Solomon Calculation Result Address Register

If error is found at only one address, the error address is stored in the NDRSCA0 register. If error is found at two addresses, the NDRSCA0 and NDRSCA1 registers are used to store the error addresses. In this manner, up to four error addresses can be stored in the NDRSCA0 to NDRSCA3 registers.

The number of error addresses can be checked by NDFMCR1<SEER1:0>.

| NAND Flash Reed-Solomon Calculation Result Data Register |             |                                                                |       |       |       |       |       |       |       |
|----------------------------------------------------------|-------------|----------------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| NDRSCD0<br>(08D2H)                                       |             | 7                                                              | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|                                                          | bit Symbol  | RS0D7                                                          | RS0D6 | RS0D5 | RS0D4 | RS0D3 | RS0D2 | RS0D1 | RS0D0 |
|                                                          | Read/Write  | R                                                              |       |       |       |       |       |       |       |
|                                                          | Reset State | 0                                                              | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
|                                                          | Function    | NAND Flash Reed-Solomon Calculation Result Data Register (7-0) |       |       |       |       |       |       |       |
| NDRSCD1<br>(08D6H)                                       |             | 7                                                              | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|                                                          | bit Symbol  | RS1D7                                                          | RS1D6 | RS1D5 | RS1D4 | RS1D3 | RS1D2 | RS1D1 | RS1D0 |
|                                                          | Read/Write  | R                                                              |       |       |       |       |       |       |       |
|                                                          | Reset State | 0                                                              | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
|                                                          | Function    | NAND Flash Reed-Solomon Calculation Result Data Register (7-0) |       |       |       |       |       |       |       |
| NDRSCD2<br>(08DAH)                                       |             | 7                                                              | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|                                                          | bit Symbol  | RS2D7                                                          | RS2D6 | RS2D5 | RS2D4 | RS2D3 | RS2D2 | RS2D1 | RS2D0 |
|                                                          | Read/Write  | R                                                              |       |       |       |       |       |       |       |
|                                                          | Reset State | 0                                                              | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
|                                                          | Function    | NAND Flash Reed-Solomon Calculation Result Data Register (7-0) |       |       |       |       |       |       |       |
| NDRSCD3<br>(08DEH)                                       |             | 7                                                              | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|                                                          | bit Symbol  | RS3D7                                                          | RS3D6 | RS3D5 | RS3D4 | RS3D3 | RS3D2 | RS3D1 | RS3D0 |
|                                                          | Read/Write  | R                                                              |       |       |       |       |       |       |       |
|                                                          | Reset State | 0                                                              | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
|                                                          | Function    | NAND Flash Reed-Solomon Calculation Result Data Register (7-0) |       |       |       |       |       |       |       |

Figure3.11.9 NAND Flash Reed-Solomon Calculation Result Data Register

If error is found at only one address, the error data is stored in the NDRSCD0 register. If error is found at two addresses, the NDRSCD0 and NDRSCD1 registers are used to store the error data. In this manner, the error data at up to four addresses can be stored in the NDRSCD0 to NDRSCD3 registers.

The number of error addresses can be checked by NDFMCR1<SEER1:0>.

### 3.11.6 An Example of Accessing NAND Flash of SLC Type

#### 1. Initialization

```
;
; ***** Initialize NDFC *****
;      Conditions: 8-bit bus, CE0, SLC, 512 (528) bytes/page, Hamming codes
;
;      ld      (ndfmcrl),0001h ; 8-bit bus, Hamming ECC, SYSCK-ON
;      ld      (ndfmcrl),2000h ; SPLW1:0=0, SPHW1:0=2
```

#### 2. Write

Writing valid data

```
; ***** Write valid data*****
;
;      ldw     (ndfmcrl),2010h ; CE0 enable
;      ldw     (ndfmcrl),20B0h ; WE enable, CLE enable
;      ld      (ndfdtr0),80h   ; Serial input command
;      ldw     (ndfmcrl),20D0h ; ALE enable
;      ld      (ndfdtr0),xxh   ; Address write (3 or 4 times)
;      ldw     (ndfmcrl),2095h ; Reset ECC, ECCE enable, CE0 enable
;      ld      (ndfdtr0),xxh   ; Data write (512 times)
```

Generating ECC → Reading ECC

```
; ***** Read ECC *****
;
;      ldw     (ndfmcrl),2010h ; ECC circuit disable
;
;      ldw     xxxx,(ndecrdr0) ; Read ECC from internal circuit
;      1'st Read: D15-0 > LPR15:0 For first 256 bytes
;      ldw     xxxx,(ndecrdr1) ; Read ECC from internal circuit
;      2'nd Read: D15-0 > FFh+CPR5:0+11b For first 256 bytes
;      ldw     xxxx,(ndecrdr0) ; Read ECC from internal circuit
;      3'rd Read: D15-0 > LPR15:0 For second 256 bytes
;      ldw     xxxx,(ndecrdr1) ; Read ECC from internal circuit
;      4'th Read: D15-0 > FFh+CPR5:0+11b For second 256 bytes
```

Writing ECC to NAND Flash

```
; ***** Write dummy data & ECC*****
;
;      ldw     (ndfmcrl),2090h ; ECC circuit disable, data write mode
;      ld      (ndfdtr0),xxh   ; Redundancy area data write (16 times)
;      Write to D520: LPR7:0 > D7-0 For second 256 bytes
;      Write to D521: LPR15:8 > D7-0 For second 256 bytes
;      Write to D522: CPR5:0+11b > D7-0 For second 256 bytes
;      Write to D525: LPR7:0 > D7-0 For first 256 bytes
;      Write to D526: LPR15:8 > D7-0 For first 256 bytes
;      Write to D527: CPR5:0+11b > D7-0 For first 256 bytes
```

## Executing page program

; \*\*\*\*\* Set auto page program\*\*\*\*\*

;

ldw (ndfmcr0),20B0h ; WE enable, CLE enable

ld (ndfdtr0),10h ; Auto page program command

ldw (ndfmcr0),2010h ; WE disable, CLE disable

;

; Wait setup time (from Busy to Ready)

;

1. Flag polling

;

2. Interrupt

;

## Reading status

; \*\*\*\*\* Read Status\*\*\*\*\*

;

ldw (ndfmcr0),20B0h ; WE enable, CLE enable

ld (ndfdtr0),70h ; Status read command

ldw (ndfmcr0),2010h ; WE disable, CLE disable

ld xx,(ndfdtr0) ; Status read

## 3. Read

## Reading valid data

; \*\*\*\*\* Read valid data\*\*\*\*\*

;

```

ldw    (ndfmc0),2010h ; CE0 enable
ldw    (ndfmc0),20B0h ; WE enable, CLE enable
ld      (ndfdtr0),00h  ; Read command
ldw    (ndfmc0),20D0h ; ALE enable
ld      (ndfdtr0),xxh  ; Address write (3 or 4 times)

```

;

;

Wait setup time (from Busy to Ready)

;

1. Flag polling

;

2. Interrupt

;

```

ldw    (ndfmc0),2015h ; Reset ECC, ECCE enable, CE0 enable
ld      xx,(ndfdtr0)   ; Data read (512 times)
ldw    (ndfmc0),2010h ; ECC circuit disable
ld      xx,(ndfdtr0)   ; Redundancy data read (8 times)
ld      xx,(ndfdtr0)   ; ECC data read (3 times)
ld      xx,(ndfdtr0)   ; Redundancy data read (2 times)
ld      xx,(ndfdtr0)   ; ECC data read (3 times)

```

## Generating ECC → Reading ECC

; \*\*\*\*\* Read ECC \*\*\*\*\*

;

```

ldw    (ndfmc0),2010h ; ECC circuit disable
ldw    xxxx,(ndeccrd0) ; Read ECC from internal circuit
;      1'st Read:      D15-0 > LPR15:0          For first 256 bytes
ldw    xxxx,(ndeccrd1) ; Read ECC from internal circuit
;      2'nd Read:      D15-0 > FFh+CPR5:0+11b For first 256 bytes
ldw    xxxx,(ndeccrd0) ; Read ECC from internal circuit
;      3'rd Read:      D15-0 > LPR15:0          For second 256 bytes
ldw    xxxx,(ndeccrd1) ; Read ECC from internal circuit
;      4'th Read:      D15-0 > FFh+CPR5:0+11b For second 256 bytes

```

## Software processing

The ECC data generated for the read operation and the ECC in the redundant area in the NAND Flash are compared. If any error is found, the error processing routine is performed to correct the error data. For details, see 3.11.4.2 “Error Correction Methods”.

## 4. ID Read

The ID read routine is as follows:

```
ldw    (ndfmc0),20B0h ; WE Enable, CLE enable
ld      (ndfdtr0),90h  ; Write ID read command
ldw    (ndfmc0),20D0h ; ALE enable, CLE disable
ld      (ndfdtr0),00h  ; Write 00
ldw    (ndfmc0),2010h ; WE disable, CLE disable
ld      xx,(ndfdtr0)   ; Read 1'st ID maker code
ld      xx,(ndfdtr0)   ; Read 2'nd ID device code
```



### 3.11.7 An Example of Accessing NAND Flash of MLC Type (When the valid data is processed as 518byte)

#### 1. Initialization

```
;
; ***** Initialize NDFC *****
;      Conditions: 16-bit bus, CE1, MLC, 2048 (2112) bytes/page, Reed-Solomon codes
;
;      ld      (ndfmcr1),0007h ; 16-bit bus, Reed-Solomon ECC, SYSCK-ON
;      ld      (ndfmcr0),5000h ; SPLW1:0=1, SPHW1:0=1
```

#### 2. Write

Writing valid data

```
; ***** Write valid data*****
;
;      ldw     (ndfmcr0),5008h ; CE1 enable
;      ldw     (ndfmcr0),50A8h ; WE enable, CLE enable
;      ldw     (ndfdtr0),0080h ; serial input command
;      ldw     (ndfmcr0),50C8h ; ALE enable
;      ldw     (ndfdtr0),00xxh ; Address write ( 4 or 5 times)
;      ldw     (ndfmcr0),508Dh ; Reset ECC code, ECCE enable
;      ldw     (ndfdtr0),xxxxh ; Data write (259-times/:518byte)
;                               (256-times/512byte)
```

Generating ECC → Reading ECC

```
; ***** Read ECC *****
;
;      ldw     (ndfmcr0),5008h ; ECC circuit disable
;      ldw     (ndfmcr0),50A8h ; WE enable, CLE enable
;      ldw     (ndfdtr0),0080h ; serial input command
;      ldw     (ndfmcr0),50C8h ; ALE enable
;      ldw     (ndfdtr0),00xxh ; Address write ( 4 or 5 times)
;
;      ldw     xxxx,(ndeccrd0) ; Read ECC from internal circuit
;      Read:   D79-64
;      ldw     xxxx,(ndeccrd1) ; Read ECC from internal circuit
;      Read:   D63-48
;      ldw     xxxx,(ndeccrd2) ; Read ECC from internal circuit
;      Read:   D47-32
;      ldw     xxxx,(ndeccrd3) ; Read ECC from internal circuit
;      Read:   D31-16
;      ldw     xxxx,(ndeccrd4) ; Read ECC from internal circuit
;      Read:   D15-0
```

## Writing ECC to NAND Flash

; \*\*\*\*\* Write dummy data &amp; ECC \*\*\*\*\*

;

ldw (ndfmcr0),5088h ; ECC circuit disable, data write mode

ldw (ndfdtr0),xxxxh ; Redundancy area data write

; Write to 207-206hex address: &gt; D79-64

ldw (ndfdtr1),xxxxh ; Redundancy area data write

; Write to 209-208hex address: &gt; D63-48

ldw (ndfdtr0),xxxxh ; Redundancy area data write

; Write to 20B-20Ahex address: &gt; D47-32

ldw (ndfdtr1),xxxxh ; Redundancy area data write

; Write to 20D-20Chex address: &gt; D31-16

ldw (ndfdtr0),xxxxh ; Redundancy area data write

; Write to 20F-20Ehex address: &gt; D15-0

;

; The write operation is repeated four times to write 2112 bytes.

## Executing page program

; \*\*\*\*\* Set auto page program\*\*\*\*\*

;

ldw (ndfmcr0),50A8h ; WE enable, CLE enable

ldw (ndfdtr0),0010h ; Auto page program command

ldw (ndfmcr0),5008h ; WE disable, CLE disable

;

; Wait set up time (from Busy to Ready)

; 1. Flag polling

; 2. Interrupt

Note: In case of LB type NANDF, programming page size is normally each 2112 bytes and ECC calculation is processed each 518 (512) bytes. Please take care of programming flow. In details, refer the NANDF memory specifications.

## Reading status

; \*\*\*\*\* Read status\*\*\*\*\*

;

ldw (ndfmcr0),50A8h ; WE enable, CLE enable

ldw (ndfdtr0),0070h ; Status read command

ldw (ndfmcr0),5008h ; WE disable, CLE disable

ldw xxxx,(ndfdtr0) ; Status read

## 3. Read (including ECC data read)

## Reading valid data

; \*\*\*\*\* Read valid data\*\*\*\*\*

;

```
ldw      (ndfmcr0),5008h ; CE1 enable
ldw      (ndfmcr0),50A8h ; WE enable, CLE enable
ldw      (ndfdtr0),0000h ; Read command 1
ldw      (ndfmcr0),50C8h ; ALE enable
ldw      (ndfdtr0),00xxh ; Address write (4 or 5 times)
ldw      (ndfmcr0),50A8h ; WE enable, CLE enable
ldw      (ndfdtr0),0030h ; Read command 2
```

;

; Wait set up time (from Busy to Ready)

;

1. Flag polling

;

2. Interrupt

;

```
ldw      (ndfmcr0),540Dh ; ECC reset, ECC circuit enable, decode mode
ldw      xxxx,(ndfdtr0)   ; Data read (259 times: 518 bytes)
                                (256-times:512 byte)
```

```
ldw      (ndfmcr0),550Ch ; RSECGW enable
ldw      xxxx,(ndfdtr0)   ; Read ECC (5 times: 80 bits)
```

;

; Wait set up time (20 system clocks)

;

## (1) Error bit calculation

```
ldw      (ndfmcr1),0047h ; Error bit calculation interrupt enable
ldw      (ndfmcr0),560Ch ; Error bit calculation circuit start
```

;

; Wait set up time

;

; Interrupt routine (End of calculation for Reed-Solomon Error bit)

;

INT: ldw xxxx,(ndfmcr1) ; Check error status "STATE3:0, SEER1:0"

;

```
; If error is found, the error processing routine is performed to
; correct the error data. For details see 3.11.4.2 "Error Correction
; Methods".
```

;

; The read operation is repeated four times to read 2112 bytes.

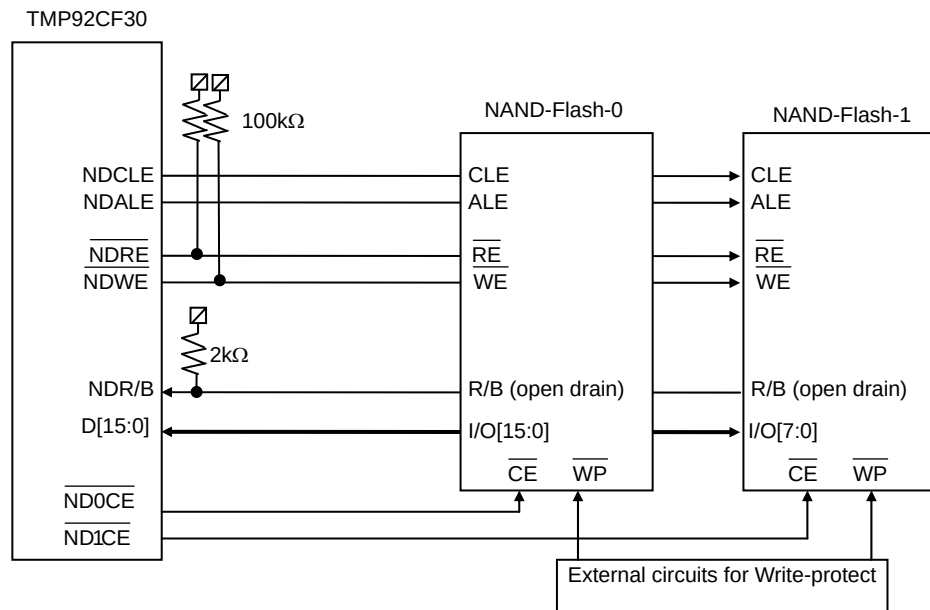
;

## 4. ID Read

The ID read routine is as follows:

```
ldw      (ndfmc0),50A8h ; WE enable, CLE enable
ldw      (ndfdtr0),0090h ; Write ID read command
ldw      (ndfmc0),50C8h ; ALE enable, CLE disable
ldw      (ndfdtr0),0000h ; Write 00
ldw      (ndfmc0),5008h ; WE disable, CLE disable
ldw      xxxx,(ndfdtr0)  ; Read 1'st ID maker code
ldw      xxxx,(ndfdtr1)  ; Read 2'ndID device code
```

## 3.11.8 An Example of Connections with NAND Flash



Note 1: A reset sets the  $\overline{\text{NDRE}}$  and  $\overline{\text{NDWE}}$  pins as input ports, so pull-up resistors are needed.

Note 2: The pull-up resistor value for the NDR/B pin must be set appropriately according to the NAND Flash memory to be used and the capacity of the board (typical: 2 k $\Omega$ ).

Note 3: The  $\overline{\text{WP}}$  (Write Protect) pin of NAND Flash is not supported. When this function is needed, prepare it on an external circuit.

Figure3.11.10 An Example of Connections with NAND Flash

### 3.12 8 Bit Timer (TMRA)

The TMP92CF30 features 8 channel built-in 8-bit timers (TMRA0 to TMRA7).

These timers are paired into 4 modules: TMRA01, TMRA23, TMRA45 and TMRA67. Each module consists of 2 channels and can operate in any of the following 4 operating modes.

- 8-bit interval timer mode
- 16-bit interval timer mode
- 8-bit programmable square wave pulse generation output mode (PPG: Variable duty cycle with variable period)
- 8-bit pulse width modulation output mode (PWM – Variable duty cycle with constant period)

Figure 3.12.1 to Figure 3.12.4 show block diagrams for TMRA01 to TMRA67.

Each channel consists of an 8-bit up counter, an 8-bit comparator and an 8-bit timer register. In addition, a timer flip-flop and a prescaler are provided for each pair of channels.

The operation mode and timer flip-flops are controlled by a 5bytes registers SFRs (Special-function registers).

Each of the 4 modules (TMRA01 to TMRA67) can be operated independently. All modules operate in the same manner; hence only the operation of TMRA01 is explained here.

The contents of this chapter are as follows.

Table 3.12.1 Registers and Pins for Each Module

| Module           |                                  | TMRA01                           | TMRA23                           | TMRA45                           | TMRA67                           |
|------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| Specification    |                                  |                                  |                                  |                                  |                                  |
| External pin     | Input pin for external clock     | TA0IN<br>(Shared with PC1)       | TA2IN<br>(Shared with PC3)       | Low-frequency clock<br>fs        | Low-frequency clock<br>fs        |
|                  | Output pin for timer flip-flop   | TA1OUT<br>(Shared with PM1)      | –                                | –                                | TA7OUT<br>(Shared with PP3)      |
| SFR<br>(Address) | Timer run register               | TA01RUN (1100H)                  | TA23RUN (1108H)                  | TA45RUN (1110H)                  | TA67RUN (1118H)                  |
|                  | Timer register                   | TA0REG (1102H)<br>TA1REG (1103H) | TA2REG (110AH)<br>TA3REG (110BH) | TA4REG (1112H)<br>TA5REG (1113H) | TA6REG (111AH)<br>TA7REG (111BH) |
|                  | Timer mode register              | TA01MOD (1104H)                  | TA23MOD (110CH)                  | TA45MOD (1114H)                  | TA67MOD (111CH)                  |
|                  | Timer flip-flop control register | TA1FFCR (1105H)                  | TA3FFCR (110DH)                  | –                                | TA7FFCR (111DH)                  |

## 3.12.1 Block Diagram

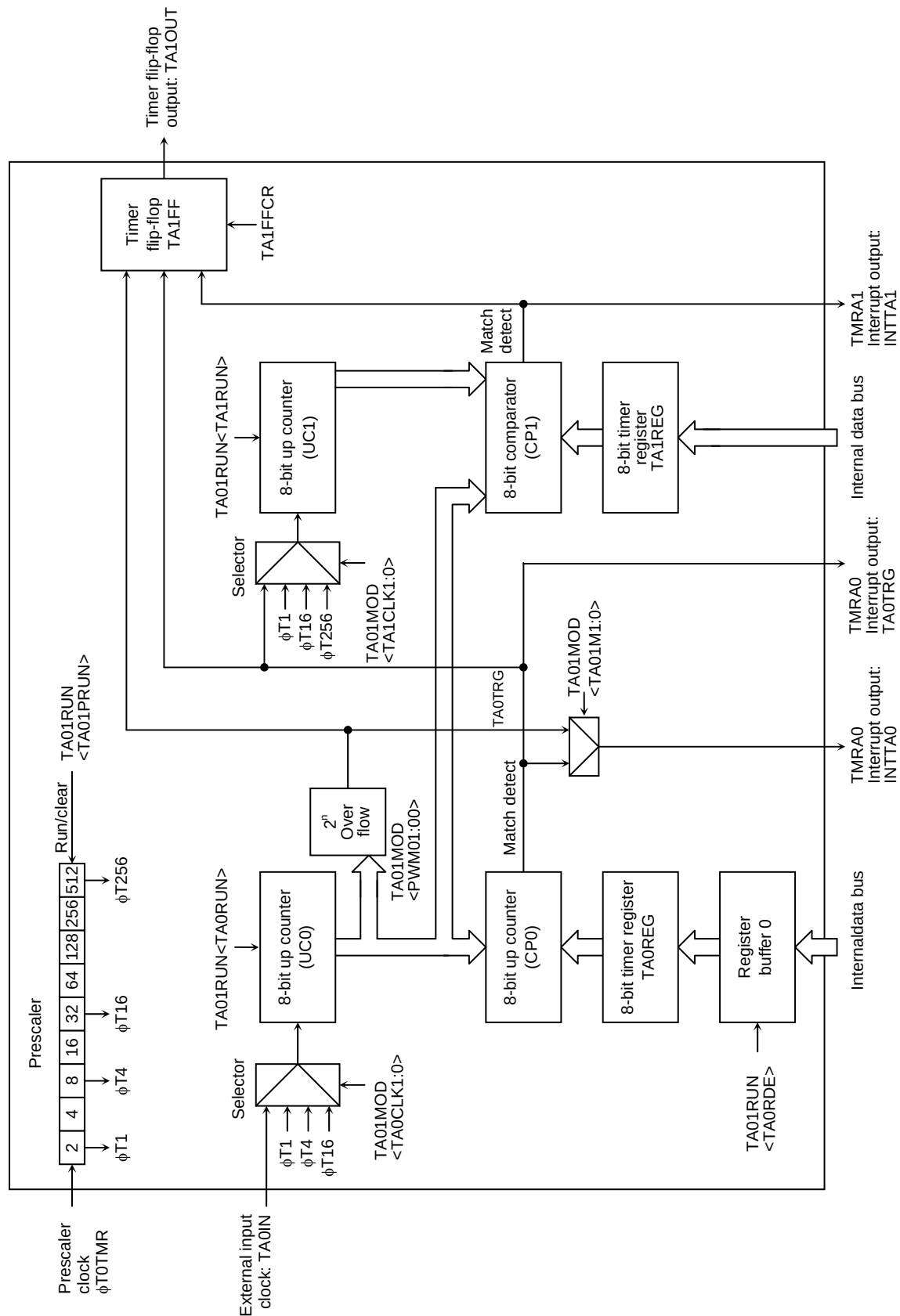


Figure 3.12.1 TMRA01 Block Diagram

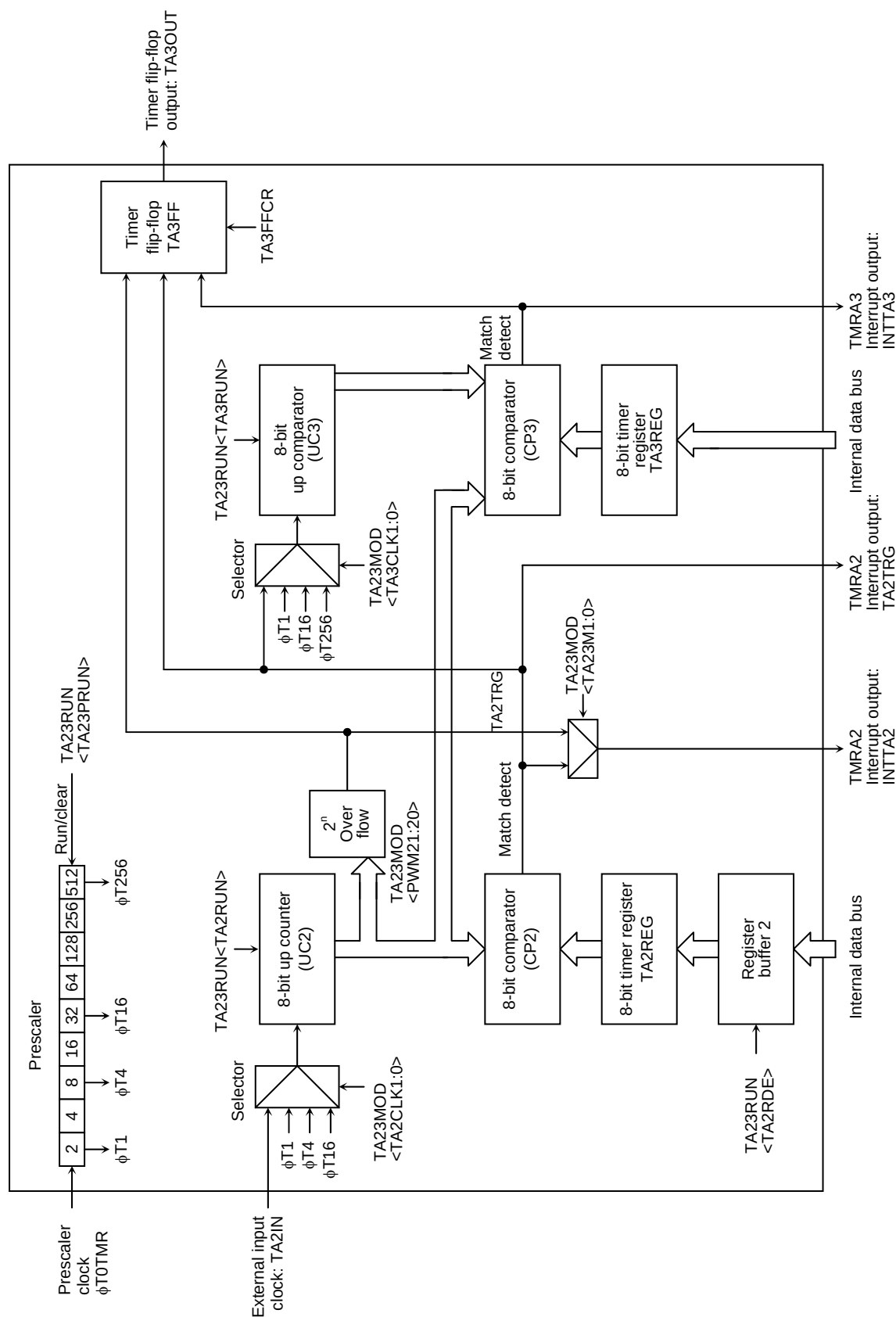


Figure 3.12.2 TMRA23 Block Diagram



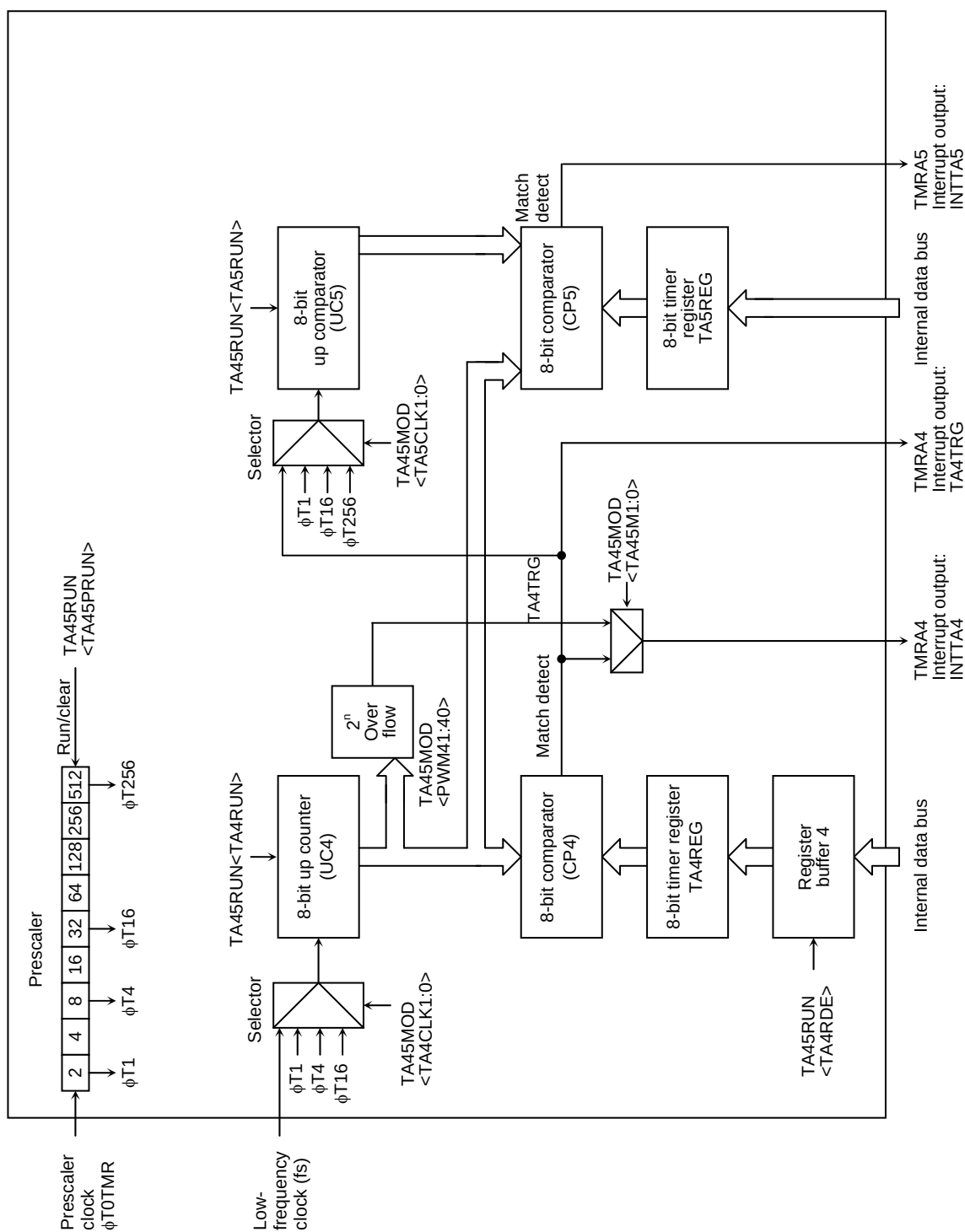


Figure 3.12.3 TMRA45 Block Diagram

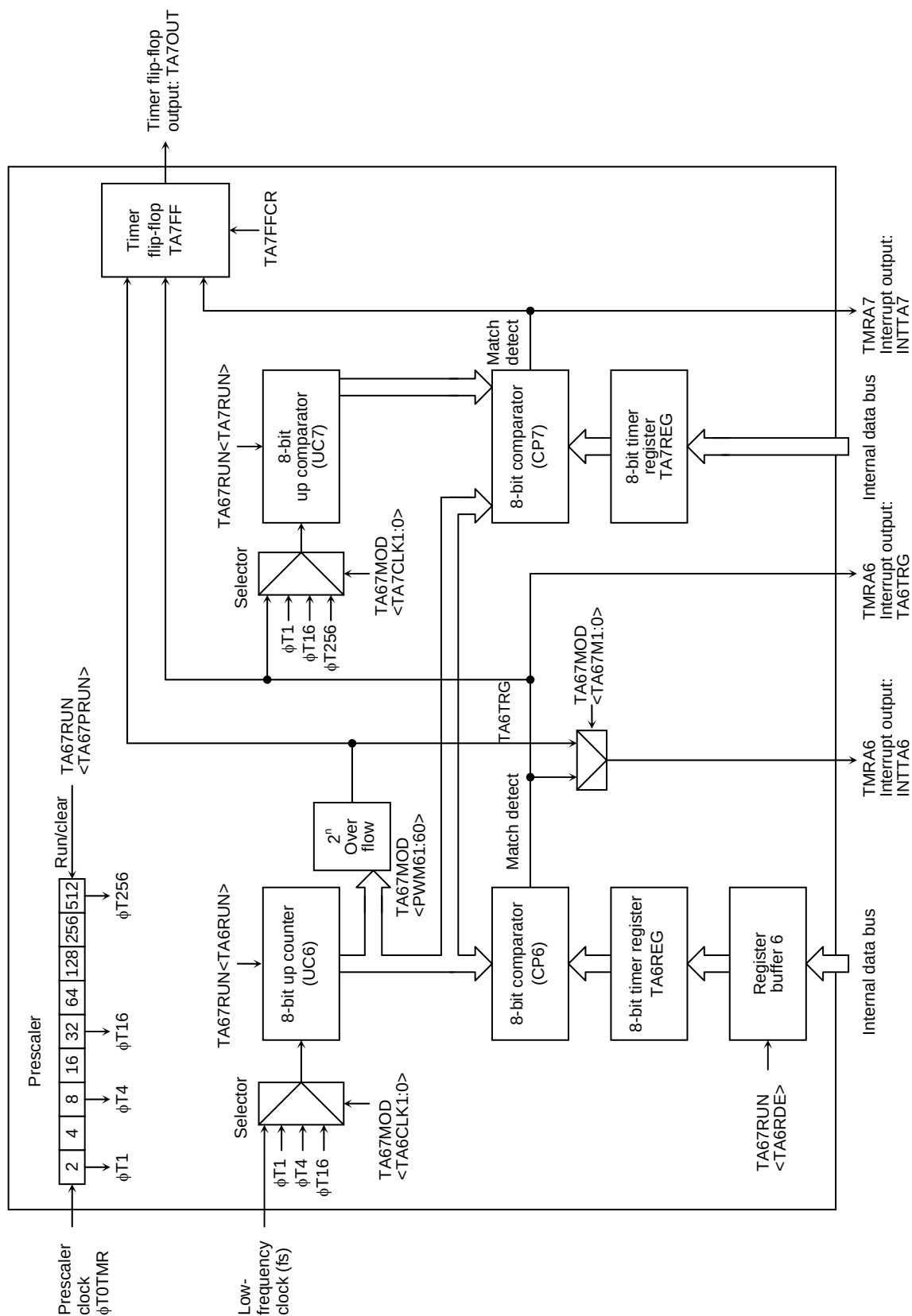


Figure 3.12.4 TMRA67 Block Diagram

### 3.12.2 Operation of Each Circuit

#### (1) Prescaler

A 9-bit prescaler generates the input clock to TMRA01. The clock  $\phi T0TMR$  is selected using the prescaler clock selection register SYSCR0<PRCK>.

The prescaler operation can be controlled using TA01RUN<TA0PRUN> in the timer control register. Setting <TA01PRUN> to “1” starts the count; setting <TA01PRUN> to “0” clears the prescaler to “0” and stops operation. Table 3.12.2 shows the various prescaler output clock resolutions.

(Although the prescaler and the timer counter can be started separately, the timer counter’s operation depends on the prescaler’s input timing.)

Table 3.12.2 Prescaler Output Clock Resolution

|    | Clock gear selection<br>SYSCR1<br><GEAR2:0> | Prescaler of clock gear<br>SYSCR0<br><PRCK> | —   | Timer counter input clock<br>Prescaler of TMRA<br>TAxxMOD<TAxCLK1:0> |          |            |              |
|----|---------------------------------------------|---------------------------------------------|-----|----------------------------------------------------------------------|----------|------------|--------------|
|    |                                             |                                             |     | ϕT1(1/2)                                                             | ϕT4(1/8) | ϕT16(1/32) | ϕT256(1/512) |
| fc | 000(1/1)                                    | 0(1/2)                                      | 1/2 | fc/8                                                                 | fc/32    | fc/128     | fc/2048      |
|    | 001(1/2)                                    |                                             |     | fc/16                                                                | fc/64    | fc/256     | fc/4096      |
|    | 010(1/4)                                    |                                             |     | fc/32                                                                | fc/128   | fc/512     | fc/8192      |
|    | 011(1/8)                                    |                                             |     | fc/64                                                                | fc/256   | fc/1024    | fc/16384     |
|    | 100(1/16)                                   |                                             |     | fc/128                                                               | fc/512   | fc/2048    | fc/32768     |
|    | 000(1/1)                                    | 1(1/8)                                      |     | fc/32                                                                | fc/128   | fc/512     | fc/8192      |
|    | 001(1/2)                                    |                                             |     | fc/64                                                                | fc/256   | fc/1024    | fc/16384     |
|    | 010(1/4)                                    |                                             |     | fc/128                                                               | fc/512   | fc/2048    | fc/32768     |
|    | 011(1/8)                                    |                                             |     | fc/256                                                               | fc/1024  | fc/4096    | fc/65536     |
|    | 100(1/16)                                   |                                             |     | fc/512                                                               | fc/2048  | fc/8192    | fc/131072    |

#### (2) Up counters (UC0 and UC1)

These are 8-bit binary counters which count up the input clock pulses for the clock specified by TA01MOD.

The input clock for UC0 is selectable and can be either the external clock input via the TA0IN pin or one of the three internal clocks  $\phi T1$ ,  $\phi T4$  or  $\phi T16$ . The clock setting is specified by the value set in TA01MOD<TA01CLK1:0>.

The input clock for UC1 depends on the operation mode. In 16-bit timer mode, the overflow output from UC0 is used as the input clock. In any mode other than 16-bit timer mode, the input clock is selectable and can be either be one of the internal clocks  $\phi T1$ ,  $\phi T16$  or  $\phi T256$ , or the comparator output (The match detection signal) from TMRA0.

For each interval timer the timer operation control register bits TA01RUN<TA0RUN> and TA01RUN<TA1RUN> can be used to stop and clear the up counters and to control their count. A reset clears both up counters, stopping the timers.

Note: TMR45 and TMR67 can be selected low-frequency clock(fs) instead of external clock input.

## (3) Timer registers (TA0REG and TA1REG)

These are 8-bit registers, which can be used to set a time interval. When the value set in the timer register TA0REG or TA1REG matches the value in the corresponding up counter, the comparator match detect signal goes active. If the value set in the timer register is 00H, the signal goes active when the up counter overflows.

TA0REG has a double buffer structure, making a pair with the register buffer.

The setting of the bit TA01RUN<TA0RDE> determines whether TA0REG's double buffer structure is enabled or disabled. It is disabled if <TA0RDE> = "0" and enabled if <TA0RDE> = "1".

When the double buffer is enabled, data is transferred from the register buffer to the timer register when a 2<sup>n</sup> overflow occurs in PWM mode, or at the start of the PPG cycle in PPG mode. Hence the double buffer cannot be used in timer mode.

(When using the double buffer, method of renewing timer register is only overflow in PWM mode or frequency agreement in PPG mode.)

A reset initializes <TA0RDE> to "0", disabling the double buffer. To use the double buffer, write data to the timer register, set <TA0RDE> to "1", and write the following data to the register buffer. Figure 3.12.5 shows the configuration of TA0REG.

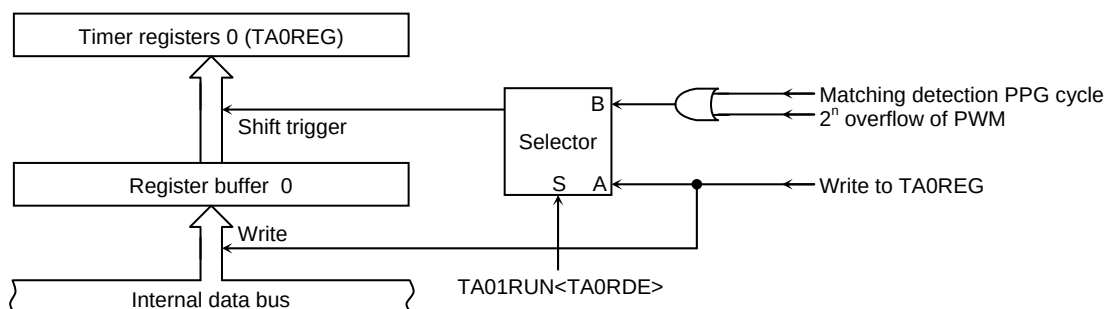


Figure 3.12.5 Configuration of timer register (TA0REG)

Note: The same memory address is allocated to the timer register and the register buffer 0. When <TA0RDE> = "0", the same value is written to the register buffer 0 and the timer register; when <TA0RDE> = "1", only the register buffer 0 is written to.

## (4) Comparator (CP0, CP1)

The comparator compares the value in an up counter with the value set in a timer register. If they match, the up counter is cleared to “0” and an interrupt signal (INTTA0 or INTTA1) is generated. If timer flip-flop inversion is enabled, the timer flip-flop is inverted at the same time.

Note: If a value smaller than the up-counter value is written to the timer register while the timer is counting up, this will cause the timer to overflow and an interrupt cannot be generated at the expected time. (The value in the timer register can be changed without any problem if the new value is larger than the up-counter value.) In 16-bit interval timer mode, be sure to write to both TA0REG and TA1REG in this order (16 bits in total). The compare circuit will not function if only the lower 8 bits are set.

## (5) Timer flip-flop (TA1FF)

The timer flip-flop (TA1FF) is a flip-flop inverted by the match detect signals (8-bit comparator output) of each interval timer.

Whether inversion is enabled or disabled is determined by the setting of the bit TA1FFCR<TA1FFIE> in the timer flip-flops control register. A reset clears the value of TA1FF to “0”. Writing “01” or “10” to TA1FFCR<TA1FFC1:0> sets TA1FF to “0” or “1”. Writing “00” to these bits inverts the value of TA1FF. (This is known as software inversion.)

The TA1FF signal is output via the TA1OUT pin. When this pin is used as the timer output, the timer flip-flop should be set beforehand using the port function registers.

The condition for TA1FF inversion varies with mode as shown below

|                            |                                                                              |
|----------------------------|------------------------------------------------------------------------------|
| 8-bit interval timer mode  | : UC0 matches TA0REG or UC1 matches TA1REG<br>(Select either one of the two) |
| 16-bit interval timer mode | : UC0 matches TA0REG or UC1 matches TA1REG                                   |
| 80bit PWM mode             | : UC0 matches TA0REG or a $2^n$ overflow occurs                              |
| 8-bit PPG mode             | : UC0 matches TA0REG or UC0 matches TA1REG                                   |

Note: If an inversion by the match-detect signal and a setting change via the TMRA1 flip-flop control register occur simultaneously, the resultant operation varies depending on the situation, as shown below.

- If an inversion by the match-detect signal and an inversion via the register occur simultaneously, the flip-flop will be inverted only once.
- If an inversion by the match-detect signal and an attempt to set the flip-flop to 1 via the register occur simultaneously, the timer flip-flop will be set to 1.
- If an inversion by the match-detect signal and an attempt to clear the flip-flop to 0 via the register occur simultaneously the flip-flop will be cleared to 1.

Be sure to stop the timer before changing the flip-flop inversion setting.

If the setting is changed while the timer is counting, proper operation cannot be obtained.

3.12.3 SFR

| TMRA01 RUN Register |             |                                             |   |   |                                           |                                                               |                     |                     |
|---------------------|-------------|---------------------------------------------|---|---|-------------------------------------------|---------------------------------------------------------------|---------------------|---------------------|
|                     | 7           | 6                                           | 5 | 4 | 3                                         | 2                                                             | 1                   | 0                   |
| TA01RUN<br>(1100H)  | Bit symbol  | TA0RDE                                      |   |   | I2TA01                                    | TA01PRUN                                                      | TA1RUN              | TA0RUN              |
|                     | Read/Write  | R/W                                         |   |   | R/W                                       |                                                               |                     |                     |
|                     | Reset State | 0                                           |   |   | 0                                         | 0                                                             | 0                   | 0                   |
|                     | Function    | Double<br>buffer<br>0: Disable<br>1: Enable |   |   | In IDLE2<br>mode<br>0: Stop<br>1: Operate | TMRA01<br>prescaler<br>0: Stop and clear<br>1: Run (Count up) | Up counter<br>(UC1) | Up counter<br>(UC0) |

TA0REG double buffer control

|   |         |
|---|---------|
| 0 | Disable |
| 1 | Enable  |

Count control

|   |                |
|---|----------------|
| 0 | Stop and clear |
| 1 | Run (Count up) |

Note: The values of bits 4 to 6 of TA01RUN are “1” when read.

| TMRA23 RUN Register |             |                                             |   |   |                                           |                                                               |                     |                     |
|---------------------|-------------|---------------------------------------------|---|---|-------------------------------------------|---------------------------------------------------------------|---------------------|---------------------|
|                     | 7           | 6                                           | 5 | 4 | 3                                         | 2                                                             | 1                   | 0                   |
| TA23RUN<br>(1108H)  | Bit symbol  | TA2RDE                                      |   |   | I2TA23                                    | TA23PRUN                                                      | TA3RUN              | TA2RUN              |
|                     | Read/Write  | R/W                                         |   |   | R/W                                       |                                                               |                     |                     |
|                     | Reset State | 0                                           |   |   | 0                                         | 0                                                             | 0                   | 0                   |
|                     | Function    | Double<br>buffer<br>0: Disable<br>1: Enable |   |   | In IDLE2<br>mode<br>0: Stop<br>1: Operate | TMRA23<br>prescaler<br>0: Stop and clear<br>1: Run (Count up) | Up counter<br>(UC3) | Up counter<br>(UC2) |

TA3REG double buffer control

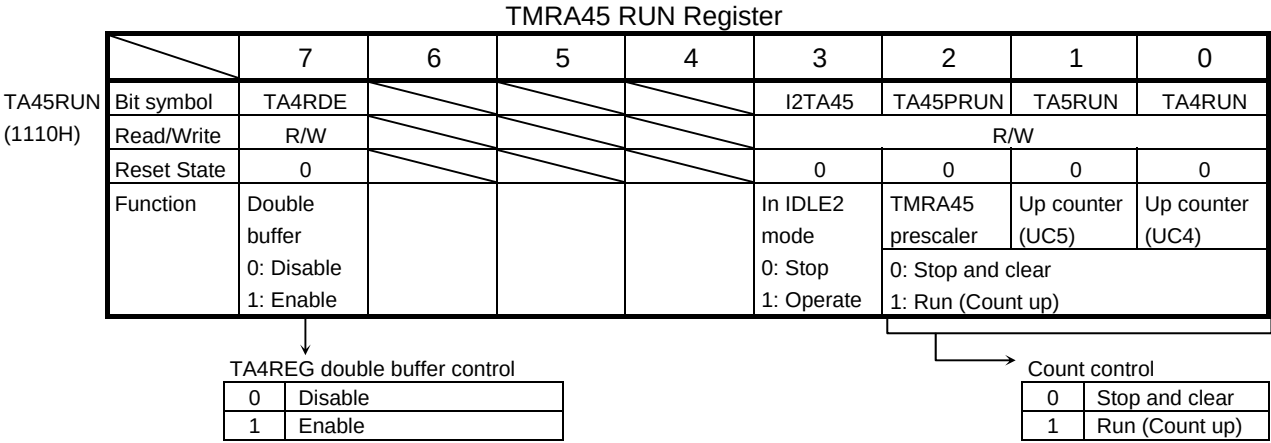
|   |         |
|---|---------|
| 0 | Disable |
| 1 | Enable  |

Count control

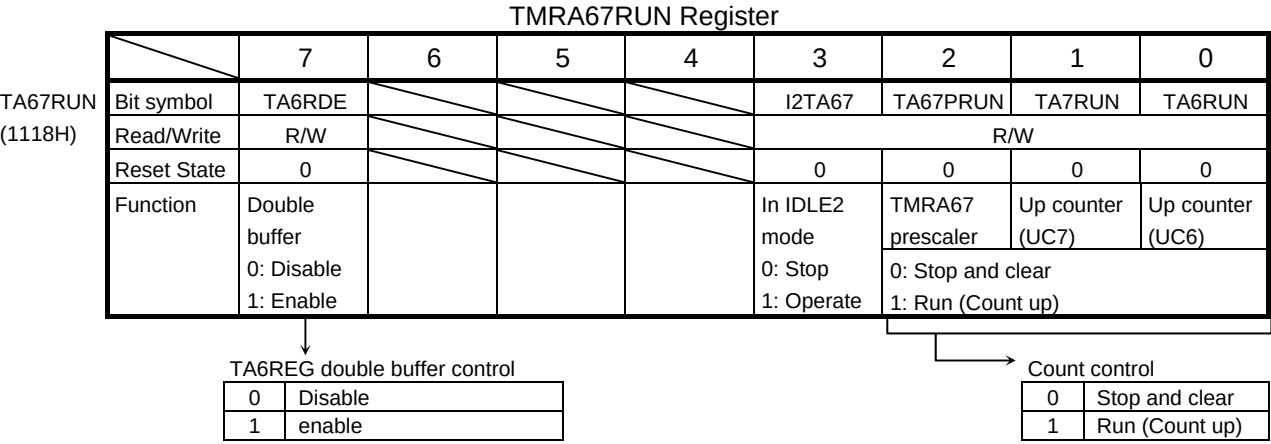
|   |                |
|---|----------------|
| 0 | Stop and clear |
| 1 | Run (Count up) |

Note: The values of bits 4 to 6 of TA23RUN are “1” when read.

Figure 3.12.6 Register for TMRA



Note: The values of bits 4 to 6 of TA45RUN are "1" when read.



Note: The values of bits 4 to 6 of TA67RUN are "1" when read.

Figure 3.12.7 Register for TMRA

| TMRA01 Mode Register |                                                                                                             |        |                                                                  |       |                                                                                            |         |                                                                                             |         |
|----------------------|-------------------------------------------------------------------------------------------------------------|--------|------------------------------------------------------------------|-------|--------------------------------------------------------------------------------------------|---------|---------------------------------------------------------------------------------------------|---------|
|                      | 7                                                                                                           | 6      | 5                                                                | 4     | 3                                                                                          | 2       | 1                                                                                           | 0       |
| Bit symbol           | TA01M1                                                                                                      | TA01M0 | PWM01                                                            | PWM00 | TA1CLK1                                                                                    | TA1CLK0 | TA0CLK1                                                                                     | TA0CLK0 |
| Read/Write           | R/W                                                                                                         |        |                                                                  |       |                                                                                            |         |                                                                                             |         |
| Reset State          | 0                                                                                                           | 0      | 0                                                                | 0     | 0                                                                                          | 0       | 0                                                                                           | 0       |
| Function             | Operation mode<br>00: 8-bit timer mode<br>01: 16-bit timer mode<br>10: 8-bit PPG mode<br>11: 8-bit PWM mode |        | PWM cycle<br>00: Reserved<br>01: $2^6$<br>10: $2^7$<br>11: $2^8$ |       | Source clock for TMRA1<br>00: TA0TRG<br>01: $\phi T1$<br>10: $\phi T16$<br>11: $\phi T256$ |         | Source clock for TMRA0<br>00: TA0IN pin<br>01: $\phi T1$<br>10: $\phi T4$<br>11: $\phi T16$ |         |

TMRA0 input clock

|             |    |                        |
|-------------|----|------------------------|
| <TA0CLK1:0> | 00 | TA0IN (External input) |
|             | 01 | $\phi T1$              |
|             | 10 | $\phi T4$              |
|             | 11 | $\phi T16$             |

TMRA1 input clock

|             |    | TA01MOD<TA01M1:0>=01         | TA01MOD<TA01M1:0>=01                           |
|-------------|----|------------------------------|------------------------------------------------|
| <TA1CLK1:0> | 00 | Comparator output from TMRA0 | Overflow output from TMRA0 (16-bit timer mode) |
|             | 01 | $\phi T1$                    |                                                |
|             | 10 | $\phi T16$                   |                                                |
|             | 11 | $\phi T256$                  |                                                |

PWM cycle selection

|            |    |                           |
|------------|----|---------------------------|
| <PWM01:00> | 00 | Reserved                  |
|            | 01 | $2^6 \times$ Source clock |
|            | 10 | $2^7 \times$ Source clock |
|            | 11 | $2^8 \times$ Source clock |

TMRA01 operation mode selection

|             |    |                                           |
|-------------|----|-------------------------------------------|
| <TA01MA1:0> | 00 | 8 timer $\times$ 2ch                      |
|             | 01 | 16-bit timer                              |
|             | 10 | 8-bit PPG                                 |
|             | 11 | 8-bit PWM (TMRA0),<br>8-bit timer (TMRA1) |

Figure 3.12.8 Register for TMRA



| TMRA23 Mode Register |                                                                                                             |        |                                                                  |       |                                                                                           |         |                                                                                            |         |
|----------------------|-------------------------------------------------------------------------------------------------------------|--------|------------------------------------------------------------------|-------|-------------------------------------------------------------------------------------------|---------|--------------------------------------------------------------------------------------------|---------|
|                      | 7                                                                                                           | 6      | 5                                                                | 4     | 3                                                                                         | 2       | 1                                                                                          | 0       |
| Bit symbol           | TA23M1                                                                                                      | TA23M0 | PWM21                                                            | PWM20 | TA3CLK1                                                                                   | TA3CLK0 | TA2CLK1                                                                                    | TA2CLK0 |
| Read/Write           | R/W                                                                                                         |        |                                                                  |       |                                                                                           |         |                                                                                            |         |
| Reset State          | 0                                                                                                           | 0      | 0                                                                | 0     | 0                                                                                         | 0       | 0                                                                                          | 0       |
| Function             | Operation mode<br>00: 8-bit timer mode<br>01: 16-bit timer mode<br>10: 8-bit PPG mode<br>11: 8-bit PWM mode |        | PWM cycle<br>00: Reserved<br>01: $2^6$<br>10: $2^7$<br>11: $2^8$ |       | TMRA3 clock for TMRA3<br>00: TA2TRG<br>01: $\phi T1$<br>10: $\phi T16$<br>11: $\phi T256$ |         | TMRA2 clock for TMRA2<br>00: TA2IN pin<br>01: $\phi T1$<br>10: $\phi T4$<br>11: $\phi T16$ |         |

TMRA2 input clock

|             |    |                        |
|-------------|----|------------------------|
| <TA2CLK1:0> | 00 | TA2IN (External input) |
|             | 01 | $\phi T1$              |
|             | 10 | $\phi T4$              |
|             | 11 | $\phi T16$             |

TMRA3 input clock

|             |    |                              |                                                   |
|-------------|----|------------------------------|---------------------------------------------------|
|             |    | TA23MOD<TA23M1:0>≠01         | TA23MOD<TA23M1:0>=01                              |
| <TA3CLK1:0> | 00 | Comparator output from TMRA2 | Overflow output from TMRA2<br>(16-bit timer mode) |
|             | 01 | $\phi T1$                    |                                                   |
|             | 10 | $\phi T16$                   |                                                   |
|             | 11 | $\phi T256$                  |                                                   |

PWM cycle selection

|            |    |                           |
|------------|----|---------------------------|
| <PWM21:20> | 00 | Reserved                  |
|            | 01 | $2^6 \times$ Source clock |
|            | 10 | $2^7 \times$ Source clock |
|            | 11 | $2^8 \times$ Source clock |

TMRA23 operation mode selection

|             |    |                                           |
|-------------|----|-------------------------------------------|
| <TA23MA1:0> | 00 | 8 timer $\times$ 2ch                      |
|             | 01 | 16-bit timer                              |
|             | 10 | 8-bit PPG                                 |
|             | 11 | 8-bit PWM (TMRA2),<br>8-bit timer (TMRA3) |

Figure 3.12.9 Register for TMRA

| TMRA45 Mode Register |             |                                                                                                             |        |                                                                                             |       |                                                                         |         |                                                                                    |         |
|----------------------|-------------|-------------------------------------------------------------------------------------------------------------|--------|---------------------------------------------------------------------------------------------|-------|-------------------------------------------------------------------------|---------|------------------------------------------------------------------------------------|---------|
| TA45MOD<br>(1114H)   |             | 7                                                                                                           | 6      | 5                                                                                           | 4     | 3                                                                       | 2       | 1                                                                                  | 0       |
|                      | Bit symbol  | TA45M1                                                                                                      | TA45M0 | PWM41                                                                                       | PWM40 | TA5CLK1                                                                 | TA5CLK0 | TA4CLK1                                                                            | TA4CLK0 |
|                      | Read/Write  | R/W                                                                                                         |        |                                                                                             |       |                                                                         |         |                                                                                    |         |
|                      | Reset State | 0                                                                                                           | 0      | 0                                                                                           | 0     | 0                                                                       | 0       | 0                                                                                  | 0       |
|                      | Function    | Operation mode<br>00: 8-bit timer mode<br>01: 16-bit timer mode<br>10: 8-bit PPG mode<br>11: 8-bit PWM mode |        | PWM cycle<br>00: Reserved<br>01: 2 <sup>6</sup><br>10: 2 <sup>7</sup><br>11: 2 <sup>8</sup> |       | TMRA5 clock for TMRA5<br>00: TA4TRG<br>01: φT1<br>10: φT16<br>11: φT256 |         | TMRA4 clock for TMRA4<br>00: low-frequency clock<br>01: φT1<br>10: φT4<br>11: φT16 |         |

TMRA4 input clock

|             |    |                         |
|-------------|----|-------------------------|
| <TA4CLK1:0> | 00 | low-frequency clock(fs) |
|             | 01 | $\phi T1$               |
|             | 10 | $\phi T4$               |
|             | 11 | $\phi T16$              |

TMRA5 input clock

|             |    |                              |                                                   |
|-------------|----|------------------------------|---------------------------------------------------|
|             |    | TA45MOD<TA45M1:0>≠01         | TA45MOD<TA45M1:0>=01                              |
| <TA5CLK1:0> | 00 | Comparator output from TMRA4 | Overflow output from TMRA4<br>(16-bit timer mode) |
|             | 01 | $\phi T1$                    |                                                   |
|             | 10 | $\phi T16$                   |                                                   |
|             | 11 | $\phi T256$                  |                                                   |

PWM cycle selection

|            |    |                           |
|------------|----|---------------------------|
| <PWM41:40> | 00 | Reserved                  |
|            | 01 | $2^6 \times$ Source clock |
|            | 10 | $2^7 \times$ Source clock |
|            | 11 | $2^8 \times$ Source clock |

TMRA45 operation mode selection

|             |    |                                           |
|-------------|----|-------------------------------------------|
| <TA45MA1:0> | 00 | 8 timer $\times$ 2ch                      |
|             | 01 | 16-bit timer                              |
|             | 10 | 8-bit PPG                                 |
|             | 11 | 8-bit PWM (TMRA4),<br>8-bit timer (TMRA5) |

Figure 3.12.10 Register for TMRA

| TMRA67 Mode Register |             |                                                                                                             |        |                                                                                             |       |                                                                         |         |                                                                                    |         |
|----------------------|-------------|-------------------------------------------------------------------------------------------------------------|--------|---------------------------------------------------------------------------------------------|-------|-------------------------------------------------------------------------|---------|------------------------------------------------------------------------------------|---------|
| TA67MOD<br>(111CH)   |             | 7                                                                                                           | 6      | 5                                                                                           | 4     | 3                                                                       | 2       | 1                                                                                  | 0       |
|                      | Bit symbol  | TA67M1                                                                                                      | TA67M0 | PWM61                                                                                       | PWM60 | TA7CLK1                                                                 | TA7CLK0 | TA6CLK1                                                                            | TA6CLK0 |
|                      | Read/Write  | R/W                                                                                                         |        |                                                                                             |       |                                                                         |         |                                                                                    |         |
|                      | Reset State | 0                                                                                                           | 0      | 0                                                                                           | 0     | 0                                                                       | 0       | 0                                                                                  | 0       |
|                      | Function    | Operation mode<br>00: 8-bit timer mode<br>01: 16-bit timer mode<br>10: 8-bit PPG mode<br>11: 8-bit PWM mode |        | PWM cycle<br>00: Reserved<br>01: 2 <sup>6</sup><br>10: 2 <sup>7</sup><br>11: 2 <sup>8</sup> |       | TMRA7 clock for TMRA7<br>00: TA6TRG<br>01: φT1<br>10: φT16<br>11: φT256 |         | TMRA6 clock for TMRA6<br>00: low-frequency clock<br>01: φT1<br>10: φT4<br>11: φT16 |         |

TMRA6 input clock

|             |    |                         |
|-------------|----|-------------------------|
| <TA6CLK1:0> | 00 | low-frequency clock(fs) |
|             | 01 | $\phi T1$               |
|             | 10 | $\phi T4$               |
|             | 11 | $\phi T16$              |

TMRA1 input clock

|             |    |                              |                                                   |
|-------------|----|------------------------------|---------------------------------------------------|
|             |    | TA67MOD<TA67M1:0>≠01         | TA67MOD<TA67M1:0>=01                              |
| <TA7CLK1:0> | 00 | Comparator output from TMRA6 | Overflow output from TMRA6<br>(16-bit timer mode) |
|             | 01 | $\phi T1$                    |                                                   |
|             | 10 | $\phi T16$                   |                                                   |
|             | 11 | $\phi T256$                  |                                                   |

PWM cycle selection

|            |    |                           |
|------------|----|---------------------------|
| <PWM61:60> | 00 | Reserved                  |
|            | 01 | $2^6 \times$ Source clock |
|            | 10 | $2^7 \times$ Source clock |
|            | 11 | $2^8 \times$ Source clock |

TMRA67 operation mode selection

|             |    |                                           |
|-------------|----|-------------------------------------------|
| <TA67MA1:0> | 00 | 8 timer $\times$ 2ch                      |
|             | 01 | 16-bit timer                              |
|             | 10 | 8-bit PPG                                 |
|             | 11 | 8-bit PWM (TMRA6),<br>8-bit timer (TMRA7) |

Figure 3.12.11 Register for TMRA

| TMRA1 Flip-Flop Control Register                                                     |             |   |   |   |                                                                        |         |                                                              |                                                      |
|--------------------------------------------------------------------------------------|-------------|---|---|---|------------------------------------------------------------------------|---------|--------------------------------------------------------------|------------------------------------------------------|
|                                                                                      | 7           | 6 | 5 | 4 | 3                                                                      | 2       | 1                                                            | 0                                                    |
| TA1FFCR<br>(1105H)<br>A read-<br>modify-write<br>operation<br>cannot be<br>performed | Bit symbol  |   |   |   | TA1FFC1                                                                | TA1FFC0 | TA1FFIE                                                      | TA1FFIS                                              |
|                                                                                      | Read/Write  |   |   |   | R/W                                                                    |         | R/W                                                          |                                                      |
|                                                                                      | Reset State |   |   |   | 1                                                                      | 1       | 0                                                            | 0                                                    |
|                                                                                      | Function    |   |   |   | 00: Invert TA1FF<br>01: Set TA1FF<br>10: Clear TA1FF<br>11: Don't care |         | TA1FF<br>control for<br>inversion<br>0: Disable<br>1: Enable | TA1FF<br>inversion<br>select<br>0: TMRA0<br>1: TMRA1 |

Inversion signal for timer flip-flop 1 (TA1FF)  
(Don't care except in 8-bit timer mode)

|         |   |                    |
|---------|---|--------------------|
| TA1FFIS | 0 | Inversion by TMRA0 |
|         | 1 | Inversion by TMRA1 |

Inversion of TA1FF

|         |   |          |
|---------|---|----------|
| TA1FFIE | 0 | Disabled |
|         | 1 | Enabled  |

Control of TA1FF

|             |    |                                                 |
|-------------|----|-------------------------------------------------|
| <TA1FFC1:0> | 00 | Inverts the value of TA1FF (Software inversion) |
|             | 01 | Sets TA1FF to "1"                               |
|             | 10 | Clears TA1FF to "0"                             |
|             | 11 | Don't care                                      |

Note: The values of bits 4 to 6 of TA1FFCR are "1" when read.

Figure 3.12.12 Register for TMRA

TMRA3 Flip-Flop Control Register

TA3FFCR  
(110DH)  
A read-  
modify-write  
operation  
cannot be  
performed

|             | 7 | 6 | 5 | 4 | 3                                                                      | 2       | 1                                                            | 0                                                    |
|-------------|---|---|---|---|------------------------------------------------------------------------|---------|--------------------------------------------------------------|------------------------------------------------------|
| Bit symbol  |   |   |   |   | TA3FFC1                                                                | TA3FFC0 | TA3FFIE                                                      | TA3FFIS                                              |
| Read/Write  |   |   |   |   | R/W                                                                    |         | R/W                                                          |                                                      |
| Reset State |   |   |   |   | 1                                                                      | 1       | 0                                                            | 0                                                    |
| Function    |   |   |   |   | 00: Invert TA3FF<br>01: Set TA3FF<br>10: Clear TA3FF<br>11: Don't care |         | TA3FF<br>control for<br>inversion<br>0: Disable<br>1: Enable | TA3FF<br>inversion<br>select<br>0: TMRA2<br>1: TMRA3 |

Inversion signal for timer flip-flop 3 (TA3FF)  
(Don't care except in 8-bit timer mode)

|         |   |                    |
|---------|---|--------------------|
| TA3FFIS | 0 | Inversion by TMRA2 |
|         | 1 | Inversion by TMRA3 |

Inversion of TA3FF

|         |   |          |
|---------|---|----------|
| TA3FFIE | 0 | Disabled |
|         | 1 | Enabled  |

Control of TA3FF

|             |    |                                                 |
|-------------|----|-------------------------------------------------|
| <TA3FFC1:0> | 00 | Inverts the value of TA3FF (Software inversion) |
|             | 01 | Sets TA3FF to "1"                               |
|             | 10 | Clears TA3FF to "0"                             |
|             | 11 | Don't care                                      |

Note: The values of bits 4 to 6 of TA3FFCR are "1" when read.

Figure 3.12.13 Register for TMRA

| TMRA7 Flip-Flop Control Register                                                 |             |   |   |   |                                                                        |         |                                                              |                                                      |
|----------------------------------------------------------------------------------|-------------|---|---|---|------------------------------------------------------------------------|---------|--------------------------------------------------------------|------------------------------------------------------|
|                                                                                  | 7           | 6 | 5 | 4 | 3                                                                      | 2       | 1                                                            | 0                                                    |
| TA7FFCR<br>(111DH)<br>A read-modify-write<br>operation<br>cannot be<br>performed | Bit symbol  |   |   |   | TA7FFC1                                                                | TA7FFC0 | TA7FFIE                                                      | TA7FFIS                                              |
|                                                                                  | Read/Write  |   |   |   | R/W                                                                    |         | R/W                                                          |                                                      |
|                                                                                  | Reset State |   |   |   | 1                                                                      | 1       | 0                                                            | 0                                                    |
|                                                                                  | Function    |   |   |   | 00: Invert TA7FF<br>01: Set TA7FF<br>10: Clear TA7FF<br>11: Don't care |         | TA7FF<br>control for<br>inversion<br>0: Disable<br>1: Enable | TA7FF<br>inversion<br>select<br>0: TMRA6<br>1: TMRA7 |

Inversion signal for timer flip-flop 7 (TA7FF)  
(Don't care except in 8-bit timer mode)

|                               |   |                    |
|-------------------------------|---|--------------------|
| TA7FFIS<br>Inversion of TA7FF | 0 | Inversion by TMRA6 |
|                               | 1 | Inversion by TMRA7 |

|                             |   |          |
|-----------------------------|---|----------|
| TA7FFIE<br>Control of TA7FF | 0 | Disabled |
|                             | 1 | Enabled  |

|             |    |                                                 |
|-------------|----|-------------------------------------------------|
| <TA7FFC1:0> | 00 | Inverts the value of TA7FF (Software inversion) |
|             | 01 | Sets TA7FF to "1"                               |
|             | 10 | Clears TA7FF to "0"                             |
|             | 11 | Don't care                                      |

Note: The values of bits 4 to 6 of TA7FFCR are "1" when read.

Figure 3.12.14 Register for TMRA

| Timer Registers   |             |   |   |   |   |   |   |   |   |
|-------------------|-------------|---|---|---|---|---|---|---|---|
|                   |             | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TA0REG<br>(1102H) | bit Symbol  | – |   |   |   |   |   |   |   |
|                   | Read/Write  | W |   |   |   |   |   |   |   |
|                   | Reset State | 0 |   |   |   |   |   |   |   |
| TA1REG<br>(1103H) | bit Symbol  | – |   |   |   |   |   |   |   |
|                   | Read/Write  | W |   |   |   |   |   |   |   |
|                   | Reset State | 0 |   |   |   |   |   |   |   |
| TA2REG<br>(110AH) | bit Symbol  | – |   |   |   |   |   |   |   |
|                   | Read/Write  | W |   |   |   |   |   |   |   |
|                   | Reset State | 0 |   |   |   |   |   |   |   |
| TA3REG<br>(110BH) | bit Symbol  | – |   |   |   |   |   |   |   |
|                   | Read/Write  | W |   |   |   |   |   |   |   |
|                   | Reset State | 0 |   |   |   |   |   |   |   |
| TA4REG<br>(1112H) | bit Symbol  | – |   |   |   |   |   |   |   |
|                   | Read/Write  | W |   |   |   |   |   |   |   |
|                   | Reset State | 0 |   |   |   |   |   |   |   |
| TA5REG<br>(1113H) | bit Symbol  | – |   |   |   |   |   |   |   |
|                   | Read/Write  | W |   |   |   |   |   |   |   |
|                   | Reset State | 0 |   |   |   |   |   |   |   |
| TA6REG<br>(111AH) | bit Symbol  | – |   |   |   |   |   |   |   |
|                   | Read/Write  | W |   |   |   |   |   |   |   |
|                   | Reset State | 0 |   |   |   |   |   |   |   |
| TA7REG<br>(111BH) | bit Symbol  | – |   |   |   |   |   |   |   |
|                   | Read/Write  | W |   |   |   |   |   |   |   |
|                   | Reset State | 0 |   |   |   |   |   |   |   |

Note: A read-modify-write operation cannot be performed for All registers.

Figure 3.12.15 TMRA Registers

### 3.12.4 Operation in Each Mode

#### (1) 8-bit timer mode

Both TMRA0 and TMRA1 can be used independently as 8-bit interval timers.

##### a. Generating interrupts at a fixed interval (Using TMRA1)

To generate interrupts at constant intervals using TMRA1 (INTTA1), first stop TMRA1 then set the operation mode, input clock and a cycle to TA01MOD and TA1REG register respectively. Then, enable the interrupt INTTA1 and start TMRA1 counting.

Example: To generate an INTTA1 interrupt every 20  $\mu$ s at  $f_{SYS}$  = 50 MHz, set each register as follows;

|         |   |               |   |                              |   |     |   |   |   |                                                                                       |  |
|---------|---|---------------|---|------------------------------|---|-----|---|---|---|---------------------------------------------------------------------------------------|--|
|         |   | * Clock state |   | Clcok gear : 1/1             |   |     |   |   |   |                                                                                       |  |
|         |   |               |   | Prescaler of clock gear :1/2 |   |     |   |   |   |                                                                                       |  |
|         |   | MSB           |   |                              |   | LSB |   |   |   |                                                                                       |  |
|         |   | 7             | 6 | 5                            | 4 | 3   | 2 | 1 | 0 |                                                                                       |  |
| TA01RUN | ← | –             | X | X                            | X | –   | – | 0 | – | Stop TMRA1 and clear it to 0.                                                         |  |
| TA01MOD | ← | 0             | 0 | X                            | X | 0   | 1 | X | X | Select 8-bit timer mode and select φT1 (0.16 μs at fSYS = 50 MHz) as the input clock. |  |
| TA1REG  | ← | 0             | 1 | 1                            | 1 | 1   | 1 | 0 | 1 | Set TA1REG to 20 μs ÷ φT1 = 125(7DH)                                                  |  |
| INTETA1 | ← | X             | 1 | 0                            | 1 | X   | – | – | – | Enable INTTA1 and set it to level 5.                                                  |  |
| TA01RUN | ← | –             | X | X                            | X | –   | 1 | 1 | – | Start TMRA1 counting.                                                                 |  |

X: Don't Care, –: No change

Select the input clock using Table 3.12.2.

Note: The input clocks for TMRA0 and TMRA1 are different from as follows.

TMRA0: TA0IN input,  $\phi T1$ ,  $\phi T4$  or  $\phi T16$ .

TMRA1: Matches output of TMRA0,  $\phi T1$ ,  $\phi T16$ , and  $\phi T256$ .



## b. Generating a 50% duty ratio square wave pulse

The state of the timer flip-flop (TA1FF) is inverted at constant intervals and its status output via the timer output pin (TA1OUT).

Example: To output a 3.2μs square wave pulse from the TA1OUT pin at  $f_{SYS} = 50$  MHz, use the following procedure to make the appropriate register settings. This example uses TMRA1; however, either TMRA0 or TMRA1 may be used.

|               |                                                                      |   |   |   |   |   |   |   |   |                                                                                                       |
|---------------|----------------------------------------------------------------------|---|---|---|---|---|---|---|---|-------------------------------------------------------------------------------------------------------|
| * Clock state | <div>Clcok gear : 1/1</div> <div>Prescaler of clock gear : 1/2</div> |   |   |   |   |   |   |   |   |                                                                                                       |
|               | 7                                                                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |                                                                                                       |
| TA01RUN       | ←                                                                    | – | X | X | X | – | – | 0 | – | Stop TMRA1 and clear it to “0”.                                                                       |
| TA01MOD       | ←                                                                    | 0 | 0 | X | X | 0 | 1 | X | X | Select 8-bit timer mode and select $\phi T1$ (0.16 $\mu s$ at $f_{SYS} = 50$ MHz) as the input clock. |
| TA1REG        | ←                                                                    | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | Set the timer register to $3.2 \mu s \div \phi T1 \div 2 = 0AH$                                       |
| TA1FFCR       | ←                                                                    | X | X | X | X | 1 | 0 | 1 | 1 | Clear TA1FF to “0” and set it to invert on the match detect signal from TMRA1.                        |
| PM            | ←                                                                    | – | X | X | X | X | – | 0 | X | Set PM1 to function as the TA1OUT pin.                                                                |
| PMFC          | ←                                                                    | – | X | X | X | X | – | 1 | X |                                                                                                       |
| TA01RUN       | ←                                                                    | – | X | X | X | – | 1 | 1 | – | Start TMRA1 counting.                                                                                 |

X: Don't care, –: No change

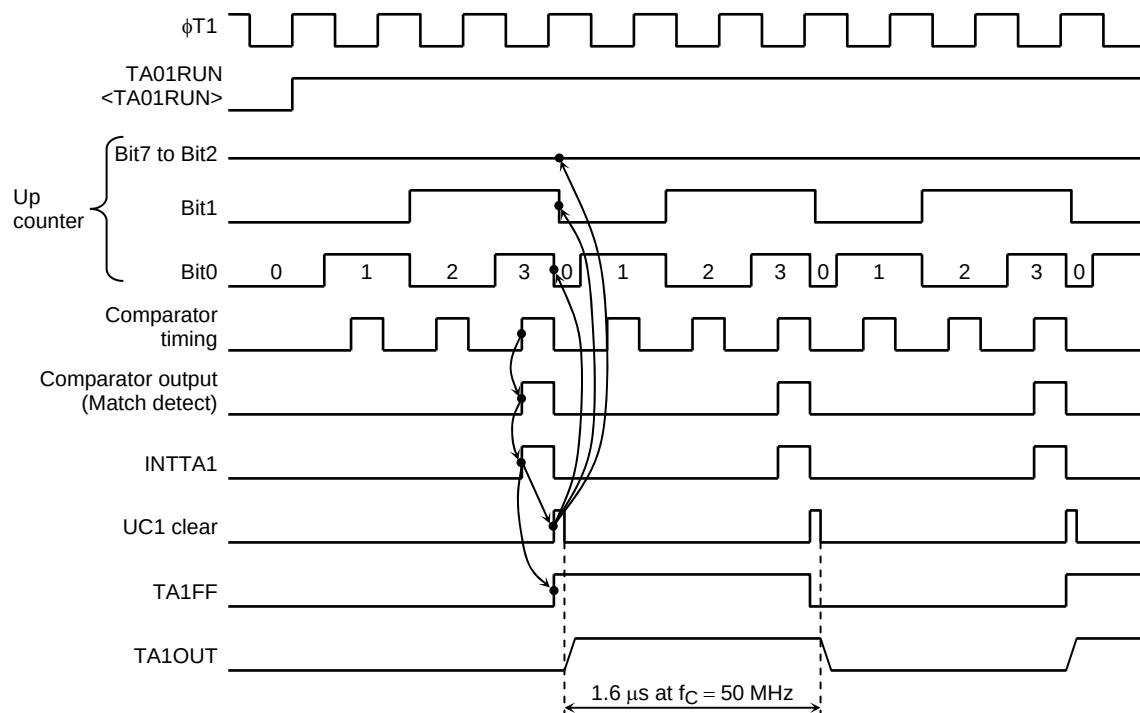


Figure 3.12.16 Square Wave Output Timing Chart (50% duty)

- c. Making TMRA1 count up on the match signal from the TMRA0 comparator
  - Select 8-bit timer mode and set the comparator output from TMRA0 to be the input clock to TMRA1.

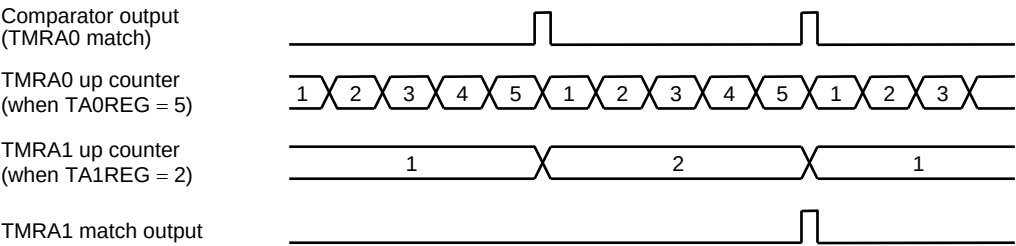


Figure 3.12.17 TMRA1 Count Up on Signal from TMRA0

(2) 16 bit timer mode

Pairing the two 8-bit timers TMRA0 and TMRA1 configures a 16-bit interval timer. To make a 16-bit interval timer in which TMRA0 and TMRA1 are cascaded together, set TA01MOD<TA01M1:0> to “01”.

In 16-bit timer mode, the overflow output from TMRA0 is used as the input clock for TMRA1, regardless of the value set in TA01MOD<TA01CLK1:0>. Table 3.12.2 shows the relationship between the timer (Interrupt) cycle and the input clock selection.

Example: To generate an INTTA1 interrupt every 0.13 s at  $f_{SYS} = 50 \text{ MHz}$ , set the timer registers TA0REG and TA1REG as follows:

\* Clock state       $\left\{ \begin{array}{l} \text{Clcok gear : } 1/1 \\ \text{Prescaler of clock gear : } 1/2 \end{array} \right.$

If  $\phi T16$  ( $2.6 \mu\text{s}$  at  $f_{SYS} = 50 \text{ MHz}$ ) is used as the input clock for counting, set the following value in the registers:  $0.13 \text{ s} \div 2.6 \mu\text{s} = 50000 = \text{C350H}$ ; e.g. set TA1REG to C3H and TA0REG to 50H.

The comparator match signal is output from TMRA0 each time the up counter UC0 matches TA0REG, though the up counter UC0 is not cleared.

In the case of the TMRA1 comparator, the match detect signal is output on each comparator pulse on which the values in the up counter UC1 and TA1REG match. When the match detect signal is output simultaneously from both the comparator TMRA0 and TMRA1, the up counters UC0 and UC1 are cleared to 0 and the interrupt INTTA1 is generated. Also, if inversion is enabled, the value of the timer flip-flop TA1FF is inverted.

Example: When TA1REG = 04H and TA0REG = 80H

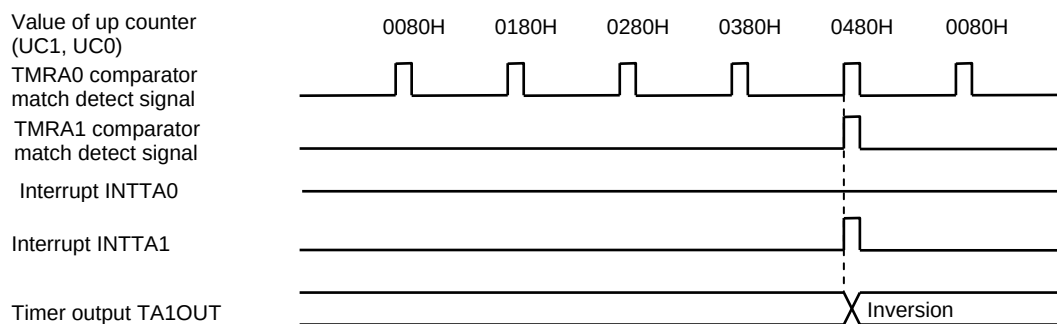


Figure 3.12.18 Timer Output by 16-Bit Timer Mode

### (3) 8-bit PPG (Programmable pulse generation) output mode

Square wave pulses can be generated at any frequency and duty ratio by TMRA0. The output pulses may be active-low or active-high. In this mode TMRA1 cannot be used.

TMRA0 outputs pulses on the TA1OUT pin.

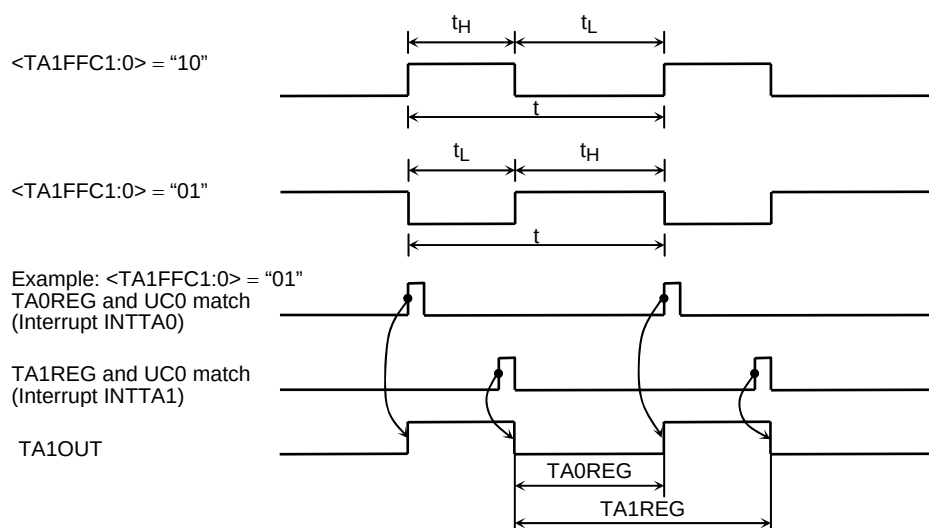


Figure 3.12.19 8-Bit PPG Output Waveforms

In this mode a programmable square wave is generated by inverting the timer output each time the 8-bit up counter (UC0) matches the value in one of the timer registers TA0REG or TA1REG.

The value set in TA0REG must be smaller than the value set in TA1REG.

Although the up counter for TMRA1 (UC1) is not used in this mode, TA01RUN<TA1RUN> should be set to 1 so that UC1 is set for counting.

Figure 3.12.20 shows a block diagram representing this mode.

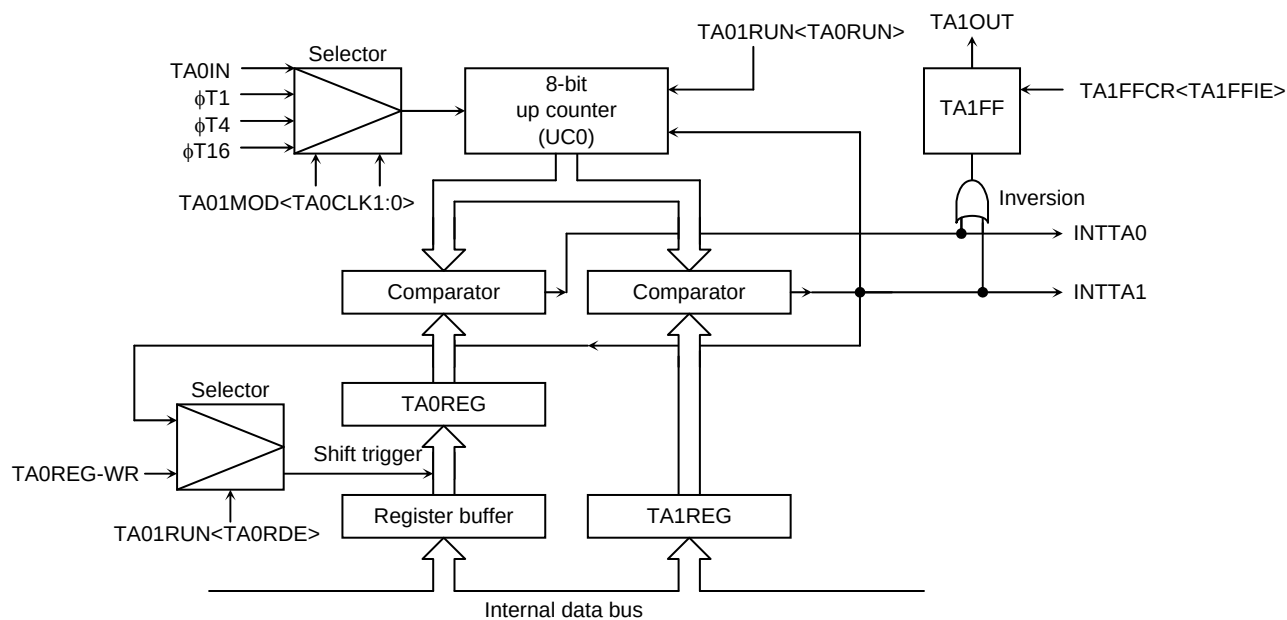


Figure 3.12.20 Block Diagram of 8-Bit PPG Output Mode

If the TA0REG double buffer is enabled in this mode, the value of the register buffer will be shifted into TA0REG each time TA1REG matches UC0.

Use of the double buffer facilitates the handling of low-duty waves (when duty is varied).

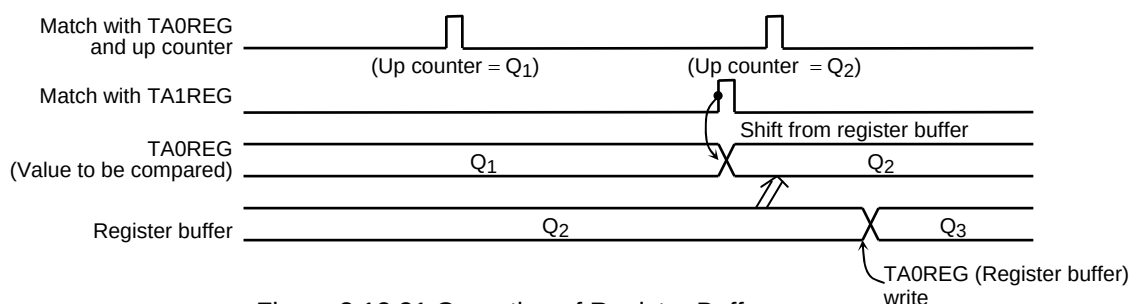
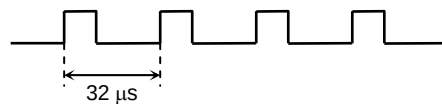


Figure 3.12.21 Operation of Register Buffer

Note: The values that can be set in TAxREG range from 01h to 00h (equivalent to 100h). If the maximum value 00h is set, the match-detect signal goes active when the up-counter overflows.

Example: To generate 1/4 duty 31.25 kHz pulses (at  $f_{SYS}=50$  MHz)



\* Clock state      { Clcok gear :            1/1  
                              Prescaler of clock gear : 1/2

Calculate the value which should be set in the timer register.

To obtain a frequency of 31.25 kHz, the pulse cycle  $t$  should be:  $t = 1/31.25\text{kHz} = 32 \mu\text{s}$

$\phi T1 = 0.16 \mu\text{s}$  (at 50 MHz);

$32 \mu\text{s} \div 0.16 \mu\text{s} = 200$

Therefore set TA1REG to 200 (C8H)

The duty is to be set to 1/4:  $t \times 1/4 = 32 \mu\text{s} \times 1/4 = 8 \mu\text{s}$

$8 \mu\text{s} \div 0.16 \mu\text{s} = 50$

Therefore, set TA0REG = 50 = 32H.

|         | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |                                                              |
|---------|---|---|---|---|---|---|---|---|---|--------------------------------------------------------------|
| TA01RUN | ← | – | X | X | X | – | – | 0 | 0 | Stop TMRA0 and TMRA1 and clear it to “0”.                    |
| TA01MOD | ← | 1 | 0 | X | X | X | X | 0 | 1 | Set the 8-bit PPG mode, and select $\phi T1$ as input clock. |
| TA0REG  | ← | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | Write 32H.                                                   |
| TA1REG  | ← | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | Write C8H.                                                   |
| TA1FFCR | ← | X | X | X | X | 0 | 1 | 1 | X | Set TA1FF, enabling both inversion and the double buffer.    |
|         |   |   |   |   |   |   |   |   |   | Writing 10 provides negative logic pulse.                    |
| PM      | ← | – | X | X | X | X | – | 0 | X | Set PM1 as the TA1OUT pin.                                   |
| PMFC    | ← | – | X | X | X | X | – | 1 | X |                                                              |
| TA01RUN | ← | 1 | X | X | X | – | 1 | 1 | 1 | Start TMRA0 and TMRA1 counting.                              |

X: Don't care, –: No change

## (4) 8-bit PWM (Pulse width modulation) output mode

This mode is only valid for TMRA0. In this mode, a PWM pulse with the maximum resolution of 8 bits can be output.

When TMRA0 is used the PWM pulse is output on the TA1OUT pin (Shared with PM1). TMRA1 can also be used as an 8-bit timer.

The timer output is inverted when the up counter (UC0) matches the value set in the timer register TA0REG or when  $2^n$  counter overflow occurs ( $n = 6, 7$  or  $8$  as specified by TA01MOD<PWM01:00>). The up counter UC0 is cleared when  $2^n$  counter overflow occurs.

The following conditions must be satisfied before this PWM mode can be used.

Value set in TA0REG < Value set for  $2^n$  counter overflow

Value set in TA0REG  $\neq 0$

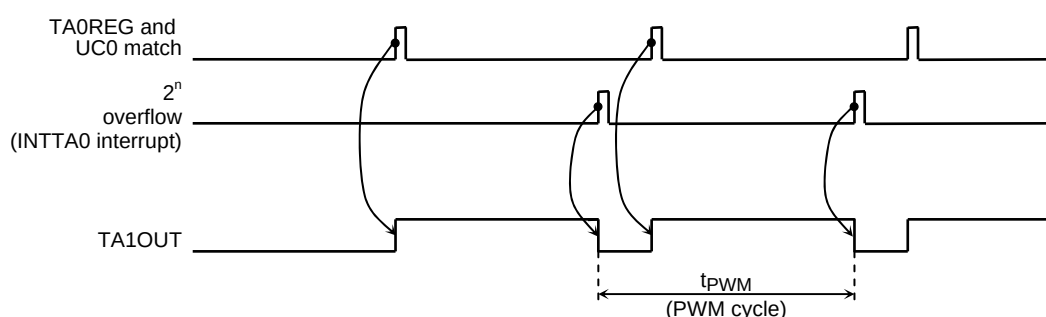


Figure 3.12.22 8-Bit PWM Waveforms

Figure 3.12.23 shows a block diagram representing this mode.

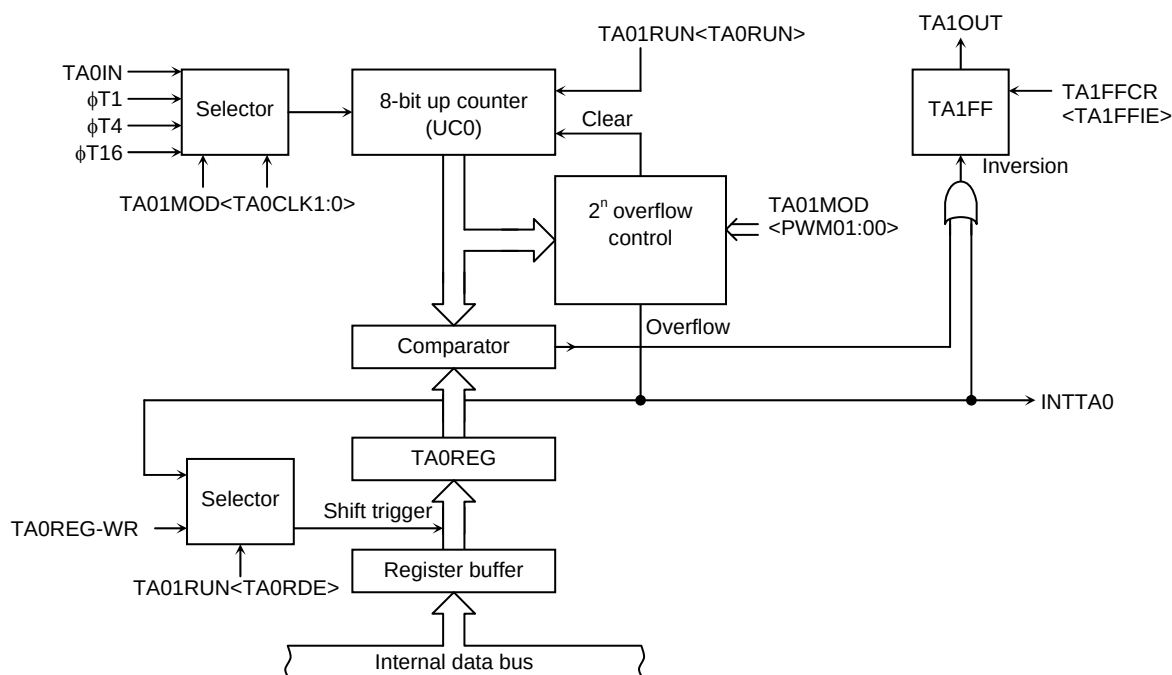


Figure 3.12.23 Block Diagram of 8-Bit PWM Mode

In this mode the value of the register buffer will be shifted into TA0REG if  $2^n$  overflow is detected when the TA0REG double buffer is enabled.

Use of the double buffer facilitates the handling of low duty ratio waves.

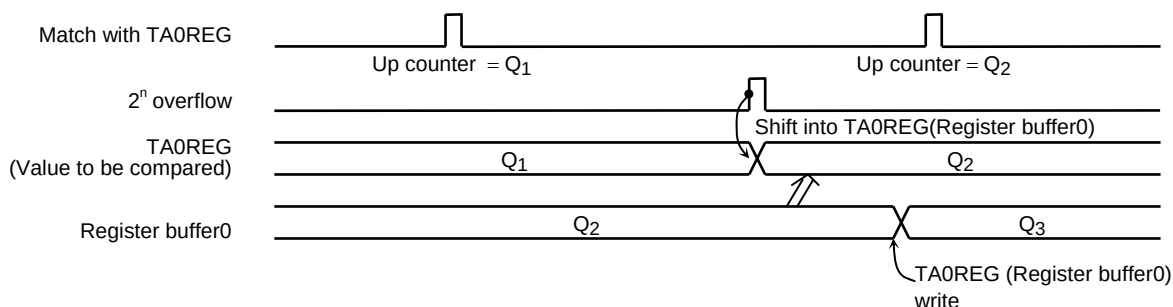
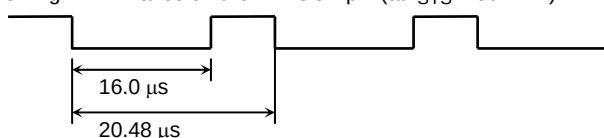


Figure 3.12.24 Register Buffer Operation

Example: To output the following PWM waves on the TA1OUT pin (at  $f_{SYS} = 50$  MHz).



\* Clock state      { Clock gear :            1/1  
                              Prescaler of clock gear : 1/2

To achieve a 20.48μs PWM cycle by setting  $\phi T1$  to 0.16 μs (at  $f_{SYS} = 50$  MHz):

$$20.48 \mu s \div 0.16 \mu s = 128$$

$$2^n = 128$$

Therefore n should be set to 7.

Since the low level period is 16.0 μs when  $\phi T1 = 0.16 \mu s$ ,

set the following value for TAREG:

$$16.0 \mu s \div 0.16 \mu s = 100 = 64H$$

|         | MSB |   |   |   | LSB |   |   |   |   |                                                                                   |
|---------|-----|---|---|---|-----|---|---|---|---|-----------------------------------------------------------------------------------|
|         | 7   | 6 | 5 | 4 | 3   | 2 | 1 | 0 |   |                                                                                   |
| TA01RUN | ←   | – | X | X | X   | – | – | – | 0 | Stop TMRA0 and clear it to 0                                                      |
| TA01MOD | ←   | 1 | 1 | 1 | 0   | X | X | 0 | 1 | Select 8-bit PWM mode (cycle: 2 <sup>7</sup> ) and select ϕT1 as the input clock. |
| TA0REG  | ←   | 0 | 1 | 1 | 0   | 0 | 1 | 0 | 0 | Write 64H.                                                                        |
| TA1FFCR | ←   | X | X | X | X   | 1 | 0 | 1 | X | Clear TA1FF to 0, enable the inversion and double buffer.                         |
| PM      | ←   | – | X | X | X   | X | – | 0 | X | } Set PM1 as the TA1OUT pin.                                                      |
| PMFC    | ←   | – | X | X | X   | X | – | 1 | X |                                                                                   |
| TA01RUN | ←   | 1 | X | X | X   | – | 1 | – | 1 | Start TMRA0 counting.                                                             |

X: Don't care, –: No change

X: Don't care, –: No change

Table 3.12.3 PWM Cycle

|      | Clock gear<br>selection<br>SYSCR1<br><GEAR2:0> | Prescaler of<br>clock gear<br>SYSCR0<br><PRCK> |    | PWM cycle<br>TAxxMOD<PWMx1:0> |           |           |                       |           |            |                       |           |            |
|------|------------------------------------------------|------------------------------------------------|----|-------------------------------|-----------|-----------|-----------------------|-----------|------------|-----------------------|-----------|------------|
|      |                                                |                                                |    | 2 <sup>6</sup> (x64)          |           |           | 2 <sup>7</sup> (x128) |           |            | 2 <sup>8</sup> (x256) |           |            |
|      |                                                |                                                |    | TAxxMOD<TAxCLK1:0>            |           |           | TAxxMOD<TAxCLK1:0>    |           |            | TAxxMOD<TAxCLK1:0>    |           |            |
|      |                                                |                                                |    | φT1(x2)                       | φT4(x8)   | φT16(x32) | φT1(x2)               | φT4(x8)   | φT16(x32)  | φT1(x2)               | φT4(x8)   | φT16(x32)  |
| 1/fc | 000(x1)                                        | 0(x2)                                          | x2 | 512/fc                        | 2048/fc   | 8192/fc   | 1024/fc               | 4096/fc   | 16384/fc   | 2048/fc               | 8192/fc   | 32768/fc   |
|      | 001(x2)                                        |                                                |    | 1024/fc                       | 4096/fc   | 16384/fc  | 2048/fc               | 8192/fc   | 32768/fc   | 4096/fc               | 16384/fc  | 65536/fc   |
|      | 010(x4)                                        |                                                |    | 2048/fc                       | 8192/fc   | 32768/fc  | 4096/fc               | 16384/fc  | 65536/fc   | 8192/fc               | 32768/fc  | 131072/fc  |
|      | 011(x8)                                        |                                                |    | 4096/fc                       | 16384/fc  | 65536/fc  | 8192/fc               | 32768/fc  | 131072/fc  | 16384/fc              | 65536/fc  | 262144/fc  |
|      | 100(x16)                                       |                                                |    | 8192/fc                       | 32768/fc  | 131072/fc | 16384/fc              | 65536/fc  | 262144/fc  | 32768/fc              | 131072/fc | 524288/fc  |
|      | 000(x1)                                        | 1(x8)                                          |    | 2048/fc                       | 8192/fc   | 32768/fc  | 4096/fc               | 16384/fc  | 65536/fc   | 8192/fc               | 32768/fc  | 131072/fc  |
|      | 001(x2)                                        |                                                |    | 4096/fc                       | 16384/fc  | 65536/fc  | 8192/fc               | 32768/fc  | 131072/fc  | 16384/fc              | 65536/fc  | 262144/fc  |
|      | 010(x4)                                        |                                                |    | 8192/fc                       | 32768/fc  | 131072/fc | 16384/fc              | 65536/fc  | 262144/fc  | 32768/fc              | 131072/fc | 524288/fc  |
|      | 011(x8)                                        |                                                |    | 16384/fc                      | 65536/fc  | 262144/fc | 32768/fc              | 131072/fc | 524288/fc  | 65536/fc              | 262144/fc | 1048576/fc |
|      | 100(x16)                                       |                                                |    | 32768/fc                      | 131072/fc | 524288/fc | 65536/fc              | 262144/fc | 1048576/fc | 131072/fc             | 524288/fc | 2097152/fc |

## (5) Settings for each mode

Table 3.12.4 shows the SFR settings for each mode.

Table 3.12.4 Timer Mode Setting Registers

| Register Name            | TA01MOD    |                                                                  |                                                           |                                                      | TA1FFCR                                        |
|--------------------------|------------|------------------------------------------------------------------|-----------------------------------------------------------|------------------------------------------------------|------------------------------------------------|
| <Bit Symbol>             | <TA01M1:0> | <PWM01:00>                                                       | <TA1CLK1:0>                                               | <TA0CLK1:0>                                          | TA1FFIS                                        |
| Function                 | Timer Mode | PWM Cycle                                                        | Upper Timer Input Clock                                   | Lower Timer Input Clock                              | Timer F/F Invert Signal Select                 |
| 8-bit timer × 2 channels | 00         | —                                                                | Lower timer match<br>φT1, φT16, φT256<br>(00, 01, 10, 11) | External clock<br>φT1, φT4, φT16<br>(00, 01, 10, 11) | 0: Lower timer output<br>1: Upper timer output |
| 16-bit timer mode        | 01         | —                                                                | —                                                         | External clock<br>φT1, φT4, φT16<br>(00, 01, 10, 11) | —                                              |
| 8-bit PPG × 1 channel    | 10         | —                                                                | —                                                         | External clock<br>φT1, φT4, φT16<br>(00, 01, 10, 11) | —                                              |
| 8-bit PWM × 1 channel    | 11         | 2 <sup>6</sup> , 2 <sup>7</sup> , 2 <sup>8</sup><br>(01, 10, 11) | —                                                         | External clock<br>φT1, φT4, φT16<br>(00, 01, 10, 11) | —                                              |
| 8-bit timer × 1 channel  | 11         | —                                                                | φT1, φT16, φT256<br>(01, 10, 11)                          | —                                                    | Output disabled                                |

—: Don't care



### 3.13 16 bit timer / Event counter (TMRB)

The TMP92CF30 incorporates two multifunctional 16-bit timer/event counter (TMRB0, TMRB1) which have the following operation modes:

- 16 bit interval timer mode
- 16 bit event counter mode
- 16 bit programmable pulse generation mode (PPG)

Can be used following operation modes by capture function.

- Frequency measurement mode
- Pulse width measurement mode

The timer/event counter consists of a 16-bit up counter, two 16-bit timer registers (one of them with a double-buffer structure), a 16-bit capture registers two comparators, a capture input controller, a timer flip-flop and a control circuit.

The timer/event counter is controlled by an 11-byte control SFR.

Each channel (TMRB0,TMRB1) operate independently. In this section, the explanation describes only for TMRB0 because each channel is identical operation except for the difference as follows;

Table 3.13.1 Difference between TMRB0 and TMRB1

| Channel          |                                               | TMRB0                        | TMRB1                       |
|------------------|-----------------------------------------------|------------------------------|-----------------------------|
| Specification    |                                               |                              |                             |
| External pins    | External clock/<br>capture trigger input pins | TB0IN0<br>(Shared with PP4)  | TB1IN0<br>(Shared with PP5) |
|                  | Timer flip-flop output pins                   | TB0OUT0<br>(Shared with PP6) | –                           |
| SFR<br>(Address) | Timer run register                            | TB0RUN (1180H)               | TB1RUN (1190H)              |
|                  | Timer mode register                           | TB0MOD (1182H)               | TB1MOD (1192H)              |
|                  | Timer flip-flop<br>control register           | TB0FFCR (1183H)              | –                           |
|                  | Timer register                                | TB0RG0L (1188H)              | TB1RG0L (1198H)             |
|                  |                                               | TB0RG0H (1189H)              | TB1RG0H (1199H)             |
|                  |                                               | TB0RG1L (118AH)              | TB1RG1L (119AH)             |
|                  |                                               | TB0RG1H (118BH)              | TB1RG1H (119BH)             |
|                  | Capture register                              | TB0CP0L (118CH)              | TB1CP0L (119CH)             |
|                  |                                               | TB0CP0H (118DH)              | TB1CP0H (119DH)             |
|                  |                                               | TB0CP1L (118EH)              | TB1CP1L (119EH)             |
|                  |                                               | TB0CP1H (118FH)              | TB1CP1H (119FH)             |

## 3.13.1 Block diagram

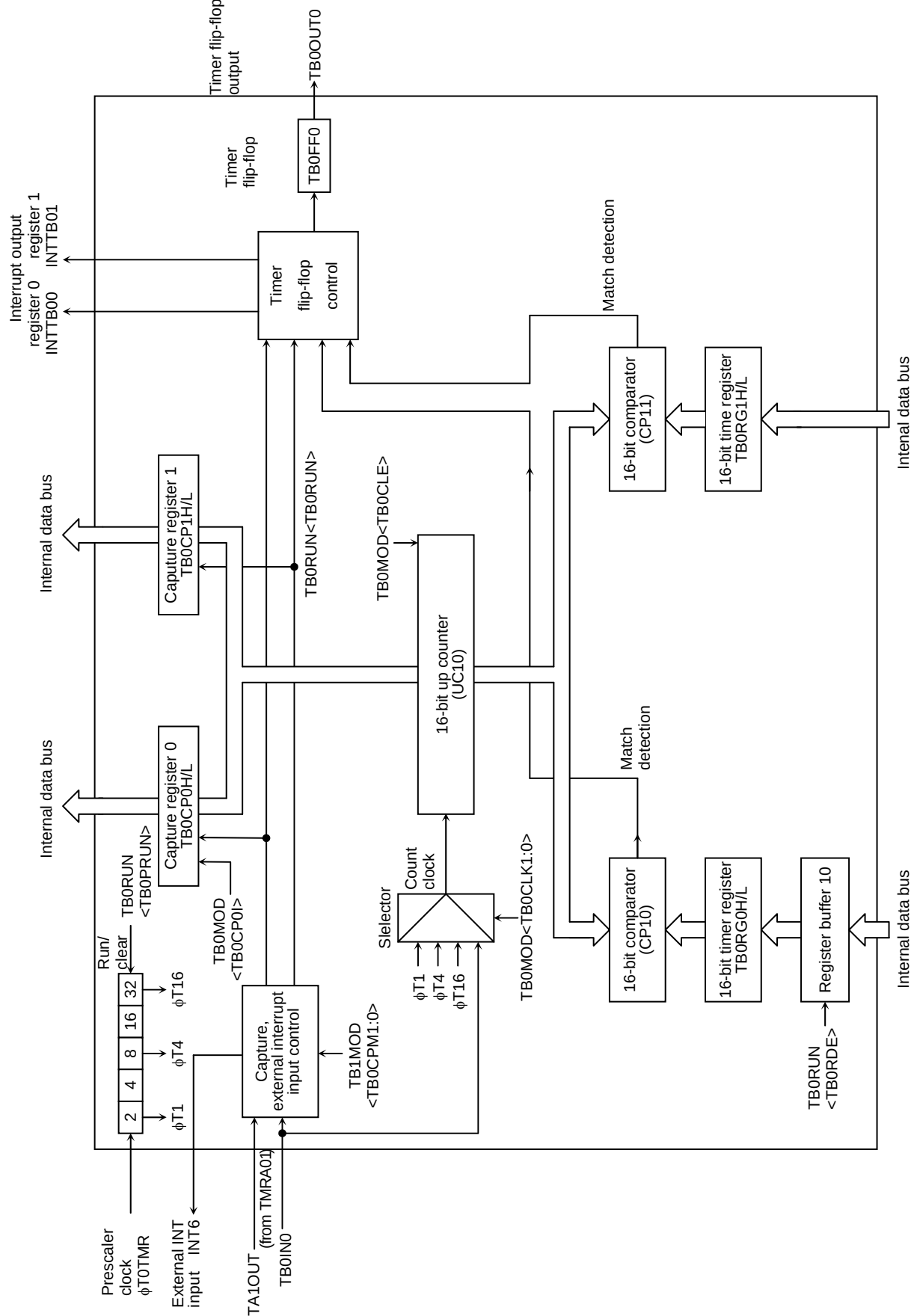


Figure 3.13.1 Block diagram of TMRB0

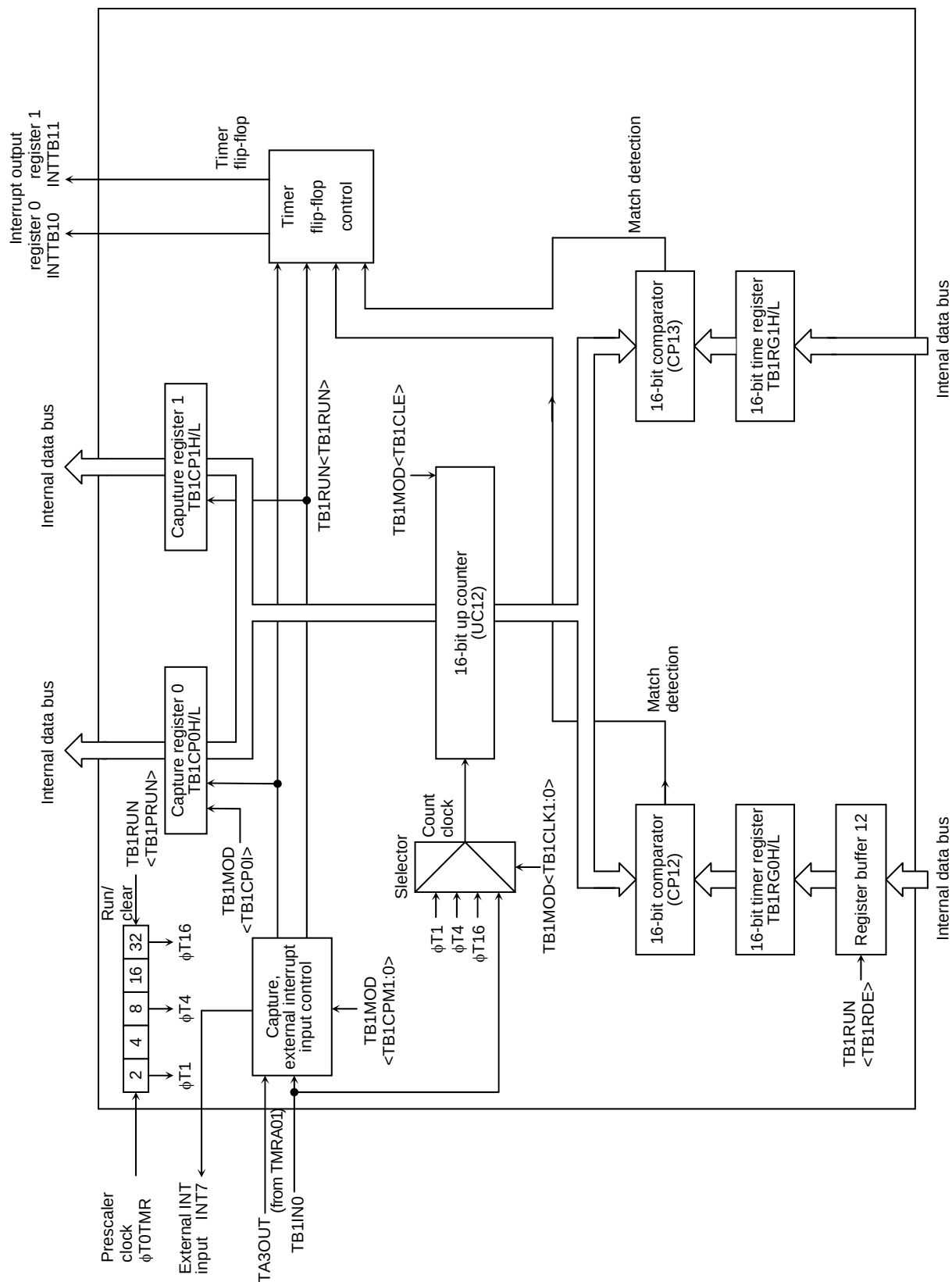


Figure 3.13.2 Block diagram of TMRB1

### 3.13.2 Operation

#### (1) Prescaler

The 5-bit prescaler generates the source clock for TMRB0. The prescaler clock ( $\phi$ T0TMR) is selected by the register SYSCR0<PRCK> of clock gear. This prescaler can be started or stopped using TB0RUN<TB0PRUN>. Counting starts when <TB0RUN> is set to “1”; the prescaler is cleared to “0” and stops operation when <TB0RUN> is cleared to “0”.

The resolution of prescaler is showed in the Table 3.13.2.

Table 3.13.2 Prescaler Clock Resolution

|    | Clock gear selection<br>SYSCR1<br><GEAR2:0> | Prescaler of clock gear<br>SYSCR0<br><PRCK> | —   | Timer counter input clock<br>Prescaler of TMRB<br>TBxMOD<TBxCLK1:0> |          |            |
|----|---------------------------------------------|---------------------------------------------|-----|---------------------------------------------------------------------|----------|------------|
|    |                                             |                                             |     | ϕT1(1/2)                                                            | ϕT4(1/8) | ϕT16(1/32) |
| fc | 000(1/1)                                    | 0(1/2)                                      | 1/2 | fc/8                                                                | fc/32    | fc/128     |
|    | 001(1/2)                                    |                                             |     | fc/16                                                               | fc/64    | fc/256     |
|    | 010(1/4)                                    |                                             |     | fc/32                                                               | fc/128   | fc/512     |
|    | 011(1/8)                                    |                                             |     | fc/64                                                               | fc/256   | fc/1024    |
|    | 100(1/16)                                   |                                             |     | fc/128                                                              | fc/512   | fc/2048    |
|    | 000(1/1)                                    | 1(1/8)                                      |     | fc/32                                                               | fc/128   | fc/512     |
|    | 001(1/2)                                    |                                             |     | fc/64                                                               | fc/256   | fc/1024    |
|    | 010(1/4)                                    |                                             |     | fc/128                                                              | fc/512   | fc/2048    |
|    | 011(1/8)                                    |                                             |     | fc/256                                                              | fc/1024  | fc/4096    |
|    | 100(1/16)                                   |                                             |     | fc/512                                                              | fc/2048  | fc/8192    |

#### (2) Up counter (UC10)

UC10 is a 16-bit binary counter which counts up pulses input from the clock specified by TB0MOD<TB0CLK1:0>.

Any one of the prescaler internal clocks  $\phi$ T1,  $\phi$ TB0 and  $\phi$ T16 or an external clock input via the TB0IN0 pin can be selected as the input clock. Counting or stopping and clearing of the counter is controlled by TB0RUN<TB0RUN>.

When clearing is enabled, the up counter UC10 will be cleared to “0” each time its value matches the value in the timer register TB0RG1H/L. If clearing is disabled, the counter operates as a free running counter.

Clearing can be enabled or disabled using TB0MOD<TB0CLE>.

(3) Timer registers (TB0RG0H/L, TB0RG1H/L)

These two 16-bit registers are used to set the interval time. When the value in the up counter UC10 matches the value set in this timer register, the comparator match detect signal will go active.

Setting data for both upper and lower timer registers is always needed. For example, either using a 2-byte data transfer instruction or using a 1-byte data transfer instruction twice for the lower 8 bits and upper 8 bits in order.

(The compare circuit will not operate if only the lower 8 bits are written. Be sure to write to both timer registers (16 bits) from the lower 8 bits followed by the upper 8 bits.)

The TB0RG0H/L timer register has a double-buffer structure, which is paired with a register buffer 10. The value set in TB0RUN<TB0RDE> determines whether the double-buffer structure is enabled or disabled: it is disabled when <TB0RDE> = "0", and enabled when <TB0RDE> = "1".

When the double buffer is enabled, data is transferred from the register buffer 10 to the timer register when the values in the up counter (UC10) and the timer register TB0RG1H/L match.

The double buffer circuit incorporates two flags to indicate whether or not data is written to the lower 8 bits and the upper 8 bits of the register buffer, respectively. Only when both flags are set can data be transferred from the register buffer to the timer register by a match between the up-counter UC10 and the timer register TB0RG1H/L. This data transfer is performed so long as 16-bit data is written in the register buffer regardless of the register buffer to the timer register unexpectedly as explained below.

For example, let us assume that an interrupt occurs when only the lower 8 bits (L1) of the register buffer data (H1L1) have been written and the interrupt routine includes writes to all 16 bits in the register buffer and a transfer of the data to the timer register. In this case, if the higher 8 bits (H1) are written after the interrupt routine is completed, only the flag for the higher 8 bits will be set, the flag for the lower 8 bits having been cleared in the interrupt routine. Therefore, even if a match occurs between UC10 and TB0RG1H/L, no data transfer will be performed.

Then, in an attempt to set the next set of data (H2L2) in the register buffer, when the lower 8 bits (L2) are written, this will cause the flag for the lower 8 bits to be set as well as the flag for the higher 8 bits which has been set by writing the previous data (H1). If a match between UC10 and TB0RG1H/L occurs before the higher 8 bits (H2) are written, this will cause unexpected data (H1L2) to be sent to the timer register instead of the intended data (H2L2).

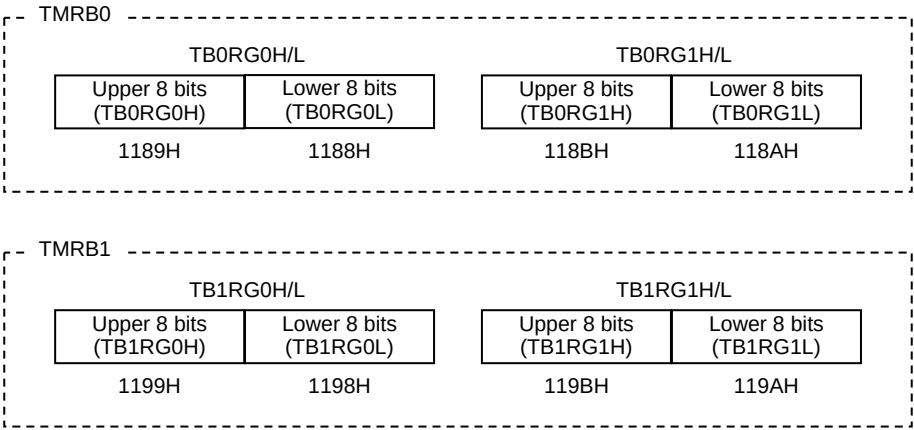
To avoid such transfer timing problems due to interrupts, the DI instruction (disable interrupts) and the EI (enable interrupts) can be executed before and after setting data in the register buffer, respectively.

After a reset, TB0RG0H/L and TB0RG1H/L are undefined. If the 16-bit timer is to be used after a reset, data should be written to it beforehand.

On a reset <TB0RDE> is initialized to "0", disabling the double buffer. To use the double buffer, write data to the timer register, set <TB0RDE> to "1", then write data to the register buffer 10 as shown below.

TB0RG0H/L and the register buffer 10 both have the same memory addresses (1188H and 1189H) allocated to them. If <TB0RDE> = “0”, the value is written to both the timer register and the register buffer 10. If <TB0RDE> = “1”, the value is written to the register buffer 10 only.

The addresses of the timer registers are as follows:



The timer registers are write-only registers and thus cannot be read.

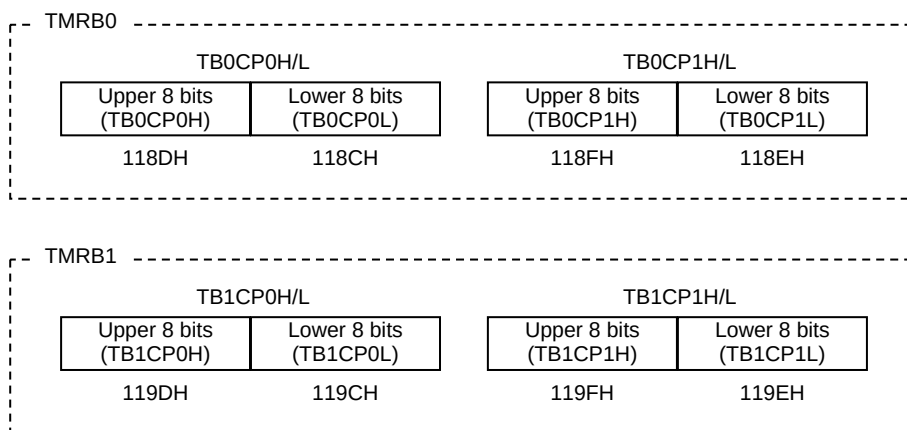
## (4) Capture registers (TB0CP0H/L, TB0CP1H/L)

These 16-bit registers are used to latch the values in the up counter (UC10).

All 16 bits of data in the capture registers should be read. For example, using a 2-byte data load instruction or two 1-byte data load instructions. The least significant byte is read first, followed by the most significant byte.

(during capture is read, capture operation is prohibited. In that case, the lower 8 bits should be read first, followed by the 8 bits.)

The addresses of the capture registers are as follows;



The capture registers are read-only registers and thus cannot be written to.

## (5) Capture input and external interrupt control

This circuit controls the timing to latch the value of the up-counter UC10 into TB0CP0H/L and TB0CP1H/L, and generates external interrupt. The latch timing of capture register and selection of edge for external interrupt is controlled by TB0MOD<TB0CPM1:0>.

The value in the up-counter (UC10) can be loaded into a capture register by software. Whenever "0" is written to TB0MOD<TB0CP0I>, the current value in the up counter (UC10) is loaded into capture register TB0CP0H/L. It is necessary to keep the prescaler in RUN mode (i.e., TB0RUN<TB0PRUN> must be held at a value of "1").

(6) Comparators (CP10, CP11)

CP10 and CP11 are 16-bit comparators which compare the value in the up counter UC10 with the value set in TB0RG0H/L or TB0RG1H/L respectively, in order to detect a match. If a match is detected, the comparator generates an interrupt (INTTB00 or INTTB01 respectively).

(7) Timer flip-flops (TB0FF0)

These flip-flops are inverted by the match detect signals from the comparators and the latch signals to the capture registers. Inversion can be enabled and disabled for each element using TB0FFCR<TB0C1T1, TB0C0T1, TB0E1T1, TB0E0T1>.

After a reset the value of TB0FF0 is undefined. If "00" is written to TB0FFCR <TB0FF0C1:0>, TB0FF0 will be inverted. If "01" is written to the capture registers, the value of TB0FF0 will be set to "1". If "10" is written to the capture registers, the value of TB0FF0 will be set to "0".

Note: If an inversion by the match-detect signal and a setting change via the TB0FFCR register occurs simultaneously, the resultant operation varies depending on the situation, as shown below.

- If an inversion by the match-detect signal and an inversion via the register occur simultaneously, the flip-flop will be inverted only once.
- If an inversion by the match-detect signal and an attempt to set the flip-flop to "1" via the register occur simultaneously, the flip-flop will be set to "1".
- If an inversion by the match-detect signal and an attempt to clear the flip-flop to "0" via the register occur simultaneously, the flip-flop will be cleared to "0".

If an inversion by match-detect signal and inversion disable setting occur simultaneously, two cases (it is inverted and it is not inverted) are occurred. Therefore, if changing inversion control (inversion enable/disable), stop timer operation beforehand.

The values of TB0FF0 can be output via the timer output pins TB0OUT0 (which is shared with PP6) and TB0OUT1 (which is shared with PP7). Timer output should be specified using the port P function register.



## 3.13.3 SFR

TMRB0 RUN Register

|             | 7                                        | 6                | 5 | 4 | 3                                      | 2                                                         | 1 | 0                 |
|-------------|------------------------------------------|------------------|---|---|----------------------------------------|-----------------------------------------------------------|---|-------------------|
| Bit symbol  | TB0RDE                                   | –                |   |   | I2TB0                                  | TB0PRUN                                                   |   | TB0RUN            |
| Read/Write  | R/W                                      | R/W              |   |   | R/W                                    | R/W                                                       |   | R/W               |
| Reset State | 0                                        | 0                |   |   | 0                                      | 0                                                         |   | 0                 |
| Function    | Double buffer<br>0: disable<br>1: enable | Always write "0" |   |   | In IDLE2 mode<br>0: Stop<br>1: Operate | TMRB0 prescaler<br>0: Stop and clear<br>1: Run (Count up) |   | Up counter (UC10) |

Count operation

|                     |   |                |
|---------------------|---|----------------|
| <TB0PRUN>, <TB0RUN> | 0 | Stop and clear |
|                     | 1 | Count up       |

Note: 1, 4 and 5 of TB0RUN are read as "1" values.

TMRB1 RUN Register

|             | 7                                        | 6                | 5 | 4 | 3                                      | 2                                                         | 1 | 0                 |
|-------------|------------------------------------------|------------------|---|---|----------------------------------------|-----------------------------------------------------------|---|-------------------|
| Bit symbol  | TB1RDE                                   | –                |   |   | I2TB1                                  | TB1PRUN                                                   |   | TB1RUN            |
| Read/Write  | R/W                                      | R/W              |   |   | R/W                                    | R/W                                                       |   | R/W               |
| Reset State | 0                                        | 0                |   |   | 0                                      | 0                                                         |   | 0                 |
| Function    | Double buffer<br>0: disable<br>1: enable | Always write "0" |   |   | In IDLE2 mode<br>0: Stop<br>1: Operate | TMRB1 prescaler<br>0: Stop and clear<br>1: Run (Count up) |   | Up counter (UC12) |

Count operation

|                     |   |                |
|---------------------|---|----------------|
| <TB1PRUN>, <TB1RUN> | 0 | Stop and clear |
|                     | 1 | Count up       |

Note: 1, 4 and 5 of TB1RUN are read as "1" values.

Figure 3.13.3 Register for TMRB

TMRB0 Mode Register

TB0MOD  
(1182H)  
A read-  
modify-write  
operation  
cannot be  
performed

|             | 7                 | 6 | 5                                                               | 4                                                                                                                                                                                                                           | 3       | 2                                                | 1                                                                                          | 0       |
|-------------|-------------------|---|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|--------------------------------------------------|--------------------------------------------------------------------------------------------|---------|
| Bit symbol  | –                 | – | TB0CP0I                                                         | TB0CPM1                                                                                                                                                                                                                     | TB0CPM0 | TB0CLE                                           | TB0CLK1                                                                                    | TB0CLK0 |
| Read/Write  | R/W               |   | W*                                                              | R/W                                                                                                                                                                                                                         |         |                                                  |                                                                                            |         |
| Reset State | 0                 | 0 | 1                                                               | 0                                                                                                                                                                                                                           | 0       | 0                                                | 0                                                                                          | 0       |
| Function    | Always write "0". |   | Software capture control<br>0: Software capture<br>1: Undefined | Capture timing<br>00: Disable<br>INT6 occurs at rising edge<br>01: TB0IN0 ↑<br>INT6 occurs at rising edge<br>10: TB0IN0 ↑ TB0IN0 ↓<br>INT6 occurs at falling edge<br>11: TA1OUT ↑<br>TA1OUT ↓<br>INT6 occurs at rising edge |         | Control<br>Up counter<br>0: Disable<br>1: Enable | TMRB0 source clock<br>00: TB0IN0 input<br>01: $\phi T1$<br>10: $\phi T4$<br>11: $\phi T16$ |         |

TMRB0 source clock

|             |    |                  |
|-------------|----|------------------|
| <TB0CLK1:0> | 00 | TB0IN0 pin input |
|             | 01 | $\phi T1$        |
|             | 10 | $\phi T4$        |
|             | 11 | $\phi T16$       |

Control clearing for up counter (UC10)

|          |   |                                         |
|----------|---|-----------------------------------------|
| <TB0CLE> | 0 | Disable                                 |
|          | 1 | Enable clearing by match with TB0RG1H/L |

Capture/interrupt timing

|             |    | Capture control                                                                                 | INT6 control                                                                                                                   |
|-------------|----|-------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|
| <TB0CPM1:0> | 00 | Disable                                                                                         | INT6 occurs at the rising edge of TB0IN0  |
|             | 01 | Capture to TB0CP0H/L at rising edge of TB0IN0                                                   |                                                                                                                                |
|             | 10 | Capture to TB0CP0H/L at rising edge of TB0IN0<br>Capture to TB0CP1H/L at falling edge of TB0IN0 | INT6 occurs at the rising edge of TB0IN0  |
|             | 11 | Capture to TB0CP0H/L at rising edge of TA1OUT<br>Capture to TB0CP1H/L at falling edge of TA1OUT | INT6 occurs at the rising edge of TB0IN0  |

Software capture

|           |   |                                                  |
|-----------|---|--------------------------------------------------|
| <TB0CP0I> | 0 | The value of up counter is captured to TB0CP0H/L |
|           | 1 | Undefined                                        |

Figure 3.13.4 Register for TMRB

| TMRB1 Mode Register |                   |   |                                                                 |                                                                                                                                                                                                                          |         |                                                  |                                                                                            |         |
|---------------------|-------------------|---|-----------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|--------------------------------------------------|--------------------------------------------------------------------------------------------|---------|
|                     | 7                 | 6 | 5                                                               | 4                                                                                                                                                                                                                        | 3       | 2                                                | 1                                                                                          | 0       |
| Bit symbol          | –                 | – | TB1CP0I                                                         | TB1CPM1                                                                                                                                                                                                                  | TB1CPM0 | TB1CLE                                           | TB1CLK1                                                                                    | TB1CLK0 |
| Read/Write          | R/W               |   | W*                                                              | R/W                                                                                                                                                                                                                      |         |                                                  |                                                                                            |         |
| Reset State         | 0                 | 0 | 1                                                               | 0                                                                                                                                                                                                                        | 0       | 0                                                | 0                                                                                          | 0       |
| Function            | Always write "0". |   | Software capture control<br>0: Software capture<br>1: Undefined | Capture timing<br>00: Disable<br>INT7 occurs at rising edge<br>01: TB1IN0 ↑<br>INT7 occurs at rising edge<br>10: TB1IN0 ↑ TB1IN0 ↓<br>INT7 occurs at falling edge<br>11: TA3OUT ↑ TA3OUT ↓<br>INT7 occurs at rising edge |         | Control<br>Up counter<br>0: Disable<br>1: Enable | TMRB1 source clock<br>00: TB1IN0 input<br>01: $\phi T1$<br>10: $\phi T4$<br>11: $\phi T16$ |         |

TB1MOD  
(1192H)  
A read-modify-write operation cannot be performed

TMRB1 source clock

|             |    |                  |
|-------------|----|------------------|
| <TB1CLK1:0> | 00 | TB1IN0 pin input |
|             | 01 | $\phi T1$        |
|             | 10 | $\phi T4$        |
|             | 11 | $\phi T16$       |

Control clearing for up counter (UC12)

|          |   |                                         |
|----------|---|-----------------------------------------|
| <TB1CLE> | 0 | Disable                                 |
|          | 1 | Enable clearing by match with TB1RG1H/L |

Capture/interrupt timing

|             |    | Capture control                                                                                 | INT7 control                                                                                                                   |
|-------------|----|-------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|
| <TB1CPM1:0> | 00 | Disable                                                                                         | INT7 occurs at the rising edge of TB1IN0  |
|             | 01 | Capture to TB1CP0H/L at rising edge of TB1IN0                                                   |                                                                                                                                |
|             | 10 | Capture to TB1CP0H/L at rising edge of TB1IN0<br>Capture to TB1CP1H/L at falling edge of TB1IN0 | INT7 occurs at the rising edge of TB1IN0  |
|             | 11 | Capture to TB1CP0H/L at rising edge of TA3OUT<br>Capture to TB1CP1H/L at falling edge of TA3OUT | INT7 occurs at the rising edge of TB1IN0  |

Software capture

|           |   |                                                  |
|-----------|---|--------------------------------------------------|
| <TB1CP0I> | 0 | The value of up counter is captured to TB1CP0H/L |
|           | 1 | Undefined                                        |

Figure 3.13.5 Register for TMRB

TMRB0 Flip-Flop Control Register

TB0FFCR  
(1183H)  
A read  
-modify-write  
operation  
cannot be  
performed

|             | 7                                              | 6 | 5                                                                   | 4                              | 3                                | 2                                | 1                                                                                                  | 0        |
|-------------|------------------------------------------------|---|---------------------------------------------------------------------|--------------------------------|----------------------------------|----------------------------------|----------------------------------------------------------------------------------------------------|----------|
| Bit symbol  | –                                              | – | TB0C1T1                                                             | TB0C0T1                        | TB0E1T1                          | TB0E0T1                          | TB0FF0C1                                                                                           | TB0FF0C0 |
| Read/Write  | W*                                             |   | R/W                                                                 |                                |                                  |                                  | W*                                                                                                 |          |
| Reset State | 1                                              | 1 | 0                                                                   | 0                              | 0                                | 0                                | 1                                                                                                  | 1        |
| Function    | Always write "11"<br><br>*Always read as "11". |   | TB0FF0 inversion trigger<br>0: Disable trigger<br>1: Enable trigger |                                |                                  |                                  | Control TB0FF0<br>00: Invert<br>01: Set<br>10: Clear<br>11: Undefined<br><br>*Always read as "11". |          |
|             |                                                |   | When capture UC10 to TB0CP1H/L                                      | When capture UC10 to TB0CP0H/L | When UC10 matches with TB0RG1H/L | When UC10 matches with TB0RG0H/L |                                                                                                    |          |

Timer flip-flop control(TB0FF0)

|              |    |                                 |
|--------------|----|---------------------------------|
| <TB0FF0C1:0> | 00 | Invert                          |
|              | 01 | Set to "11"                     |
|              | 10 | Clear to "00"                   |
|              | 11 | Undefined (Always read as "11") |

TB0FF0 control

Inverted when UC10 value matches the valued in TB0RG0H/L

|           |   |                 |
|-----------|---|-----------------|
| <TB0E0T1> | 0 | Disable trigger |
|           | 1 | Enable trigger  |

TB0FF0 control

Inverted when UC10 value matches the valued in TB0RG1H/L

|           |   |                 |
|-----------|---|-----------------|
| <TB0E1T1> | 0 | Disable trigger |
|           | 1 | Enable trigger  |

TB0FF0 control

Inverted when UC10 value is captured into TB0CP0H/L

|           |   |                 |
|-----------|---|-----------------|
| <TB0C0T1> | 0 | Disable trigger |
|           | 1 | Enable trigger  |

TB0FF0 control

Inverted when UC10 value is captured into TB0CP1H/L

|           |   |                 |
|-----------|---|-----------------|
| <TB0C1T1> | 0 | Disable trigger |
|           | 1 | Enable trigger  |

Figure 3.13.6 Register for TMRB

|                    |             | TMRB0 register |   |   |   |   |   |   |   |
|--------------------|-------------|----------------|---|---|---|---|---|---|---|
|                    |             | 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TB0RG0L<br>(1188H) | bit Symbol  | –              |   |   |   |   |   |   |   |
|                    | Read/Write  | W              |   |   |   |   |   |   |   |
|                    | Reset State | 0              |   |   |   |   |   |   |   |
| TB0RG0H<br>(1189H) | bit Symbol  | –              |   |   |   |   |   |   |   |
|                    | Read/Write  | W              |   |   |   |   |   |   |   |
|                    | Reset State | 0              |   |   |   |   |   |   |   |
| TB0RG1L<br>(118AH) | bit Symbol  | –              |   |   |   |   |   |   |   |
|                    | Read/Write  | W              |   |   |   |   |   |   |   |
|                    | Reset State | 0              |   |   |   |   |   |   |   |
| TB0RG1H<br>(118BH) | bit Symbol  | –              |   |   |   |   |   |   |   |
|                    | Read/Write  | W              |   |   |   |   |   |   |   |
|                    | Reset State | 0              |   |   |   |   |   |   |   |
| TB1RG0L<br>(1198H) | bit Symbol  | –              |   |   |   |   |   |   |   |
|                    | Read/Write  | W              |   |   |   |   |   |   |   |
|                    | Reset State | 0              |   |   |   |   |   |   |   |
| TB1RG0H<br>(1199H) | bit Symbol  | –              |   |   |   |   |   |   |   |
|                    | Read/Write  | W              |   |   |   |   |   |   |   |
|                    | Reset State | 0              |   |   |   |   |   |   |   |
| TB1RG1L<br>(119AH) | bit Symbol  | –              |   |   |   |   |   |   |   |
|                    | Read/Write  | W              |   |   |   |   |   |   |   |
|                    | Reset State | 0              |   |   |   |   |   |   |   |
| TB1RG1H<br>(119BH) | bit Symbol  | –              |   |   |   |   |   |   |   |
|                    | Read/Write  | W              |   |   |   |   |   |   |   |
|                    | Reset State | 0              |   |   |   |   |   |   |   |

Note: A read-modify-write operation cannot be performed for All registers.

Figure 3.13.7 Register for TMRB

### 3.13.4 Operation in Each Mode

#### (1) 16 bit timer mode

Generating interrupts at fixed intervals

In this example, the interrupt INTTB01 is set to be generated at fixed intervals. The interval time is set in the timer register TB0RG1H/L.

|           |   | 7 | 6 | 5 | 4 | 3                 | 2 | 1 | 0 |                                                                      |
|-----------|---|---|---|---|---|-------------------|---|---|---|----------------------------------------------------------------------|
| TB0RUN    | ← | – | 0 | X | X | –                 | – | X | 0 | Stop TMRB0                                                           |
|           | ← | X | 1 | 0 | 0 | X                 | 0 | 0 | 0 | Enable INTTB01 and set interrupt level 4.                            |
|           |   |   |   |   |   |                   |   |   |   | Disable INTTB00                                                      |
| TB0FFCR   | ← | 1 | 1 | 0 | 0 | 0                 | 0 | 1 | 1 | Disable the trigger                                                  |
| TB0MOD    | ← | 0 | 0 | 1 | 0 | 0                 | 1 | * | * | Select internal clock for input and<br>disable the capture function. |
|           |   |   |   |   |   | (** = 01, 10, 11) |   |   |   |                                                                      |
| TB0RG1H/L | ← | * | * | * | * | *                 | * | * | * | Set the interval time<br>(16 bits).                                  |
|           |   |   |   |   |   |                   |   |   |   |                                                                      |
| TB0RUN    | ← | – | 0 | X | X | –                 | 1 | X | 1 | Start TMRB0.                                                         |

X: Don't care, –: No change

X: Don't care, –: No change

#### (2) 16 bit event counter mode

In 16 bit timer mode as described in above, the timer can be used as an event counter by selecting the external clock (TB0IN0 pin input) as the input clock. Up counter (UC10) counts up at the rising edge of TB0IN0 input. To read the value of the counter, first perform “software capture” once and read the captured value.

|           | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |                                           |
|-----------|---|---|---|---|---|---|---|---|---|-------------------------------------------|
| TB0RUN    | ← | – | 0 | X | X | – | – | X | 0 | Stop TMRB0                                |
| PPCR      | ← | X | X | – | 1 | – | – | – | X | Set PP4 to input mode for TB0IN0          |
| PPFC      | ← | – | – | – | 1 | – | – | – | X |                                           |
| INTETB0   | ← | X | 1 | 0 | 0 | X | 0 | 0 | 0 | Enable INTTB01 and sets interrupt level 4 |
|           |   |   |   |   |   |   |   |   |   | Disable INTTB00                           |
| TB0FFCR   | ← | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | Disable trigger                           |
| TB0MOD    | ← | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | Select TB0IN0 as the input clock          |
| TB0RG1H/L | ← | * | * | * | * | * | * | * | * | Set the number of counts                  |
|           |   | * | * | * | * | * | * | * | * | (16 bit)                                  |
| TB0RUN    | ← | – | 0 | X | X | – | 1 | X | 1 | Start TMRB0                               |

X: Don't care, –: No change

X: Don't care, –: No change

When used as an event counter, set the prescaler in RUN mode.

(TB0RUN <TB0PRUN> = “1”)

(3) 16-bit programmable pulse generation (PPG) output mode

Square wave pulses can be generated at any frequency and duty ratio. The output pulse may be either low active or high active.

The PPG mode is obtained by inversion of the timer flip-flop TB0FF0 that is enabled by the match of the up counter UC10 with timer register TB0RG0H/L or TB0RG1H/L and is output to TB0OUT0. In this mode the following conditions must be satisfied.

$$(\text{Value set in TB0RG0H/L}) < (\text{Value set in TB0RG1H/L})$$

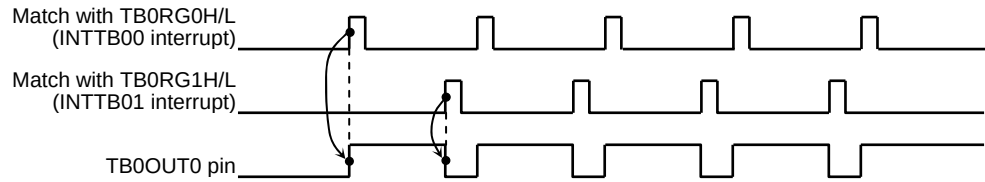


Figure 3.13.8 Programmable Pulse Generation (PPG) Output Waveforms

When the TB0RG0H/L double buffer is enabled in this mode, the value of register buffer 10 will be shifted into TB0RG0H/L at match with TB0RG1H/L. This feature facilitates the handling of low-duty waves.

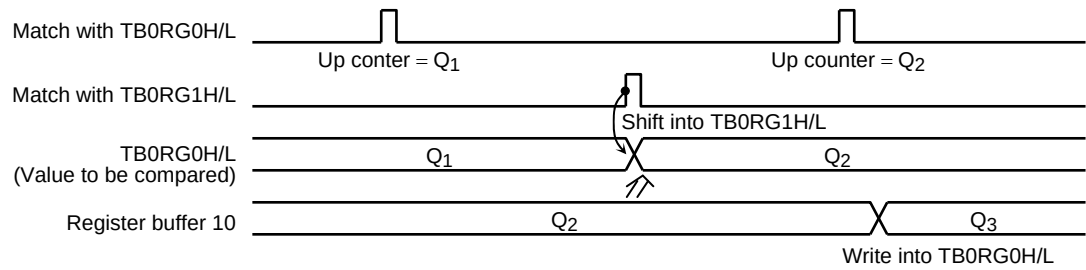


Figure 3.13.9 Operation of double buffer

Note: The values that can be set in TBxRGxH/L range from 0001h to 0000h (equivalent to 10000h). If the maximum value 000h is set, the match-detect signal goes active when the up-counter overflows.

The following block diagram illustrates this mode.

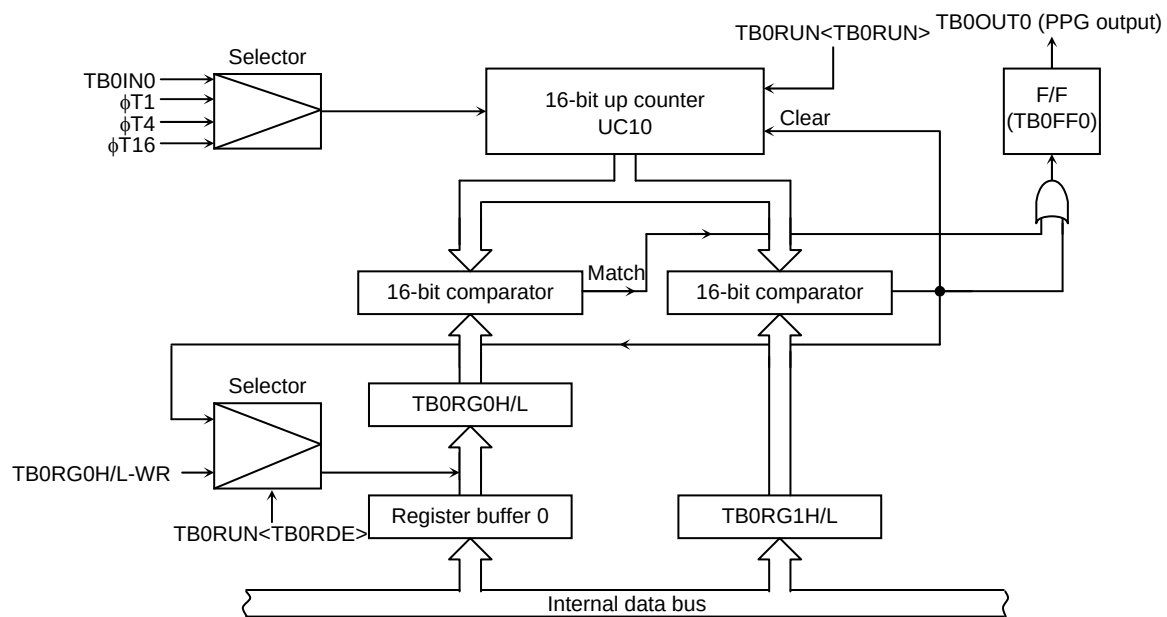


Figure 3.13.10 Block Diagram of 16-Bit Mode

The following example shows how to set 16-bit PPG output mode:

|                   |           | 7         | 6      | 5 | 4 | 3 | 2 | 1 | 0 |                                                                                                                      |   |                               |
|-------------------|-----------|-----------|--------|---|---|---|---|---|---|----------------------------------------------------------------------------------------------------------------------|---|-------------------------------|
| TB0RUN            | ←         | 0         | 0      | X | X | — | — | X | 0 | Disable the TB0RG0H/L double buffer and stop TMRB0.<br>Set the duty ratio<br>(16 bit)                                |   |                               |
|                   | TB0RG0H/L | ←         | *      | * | * | * | * | * | * |                                                                                                                      | * |                               |
|                   |           | TB0RG1H/L | ←      | * | * | * | * | * | * |                                                                                                                      | * | Set the frequency<br>(16 bit) |
|                   |           |           | TB0RUN | ← | 1 | 0 | X | X | — |                                                                                                                      | 0 |                               |
| TB0FFCR           | ←         | X         | X      | 0 | 0 | 1 | 1 | 1 | 0 | Set the mode to invert TB0FF0 at the match with TB0RG0H/L/TB0RG1H/L. Set TB0FF0 to 0.                                |   |                               |
| TB0MOD            | ←         | 0         | 0      | 1 | 0 | 0 | 1 | * | * | Select the internal clock as the input clock and disable the capture function.<br><br>Set PP6 to function as TB0OUT0 |   |                               |
| (**) = 01, 10, 11 |           |           |        |   |   |   |   |   |   |                                                                                                                      |   |                               |
| PPFC              | ←         | —         | 1      | — | — | — | — | — | X | Start TMRB0.                                                                                                         |   |                               |
| TB0RUN            | ←         | 1         | 0      | X | X | — | 1 | X | 1 |                                                                                                                      |   |                               |

X: Don't care, —: No change

X: Don't care, —: No change



## (4) Application examples of capture function

Used capture function, they can be applied in many ways, for example;

1. One-shot pulse output from external trigger pulse
2. Frequency measurement
3. Pulse width measurement

1. One-shot pulse output from external trigger pulse

Set the up counter UC10 in free-running mode with the internal input clock, input the external trigger pulse from TB0IN0 pin, and load the value of up counter into capture register TB0CP0H/L at the rising edge of the TB0IN0 pin.

When the interrupt INT6 is generated at the rising edge of TB0IN0 input, set the TB0CP0H/L value (c) plus a delay time (d) to TB0RG0H/L ( $=c+d$ ), and set the above set value (c+d) plus a one-shot pulse width (p) to TB0RG1H/L ( $=c+d+p$ ).

The TB0FFCR<TB0E1T1, TB0E0T1> register should be set “11” and that the TB0FF0 inversion is enabled only when the up counter value matches TB0RG0H/L or TB0RG1H/L. When interrupt INTTB01 occurs, this inversion will be disabled after one-shot pulse is output.

The (c), (d) and (p) correspond to c, d, and p in the Figure 3.13.11.

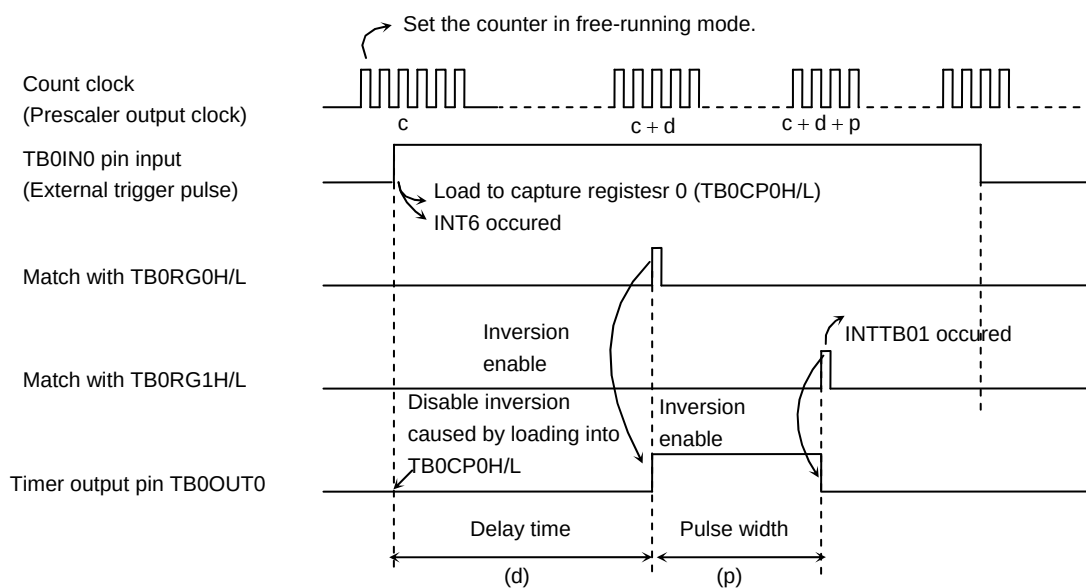


Figure 3.13.11 One-shot Pulse Output (with delay)

Example: To output 2ms one-shot pulse with 3ms delay to the external trigger pulse to TB0IN0 pin

\*Clock state

System clock :  $f_{sys}$   
Prescaler clock :  $f_{sys}/4$

#### Main setting

|         |   |   |   |   |   |   |   |   |   |                                                                                             |
|---------|---|---|---|---|---|---|---|---|---|---------------------------------------------------------------------------------------------|
| TB0MOD  | ← | X | X | 1 | 0 | 1 | 0 | 0 | 1 | Free-running<br>Count with $\phi T1$                                                        |
| TB0FFCR | ← | X | X | 0 | 0 | 0 | 0 | 1 | 0 | Load to TB0CP0H/L at the rising edge of TB0IN0                                              |
| PPFC    | ← | - | 1 | - | - | - | - | - | X | Clear TB0FF0 to "0"<br>Disable TB0FF0 inversion<br>Select PP6 as TB0OUT0 pin (port setting) |
| INTE56  | ← | X | 1 | 0 | 0 | X | - | - | - | Enable INT6                                                                                 |
| INTETB0 | ← | X | 0 | 0 | 0 | X | 0 | 0 | 0 | Disable INTTB00, INTTB01                                                                    |
| TB0RUN  | ← | - | 0 | X | X | - | 1 | X | 1 | Start TMRB0                                                                                 |

#### Setting in INT6 routine

|           |   |                            |   |   |   |   |   |   |   |                                                                                  |
|-----------|---|----------------------------|---|---|---|---|---|---|---|----------------------------------------------------------------------------------|
| TB0RG0H/L | ← | TB0CP0H/L + 3ms/ $\phi T1$ |   |   |   |   |   |   |   |                                                                                  |
| TB0RG1H/L | ← | TB0RG0H/L + 2ms/ $\phi T1$ |   |   |   |   |   |   |   |                                                                                  |
| TB0FFCR   | ← | X                          | X | - | - | 1 | 1 | - | - | Enable TB0FF0 inversion when the up counter value matches TB0RG0H/L or TB0RG1H/L |
| INTETB0   | ← | X                          | 1 | 0 | 0 | X | 0 | 0 | 0 | Enable INTTB01                                                                   |

#### Setting in INTTB01 routine

|         |   |   |   |   |   |   |   |   |   |                                                                                   |
|---------|---|---|---|---|---|---|---|---|---|-----------------------------------------------------------------------------------|
| TB0FFCR | ← | X | X | - | - | 0 | 0 | - | - | Disable TB0FF0 inversion when the up counter value matches TB0RG0H/L or TB0RG1H/L |
| INTETB0 | ← | X | 0 | 0 | 0 | X | 0 | 0 | 0 | Disable INTTB01                                                                   |

X: Don't care, -: No change

When delay time is unnecessary, invert timer flip-flop TB0FF0 when the up counter value is loaded into capture register (TB0CP0H/L), and set the TB0CP0H/L value (c) plus the one-shot pulse width (p) to TB0RG1H/L when the interrupt INT6 occurs. The TB0FF0 inversion should be enabled when the up counter (UC10) value matched TB0RG1H/L, and disabled when generating the interrupt INTTB01.

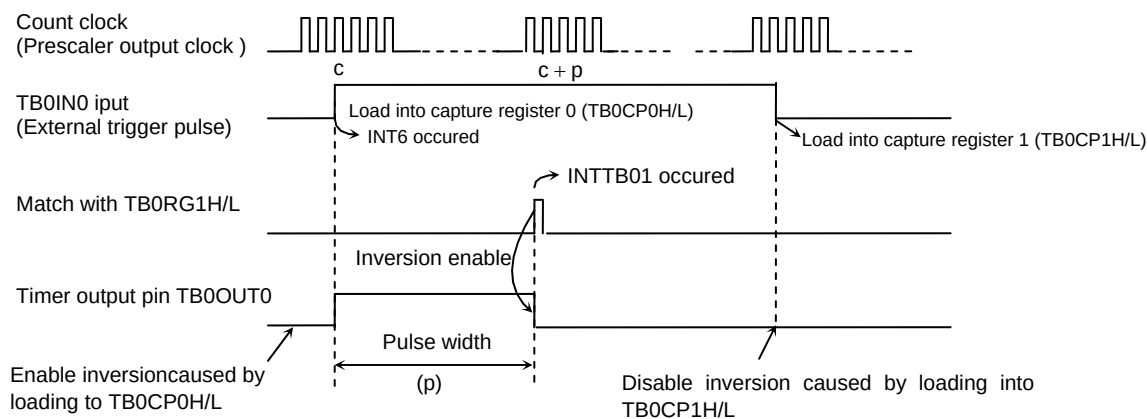


Figure 3.13.12 One-shot Pulse Output (without delay)

## 2. Frequency measurement

The frequency of the external clock can be measured in this mode. The clock is input through the TB0IN0 pin, and its frequency is measured by the 8 bit timers TMRA01 and the 16 bit timer/event counter (TMRB0).

The TB0IN0 pin input should be selected for the input clock of TMRB0. Set to TB0MOD<TB0CPM1:0>="11". The value of the up counter is loaded into the capture register TB0CP0H/L at the rising edge of the timer flip-flop TA1FF of 8bit timers (TMRA01), and TB0CP1H/L at its falling edge.

The frequency is calculated by the difference between the loaded values in TB0CP0H/L and TB0CP1H/L when the interrupt (INTTA0 or INTTA1) is generated by either 8 bit timer.

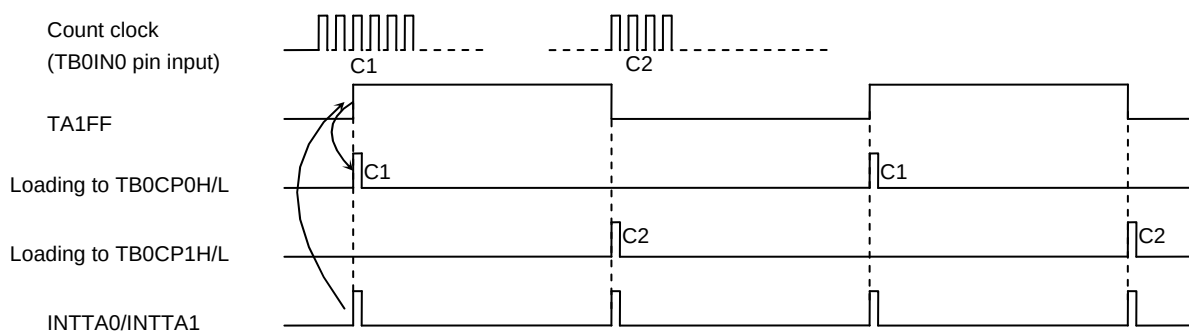


Figure 3.13.13 Frequency Measurement

For example, if the value for the level 1 width of TA1FF of the 8 bit timer is set to 0.5[s] and the difference between TB0CP0H/L and TB0CP1H/L is 100, the frequency will be  $100/0.5[s] = 200[Hz]$ .

Note: The frequency in this example is calculated with 50% duty.

### 3. Pulse width measurement

This mode allows measuring the H level width of an external pulse. While keeping the 16 bit timer/event counter counting (free-running) with the internal clock input, the external pulse is input through the TB0IN0 pin. Then the capture function is used to load the UC10 values into TB0CP0H/L and TB0CP1H/L at the rising edge and falling edge of the external trigger pulse respectively. The interrupt INT6 occurs at the falling edge of TB0IN0.

The pulse width is obtained from the difference between the values of TB0CP0H/L and TB0CP1H/L and the internal clock cycle.

For example, if the internal clock is 0.8[us] and the difference between TB0CP0H/L and TB0CP1H/L is 100, the pulse width will be  $100 \times 0.8[\mu\text{s}] = 80\mu\text{s}$

Additionally, the pulse width which is over the UC10 maximum count time specified by the clock source can be measured by changing software.

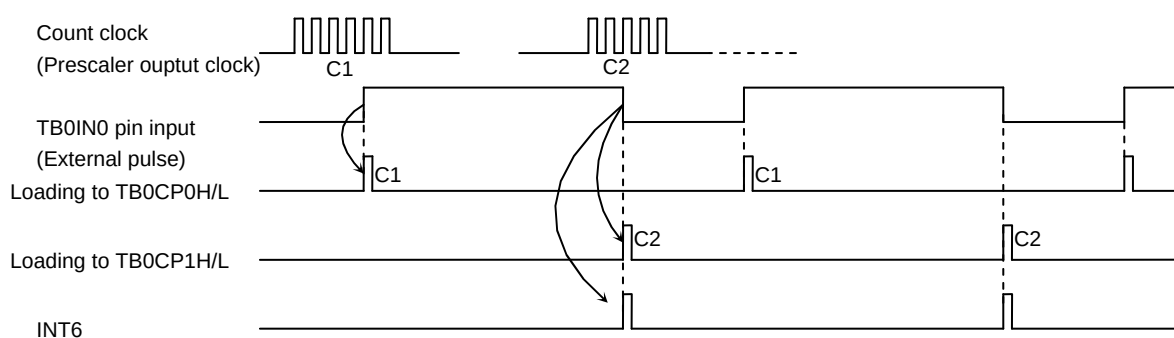


Figure 3.13.14 Pulse Width Measurement

Note: Only in this pulse width measuring mode(TB0MOD<TB0CPM1:0>= "10"), external interrupt INT6 occurs at the falling edge of TB0IN0 pin input. In other modes, it occurs at the rising edge.

The width of L level can be measured by multiplying the difference between the first C1 and the second C0 at the second INT6 interrupt and the internal clock cycle together.

### 3.14 Serial Channels (SIO)

The TMP92CF30 include 2 serials I/O channel (SIO0 and SIO1). For channels either UART mode (Asynchronous transmission) or I/O interface mode (Synchronous transmission) can be selected. And, SIO0 and SIO1 include data modulator that supports the IrDA 1.0 infrared data communication specification.

- I/O interface mode — Mode 0: For transmitting and receiving I/O data using the synchronizing signal SCLK for extending I/O.
- UART mode — Mode 1: 7-bit data  
                                   Mode 2: 8-bit data  
                                   Mode 3: 9-bit data

In mode 1 and mode 2, a parity bit can be added. Mode 3 has a wakeup function for making the master controller start slave controllers via a serial link (A multi-controller system).

Figure 3.14.1 is block diagrams for each channel.

Each channel is compounded mainly prescaler, serial clock generation circuit, receiving buffer and control circuit, transmission buffer and control circuit.

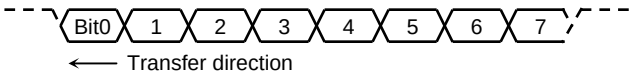
Each channel can be used independently.

Each channel operates in the same fashion except for the following points; hence only the operation of channel 0 is explained below.

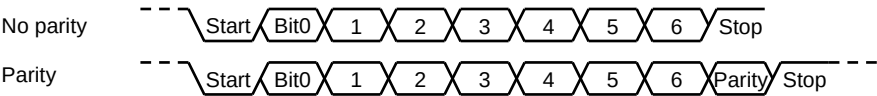
Table 3.14.1 Differences between Channels 0 to 1

|           | Channel 0                                                                               | Channel 1                                                                               |
|-----------|-----------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| Pin name  | TXD0 (P90 or PP3)<br>RXD0 (P91 or PP4)<br>$\overline{\text{CTS0}}$ , SCLK0 (P92 or PP5) | TXD1 (P90 or PP3)<br>RXD1 (P91 or PP4)<br>$\overline{\text{CTS1}}$ , SCLK1 (P92 or PP5) |
| IrDA mode | Yes                                                                                     | Yes                                                                                     |

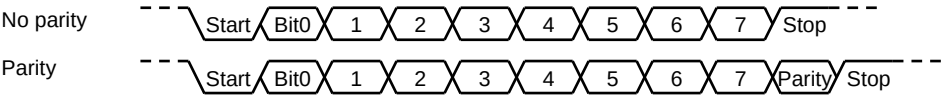
- Mode 0 (I/O interface mode)



- Mode 1 (7-bit UART mode)



- Mode 2 (8-bit UART mode)



- Mode 3 (9-bit UART mode)

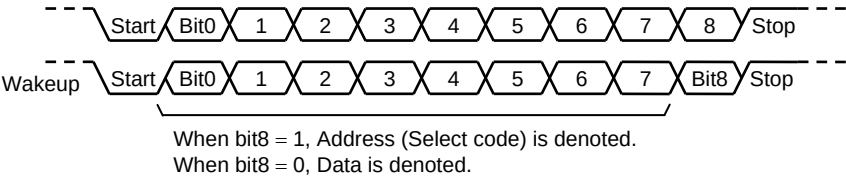


Figure 3.14.1 Data Formats

## 3.14.1 Block Diagram

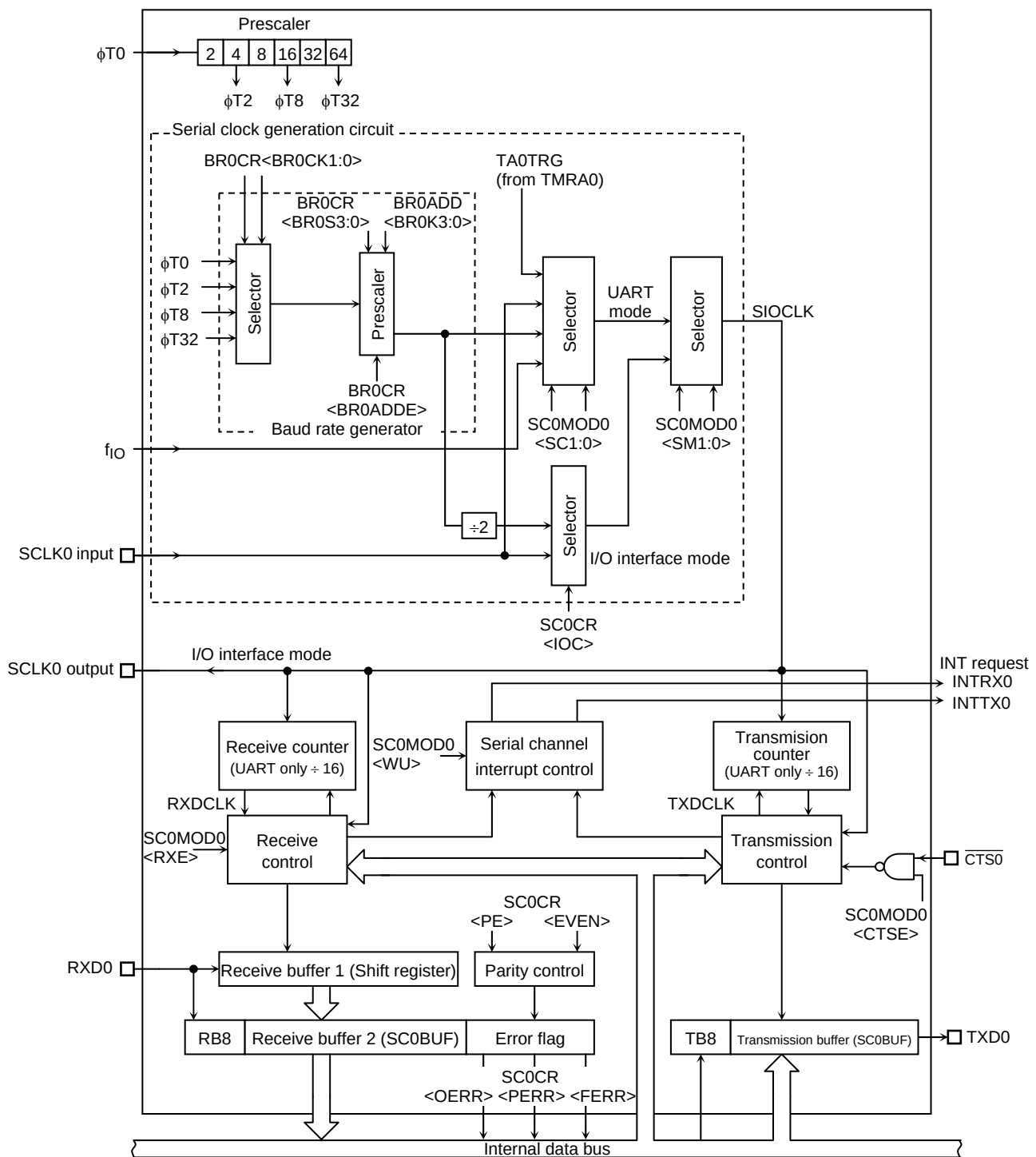


Figure 3.14.2 SIO0 Block Diagram

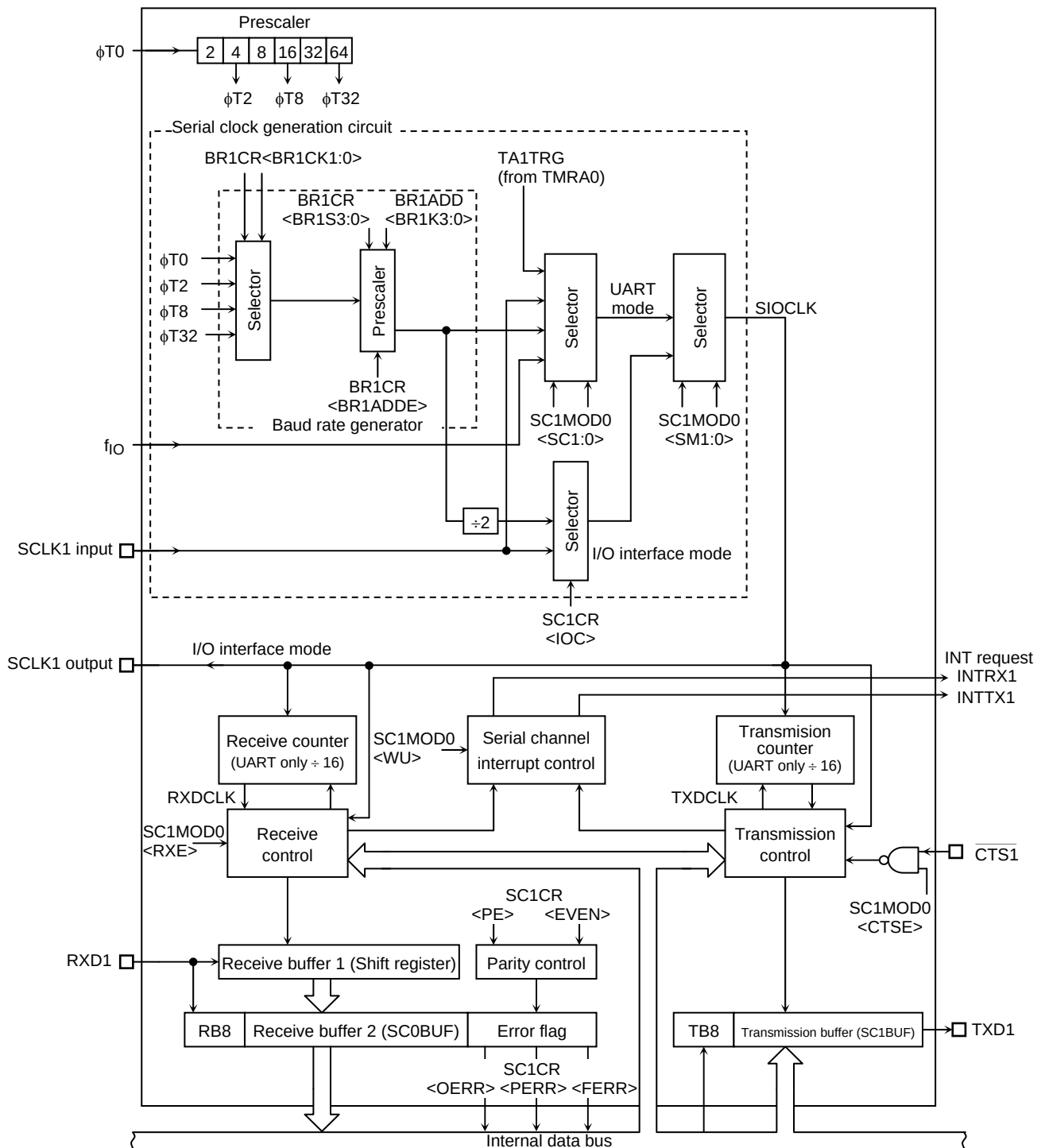


Figure 3.14.3 SIO1 Block Diagram



## 3.14.1.1 Block Diagram

Figure 3.14.4 shows the connection image for SIO circuits in TMP92CF30.

SIO circuit are built-in 2ch, it can set each signal to P90, P91, P92 or PP3, PP4, PP5.

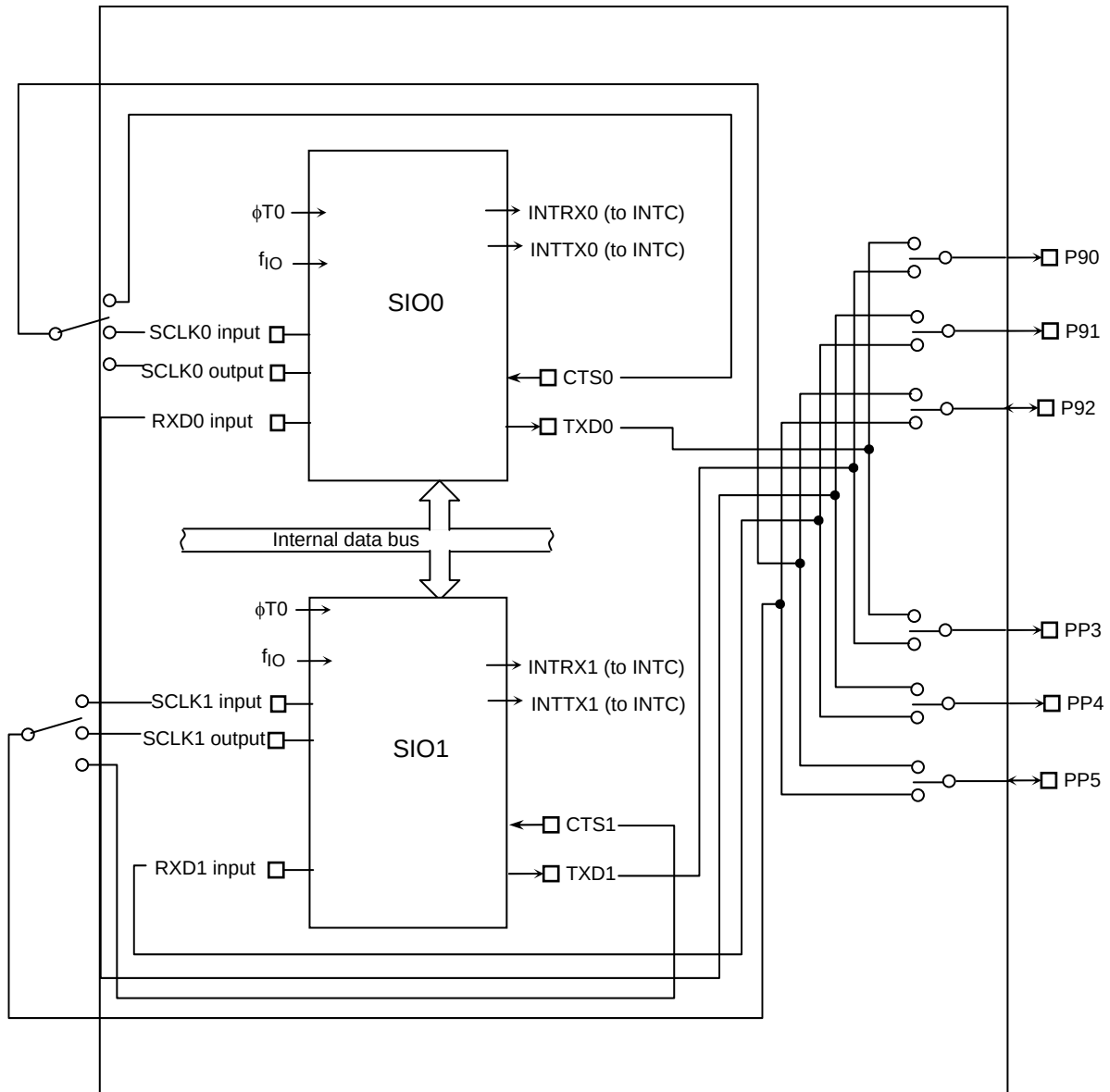


Figure 3.14.4 Connection images of internal circuit and external port

Note1: Figure 3.14.4 shows connection image. The circuit compounds and a setting procedure Refer to section of Port.

Note2: When shifting external port, shift port after stop internal circuits completely.

### 3.14.2 Operation of Each Circuit

#### (1) Prescaler

There is a 6-bit prescaler for generating a clock to SIO0. The prescaler can be run by selecting the baud rate generator as the serial transfer clock.

Table 3.14.2 shows prescaler clock resolution into the baud rate generator.

Table 3.14.2 Prescaler Clock Resolution to Baud Rate Generator

| –  | Clock gear<br>SYSCR1<br><GEAR2:0> | –   | Baud Rate Generator input clock<br>SIO Prescaler<br>BR0CR<BR0CK1:0> |                |                 |                  |
|----|-----------------------------------|-----|---------------------------------------------------------------------|----------------|-----------------|------------------|
|    |                                   |     | $\phi T0(1/1)$                                                      | $\phi T2(1/4)$ | $\phi T8(1/16)$ | $\phi T32(1/64)$ |
| fc | 000(1/1)                          | 1/4 | fc/4                                                                | fc/16          | fc/64           | fc/256           |
|    | 001(1/2)                          |     | fc/8                                                                | fc/32          | fc/128          | fc/512           |
|    | 010(1/4)                          |     | fc/16                                                               | fc/64          | fc/256          | fc/1024          |
|    | 011(1/8)                          |     | fc/32                                                               | fc/128         | fc/512          | fc/2048          |
|    | 100(1/16)                         |     | fc/64                                                               | fc/256         | fc/1024         | fc/4096          |

The baud rate generator selects between 4-clock inputs:  $\phi T0$ ,  $\phi T2$ ,  $\phi T8$ , and  $\phi T32$  among the prescaler outputs.

## (2) Baud rate generator

The baud rate generator is the circuit which generates transmission/receiving clock and determines the transfer rate of the serial channels.

The input clock to the baud rate generator,  $\phi T0$ ,  $\phi T2$ ,  $\phi T8$  or  $\phi T32$ , is generated by the 6-bit prescaler which is shared by the timers. One of these input clocks is selected using the  $BR0CR<BR0CK1:0>$  field in the baud rate generator control register.

The baud rate generator includes a frequency divider, which divides the frequency by 1 or  $N + (16 - K)/16$  to 16 values, thereby determining the transfer rate.

The transfer rate is determined by the settings of  $BR0CR<BR0ADDE, BR0S3:0>$  and  $BR0ADD<BR0K3:0>$ .

<In UART mode>

When  $BR0CR<BR0ADDE> = "0"$

The settings  $BR0ADD<BR0K3:0>$  are ignored. The baud rate generator divides the selected prescaler clock by N, which is set in  $BR0CK<BR0S3:0>$ . (N = 1, 2, 3 ... 16)

When  $BR0CR<BR0ADDE> = "1"$

The  $N + (16 - K)/16$  division function is enabled. The baud rate generator divides the selected prescaler clock by  $N + (16 - K)/16$  using the value of N set in  $BR0CR<BR0S3:0>$  (N = 2, 3 ... 15) and the value of K set in  $BR0ADD<BR0K3:0>$  (K = 1, 2, 3 ... 15)

Note: If N = 1 or N = 16, the  $N + (16 - K)/16$  division function is disabled. Clear  $BR0CR<BR0ADDE>$  to "0".

<In I/O interface mode>

The  $N + (16 - K)/16$  division function is not available in I/O interface mode. Clear  $BR0CR<BR0ADDE>$  to "0" before dividing by N.

The method for calculating the transfer rate when the baud rate generator is used is explained below.

- In UART mode

$$\text{Baud rate} = \frac{\text{Input clock of baud rate generator}}{\text{Frequency divider for baud rate generator}} \div 16$$

- In I/O interface mode

$$\text{Baud rate} = \frac{\text{Input clock of baud rate generator}}{\text{Frequency divider for baud rate generator}} \div 2$$

## &lt;Integer divider (N divider)&gt;

For example, when the source clock frequency ( $f_c$ ) is 19.6608 MHz, the input clock is  $\phi T_2$ , the frequency divider N (BR0CR<BR0S3:0>) = 8, and BR0CR<BR0ADDE> = "0", the baud rate in UART Mode is as follows:

$$\begin{aligned}
 \text{*Clock state} & \left[ \begin{array}{ll} \text{Clock gear} & : 1/1 \end{array} \right. \\
 \text{Baud Rate} &= \frac{\text{Input clock of baud rate generator}}{\text{Frequency divider for baud rate generator}} \div 16 \\
 &= \frac{f_c/16}{8} \div 16 \\
 &= 19.6608 \times 10^6 \div 16 \div 8 \div 16 = 9600 \text{ (bps)}
 \end{aligned}$$

Note: The  $N + (16 - K) / 16$  division function is disabled and setting BR0ADD <BR0K3:0> is invalid.

## &lt;N+(16-K)/16 divider (UART Mode only)&gt;

Accordingly, when the source clock frequency ( $f_c$ ) = 15.9744 MHz, the input clock is  $\phi T_2$ , the frequency divider N (BR0CR<BR0S3:0>) = 6, K (BR0ADD<BR0K3:0>) = 8, and BR0CR <BR0ADDE> = "1", the baud rate in UART Mode is as follows:

$$\begin{aligned}
 \text{* Clock state} & \left[ \begin{array}{ll} \text{Clock gear} & : 1/1 \end{array} \right. \\
 \text{Baud Rate} &= \frac{\text{Input clock of baud rate generator}}{\text{Frequency divider for baud rate generator}} \div 16 \\
 &= \frac{f_c/16}{6 + \frac{(16-8)}{16}} \div 16 \\
 &= 15.9744 \times 10^6 \div 16 \div \left(6 + \frac{8}{16}\right) \div 16 = 9600 \text{ (bps)}
 \end{aligned}$$

Table 3.14.3 show examples of UART Mode transfer rates.

Additionally, the external clock input is available in the serial clock. (Serial Channel 0). The method for calculating the baud rate is explained below:

- In UART Mode

Baud rate = external clock input frequency  $\div 16$

It is necessary to satisfy (external clock input cycle)  $\geq 4/f_{\text{sys}}$

- In I/O Interface Mode

Baud rate = external clock input frequency

It is necessary to satisfy (external clock input cycle)  $\geq 16/f_{\text{sys}}$

Table 3.14.3 Transfer Rate Selection  
(When baud rate generator is used and BR0CR<BR0ADDE> = "0")

Unit (kbps)

| f <sub>SYS</sub> [MHz] | Input Clock         |  | φT0                   | φT2                    | φT8                    | φT32                    |
|------------------------|---------------------|--|-----------------------|------------------------|------------------------|-------------------------|
|                        | Frequency Divider N |  | (f <sub>SYS</sub> /4) | (f <sub>SYS</sub> /16) | (f <sub>SYS</sub> /64) | (f <sub>SYS</sub> /256) |
| 7.3728                 | 1                   |  | 115.200               | 28.800                 | 7.200                  | 1.800                   |
| ↑                      | 3                   |  | 38.400                | 9.600                  | 2.400                  | 0.600                   |
| ↑                      | 6                   |  | 19.200                | 4.800                  | 1.200                  | 0.300                   |
| ↑                      | A                   |  | 11.520                | 2.880                  | 0.720                  | 0.180                   |
| ↑                      | C                   |  | 9.600                 | 2.400                  | 0.600                  | 0.150                   |
| ↑                      | F                   |  | 7.680                 | 1.920                  | 0.480                  | 0.120                   |
| 9.8304                 | 1                   |  | 153.600               | 38.400                 | 9.600                  | 2.400                   |
| ↑                      | 2                   |  | 76.800                | 19.200                 | 4.800                  | 1.200                   |
| ↑                      | 4                   |  | 38.400                | 9.600                  | 2.400                  | 0.600                   |
| ↑                      | 5                   |  | 30.720                | 7.680                  | 1.920                  | 0.480                   |
| ↑                      | 8                   |  | 19.200                | 4.800                  | 1.200                  | 0.300                   |
| ↑                      | 0                   |  | 9.600                 | 2.400                  | 0.600                  | 0.150                   |
| 44.2368                | 6                   |  | 115.20                | 28.800                 | 7.200                  | 1.800                   |
| ↑                      | 9                   |  | 76.800                | 19.200                 | 4.800                  | 1.200                   |
| 58.9824                | 2                   |  | 460.800               | 115.200                | 28.800                 | 7.200                   |
| ↑                      | 3                   |  | 307.200               | 76.800                 | 19.200                 | 4.800                   |
| ↑                      | 5                   |  | 184.320               | 46.080                 | 11.520                 | 2.880                   |
| ↑                      | 6                   |  | 153.600               | 38.400                 | 9.600                  | 2.400                   |
| ↑                      | 8                   |  | 115.200               | 28.800                 | 7.200                  | 1.800                   |
| ↑                      | C                   |  | 76.800                | 19.200                 | 4.800                  | 1.200                   |
| ↑                      | F                   |  | 61.440                | 15.360                 | 3.840                  | 0.960                   |
| 73.728                 | 1                   |  | 1152.000              | 288.000                | 72.000                 | 18.000                  |
| ↑                      | 3                   |  | 384.000               | 96.000                 | 24.000                 | 6.000                   |
| ↑                      | 6                   |  | 192.000               | 48.000                 | 12.000                 | 3.000                   |
| ↑                      | A                   |  | 115.200               | 28.800                 | 7.200                  | 1.800                   |
| ↑                      | C                   |  | 96.000                | 24.000                 | 6.000                  | 1.500                   |
| ↑                      | F                   |  | 76.800                | 19.200                 | 4.800                  | 1.200                   |

Note1: Transfer rates in I/O interface mode are eight times faster than the values given above.

In UART mode, TMRA match detect signal (TA0TRG) can be used for serial transfer clock.

Method for calculating the timer output frequency which is needed when outputting trigger of timer

$$\text{TA0TRG frequency} = \text{Baud rate} \times 16$$

Note2: The TMRA0 match detect signal cannot be used as the transfer clock in I/O Interface mode.

(3) Serial clock generation circuit

This circuit generates the basic clock for transmitting and receiving data.

- In I/O Interface Mode

In SCLK Output Mode with the setting SC0CR<IOC> = “0”, the basic clock is generated by dividing the output of the baud rate generator by 2, as described previously.

In SCLK Input Mode with the setting SC0CR<IOC> = “1”, the rising edge or falling edge will be detected according to the setting of the SC0CR<SCLKS> register to generate the basic clock.

- In UART Mode

The SC0MOD0 <SC1:0> setting determines whether the baud rate generator clock, the internal clock  $f_{i0}$ , the match detect signal from timer TMRA0 or the external clock (SCLK0) is used to generate the basic clock SIOCLK.

(4) Receiving counter

The receiving counter is a 4-bit binary counter used in UART Mode, which counts up the pulses of the SIOCLK clock. It takes 16 SIOCLK pulses to receive 1 bit of data; each data bit is sampled three times - on the 7th, 8th and 9th clock cycles.

The value of the data bit is determined from these three samples using the majority rule.

For example, if the data bit is sampled respectively as “1”, “0” and “1” on 7th, 8th and 9th clock cycles, the received data bit is taken to be 1. A data bit sampled as “0”, “0” and “1” is taken to be “0”.

(5) Receiving control

- In I/O Interface Mode

In SCLK Output Mode with the setting SC0CR<IOC> = “0”, the RXD0 signal is sampled on the rising or falling edge of the shift clock which is output on the SCLK0 pin, according to the SC0CR<SCLKS> setting.

In SCLK Input Mode with the setting SC0CR<IOC> = “1”, the RXD0 signal is sampled on the rising or falling edge of the SCLK0 input, according to the SC0CR<SCLKS> setting

- In UART Mode

The receiving control block has a circuit, which detects a start bit using the majority rule. Received bits are sampled three times; when two or more out of three samples are 0, the bit is recognized as the start bit and the receiving operation commences.

The values of the data bits that are received are also determined using the majority rule.

## (6) The Receiving Buffers

To prevent Overrun errors, the Receiving Buffers are arranged in a double-buffer structure.

Received data is stored one bit at a time in Receiving Buffer 1 (which is a shift register). When 7 or 8 bits of data have been stored in Receiving Buffer 1, the stored data is transferred to Receiving Buffer 2 (SC0BUF); this causes an INTRX0 interrupt to be generated. The CPU only reads Receiving Buffer 2 (SC0BUF). Even before the CPU reads receiving Buffer 2 (SC0BUF), the received data can be stored in Receiving Buffer 1. However, unless Receiving Buffer 2 (SC0BUF) is read before all bits of the next data are received by Receiving Buffer 1, an overrun error occurs. If an Overrun error occurs, the contents of Receiving Buffer 1 will be lost, although the contents of Receiving Buffer 2 and SC0CR<RB8> will be preserved.

SC0CR<RB8> is used to store either the parity bit - added in 8-Bit UART Mode - or the most significant bit (MSB) - in 9-Bit UART Mode.

In 9-Bit UART Mode the wake-up function for the slave controller is enabled by setting SC0MOD0<WU> to "1"; in this mode INTRX0 interrupts occur only when the value of SC0CR<RB8> is "1".

SIO interrupt mode is selectable by the register SIMC.

Note1: The double buffer structure does not support SC0CR<RB8>.

Note2: If the CPU reads receive buffer 2 while data is being transferred from receive buffer 1 to receive buffer 2, the data may not be read properly. To avoid this situation, a read of receive buffer 2 should be triggered by a receive interrupt.

## (7) Notes for Using Receive Interrupts

- Receive interrupts can be detected either in level or edge mode. For details, see the description of the SIO/SEI receive interrupt mode select register SIMC in the section on interrupts.
- When receive interrupts are set to level mode, once an interrupt occurs, the same interrupt will occur repeatedly even after control has jumped to the interrupt routine unless interrupts are disabled.

## (8) Transmission counters

The transmission counter is a 4-bit binary counter used in UART Mode and which, like the receiving counter, counts the SIOCLK clock pulses; a TXDCLK pulse is generated every 16 SIOCLK clock pulses.

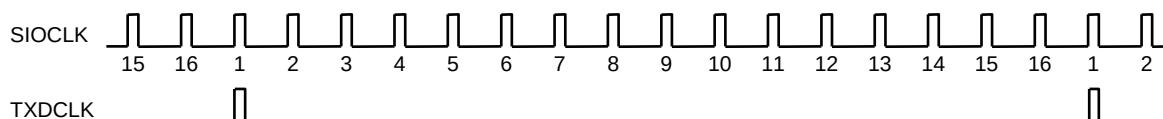


Figure 3.14.5 Generation of the transmission clock

## (9) Transmission controller

- In I/O Interface Mode

In SCLK Output Mode with the setting SC0CR<IOC> = “0”, the data in the Transmission Buffer is output one bit at a time to the TXD0 pin on the rising edge or falling of the shift clock which is output on the SCLK0 pin, according to the SC0CR<SCLKS> setting.

In SCLK Input Mode with the setting SC0CR<IOC> = “1”, the data in the Transmission Buffer is output one bit at a time on the TXD0 pin on the rising or falling edge of the SCLK0 input, according to the SC0CR<SCLKS> setting.

- In UART Mode

When transmission data sent from the CPU is written to the Transmission Buffer, transmission starts on the rising edge of the next TXDCLK.



### Handshake function

Use of  $\overline{\text{CTS0}}$  pin allows data can to be sent in units of one frame; thus, overrun errors can be avoided. The handshake functions is enabled or disabled by the SC0MOD<CTSE> setting.

When the  $\overline{\text{CTS0}}$  pin goes high on completion of the current data send, data transmission is halted until the  $\overline{\text{CTS0}}$  pin goes low again. However, the INTTX0 interrupt is generated, and it requests the next data send to from the CPU. The next data is written in the transmission buffer and data sending is halted.

Though there is no  $\overline{\text{RTS}}$  pin, a handshake function can be easily configured by setting any port assigned to be the  $\overline{\text{RTS}}$  function. The  $\overline{\text{RTS}}$  should be output "high" to request send data halt after data receive is completed by software in the RXD interrupt routine.

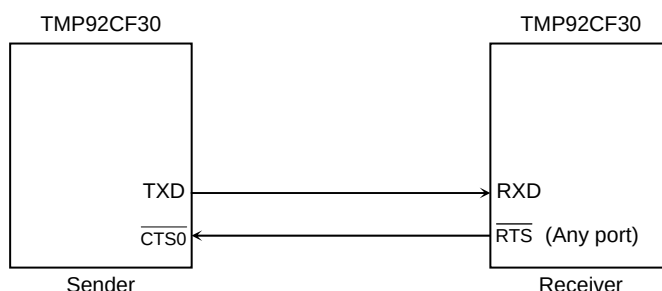
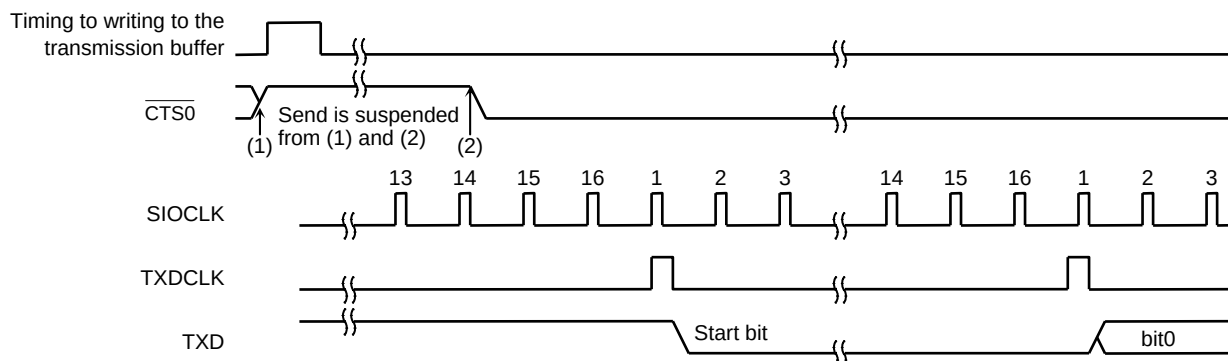


Figure 3.14.6 Handshake function



Note 1: If the  $\overline{\text{CTS0}}$  signal goes High during transmission, no more data will be sent after completion of the current transmission.

Note 2: Transmission starts on the first falling edge of the TXDCLK clock after the  $\overline{\text{CTS0}}$  signal has fallen.

Figure 3.14.7  $\overline{\text{CTS0}}$  (Clear to send) Timing

## (10) Transmission buffer

The transmission buffer (SC0BUF) shifts out and sends the transmission data written from the CPU in order from the least significant bit (LSB). When all the bits are shifted out, the transmission buffer becomes empty and generates an INTTX0 interrupt.

## (11) Parity control circuit

When SC0CR<PE> in the serial channel control register is set to “1”, it is possible to transmit and receive data with parity. However, parity can be added only in 7-bit UART mode or 8-bit UART mode. The SC0CR<EVEN> field in the serial channel control register allows either even or odd parity to be selected.

In the case of transmission, parity is automatically generated when data is written to the transmission buffer SC0BUF. The data is transmitted after the parity bit has been stored in SC0BUF<TB7> in 7-bit UART mode or in SC0MOD0<TB8> in 8-bit UART mode. SC0CR<PE> and SC0CR<EVEN> must be set before the transmission data is written to the transmission buffer.

In the case of receiving, data is shifted into receiving buffer 1, and the parity is added after the data has been transferred to receiving buffer 2 (SC0BUF), and then compared with SC0BUF<RB7> in 7-bit UART mode or with SC0CR<RB8> in 8-bit UART mode. If they are not equal, a parity error is generated and the SC0CR<PERR> flag is set.

## (12) Error flags

Three error flags are provided to increase the reliability of data reception.

## 1. Overrun error &lt;OERR&gt;

If all the bits of the next data item have been received in receiving buffer 1 while valid data still remains stored in receiving buffer 2 (SC0BUF), an overrun error is generated.

The below is a recommended flow when the overrun error is generated.

(INTRX interrupt routine)

1) Read receiving buffer

2) Read error flag

3) If <OERR> = “1”

then

a) Set to disable receiving (Write “0” to SC0MOD0<RXE>)

b) Wait to terminate current frame

c) Read receiving buffer

d) Read error flag

e) Set to enable receiving (Write “1” to SC0MOD0<RXE>)

f) Request to transmit again

4) Others

Note: Overrun errors are generated only with regard to receive buffer 2 (SC0BUF). Thus, if SC0CR<RB8> is not read, no overrun error will occur.

## 2. Parity error <PERR>

The parity generated for the data shifted into receiving buffer 2 (SC0BUF) is compared with the parity bit received via the RXD pin. If they are not equal, a parity error is generated.

Note: The parity error flag is cleared every time it is read. However, if a parity error is detected twice in succession and the parity error flag is read between the two parity errors, it may seem as if the flag had not been cleared. To avoid this situation, a read of the parity error flag should be triggered by a receive interrupt.

## 3. Framing error <FERR>

The stop bit for the received data is sampled three times around the center. If the majority of the samples are “0”, a Framing error is generated.

### (13) Timing generation

#### a. In UART Mode

##### Receiving

| Mode                 | 9-Bit<br>(Note)               | 8-Bit + Parity<br>(Note)           | 8-Bit, 7-Bit + Parity, 7-Bit |
|----------------------|-------------------------------|------------------------------------|------------------------------|
| Interrupt timing     | Center of last bit<br>(bit 8) | Center of last bit<br>(parity bit) | Center of stop bit           |
| Framing error timing | Center of stop bit            | Center of stop bit                 | Center of stop bit           |
| Parity error timing  | —                             | Center of last bit<br>(parity bit) | Center of stop bit           |
| Overrun error timing | Center of last bit<br>(bit 8) | Center of last bit<br>(parity bit) | Center of stop bit           |

Note: In 9-Bit and 8-Bit + Parity Modes, interrupts coincide with the ninth bit pulse.

Thus, when servicing the interrupt, it is necessary to wait for a 1-bit period (to allow the stop bit to be transferred) to allow checking for a framing error.

##### Transmitting

| Mode             | 9-Bit                                  | 8-Bit + Parity                         | 8-Bit, 7-Bit + Parity, 7-Bit           |
|------------------|----------------------------------------|----------------------------------------|----------------------------------------|
| Interrupt timing | Just before stop bit is<br>transmitted | Just before stop bit is<br>transmitted | Just before stop bit is<br>transmitted |

#### b. I/O interface

|                                     |                  |                                                                                                                              |
|-------------------------------------|------------------|------------------------------------------------------------------------------------------------------------------------------|
| Transmission<br>Interrupt<br>timing | SCLK Output Mode | Immediately after last bit. (See Figure 3.14.20.)                                                                            |
|                                     | SCLK Input Mode  | Immediately after rise of last SCLK signal Rising Mode, or immediately after fall in Falling Mode. (See Figure 3.14.21.)     |
| Receiving<br>Interrupt<br>timing    | SCLK Output Mode | Timing used to transfer received data to Receive Buffer 2 (SC0BUF) (i.e. immediately after last SCLK). (See Figure 3.14.22.) |
|                                     | SCLK Input Mode  | Timing used to transfer received data to Receive Buffer 2 (SC0BUF) (i.e. immediately after last SCLK). (See Figure 3.14.23.) |

3.14.3 SFR

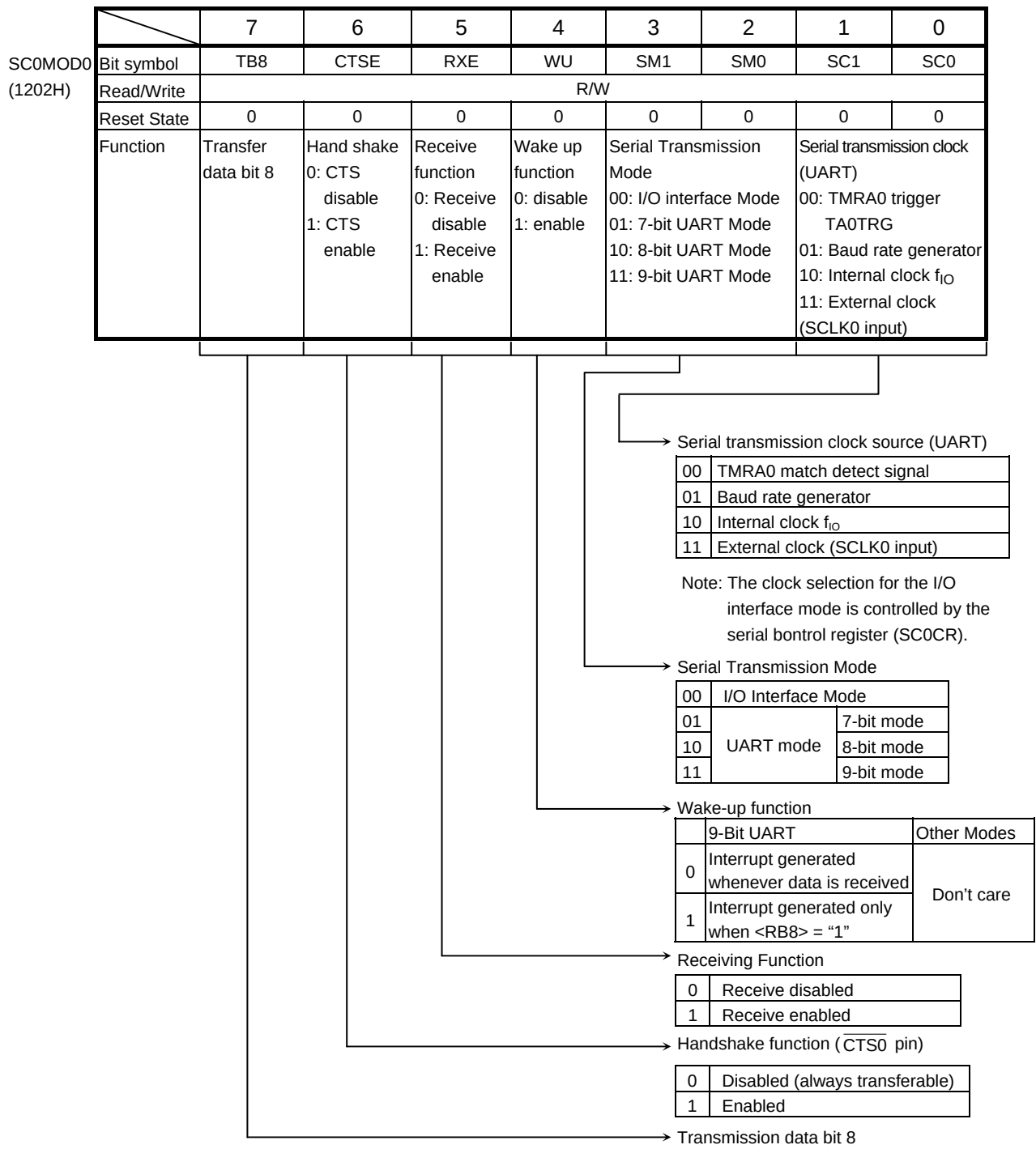
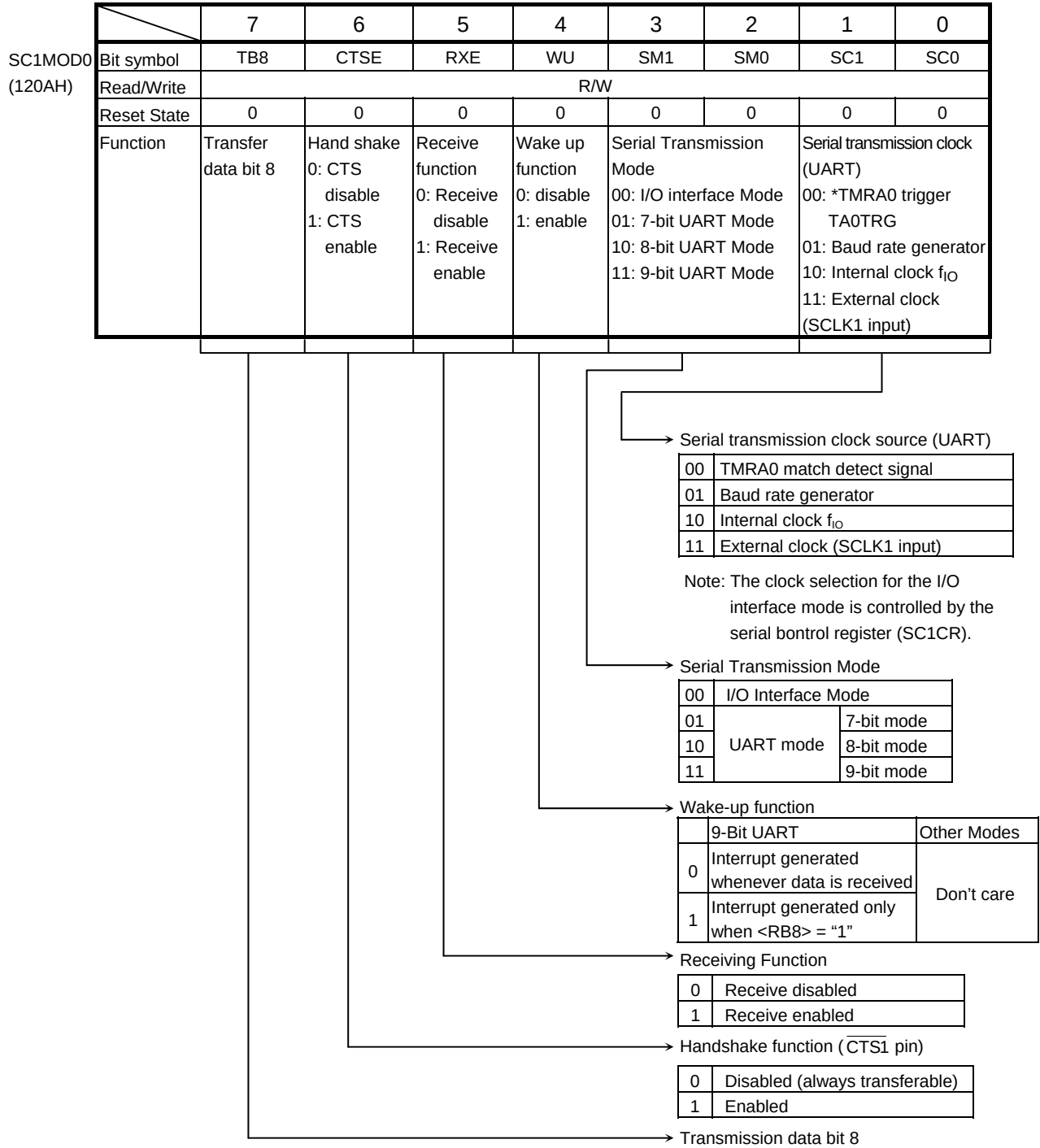


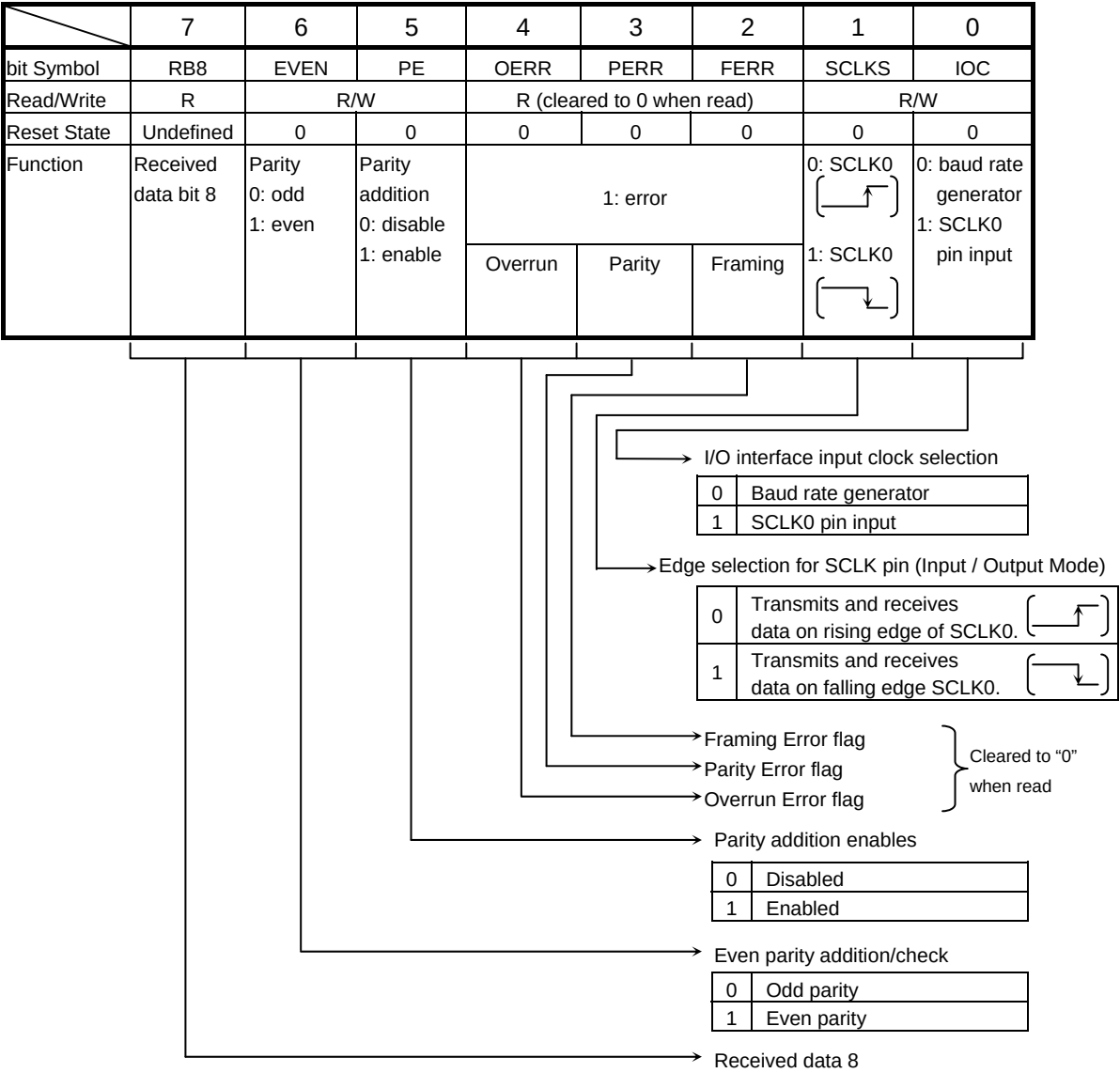
Figure 3.14.8 Serial Mode Control Register (channel 0, SC0MOD0)



Note: SIO1 can input SIO1 source clock from timer, however, it is possible to use only TMRA0 same with timer of SIO0. Timer differ with SIO0 cannot use. Please be careful.

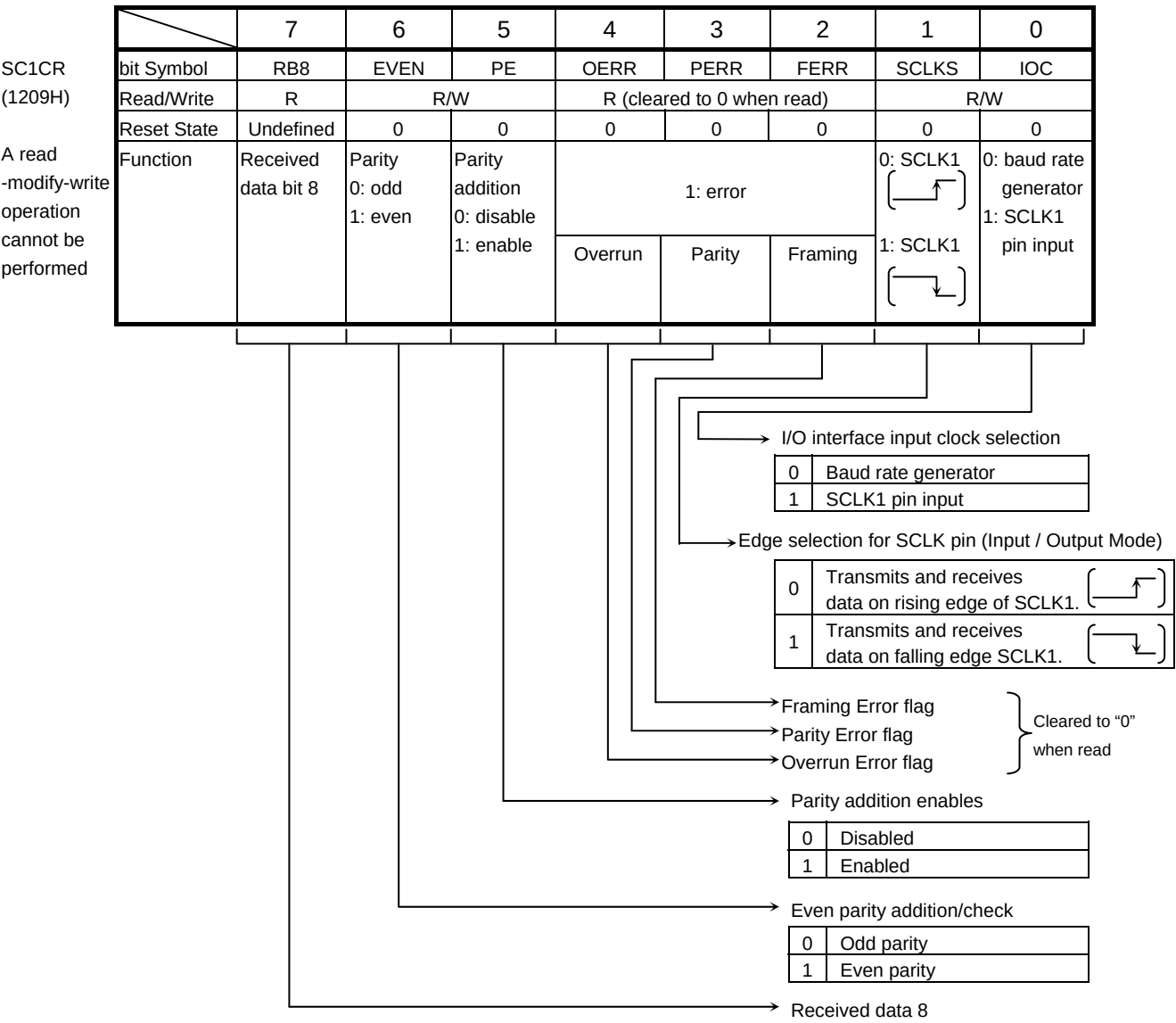
Figure 3.14.9 Serial Mode Control Register (channel 1, SC1MOD0)

SC0CR  
(1201H)  
  
A read  
-modify-write  
operation  
cannot be  
performed



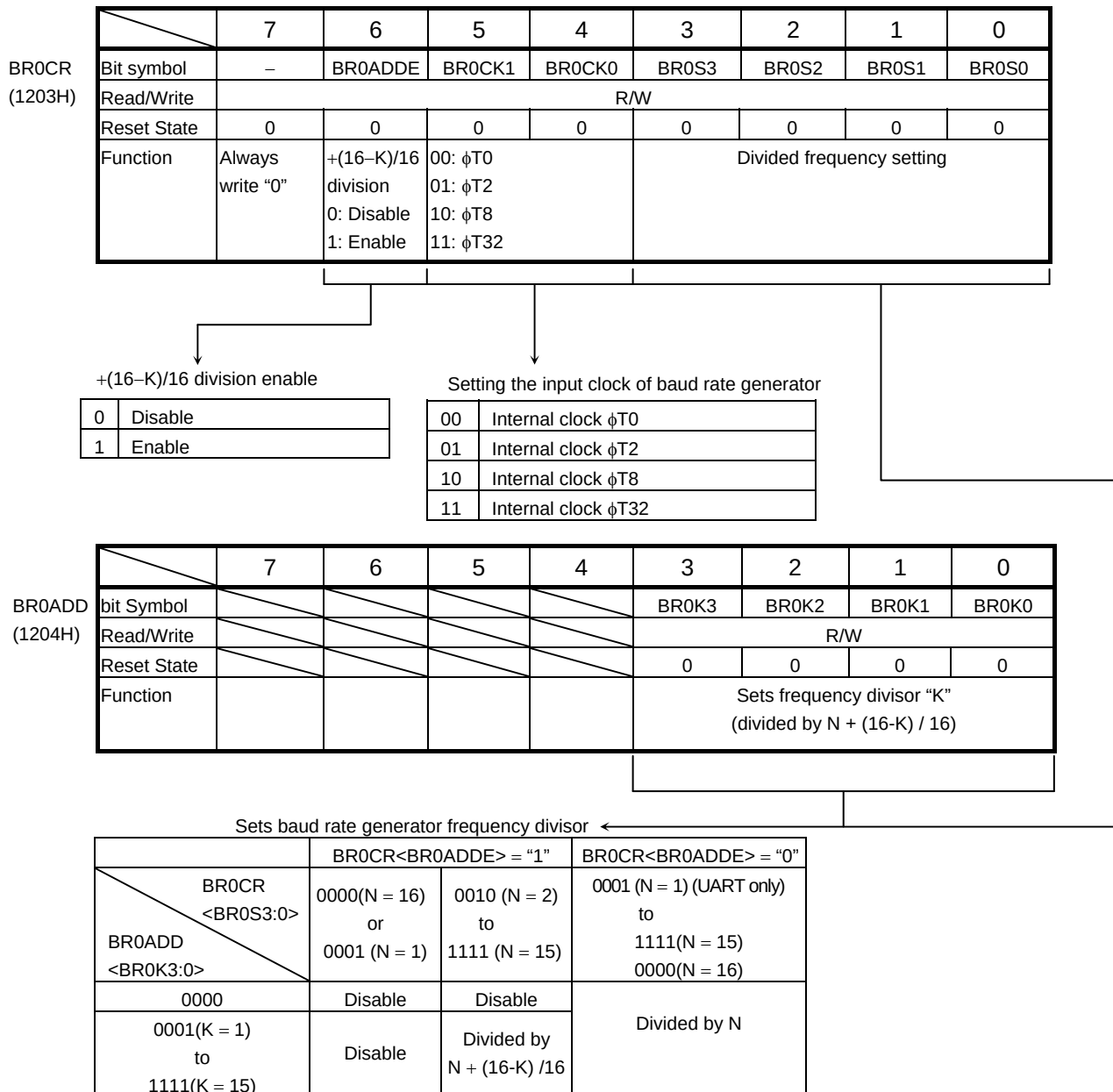
Note: As all error flags are cleared after reading, do not test only a single bit with a bit-testing instruction.

Figure 3.14.10 Serial Control Register (channel 0, SC0CR)



Note: As all error flags are cleared after reading, do not test only a single bit with a bit-testing instruction.

Figure 3.14.11 Serial Control Register (channel 1, SC1CR)



Note1: Availability of + (16-K)/16 division function

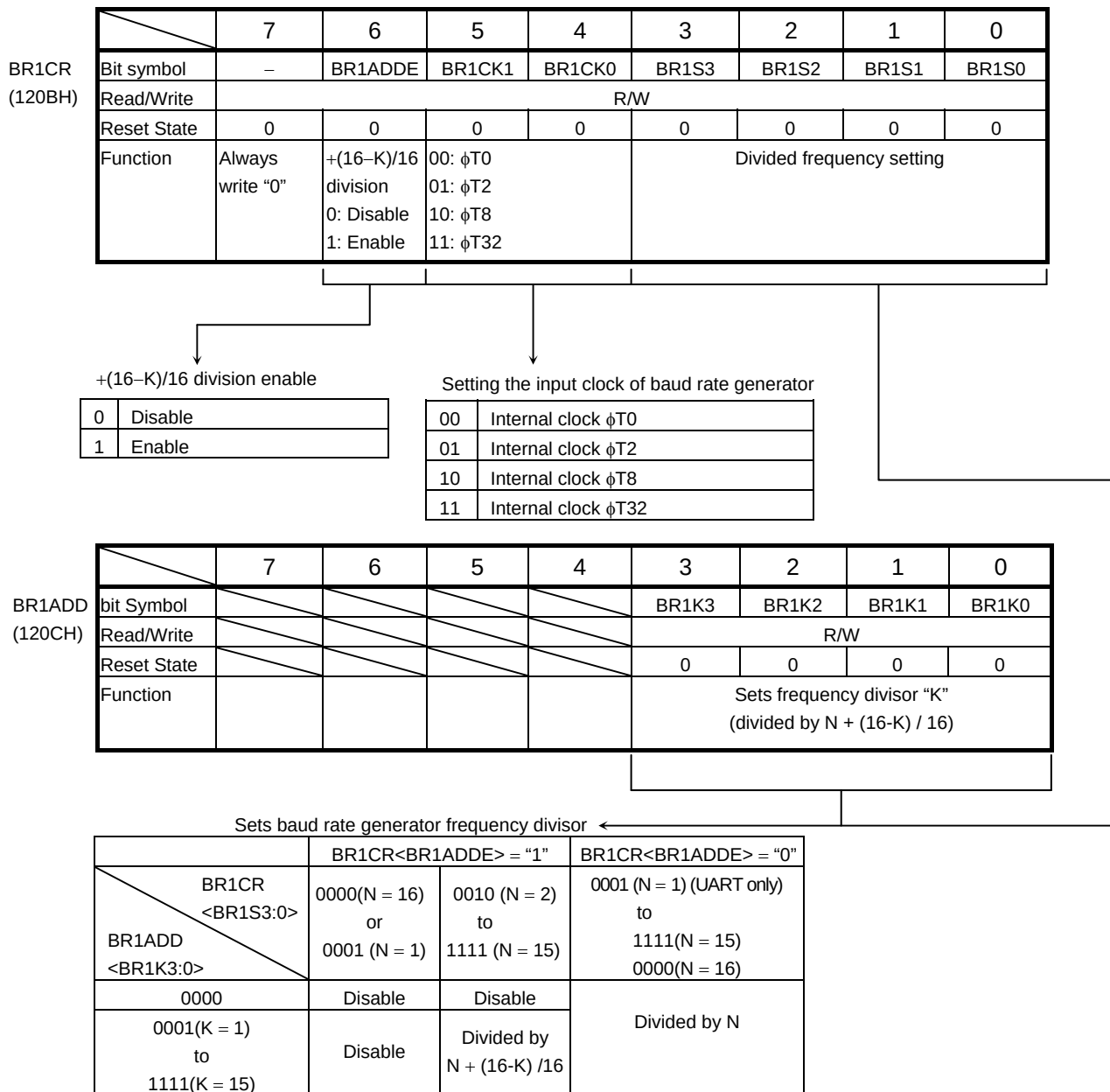
| N       | UART mode | I/O mode |
|---------|-----------|----------|
| 2 to 15 | ○         | ×        |
| 1, 16   | ×         | ×        |

The baud rate generator can be set to "1" in UART mode only when the + (16-K)/16 division function is not used. Do not use in I/O interface mode.

Note2: Set BR0CR <BR0ADDE> to "1" after setting K (K = 1 to 15) to BR0ADD<BR0K3:0> when the + (16-K)/16 division function is used. If the unused bits in the BR0ADD register is written, it does not affect operation. If that bits is read, it becomes undefined.

Figure 3.14.12 Baud rate generator control (channel 0, BR0CR, BR0ADD)





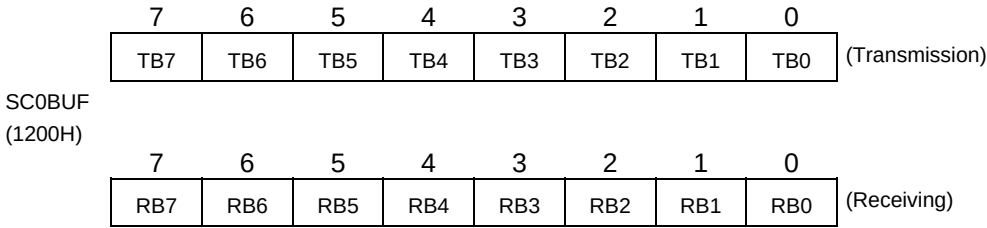
Note1: Availability of +(16-K)/16 division function

| N       | UART mode | I/O mode |
|---------|-----------|----------|
| 2 to 15 | ○         | ×        |
| 1, 16   | ×         | ×        |

The baud rate generator can be set to "1" in UART mode only when the +(16-K)/16 division function is not used. Do not use in I/O interface mode.

Note2: Set BR1CR <BR1ADDE> to "1" after setting K (K = 1 to 15) to BR1ADD<BR1K3:0> when the +(16-K)/16 division function is used. If the unused bits in the BR1ADD register is written, it does not affect operation. If that bits is read, it becomes undefined.

Figure 3.14.13 Baud rate generator control (channel 1, BR1CR, BR1ADD)

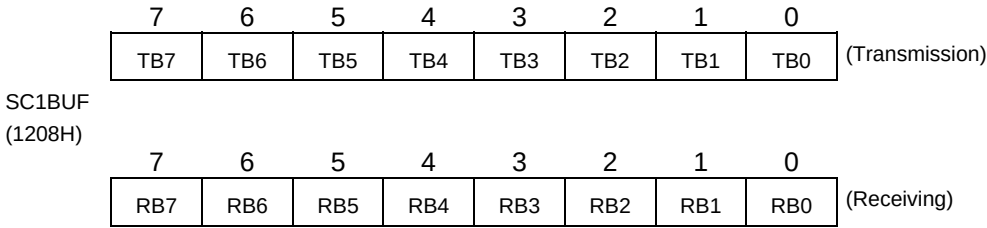


Note: Prohibit read-modify-write for SC0BUF.

Figure 3.14.14 Serial Transmission/Receiving Buffer Registers (channel 0, SC0BUF)

|             |                            |                              |   |   |   |   |   |   |
|-------------|----------------------------|------------------------------|---|---|---|---|---|---|
|             | 7                          | 6                            | 5 | 4 | 3 | 2 | 1 | 0 |
| Bit symbol  | I2S0                       | FDPX0                        |   |   |   |   |   |   |
| Read/Write  | R/W                        | R/W                          |   |   |   |   |   |   |
| Reset State | 0                          | 0                            |   |   |   |   |   |   |
| Function    | IDLE2<br>0: Stop<br>1: Run | duplex<br>0: half<br>1: full |   |   |   |   |   |   |

Figure 3.14.15 Serial Mode Control Register 1 (channel 0, SC0MOD1)



Note: Prohibit read-modify-write for SC1BUF.

Figure 3.14.16 Serial Transmission/Receiving Buffer Registers (channel 1, SC1BUF)

|             |                            |                              |   |   |   |   |   |   |
|-------------|----------------------------|------------------------------|---|---|---|---|---|---|
|             | 7                          | 6                            | 5 | 4 | 3 | 2 | 1 | 0 |
| Bit symbol  | I2S1                       | FDPX1                        |   |   |   |   |   |   |
| Read/Write  | R/W                        | R/W                          |   |   |   |   |   |   |
| Reset State | 0                          | 0                            |   |   |   |   |   |   |
| Function    | IDLE2<br>0: Stop<br>1: Run | duplex<br>0: half<br>1: full |   |   |   |   |   |   |

Figure 3.14.17 Serial Mode Control Register 1 (channel 1, SC1MOD1)

### 3.14.4 Operation in each mode

#### (1) Mode 0 (I/O Interface Mode)

This mode allows an increase in the number of I/O pins available for transmitting data to or receiving data from an external shift register.

This mode includes the SCLK output mode to output synchronous clock SCLK and SCLK input mode to input external synchronous clock SCLK.

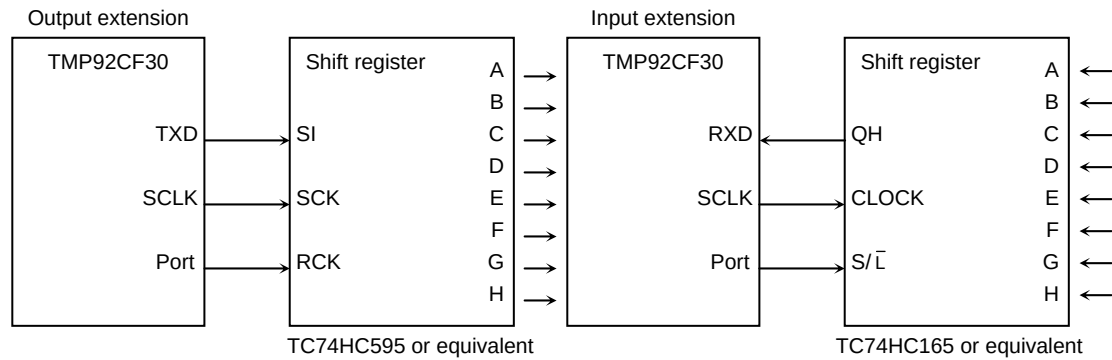


Figure 3.14.18 SCLK Output Mode connection example

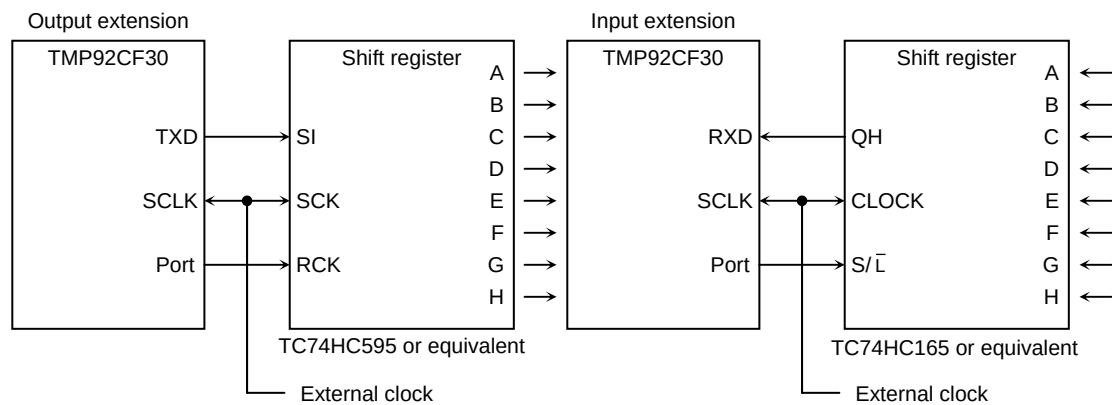


Figure 3.14.19 Example of SCLK Input Mode Connection

## a. Transmission

In SCLK output mode 8-bit data and a synchronous clock are output on the TXD0 and SCLK0 pins respectively each time the CPU writes the data to the Transmission Buffer. When all data is output, INTES0 <ITX0C> will be set to generate the INTTX0 interrupt.

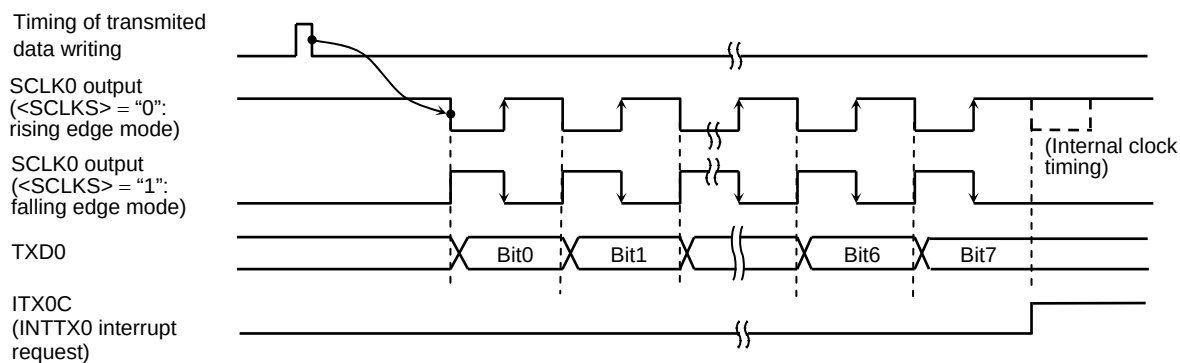


Figure 3.14.20 Transmitting Operation in I/O Interface Mode (SCLK0 Output Mode)

In SCLK Input Mode, 8-bit data is output on the TXD0 pin when the SCLK0 input becomes active after the data has been written to the Transmission Buffer by the CPU.

When all data is output, INTES0 <ITX0C> will be set to generate INTTX0 interrupt.

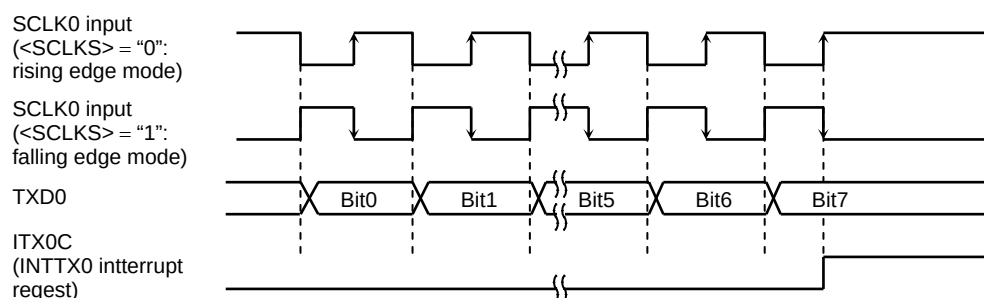


Figure 3.14.21 Transmitting Operation in I/O Interface Mode (SCLK0 Input Mode)

## b. Receiving

In SCLK Output Mode the synchronous clock is output on the SCLK0 pin and the data is shifted to Receiving Buffer 1. This is initiated when the Receive Interrupt flag INTES0<IRX0C> is cleared as the received data is read. When 8-bit data is received, the data is transferred to Receiving Buffer 2 (SC0BUF) following the timing shown below and INTES0<IRX0C> is set to “1” again, causing an INTRX0 interrupt to be generated.

Setting SC0MOD0<RXE> to “1” initiates SCLK0 output.

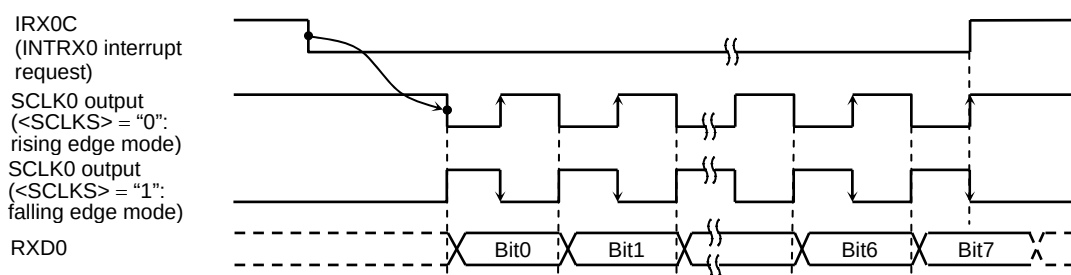


Figure 3.14.22 Receiving operation in I/O Interface Mode (SCLK0 Output Mode)

In SCLK Input Mode the data is shifted to Receiving Buffer 1 when the SCLK input goes active. The SCLK input goes active when the Receive Interrupt flag INTES0 <IRX0C> is cleared as the received data is read. When 8-bit data is received, the data is shifted to Receiving Buffer 2 (SC0BUF) following the timing shown below and INTES0 <IRX0C> is set to “1” again, causing an INTRX0 interrupt to be generated.

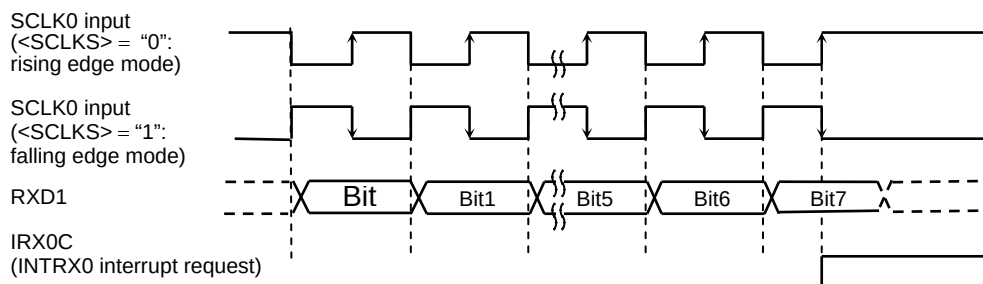


Figure 3.14.23 Receiving Operation in I/O interface Mode (SCLK0 Input Mode)

Note: The system must be put in the receive-enable state (SC0MOD0<RXE> = “1”) before data can be received.

## c. Transmission and Receiving (Full Duplex Mode)

When Full Duplex Mode is used, set the Receive Interrupt Level to 0, and only set the interrupt level (from 1 to 6) of the transmit interrupt. Ensure that the program which transmits the interrupt reads the receiving buffer before setting the next transmit data.

The following is an example of this:

Example: Channel 0, SCLK output

Baud rate = 9600 bps

$f_{\text{SYS}} = 2.4576 \text{ MHz}$

## Main routine

|         | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|---|
| INTES0  | X | 0 | 0 | 1 | X | 0 | 0 | 0 |
| P9CR    | X | X | X | X | X | 1 | 0 | 1 |
| P9FC    | – | – | X | X | X | 1 | X | 1 |
| SC0MOD0 | – | – | – | – | 0 | 0 | – | – |
| SC0MOD1 | – | 1 | X | X | X | X | X | X |
| SC0CR   | – | – | – | – | – | – | 0 | 0 |
| BR0CR   | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| SC0MOD0 | – | – | 1 | – | – | – | – | – |
| SC0BUF  | * | * | * | * | * | * | * | * |

Set the INTTX0 level to 1.

Set the INTRX0 level to 0.

Set P90, P91 and P92 to function as the TXD0, RXD0 and SCLK0 pins respectively.

Select I/O interface mode.

Select full duplex mode.

SCLK0 output mode, select rising edge

Baud rate = 9600 bps.

Enable receiving.

Set the transmit data and start.

## INTTX0 interrupt routine

|        |   |        |   |   |   |   |   |   |
|--------|---|--------|---|---|---|---|---|---|
| Acc    | ← | SC0BUF |   |   |   |   |   |   |
| SC0BUF | * | *      | * | * | * | * | * | * |

Read the receiving buffer.

Set the next transmit data.

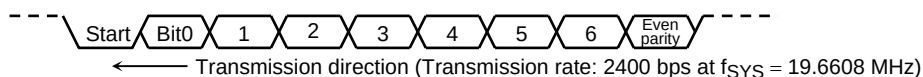
X: Don't care, –: No change

## (2) Mode 1 (7-bit UART Mode)

7-Bit UART Mode is selected by setting the Serial Channel Mode Register SC0MOD0<SM1:0> field to “01”.

In this mode a parity bit can be added. Use of a parity bit is enabled or disabled by the setting of the Serial Channel Control Register SC0CR<PE> bit; whether even parity or odd parity will be used is determined by the SC0CR<EVEN> setting when SC0CR<PE> is set to “1” (enabled).

Setting example: When transmitting data of the following format, the control registers should be set as described below.



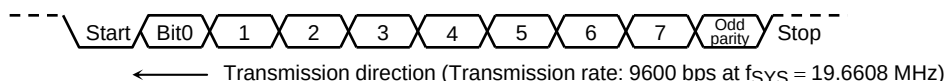
|         | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                              |
|---------|---|---|---|---|---|---|---|---|--------------------------------------------------------------|
| P9CR    | ← | X | X | X | X | – | – | 1 | } Set P90 to function as the TXD0 pin.                       |
| P9FC    | ← | – | – | X | X | X | – | X |                                                              |
| SC0MOD0 | ← | X | 0 | – | X | 0 | 1 | 0 | Select 7-bit UART mode.                                      |
| SC0CR   | ← | – | 1 | 1 | – | – | – | – | Add even parity.                                             |
| BR0CR   | ← | 0 | 0 | 1 | 0 | 1 | 0 | 0 | Set the transfer rate to 2400 bps.                           |
| INTES0  | ← | X | 1 | 0 | 0 | X | 0 | 0 | Enable the INTTX0 interrupt and set it to interrupt level 4. |
| SC0BUF  | ← | * | * | * | * | * | * | * | Set data for transmission.                                   |

X: Don't care, –: No change

## (3) Mode 2 (8-Bit UART Mode)

8-Bit UART Mode is selected by setting SC0MOD0<SM1:0> to “10”. In this mode a parity bit can be added (use of a parity bit is enabled or disabled by the setting of SC0CR<PE>); whether even parity or odd parity will be used is determined by the SC0CR<EVEN> setting when SC0CR<PE> is set to “1” (enabled).

Setting example: When receiving data of the following format, the control registers should be set as described below



## Main routine

|         | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |                                                              |
|---------|---|---|---|---|---|---|---|---|---|--------------------------------------------------------------|
| P9CR    | ← | X | X | X | X | X | – | 0 | – | Set P91 to function as the RXD0 pin.                         |
| P9FC    | ← | – | – | X | X | X | – | X | – |                                                              |
| SC0MOD0 | ← | – | – | 1 | – | 1 | 0 | 0 | 1 | Enable receiving in 8-bit UART mode.                         |
| SC0CR   | ← | – | 0 | 1 | – | – | – | – | – | Add odd parity.                                              |
| BR0CR   | ← | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | Set the transfer rate to 9600 bps.                           |
| INTES0  | ← | X | 1 | 0 | 0 | X | 0 | 0 | 0 | Enable the INTTX0 interrupt and set it to interrupt level 4. |

## Interrupt routine

|                       |   |                    |                        |
|-----------------------|---|--------------------|------------------------|
| Acc                   | ← | SC0CR AND 00011100 | } Check for errors     |
| if Acc ≠ 0 then ERROR |   |                    |                        |
| Acc                   | ← | SC0BUF             | Read the received data |

X: Don't care, -: No change

X: Don't care, –: No change

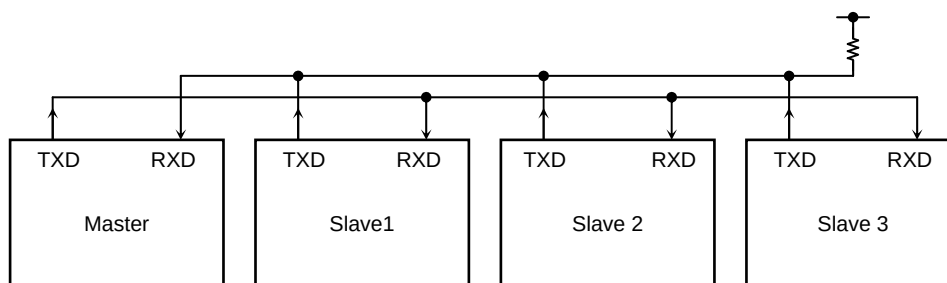
## (4) Mode 3 (9-Bit UART Mode)

9-Bit UART Mode is selected by setting SC0MOD0<SM1:0> to “11”. In this mode a parity bit cannot be added.

In the case of transmission the MSB (9th bit) is written to SC0MOD0<TB8>. In the case of receiving it is stored in SC0CR<RB8>. When the buffer is written or read, <TB8> or <RB8> is read or written first, before the rest of the SC0BUF data.

Wake-up function

In 9-Bit UART Mode, the wake-up function for slave controllers is enabled by setting SC0MOD0<WU> to “1”. The interrupt INTRX0 can only be generated when <RB8> = “1”.



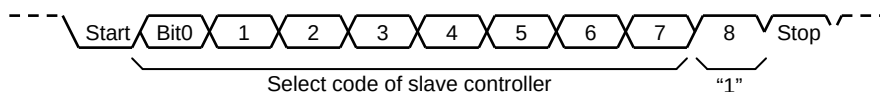
Note: The TXD pin of each slave controller must be in Open-Drain Output Mode.

Figure 3.14.24 Serial Link using Wake-up function



## Protocol

1. Select 9-Bit UART Mode on the master and slave controllers.
2. Set the SC0MOD0<WU> bit on each slave controller to “1” to enable data receiving.
3. The master controller transmits data one frame at a time. Each frame includes an 8-bit select code which identifies a slave controller. The MSB (bit 8) of the data (<TB8>) is set to “1”.

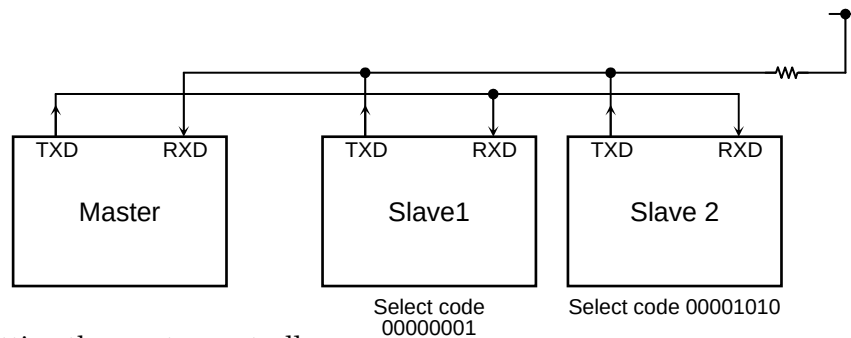


4. Each slave controller receives the above frame. Each controller checks the above select code against its own select code. The controller whose code matches clears its <WU> bit to “0”.
5. The master controller transmits data to the specified slave controller (the controller whose SC0MOD0<WU> bit has been cleared to “0”). The MSB (bit 8) of the data (<TB8>) is cleared to “0”.



6. The other slave controllers (whose <WU> bits remain at 1) ignore the received data because their MSBs (bit 8 or <RB8>) are set to “0”, disabling INTRX0 interrupts. The slave controller whose <WU> bit = “0” can also transmit to the master controller. In this way it can signal the master controller that the data transmission from the master controller has been completed.

Setting example: To link two slave controllers serially with the master controller using the internal clock  $f_{IO}$  as the transfer clock.



### Setting the master controller

#### Main routine

|         |   |                 |                                                                       |
|---------|---|-----------------|-----------------------------------------------------------------------|
| P9CR    | ← | X X X X X - 0 1 | } Set P90 and P91 to function as the TXD0 and RXD0 pins respectively. |
| P9FC    | ← | - - X X X - X 1 |                                                                       |
| INTES0  | ← | X 1 0 0 X 1 0 1 | Enable the INTTX0 interrupt and set it to Interrupt Level 4.          |
|         |   |                 | Enable the INTRX0 interrupt and set it to Interrupt Level 5.          |
| SC0MOD0 | ← | 1 0 1 0 1 1 1 0 | Set $f_{IO}$ as the transmission clock for 9-Bit UART Mode.           |
| SC0BUF  | ← | 0 0 0 0 0 0 0 1 | Set the select code for slave controller 1.                           |

#### Interrupt routine (INTTX0)

|         |   |             |                            |
|---------|---|-------------|----------------------------|
| SC0MOD0 | ← | 0 - - - - - | Set TB8 to "0".            |
| SC0BUF  | ← | * * * * *   | Set data for transmission. |

### Setting the slave controller

#### Main routine

|         |   |                 |                                                                                              |
|---------|---|-----------------|----------------------------------------------------------------------------------------------|
| P9CR    | ← | X X X X X - 0 1 | } Select P91 and P90 to function as the RXD0 and TXD0 pins respectively (open-drain output). |
| P9FC    | ← | - - X X X - X 1 |                                                                                              |
| P9FC2   | ← | X X X X X X X 1 |                                                                                              |
| INTES0  | ← | X 1 0 0 X 1 0 0 | Enable INTRX0 and INTTX0.                                                                    |
| SC0MOD0 | ← | 0 0 1 1 1 1 1 0 | Set <WU> to "1" in 9-Bit UART Transmission Mode using $f_{IO}$ as the transfer clock.        |

#### Interrupt routine (INTRX0)

```

Acc ← SC0BUF
if Acc = Select code
Then SC0MOD0 ← - - - - 0 - - - - Clear <WU> to "0".
  
```

### 3.14.5 Support for IrDA

SIO0 and SIO1 include support for the IrDA 1.0 infrared data communication specification.

Figure 3.14.25 shows the block diagram.

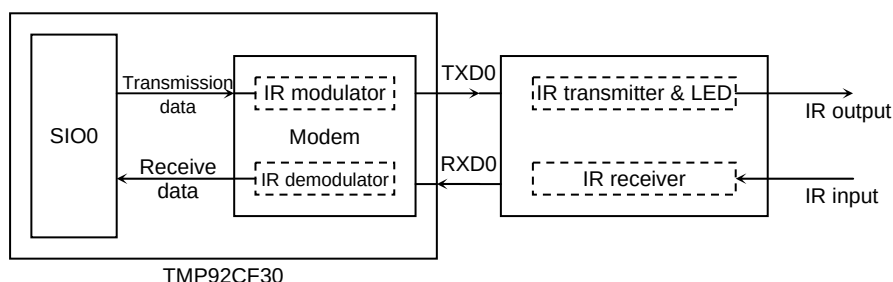


Figure 3.14.25 Block Diagram

#### (1) Modulation of the transmission data

When the transmit data is “0”, the modem outputs 1 to TXD0 pin with either 3/16 or 1/16 times for width of baud-rate. The pulse width is selected by the SIR0CR<PLSEL>. When the transmit data is “1”, the modem outputs “0”.

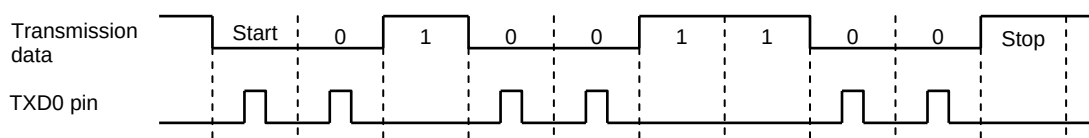


Figure 3.14.26 Transmission example

#### (2) Modulation of the receive data

When the receive data has an effective pulse width of pulse “1”, the modem outputs “0” to SIO0. Otherwise the modem outputs “1” to SIO0. The effective pulse width is selected by SIR0CR<SIR0WD3:0>.

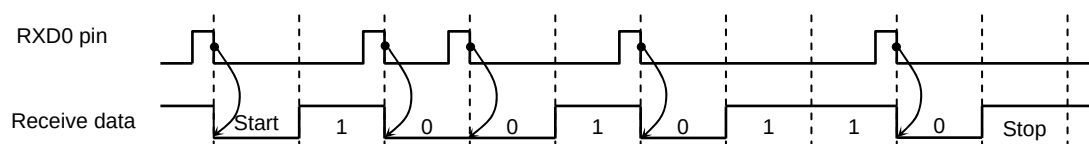


Figure 3.14.27 Receiving example

#### (3) Data format

The data format is fixed as follows:

- Data length: 8-bit
- Parity bits: none
- Stop bits: 1bit

## (4) SFR

Figure 3.14.28 shows the control register SI00CR. Set SI00CR data while SIO0 is stopped. The following example describes how to set this register:

- |                                              |                                                     |
|----------------------------------------------|-----------------------------------------------------|
| 1) SIO setting                               | ; Set the SIO to UART Mode.                         |
| ↓                                            |                                                     |
| 2) LD (SI00CR), 07H                          | ; Set the receive data pulse width to 16×           |
| 3) LD (SI00CR), 37H                          | ; TXEN, RXEN Enable the Transmission and receiving. |
| ↓                                            |                                                     |
| 4) Start transmission and receiving for SIO0 | ; The modem operates as follows:                    |
|                                              | • SIO0 starts transmitting.                         |
|                                              | • IR receiver starts receiving.                     |

## (5) Notes

## 1. Baud rate for IrDA

When IrDA is operated, set 01 to SC0MOD0<SC1:0> to generate baud-rate.

Setting other than the above (TA0TRG, f<sub>IO</sub> and SCLK0-input) cannot be used.

## 2. The pulse width for transmission

The IrDA 1.0 specification is defined in Table 3.14.4.

Table 3.14.4 Baud rate and pulse width specifications

| Baud Rate  | Modulation | Rate Tolerance (% of rate) | Pulse Width (minimum) | Pulse Width (typical) | Pulse width (maximum) |
|------------|------------|----------------------------|-----------------------|-----------------------|-----------------------|
| 2.4 kbps   | RZI        | ±0.87                      | 1.41 μs               | 78.13 μs              | 88.55 μs              |
| 9.6 kbps   | RZI        | ±0.87                      | 1.41 μs               | 19.53 μs              | 22.13 μs              |
| 19.2 kbps  | RZI        | ±0.87                      | 1.41 μs               | 9.77 μs               | 11.07 μs              |
| 38.4 kbps  | RZI        | ±0.87                      | 1.41 μs               | 4.88 μs               | 5.96 μs               |
| 57.6 kbps  | RZI        | ±0.87                      | 1.41 μs               | 3.26 μs               | 4.34 μs               |
| 115.2 kbps | RZI        | ±0.87                      | 1.41 μs               | 1.63 μs               | 2.23 μs               |

The infra-red pulse width is specified either baud rate  $T \times 3/16$  or 1.6 μs (1.6 μs is equal to  $3/16$  pulse width when baud rate is 115.2 kbps).

The TMP92CF30 has a function which can select the pulse width of Transmission as either  $3/16$  or  $1/16$ . However,  $1/16$  pulse width can only be selected when the baud rate is equal to or less than 38.4 kbps.

For the same reason, the  $+(16 - k)/16$  division functions in the baud rate generator of SIO0 cannot be used to generate a 115.2 kbps baud rate. The  $+(16 - K)/16$  division function cannot be used also when the baud rate is 38.4 kbps and the pulse width is  $1/16$ .

Table 3.14.5 Baud rate and pulse width for  $(16 - K) / 16$  division function

| Pulse Width     | Baud Rate  |           |           |           |          |          |
|-----------------|------------|-----------|-----------|-----------|----------|----------|
|                 | 115.2 Kbps | 57.6 Kbps | 38.4 Kbps | 19.2 Kbps | 9.6 Kbps | 2.4 Kbps |
| $T \times 3/16$ | × (Note)   | ○         | ○         | ○         | ○        | ○        |
| $T \times 1/16$ | —          | —         | ×         | ○         | ○        | ○        |

○:  $(16 - K)/16$  division function can be used.

×:  $(16 - K)/16$  division function cannot be used.

—: Cannot be set to  $1/16$  pulse width

Note:  $(16 - K)/16$  division function can be used under special conditions.

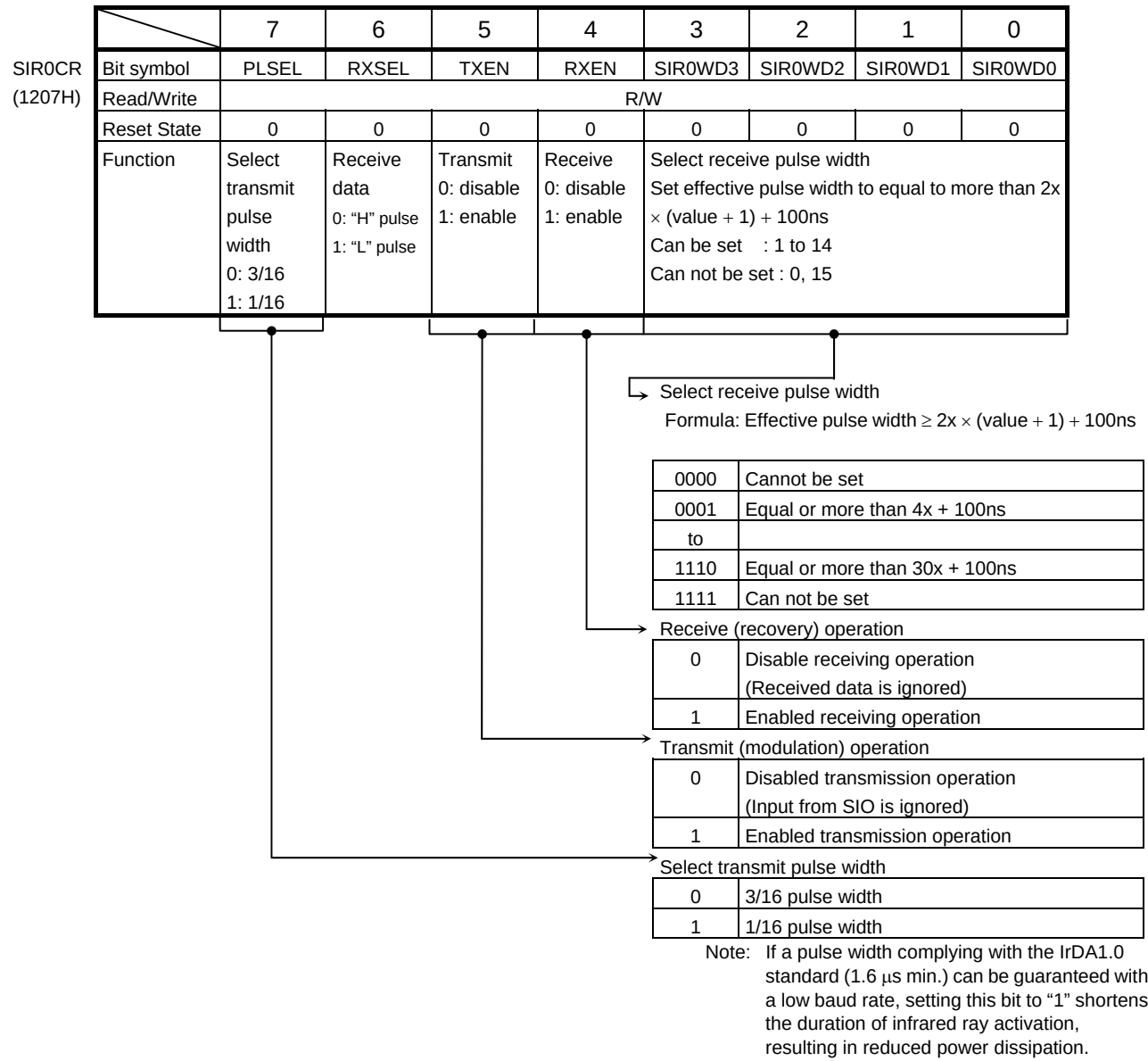


Figure 3.14.28 IrDA Control Register (for SIO0)

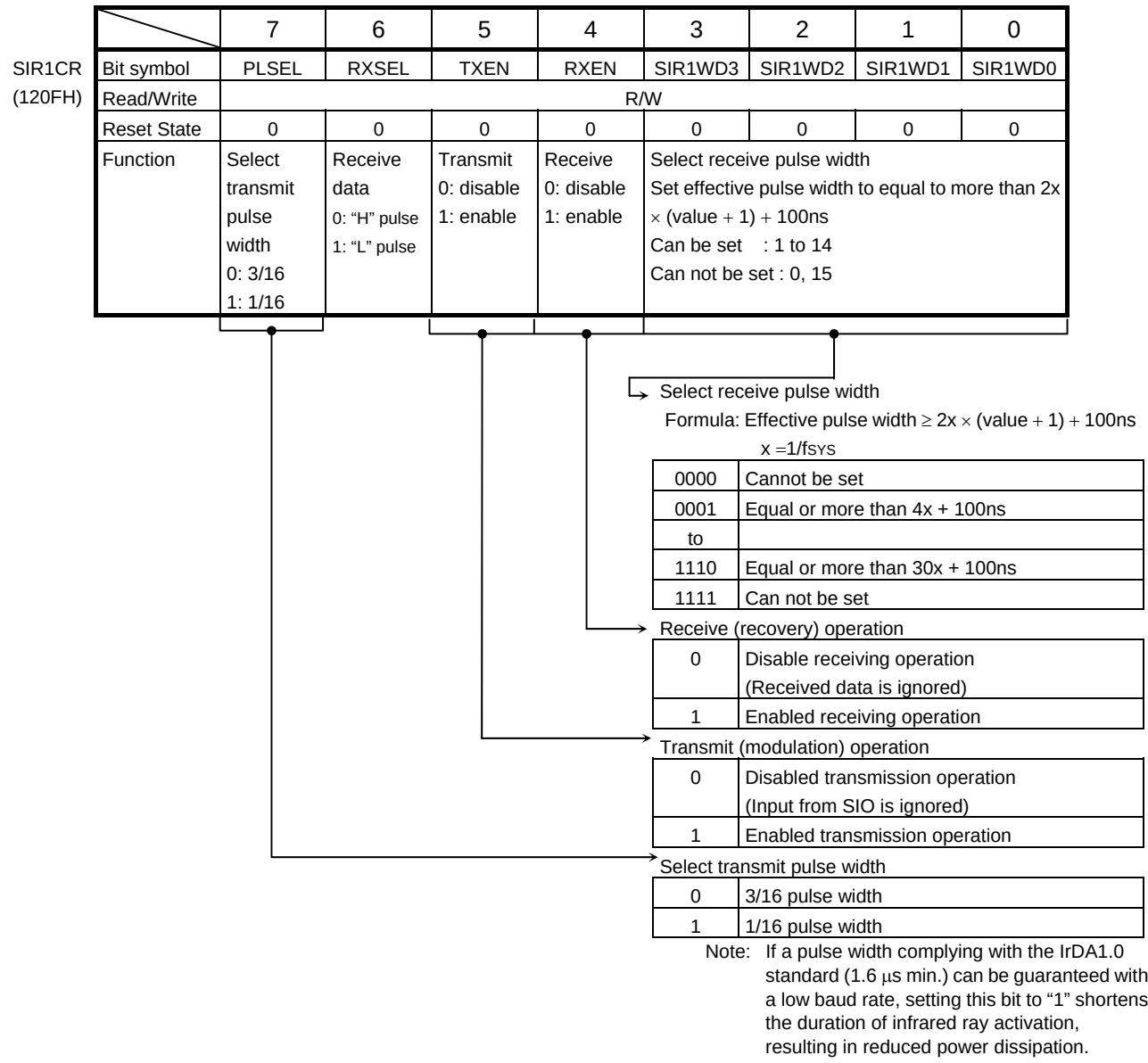


Figure 3.14.29 IrDA Control Register (for SIO1)

### 3.15 Serial Bus Interface (SBI)

The TMP92CF30 has a 1-channel serial bus interface which an I<sup>2</sup>C bus mode. This circuit supports only I<sup>2</sup>C bus mode (Multi master).

The serial bus interface is connected to an external device through PV6 (SDA) and PV7 (SCL) in the I<sup>2</sup>C bus mode.

Each pin is specified as follows.

|                           | PVFC2<PV7F2, PV6F2> | PVCR<PV7C, PV6C> | PVFC<PV7F, PV6F> |
|---------------------------|---------------------|------------------|------------------|
| I <sup>2</sup> C bus mode | 11                  | 11               | 11               |

#### 3.15.1 Configuration

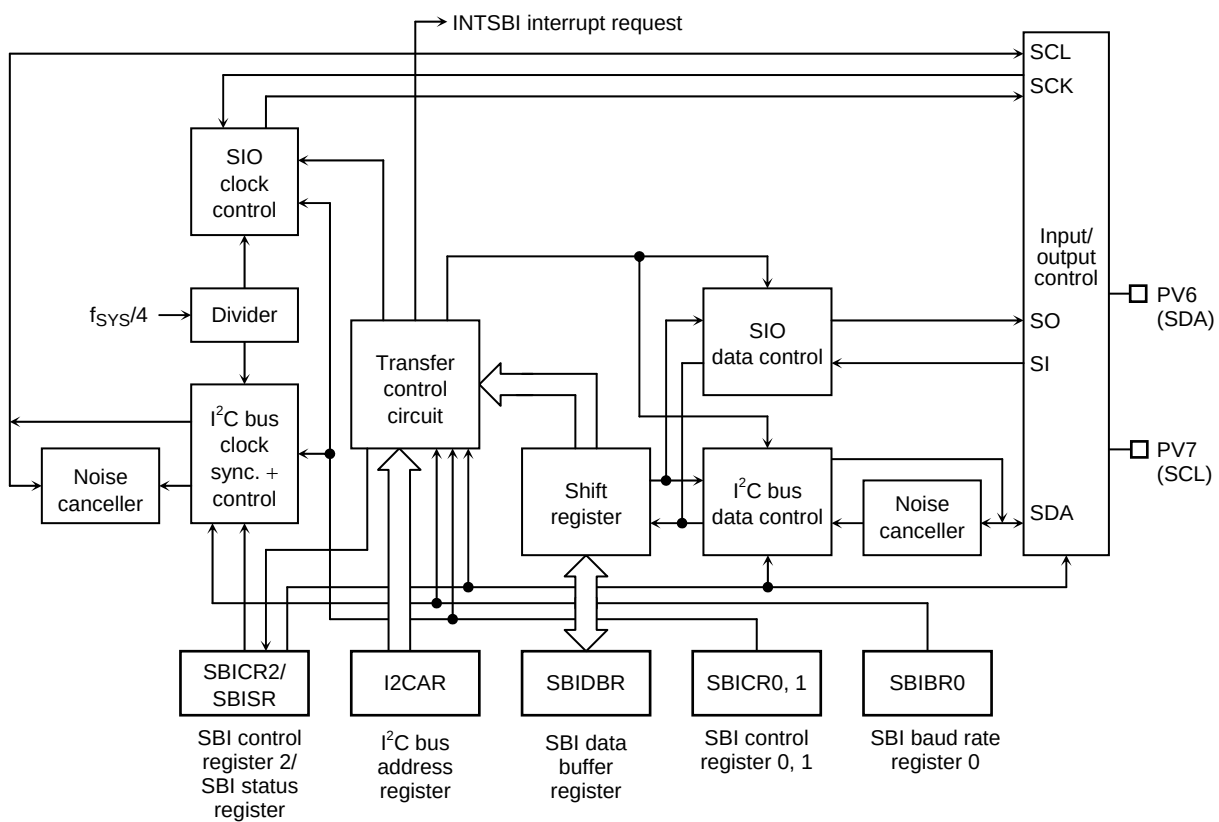


Figure 3.15.1 Serial bus interface (SBI)

### 3.15.2 Serial Bus Interface (SBI) Control

The following registers are used to control the serial bus interface and monitor the operation status.

- Serial bus interface control register 0 (SBICR0)
- Serial bus interface control register 1 (SBICR1)
- Serial bus interface control register 2 (SBICR2)
- Serial bus interface data buffer register (SBIDBR)
- I<sup>2</sup>C bus address register (I2CAR)
- Serial bus interface status register (SBISR)
- Serial bus interface baud rate register 0 (SBIBR0)

### 3.15.3 The Data Formats in the I<sup>2</sup>C Bus Mode

The data formats in the I<sup>2</sup>C bus mode is shown below.

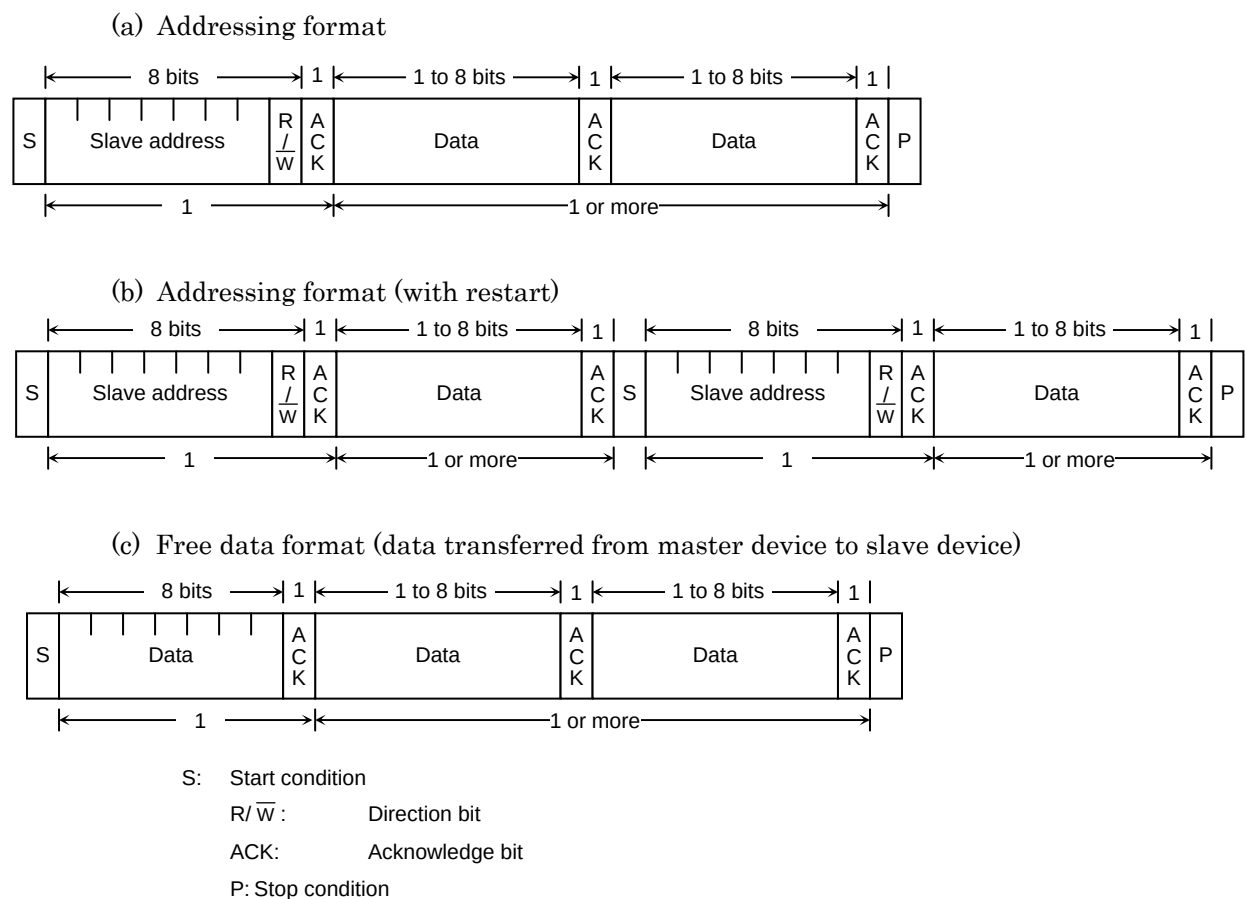


Figure 3.15.2 Data format in the I<sup>2</sup>C bus mode



3.15.4 I<sup>2</sup>C Bus Mode Control Register

The following registers are used to control and monitor the operation status when using the serial bus interface (SBI) in the I<sup>2</sup>C bus mode.

| Serial Bus Interface Control Register 0 |             |                                            |                  |   |   |   |   |   |
|-----------------------------------------|-------------|--------------------------------------------|------------------|---|---|---|---|---|
|                                         | 7           | 6                                          | 5                | 4 | 3 | 2 | 1 | 0 |
| SBICR0<br>(1247H)                       | Bit symbol  | SBIEN                                      | –                | – | – | – | – | – |
|                                         | Read/Write  | R/W                                        | R                |   |   |   |   |   |
|                                         | Reset State | 0                                          | 0                | 0 | 0 | 0 | 0 | 0 |
|                                         | Function    | SBI operation<br>0 : disable<br>1 : enable | Always read "0". |   |   |   |   |   |

A read-modify-write operation cannot be performed

<SBIEN> : When using SBI, <SBIEN> should be set "1" (SBI operation enable) before setting each register of SBI module.

Figure 3.15.3 Registers for the I<sup>2</sup>C bus mode

SBICR1  
(1240H)  
A read-  
modify-write  
operation  
cannot be  
performed

Serial Bus Interface Control Register 1

|             | 7                                      | 6   | 5   | 4                                                                         | 3                         | 2                                                             | 1    | 0               |
|-------------|----------------------------------------|-----|-----|---------------------------------------------------------------------------|---------------------------|---------------------------------------------------------------|------|-----------------|
| Bit symbol  | BC2                                    | BC1 | BC0 | ACK                                                                       | –                         | SCK2                                                          | SCK1 | SCK0/<br>SWRMON |
| Read/Write  | R/W                                    |     |     | R/W                                                                       | R                         | R/W                                                           |      | R/W             |
| Reset State | 0                                      | 0   | 0   | 0                                                                         | 1                         | 0                                                             | 0    | 0/1(Note2)      |
| Function    | Number of transferred bits<br>(Note 1) |     |     | Acknowledge<br>mode<br>specification<br>0: Not<br>generate<br>1: Generate | Always<br>read as<br>“1”. | Internal serial clock selection and<br>software reset monitor |      |                 |

Internal serial clock selection <SCK2:0> at write  
 $f_{SYS}=80\text{MHz}$  (Output to SCL pin), Clock gear =  $fc/1$

|     |            |            |                                                                                                                                                                                                    |
|-----|------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 000 | n = 4      | – (Note3)  | $\left( \begin{array}{l} \text{System Clock: } f_{SYS} \\ \quad \quad \quad (=80\text{MHz}) \\ \text{Clock Gear : } fc/1 \\ f_{scl} = \frac{f_{SYS}/4}{2^n + 36} \text{ [Hz]} \end{array} \right)$ |
| 001 | n = 5      | – (Note3)  |                                                                                                                                                                                                    |
| 010 | n = 6      | – (Note3)  |                                                                                                                                                                                                    |
| 011 | n = 7      | – (Note3)  |                                                                                                                                                                                                    |
| 100 | n = 8      | 68 kHz     |                                                                                                                                                                                                    |
| 101 | n = 9      | 36 kHz     |                                                                                                                                                                                                    |
| 110 | n = 10     | 19 kHz     |                                                                                                                                                                                                    |
| 111 | (Reserved) | (Reserved) |                                                                                                                                                                                                    |

Software reset state monitor <SWRMON> at read

|   |                       |
|---|-----------------------|
| 0 | During software reset |
| 1 | (Initial Data)        |

Acknowledge mode specification

|   |                                                 |
|---|-------------------------------------------------|
| 0 | Not generate clock pulse for acknowledge signal |
| 1 | Generate clock pulse for acknowledge signal     |

Number of bits transferred

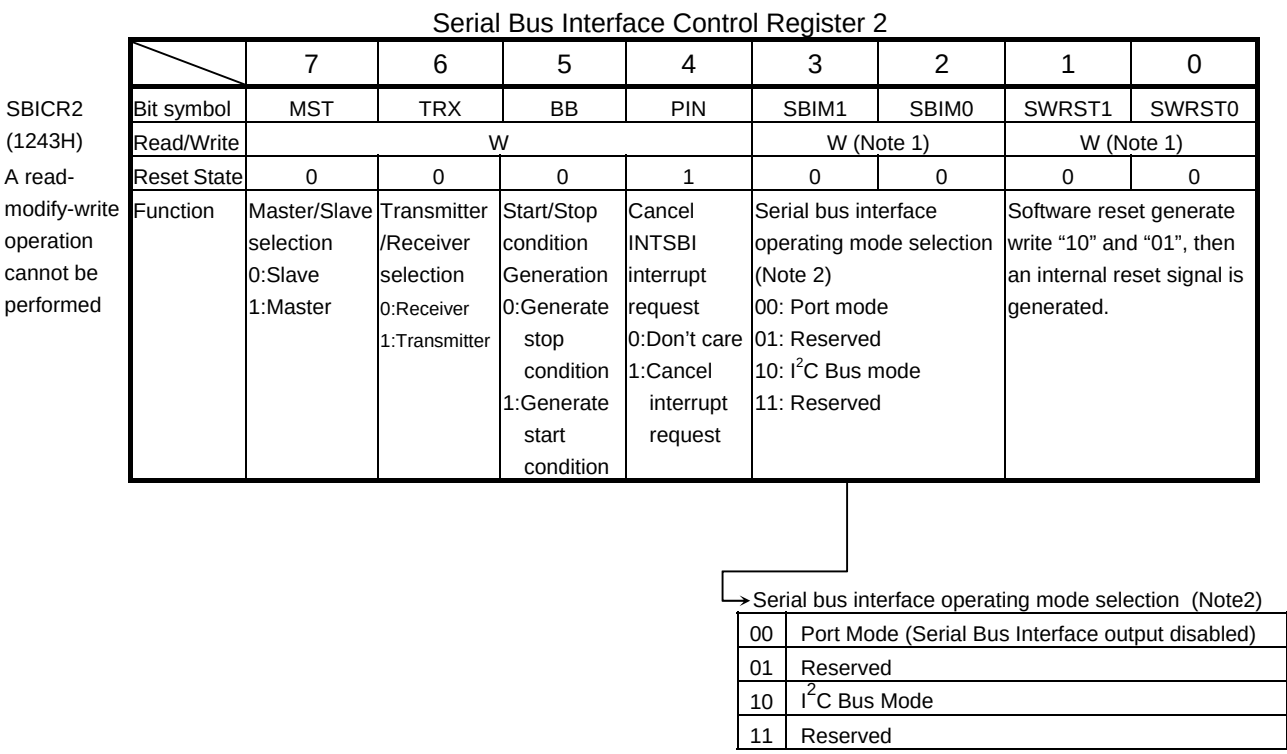
| <BC2:0> | <ACK> = 0                 |      | <ACK> = 1                 |      |
|---------|---------------------------|------|---------------------------|------|
|         | Number of<br>clock pulses | Bits | Number of<br>clock pulses | Bits |
| 000     | 8                         | 8    | 9                         | 8    |
| 001     | 1                         | 1    | 2                         | 1    |
| 010     | 2                         | 2    | 3                         | 2    |
| 011     | 3                         | 3    | 4                         | 3    |
| 100     | 4                         | 4    | 5                         | 4    |
| 101     | 5                         | 5    | 6                         | 5    |
| 110     | 6                         | 6    | 7                         | 6    |
| 111     | 7                         | 7    | 8                         | 7    |

Note1: For the frequency of the SCL line clock, see 3.15.5 (3) Serial clock.

Note2: The initial data of SCK0 is “0”, the initialdata of SWRMON is “1” if SBI operation is enable (SBICR0<SBIEN> = “1”). If SBI operation is disable (SBICR0<SBIEN> = “0”), the initialdata of SWRMON is “0”.

Note3: This I<sup>2</sup>C bus circuit does not support Fast-mode, it supports the Standard mode only. Although the I<sup>2</sup>C bus circuit itself allows the setting of a baud rate over 100kbps, the compliance with the I<sup>2</sup>C specification is not guaranteed in that case.

Figure 3.15.4 Registers for the I<sup>2</sup>C bus mode



Note 1: Reading this register functions as SBISR register.

Note 2: Switch a mode to port mode after confirming that the bus is free.

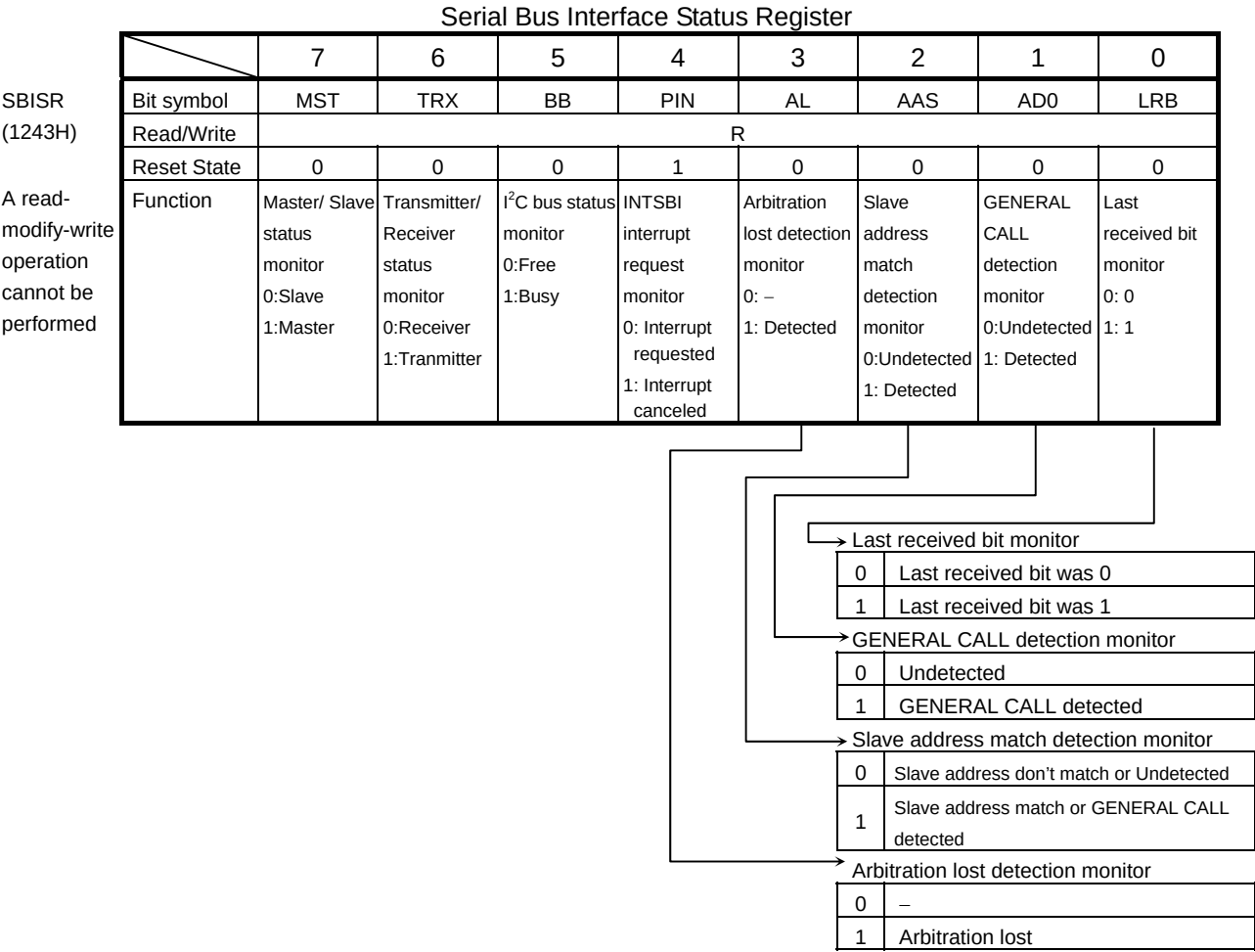
Switch a mode between I<sup>2</sup>C bus mode and port mode after confirming that input signals via port are high-level.

Figure 3.15.5 Registers for the I<sup>2</sup>C bus mode

Table 3.15.1Resolution of base clock

@f<sub>sys</sub> = 80MHz

| Clock Gear<br><GEAR1:0> | Base Clock<br>Resolution                 |
|-------------------------|------------------------------------------|
| 000(fc)                 | f <sub>sys</sub> /2 <sup>2</sup> (50ns)  |
| 001(fc/2)               | f <sub>sys</sub> /2 <sup>3</sup> (0.1μs) |
| 010(fc/4)               | f <sub>sys</sub> /2 <sup>4</sup> (0.2μs) |
| 011(fc/8)               | f <sub>sys</sub> /2 <sup>5</sup> (0.4μs) |
| 100(fc/16)              | f <sub>sys</sub> /2 <sup>6</sup> (0.8μs) |



Note1: Writing in this register functions as SBICR2.

Note2: The initialdata SBISR<PIN> is "1" if SBI operation is enable (SBICR0<SBIEN>="1"). If SBI operation is disable (SBICR0<SBIEN>="0"), the initialdata of SBISR<PIN> is "0".

Figure 3.15.6 Registers for the I<sup>2</sup>C bus mode

| Serial Bus Interface Baud Rate Register 0 |                 |                            |                    |   |   |   |   |                   |
|-------------------------------------------|-----------------|----------------------------|--------------------|---|---|---|---|-------------------|
|                                           | 7               | 6                          | 5                  | 4 | 3 | 2 | 1 | 0                 |
| Bit symbol                                | –               | I2SBI                      | –                  | – | – | – | – | –                 |
| Read/Write                                | W               | R/W                        | R                  |   |   |   |   | R/W               |
| Reset State                               | 0               | 0                          | 1                  | 1 | 1 | 1 | 1 | 0                 |
| Function                                  | Always read "0" | IDLE2<br>0: Stop<br>1: Run | Always read as "1" |   |   |   |   | Always write "0". |

SBIBR0 (1244H)  
A read-modify-write operation cannot be performed

Operation during IDLE 2 mode

|   |           |
|---|-----------|
| 0 | Stop      |
| 1 | Operation |

| Serial Bus Interface Data Buffer Register |                           |     |     |     |     |     |     |     |
|-------------------------------------------|---------------------------|-----|-----|-----|-----|-----|-----|-----|
|                                           | 7                         | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Bit symbol                                | DB7                       | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| Read/Write                                | R (received)/W (transfer) |     |     |     |     |     |     |     |
| Reset State                               | Undefined                 |     |     |     |     |     |     |     |

SBIDBR (1241H)  
A read-modify-write operation cannot be performed

Note1: When writing transmitted data, start from the MSB (bit 7). Receiving data is placed from LSB (bit 0).

Note2: SBIDBR can't be read the written data because of it has buffer for writing and buffer for reading individually. Therefore Read modify write instruction (e.g. "BIT" instruction) is prohibited.

| I <sup>2</sup> C Bus Address Register |                                                                      |     |     |     |     |     |     |                                        |
|---------------------------------------|----------------------------------------------------------------------|-----|-----|-----|-----|-----|-----|----------------------------------------|
|                                       | 7                                                                    | 6   | 5   | 4   | 3   | 2   | 1   | 0                                      |
| Bit symbol                            | SA6                                                                  | SA5 | SA4 | SA3 | SA2 | SA1 | SA0 | ALS                                    |
| Read/Write                            | R/W                                                                  |     |     |     |     |     |     |                                        |
| Reset State                           | 0                                                                    | 0   | 0   | 0   | 0   | 0   | 0   | 0                                      |
| Function                              | Slave address selection for when device is operating as slave device |     |     |     |     |     |     | Address recognition mode specification |

I2CAR (1242H)  
A read-modify-write operation cannot be performed

Address recognition mode specification

|   |                               |
|---|-------------------------------|
| 0 | Slave address recognition     |
| 1 | Non slave address recognition |

Figure 3.15.7 Registers for the I<sup>2</sup>C bus mode

3.15.5 Control in I<sup>2</sup>C Bus Mode

(1) Acknowledge Mode Specification

When slave address is matched or detecting GENERAL CALL, and set the SBICR1<ACK> to “1”, TMP92CF30 operates in the acknowledge mode. The TMP92CF30 generates an additional clock pulse for an Acknowledge signal when operating in Master Mode. In the transmitter mode during the clock pulse cycle, the SDA pin is released in order to receive the acknowledge signal from the receiver. In the receiver mode during the clock pulse cycle, the SDA pin is set to the Low in order to generate the acknowledge signal.

Clear the <ACK> to “0” for operation in the Non-Acknowledge Mode; The TMP92CF30 does not generate a clock pulse for the Acknowledge signal when operating in the Master Mode.

(2) Number of transfer bits

The SBICR1<BC2:0> is used to select a number of bits for next transmitting and receiving data.  
Since the <BC2:0> is cleared to 000 as a start condition, a slave address and direction bit transmission are executed in 8 bits. Other than these, the <BC2:0> retains a specified value.

(3) Serial clock

a. Clock source

The SBICR1 <SCK2:0> is used to select a maximum transfer frequency outputted on the SCL pin in Master Mode. Set a communication baud rates that meets the I<sup>2</sup>C bus specification, such as the shortest pulse width of t<sub>LOW</sub>, based on the equations shown below.

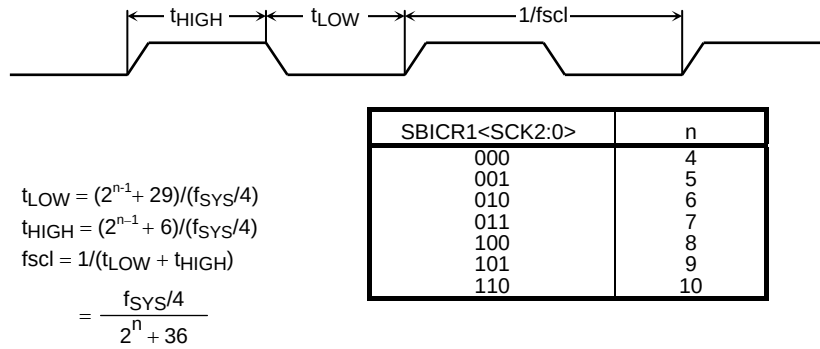


Figure 3.15.8 Clock source

## b. Clock synchronization

In the I<sup>2</sup>C bus mode, in order to wired-AND a bus, a master device which pulls down a clock line to low-level, in the first place, invalidate a clock pulse of another master device which generates a high-level clock pulse. The master device with a high-level clock pulse needs to detect the situation and implement the following procedure.

The TMP92CF30 has a clock synchronization function for normal data transfer even when more than one master exists on the bus.

The example explains the clock synchronization procedures when two masters simultaneously exist on a bus.

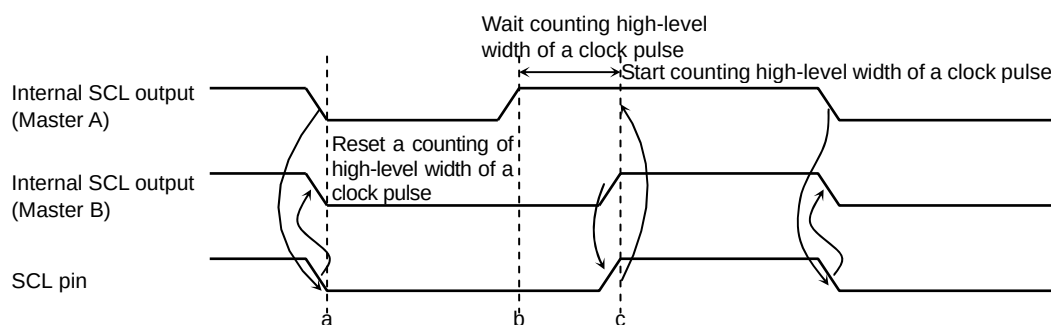


Figure 3.15.9 Clock synchronization

As Master A pulls down the internal SCL output to the Low level at point “a”, the SCL line of the bus becomes the Low-level. After detecting this situation, Master B resets a counter of High-level width of an own clock pulse and sets the internal SCL output to the Low-level.

Master A finishes counting Low-level width of an own clock pulse at point “b” and sets the internal SCL output to the High-level. Since Master B holds the SCL line of the bus at the Low-level, Master A wait for counting high-level width of an own clock pulse. After Master B finishes counting low-level width of an own clock pulse at point “c” and Master A detects the SCL line of the bus at the High-level, and starts counting High-level of an own clock pulse. The clock pulse on the bus is determined by the master device with the shortest High-level width and the master device with the longest Low-level width from among those master devices connected to the bus.

## (4) Slave address and address recognition mode specification

When the TMP92CF30 is used as a slave device, set the slave address <SA6:0> and <ALS> to the I2CAR. Clear the <ALS> to “0” for the address recognition mode.

## (5) Master/Slave selection

Set the SBICR2<MST> to “1” for operating the TMP92CF30 as a master device. Clear the SBICR2<MST> to “0” for operation as a slave device. The <MST> is cleared to “0” by the hardware after a stop condition on the bus is detected or arbitration is lost.

## (6) Transmitter/Receiver selection

Set the SBICR2<TRX> to “1” for operating the TMP92CF30 as a transmitter. Clear the <TRX> to “0” for operation as a receiver.

In Slave Mode,

- Data with an addressing format is transferred
- A slave address with the same value that an I2CAR
- A GENERAL CALL is received (all 8-bit data are “0” after a start condition)

The <TRX> is set to “1” by the hardware if the direction bit ( $R/\overline{W}$ ) sent from the master device is “1”, and is cleared to “0” by the hardware if the bit is “0”.

In the Master Mode, after an Acknowledge signal is returned from the slave device, the <TRX> is cleared to “0” by the hardware if a transmitted direction bit is “1”, and is set to “1” by the hardware if it is “0”. When an Acknowledge signal is not returned, the current condition is maintained.

The <TRX> is cleared to “0” by the hardware after a stop condition on the I<sup>2</sup>C bus is detected or arbitration is lost.

## (7) Start/Stop condition generation

When the SBISR<BB> is “0”, slave address and direction bit which are set to SBIDBR are output on a bus after generating a start condition by writing “1” to the SBICR2 <MST, TRX, BB, PIN>. It is necessary to set transmitted data to the data buffer register (SBIDBR) and set “1” to <ACK> beforehand.

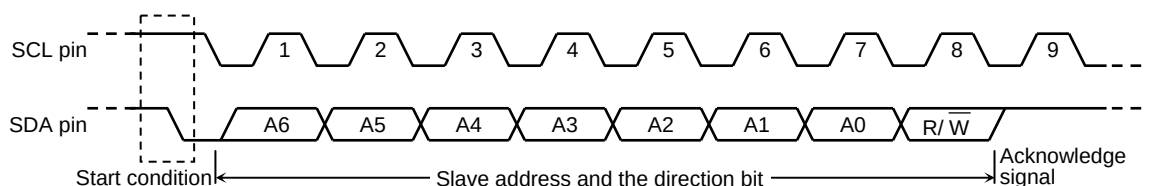
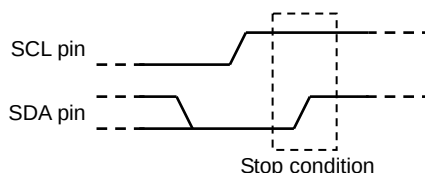


Figure 3.15.10 Start condition generation and slave address generation

When the <BB> is “1”, a sequence of generating a stop condition is started by writing “1” to the <MST, TRX, PIN>, and “0” to the <BB>. Do not modify the contents of <MST, TRX, BB, PIN> until a stop condition is generated on a bus.

Figure 3.15.11 Stop condition generation



The state of the bus can be ascertained by reading the contents of SBISR<BB>. SBISR<BB> will be set to 1 if a start condition has been detected on the bus, and will be cleared to 0 if a stop condition has been detected.



## (8) Interrupt service requests and interrupt cancellation

When a serial bus interface interrupt request (INTSBI) occurs, the SBICR2 <PIN> is cleared to "0". During the time that the SBICR2<PIN> is "0", the SCL line is pulled down to the Low level.

The <PIN> is cleared to "0" when a 1-word of data is transmitted or received. Either writing/reading data to/from SBIDBR sets the <PIN> to "1".

The time from the <PIN> being set to "1" until the SCL line is released takes tLOW.

In the address recognition mode (<ALS> = "0"), <PIN> is cleared to "0" when the received slave address is the same as the value set at the I2CAR or when a GENERAL CALL is received (all 8-bit data are "0" after a start condition). Although SBICR2<PIN> can be set to "1" by the program, the <PIN> is not clear it to "0" when it is written "0".

## (9) Serial bus interface operation mode selection

SBICR2<SBIM1:0> is used to specify the serial bus interface operation mode. Set SBICR2< SBIM1:0> to "10" when the device is to be used in I<sup>2</sup>C Bus Mode after confirming pin condition of serial bus interface to "H".

Switch a mode to port after confirming a bus is free.

## (10) Arbitration lost detection monitor

Since more than one master device can exist simultaneously on the bus in I<sup>2</sup>C Bus Mode, a bus arbitration procedure has been implemented in order to guarantee the integrity of transferred data.

In case set start condition bit with bus is busy, start condition is not output on SCL and SDA pin, but arbitration lost is generated.

Data on the SDA line is used for I<sup>2</sup>C bus arbitration.

The following shows an example of a bus arbitration procedure when two master devices exist simultaneously on the bus. Master A and Master B output the same data until point "a". After Master A outputs "L" and Master B, "H", the SDA line of the bus is wire-AND and the SDA line is pulled down to the Low-level by Master A. When the SCL line of the bus is pulled up at point b, the slave device reads the data on the SDA line, that is, data in Master A. A data transmitted from Master B becomes invalid. The state in Master B is called "ARBITRATION LOST". Master B device which loses arbitration releases the internal SDA output in order not to affect data transmitted from other masters with arbitration. When more than one master sends the same data at the first word, arbitration occurs continuously after the second word.

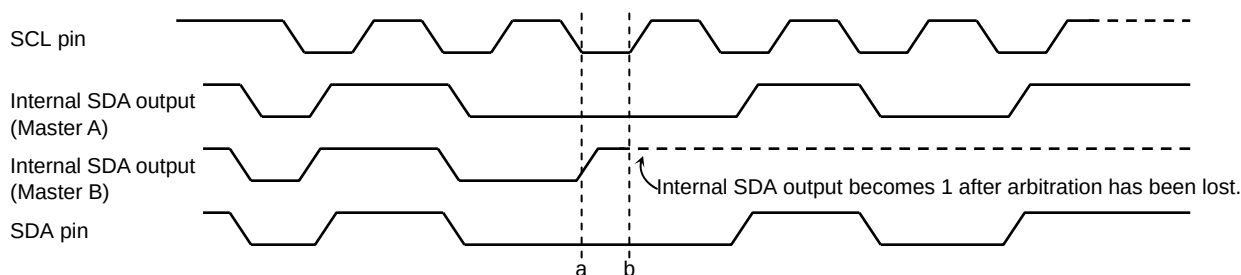


Figure 3.15.12 Arbitration lost

The TMP92CF30 compares the levels on the bus's SDA line with those of the internal SDA output on the rising edge of the SCL line. If the levels do not match, arbitration is lost and SBISR<AL> is set to "1".

When SBISR<AL> is set to "1", SBISR<MST, TRX> are cleared to "00" and the mode is switched to Slave Receiver Mode. Thus, clock output is stopped in data transfer after setting <AL>="1".

SBISR<AL> is cleared to "0" when data is written to or read from SBIDBR or when data is written to SBICR2.

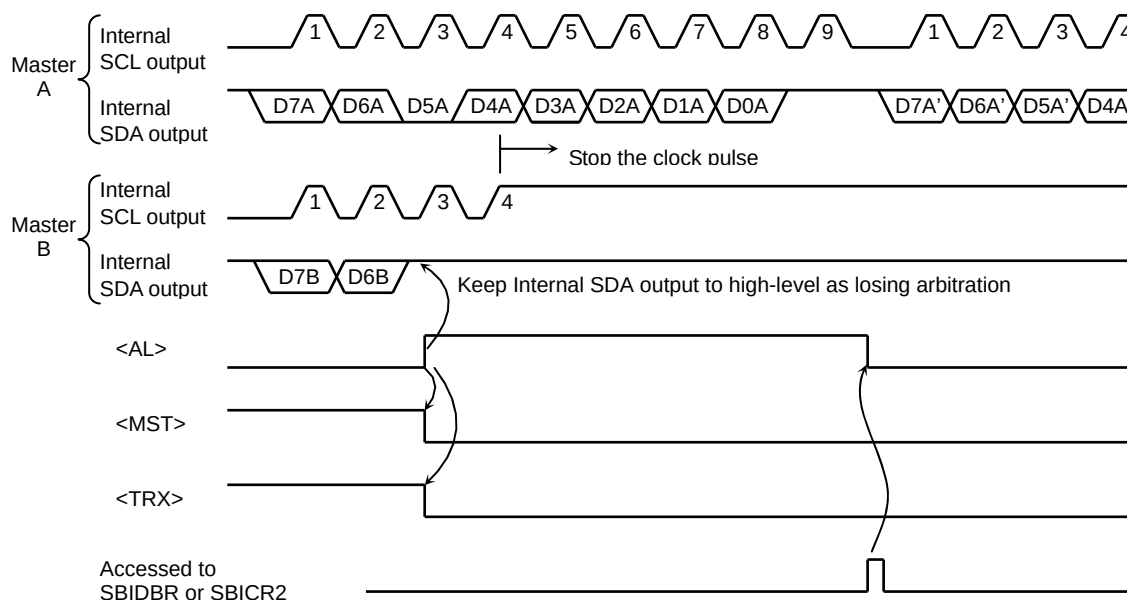


Figure 3.15.13 Example of when TMP92CF30 is a master device B  
(D7A = D7B, D6A = D6B)

(11) Slave address match detection monitor

SBISR<AAS> is set to "1" in Slave Mode, in Address Recognition Mode (i.e. when I2CAR<ALS> = "0"), when a GENERAL CALL is received, or when a slave address matches the value set in I2CAR. When I2CAR<ALS> = "1", SBISR<AAS> is set to "1" after the first word of data has been received. SBISR<AAS> is cleared to "0" when data is written to or read from the data buffer register SBIDBR.

(12) GENERAL CALL detection monitor

SBISR<AD0> is set to "1" in Slave Mode, when a GENERAL CALL is received (all 8-bit received data is "0", after a start condition). SBISR<AD0> is cleared to "0" when a start condition or stop condition is detected on the bus.

(13) Last received bit monitor

The SDA line value stored at the rising edge of the SCL line is set to the SBISR<LRB>. In the acknowledge mode, immediately after an INTSBI interrupt request is generated, an acknowledge signal is read by reading the contents of the SBISR<LRB>.

(14) Software Reset function

The software Reset function is used to initialize the SBI circuit, when SBI is rocked by external noises, etc.

An internal Reset signal pulse can be generated by setting SBICR2<SWRST1:0> to “10” and “01”. This initializes the SBI circuit internally. All command registers and status registers are initialized as well.

SBICR1<SWRMON> is automatically set to “1” after the SBI circuit has been initialized.

Note: If the software reset is executed, operation selection is reset, and its mode is set to port mode from I<sup>2</sup>C mode.

(15) Serial Bus Interface Data Buffer Register (SBIDBR)

The received data can be read and transferred data can be written by reading or writing the SBIDBR.

In the master mode, after the start condition is generated the slave address and the direction bit are set in this register.

(16) I<sup>2</sup>C BUS Address Register (I2CAR)

I2CAR<SA6:0> is used to set the slave address when the TMP92CF30 functions as a slave device.

The slave address output from the master device is recognized by setting the I2CAR<ALS> to “0”. The data format is the addressing format. When the slave address is not recognized at the <ALS> = “1”, the data format is the free data format.

(17) Setting register for IDLE2 mode operation (SBIBR0)

SBIBR0<I2SBI> is the register setting operation/stop during IDLE2-mode. Therefore, setting <I2SBI> is necessary before the HALT instruction is executed.

### 3.15.6 Data Transfer in I<sup>2</sup>C Bus Mode

#### (1) Device initialization

Set the SBICR1<ACK, SCK2:0>, Set SBIBR1 to “1” and clear bits 7 to 5 and 3 in the SBICR1 to “0”.

Set a slave address <SA6:0> and the <ALS> (<ALS> = “0” when an addressing format) to the I2CAR.

For specifying the default setting to a slave receiver mode, clear “0” to the <MST, TRX, BB> and set “1” to the <PIN>, “10” to the <SBIM1:0>.

|        | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
|--------|---|---|---|---|---|---|---|---|---|
| SBICR1 | ← | 0 | 0 | 0 | X | 0 | X | X | X |
| I2CAR  | ← | X | X | X | X | X | X | X | X |
| SBICR2 | ← | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

Note: X: Don't care

Set acknowledge and SCL clock.  
Set slave address and address recognition mode.  
Set to slave receiver mode.

#### (2) Start condition and slave address generation

##### a. Master Mode

In the Master Mode, the start condition and the slave address are generated as follows.

Check a bus free status (when <BB> = “0”).

Set the SBICR1<ACK> to “1” (Acknowledge Mode) and specify a slave address and a direction bit to be transmitted to the SBIDBR.

When SBICR2<BB> = “0”, the start condition are generated by writing “1111” to SBICR2<MST, TRX, BB, PIN>. Subsequently to the start condition, nine clocks are output from the SCL pin. While eight clocks are output, the slave address and the direction bit which are set to the SBIDBR. At the 9th clock, the SDA line is released and the acknowledge signal is received from the slave device.

An INTSBI interrupt request occurs at the falling edge of the 9th clock. The <PIN> is cleared to “0”. In the Master Mode, the SCL pin is pulled down to the Low-level while <PIN> is “0”. When an interrupt request occurs, the <TRX> is changed according to the direction bit only when an acknowledge signal is returned from the slave device.

#### Setting in main routine

|         | 7 | 6    | 5 | 4    | 3 | 2 | 1 | 0 |                         |
|---------|---|------|---|------|---|---|---|---|-------------------------|
| → Reg.  | ← | S    | B | I    | S | R |   |   |                         |
| Reg.    | ← | Reg. | e | 0x20 |   |   |   |   |                         |
| if Reg. | ≠ | 0x00 |   |      |   |   |   |   | Wait until bus is free. |
| Then    |   |      |   |      |   |   |   |   |                         |
| SBICR1  | ← | X    | X | X    | 1 | X | X | X | X                       |
| SBIDBR1 | ← | X    | X | X    | X | X | X | X | X                       |
| SBICR2  | ← | 1    | 1 | 1    | 1 | 1 | 0 | 0 | 0                       |

Set to acknowledgement mode.  
Set slave address and direction bit.  
Generate start condition.

#### In INTSBI interrupt routine

INTCLR ← 0X2a      Clear the interrupt request  
Process  
End of interrupt

## b. Slave Mode

In the Slave Mode, the start condition and the slave address are received.

After the start condition is received from the master device, while eight clocks are output from the SCL pin, the slave address and the direction bit that are output from the master device are received.

When a GENERAL CALL or the same address as the slave address set in I2CAR is received, the SDA line is pulled down to the Low-level at the 9th clock, and the acknowledge signal is output.

An INTSBI interrupt request occurs on the falling edge of the 9th clock. The <PIN> is cleared to "0". In Slave Mode the SCL line is pulled down to the Low-level while the <PIN> = "0".

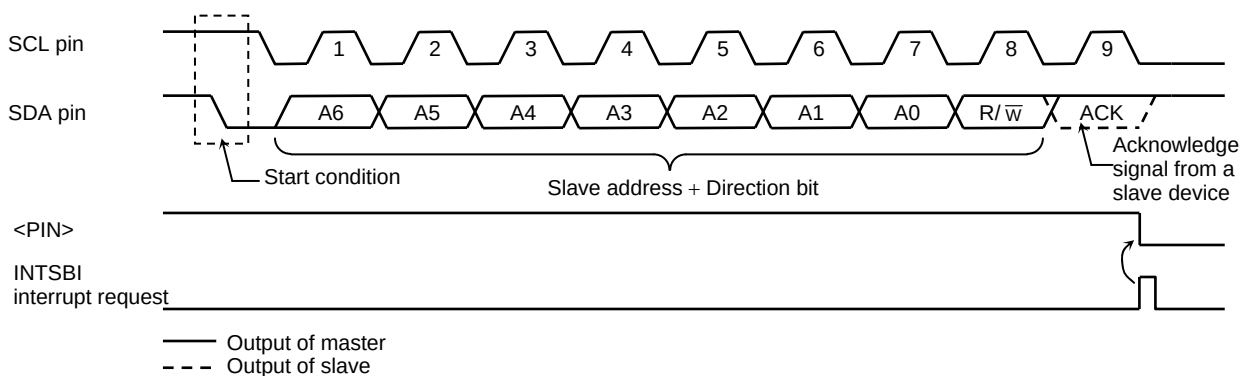


Figure 3.15.14 Start condition generation and slave address transfer

## (3) 1-word Data Transfer

Check the <MST> by the INTSBI interrupt process after the 1-word data transfer is completed, and determine whether the mode is a master or slave.

## a. If &lt;MST&gt; = "1" (Master Mode)

Check the <TRX> and determine whether the mode is a transmitter or receiver.

When the <TRX> = "1" (Transmitter mode)

Check the <LRB>. When <LRB> is "1", a receiver does not request data. Implement the process to generate a stop condition (Refer to 3.15.6 (4)) and terminate data transfer.

When the <LRB> is "0", the receiver requests new data. When the next transmitted data is 8 bits, write the transmitted data to SBIDBR. When the next transmitted data is other than 8 bits, set the <BC2:0> <ACK> and write the transmitted data to SBIDBR. After written the data, <PIN> becomes "1", a serial clock pulse is generated for transferring a new 1-word of data from the SCL pin, and then the 1-word data is transmitted. After the data is transmitted, an INTSBI interrupt request occurs. The <PIN> becomes "0" and the SCL line is pulled down to the Low-level. If the data to be transferred is more than one word in length, repeat the procedure from the <LRB> checking above.

INTSBI interrupt

if MST = 0

Then shift to the process when slave mode

if TRX = 0

Then shift to the process when receiver mode.

if LRB = 0

Then shift to the process that generates stop condition.

|                     |   |   |   |   |   |   |   |   |                                         |
|---------------------|---|---|---|---|---|---|---|---|-----------------------------------------|
|                     | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                         |
| SBICR1              | ← | X | X | X | X | X | X | X | Set the bit number of transmit and ACK. |
| SBIDBR              | ← | X | X | X | X | X | X | X | Write the transmit data.                |
| End of interrupt    |   |   |   |   |   |   |   |   |                                         |
| Note: X: Don't care |   |   |   |   |   |   |   |   |                                         |

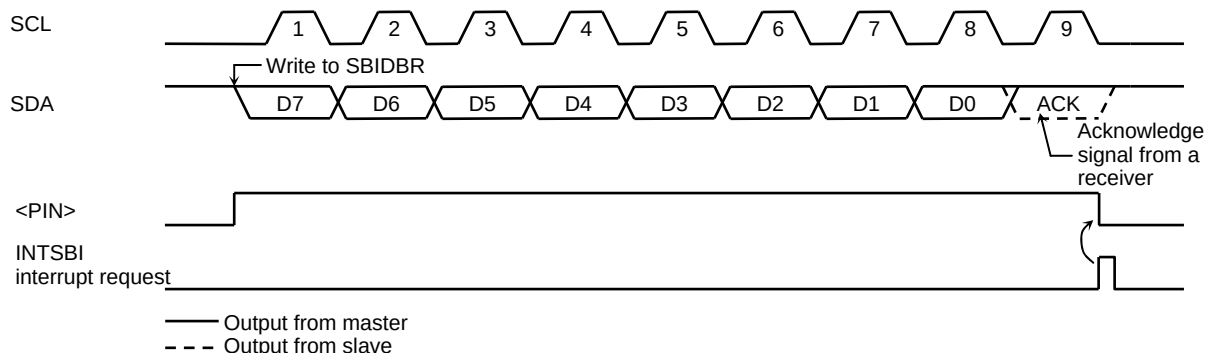


Figure 3.15.15 Example in which <BC2:0> = "000" and <ACK> = "1" in transmitter mode

### When the <TRX> is "0" (Receiver mode)

When the next transmitted data is other than 8 bits, set <BC2:0> <ACK> and read the received data from SBIDBR to release the SCL line (data which is read immediately after a slave address is sent is undefined). After the data is read, <PIN> becomes "1".

Serial clock pulse for transferring new 1 word of data is defined SCL and outputs "L" level from SDA pin with acknowledge timing.

An INTSBI interrupt request then occurs and the <PIN> becomes "0", Then the TMP92CF30 pulls down the SCL pin to the Low-level. The TMP92CF30 outputs a clock pulse for 1-word of data transfer and the acknowledge signal each time that received data is read from the SBIDBR.

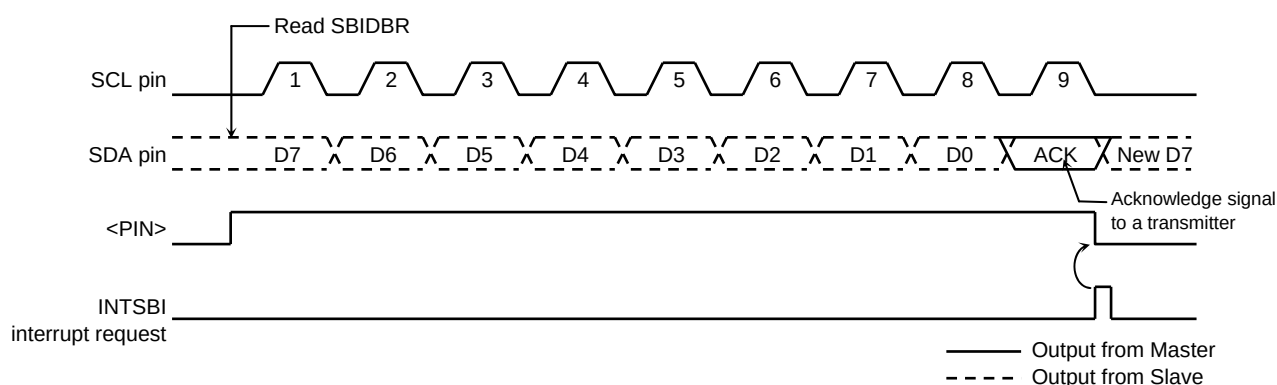


Figure 3.15.16 Example of when <BC2:0> = "000", <ACK> = "1" in receiver mode

In order to terminate the transmission of data to a transmitter, clear <ACK> to "0" before reading data which is 1-word before the last data to be received. The last data word does not generate a clock pulse as the Acknowledge signal. After the data has been transmitted and an interrupt request has been generated, set <BC2:0> to "001" and read the data. The TMP92CF30 generates a clock pulse for a 1-bit data transfer. Since the master device is a receiver, the SDA line on the bus remains High. The transmitter interprets the High signal as an ACK signal. The receiver indicates to the transmitter that data transfer is complete.

After the one data bit has been received and an interrupt request been generated, the TMP92CF30 generates a stop condition (see Section 3.15.6 (4) Stop condition generation) and terminates data transfer.

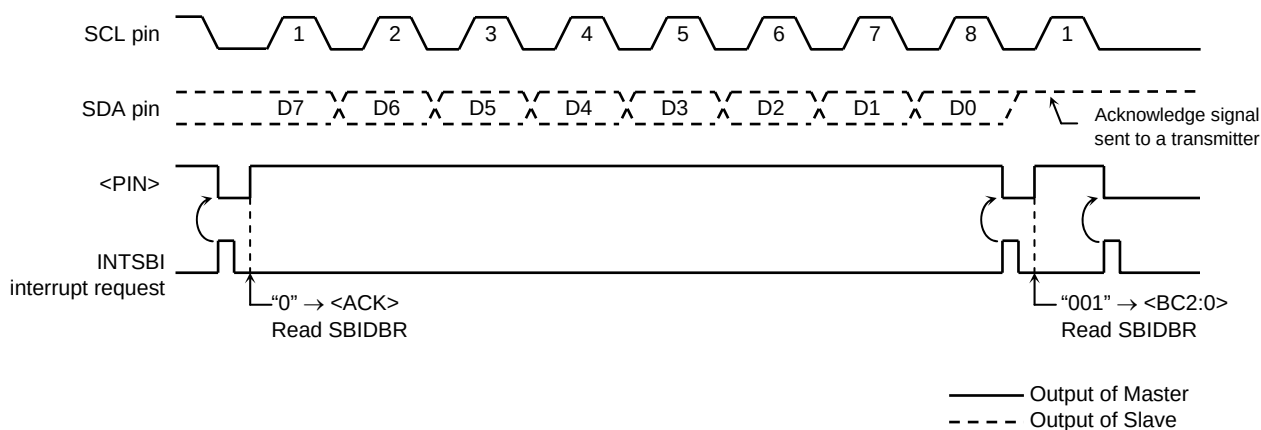


Figure 3.15.17 Termination of data transfer in master receiver mode

Example: In case receive data N times

INTSBI interrupt (After transmitting data)

|                  |                   |                                             |
|------------------|-------------------|---------------------------------------------|
|                  | 7 6 5 4 3 2 1 0   |                                             |
| SBICR1           | ← X X X X X X X X | Set the bit number of receive data and ACK. |
| Reg.             | ← SBIDBR          | Load the dummy data.                        |
| End of interrupt |                   |                                             |

INTSBI interrupt (Receive data of 1st to (N-2) th)

|                  |                 |                                  |
|------------------|-----------------|----------------------------------|
|                  | 7 6 5 4 3 2 1 0 |                                  |
| Reg.             | ← SBIDBR        | Load the data of 1st to (N-2)th. |
| End of interrupt |                 |                                  |

INTSBI interrupt ((N-1) th Receive data)

|                  |                   |                                 |
|------------------|-------------------|---------------------------------|
|                  | 7 6 5 4 3 2 1 0   |                                 |
| SBICR1           | ← X X X 0 0 X X X | Not generate acknowledge signal |
| Reg.             | ← SBIDBR          | Load the data of (N-1)th        |
| End of interrupt |                   |                                 |

INTSBI interrupt (Nth Receive data)

|                  |                   |                                      |
|------------------|-------------------|--------------------------------------|
|                  | 7 6 5 4 3 2 1 0   |                                      |
| SBICR1           | ← 0 0 1 0 0 X X X | Generate the clock for 1bit transmit |
| Reg.             | ← SBIDBR          | Receive the data of Nth.             |
| End of interrupt |                   |                                      |

INTSBI interrupt (After receiving data)

|                                          |                             |
|------------------------------------------|-----------------------------|
| The process of generating stop condition | Finish the transmit of data |
| End of interrupt                         |                             |

Note: X: Don't care



## b. If &lt;MST&gt; = 0 (Slave Mode)

In the slave mode the TMP92CF30 operates either in normal slave mode or in slave mode after losing arbitration.

In the slave mode, an INTSBI interrupt request occurs when the TMP92CF30 receives a slave address or a GENERAL CALL from the master device, or when a GENERAL CALL is received and data transfer is complete, or after matching received address. In the master mode, the TMP92CF30 operates in a slave mode if it losing arbitration. An INTSBI interrupt request occurs when a word data transfer terminates after losing arbitration. When an INTSBI interrupt request occurs the <PIN> is cleared to "0" and the SCL pin is pulled down to the Low-level. Either reading/writing from/to the SBIDBR or setting the <PIN> to "1" will release the SCL pin after taking tLOW time.

Check the SBISR<AL>, <TRX>, <AAS>, and <AD0> and implements processes according to conditions listed in the next table.

Example: In case matching slave address in slave receive mode, direction bit is "1".

INTSBI interrupt

if TRX = 0

Then shift to other process

if AL = 1

Then shift to other process

if AAS = 0

Then shift to other process

|        |   |   |   |   |   |   |   |   |   |
|--------|---|---|---|---|---|---|---|---|---|
|        |   | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SBICR1 | ← | X | X | X | 1 | X | X | X | X |
| SBIDBR | ← | X | X | X | X | X | X | X | X |

Set the bit number of transmit.

Set the data of transmit.

Note: X: Don't care

Table 3.15.2 Operation in the slave mode

| <TRX> | <AL> | <AAS> | <AD0> | Conditions                                                                                                                                                                               | Process                                                                                                                                                                                                                                                                                                                          |
|-------|------|-------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | 1    | 1     | 0     | The TMP92CF30 loses arbitration when transmitting a slave address and receives a slave address for which the value of the direction bit sent from another master is "1".                 | Set the number of bits a word in <BC2:0> and write the transmitted data to SBIDBR                                                                                                                                                                                                                                                |
|       | 0    | 1     | 0     | In Slave Receiver Mode, the TMP92CF30 receives a slave address for which the value of the direction bit sent from the master is "1".                                                     |                                                                                                                                                                                                                                                                                                                                  |
|       |      | 0     | 0     | In Slave Transmitter Mode, a single word of is transmitted.                                                                                                                              | Check the <LRB> setting. If <LRB> is set to "1", set <PIN> to "1" since the receiver win no request the data which follows. Then, clear <TRX> to "0" to release the bus. If <LRB> is cleared to "0", set <BC2:0> to the number of bits in a word and write the transmitted data to SBIDBR since the receiver requests next data. |
| 0     | 1    | 1     | 1/0   | The TMP92CF30 loses arbitration when transmitting a slave address and receives a slave address or GENERAL CALL for which the value of the direction bit sent from another master is "0". | Read the SBIDBR for setting the <PIN> to "1" (reading dummy data) or set the <PIN> to "1".                                                                                                                                                                                                                                       |
|       |      | 0     | 0     | The TMP92CF30 loses arbitration when transmitting a slave address or data and terminates word data transfer.                                                                             |                                                                                                                                                                                                                                                                                                                                  |
|       | 0    | 1     | 1/0   | In Slave Receiver Mode, the TMP92CF30 receives a slave address or GENERAL CALL for which the value of the direction bit sent from the master is "0".                                     |                                                                                                                                                                                                                                                                                                                                  |
|       |      | 0     | 1/0   | In Slave Receiver Mode, the TMP92CF30 terminates receiving word data.                                                                                                                    | Set <BC2:0> to the number of bits in a word and read the received data from SBIDBR.                                                                                                                                                                                                                                              |

## (4) Stop condition generation

When SBISR<BB> = "1", the sequence for generating a stop condition start by writing "1" to SBICR2<MST, TRX, PIN> and "0" to SBICR2<BB>. Do not modify the contents of SBICR2<MST, TRX, PIN, BB> until a stop condition has been generated on the bus. When the bus's SCL line has been pulled Low by another device, the TMP92CF30 generates a stop condition when the other device has released the SCL line and SDA pin rising.

7 6 5 4 3 2 1 0  
SBICR2 ← 1 1 0 1 1 0 0 0      Generate stop condition.

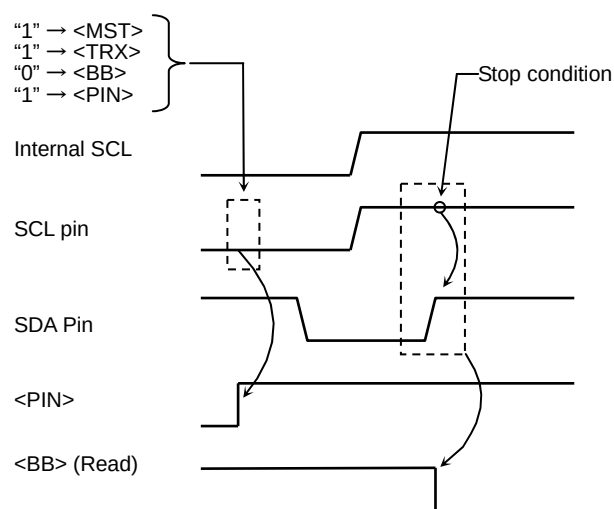


Figure 3.15.18 Stop condition generation (Single master)

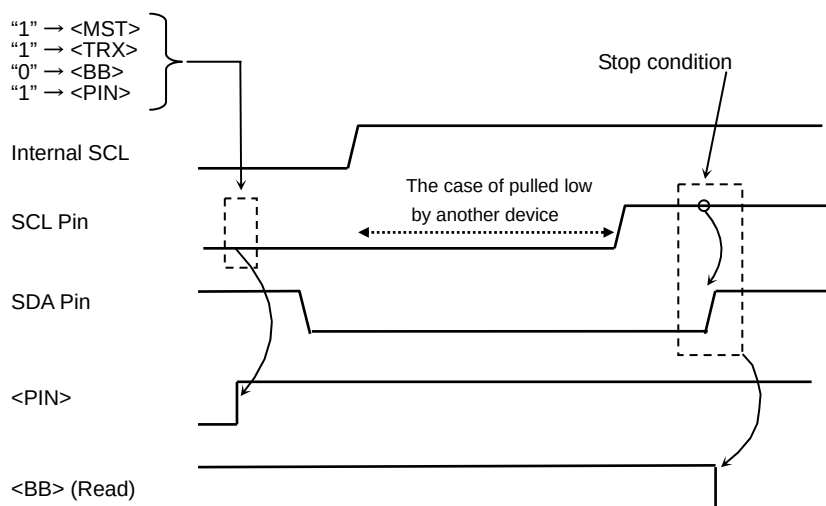


Figure 3.15.19 Stop condition generation (Multi master)

(5) Restart

Restart is used during data transfer between a master device and a slave device to change the data transfer direction.

The following description explains how to restart when the TMP92CF30 is in Master Mode.

Clear SBICR2<MST, TRX, and BB> to “0” and set SBICR2<PIN> to “1” to release the bus. The SDA line remains High and the SCL pin is released. Since a stop condition has not been generated on the bus, other devices assume the bus to be in busy state.

And confirm SCL pin, that SCL pin is released and become bus-free state by SBISR<BB> = “0” or signal level “1” of SCL pin in port mode. Check the <LRB> until it becomes 1 to check that the SCL line on a bus is not pulled down to the low-level by other devices. After confirming that the bus remains in a free state, generate a start condition using the procedure described in (2).

In order to satisfy the set-up time requirements when restarting, take at least 4.7 μs of waiting time by software from the time of restarting to confirm that the bus is free until the time to generate the start condition.

7 6 5 4 3 2 1 0

SBICR2 ← 0 0 0 1 1 0 0 0

if SBISR<BB> ≠ 0

Then

if SBISR<LRB> ≠ 1

Then

4.7 μs Wait

SBICR1 ← X X X 1 X X X X

SBIDBR ← X X X X X X X X

SBICR2 ← 1 1 1 1 1 0 0 0

Release the bus

Check if SCL pin is released.

Check if SCL pin of other device is “L” level.

Set acknowledgement mode.

Set the slave address and direction bit.

Generate start condition.

Note: X: Don't care

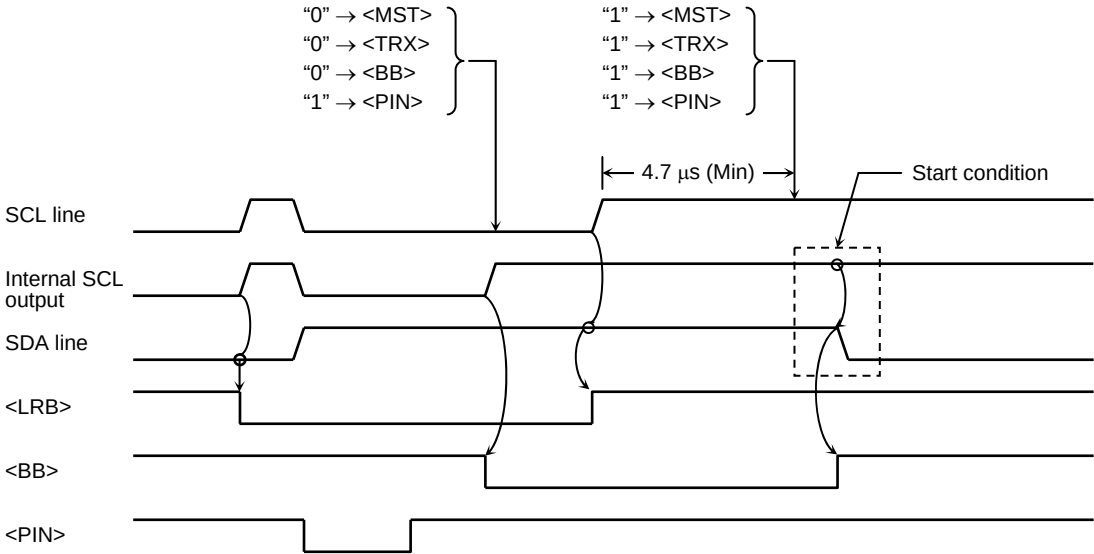


Figure 3.15.20 Timing chart for generate restart

Note: Don't write <MST> = “0”, when <MST> = “0” condition. (Cannot be restarted)

## 3.16 USB Controller

### 3.16.1 Outline

This USB controller (UDC) is designed to support a variety of serial links in the construction of a USB system.

The outline is as follows:

- (1) Compliant with USB rev1.1
- (2) Full-speed: 12 Mbps (low-speed (1.5 Mbps) not supported)
- (3) Auto bus enumeration with 384-byte descriptor RAM
- (4) Supports 3 kinds of transfer type: Control, interrupt and bulk
  - Endpoint 0: Control 64 bytes × 1-FIFO
  - Endpoint 1: BULK (out) 64 bytes × 2-FIFOs
  - Endpoint 2: BULK (in) 64 bytes × 2-FIFOs
  - Endpoint 3: Interrupt (in) 8 bytes × 1-FIFO
- (5) Built-in DPLL which generates sampling clock for receive data
- (6) Detecting and generating SOP, EOP, RESUME, RESET and TIMEOUT
- (7) Encoding and decoding NRZI data
- (8) Inserting and discarding stuffed bit
- (9) Detecting and checking CRC
- (10) Generating and decoding packet ID
- (11) Built-in power management function
- (12) Dual packet mode supported

Note1: The TMP92CF30 does not include the pull-up resistor necessary for D+pin. An external pull-up resistor plus software support is required.

Note2: There are some differences between our specifications and USB 1.1. Refer to check "3.16.11 Notice and Restrictions".

### 3.16.1.1 System Configuration

The USB controller (UDC) consists of the following 3 blocks.

1. 900/H1 CPU I/F (details given in Section 3.16.2, below).
2. UDC core block (DPLL, SIE, IFM and PWM), request controller, descriptor RAM and 4 endpoint FIFO (details given in Section 3.16.3, below).
3. USB transceiver

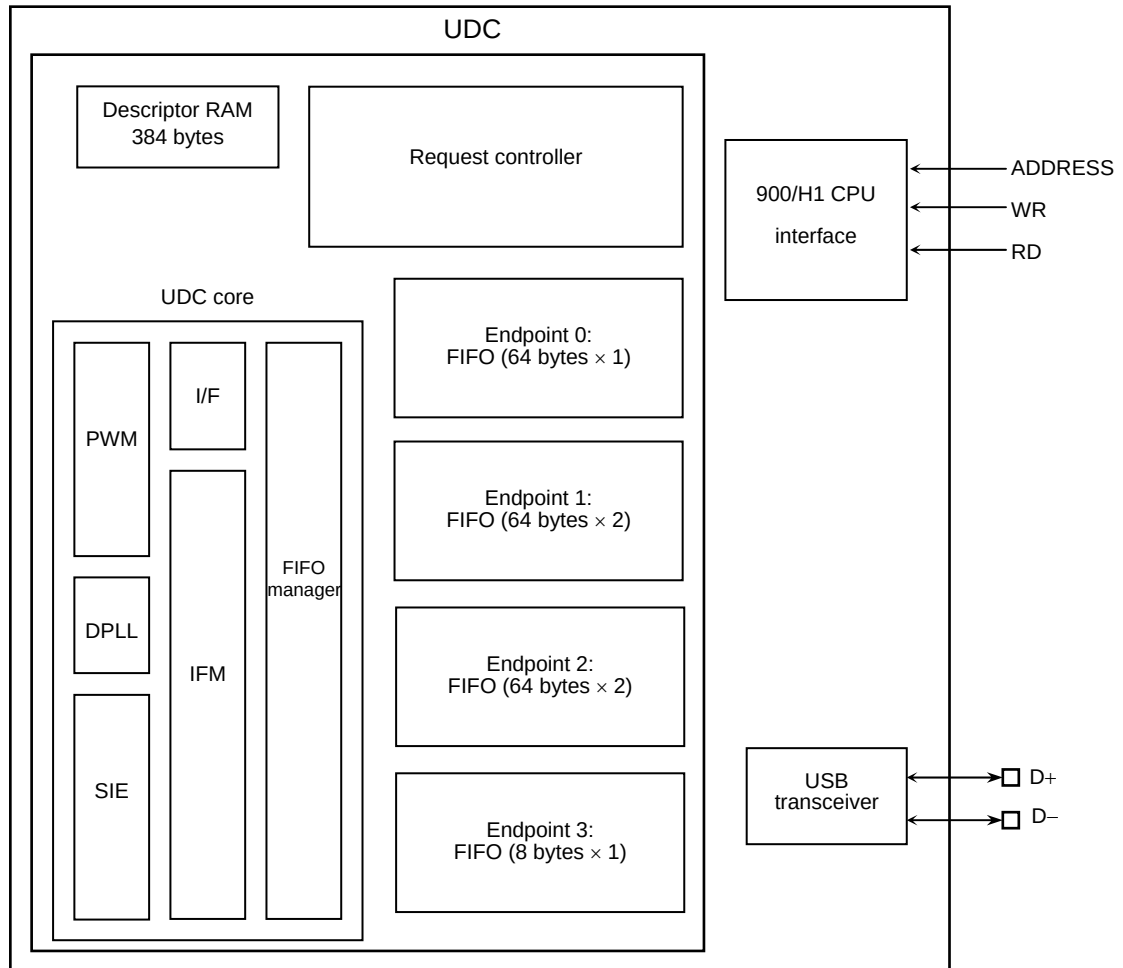
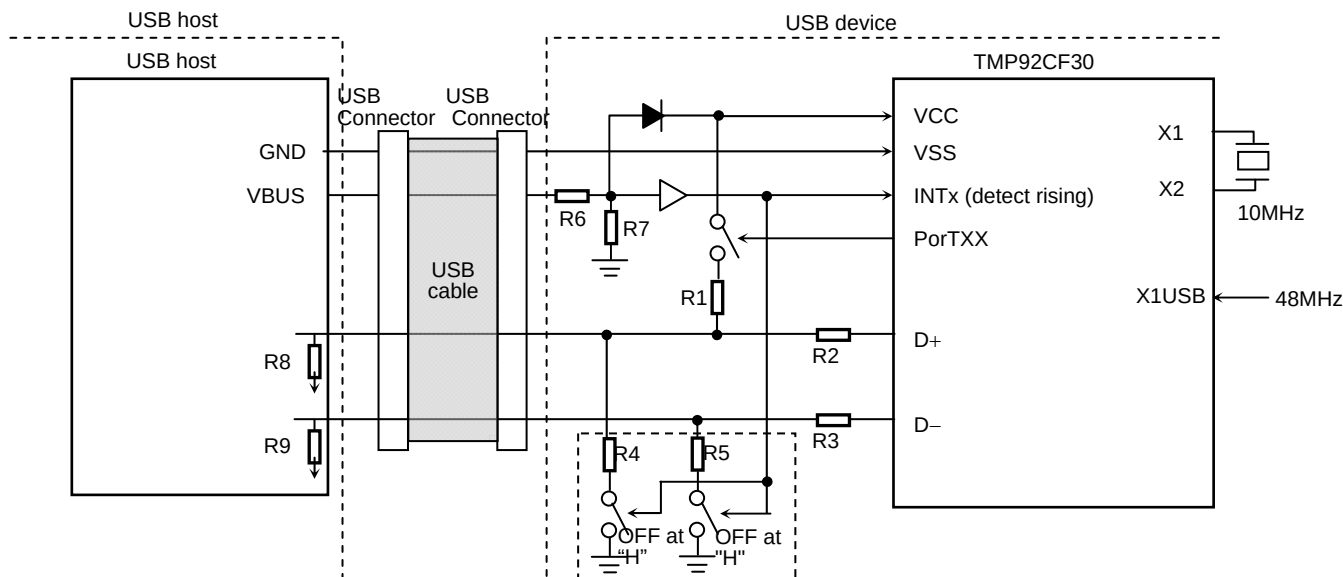


Figure 3.16.1 UDC Block Diagram

## 3.16.1.2 Example



The above setting is required if when using the TMP92CF30's USB controller.

1) Pull-up of D<sup>+</sup> pin

- In the USB standard, in Full Speed connection, the D<sup>+</sup> pin must be set to pull-up. The ON/OFF control of this pull-up must be by S/W.

Recommended value: R1=1.5kΩ

2) Add cascade resistor of D<sup>+</sup>, D<sup>-</sup> signal

- In the USB standard, for a D<sup>+</sup> or D<sup>-</sup> signal, a cascade resistor must be added to each signal. Recommended value : R2=27Ω, R3=27Ω

3) Flow current provision of the Connector connection and D<sup>+</sup> pin, D<sup>-</sup> pin

- For the D<sup>+</sup> and D<sup>-</sup> pin of the TMP92CF30, the level must be fixed for flow current provision when not in use (when not connected to host). In this case, the connector detection signal is used to control the pull-down resistor which determines the level.

Recommended value: R4=10kΩ, R5=10kΩ

- The example shows use of the connector detection method by using VBUS (5V voltage).

Note: Where waveform rise is slow, buffering of waveform is recommended.

Recommended value: R6=60kΩ, R7=100kΩ

(VBUS current consumption when suspended is <500μA)

## 4) Connection of 10MHz oscillator to X1,X2, or input 48MHz clock to X1USB

- When using USB with a combination of 10MHz external oscillator and internal PLL, the number of external hub stages which can be used is restricted by the accuracy of the internal (Max 3 stages).
- If 5 stages connection is required for external hub, it is required that input 48MHz clock from X1USB pin (Restriction  $\leq \pm 2500\text{ppm}$ .)

## 5) HOST side pull-down resistor

- In the USB standard, set pull-down D<sup>+</sup> pin and D<sup>-</sup> signal at USB\_HOST side.

Recommended value: R8=15k $\Omega$ , R9=15k $\Omega$

Note: The above connections and resistor values, etc, are given as examples only. Operation is not guaranteed. Please confirm the latest USB standar specifications and operations on your system.



### 3.16.2 900/H1 CPU I/F

The 900/H1 CPU I/F is a bridge between the 900/H1 CPU and the UDC. Its main functions are as follow.

- INTUSB (interrupt from UDC) generation
- A bridge for SFR
- USB clock control (48 MHz)

#### 3.16.2.1 SFRs

The 900/H1 CPU I/F incorporates the following SFRs to control the UDC and USB transceiver.

- USB control  
USBCR1 (USB control register 1)
- USB interrupt control  
USBINTFR1 (USB interrupt flag register 1)  
USBINTFR2 (USB interrupt flag register 2)  
USBINTFR3 (USB interrupt flag register 3)  
USBINTFR4 (USB interrupt flag register 4)  
USBINTMR1 (USB interrupt mask register 1)  
USBINTMR2 (USB interrupt mask register 2)  
USBINTMR3 (USB interrupt mask register 3)  
USBINTMR4 (USB interrupt mask register 4)

Table 3.16.1 900/H1 CPU I/F SFR

| Address | Read/Write | SFR Symbol |
|---------|------------|------------|
| 07F0H   | R/W        | USBINTFR1  |
| 07F1H   | R/W        | USBINTFR2  |
| 07F2H   | R/W        | USBINTFR3  |
| 07F3H   | R/W        | USBINTFR4  |
| 07F4H   | R/W        | USBINTMR1  |
| 07F5H   | R/W        | USBINTMR2  |
| 07F6H   | R/W        | USBINTMR3  |
| 07F7H   | R/W        | USBINTMR4  |
| 07F8H   | R/W        | USBCR1     |

## 3.16.2.2 USBCR1 Register

This register is used to set USB clock enables, transceiver enable etc.

|                   | 7           | 6        | 5      | 4 | 3 | 2 | 1     | 0       |
|-------------------|-------------|----------|--------|---|---|---|-------|---------|
| USBCR1<br>(07F8H) | bit Symbol  | TRNS_USE | WAKEUP |   |   |   | SPEED | USBCLKE |
|                   | Read/Write  | R/W      | R/W    |   |   |   | R/W   | R/W     |
|                   | Reset State | 0        | 0      |   |   |   | 1     | 0       |
|                   | Function    |          |        |   |   |   |       |         |

- TRNS\_USE (Bit7)

- 0: Disable USB transceiver
- 1: Enable USB transceiver

Always set to “1” on the application using USB.

- WAKEUP (Bit6)

- 0: –
- 1: Start remote-wakeup function

When the remote-wakeup function is needed, first check Current\_Config<REMOTE WAKEUP>.

If <REMOTE WAKEUP> = “1” (meaning SUSPEND-status), write “1”, and “0” to <WAKEUP>. This will initiate the remote-wakeup function.

If <REMOTE WAKEUP> = “0” or EP0, 1, 2, 3\_STATUS<SUSPEND> = “0”, do not write “1” to <WAKEUP>.

- SPEED (Bit1)

- 1: Full speed (12 MHz)
- 0: Reserved

This bit selects USB speed.

Always set to “1”.

- USBCLKE (Bit0)

- 0: Disable USB clock
- 1: Enable USB clock

This bit controls supply of USB clock.

The USB clock (“f<sub>USB</sub>”: 48MHz) is generated by an internal PLL. When the USB is started, write “1” to <USBCLKE> after confirming PLL lock up is terminated.

Also, write “0” to <USBCLKE> before stopping the PLL.

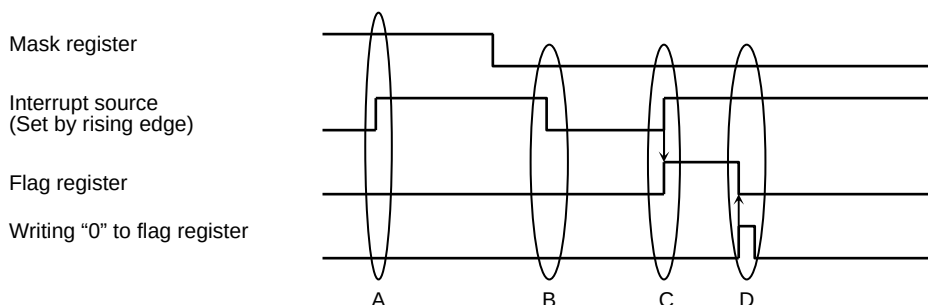
### 3.16.2.3 USBINTFRn, MRn Register

These SFRs control the INTUSB (only one interrupt to CPU) using the 23 interrupt sources output by the UDC.

The USBINTMRn are mask registers and the USBINTFRn are flag registers. In the INTUSB routine, execute operations according to generated interrupt source after checking USBINTFRn.

The common specification for all MASK and FLAG registers is shown below.

(Common specifications for all mask and flag registers.)



A: The flag register is not set because mask register = "1".

B: The flag register is not set because interrupt source changes "1" → "0".

C: The flag register is set because mask register = "0" and interrupt source changes "0" → "1".

D: The flag register is reset to "0" by writing "0" to flag register.

Note 1: The "INTUSB generated number" and "bit number which is set to flag register" are not always equal. In the INTUSB interrupt routine, clear FLAG register (USBINTFRn) after checking it. The interrupt request flag, which occurs between the INTUSB interrupt routine and flag register (USBINTFRn) read, is kept in the interrupt controller.

Therefore, after returning from the interrupt routine, the CPU jumps to INTUSB interrupt routine again. Software support is required to avoid ending in an error routine when none of the bits in the flag register (USBINTFRn) is set to "1".

Note 2: Disable INTUSB (write 00H to INTEUSB register) before writing to USBINTMRn or USBINTFRn.

|                      | 7                                                            | 6            | 5       | 4          | 3           | 2         | 1 | 0 |
|----------------------|--------------------------------------------------------------|--------------|---------|------------|-------------|-----------|---|---|
| USBINTFR1<br>(07F0H) | INT_URST_STR                                                 | INT_URST_END | INT_SUS | INT_RESUME | INT_CLKSTOP | INT_CLKON |   |   |
| Read/Write           | R/W                                                          | R/W          | R/W     | R/W        | R/W         | R/W       |   |   |
| Reset State          | 0                                                            | 0            | 0       | 0          | 0           | 0         |   |   |
| Function             | When read 0: Not generate interrupt<br>1: Generate interrupt |              |         |            |             |           |   |   |

Note: The above interrupts can release Halt state from IDLE2 and IDLE1 mode. (STOP mode cannot be released)

\*Those 6 interrupts of all 24 INTUSB sources can release Halt state from IDLE1 mode. Therefore, a low power dissipation system can be built. However, the method of use is limited as below.

Shift to IDLE1 mode :

Execute Halt instruction when the INT\_SUS or INT\_CLKSTOP flag is "1" (SUSPEND state)

Release from IDLE1 mode :

Release Halt state by INT\_RESUME or INT\_CLKON request (request of release SUSPEND)

Release Halt state by INT\_URST\_STR or INT\_URST\_request (request of RESET)

- INT\_URST\_STR (Bit7)

This is the flag register for INT\_URST\_STR ("USB reset" start - interrupt).

This is set to "1" when the UDC started to receive a "USB reset" signal from a USB-host.

An application program has to initialize the whole UDC with this interrupt.

- INT\_URST\_END (Bit6)

This is the flag register for INT\_URST\_END ("USB reset" end - interrupt).

This is set to "1" when the UDC receives a "USB reset end" signal from a USB-host.

- INT\_SUS (Bit5)

This is the flag register for INT\_SUS (suspend - interrupt).

This is set to "1" when the USB changes to "suspend status".

- INT\_RESUME (Bit4)

This is the flag register for INT\_RESUME (resume - interrupt).

This is set to "1" when the USB changes to "resume status".

- INT\_CLKSTOP (Bit3)

This is the flag register for INT\_CLKSTOP (enables stopping of the clock supply - interrupt).

This is set to "1" after the USB changes to "suspend status". Set USBCCR1<USBCLKE> to "0" to stop the clock after detecting this interrupt if needed.

- INT\_CLKON (Bit2)

This is the flag register for INT\_CLKON (enabled starting clock supply - interrupt).

This is set to "1" after changing to "resume status" or when the UDC started to receive a "USB reset" signal from a USB-host. In case the clock has been stopped, set USBCCR1<USBCLKE> to "1" to start the clock after detecting this interrupt if needed.

USBINTFR2  
(07F1H)  
Prohibit to  
read  
-modify  
-write

Note: The above interrupt can release Halt state from IDLE2 mode. (IDLE1 and STOP mode cannot be released.)

USBINTFR3  
(07F2H)

Prohibit to  
read  
-modify  
-write

Note: The above interrupt can release Halt state from IDLE2 mode. (IDLE1 and STOP mode cannot be released.)

- **EPx\_FULL\_A/B:**
  - (When transmitting)  
This is set to “1” when CPU full write data to FIFO\_A/B.
  - (When receiving)  
This is set to “1” when UDC full receive data to FIFO\_A/B.
- **EPx\_Empty\_A/B:**
  - (When transmitting)  
This is set to “1” when FIFO become empty after transmission.
  - (When receiving)  
This is set to “1” when FIFO becomes empty after CPU reads all data from FIFO.

Note: The EPx\_FULL\_A/B and EPx\_Empty\_A/B flags are not status flags. Therefore, check DATASET register to determine if the FIFO-status is needed.

|                      | 7                                                                                                | 6       | 5        | 4         | 3        | 2        | 1        | 0 |
|----------------------|--------------------------------------------------------------------------------------------------|---------|----------|-----------|----------|----------|----------|---|
| USBINTFR4<br>(07F3H) | INT_SETUP                                                                                        | INT_EP0 | INT_STAS | INT_STASN | INT_EP1N | INT_EP2N | INT_EP3N |   |
| Read/Write           | R/W                                                                                              | R/W     | R/W      | R/W       | R/W      | R/W      | R/W      |   |
| Reset State          | 0                                                                                                | 0       | 0        | 0         | 0        | 0        | 0        |   |
| Function             | When read 0: Not generate interrupt<br>1: Generate interrupt<br>When write 0: Clear flag<br>1: – |         |          |           |          |          |          |   |

Note: The above interrupt can release Halt state from IDLE2 mode. (IDLE1 and STOP mode cannot be released.)

- INT\_SETUP (Bit7)

This is the flag register for INT\_SETUP (setup - interrupt).

This is set to “1” when the UDC receives a request that S/W (software) control is needed from USB host.

Using S/W (INT\_SETUP routine), first read 8-byte device requests from the UDC and execute operation according to each request.

- INT\_EP0 (Bit6)

This is the flag register for INT\_EP0 (received data of the data phase for Control transfer type - interrupt).

This is set to “1” when the UDC receives data of the data phase for Control transfer type. If this interrupt occurs during Control write transfer, data reading from FIFO is needed. If this interrupt occurs during Control read transfer, transmission data writing to FIFO is needed.

In some cases, the host may not assert “ACK” of the last packet in the data stage. In this case, this interrupt cannot be generated. Therefore, ignore this interrupt if it occurs after the last packet data has been written in the data stage because the transmission data number is specified by the host, or it depends on the capacity of the device.

- INT\_STAS (Bit5)

This is the flag register for INT\_STAS (status stage end - interrupt).

This is set to “1” when the status stage ends.

If this interrupt is generated, it means that request ended normally.

If this interrupt is not generated and INT\_SETUP is generated, EP0\_STATUS <STAGE\_ERR> is set to “1”, and it means that request did not end normally.

- INT\_STASN (Bit4)

This is the flag register for INT\_STASN (change host status stage - interrupt).

This is set to “1” when the USB host changes to status stage at the Control read transfer. This interrupt is needed if data length is less than wLength (specified by the host).

- INT\_EPxN (Bit3, 2, 1)

This is the flag register for INT\_EPxN (NAK acknowledge to the USB host - interrupt).

This is set to “1” when the Endpoint1, 2 and 3 transmit NAK.

USBINTMR1  
(07F4H)

- **MSK\_URST\_STR (Bit7)**  
This is the mask register for USBINTFR1<INT\_URST\_STR>.
- **MSK\_URST\_END (Bit6)**  
This is the mask register for USBINTFR1<INT\_URST\_END>.
- **MSK\_SUS (Bit5)**  
This is the mask register for USBINTFR1<INT\_SUS>.
- **MSK\_RESUME (Bit4)**  
This is the mask register for USBINTFR1<INT\_RESUME>.
- **MSK\_CLKSTOP (Bit3)**  
This is the mask register for USBINTFR1<INT\_CLKSTOP>.
- **MSK\_CLKON (Bit2)**  
This is the mask register for USBINTFR1<INT\_CLKON>.



USBINTMR2  
(07F5H)

- This is the mask register for USBINTFR2<EPx\_FULL\_A/B> or <EPx\_Empty\_A/B>.

USBINTMR3  
(07F6H)

- This is the mask register for USBINTFR3<EP3\_FULL\_A> or <EP3\_Empty\_A>.

USBINTMR4  
(07F7H)

- **MSK\_SETUP (Bit7)**  
This is the mask register for USBINTFR4<INT\_SETUP>.
- **MSK\_EP0 (Bit6)**  
This is the mask register for USBINTFR4<INT\_EP0>.
- **MSK\_STAS (Bit5)**
- This is the mask register for USBINTFR4<INT\_STAS>.
- **MSK\_STASN (Bit4)**  
This is the mask register for USBINTFR4<INT\_STASN>.
- **MSK\_EP1N (Bit3)**  
This is the mask register for USBINTFR4<INT\_EP1N>.
- **MSK\_EP2N (Bit2)**  
This is the mask register for USBINTFR4<INT\_EP2N>.
- **MSK\_EP3N (Bit1)**  
This is the mask register for USBINTFR4<INT\_EP3N>.

### 3.16.3 UDC CORE

#### 3.16.3.1 SFRs

The UDC CORE has the following SFRs to control the UDC and USB transceiver.

##### a) FIFO

Endpoint 0 to 3 FIFO register

##### b) Device request

|               |          |           |          |
|---------------|----------|-----------|----------|
| bmRequestType | register | bRequest  | register |
| wValue_L      | register | wValue_H  | register |
| wIndex_L      | register | wIndex_H  | register |
| wLength_L     | register | wLength_H | register |

##### c) Status

|                 |          |           |          |
|-----------------|----------|-----------|----------|
| Current_Config  | register | USB_STATE | register |
| StandardRequest | register | Request   | register |
| EPx_STATUS      | register |           |          |

##### d) Setup

|                       |          |              |          |
|-----------------------|----------|--------------|----------|
| EPx_BCS               | register | EPx_SINGLE   | register |
| Standard Request Mode | register | Request Mode | register |
| Descriptor RAM        | register | PortStatus   | register |

##### e) Control

|                |          |             |          |
|----------------|----------|-------------|----------|
| EPx_MODE       | register | EOP         | register |
| COMMAND        | register | INT_Control | register |
| Setup Received | register | USBREADY    | register |

##### f) Others

|              |          |              |          |
|--------------|----------|--------------|----------|
| ADDRESS      | register | DATASET      | register |
| EPx_SIZE_L_A | register | EPx_SIZE_H_A | register |
| EPx_SIZE_L_B | register | EPx_SIZE_H_B | register |
| FRAME_L      | register | FRAME_H      | register |
| USBBUFF TEST | register |              |          |

Table 3.16.2 UDC CORE SFRs (1/3)

| Address | Read/Write | SFR Symbol        |
|---------|------------|-------------------|
| 0500H   | R/W        | Descriptor RAM0   |
| 0501H   | R/W        | Descriptor RAM1   |
| 0502H   | R/W        | Descriptor RAM2   |
| 0503H   | R/W        | Descriptor RAM3   |
| ⋮       | ⋮          | ⋮                 |
| 067DH   | R/W        | Descriptor RAM381 |
| 067EH   | R/W        | Descriptor RAM382 |
| 067FH   | R/W        | Descriptor RAM383 |
| 0780H   | R/W        | ENDPOINT0         |
| 0781H   | R/W        | ENDPOINT1         |
| 0782H   | R/W        | ENDPOINT2         |
| 0783H   | R/W        | ENDPOINT3         |
| *0784H  | R/W        | ENDPOINT4         |
| *0785H  | R/W        | ENDPOINT5         |
| *0786H  | R/W        | ENDPOINT6         |
| *0787H  | R/W        | ENDPOINT7         |
| 0788H   | —          | Reserved          |
| 0789H   | R/W        | EP1_MODE          |
| 078AH   | R/W        | EP2_MODE          |
| 078BH   | R/W        | EP3_MODE          |
| *078CH  | R/W        | EP4_MODE          |
| *078DH  | R/W        | EP5_MODE          |
| *078EH  | R/W        | EP6_MODE          |
| *078FH  | R/W        | EP7_MODE          |
| 0790H   | R          | EP0_STATUS        |
| 0791H   | R          | EP1_STATUS        |
| 0792H   | R          | EP2_STATUS        |
| 0793H   | R          | EP3_STATUS        |
| *0794H  | R          | EP4_STATUS        |
| *0795H  | R          | EP5_STATUS        |
| *0796H  | R          | EP6_STATUS        |
| *0797H  | R          | EP7_STATUS        |
| 0798H   | R          | EP0_SIZE_L_A      |
| 0799H   | R          | EP1_SIZE_L_A      |
| 079AH   | R          | EP2_SIZE_L_A      |
| 079BH   | R          | EP3_SIZE_L_A      |
| *079CH  | R          | EP4_SIZE_L_A      |
| *079DH  | R          | EP5_SIZE_L_A      |
| *079EH  | R          | EP6_SIZE_L_A      |
| *079FH  | R          | EP7_SIZE_L_A      |
| 07A1H   | R          | EP1_SIZE_L_B      |
| 07A2H   | R          | EP2_SIZE_L_B      |
| 07A3H   | R          | EP3_SIZE_L_B      |
| *07A4H  | R          | EP4_SIZE_L_B      |
| *07A5H  | R          | EP5_SIZE_L_B      |
| *07A6H  | R          | EP6_SIZE_L_B      |
| *07A7H  | R          | EP7_SIZE_L_B      |
| 07A8H   | —          | Reserved          |

Note: "\*" is not used in the TMP92CF30.

Table 3.16.3 UDC CORE SFRs (2/3)

| Address | Read/Write | SFR Symbol            |
|---------|------------|-----------------------|
| 07A9H   | R          | EP1_SIZE_H_A          |
| 07AAH   | R          | EP2_SIZE_H_A          |
| 07ABH   | R          | EP3_SIZE_H_A          |
| *07ACH  | R          | EP4_SIZE_H_A          |
| *07ADH  | R          | EP5_SIZE_H_A          |
| *07AEH  | R          | EP6_SIZE_H_A          |
| *07AFH  | R          | EP7_SIZE_H_A          |
| 07B1H   | R          | EP1_SIZE_H_B          |
| 07B2H   | R          | EP2_SIZE_H_B          |
| 07B3H   | R          | EP3_SIZE_H_B          |
| *07B4H  | R          | EP4_SIZE_H_B          |
| *07B5H  | R          | EP5_SIZE_H_B          |
| *07B6H  | R          | EP6_SIZE_H_B          |
| *07B7H  | R          | EP7_SIZE_H_B          |
| 07C0H   | R          | bmRequestType         |
| 07C1H   | R          | bRequest              |
| 07C2H   | R          | wValue_L              |
| 07C3H   | R          | wValue_H              |
| 07C4H   | R          | wIndex_L              |
| 07C5H   | R          | wIndex_H              |
| 07C6H   | R          | wLength_L             |
| 07C7H   | R          | wLength_H             |
| 07C8H   | W          | Setup Received        |
| 07C9H   | R          | Current_Config        |
| 07CAH   | R          | Standard Request      |
| 07CBH   | R          | Request               |
| 07CCH   | R          | DATASET1              |
| 07CDH   | R          | DATASET2              |
| 07CEH   | R          | USB_STATE             |
| 07CFH   | W          | EOP                   |
| 07D0H   | W          | COMMAND               |
| 07D1H   | R/W        | EPx_SINGLE1           |
| *07D2H  | R/W        | EPx_SINGLE2           |
| 07D3H   | R/W        | EPx_BCS1              |
| *07D4H  | R/W        | EPx_BCS2              |
| 07D5H   | —          | Reserved              |
| 07D6H   | R/W        | INT_Control           |
| 07D7H   | —          | Reserved              |
| 07D8H   | R/W        | Standard Request Mode |
| 07D9H   | R/W        | Request Mode          |
| 07DAH   | —          | Reserved              |
| 07DBH   | —          | Reserved              |
| 07DCH   | —          | Reserved              |
| 07DDH   | —          | Reserved              |
| 07DEH   | W          | ID_CONTROL            |
| 07DFH   | R          | ID_STATE              |

Note: “\*” is not used in the TMP92CF30.

Table 3.16.4 UDC CORE SFRs (3/3)

| Address | Read/Write | SFR Symbol           |
|---------|------------|----------------------|
| 07E0H   | R/W        | Port_Status          |
| 07E1H   | R          | FRAME_L              |
| 07E2H   | R          | FRAME_H              |
| 07E3H   | R          | ADDRESS              |
| *07E4H  | —          | Reserved             |
| *07E5H  | —          | Reserved             |
| 07E6H   | R/W        | USBREADY             |
| *07E7H  | —          | Reserved             |
| 07E8H   | W          | Set Descriptor STALL |

Note: “\*” is not used in the TMP92CF30.

## 3.16.3.2 EPx\_FIFO Register (x: 0 to 3)

This register is prepared for each endpoint independently.

This is the window register from or to FIFO RAM.

In the auto bus enumeration, the request controller in UDC sets the mode, which is defined by the endpoint descriptor for each endpoint automatically. By this means, each endpoint is automatically set to each voluntary direction.

|                      |             | 7         | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|----------------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Endpoint0<br>(0780H) | bit Symbol  | EP0_DATA7 | EP0_DATA6 | EP0_DATA5 | EP0_DATA4 | EP0_DATA3 | EP0_DATA2 | EP0_DATA1 | EP0_DATA0 |
|                      | Read/Write  | R/W       | R/W       | R/W       | R/W       | R/W       | R/W       | R/W       | R/W       |
|                      | Reset State | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |

|                      |             | 7         | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|----------------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Endpoint1<br>(0781H) | bit Symbol  | EP1_DATA7 | EP1_DATA6 | EP1_DATA5 | EP1_DATA4 | EP1_DATA3 | EP1_DATA2 | EP1_DATA1 | EP1_DATA0 |
|                      | Read/Write  | R/W       | R/W       | R/W       | R/W       | R/W       | R/W       | R/W       | R/W       |
|                      | Reset State | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |

|                      |             | 7         | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|----------------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Endpoint2<br>(0782H) | bit Symbol  | EP2_DATA7 | EP2_DATA6 | EP2_DATA5 | EP2_DATA4 | EP2_DATA3 | EP2_DATA2 | EP2_DATA1 | EP2_DATA0 |
|                      | Read/Write  | R/W       | R/W       | R/W       | R/W       | R/W       | R/W       | R/W       | R/W       |
|                      | Reset State | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |

|                      |             | 7         | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|----------------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Endpoint3<br>(0783H) | bit Symbol  | EP3_DATA7 | EP3_DATA6 | EP3_DATA5 | EP3_DATA4 | EP3_DATA3 | EP3_DATA2 | EP3_DATA1 | EP3_DATA0 |
|                      | Read/Write  | R/W       | R/W       | R/W       | R/W       | R/W       | R/W       | R/W       | R/W       |
|                      | Reset State | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |

Note: Read or write to these window registers using 1-byte load instructions only, since each register has only a 1-byte address. Do not use load instructions of 2 bytes or 4 bytes.

The device request that is received from the USB host is stored in the to following 8-byte registers:

bmRequestType, bRequest, wValue\_L, wValue\_H, wIndex\_L, wIndex\_H, wLength\_L and wLength\_H. These are updated whenever a new SETUP token is received from the host.

When the UDC receives without error, INT\_SETUP interrupt is asserted, meaning the new device request has been received.

There is also request which is operated automatically by the UDC, depending on the request received.

In that case, the UDC does not assert the INT\_SETUP interrupt. Any request which the UDC is currently operating can be checked by reading STANDARD\_REQUEST\_FLAG and REQUEST\_FLAG.

## 3.16.3.3 bmRequestType Register

This register shows the bmRequestType field of the device request.

|                          | 7         | 6         | 5         | 4          | 3          | 2          | 1          | 0          |
|--------------------------|-----------|-----------|-----------|------------|------------|------------|------------|------------|
| bmRequestType<br>(07C0H) | DIRECTION | REQ_TYPE1 | REQ_TYPE0 | RECIPIENT4 | RECIPIENT3 | RECIPIENT2 | RECIPIENT1 | RECIPIENT0 |
| Read/Write               | R         | R         | R         | R          | R          | R          | R          | R          |
| Reset State              | 0         | 0         | 0         | 0          | 0          | 0          | 0          | 0          |

## DIRECTION (Bit7)

0: from host to device  
1: from device to host

## REQ\_TYPE [1:0] (Bit6 to bit5)

00: Standard  
01: Class  
10: Vendor  
11: (Reserved)

## RECIPIENT [4:0] (Bit4 to bit0)

00000: Device  
00001: Interface  
00010: Endpoint  
00011: etc.  
Others: (Reserved)

## 3.16.3.4 bRequest Register

This register shows the bRequest field of the device request.

|                     | 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|---------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| bRequest<br>(07C1H) | REQUEST7 | REQUEST6 | REQUEST5 | REQUEST4 | REQUEST3 | REQUEST2 | REQUEST1 | REQUEST0 |
| Read/Write          | R        | R        | R        | R        | R        | R        | R        | R        |
| Reset State         | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        |

(Standard)

00000000: GET\_STATUS  
00000001: CLEAR\_FEATURE  
00000010: Reserved  
00000011: SET\_FEATURE  
00000100: Reserved  
00000101: SET\_ADDRESS  
00000110: GET\_DESCRIPTOR  
00000111: SET\_DESCRIPTOR  
00001000: GET\_CONFIGURATION  
00001001: SET\_CONFIGURATION  
00001010: GET\_INTERFACE  
00001011: SET\_INTERFACE  
00001100: SYNCH\_FRAME

(Printer class)

00000000: GET\_DEVICE\_ID  
00000001: GET\_PORT\_STATUS  
00000010: SOFT\_RESET



## 3.16.3.5 wValue Register

There are 2 registers; the wValue\_L register and wValue\_H register. wValue\_L shows the lower-byte of the wValue field of the device request, and wValue\_H register shows the upper byte.

|                     | 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|---------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| wValue_L<br>(07C2H) | VALUE_L7 | VALUE_L6 | VALUE_L5 | VALUE_L4 | VALUE_L3 | VALUE_L2 | VALUE_L1 | VALUE_L0 |
| Read/Write          | R        | R        | R        | R        | R        | R        | R        | R        |
| Reset State         | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        |

|                     | 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|---------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| wValue_H<br>(07C3H) | VALUE_H7 | VALUE_H6 | VALUE_H5 | VALUE_H4 | VALUE_H3 | VALUE_H2 | VALUE_H1 | VALUE_H0 |
| Read/Write          | R        | R        | R        | R        | R        | R        | R        | R        |
| Reset State         | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        |

## 3.16.3.6 wIndex Register

There are 2 registers, the wIndex\_L register and wIndex\_H register. the wIndex\_L register shows the lower byte of the wIndex field of the device request, and wIndex\_H register shows the upper byte.

These are usually used to transfer index or offset.

|                     | 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|---------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| wIndex_L<br>(07C4H) | INDEX_L7 | INDEX_L6 | INDEX_L5 | INDEX_L4 | INDEX_L3 | INDEX_L2 | INDEX_L1 | INDEX_L0 |
| Read/Write          | R        | R        | R        | R        | R        | R        | R        | R        |
| Reset State         | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        |

|                     | 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|---------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| wIndex_H<br>(07C5H) | INDEX_H7 | INDEX_H6 | INDEX_H5 | INDEX_H4 | INDEX_H3 | INDEX_H2 | INDEX_H1 | INDEX_H0 |
| Read/Write          | R        | R        | R        | R        | R        | R        | R        | R        |
| Reset State         | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        |

## 3.16.3.7 wLength Register

There are 2 registers, the wLength\_L register and wLength\_H register. The wLength\_L register shows the lower-byte of the wLength field of the device request and wLength\_H register shows the upper byte.

In the case of data phase, these registers show the byte number to transfer.

|                      | 7         | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|----------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| wLength_L<br>(07C6H) | LENGTH_L7 | LENGTH_L6 | LENGTH_L5 | LENGTH_L4 | LENGTH_L3 | LENGTH_L2 | LENGTH_L1 | LENGTH_L0 |
| Read/Write           | R         | R         | R         | R         | R         | R         | R         | R         |
| Reset State          | 0         | 0         | 0         | 0         | 0         | 0         | 0         | 0         |

|                      | 7         | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|----------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| wLength_H<br>(07C7H) | LENGTH_H7 | LENGTH_H6 | LENGTH_H5 | LENGTH_H4 | LENGTH_H3 | LENGTH_H2 | LENGTH_H1 | LENGTH_H0 |
| Read/Write           | R         | R         | R         | R         | R         | R         | R         | R         |
| Reset State          | 0         | 0         | 0         | 0         | 0         | 0         | 0         | 0         |

### 3.16.3.8 Setup Received Register

This register informs the UDC that an application program has recognized the INT\_SETUP interrupt.

|                          |             | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|--------------------------|-------------|----|----|----|----|----|----|----|----|
|                          |             | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| SetupReceived<br>(07C8H) | bit Symbol  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|                          | Read/Write  | W  | W  | W  | W  | W  | W  | W  | W  |
|                          | Reset State | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

If this register is accessed by an application program, the UDC disables access to the EP0's FIFO RAM because the UDC recognizes the device request has been received.

This is to protect data stored in the EP0 in the time between the completion of the previous device request and the recognition by the application program of the INT\_SETUP interrupt relating to a new request f.

Therefore, write "00H" to this register when the device request in INT\_SETUP routine is recognized.

Note : A recovery time of 2clock at 12MHz is needed after writing to this register in order to access EP0\_FIFO.

### 3.16.3.9 Current\_Config Register

This register shows the present value that is set by SET\_CONFIGURATION and SET\_INTERFACE.

|                           |             | 7            | 6 | 5            | 4            | 3            | 2            | 1         | 0         |
|---------------------------|-------------|--------------|---|--------------|--------------|--------------|--------------|-----------|-----------|
|                           |             | REMOTEWAKEUP |   | ALTERNATE[1] | ALTERNATE[0] | INTERFACE[1] | INTERFACE[0] | CONFIG[1] | CONFIG[0] |
| Current_Config<br>(07C9H) | bit Symbol  | REMOTEWAKEUP |   | ALTERNATE[1] | ALTERNATE[0] | INTERFACE[1] | INTERFACE[0] | CONFIG[1] | CONFIG[0] |
|                           | Read/Write  | R            |   | R            | R            | R            | R            | R         | R         |
|                           | Reset State | 0            |   | 0            | 0            | 0            | 0            | 0         | 0         |

#### CONFIG[1:0] (Bit1 to bit0)

|                  |                                  |
|------------------|----------------------------------|
| 00: UNCONFIGURED | Set to UNCONFIGURED by the host. |
| 01: CONFIGURED1  | Set to CONFIGURED 1 by the host. |
| 10: CONFIGURED2  | Set to CONFIGURED 2 by the host. |

#### INTERFACE[1:0] (Bit3 to bit2)

|                |                                 |
|----------------|---------------------------------|
| 00: INTERFACE0 | Set to INTERFACE 0 by the host. |
| 01: INTERFACE1 | Set to INTERFACE 1 by the host. |
| 10: INTERFACE2 | Set to INTERFACE 2 by the host. |

#### ALTERNATE[1:0] (Bit5 to bit4)

|                |                                 |
|----------------|---------------------------------|
| 00: ALTERNATE0 | Set to ALTERNATE 0 by the host. |
| 01: ALTERNATE1 | Set to ALTERNATE 1 by the host. |
| 10: ALTERNATE2 | Set to ALTERNATE 2 by the host. |

#### REMOTE WAKEUP (Bit7)

|            |                                     |
|------------|-------------------------------------|
| 0: Disable | Disabled remote wakeup by the host. |
| 1: Enable  | Enabled remote wakeup by the host.  |

Note1: CONFIG, INTERFACE and ALTERNATE each support 3 kinds (0,1 and 2).

Note2: If each request is controlled by S/W, this register is not set.

## 3.16.3.10 Standard Request Register

This register shows the standard request currently being executed.

Any bit which is set to “1” shows a request currently being executed.

|                             | 7           | 6           | 5           | 4        | 3        | 2            | 1         | 0         |          |
|-----------------------------|-------------|-------------|-------------|----------|----------|--------------|-----------|-----------|----------|
| Standard Request<br>(07CAH) | bit Symbol  | S_INTERFACE | G_INTERFACE | S_CONFIG | G_CONFIG | G_DESCRIPTOR | S_FEATURE | C_FEATURE | G_STATUS |
|                             | Read/Write  | R           | R           | R        | R        | R            | R         | R         | R        |
|                             | Reset State | 0           | 0           | 0        | 0        | 0            | 0         | 0         | 0        |

|              |                             |
|--------------|-----------------------------|
| S_INTERFACE  | (Bit 7) : SET_INTERFACE     |
| G_INTERFACE  | (Bit 6) : GET_INTERFACE     |
| S_CONFIG     | (Bit 5) : SET_CONFIGURATION |
| G_CONFIG     | (Bit 4) : GET_CONFIGURATION |
| G_DESCRIPTOR | (Bit 3) : GET_DESCRIPTOR    |
| S_FEATURE    | (Bit 2) : SET_FEATURE       |
| C_FEATURE    | (Bit 1) : CLEAR_FEATURE     |
| G_STATUS     | (Bit 0) : GET_STATUS        |

## 3.16.3.11 Request Register

This register shows the device request currently being executed.

Any bit which is set to “1” shows a request currently being executed.

|                    |             |   |            |            |             |        |       |            |          |
|--------------------|-------------|---|------------|------------|-------------|--------|-------|------------|----------|
|                    |             | 7 | 6          | 5          | 4           | 3      | 2     | 1          | 0        |
| Request<br>(07CBH) | bit Symbol  |   | SOFT_RESET | G_PORT_STS | G_DEVICE_ID | VENDOR | CLASS | ExSTANDARD | STANDARD |
|                    | Read/Write  |   | R          | R          | R           | R      | R     | R          | R        |
|                    | Reset State |   | 0          | 0          | 0           | 0      | 0     | 0          | 0        |

|             |                                                                               |
|-------------|-------------------------------------------------------------------------------|
| SOFT_RESET  | (Bit 6) : SOFT_RESET                                                          |
| G_PORT_STS  | (Bit 5) : GET_PORT_STATUS                                                     |
| G_DEVICE_ID | (Bit 4) : GET_DEVICE_ID                                                       |
| VENDOR      | (Bit 3) : Vendor class request                                                |
| CLASS       | (Bit 2) : Class request                                                       |
| ExSTANDARD  | (Bit 1) : Auto Bus Enumeration not supported<br>(SET_DESCRIPTOR, SYNCH_FRAME) |
| STANDARD    | (Bit 0) : Standard request                                                    |

## 3.16.3.12 DATASET Register

This register shows whether FIFO contains data or not.

The application program can access this register to check whether FIFO contains data or not.

In the receiving status, when valid data transfer from the USB host has finished, the bit which corresponds to the corresponding endpoint is set to “1” and an interrupt generated. And, when the application reads the 1-packet data, this bit is cleared to “0”. In transmit status, when it has completed the 1-packet data transfer to FIFO, this bit is set to “1”. And when valid data is transferred to the USB host, this bit is cleared to “0” and an interrupt generated.

|                     |             |            |            |            |            |            |            |   |            |
|---------------------|-------------|------------|------------|------------|------------|------------|------------|---|------------|
| DATASET1<br>(07CCH) |             | 7          | 6          | 5          | 4          | 3          | 2          | 1 | 0          |
|                     | bit Symbol  | EP3_DSET_B | EP3_DSET_A | EP2_DSET_B | EP2_DSET_A | EP1_DSET_B | EP1_DSET_A |   | EP0_DSET_A |
|                     | Read/Write  | R          | R          | R          | R          | R          | R          |   | R          |
|                     | Reset State | 0          | 0          | 0          | 0          | 0          | 0          |   | 0          |

|                     |             |            |            |            |            |            |            |            |            |
|---------------------|-------------|------------|------------|------------|------------|------------|------------|------------|------------|
| DATASET2<br>(07CDH) |             | 7          | 6          | 5          | 4          | 3          | 2          | 1          | 0          |
|                     | bit Symbol  | EP7_DSET_B | EP7_DSET_A | EP6_DSET_B | EP6_DSET_A | EP5_DSET_B | EP5_DSET_A | EP4_DSET_B | EP4_DSET_A |
|                     | Read/Write  | R          | R          | R          | R          | R          | R          | R          | R          |
|                     | Reset State | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          |

Note: DATASET1<EP3\_DSET\_B>, DATASET2 registers are not used in the TMP92CF30.

- Single packet mode  
(DATASET1: Bit0, bit2, bit4 and bit6     DATASET2: Bit0, bit2, bit4 and bit6)

These bits show whether FIFO of the corresponding endpoint has data or not.

In receive mode endpoint, if the corresponding endpoint bit is “1”, FIFO contains data to be read. Access EPx\_SIZE register, determine the size of the data that should be read, and read data of this size. When this bit is “0”, there is no data to be read.

In transmit mode endpoint, if the corresponding endpoint bit is “0”, the CPU can transfer data under the FIFO payload. If this bit is “1”, because FIFO has transfer data waiting, transfer data to FIFO from UDC after the corresponding bit has been cleared to “0”. When a short-packet is transferred, access EOP register after writing transmission data to the corresponding endpoint.

- Dual packet mode  
(DATASET1: Bit3, bit5 and bit7     DATASET2: Bit1, bit3 bit5 and bit7)

These bits become effective in the dual packet mode. FIFO has 2-packets in this mode.

Each packet (packet-A and packet-B) has its own DATASET-bit.

Unlike as in the case above, in isochronous transfer, this shows the packet that can access the current frame. In this case, whether bit A or B is set to “1”, it is renewed according to the shifting frame.

Note1: In receive mode, if the endpoint bits corresponding to packet-A or packet-B are "1", read the required packet-number data after checking EPx\_SIZE<PKT\_ACTIVE>.

Note2: In transmit mode, if both A and B bits are not "1", this means there is space in FIFO. So, write data of payload or less to FIFO. If the transmission is short-packet, write "0" to EOP<EPn\_EOPB> after writing data to the FIFO. The maximum size that can be written to A or B packet is the same as the maximum payload size. If both A and B bits are "0", continuous writing of double maximum payload size is available.

Note3: In dual packet transmit mode, if both A and B packet are empty and EOP<EPn\_EOPB> is written "0", the NULL-data is set to FIFO. In single mode, the NULL-data is also set to FIFO if the above operation is executed when packet-A contains no data.

Note4: No data is set in this register when NULL-packet (0Length-packet) is received.

## 3.16.3.13 EPx\_STATUS Register (x: 0 to 7)

These registers are status registers for each endpoint. The <SUSPEND> is common to all endpoints.

|                       |             | 7 | 6      | 5       | 4         | 3         | 2         | 1            | 0         |
|-----------------------|-------------|---|--------|---------|-----------|-----------|-----------|--------------|-----------|
| EP0_STATUS<br>(0790H) | bit Symbol  |   | TOGGLE | SUSPEND | STATUS[2] | STATUS[1] | STATUS[0] | FIFO_DISABLE | STAGE_ERR |
|                       | Read/Write  |   | R      | R       | R         | R         | R         | R            | R         |
|                       | Reset State |   | 0      | 0       | 1         | 1         | 1         | 0            | 0         |
|                       |             | 7 | 6      | 5       | 4         | 3         | 2         | 1            | 0         |
| EP1_STATUS<br>(0791H) | bit Symbol  |   | TOGGLE | SUSPEND | STATUS[2] | STATUS[1] | STATUS[0] | FIFO_DISABLE | STAGE_ERR |
|                       | Read/Write  |   | R      | R       | R         | R         | R         | R            | R         |
|                       | Reset State |   | 0      | 0       | 1         | 1         | 1         | 0            | 0         |
|                       |             | 7 | 6      | 5       | 4         | 3         | 2         | 1            | 0         |
| EP2_STATUS<br>(0792H) | bit Symbol  |   | TOGGLE | SUSPEND | STATUS[2] | STATUS[1] | STATUS[0] | FIFO_DISABLE | STAGE_ERR |
|                       | Read/Write  |   | R      | R       | R         | R         | R         | R            | R         |
|                       | Reset State |   | 0      | 0       | 1         | 1         | 1         | 0            | 0         |
|                       |             | 7 | 6      | 5       | 4         | 3         | 2         | 1            | 0         |
| EP3_STATUS<br>(0793H) | bit Symbol  |   | TOGGLE | SUSPEND | STATUS[2] | STATUS[1] | STATUS[0] | FIFO_DISABLE | STAGE_ERR |
|                       | Read/Write  |   | R      | R       | R         | R         | R         | R            | R         |
|                       | Reset State |   | 0      | 0       | 1         | 1         | 1         | 0            | 0         |
|                       |             | 7 | 6      | 5       | 4         | 3         | 2         | 1            | 0         |
| EP4_STATUS<br>(0794H) | bit Symbol  |   | TOGGLE | SUSPEND | STATUS[2] | STATUS[1] | STATUS[0] | FIFO_DISABLE | STAGE_ERR |
|                       | Read/Write  |   | R      | R       | R         | R         | R         | R            | R         |
|                       | Reset State |   | 0      | 0       | 1         | 1         | 1         | 0            | 0         |
|                       |             | 7 | 6      | 5       | 4         | 3         | 2         | 1            | 0         |
| EP5_STATUS<br>(0795H) | bit Symbol  |   | TOGGLE | SUSPEND | STATUS[2] | STATUS[1] | STATUS[0] | FIFO_DISABLE | STAGE_ERR |
|                       | Read/Write  |   | R      | R       | R         | R         | R         | R            | R         |
|                       | Reset State |   | 0      | 0       | 1         | 1         | 1         | 0            | 0         |
|                       |             | 7 | 6      | 5       | 4         | 3         | 2         | 1            | 0         |
| EP6_STATUS<br>(0796H) | bit Symbol  |   | TOGGLE | SUSPEND | STATUS[2] | STATUS[1] | STATUS[0] | FIFO_DISABLE | STAGE_ERR |
|                       | Read/Write  |   | R      | R       | R         | R         | R         | R            | R         |
|                       | Reset State |   | 0      | 0       | 1         | 1         | 1         | 0            | 0         |
|                       |             | 7 | 6      | 5       | 4         | 3         | 2         | 1            | 0         |
| EP7_STATUS<br>(0797H) | bit Symbol  |   | TOGGLE | SUSPEND | STATUS[2] | STATUS[1] | STATUS[0] | FIFO_DISABLE | STAGE_ERR |
|                       | Read/Write  |   | R      | R       | R         | R         | R         | R            | R         |
|                       | Reset State |   | 0      | 0       | 1         | 1         | 1         | 0            | 0         |
|                       |             | 7 | 6      | 5       | 4         | 3         | 2         | 1            | 0         |

Note: EP4, 5, 6 and 7\_STATUS registers are not used in the TMP92CF30.

## TOGGLE Bit (Bit6)

0: TOGGLE      Bit0  
1: TOGGLE      Bit1

This bit shows status of toggle sequence bit.

## SUSPEND (Bit5)

0: RESUME  
1: SUSPEND

This bit shows status of UDC power management.

In the SUSPEND status, access to UDC is limited.

For details, refer to 3.16.9.

STATUS [2:0]  
(Bit4 to bit2)

These bits show status of UDC endpoint.

The status shows whether transfer is possible or not, and the result of the transfer. These depend on transfer type.

(For the Isochronous transfer type, refer to 3.16.9.)

|              |               |                                                                                                                                                                                                                                                                                                                                                                    |
|--------------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 000: READY   | Receiving:    | <p>Device can be received.</p> <p>In endpoints 1 to 7, this register is initialized to "READY" by setting transfer type at SET_CONFIGURATION.</p> <p>In endpoint 0, this register is initialized to "READY" by detecting USB reset from the host.</p> <p>This is initialized to "READY" by terminating the status stage without error.</p>                         |
|              | Transmitting: | <p>Basically, the same as with "Receiving".</p> <p>But in transmitting, when data for transmission is set to FIFO and answer to token from host and transfer data to host collect and received ACK, status register does not change, and it remains "READY". In this case, EPx_Empty_A or EPx_Empty_B interrupt terminates the transfer correctly.</p>             |
| 001: DATAIN  |               | UDC set to DATAIN and generates EPx_FULL_A or EPx_FULL_B interrupt when data is received from the host without error.                                                                                                                                                                                                                                              |
| 010: FULL    |               | Refer to 3.16.8 (2) Details for the STATUS register.                                                                                                                                                                                                                                                                                                               |
| 011: TX_ERR  |               | After transfer of data to IN token from host, UDC sets TX-ER to status register when "ACK" is not received from host. In this case, an interrupt is not generated. The hosts re-try IN token transfer.                                                                                                                                                             |
| 100: RX_ERR  |               | UDC sets RX_ERR to status register without transmitting "ACK" to host when an error (such as a CRC-error) is detected in data of received token. In this case, an interrupt is not generated. The hosts re-try and IN token transfer. In case of toggle error with normal data, UDC returns ACK and set RX_ERR of STATUS register.                                 |
| 101: BUSY    |               | <p>This status is used only for the control transfer type and it is set when a status-stage token is received from the host after a terminated data-stage.</p> <p>When status-stage can be finished, terminates correctly and returns to READY. This is not used in the Bulk and interrupts transfer type.</p>                                                     |
| 110: STALL   |               | <p>This status shows that the corresponding endpoint is in STALL status.</p> <p>In this status, STALL-handshake returns, except for SETUP-token. The control endpoint returns to READY from stall condition when SETUP-token is received.</p> <p>Other endpoints return to READY when initialization command of FIFO is received.</p>                              |
| 111: INVALID |               | <p>This status shows that the corresponding endpoint is in UNCONFIGURED status.</p> <p>In this status, the UDC has no effect when a token is received from the host.</p> <p>On reset, all endpoints are set to INVALID status. Only endpoint 0 returns to READY on receiving USB-reset. Corresponding endpoints return to READY by according to configuration.</p> |

**FIFO\_DISABLE (Bit1)**

0: FIFO enabled  
1: FIFO disabled

This bit symbol shows FIFO status except for EP0.

If the FIFO is set to disabled, the UDC transmits NAK handshake for all transfers. Disabled or enabled status is set the COMMAND register. This bit is cleared to “0” when transfer type is changed.

**STAGE\_ERROR (Bit0)**

0: SUCCESS  
1: ERROR

This bit symbol shows that the status stage has not been terminated correctly. ERROR is set when a status stage is not terminated correctly and a new SETUP token is received.

When this bit is “1”, this bit is cleared to “0” by read EP0\_STATUS register. This bit is not cleared even if normal control transfer or other transfer is executed after. To clear, read this bit. When software transaction is finished and UDC writes EOP register, UDC shifts to status register and waits termination of status stage. In this case, if software is needed to confirm that the status stage has been terminated correctly, when a new request flag is received, it is possible to confirm whether or not the last request has been terminated correctly. It can also be confirmed, when a new request flag is asserted, whether or not the last request has been cancelled before completion.



## 3.16.3.14 EPx\_SIZE Register (x: 0 to 7)

These registers have the following functions.

- In receive mode, showing the 1-packet data number which has been received correctly.
- In the transmit mode, showing payload size. Showing length value when short packet is transferred.

It is not necessary to read this register when it is transmitting.

- Showing dual packet mode and currently effective packet.

Each endpoint has an H (High)-register that shows upper bit 9 to bit7 of data size and an L (Low) register which shows lower bit 6 to bit0 and control bit of FIFO.

Each H/L register also has 2-set for dual-packet mode.

|                         |             | 7          | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|-------------------------|-------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| EP0_SIZE_L_A<br>(0798H) | bit Symbol  | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1 | DATASIZE0 |
|                         | Read/Write  | R          | R         | R         | R         | R         | R         | R         | R         |
|                         | Reset State | 1          | 0         | 0         | 0         | 1         | 0         | 0         | 0         |
|                         |             | 7          | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
| EP1_SIZE_L_A<br>(0799H) | bit Symbol  | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1 | DATASIZE0 |
|                         | Read/Write  | R          | R         | R         | R         | R         | R         | R         | R         |
|                         | Reset State | 1          | 0         | 0         | 0         | 1         | 0         | 0         | 0         |
|                         |             | 7          | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
| EP2_SIZE_L_A<br>(079AH) | bit Symbol  | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1 | DATASIZE0 |
|                         | Read/Write  | R          | R         | R         | R         | R         | R         | R         | R         |
|                         | Reset State | 1          | 0         | 0         | 0         | 1         | 0         | 0         | 0         |
|                         |             | 7          | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
| EP3_SIZE_L_A<br>(079BH) | bit Symbol  | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1 | DATASIZE0 |
|                         | Read/Write  | R          | R         | R         | R         | R         | R         | R         | R         |
|                         | Reset State | 1          | 0         | 0         | 0         | 1         | 0         | 0         | 0         |
|                         |             | 7          | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
| EP4_SIZE_L_A<br>(079CH) | bit Symbol  | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1 | DATASIZE0 |
|                         | Read/Write  | R          | R         | R         | R         | R         | R         | R         | R         |
|                         | Reset State | 1          | 0         | 0         | 0         | 1         | 0         | 0         | 0         |
|                         |             | 7          | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
| EP5_SIZE_L_A<br>(079DH) | bit Symbol  | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1 | DATASIZE0 |
|                         | Read/Write  | R          | R         | R         | R         | R         | R         | R         | R         |
|                         | Reset State | 1          | 0         | 0         | 0         | 1         | 0         | 0         | 0         |
|                         |             | 7          | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
| EP6_SIZE_L_A<br>(079EH) | bit Symbol  | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1 | DATASIZE0 |
|                         | Read/Write  | R          | R         | R         | R         | R         | R         | R         | R         |
|                         | Reset State | 1          | 0         | 0         | 0         | 1         | 0         | 0         | 0         |
|                         |             | 7          | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
| EP7_SIZE_L_A<br>(079FH) | bit Symbol  | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1 | DATASIZE0 |
|                         | Read/Write  | R          | R         | R         | R         | R         | R         | R         | R         |
|                         | Reset State | 1          | 0         | 0         | 0         | 1         | 0         | 0         | 0         |
|                         |             | 7          | 6         | 5         | 4         | 3         | 2         | 1         | 0         |

Note: EP4,5,6,7\_SIZE\_L\_A registers are not used in the TMP92CF30.

|                         |             | 7          | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|-------------------------|-------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| EP1_SIZE_L_B<br>(07A1H) | bit Symbol  | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1 | DATASIZE0 |
|                         | Read/Write  | R          | R         | R         | R         | R         | R         | R         | R         |
|                         | Reset State | 0          | 0         | 0         | 0         | 1         | 0         | 0         | 0         |
|                         |             | 7          | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
| EP2_SIZE_L_B<br>(07A2H) | bit Symbol  | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1 | DATASIZE0 |
|                         | Read/Write  | R          | R         | R         | R         | R         | R         | R         | R         |
|                         | Reset State | 0          | 0         | 0         | 0         | 1         | 0         | 0         | 0         |
|                         |             | 7          | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
| EP3_SIZE_L_B<br>(07A3H) | bit Symbol  | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1 | DATASIZE0 |
|                         | Read/Write  | R          | R         | R         | R         | R         | R         | R         | R         |
|                         | Reset State | 0          | 0         | 0         | 0         | 1         | 0         | 0         | 0         |
|                         |             | 7          | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
| EP4_SIZE_L_B<br>(07A4H) | bit Symbol  | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1 | DATASIZE0 |
|                         | Read/Write  | R          | R         | R         | R         | R         | R         | R         | R         |
|                         | Reset State | 0          | 0         | 0         | 0         | 1         | 0         | 0         | 0         |
|                         |             | 7          | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
| EP5_SIZE_L_B<br>(07A5H) | bit Symbol  | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1 | DATASIZE0 |
|                         | Read/Write  | R          | R         | R         | R         | R         | R         | R         | R         |
|                         | Reset State | 0          | 0         | 0         | 0         | 1         | 0         | 0         | 0         |
|                         |             | 7          | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
| EP6_SIZE_L_B<br>(07A6H) | bit Symbol  | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1 | DATASIZE0 |
|                         | Read/Write  | R          | R         | R         | R         | R         | R         | R         | R         |
|                         | Reset State | 0          | 0         | 0         | 0         | 1         | 0         | 0         | 0         |
|                         |             | 7          | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
| EP7_SIZE_L_B<br>(07A7H) | bit Symbol  | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1 | DATASIZE0 |
|                         | Read/Write  | R          | R         | R         | R         | R         | R         | R         | R         |
|                         | Reset State | 0          | 0         | 0         | 0         | 1         | 0         | 0         | 0         |

Note EP3,4,5,6,7\_SIZE\_L\_B registers are not used in the TMP92CF30.

|                         |             | 7 | 6 | 5 | 4 | 3 | 2         | 1         | 0         |
|-------------------------|-------------|---|---|---|---|---|-----------|-----------|-----------|
| EP1_SIZE_H_A<br>(07A9H) | bit Symbol  |   |   |   |   |   | DATASIZE9 | DATASIZE8 | DATASIZE7 |
|                         | Read/Write  |   |   |   |   |   | R         | R         | R         |
|                         | Reset State |   |   |   |   |   | 0         | 0         | 0         |
| EP2_SIZE_H_A<br>(07AAH) | bit Symbol  |   |   |   |   |   | DATASIZE9 | DATASIZE8 | DATASIZE7 |
|                         | Read/Write  |   |   |   |   |   | R         | R         | R         |
|                         | Reset State |   |   |   |   |   | 0         | 0         | 0         |
| EP3_SIZE_H_A<br>(07ABH) | bit Symbol  |   |   |   |   |   | DATASIZE9 | DATASIZE8 | DATASIZE7 |
|                         | Read/Write  |   |   |   |   |   | R         | R         | R         |
|                         | Reset State |   |   |   |   |   | 0         | 0         | 0         |
| EP4_SIZE_H_A<br>(07ACH) | bit Symbol  |   |   |   |   |   | DATASIZE9 | DATASIZE8 | DATASIZE7 |
|                         | Read/Write  |   |   |   |   |   | R         | R         | R         |
|                         | Reset State |   |   |   |   |   | 0         | 0         | 0         |
| EP5_SIZE_H_A<br>(07ADH) | bit Symbol  |   |   |   |   |   | DATASIZE9 | DATASIZE8 | DATASIZE7 |
|                         | Read/Write  |   |   |   |   |   | R         | R         | R         |
|                         | Reset State |   |   |   |   |   | 0         | 0         | 0         |
| EP6_SIZE_H_A<br>(07AEH) | bit Symbol  |   |   |   |   |   | DATASIZE9 | DATASIZE8 | DATASIZE7 |
|                         | Read/Write  |   |   |   |   |   | R         | R         | R         |
|                         | Reset State |   |   |   |   |   | 0         | 0         | 0         |
| EP7_SIZE_H_A<br>(07AFH) | bit Symbol  |   |   |   |   |   | DATASIZE9 | DATASIZE8 | DATASIZE7 |
|                         | Read/Write  |   |   |   |   |   | R         | R         | R         |
|                         | Reset State |   |   |   |   |   | 0         | 0         | 0         |

Note EP4,5,6,7\_SIZE\_H\_A registers are not used in the TMP92CF30.

|                         |             | 7 | 6 | 5 | 4 | 3 | 2         | 1         | 0         |
|-------------------------|-------------|---|---|---|---|---|-----------|-----------|-----------|
| EP1_SIZE_H_B<br>(07B1H) | bit Symbol  |   |   |   |   |   | DATASIZE9 | DATASIZE8 | DATASIZE7 |
|                         | Read/Write  |   |   |   |   |   | R         | R         | R         |
|                         | Reset State |   |   |   |   |   | 0         | 0         | 0         |
| EP2_SIZE_H_B<br>(07B2H) | bit Symbol  |   |   |   |   |   | DATASIZE9 | DATASIZE8 | DATASIZE7 |
|                         | Read/Write  |   |   |   |   |   | R         | R         | R         |
|                         | Reset State |   |   |   |   |   | 0         | 0         | 0         |
| EP3_SIZE_H_B<br>(07B3H) | bit Symbol  |   |   |   |   |   | DATASIZE9 | DATASIZE8 | DATASIZE7 |
|                         | Read/Write  |   |   |   |   |   | R         | R         | R         |
|                         | Reset State |   |   |   |   |   | 0         | 0         | 0         |
| EP4_SIZE_H_B<br>(07B4H) | bit Symbol  |   |   |   |   |   | DATASIZE9 | DATASIZE8 | DATASIZE7 |
|                         | Read/Write  |   |   |   |   |   | R         | R         | R         |
|                         | Reset State |   |   |   |   |   | 0         | 0         | 0         |
| EP5_SIZE_H_B<br>(07B4H) | bit Symbol  |   |   |   |   |   | DATASIZE9 | DATASIZE8 | DATASIZE7 |
|                         | Read/Write  |   |   |   |   |   | R         | R         | R         |
|                         | Reset State |   |   |   |   |   | 0         | 0         | 0         |
| EP6_SIZE_H_B<br>(07B6H) | bit Symbol  |   |   |   |   |   | DATASIZE9 | DATASIZE8 | DATASIZE7 |
|                         | Read/Write  |   |   |   |   |   | R         | R         | R         |
|                         | Reset State |   |   |   |   |   | 0         | 0         | 0         |
| EP7_SIZE_H_B<br>(07B7H) | bit Symbol  |   |   |   |   |   | DATASIZE9 | DATASIZE8 | DATASIZE7 |
|                         | Read/Write  |   |   |   |   |   | R         | R         | R         |
|                         | Reset State |   |   |   |   |   | 0         | 0         | 0         |

Note EP3,4,5,6,7\_SIZE\_H\_B registers are not used in the TMP92CF30.

DATASIZE[9:7] (H register: Bit2 to bit0)

DATASIZE[6:0] (L register: Bit6 to bit0)

In receiving, the data number of the 1 packet received from the host is shown. This is renewed when data from the host is received with no error.

By setting EPx\_MODE register, these bits are initialized to MAX pay load size in bulk/interrupt transfer, and “0” in isochronous transfer.

PKT\_ACTIVE (L register: Bit7)

- 1: OUT\_ENABLE
- 0: OUT\_DISABLE

When dual-packet mode is selected, this bit show the packet that can be accessed. In this case, the UDC accesses packets that divide FIFO (Packet A and Packet B) mutually. When FIFO in UDC is accessed by CPU, refer to this bit. If receiving endpoint, start reading from that packet that this bit is “1”. In single-packet mode, this bit has no effect because packet-A is always used.

## 3.16.3.15 FRAME Register

This register shows the frame number which is issued with SOF token from the host and is used for Isochronous transfer type.

Each HIGH and LOW register shows upper and lower bits.

| FRAME_L<br>(07E1H) |             | 7 | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|--------------------|-------------|---|------|------|------|------|------|------|------|
|                    | bit Symbol  | – | T[6] | T[5] | T[4] | T[3] | T[2] | T[1] | T[0] |
|                    | Read/Write  | R | R    | R    | R    | R    | R    | R    | R    |
|                    | Reset State | 0 | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

| FRAME_H<br>(07E2H) |             | 7     | 6    | 5    | 4    | 3 | 2      | 1          | 0          |
|--------------------|-------------|-------|------|------|------|---|--------|------------|------------|
|                    | bit Symbol  | T[10] | T[9] | T[8] | T[7] |   | CREATE | FRAME_STS1 | FRAME_STS0 |
|                    | Read/Write  | R     | R    | R    | R    |   | R      | R          | R          |
|                    | Reset State | 0     | 0    | 0    | 0    |   | 0      | 1          | 0          |

T[10:7] (H register: Bit7 to bit4)

T[6:0] (L register: Bit6 to bit0)

These bits are renewed when SOF-token is received. They also shows the frame-number.

CREATE (H register: Bit2)

0: DISABLE

1: ENABLE

These bits show whether the function that generates SOF automatically from the UDC is enabled or not. This is used in case of error in receiving SOF token.

This function is set by accessing COMMAND register.

On reset, this bit is initialized to “0”.

FRAME\_STS[1:0]

(H register: Bit1 and bit0)

0: BEFORE

1: VALID

2: LOST

These bits show the status whether a frame number that is shown in the FRAME register is correct or not. At the LOST status, a correct frame number is undefined.

If this register is “VALID”, the number that is shown to the FRAME register is correct.

If this register is “BEFORE”, during SOF auto generation, BEFORE condition shows it from USB host controller inside that from SOF generation time to reception of SOF token. Correct frame-number value is the value that is selected from FRAME register value.

## 3.16.3.16 ADDRESS Register

This register shows the device address which is specified by the host in bus enumeration.

By reading this register, the present address can be confirmed.

| ADDRESS<br>(07E3H) |             | 7 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|--------------------|-------------|---|----|----|----|----|----|----|----|
|                    | bit Symbol  |   | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|                    | Read/Write  |   | R  | R  | R  | R  | R  | R  | R  |
|                    | Reset State |   | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

ADDRESS [6:0] (Bit6 to bit0)

The UDC compares this registers and address in all packet ID, and UDC judges whether it is an effective transaction or not.

This is initialized to “00H” by USB reset.

## 3.16.3.17 EOP Register

This register is used when a control transfer type dataphase terminates or when a short packet is transmitting bulk-IN or interrupt-IN.

| EOP<br>(07CFH) |             | 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|----------------|-------------|----------|----------|----------|----------|----------|----------|----------|----------|
|                | bit Symbol  | EP7_EOPB | EP6_EOPB | EP5_EOPB | EP4_EOPB | EP3_EOPB | EP2_EOPB | EP1_EOPB | EP0_EOPB |
|                | Read/Write  | W        | W        | W        | W        | W        | W        | W        | W        |
|                | Reset State | 1        | 1        | 1        | 1        | 1        | 1        | 1        | 1        |

Note1: EOP<EP7\_EOPB, EP6\_EOPB, EP5\_EOPB, EP4\_EOPB> registers are not used in the TMP92CF30.

Note2: When writing to this register, a recovery time of 5clocks at 12MHz is needed. After writing this register, insert dummy instruction of 420 ns or longer.

In a control transfer type dataphase, write “0” to <EP0\_EOPB> when all transmission data is written to the FIFO, or read all receiving data from the FIFO. The UDC terminates its status stage on this signal.

When a short packet is transmitted by using bulk-IN or interrupt-IN endpoint, use this to terminate writing of transmission data. In this case, write “0” to <EP0\_EOPB> of writing endpoint. Write “1” to other bits.

## 3.16.3.18 Port Status Register

This register is used when a request of printer class request is received.

In the case of a GET\_PORT\_STATUS request, the UDC operates automatically using this data.

|                        |             | 7         | 6         | 5          | 4      | 3        | 2         | 1         | 0         |
|------------------------|-------------|-----------|-----------|------------|--------|----------|-----------|-----------|-----------|
| Port Status<br>(07E0H) | bit Symbol  | Reserved7 | Reserved6 | PaperError | Select | NotError | Reserved2 | Reserved1 | Reserved0 |
|                        | Read/Write  | W         | W         | W          | W      | W        | W         | W         | W         |
|                        | Reset State | 0         | 0         | 0          | 1      | 1        | 0         | 0         | 0         |

Note: The TMP92CF30 does not use this register since not support printer-class.

The data should be written before receiving request.

Write “0” to the <Reserved> bit of this register. This register is initialized to “18H” on reset.

## 3.16.3.19 Standard Request Mode Register

This register sets the answer for Standard Request either answering automatically in hardware, or by control through software. Each bit represents a kind of request.

When the relevant bit in this register is set to “0”, the answer is executed automatically by hardware. When the relevant bit in this register is set to “1”, the answer is controlled by software. If a request is received during hardware control, the interrupt signal (INT\_SETUP, INT\_EP0, INT\_STAS, INT\_STAN) is set to disable. If a request is received during software control, the interrupt signal is asserted, and it is controlled by software.

|                                  |             | 7           | 6           | 5        | 4        | 3          | 2         | 1         | 0        |
|----------------------------------|-------------|-------------|-------------|----------|----------|------------|-----------|-----------|----------|
| Standard Request Mode<br>(07D8H) | bit Symbol  | S_Interface | G_Interface | S_Config | G_Config | G_Descript | S_Feature | C_Feature | G_Status |
|                                  | Read/Write  | R/W         | R/W         | R/W      | R/W      | R/W        | R/W       | R/W       | R/W      |
|                                  | Reset State | 0           | 0           | 0        | 0        | 0          | 0         | 0         | 0        |

|             |                             |
|-------------|-----------------------------|
| S_Inteface  | (Bit 7) : SET_INTERFACE     |
| G_Interface | (Bit 6) : GET_INTERFACE     |
| S_Config    | (Bit 5) : SET_CONFIGURATION |
| G_Config    | (Bit 4) : GET_CONFIGURATION |
| G_Descript  | (Bit 3) : GET_DESCRIPTOR    |
| S_Feature   | (Bit 2) : SET_FEATURE       |
| C_Feature   | (Bit 1) : CLEAR_FEATURE     |
| G_Status    | (Bit 0) : GET_STATUS        |

3.16.3.20 Request Mode Register

This register sets the answer for Class Request either automatically in hardware or by control through software. Each bit represents a kind of request.

When relevant bit in this register is set to “0”, the answer is executed automatically by hardware. When relevant bit in this register is set to “1”, the answer is controlled by software. If request is received during hardware control, interrupt signal (INT\_SETUP, INT\_EP0, INT\_STAS, INT\_STATUSN) is set to disable. If a request is received during software control, the interrupt signal is asserted, and it is controlled by software.

|                         |             |   |            |            |            |   |   |   |   |
|-------------------------|-------------|---|------------|------------|------------|---|---|---|---|
| Request Mode<br>(07D9H) |             | 7 | 6          | 5          | 4          | 3 | 2 | 1 | 0 |
|                         | bit Symbol  |   | Soft_Reset | G_Port_Sts | G_DeviceId |   |   |   |   |
|                         | Read/Write  |   | R/W        | R/W        | R/W        |   |   |   |   |
|                         | Reset State |   | 0          | 0          | 0          |   |   |   |   |

Note: the TMP92CF30 does not use this register since it does not support printer-class.

- 
- (Bit 7) : Reserved
- Soft\_Reset (Bit 6) : SOFT\_RESET
- G\_Port\_Sts (Bit 5) : GET\_PORT\_STATUS
- G\_Config (Bit 4) : GET\_DEVICE\_ID
- (Bit 3 to 0) : Reserved

- Note1: SET\_ADDRESS request is supported only by auto-answer .
- Note2: SET\_DESCRIPTOR and SYNCH\_FRAME are controlled only by software .
- Note3: Vendor Request and Class Request (Printer Class and so on) are controlled only by software.
- Note4: INT\_SETUP, EP0, STAS and STASN interrupts assert only when it is software-control.



## 3.16.3.21 COMMAND Register

This register sets COMMAND at each endpoint. This register can be set to select of endpoint in bit6 to bit4 and kind of COMMAND in bit3 to bit0.

COMMAND for endpoint that is supported is ignored.

|                 | 7 | 6     | 5     | 4     | 3          | 2          | 1          | 0          |
|-----------------|---|-------|-------|-------|------------|------------|------------|------------|
| COMMAND (07D0H) |   | EP[2] | EP[1] | EP[0] | Command[3] | Command[2] | Command[1] | Command[0] |
| Read/Write      |   | W     | W     | W     | W          | W          | W          | W          |
| Reset State     |   | 0     | 0     | 0     | 0          | 0          | 0          | 0          |

Note: When writing to this register, a recovery time of 5clocks at 12MHz is needed. After writing this register, insert dummy instruction of 420 ns or longer.

## EP [2:0] (Bit6 to bit4)

- 000: Select endpoint 0
- 001: Select endpoint 1
- 010: Select endpoint 2
- 011: Select endpoint 3

## COMMAND [3:0] (Bit3 to bit0)

- 0000: Reserved
- 0001: Reserved
- 0010: SET\_DATA0

This COMMAND clear toggle sequence bit of corresponding endpoint (EP0 to EP3). If this COMMAND is input, it sets toggle sequence bit of the corresponding endpoint to "0". Data toggle for transfer is renewed automatically by UDC. However, this COMMAND execution is required if setting toggle sequence bit of endpoint to "0". If control transfer type and Isochronous transfer type, execution of this COMMAND is not required because of hardware control.

## 0011: RESET

This COMMAND resets the corresponding endpoint (EP0 to EP3). If this COMMAND is input, the corresponding endpoint is initialized. CLEAR\_FEATURE request stalls endpoint. When this stall is cleared, execute this COMMAND. (This command does not affect transfer mode.) This command initializes the following.

- Clear toggle sequence bit of corresponding endpoint.
- Clear STALL of corresponding endpoint.
- Set to FIFO\_ENABLE condition.
- Clear the data in FIFO

## 0100: STALL

This COMMAND sets corresponding endpoint to STALL (EP0 to EP3). If STALL handshake must be return as answer for device request, execute this command.

## 0101: INVALID

This COMMAND sets condition to prohibition of use corresponding endpoint (EP1 to EP3). If UDC detects USB\_RESET signal from USB host, it sets all endpoints (except endpoint 0) to prohibition using it automatically. If Config and Interface are changed by device request, set endpoint that is not used to prohibit use.

## 0110: CREATE\_SOF

This COMMAND sets quasi-SOF generation function to enable (EP0). Default is set to disable, it must be used for Isochronous transfer.

## 0111: FIFO\_DISABLE

This COMMAND sets FIFO of corresponding endpoint to disable (EP1 to EP3). If this command is set from external, all of transfers except for toggle error for corresponding endpoint return NAK. When it is set externally while receiving packet, this becomes valid from next token. This command does not affect the packet that is transferring.

|                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1000: FIFO_ENABLE     | <p>This COMMAND sets FIFO of corresponding endpoint to enable (EP1 to EP3).<br/>If FIFO is set to disable by FIFO_DISABLE COMMAND, this command is used for release of disable condition. If set while receiving packet, this becomes valid from next token. If USB_RESET is detected from host and RESET COMMAND execute and transfer mode is set by using SET_CONFIG and SET_INTERFACE request, the corresponding endpoint enters FIFO_ENABLE condition.</p>                                         |
| 1001: INIT_DESCRIPTOR | <p>This COMMAND is used if descriptor RAM is rewritten during system operation (EP0).<br/>If UDC detects USB_RESET from host controller, it reads content of descriptor RAM automatically, and it performs relevant settings.<br/>If descriptor RAM is changed during system operation, it must read setting again. Therefore, execute this command. When connected to USB host, this function starts reading automatically. Therefore, in this case, it is not necessary to execute this command.</p> |
| 1010: FIFO_CLEAR      | <p>This COMMAND initializes FIFO of corresponding endpoint (EP1 to EP3).<br/>However, EPx_STATUS&lt;TOGGLE&gt; is not initialized.<br/>If resetting by software, execute this COMMAND.<br/>This command initializes the following item.</p> <ul style="list-style-type: none"><li>• Clear STALL of relevant endpoint.</li><li>• Set to FIFO_ENABLE condition.</li><li>• Clear the data in FIFO</li></ul>                                                                                               |
| 1011: STAL_CLEAR      | <p>This COMMAND clear STALL of corresponding endpoint (EP1 to EP3).<br/>If clearing only STALL of endpoint, execute this COMMAND.</p>                                                                                                                                                                                                                                                                                                                                                                  |

## 3.16.3.22 INT\_Control Register

INT\_STASN interrupt is disabled and enabled by the value that is written to this register.

This is initialized to disable by external reset. When setup packet is received, it becomes disabled.

|                        |             | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0          |
|------------------------|-------------|---|---|---|---|---|---|---|------------|
| INT_Control<br>(07D6H) | bit Symbol  |   |   |   |   |   |   |   | Status_nak |
|                        | Read/Write  |   |   |   |   |   |   |   | R/W        |
|                        | Reset State |   |   |   |   |   |   |   | 0          |

In control read transfer, if the host terminates a dataphase with small data length (smaller than the data length that is specified by the host as wLength), the device side and stage management cannot be synchronized. Therefore, INT\_STASN interrupt signals this shift to status stage. If needed, set to “1” after receiving setup packet.

## STATUS\_NAK (Bit0)

0: INT\_STATSN interrupt disable

1: INT\_STATSN interrupt enable

## 3.16.3.23 USB STATE Register

This register shows the current device state for connection with USB host.

|                      |             | 7 | 6 | 5 | 4 | 3 | 2          | 1         | 0       |
|----------------------|-------------|---|---|---|---|---|------------|-----------|---------|
| USB STATE<br>(07CEH) | bit Symbol  |   |   |   |   |   | Configured | Addressed | Default |
|                      | Read/Write  |   |   |   |   |   | R/W        | R         | R       |
|                      | Reset State |   |   |   |   |   | 0          | 0         | 1       |

Note: When writing to this register, a recovery time of 5clocks at 12MHz is needed. After writing this register, insert dummy instruction of 420 ns or longer.

Inside the UDC, the answer for each Device Request is managed by referring to these bits (Configured, Addressed and Default). If transaction for SET\_CONFIG request is executed by using software, write the present state to this register. If host appointconfig is 0, this becomes Unconfigured, and it is necessary to return to Addressed state. Therefore, if host appoint config is 0, write “0” to bit2.

When Configured bit (Bit2) is written “0”, Addressed bit (bit 1) is set automatically by hardware. When host appoint config value that supported by device, device must execute mode setting for each endpoint by using the value that is appointed by endpoint-descriptor in the config-descriptor. After finish mode setting, set Configured bit (Bit2) to “1” before accessing EOP register. When this bit is set to “1”, Addressed bit (Bit1) is set to “0” automatically.

## Bit2 to bit0

000: Default

010: Addressed

100: Configured

## 3.16.3.24 EPx\_MODE Register (x: 1 to 3)

This register sets transfer mode of endpoint (EP1 to EP3).

If SET\_CONFIG and SET\_INTERFACE processing is set to software control, this control must use appointed config or interface. Access this register to set mode.

|                     | 7           | 6 | 5          | 4          | 3          | 2       | 1       | 0         |
|---------------------|-------------|---|------------|------------|------------|---------|---------|-----------|
| EP1_MODE<br>(0789H) | bit Symbol  |   | Payload[2] | Payload[1] | Payload[0] | Mode[1] | Mode[0] | Direction |
|                     | Read/Write  |   | R/W        | R/W        | R/W        | R/W     | R/W     | R/W       |
|                     | Reset State |   | 0          | 0          | 0          | 0       | 0       | 0         |
| EP2_MODE<br>(078AH) | bit Symbol  |   | Payload[2] | Payload[1] | Payload[0] | Mode[1] | Mode[0] | Direction |
|                     | Read/Write  |   | R/W        | R/W        | R/W        | R/W     | R/W     | R/W       |
|                     | Reset State |   | 0          | 0          | 0          | 0       | 0       | 0         |
| EP3_MODE<br>(078BH) | bit Symbol  |   | Payload[2] | Payload[1] | Payload[0] | Mode[1] | Mode[0] | Direction |
|                     | Read/Write  |   | R/W        | R/W        | R/W        | R/W     | R/W     | R/W       |
|                     | Reset State |   | 0          | 0          | 0          | 0       | 0       | 0         |

There is a limitation to the timing that can be written.

If transaction for SET\_CONFIG and SET\_INTERFACE processing is set to software control, after INT\_SETUP interrupt is received, finish writing before accessing EOP register. This register prohibits writing when it is other timing, and it is ignored.

Note1: When writing to this register, a recovery time of 5clocks at 12MHz is needed. After writing this register, insert dummy instruction of 420 ns or longer.

Note2: When writing to this register, endpoint is initialized same as RESET of COMMAND register.

## DIRECTION (Bit0)

- 0: OUT      Direction from host to device
- 1: IN      Direction from device to host

## MODE [1:0] (Bit2 and bit1)

- 00: Control transfer type
- 01: Isochronous transfer type
- 10: Bulk transfer type or interrupt transfer type
- 11: Interrupt (No toggle)

## PAYLOAD [2:0] (Bit3, bit4 and bit5)

- 000: 8 bytes
- 001: 16 bytes
- 010: 32 bytes
- 011: 64 bytes
- 0100:128 bytes
- 0101:256 bytes
- 0110:512 bytes
- 0111:1023 bytes (Note1, 2)

Note1:Max packet size of Isochronous transfer type is 1023 bytes.

Note2:If wMaxPacketSize of descriptor has been set to other than 8, 16, ..., 1023, Payload more than descriptor value is set by auto-answer of Set\_Configuration and Set\_Interface.

## Others (Bit6 and bit7) Reserved

## 3.16.3.25 EPx\_SINGLE Register

This register sets mode of FIFO in each endpoint (SINGLE/DUAL).

|                        | 7          | 6          | 5          | 4 | 3          | 2          | 1          | 0 |
|------------------------|------------|------------|------------|---|------------|------------|------------|---|
| EPx_SINGLE1<br>(07D1H) | EP3_SELECT | EP2_SELECT | EP1_SELECT |   | EP3_SINGLE | EP2_SINGLE | EP1_SINGLE |   |
| Read/Write             | R/W        | R/W        | R/W        |   | R/W        | R/W        | R/W        |   |
| Reset State            | 0          | 0          | 0          |   | 0          | 0          | 0          |   |

Note: Endpoint 3 support only SINGLE mode in the TMP92CF30.

Bit number

- 0: No use
- 1: EP1\_SINGLE
- 2: EP2\_SINGLE
- 3: EP3\_SINGLE
- 4: No use
- 5: EP1\_SELECT
- 6: EP2\_SELECT
- 7: EP3\_SELECT

When EPx\_SELECT bit is "1", EPx\_SINGLE bit becomes valid in the following content.

0: DUAL mode    1: SINGLE mode

If setting content of EPx\_SINGLE bit to valid, set EPx\_SELECT bit to "1".

0: Invalid    1: Valid

## 3.16.3.26 EPx\_BCS Register

This register sets mode of access to FIFO in each endpoint.

|                     | 7          | 6          | 5          | 4 | 3       | 2       | 1       | 0 |
|---------------------|------------|------------|------------|---|---------|---------|---------|---|
| EPx_BCS1<br>(07D3H) | EP3_SELECT | EP2_SELECT | EP1_SELECT |   | EP3_BCS | EP2_BCS | EP1_BCS |   |
| Read/Write          | R/W        | R/W        | R/W        |   | R/W     | R/W     | R/W     |   |
| Reset State         | 0          | 0          | 0          |   | 0       | 0       | 0       |   |

Bit number

- 0: No use
- 1: EP1\_BCS
- 2: EP2\_BCS
- 3: EP3\_BCS
- 4: No use
- 5: EP1\_SELECT
- 6: EP2\_SELECT
- 7: EP3\_SELECT

Always write "1" to EPx\_BCS bit regardless of whether endpoint is used or not.

0: Reserved    1: CPU access

If setting content of EPx\_BCS bit to valid, set EPx\_SELECT bit to "1".

0: Invalid    1: Valid

## 3.16.3.27 USBREADY Register

This register informs finishing writing data to descriptor RAM on UDC.

After assigned data to descriptor RAM, write “0” to bit0.

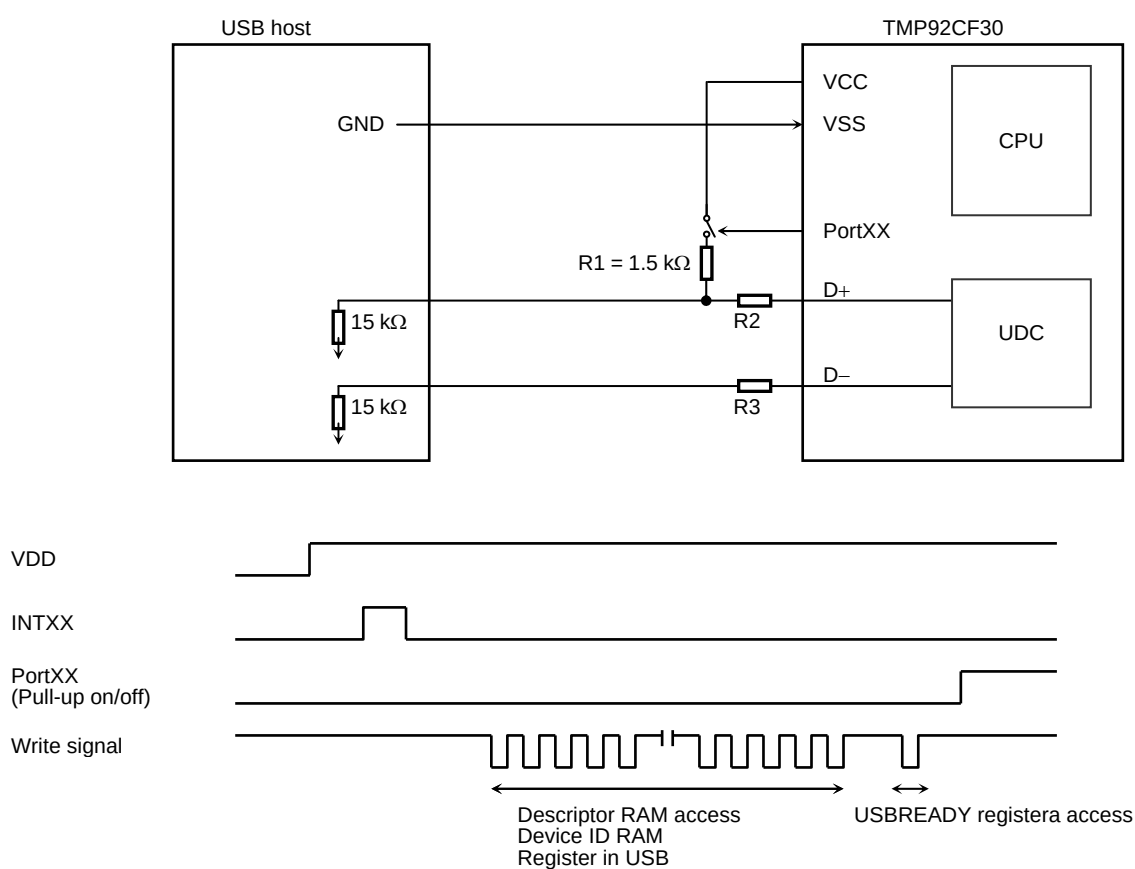
|                     | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
|---------------------|---|---|---|---|---|---|---|----------|
| USBREADY<br>(07E6H) |   |   |   |   |   |   |   | USBREADY |
| bit Symbol          |   |   |   |   |   |   |   |          |
| Read/Write          |   |   |   |   |   |   |   | R/W      |
| Reset State         |   |   |   |   |   |   |   | 0        |

## USBREADY (Bit0)

0: Writing to descriptor RAM has finished.

1: Writing to descriptor RAM is enabled.

(However, writing to descriptor RAM is prohibited when connected to host.)



Detect level of VDD signal from USB cable, and execute initialize sequence. In this case, UDC disable detecting USB\_RESET signal until USBREADY register is written “0” after release of USB\_RESET.

If the pull-up resistor on D+ signal is controlled by control signal, when pull-up resistor is connected to host in OFF condition, this condition is equivalent condition with USB\_RESET signal by pull-down resistor on the host side. Therefore UDC is not detected in USB\_RESET until “0” is written to USBREADY register

Note1: External pull-up resistor and control switch are needed with the TMP92CF30.

Note2: The above setting is an example for when communication. A specific circuit is required to prevent current flow at connector detection, no-use, and no connection.

## 3.16.3.28 Set Descriptor STALL Register

This register sets whether returns STALL automatically in data stage or status stage for Set Descriptor Request.

|                                    | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0         |
|------------------------------------|---|---|---|---|---|---|---|-----------|
| Set Descriptor<br>STALL<br>(07E8H) |   |   |   |   |   |   |   | S_D_STALL |
| bit Symbol                         |   |   |   |   |   |   |   |           |
| Read/Write                         |   |   |   |   |   |   |   | W         |
| Reset State                        |   |   |   |   |   |   |   | 0         |

## Bit0: S\_D\_STALL

0: Software control (Default)

1: Automatically STALL

## 3.16.3.29 Descriptor RAM Register

This register is used for store descriptor to RAM. The size of the descriptor is 384 bytes. However, when storing descriptor, write according to descriptor RAM structure sample.

|                                | 7         | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|--------------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Descriptor RAM<br>(0500H)<br>? | D7        | D6        | D5        | D4        | D3        | D2        | D1        | D0        |
| Read/Write                     | R/W       | R/W       | R/W       | R/W       | R/W       | R/W       | R/W       | R/W       |
| Reset State                    | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |

Read/Write timing is only possible before detection of USB\_RESET or during processing of SET\_DESCRIPTOR request.

SET\_DESCRIPTOR request processes from INT\_SETUP assert until access of EOP register.

If there is rewriting request of descriptor in SET\_DESCRIPTOR, process the request in the following sequence.

- 1) Read every packet of the descriptor that is transferred by SET\_DESCRIPTOR requests every packet.
- 2) When reading descriptor number of last packet finished, write all descriptors to RAM for descriptor.
- 3) When writing is completed, execute INIT\_DESCRIPTOR of COMMAND register.
- 4) When all the process is completed, access EOP register, and finish status stage.
- 5) When INT\_STAS is received, it shows normal finish of status stage.

If USB\_RESET is detected, it starts reading automatically. Therefore, when it connect to the host, executing INIT\_DESCRIPTOR command is not necessary.

### 3.16.4 Descriptor RAM

This area stores the descriptor that is defined in USB. Device, Config, Interface, Endpoint and String descriptor must set to RAM using the following format.

|                                                |                   |
|------------------------------------------------|-------------------|
| Device descriptor                              | 18 bytes          |
| Config 1 descriptor<br>(Interfaces, endpoints) | 255 bytes or less |
| Config 2 descriptor<br>(Interfaces, ENDPOINT)  | 255 bytes or less |
| String0 length                                 | 1 byte            |
| String1 length                                 | 1 byte            |
| String2 length                                 | 1 byte            |
| String3 length                                 | 1 byte            |
| String0 descriptor                             | 63 bytes or less  |
| String1 descriptor                             | 63 bytes or less  |
| String2 descriptor                             | 63 bytes or less  |
| String3 descriptor                             | 63 bytes or less  |

Note 1: If String Descriptor is supported, set StringxLength area to size0. No support String Dedcriptor is returned STALL.

Note 2: Config Descriptor refers to descriptor sample.

Note 3: Sequencer in UDC determines Config number, Interface number and Endpoint number. Therefore, if supporting Endpoint number is small, assign address according to priority.

Note 4: This function become effective only in case of store descriptor as RAM.

Note 5: RAM size is total 384 bytes.

Note 6: Possible timing in RD/WR of descriptor RAM is only before detection of USB\_RESET and processing of SET\_DESCRIPTOR request. (Prohibit access other than this timing.)

Writing must finish before connection to USB host and processing of SET\_DESCRIPTOR request.

SET\_DESCRIPTOR request processes from INT\_SETUP assert until access of EOP register.

Note 7: The class descriptor and the vender descriptors, etc except a standard descriptor cannot be supported by an auto bus enumeration.



## Descriptor RAM setting example:

| Address                                 | Data | Description         | Description               |
|-----------------------------------------|------|---------------------|---------------------------|
| Device Descriptor                       |      |                     |                           |
| 500H                                    | 12H  | bLength             |                           |
| 501H                                    | 01H  | bDescriptorType     | Device Descriptor         |
| 502H                                    | 00H  | bcdUSB (L)          | USB Spec 1.00             |
| 503H                                    | 01H  | bcdUSB (H)          | IFC's specify own         |
| 504H                                    | 00H  | bDeviceClass        |                           |
| 505H                                    | 00H  | bDeviceSubClass     |                           |
| 506H                                    | 00H  | bDeviceProtocol     |                           |
| 507H                                    | 08H  | bMaxPacketSize0     |                           |
| 508H                                    | 6CH  | bVendor (L)         | Toshiba                   |
| 509H                                    | 04H  | bVendor (H)         |                           |
| 50AH                                    | 01H  | IdProduct (L)       |                           |
| 50BH                                    | 10H  | IdProduct (H)       |                           |
| 50CH                                    | 00H  | bcdDevice (L)       | Release 1.00              |
| 50DH                                    | 01H  | bcdDevice (H)       |                           |
| 50EH                                    | 00H  | bManufacture        |                           |
| 50FH                                    | 00H  | IPProduct           |                           |
| 510H                                    | 00H  | bSerialNumber       |                           |
| 511H                                    | 01H  | bNumConfiguration   |                           |
| Config1 Descriptor                      |      |                     |                           |
| 512H                                    | 09H  | BLength             |                           |
| 513H                                    | 02H  | bDescriptorType     | Config Descriptor         |
| 514H                                    | 4EH  | wtotalLength (L)    | 78 bytes                  |
| 515H                                    | 00H  | wtotalLength (H)    |                           |
| 516H                                    | 01H  | bNumInterfaces      |                           |
| 517H                                    | 01H  | bConfigurationValue |                           |
| 518H                                    | 00H  | iConfiguration      |                           |
| 519H                                    | A0H  | bmAttributes        | Bus-powered-remote wakeup |
| 51AH                                    | 31H  | MaxPower            | 98 mA                     |
| Interface0 Descriptor AlternateSetting0 |      |                     |                           |
| 51BH                                    | 09H  | bLength             |                           |
| 51CH                                    | 04H  | bDescriptorType     | Interface Descriptor      |
| 51DH                                    | 00H  | bInterfaceNumber    |                           |
| 51EH                                    | 00H  | bAlternateSetting   | AlternateSetting0         |
| 51FH                                    | 01H  | bNumEndpoint        |                           |
| 520H                                    | 07H  | bInterfaceClass     |                           |
| 521H                                    | 01H  | bInterfaceSubClass  |                           |
| 522H                                    | 01H  | bInterfaceProtocol  |                           |
| 523H                                    | 00H  | iInterface          |                           |
| Endpoint1 Descriptor                    |      |                     |                           |
| 524H                                    | 07H  | bLength             |                           |
| 525H                                    | 05H  | bDescriptorType     | Endpoint Descriptor       |
| 526H                                    | 01H  | bEndpointAddress    | OUT                       |
| 527H                                    | 02H  | bmAttributes        | BULK                      |
| 528H                                    | 40H  | wMaxPacketSize (L)  | 64 bytes                  |
| 529H                                    | 00H  | wMaxPacketSize (H)  |                           |
| 52AH                                    | 00H  | bInterval           |                           |

| Address                                 | Data | Description        | Description          |
|-----------------------------------------|------|--------------------|----------------------|
| Interface0 Descriptor AlternateSetting1 |      |                    |                      |
| 52BH                                    | 09H  | bLength            |                      |
| 52CH                                    | 04H  | bDescriptorType    | Interface Descriptor |
| 52DH                                    | 00H  | bInterfaceNumber   |                      |
| 52EH                                    | 01H  | bAlternateSetting  | AlternateSetting1    |
| 52FH                                    | 02H  | bNumEndpoints      |                      |
| 530H                                    | 07H  | bInterfaceClass    |                      |
| 531H                                    | 01H  | bInterfaceSubClass |                      |
| 532H                                    | 02H  | bInterfaceProtocol |                      |
| 533H                                    | 00H  | iInterface         |                      |
| Endpoint1 Descriptor                    |      |                    |                      |
| 534H                                    | 07H  | bLength            |                      |
| 535H                                    | 05H  | bDescriptorType    | Endpoint Descriptor  |
| 536H                                    | 01H  | bEndpointAddress   | OUT                  |
| 537H                                    | 02H  | bmAttributes       | BULK                 |
| 538H                                    | 40H  | wMaxPacketSize (L) | 64 bytes             |
| 539H                                    | 00H  | wMaxPacketSize (H) |                      |
| 53AH                                    | 00H  | bInterval          |                      |
| Endpoint2 Descriptor                    |      |                    |                      |
| 53BH                                    | 07H  | bLength            |                      |
| 53CH                                    | 05H  | bDescriptorType    | Endpoint Descriptor  |
| 53DH                                    | 82H  | bEndpointAddress   | IN                   |
| 53EH                                    | 02H  | bmAttributes       | BULK                 |
| 53FH                                    | 40H  | wMaxPacketSize (L) | 64 bytes             |
| 540H                                    | 00H  | wMaxPacketSize (H) |                      |
| 541H                                    | 00H  | bInterval          |                      |
| Interface0 Descriptor AlternateSetting2 |      |                    |                      |
| 542H                                    | 09H  | bLength            |                      |
| 543H                                    | 04H  | bDescriptorType    | Interface Descriptor |
| 544H                                    | 00H  | bInterfaceNumber   |                      |
| 545H                                    | 02H  | bAlternateSetting  | AlternateSetting2    |
| 546H                                    | 03H  | bNumEndpoints      |                      |
| 547H                                    | FFH  | bInterfaceClass    |                      |
| 548H                                    | 00H  | bInterfaceSubClass |                      |
| 549H                                    | FFH  | bInterfaceProtocol |                      |
| 54AH                                    | 00H  | iInterface         |                      |
| Endpoint1 Descriptor                    |      |                    |                      |
| 54BH                                    | 07H  | bLength            |                      |
| 54CH                                    | 05H  | bDescriptorType    | Endpoint Descriptor  |
| 54DH                                    | 01H  | bEndpointAddress   | OUT                  |
| 54EH                                    | 02H  | bmAttributes       | BULK                 |
| 54FH                                    | 40H  | wMaxPacketSize (L) | 64 bytes             |
| 550H                                    | 00H  | wMaxPacketSize (H) |                      |
| 551H                                    | 00H  | bInterval          |                      |
| Endpoint2 Descriptor                    |      |                    |                      |
| 552H                                    | 07H  | bLength            |                      |
| 553H                                    | 05H  | bDescriptorType    | Endpoint Descriptor  |
| 554H                                    | 82H  | bEndpointAddress   | IN                   |
| 555H                                    | 02H  | bmAttributes       | BULK                 |
| 556H                                    | 40H  | wMaxPacketSize (L) | 64 bytes             |
| 557H                                    | 00H  | wMaxPacketSize (H) |                      |
| 558H                                    | 00H  | bInterval          |                      |

| Address                             | DATA | Description        | Description                  |
|-------------------------------------|------|--------------------|------------------------------|
| Endpoint3 Descriptor                |      |                    |                              |
| 559H                                | 07H  | bLength            |                              |
| 55AH                                | 05H  | bDescriptorType    | Endpoint Descriptor          |
| 55BH                                | 83H  | bEndpointAddress   | IN                           |
| 55CH                                | 03H  | bmAttributes       | Interrupt                    |
| 55DH                                | 08H  | wMaxPacketSize (L) | 8 bytes                      |
| 55EH                                | 00H  | wMaxPacketSize (H) |                              |
| 55FH                                | 01H  | bInterval          | 1 ms                         |
| String Descriptor Length Setup Area |      |                    |                              |
| 560H                                | 04H  | bLength            | Length of String Descriptor0 |
| 561H                                | 10H  | bLength            | Length of String Descriptor1 |
| 562H                                | 00H  | bLength            | Length of String Descriptor2 |
| 563H                                | 00H  | bLength            | Length of String Descriptor3 |
| String Descriptor0                  |      |                    |                              |
| 564H                                | 04H  | bLength            |                              |
| 565H                                | 03H  | bDescriptorType    | String Descriptor            |
| 566H                                | 09H  | bString            | Language ID 0x0409           |
| 567H                                | 04H  | bString            |                              |
| String Descriptor1                  |      |                    |                              |
| 568H                                | 10H  | bLength            |                              |
| 569H                                | 03H  | bDescriptorType    | String Descriptor            |
| 56AH                                | 00H  | bString            | (Toshiba)                    |
| 56BH                                | 54H  | bString            | T                            |
| 56CH                                | 00H  | bString            |                              |
| 56DH                                | 6FH  | bString            | o                            |
| 56EH                                | 00H  | bString            |                              |
| 56FH                                | 73H  | bString            | s                            |
| 570H                                | 00H  | bString            |                              |
| 571H                                | 68H  | bString            | h                            |
| 572H                                | 00H  | bString            |                              |
| 573H                                | 69H  | bString            | i                            |
| 574H                                | 00H  | bString            |                              |
| 575H                                | 62H  | bString            | b                            |
| 576H                                | 00H  | bString            |                              |
| 577H                                | 61H  | bString            | a                            |
| String Descriptor2                  |      |                    |                              |
| String Descriptor3                  |      |                    |                              |

### 3.16.5 Device Request

#### 3.16.5.1 Standard request

UDC support automatically answer in standard request.

##### (1) GET\_STATUS Request

This request automatically returns to status that is determined by receive side.

| bmRequestType                       | bRequest   | wValue | wIndex                     | wLength | Data                                    |
|-------------------------------------|------------|--------|----------------------------|---------|-----------------------------------------|
| 10000000B<br>10000001B<br>10000010B | GET_STATUS | 0      | 0<br>Interface<br>endpoint | 2       | Device, interface or<br>endpoint status |

Request to device returns according to priority of little endian as follows.

| D7  | D6  | D5  | D4  | D3  | D2  | D1               | D0            |
|-----|-----|-----|-----|-----|-----|------------------|---------------|
| 0   | 0   | 0   | 0   | 0   | 0   | Remote<br>wakeup | Self<br>power |
| D15 | D14 | D13 | D12 | D11 | D10 | D9               | D8            |
| 0   | 0   | 0   | 0   | 0   | 0   | 0                | 0             |

- Remote wakeup Reinstates current remote wakeup setting.  
This bit is set or reset by SET\_FEATURE or CLEAR\_FEATURE request. Default is "0".
- Self power Reinstates current power supply setting. This bit return Self or Bus Power according to value that is set to bmAttributes field in Config descriptor.

Request to interface returns 00H of 2 bytes.

Request to endpoint returns according to priority of little endian as follows.

| D7  | D6  | D5  | D4  | D3  | D2  | D1 | D0   |
|-----|-----|-----|-----|-----|-----|----|------|
| 0   | 0   | 0   | 0   | 0   | 0   | 0  | HALT |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8   |
| 0   | 0   | 0   | 0   | 0   | 0   | 0  | 0    |

- HALT Returns to halt status of selected endpoint.

## (2) CLEAR\_FEATURE request

This request clears or disables the relevant function.

| bmRequestType                       | bRequest          | wValue              | wIndex                     | wLength | Data |
|-------------------------------------|-------------------|---------------------|----------------------------|---------|------|
| 00000000B<br>00000001B<br>00000010B | CLEAR_<br>FEATURE | Feature<br>selector | 0<br>Interface<br>endpoint | 0       | None |

- Reception side device
  - Feature selector: 1 Present remote wakeup setting is disabled.
  - Feature selector: except 1 STALL state
- Reception side interface
  - STALL state
- Reception side end point
  - Feature selector: 0 Halt of relevant endpoint is cleared.
  - Note: When cleared HALT state, following is set.
    - Initialize FIFO
    - Clear the toggle sequence bit
    - Clear STALL state
  - Feature selector: except 0 STALL state

Note: Stalls if request is to non-existent endpoint.

## (3) SET\_FEATURE request

This request sets or enables the relevant function.

| bmRequestType                       | bRequest        | wValue              | wIndex                     | wLength | Data |
|-------------------------------------|-----------------|---------------------|----------------------------|---------|------|
| 00000000B<br>00000001B<br>00000010B | SET_<br>FEATURE | Feature<br>selector | 0<br>Interface<br>endpoint | 0       | None |

- Reception side device
  - Feature selector: 1 Present remote wakeup setting is disabled.
  - Feature selector: except 1 STALL state
- Reception side interface
  - STALL state
- Reception side end point
  - Feature selector: 0 Halt of relevant endpoint
  - Feature selector: except 0 STALL state

Note: Stalls if request is to non-existent endpoint.

## (4) SET\_ADDRESS request

This request sets the device address. Answer subsequent requests using this device address.

Answer requests using the current device address until the status stage of this request is terminated normally.

| bmRequestType | bRequest    | wValue         | wIndex | wLength | Data |
|---------------|-------------|----------------|--------|---------|------|
| 00000000B     | SET_ADDRESS | Device Address | 0      | 0       | None |

## (5) GET\_DESCRIPTOR request

This request returns appointed descriptor.

| bmRequestType | bRequest       | wValue                               | wIndex                 | wLength           | Data       |
|---------------|----------------|--------------------------------------|------------------------|-------------------|------------|
| 10000000B     | GET_DESCRIPTOR | Descriptor type and Descriptor index | 0<br>or<br>Language ID | Descriptor length | Descriptor |

- Device      Device transmits device descriptor that is stored in descriptor RAM.
- Config      Config transmits config descriptor that is stored in descriptor RAM.  
At this point, it transmits not only config descriptor but also interface and endpoint descriptor.
- String      String transmits string descriptor of index that is specified by lower byte of wValue field.

Note: Descriptor of short data length in wLength and descriptor length is automatically transmitted by answer of Get\_Descriptor.

## (6) SET\_DESCRIPTOR request

This request sets or enables the relevant function.

| bmRequestType | bRequest       | wValue                                  | wIndex                 | wLength           | Data       |
|---------------|----------------|-----------------------------------------|------------------------|-------------------|------------|
| 00000000B     | SET_DESCRIPTOR | Descriptor type and<br>Descriptor index | 0<br>or<br>Language ID | Descriptor length | Descriptor |

Automatic answer of this request is not supported.

According to INT\_SETUP interrupt, if the receiving requested has been identified as a SET\_DESCRIPTOR request, take back data after confirming EP0\_DSET\_A bit of DATASET register is "1". When completed, access EOP register, and write "0" to EP0\_EOPB bit, so, status stage is finished. The process is the same for a vendor request.

Please refer to vendor request section.

## (7) GET\_CONFIGURATION request

This request returns configuration value of present device.

| bmRequestType | bRequest   | wValue | wIndex | wLength | Data                |
|---------------|------------|--------|--------|---------|---------------------|
| 10000000B     | GET_CONFIG | 0      | 0      | 1       | Configuration value |

If it is not configured, it returns "0". Otherwise, it returns the configuration value.

## (8) SET\_CONFIGURATION request

This request sets device configuration.

| bmRequestType | bRequest   | wValue              | wIndex | wLength | Data |
|---------------|------------|---------------------|--------|---------|------|
| 00000000B     | SET_CONFIG | Configuration value | 0      | 0       | None |

The configuration value is that specified using lower byte of wValue field.

When this value is "0", it is not configured.

## (9) GET\_INTERFACE request

This request returns AlternateSetting value that is set by specified interface.

| bmRequestType | bRequest      | wValue | wIndex    | wLength | Data              |
|---------------|---------------|--------|-----------|---------|-------------------|
| 10000001B     | GET_INTERFACE | 0      | Interface | 1       | Alternate setting |

If there is no specified interface, it enters to STALL state.

## (10) SET\_INTERFACE request

This request selects AlternateSetting in specified interface.

| bmRequestType | bRequest      | wValue            | wIndex    | wLength | Data |
|---------------|---------------|-------------------|-----------|---------|------|
| 00000001B     | SET_INTERFACE | Alternate setting | Interface | 0       | None |

If there is no specified interface, it enters STALL state.

## (11) SYNCH\_FRAME request

This request transmits synchronous frame of endpoint.

| bmRequestType | bRequest    | wValue | wIndex   | wLength | Data      |
|---------------|-------------|--------|----------|---------|-----------|
| 10000010B     | SYNCH_FRAME | 0      | Endpoint | 2       | Frame No. |

Automatic answer of this request is not supported.

According to INT\_SETUP interrupt, if request received has been identified as a SYNCH\_FRAME request, write 2byte data in Frame No after confirming EP0\_DSET\_A bit of DATASET register is "0". When completed, access EOP register, and write "0" to EP0\_EOPB bit, so, status stage is completed. This can be used only where the endpoint supports isochronous transfer type and supports this request. The process is the same for a vendor request.

Please refer to vendor request section.



### 3.16.5.2 Printer Class Request

UDC does not support “Automatic answer” of printer class request.

Processing of Class requests is the same as for vendor requests when answering INT\_SETUP interrupt.

### 3.16.5.3 Vendor request (Class request)

UDC does not support “Automatic answer” of Vendor requests.

According to INT\_SETUP interrupt, access the register in which the device request is stored, and identify the request. If this request is a Vendor request, control the UDC externally, and process the Vendor request.

Below is an explanation for the case where data phase is transmitting (Control read), and for the case where data phase is receiving (Control write).

(a) Control Read request

| bmRequestType | bRequest        | wValue          | wIndex          | wLength                       | Data        |
|---------------|-----------------|-----------------|-----------------|-------------------------------|-------------|
| 110000xxB     | Vendor specific | Vendor specific | Vendor specific | Vendor specific<br>(Expire 0) | Vendor data |

When INT\_SETUP is received, identify contents of request by bmRequestType, bRequest, wValue, wIndex and wLength registers and process each request. According to application, access Setup\_Received register after request has been identified. UDC must also be informed that INT\_SETUP interrupt has been recognized.

After transmitting data prepared in application, access DATASET register, and confirm EP0\_DSET\_A bit is “0”. After confirming, write data FIFO of endpoint 0. If transmitting data is more than payload, write data after it confirming whether EP0\_DSET\_A bit in DATASET register is “0”. (INT\_ENDPOINT0 interrupt can be used.) If writing all data is finished, write “0” to EP0 bit of EOP register. When UDC receives this, the status stage finish automatically.

INT\_STATUS interrupt is asserted when UDC finishes status stage normally. If finishing status stage normally is recognized by external application, manage this stage by using this interrupt signal. If status stage cannot be finished normally and during status stage, a new SETUP token maybe received. In this case, when INT\_SETUP interrupt signal is asserted, “1” is set to STAGE\_ERROR bit of EP0\_STATUS register Informing externally that the status stage cannot be finished normally.

The dataphase may have finished on a data number that is shorter than the value showed to wLength by protocol of control read transfer type in USB. If the application program is configured using only the wLength value, processing cannot be carried out when the host shifts status stage without arriving at the expected data number. At this point, shifting to status stage can be confirmed by using INT\_STATUSNAK interrupt signal. (However, releasing mask of STATUS\_NAK bit by using interrupt control register is needed.) In Vendor Request, this problem will not occur because the receiving buffer size is set to host controller by driver (In every host, data (data that is transmitted from device by payload of 8 bytes) may be taken to be short packet until confirmation of payload size on device side. Therefore, exercise care if controlling standard requests by software.)

## (b) Control write/request

There is no dataphase

| bmRequestType | bRequest        | wValue          | wIndex          | wLength | Data |
|---------------|-----------------|-----------------|-----------------|---------|------|
| 010000xxB     | Vendor specific | Vendor specific | Vendor specific | 0       | None |

When INT\_SETUP is received, identify contents of request by bmRequestType, bRequest, wValue, wIndex, wLength registers and process each request. According to application, access Setup\_Received register after request has been identified. UDC must also be informed that the INT\_SETUP interrupt has been recognized. If application processing is finished, write “0” to EP0 bit of EOP register. When UDC receives this, the status stage finish automatically.

There is dataphase

| bmRequestType | bRequest        | wValue          | wIndex          | wLength                           | Data        |
|---------------|-----------------|-----------------|-----------------|-----------------------------------|-------------|
| 010000xxB     | Vendor specific | Vendor specific | Vendor specific | Vendor specific<br>(Except for 0) | Vendor data |

When INT\_SETUP is received, identify contents of device request by bmRequestType, bRequest, wValue, wIndex, wLength registers and process each request. According to application, access Setup\_Received register after request has been identified. UDC must also be informed that the INT\_SETUP interrupt has been recognized.

After receiving data prepared in application, access DATASET register, and confirm EP0\_DSET is “1”. After confirming, read data FIFO of endpoint 0. If receiving data is more than payload, write data after it confirming whether the EP0\_DSET\_A bit in DATASET register is “1”. (INT\_ENDPOINT0 interrupt can be used.) If reading all data is finished, write “0” to EP0 bit of EOP register. When UDC receives this, the status stage finishes automatically.

INT\_STATUS interrupt is asserted when UDC finishes status stage normally. If finishing status stage normally is recognized by external application, manage this stage by using this interrupt signal. If status stage cannot be finished normally and during status stage, a new SETUP token may be received. In this case, when INT\_SETUP interrupt signal is asserted, “1” is set to STAGE\_ERROR bit of EP0\_STATUS register informing externally that the status stage cannot be finished normally.

Below is control flow in UDC as seen from application.

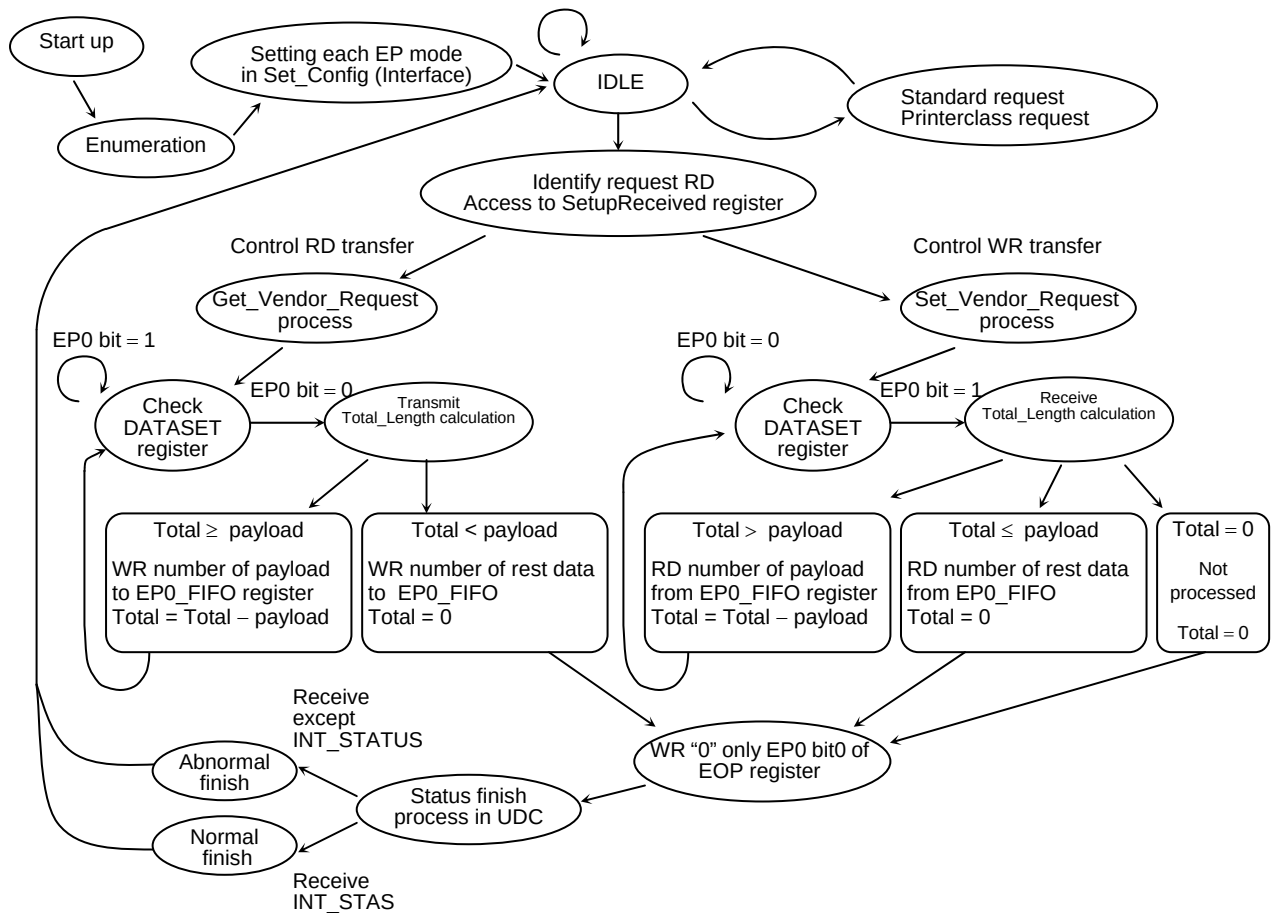


Figure 3.16.2 Control Flow in UDC as seen from Application

Note : This chart does not cover special cases in this flow such as overlap receive SETUP packet.

Please refer to 3.17.6 (2) (c) Control transfer type.

### 3.16.6 Transfer mode and Protocol Transaction

The UDC performs the following automatically in hardware;

- Receive packet
- Determine address endpoint transfer mode
- Error process
- Confirm toggle bit CRC of data receiving packet
- Generate toggle bit CRC of data transmitting packet, etc
- Handshake answer

#### (1) Protocol outline

Format of USB packet is shown below. This is processed during transmission and receiving by hardware into the UDC.

- SYNC field

This field always comes first in each packet, and input data and internal CLK is synchronized in the UDC.

- Packet identification field (PID)

This field follows SYNC field in every USB packet. The UDC distinguishes the PID type and determines the transfer type by decoding this code.

- Address field

The UDC uses this field to confirm whether or not this function was specified by the host. The UDC compares the address with that set to the ADDRESS register. If the address accords with it, the UDC continues the process. If the address does not accord, the UDC ignores this token.

- Endpoint field

If sub-channels of more than two is needed in fields of 4 bits, it decides the function. The UDC can support a maximum of seven endpoints, excluding the control endpoint. Tokens for endpoints that are not permitted are ignored.

- Frame number field

A field of 11 bits is added by the host at each frame. This field follows the SOF token that is transmitted first in each frame, and the frame number is specified. The UDC reads the content of this field when the SOF token is received, and sets the frame number to the FRAME register.

- Data field

This field is data of unit bytes in 0 to 1023. When receiving it, the UDC transfers only part of this data to FIFO, and after CRC is confirmed, an interrupt signal is asserted and the UDC informs FIFO that data transfer is completed. When transmitting, following IN token, FIFO data is transferred. Finally, data CRC field is attached.

- CRC function

5 bits CRC is attached to the token, and 15 bits CRC to the data. The UDC automatically compares the CRC of the received data with the attached CRC. When transmitting, CRC is generated automatically and is transmitted. This function may be compared by various transfer modes.

(2) Transfer mode

UDC supports FULL speed transfer mode.

- FULL speed device

Control transfer type

Interrupt transfer type

Bulk transfer type

Isochronous transfer type

The following is an explanation of UDC operation in each transfer mode.

The explanation is of data flow up until FIFO.

(a) Bulk transfer type

Bulk transfer type warrants transferring no error between host and function by using detect error and retry. Basically, 3 phases are used - token, data and handshake. However, with flow control and a STALL condition, data phase is changed to hand shake phase, and it become to 2 phases. The UDC holds status of each endpoint, and flow control is controlled in hardware. Each endpoint condition can be confirmed using EPx\_STATUS register.

## (a-1) Transmission bulk mode

Below is the transaction format for bulk transfer during transmitting.

- Token: IN
- Data: DATA0/DATA1, NAK, STALL
- Handshake: ACK

Control flow

Below is the control-flow when the UDC receive an IN token.

1. The token packet is received and the address endpoint number error is confirmed, and it checks whether the relevant endpoint transfer mode corresponds with the IN token. If it does not correspond, the state returns to IDLE.
2. Condition of EPx\_STATUS register is confirmed.
  - INVALID condition: State returns to IDLE.
  - STALL condition: Stall handshake is returned and state returns to IDLE.FIFO condition is confirmed, if data number of 1 packet is not prepared, NAK handshake is returned, and state returns to IDLE.  
If data number of 1 packet is prepared to FIFO, it shifts to 3.
3. Data packet is generated.  
Data packet generated by using toggle bit register in UDC.  
Next, data is transferred from FIFO of internal UDC to SIE, and data packet is generated. At this point, the confirms transferred data number is confirmed. And if there is more than the maximum payload size of each endpoint, bit stuff error is generated, transfer is finished and STATUS becomes STALL.
4. CRC bit (counted transfer data of FIFO from first to last) is attached to last.
5. When ACK handshake from host is received,
  - Clear FIFO.
  - Clear DATASET register.
  - Renew toggle bit, and prepare for next.
  - Set STATUS to READY.

UDC finishes normally. FIFO can receive the next data.

If a time out occurs without receiving ACK from host,

- Set STATUS to TX\_ERR.
- Return FIFO address pointer.

Execute above setting. And wait next retry keeping FIFO data.

This flow is shown in Figure 3.16.3.

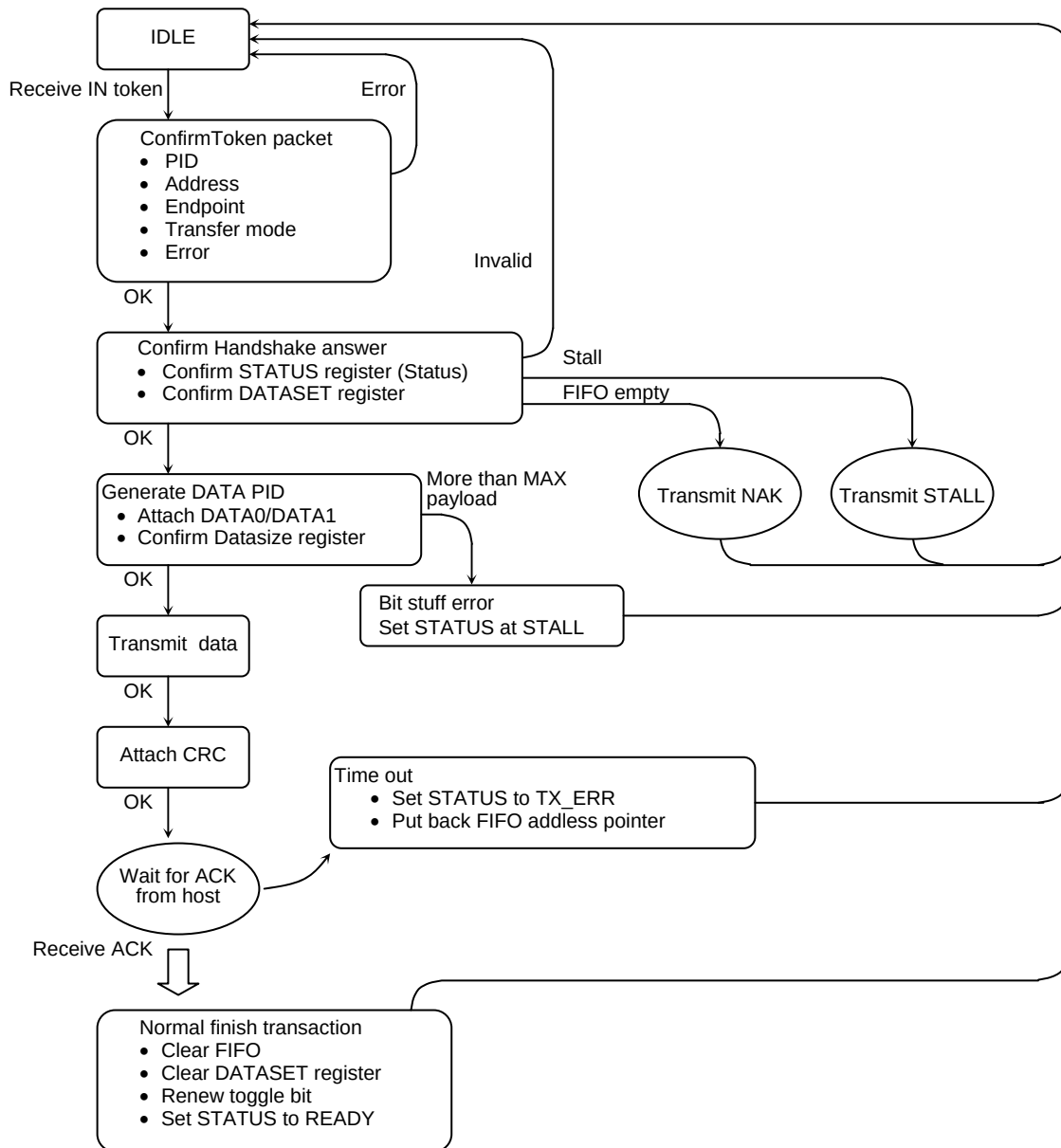


Figure 3.16.3 Control Flow in UDC (Bulk transfer type (transmission)/Interrupt transfer type (transmission))

## (a-2) Receiving bulk mode

Below is the transaction format for receiving bulk transfer type.

- Token: OUT
- Data: DATA0/DATA1
- Handshake: ACK, NAK, STALL

Control flow

Below is the control-flow when the UDC receive an IN token.

1. The token packet is received and the address endpoint number error is confirmed, and it checks whether the relevant endpoint transfer mode corresponds with the OUT token. If it does not correspond, the state returns to IDLE.
2. Condition of status register is confirmed.
  - INVALID condition: State returns to IDLE.
  - STALL condition: When dataphase finishes, stall handshake is returned, the state returns to IDLE, and data is canceled.

FIFO condition is confirmed, if data number of 1 packet is not prepared, present transferred data is canceled, NAK handshake is returned after dataphase, and the state returns to IDLE.

3. Data packet is received.

Data is transferred from SIE of internal UDC to FIFO. At this point, it confirms transferred data number and if there is more than the maximum payload size of each endpoint, STATUS becomes to STALL and the state returns to IDLE. ACK handshake does not return.
4. After last data is transferred, the counted CRC is compared with the transferred CRC. If they do not correspond, STATUS is set to RX\_ERR and the state returns to IDLE. At this point ACK is not returned.

After retry, when next data is received normally, STATUS changes to DATIN. If the data toggle does not correspond, it is judged not to have taken ACK in the last loading the current loading is regarded as a retry of the last loading and data is canceled. Set STATUS as RX\_ERR, return to host and return to IDLE. FIFO address pointer returns and the next data can be received.
5. If CRC is compared with toggle and it finishes normally, ACK handshake is returned.

Below is the process in the UDC.

- Set transfer data number to DATASIZE register.
- Set DATASET register.
- Renew toggle bit, and prepare for next.
- Set STATUS to READY.

UDC finishes normally.

This flow is shown in Figure 3.16.4.



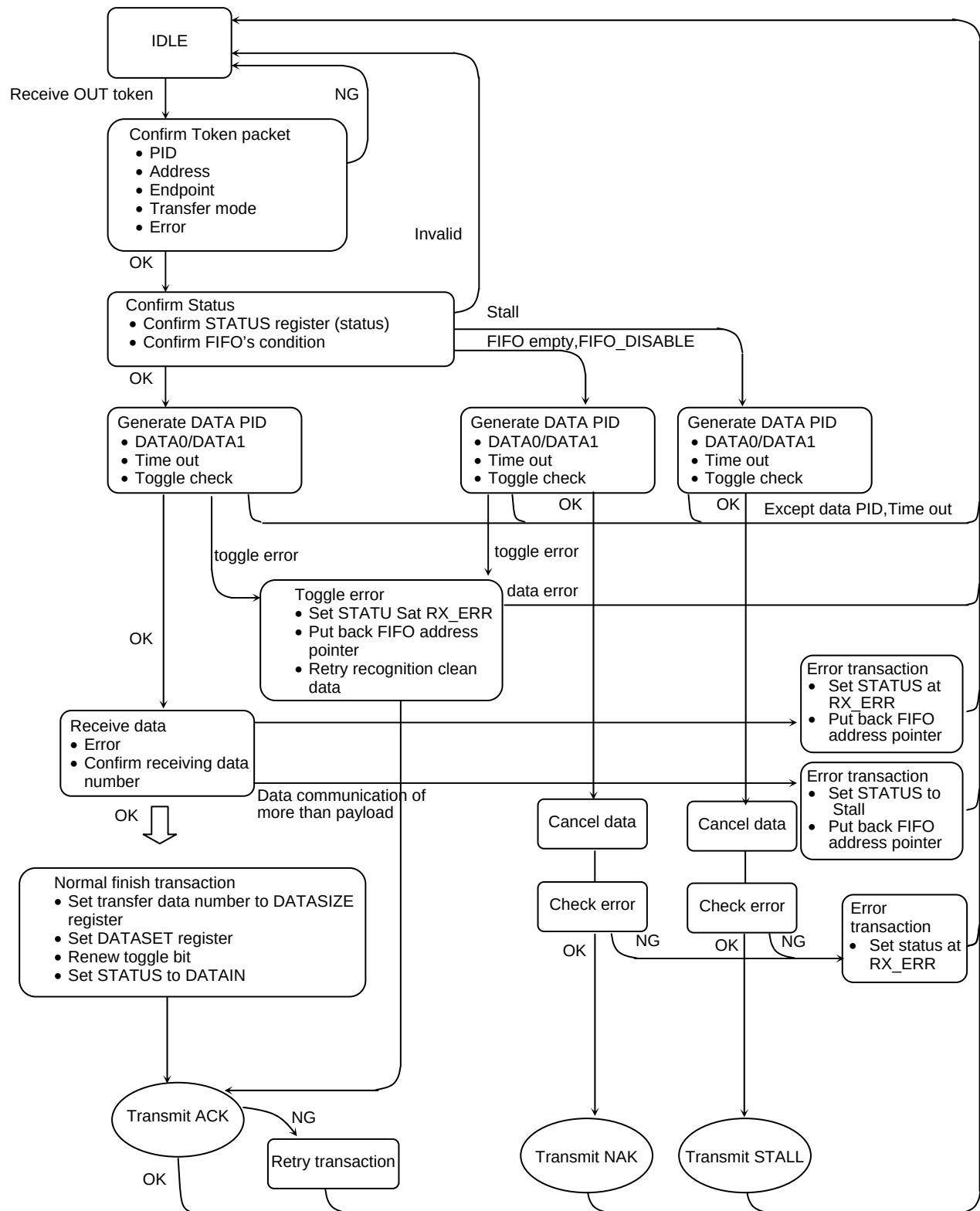


Figure 3.16.4 Control Flow in UDC (Bulk transfer type (Receiving))

(b) Interrupt transfer type

Interrupt transfer type uses the same transaction format as transmission bulk transfer.

For transmission using toggle bit, hardware setting and answer in the UDC are the same as for transmission bulk transfer. Interrupt transfer can be transferred without using toggle bit. In this case, if ACK handshake from host is not received, toggle bit is renewed, and finish is normal. The UDC clears FIFO for next transfer.

(b-1) Interrupt transmitting mode (Toggle mode)

UDC operation is same as in bulk transmission mode. Please refer to section (a).

(b-2) Interrupt transmission mode (Not toggle mode)

This is basically the same as bulk transmission mode. However, if ACK handshake from host is not received, transaction is different.

When ACK handshake from host is received after transmission of data packet

- Clear FIFO.
- Clear DATASET register.
- Renew toggle bit and prepare for next.
- Set STATUS to READY.

UDC finishes normally by above transaction. FIFO can receive next data.

If a time out occurs without receiving ACK from host,

- Clear FIFO.
- Clear DATASET register.
- Renew toggle bit and prepare for next.
- Set STATUS to TX\_ERR.

Execute above setting. This setting is the same except for STATUS changes.

## (c) Control transfer type

Control transfer type is configured in the three stages below.

- Setup stage
- Data stage
- Status stage

Data stage is sometimes skipped. Each stage is configured in one or several transactions. The UDC executes each transaction while managing three stages in hardware. Control transfer has the 3 types given below depending on whether there is data stage or not, and on direction.

- Control read transfer type
- Control write transfer type
- Control write transfer type (No data stage)

The 3 transfer sequences are shown in Figure 3.16.6, Figure 3.16.7 and Figure 3.16.8.

The UDC automatically answers standard requests in hardware. Class request and vendor request must have an intervening CPU controlling the UDC.

Below is the control flow in the UDC and the control flow in the intervening CPU.

## (c-1) Setup stage

Setup stage is the same as transmission bulk transaction except that token ID becomes SETUP.

However, control flow in the UDC is different.

- Token: SETUP
- Data: DATA 0
- Handshake: ACK

Control flow

Below is the control flow in the UDC when SETUP token is received.

1. SETUP token packet is received and address, endpoint number and error are confirmed. It also checks whether the relevant endpoint is in control transfer mode.
2. STATUS register state is confirmed.

State return to IDLE only if it is INVALID state.

In bulk transfer mode, receiving data is enabled by STATUS registers value and FIFO condition. However, in SETUP stage, STATUS is returned to READY and accessing from the CPU to FIFO is always prohibited and internal FIFO of endpoint 0 is cleared. It also prepares for following dataphase.

If the CPU accesses Setup Received registers in the UDC, it recognizes as Device request as received, and accessing from the CPU to EP0 is enabled.

This function is for receiving a new request when the current device request has not finished normally.

3. Data packet is received.

Device request of 8 bytes from SIE in UDC is transferred to the request register below.

- bmRequestType register
- bmRequest register
- wValue register
- wIndex register
- wLength register

4. After last data is transferred, counted CRC is compared with transferred CRC. If they do not correspond, STATUS is set to RX\_ERR and the state returns to IDLE. At this point it does not return ACK, and host retries.

5. If CRC corresponds with toggle and it finishes normally, ACK handshake is returned to host. The process in the UDC is shown below.

- Receiving device request is judged whether software control or hardware control. If the request needs control in software, INT\_SETUP interrupt is asserted. If hardware is used, INT\_SETUP interrupt is not asserted.
- According to stage control flow, prepare for next stage.
- Set STATUS to DATAIN.
- Set toggle bit to "1".

The Setup stage is completed by the above.

This flow is shown in Figure 3.16.2.

8-byte data that is transferred by this SETUP stage is device request.

The CPU must process corresponding to device request.

The UDC detects the following contents only from data of 8 bytes, and it manages stage in hardware.

- Whether there is data stage or not
- Data stage direction

These are used to determine control read transfer type, control write transfer type, and control write transfer type (no data phase).

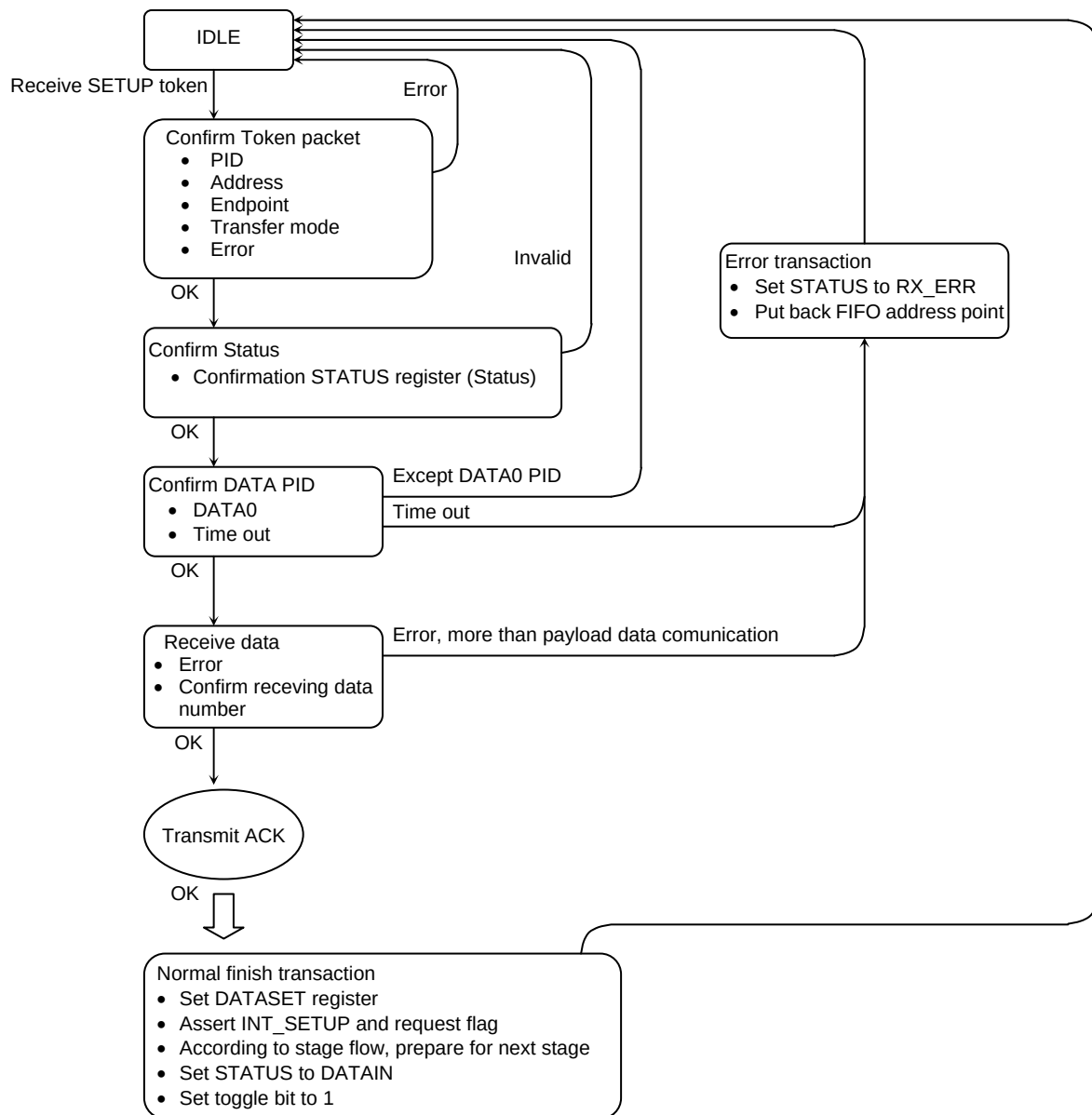


Figure 3.16.5 Control Flow in UDC (Setup stage)

## (c-2) Data stage

Data stage is configured by one or several transactions based on toggle sequence.

The transaction is the same as for format transmission or receiving bulk transaction except for the following differences;

- Toggle bit starts from “1” by SETUP stage.
- It determines whether right or not by comparing IN and OUT token with direction bit of device request. If a token of the opposite direction is received, it is recognized as status stage.
- INT\_ENDPOINT0 interrupt is asserted.

## (c-3) Status stage

Status stage is configured 0-data-length packet with DATA1's PID and handshake IN or OUT token. It uses a transaction in the opposite direction to the preceding stage.

The combination is given below.

- Control read transfer type: OUT
- Control write transfer type: IN
- Control write transfer type (not dataphase): IN

UDC processes status stage base of control flow in control transfer type. At this point, CPU must write “0” to EP0 bit of EOP register in last transaction for status stage to finish normally.

Details of status stage are given below.

## (c-3-1) IN status stage

IN status stage transaction format is given below.

- Token: IN
- Data: DATA1 (0 data length), NAK, STALL
- Handshake: ACK

Control flow

The transaction flow of IN status stage in UDC is given below.

1. Token packet is received and address, endpoint number and error are confirmed. If it does not correspond, the state returns to IDLE. If status stage is enabled based on stage control flow in the UDC, advance to next stage.
2. STATUS register state is confirmed.
  - INVALID condition: State returns to IDLE.
  - STALL condition: Stall handshake is returned and state returns to IDLE.

Confirmation of whether EOP register is accessed or not is carried out externally. If it is not accessing, NAK handshake is returned to continue control transfer and state returns to IDLE.

3. If EOP register is access is confirmed, 0-data-length data packet and CRC are transmitted.

4. If ACK handshake from host is received,
  - Set STATUS to READY.
  - Assert INT\_STATUS interrupt.

It finishes normally by the above transaction.

If a time out occurs without receiving ACK from host,

- Set STATUS register to TX\_ERR and state returns to IDLE and wait for restrung status stage.

At this point, if new SETUP stage is started without status stage finishing normally, the UDC sets error to STATUS register.

#### (c-3-2) OUT status stage

The transaction format for OUT status stage is given below.

- Token: OUT
- Data: DATA1 (0 data length)
- Handshake: ACK, NAK, STALL

#### Control flow

The transaction flow for OUT status stage in the UDC is given below.

1. Token packet is received and address, endpoint number and error are confirmed. If they do not correspond, the state returns to IDLE. If status stage is enabled base on stage control flow in the UDC, advance to next stage.
2. STATUS register state is confirmed.
  - INVALID condition: State returns to IDLE.
  - STALL condition: Data is cleared, stall handshake is returned, and state returns to IDLE.

Whether EOP register is accessed or not is confirmed externally. If it is not accessed, NAK handshake is returned to continue control transfer and state returns to IDLE.

3. If EOP register is access is confirmed, 0-data-length data packet and CRC are received.
4. If there is no error in data, ACK handshake is transmitted to host.
  - Set STATUS to READY.
  - Assert INT\_STATUS interrupt.

It finishes normally by the above transaction.

If there is an error in data, ACK handshake is not returned.

- Set RX\_ERR to STATUS register and return to IDLE. It waits to retry status stage.

At this point, if new SETUP stage is started without status stage finishing normally, the UDC sets error to STATUS register. For sequence of this protocol, refer to section supplement.

## (c-4) Stage management

The UDC manages each stage of control transfer by hardware.

Each stage is changed by receiving token from USB host, or CPU accesses register. Each stage in control transfer type has to process combination software. UDC detects the following contents from 8-byte data in SETUP stage. The stage is managed by determining control transfer type.

- Whether there is data stage or not
- Data stage direction

Based on these it is determines to be either control read transfer type control write transfer type, or control write transfer type (No data stage).

Various conditions for changing stage in control transfer are given below.

If receiving token for next stage from host before switching to next stage from state of internal UDC, NAK handshake is returned and BUSY is informed to USB host. In all control transfer types, if SETUP token is received from host current transaction is stopped, and it switches to SETUP stage in the UDC. The CPU receives new INT\_SETUP even if it is processing previous control transfer.



### Stage change condition of control read transfer type

1. Receive SETUP token from host
  - Start setup stage in UDC.
  - Receive data in request normally and judge. And assert INT\_SETUP interrupt externally.
  - Change data stage in the UDC.
2. Receive IN token from host
  - The CPU receives a request from the request register every INT\_SETUP interrupt.
  - Judge request and access Setup Received register to inform the UDC that INT\_SETUP interrupt has been recognized.
  - According to Device request, monitor EP0 bit of DATASET register, and write data to FIFO.
  - If the UDC is set data of payload to FIFO or CPU set short packet transfer in EOP register, EP0 bit of DATASET register is set.
  - The UDC transfers data that is set to FIFO to host by IN token interrupts.
  - When the CPU finishes transaction, it writes "0" to EP0 bit of EOP register.
  - Change status stage in the UDC.
3. Receive OUT token from host.
  - Return ACK to OUT token, and change state to IDLE in the UDC.
  - Assert INT\_STATUS interrupt externally.

These changing conditions are shown in Figure 3.16.6.

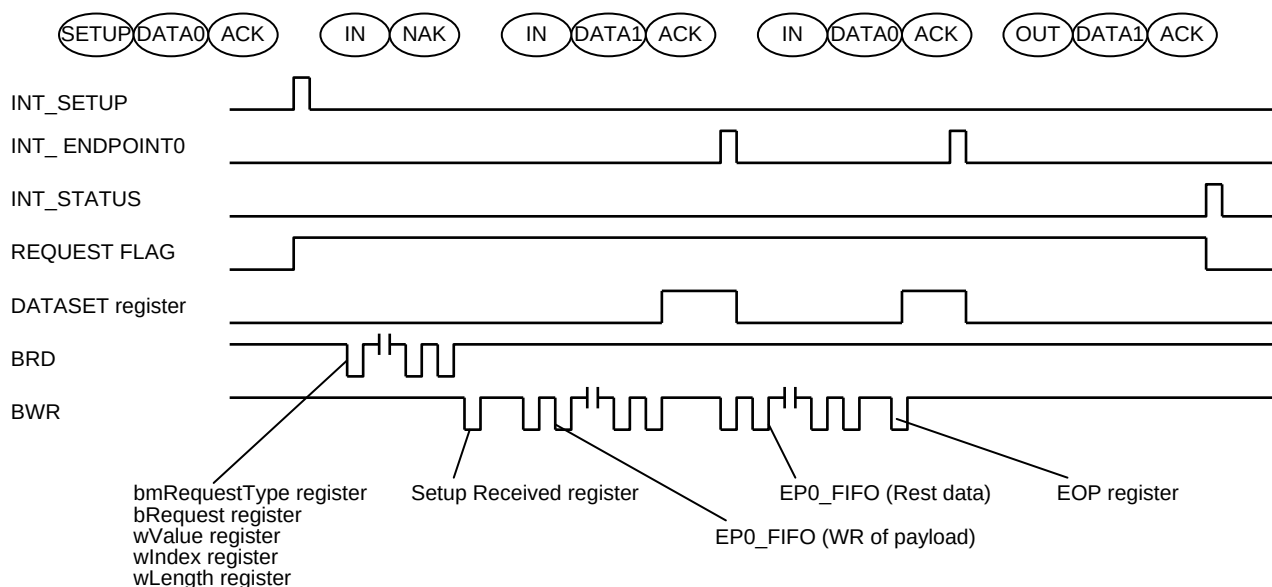


Figure 3.16.6 The Control Flow in UDC (Control Read Transfer Type)

## Stage change condition of control write transfer type

1. Receive SETUP token from host.
  - Start setup stage in the UDC.
  - Receive data in request normally and judge. And assert INT\_SETUP interrupt externally.
  - Change data stage in the UDC.
2. Receive OUT token from host.
  - CPU receives a request from the request register every INT\_SETUP interrupt.
  - Judge request and access Setup Received register for inform the UDC that INT\_SETUP interrupt has been recognized.
  - Receive dataphase data normally, and set EP0 bit of DATASET register.
  - The CPU receives data in FIFO by setting DATASET.
  - The CPU processes receiving data by device request.
  - When the CPU finishes transaction, it writes "0" to EP0 bit of EOP register.
  - Change status stage in the UDC.
3. Receive IN token from host.
  - Return data packet of 0 data to IN token, and change state to IDLE in the UDC.
  - Assert INT\_STATUS interrupt externally when ACK for 0 data packet is received.

These changing conditions are shown in Figure 3.16.7.

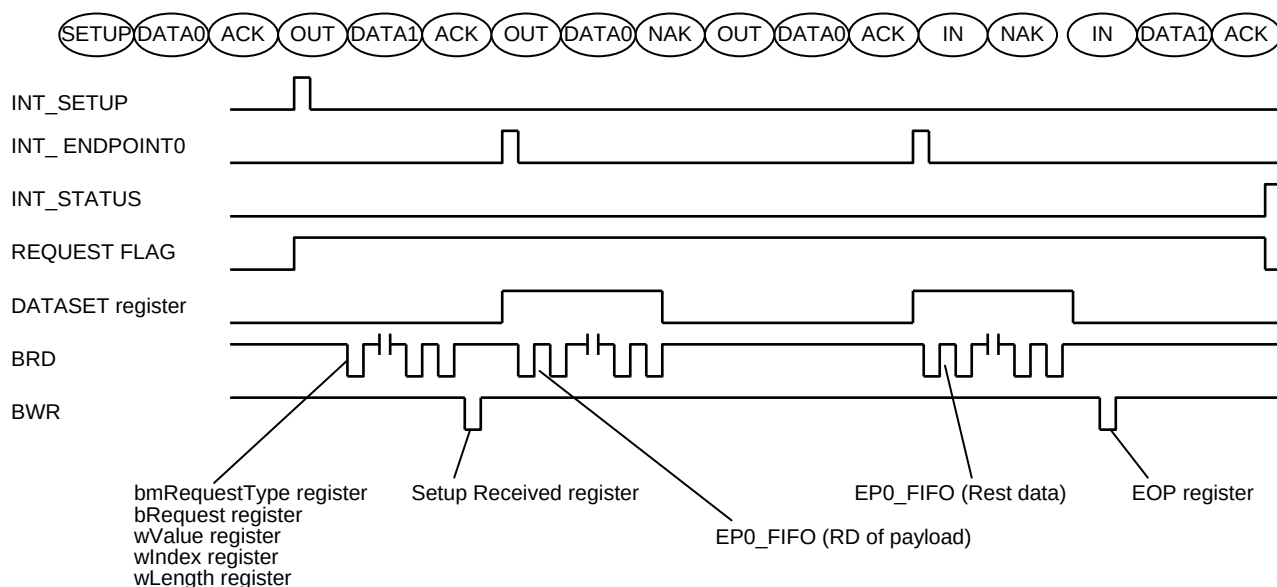


Figure 3.16.7 The Control Flow in UDC (Control Write Transfer Type)

In control read transfer type, transaction number of data stage does not always correspond with the data number specified by the device request. The CPU can therefore process using INT\_STATUSNAK interrupt. However, when class and vendor request is used, wLength value corresponds to data transfer number in data phase. With this setting, using this interrupt is not need. Data stage data can be confirmed by accessing DATASIZE register.

Stage change condition of control write (no data stage) transfer type

1. Receive SETUP token from host
  - Start setup stage in the UDC.
  - Receive data in request normally and judge. And assert INT\_SETUP interrupt externally.
  - Change data stage in the UDC.
2. Receive IN token from host
  - CPU receives a request from the request register every INT\_SETUP interrupt.
  - Judge request and access Setup Received register to inform the UDC that INT\_SETUP interrupt has been recognized.
  - The CPU processes receiving data by device request.
  - When the CPU finishes transaction, it writes “0” to EP0 bit of EOP register.
  - Change status stage in the UDC.
  - Return data packet of 0 data to IN token, and change state to IDLE in the UDC.
  - Assert INT\_STATUS interrupt externally when ACK for 0 data packet is received.

These change condition is Figure 3.16.8.

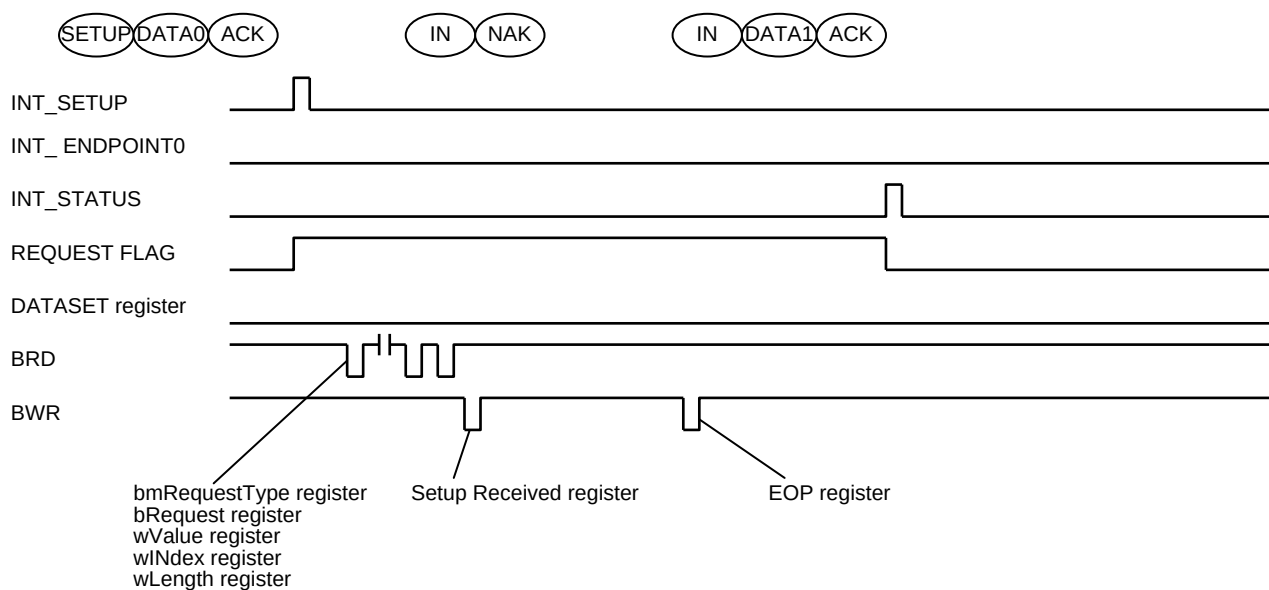


Figure 3.16.8 The Control Flow in UDC (Control Write Transfer Type not Dataphase)

## (d) Isochronous transfer type

Isochronous transfer type is guaranteed transfer by data number that is limited to each frame.

However, this transfer does not retry when an error occurs. Therefore, Isochronous transfer type transfer only 2 phases (token, data) and it does not use handshake phase. And data PID for data phase is always DATA0 because of this transaction does not support toggle sequence. Therefore, UDC does not confirm when data PID is in receiving mode.

Isochronous transfer type processes data every frame. Therefore, all transaction for completed transfer use receiving SOF token. The UDC uses FIFO that is divided into two in Isochronous transfer type.

## (d-1) Isochronous transmission mode

The transaction format for Isochronous transfer type format in transmitting is given below.

- Token : IN
- Data : DATA0

Control flow

Isochronous transfer type is frame management. And data that is written to FIFO in endpoint is transmitted by IN token in the next frame.

Below are two conditions in FIFO of Isochronous transmission mode transferring.

- X. FIFO for storing data that transmits to host in present frame  
(DATASET register bit = 1)
- Y. FIFO for storing data for transmitting host in next frame  
(DATASET register bit = 0)

FIFO that is divided into two (packet A and packet B) conditions is whether X condition or Y condition. The flow below is explained as X Condition (packet A), Y Condition (packet B) in present frame.

X and Y conditions change one after the other by receiving SOF.

Control flow in the UDC when receiving IN token is shown below.

1. Token packet is received and address endpoint number error is confirmed, and it checks whether the relevant endpoint transfer mode corresponds with the IN token. If it does not correspond, the state returns to IDLE.
2. Condition of status register is confirmed.  
INVALID condition: State returns to IDLE.
3. Data packet is generated.  
Data packet is generated. At this point, data PID is always attached to DATA0. Next, data is transferred from FIFO (X condition) of packet A in UDC to SIE and DATA packet is generated.
4. CRC bit (counted transfer data of FIFO from first to last) is attached to last.

5. Below is transaction when SOF token is received from host.

- Change the packet A's FIFO from X Condition to Y Condition and clear data.
- Change the packet B from Y Condition to X Condition.
- Set frame number to frame register.
- Assert SOF and inform externally that frame is incremented.
- DATASET register clears packet A bit and it sets packet B bit arrangement loading in present frame.
- Set STATUS to READY.

The UDC finishes normally by above transaction.

Packet A's FIFO can be received with next data.

In renewed frame, Packet A's FIFO interchanges with packet B's FIFO, and transaction uses same flow.

If SOF token is not received by error and so on, this data is lost because frame is not renewed. There is no problem in receiving PID if frame data is received with CRC error, USB sets LOST to STATUS on FRAME register, and exact frame number is unknown. However, in this case, SOF is asserted and FIFO condition is renewed. If SOF token is received without transmit and transfer Isochronous in frame, UDC clears FIFO (X Condition) and sets STATUS to FULL.

Note : EPx\_DATASETA,B change at 3 clocks of 12MHz after receiving SOF. Write data to FIFO after EPx\_DATASETA,B are changing.

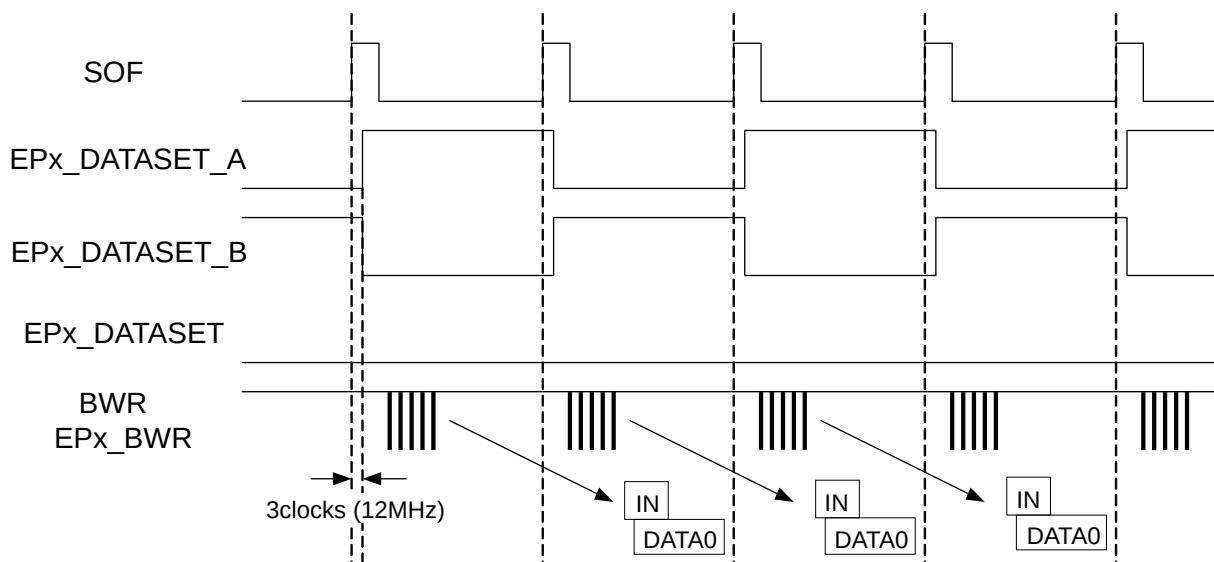


Figure 3.16.9 Isochronous transfer Mode

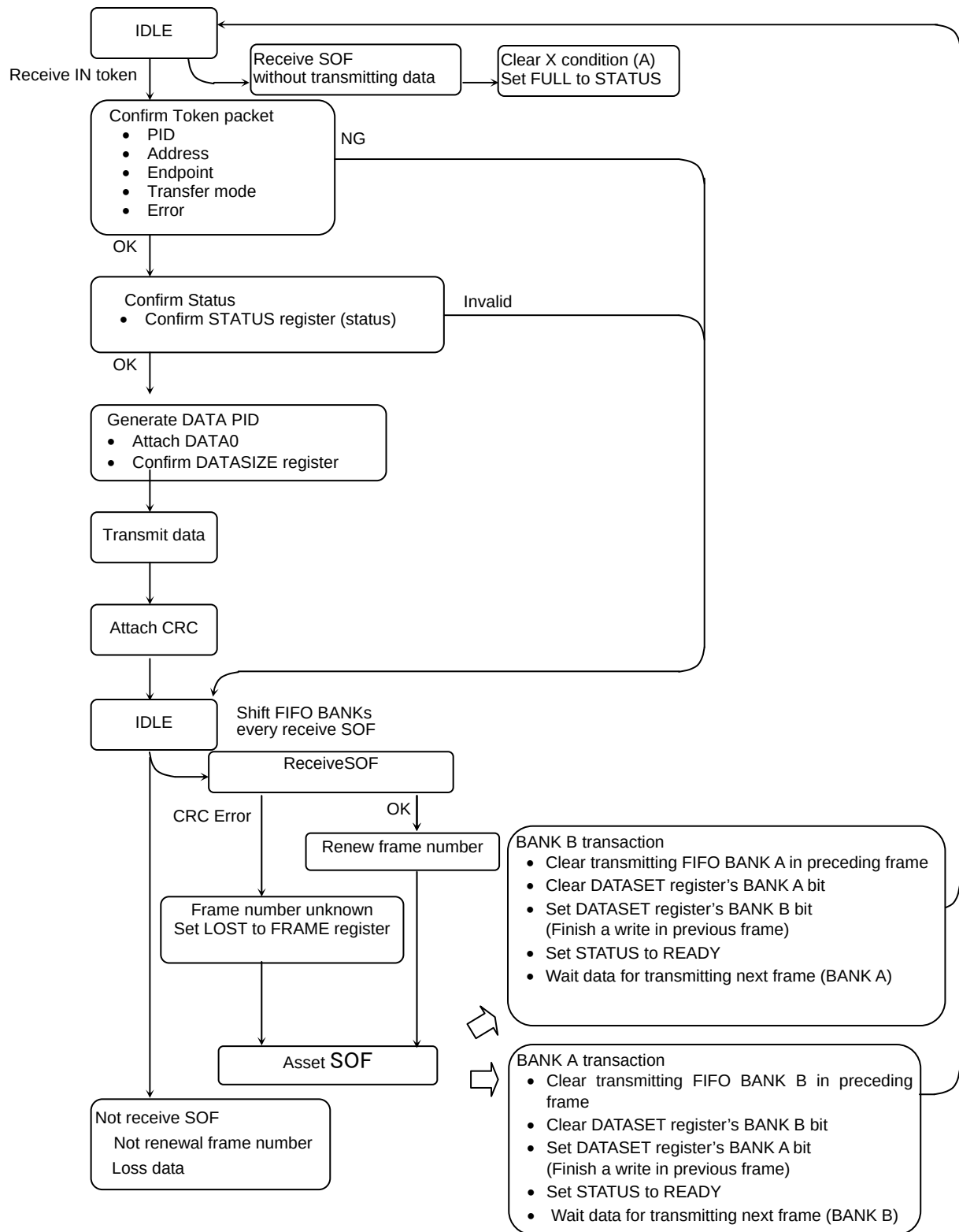


Figure 3.16.10 Control Flow in UDC (Isochronous transfer type (Transmission))

## (d-2) Isochronous receiving mode

Transaction format for Isochronous transfer type in receiving is given below.

- Token :OUT
- Data : DATA0

Control flow

Isochronous transfer type is frame management. And data that is written to FIFO by OUT token is received to the CPU in the next frame.

Below are two conditions in FIFO of Isochronous receiving mode transferring

X. FIFO for storing data received from host in present frame

(DATASET register bit = 0)

Y. FIFO for storing data for transmitting host in previous frame

(DATASET register bit = 1)

FIFO that is divided into two (packet A and packet B) conditions is whether X condition or Y condition. The flow below explains X Condition (packet A) and Y Condition (packet B) in present frame.

X and Y conditions change one after the other by receiving SOF.

Below is control flow in the UDC when receiving OUT token.

The whole transaction is processed by hardware.

1. Token packet is received and address endpoint number error is confirmed, and it checks whether the relevant endpoint transfer mode corresponds with the OUT token. If it does not correspond, the state returns to IDLE.
2. Condition of status register is confirmed.
  - INVALID condition: State return to IDLE.
3. Data packet is received.
 

Data is transferred from SIE into the UDC to packet A's FIFO (X Condition).
4. After last data has been transferred, and counted CRC is compared with transferred CRC. When transfer is finished, the result is reflected to STATUS. However, data is stored FIFO, data number that packet A is received is set to DATASIZE register of packet A.
5. The transaction when SOF token from host is received is given below.
  - Change packet A's FIFO from X Condition to Y Condition.
  - Change packet B from Y Condition to X Condition, and clear data. Prepare for next transfer.
  - Set frame number to frame register.
  - Assert SOF and inform externally that frame is incremented.
  - DATASET register set packet A bit and clear packet B bit arrangement loading in present frame.
  - If CRC comparison result agrees it, DATAIN is set to STATUS. If result does not agree, RX\_ERR is set to STATUS.

The UDC finishes normally by the above transaction.

The CPU takes back packet A's data.

In renewed frame, Packet A's FIFO interchanges with packet B's FIFO, and the transaction uses the same flow.

If SOF token is not received by error and so on, this data is lost because the frame is not renewed. There is no problem in receiving PID and if frame data is received with CRC error, USB sets LOST to STATUS on FRAME register, and exact frame number is unknown. However, in this case, SOF is asserted and FIFO condition is renewed. If SOF token is received without transmit and transfer Isochronous in frame, UDC clears FIFO (X Condition) and sets STATUS to FULL.

These are shown in Figure 3.16.12.

Note : EPx\_DATASET changes at 2 clocks of 12MHz after receiving SOF. Read data from FIFO after EPx\_DATASET is rising.

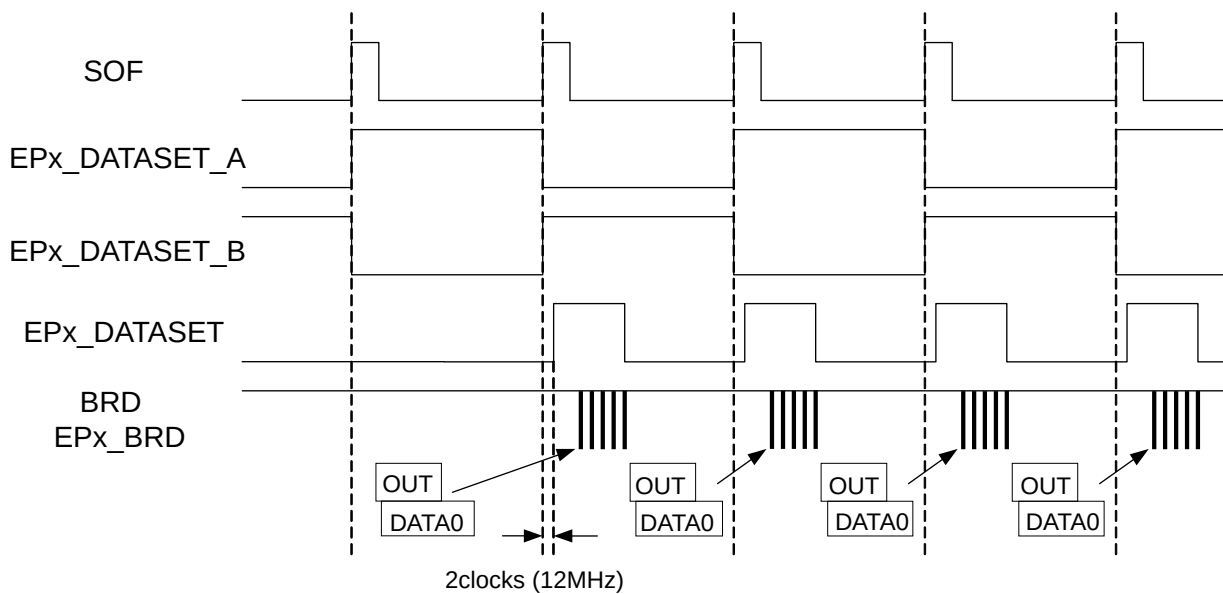


Figure 3.16.11 Isochronous Receiving mode



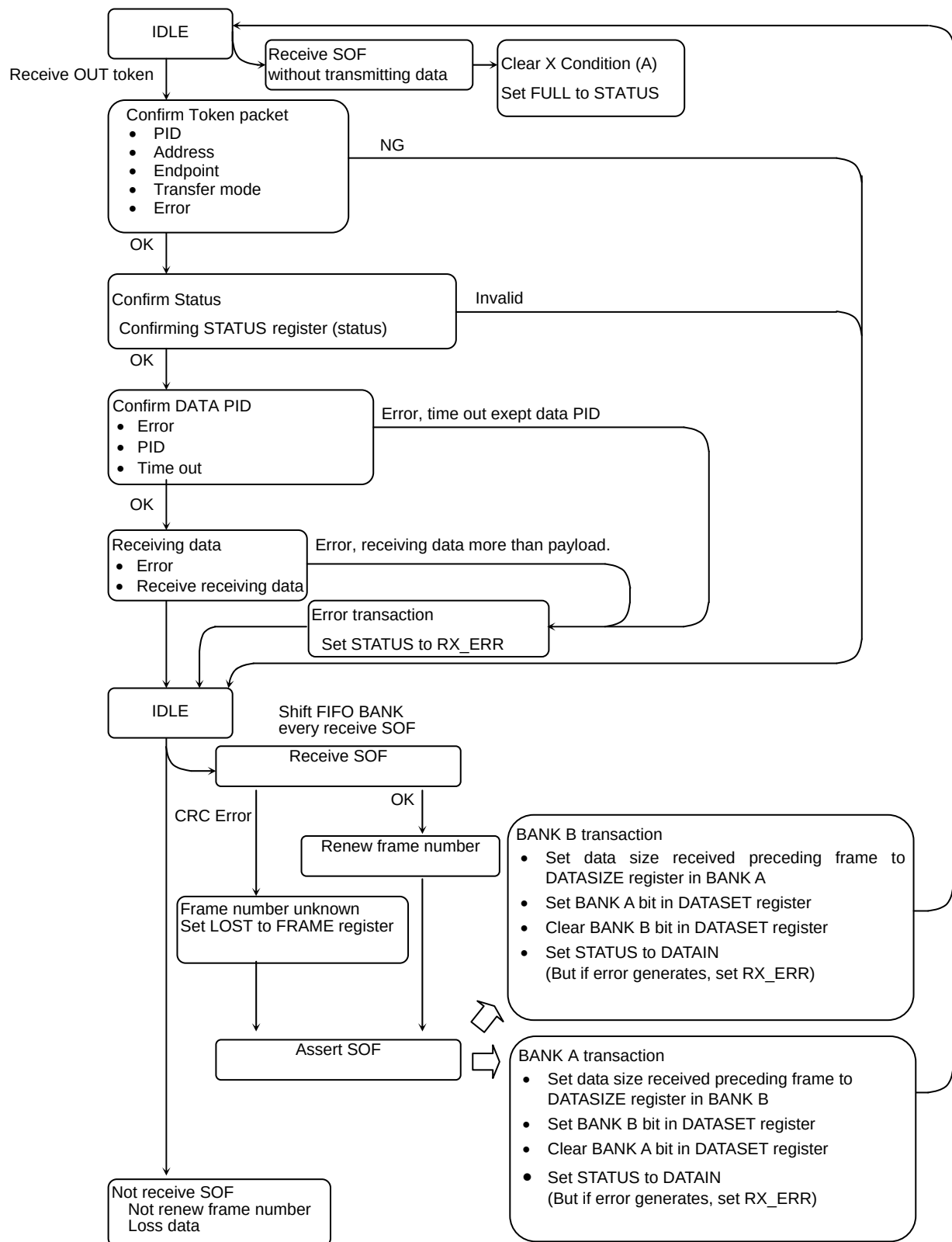


Figure 3.16.12 Control Flow in UDC (Isochronous transfer type (Receiving))

### 3.16.7 Bus Interface and Access to FIFO

#### (1) CPU bus interface

The UDC prepares two types of FIFO access, single packet and dual packet. In single packet mode, FIFO capacity that is implemented by hardware is used as large FIFO. In dual packet mode, FIFO capacity is divided into two and used as two FIFOs. It is also used as an independent FIFO. Even if the UDC is transmitting and receiving to USB host, it can be used as an efficient bus by possible load to FIFO.

But control transfer type receives only single packet mode.

Epx\_SINGLE signal in dual packet mode must be fixed to "0". If this signal is fixed to "0", FIFO register runs in single mode.

Sample: Where endpoint 1 is used to dual packet of payload 64 bytes.

|                        |   |                   |
|------------------------|---|-------------------|
| EP1_FIFO size          | : | Prepare 128 bytes |
| EP1_SINGLE signal      | : | Hold 0            |
| EP1 Descriptor setting |   |                   |
| Direction              | : | Optional          |
| Max payload size       | : | 64 bytes          |
| Transfer mode          | : | Optional          |

## (a) Single packet mode

This is data sequence of single packet mode when CPU bus interface is used. Figure 3.16.13 is receiving sequence. Figure 3.16.14 is transmitting sequence. This chapter focuses on access to FIFO. For Data sequence with USB host refer to chapter 5.

Endpoint 0 cannot be changed to exclusive single packet mode. Endpoints 1 to 3 can be changed between single packet and dual packet by setting Epx\_SINGLE register. Do not change packet when transferring.

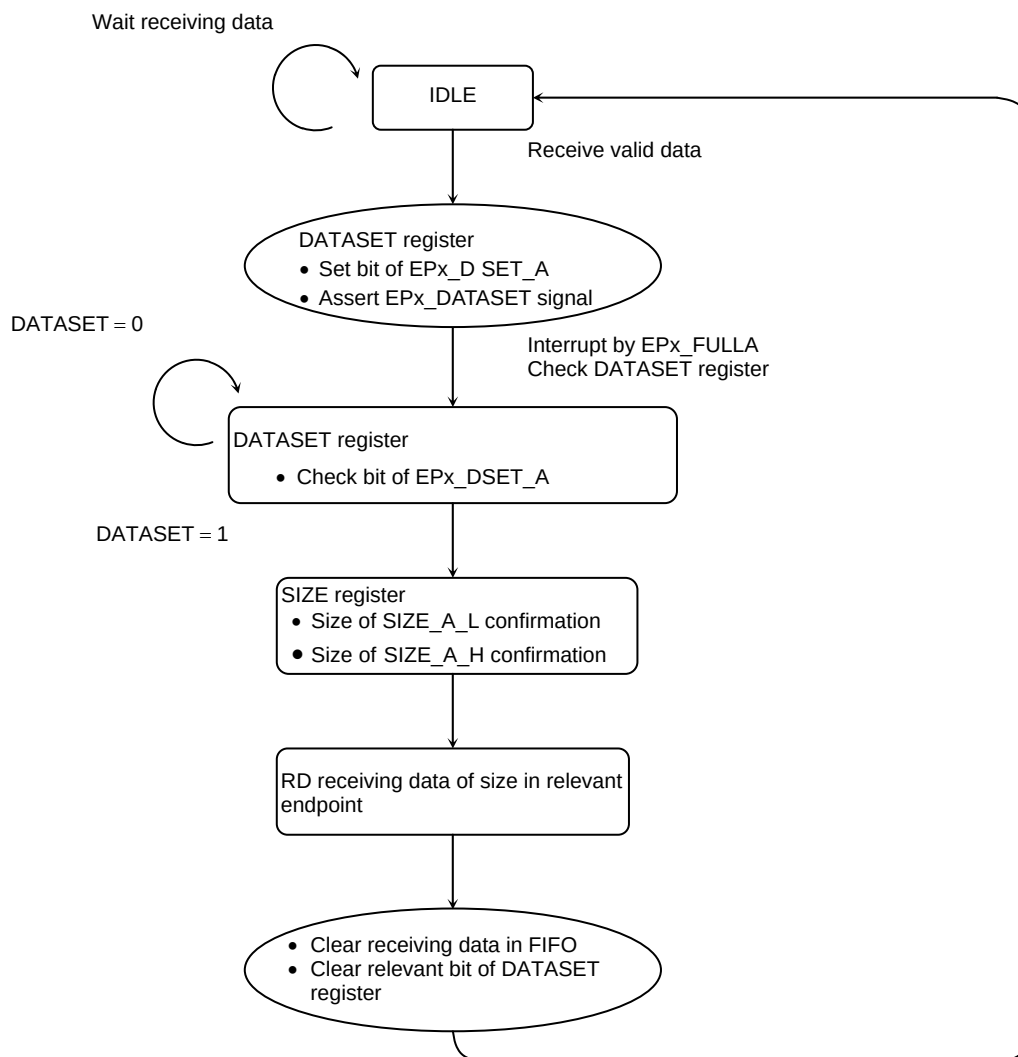
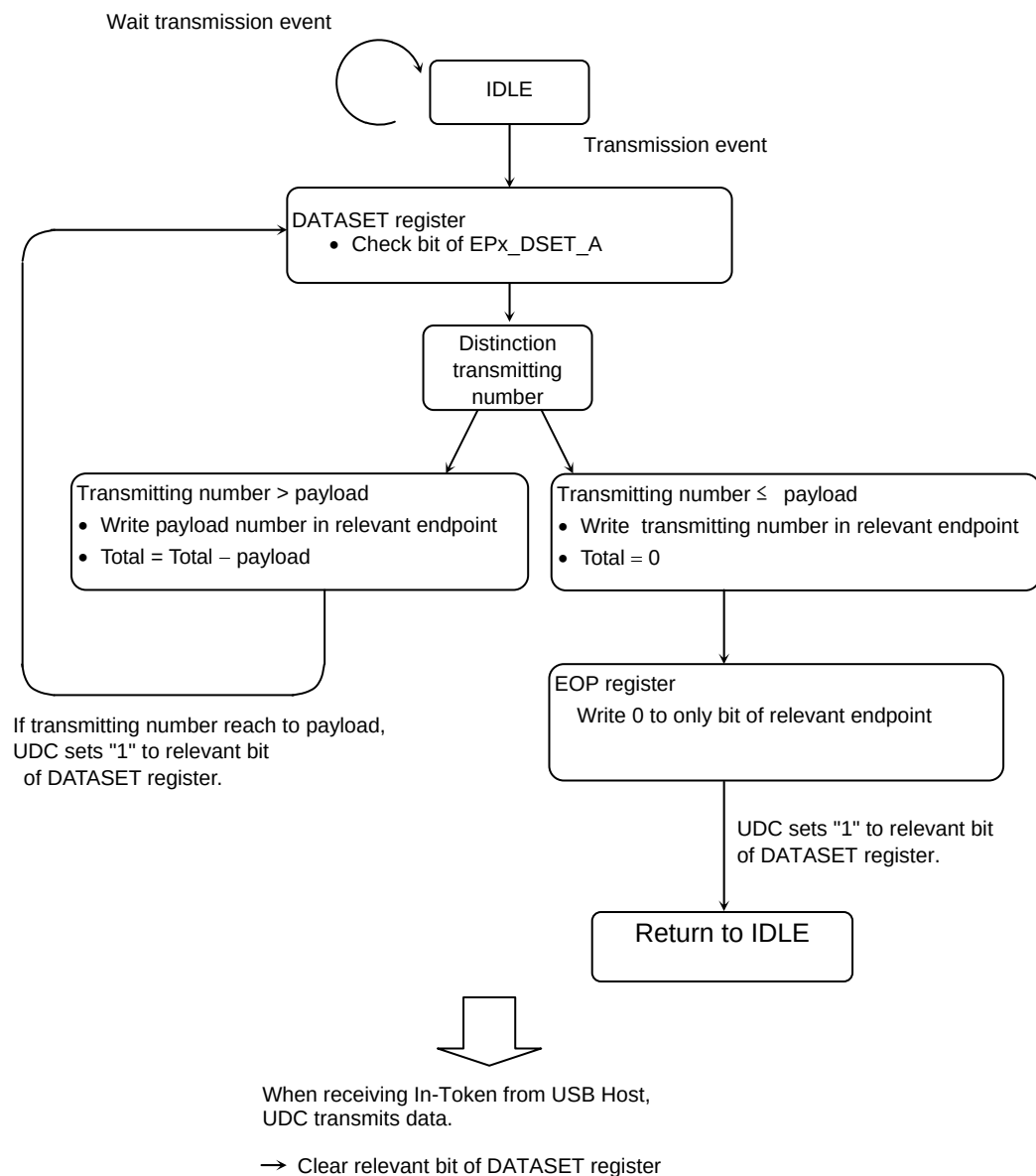


Figure 3.16.13 Receiving Sequence in Single Packet Mode

Below is the transmitting sequence in single packet mode.



- Accessing to EOP register is needed in transmitting short packet.
- Accessing endpoint0 is used for showing closing control transfer. Therefore, always access to endpoint 0 in closing control transfer whether short packet or not.

Figure 3.16.14 Transmitting Sequence in Single Packet Mode

## (b) Dual packet mode

In dual packet mode, FIFO is divided into A and B packet, and is controlled according to priority in hardware. It can be performed at once, transmitting and receiving data to USB host and exchanges to external of UDC.

When it reads out data from FIFO for receiving, confirm condition of two packets, and consider the order of priority. If it has received data to two packets, the UDC outputs from first receiving data by FIFO that can be accessed are common in two packets. EPx\_SIZE register is prepared for both packet A and packet B. First, the CPU must recognize the data number of first receiving packet by PKT\_ACTIVE bit. If PKT\_ACTIVE bit has been set to 1, that packet is received first. Packet A and packet B set data turn about always.

This is shown below.

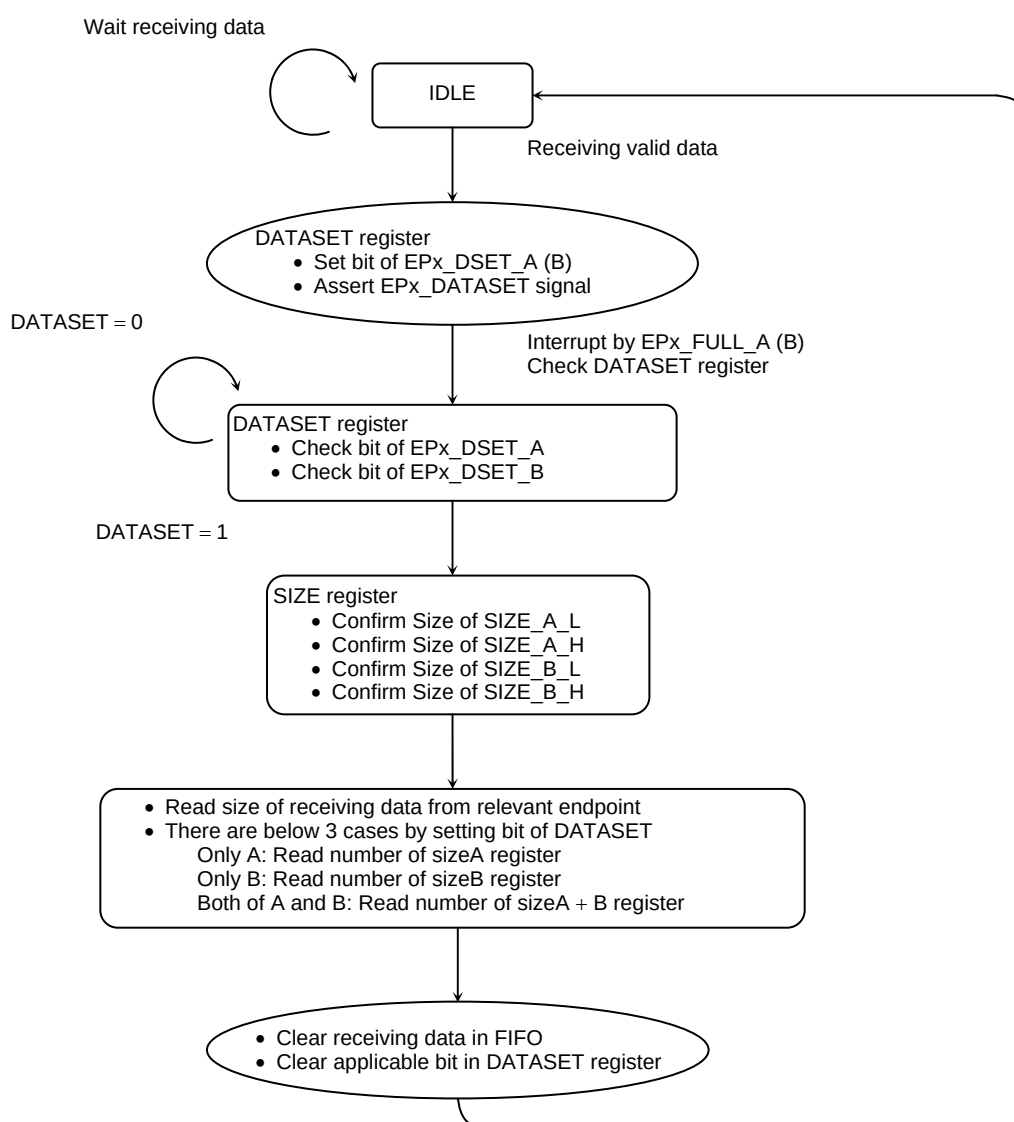
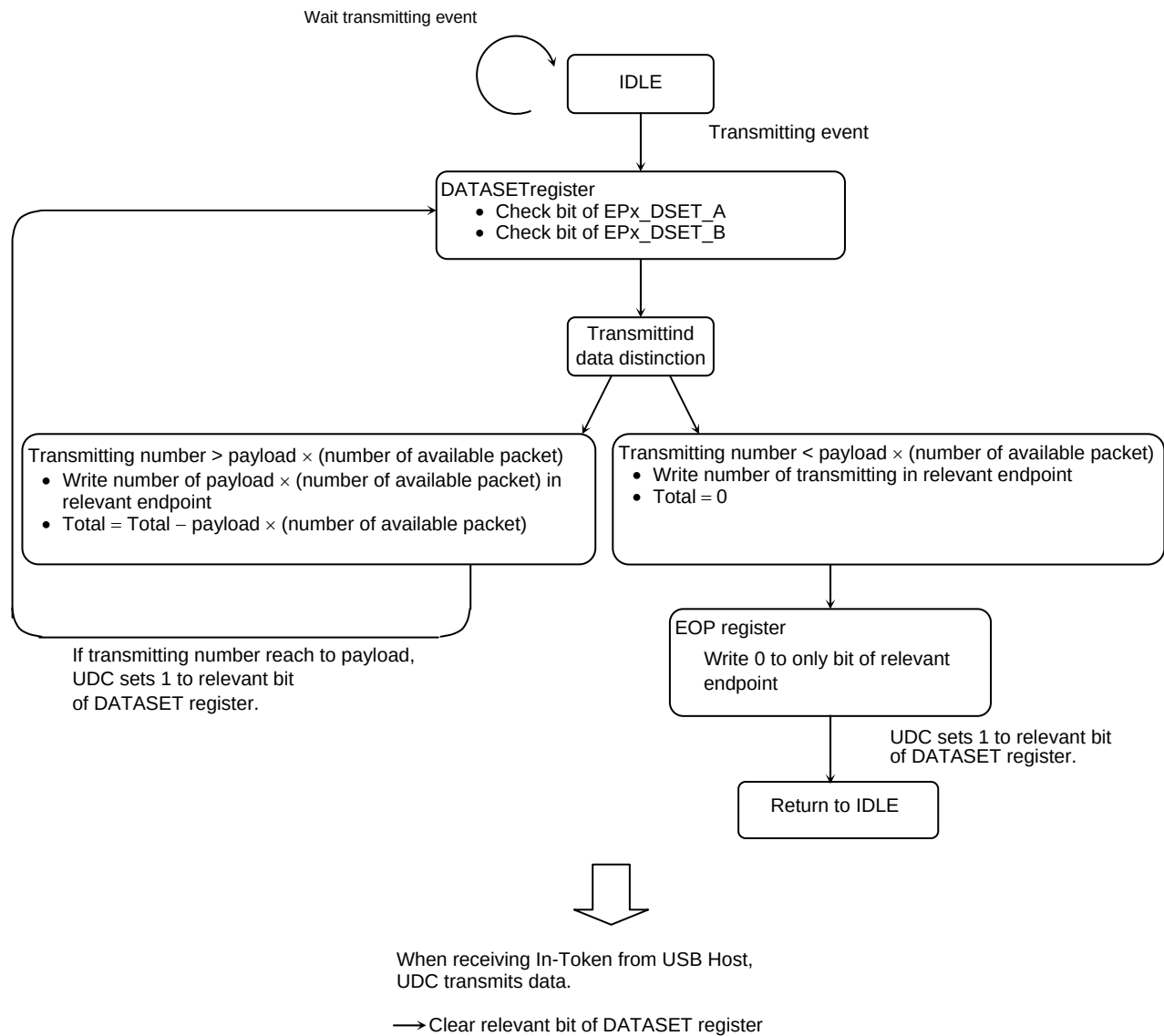


Figure 3.16.15 Receiving Sequence in Dual Packet Mode

Data can be set to available FIFO when transmitting regardless of packet A or B.  
Below is the Transmitting Sequence in Dual Packet Mode.



- Accessing to EOP register is needed in transmitting short packet.
- Control transfer type is supported in only single mode.

Figure 3.16.16 Transmitting Sequence in Dual Packet Mode

## (c) Issuance of NULL packet

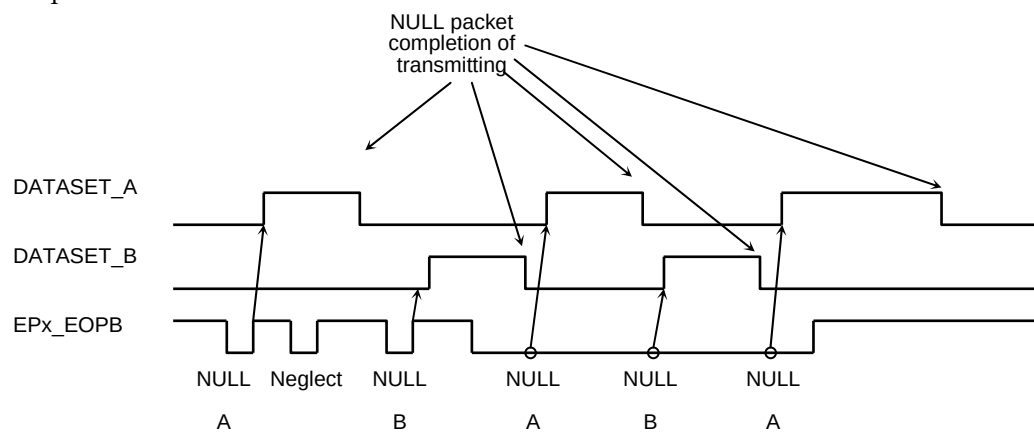
If transmitting NULL packet, by input L pulse from EPx\_EOPB signal, data of 0 length is set to FIFO, and NULL packet can be transferred to IN token.

But if NULL data is set to FIFO, it is valid only in the case whole SET signal is L level condition (where FIFO is empty). If it answers to receiving IN token by using NULL packet in a certain period, it is answered by keeping EPx\_EOPB signal to L level.

However, if mode is dual packet mode, EPx\_DATASET signal assert L level for showing space of data. Therefore, data condition (whether either has data or not) cannot be confirmed externally.

Note: NULL packet can also be set by accessing EOP register.

Example:



## (2) Interrupt control

Interrupt signal is prepared. This function use adept system.

For detail refer to 3.16.2 900/H1 CPU I/F.

### 3.16.8 USB Device answer

The USB controller (UDC) sets various register and initialization in the UDC in detecting of hardware reset, detecting of USB bus reset, and enumeration answer.

Each condition is explained below.

#### (1) bus reset detect condition.

When the UDC detects a bus reset on the USB signal line, it initializes internal register, and it prepares enumeration operation from USB host. After detecting a USB reset, the UDC sets ENDPOINT0 to control transfer type 8-byte payload and default address for using default pipe. Any endpoint other than this is prohibited.

| Register name   |                | Initial value |
|-----------------|----------------|---------------|
| ENDPOINT STATUS | EP0            | 00H           |
|                 | Except for EP0 | 1CH           |

#### (2) Detail of STATUS register

Status register that has been prepared for each endpoint shows the condition of each endpoint in the UDC.

Each condition affects the various USB transfers. Refer to chapter 5 for the changing conditions for each transfer type.

EPx\_STATUS register value is 0 to 3, and its shows conditions are shown. 0 to 4 are the results of various transfers. It can be confirmed previous result that is transferred to endpoint by confirming from external of UDC.

|   |        |
|---|--------|
| 0 | READY  |
| 1 | DATAIN |
| 2 | FULL   |
| 3 | TX_ERR |
| 4 | RX_ERR |

These conditions mean that the endpoint is operating normally. The meaning that is showed is different for each transfer mode. Therefore, please refer to each transfer mode column below.



## ISO transfer mode

Below is the transfer condition for the previous frame. Receiving SOF renews this.

|                 | OUT (RX) | IN (TX) |
|-----------------|----------|---------|
| Initial         | READY    | READY   |
| Not transfer    | READY    | FULL    |
| Finish normally | DATAIN   | READY   |
| Detect an error | RXERR    | TXERR   |

## Transfer modes other than ISO transfer

This is the result of the previous transfer. When transfer is finished, this is renewed.

|                          | OUT, SETUP | IN    |
|--------------------------|------------|-------|
| Initial                  | READY      | READY |
| Transfer finish normally | DATAIN     | READY |
| Status stage finish      | READY      | READY |
| Transfer error           | RXERR      | TXERR |

“Initial” is that renew RESET, USB reset, Current\_Config register. In detect error, it does not generate EPx\_DATASET except in toggle transfer mode and Isochronous transfer mode of interrupt.

5 to 7 in shows the status register means that the endpoint is in special condition.

- |   |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|---|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5 | BUSY    | BUSY is generated only at endpoint of control transfer. If UDC transfer in control writes transfer, when CPU has not finished enumeration transaction, and if it receives ID of status stage from USB host, BUSY is set. STATUS is BUSY until CPU finishes enumeration transaction and EP0 bit of EOP register is written 0 in UDC. If CPU enumeration transaction finishes and EP0 bit of EOP register is written 0 and status stage from USB host finishes normally, it displays READY.      |
| 6 | STALL   | STALL shows that endpoint is in STALL condition.<br>This condition is generated if it violates protocol or error in bus enumeration. To return endpoint to normal transfer condition, USB device request is needed. This request returns to normal condition. But control endpoint returns to normal condition by receiving SETUP token. And it becomes to SETUP stage.                                                                                                                        |
| 7 | INVALID | This condition shows condition that endpoint cannot be used. UDC sets condition that isn't designated in ENDPOINT to INVALID condition, and it ignores all tokens for this endpoint. In initializing, this condition is always generated. When UDC detects hardware reset, it sets all endpoints to INVALID condition. Next, if USB reset is received, endpoint 0 only is renewed to READY. Other endpoints that are defined on disruptor are renewed if SET_CONFIG request finishes normally. |

### 3.16.9 Power Management

USB controller (UDC) can be switched from optional resume condition (turn on the power supply condition) to suspend (Suspension) condition, and it can be returned from suspend condition to turn on the power supply condition.

This function can be set to low electricity consumption by operating CLK supplying for UDC.

#### (1) Switch to suspend condition

The USB host can set the USB device to suspend condition by maintaining IDLE state. The UDC switches to suspend condition by the following process.

- UDC switches to suspend condition if it detects IDLE state of more than 3 ms (about 3.07ms) on USB signal. At this point, UDC sets SUSPEND bit of STATUS register to “1”.
- UDC renews USBINTFR1<INT\_SUS> and <INT\_CLKSTOP> from “0” to “1” if it detects IDLE state of more than 5 ms (about 5.46ms) on USB signal. Afterward reset USBCR1<USBCLKE> to “0” to stop USB clock.
- In this condition, all register values into the UDC are kept. However, external access is not possible except for reading of STATUS register, Current\_Config register, and USBINTFR1, USBINTFR2, USBINTMR1, USBINTMR2 and USBCR1.

#### (2) Return from suspend condition by host resume

When activity of bus on USB signal is restored by resume condition output from USB host, the UDC releases SUSPEND condition, and it resets SUSPEND bit of STATUS register to “0”. The system is thereby resumed. The resume condition output from the host is maintained for at least 20 ms. Therefore effective protocol occurs on USB signal line after this time has elapsed.

#### (3) Return from suspend condition by remote wakeup

Remote wakeup is system for prompt resume from suspended USB device to USB host. Some applications do not support remote wakeup. Remote wakeup is also limited using from USB host by bus enumeration.

UDC remote wakeup function can be used when it is permitted.

Setting remote wakeup by bus can be confirmed by bit7 of Current\_Config register. When this bit is “1”, remote wakeup can be used. Remote wakeup is not disabled by this bit. Therefore, if this bit shows disabled, remote wakeup must not be set. If it fill the conditions, output resume condition output to USB host by writing USBCR1<WAKEUP> from “1” to “0” of UDC in suspend condition. And it prompts resume from UDC to host. After UDC changes to suspend condition, WAKEUP input is ignored for 2 ms. Therefore, remote wakeup becomes effective when USBINTFR1<INT\_SUS> is set to “1”.

(4) Low power consumption by control of CLK input signal

When the UDC switches to suspend condition, it stops CLK and switches to low power consumption condition. But as system, this function enables low power consumption by stopping source of CLK. CLK that is supplied to the UDC can be controlled by using USBINTFR1<INT\_SUS>, <INT\_CLKSTOP> and USBCR1<USBCLKE>.

If UDC switches to suspend condition, USBINTFR1<INT\_SUS> is set to “1”, and <INT\_CLKSTOP> is set to “1”. After confirmation, stop CLK supply (USBCLK) by setting “0” to USBCR1<USBCLKE>. If SUSPEND condition is released by resuming from host, supply normal CLK to UDC within 3 ms.

When remote wakeup is used, it is necessary to supply a stable CLK to the UDC before use. When doubler circuit is used as generation source, the above control is needed.

- Return from suspend condition by USB reset (by INT\_CLKON interrupt)

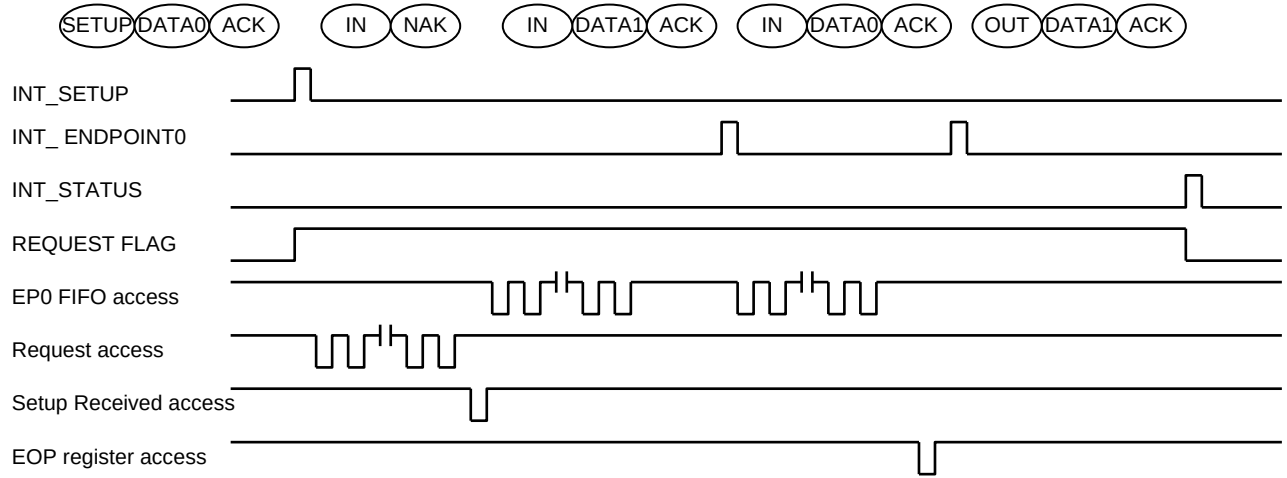
When UDC stops CLK in suspend condition, UDC can not detect USB reset and control CLK in suspend condition as above mentioned.

In case CLK is stopped in suspend condition, UDC can detect USB reset and return from suspend condition by supplying CLK (USBCR1<USBCLKE>=1) after detecting INT\_CLKON interrupt.

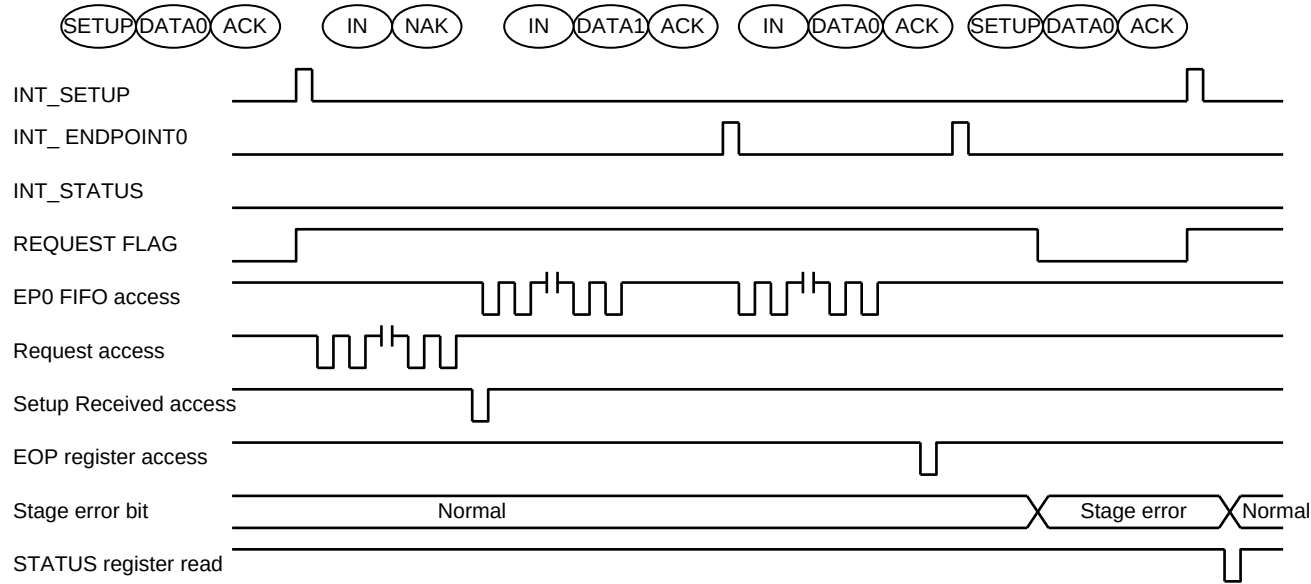
3.16.10 Supplement

(1) External access flow to USB communication

a) Normal movement



b) Stage error



## (2) Register Initial value

| Register Name         | Initial Value<br>OUTSIDE Reset | Initial Value<br>USB_RESET | Register Name | Initial Value<br>OUTSIDE Reset | Initial Value<br>USB_RESET |
|-----------------------|--------------------------------|----------------------------|---------------|--------------------------------|----------------------------|
| bmRequestType         | 0x00                           | 0x00                       | INT control   | 0x00                           | 0x00                       |
| bRequest              | 0x00                           | 0x00                       | USBUFF_TEST   | 0x00                           | Hold                       |
| wValue_L              | 0x00                           | 0x00                       | USB state     | 0x01                           | 0x01                       |
| wValue_H              | 0x00                           | 0x00                       | EPx_MODE      | 0x00                           | 0x00                       |
| wIndex_L              | 0x00                           | 0x00                       | EPx_STATUS    | 0x1C                           | 0x1C                       |
| wIndex_H              | 0x00                           | 0x00                       | EPx_SIZE_L_A  | 0x88                           | 0x88                       |
| wLength_L             | 0x00                           | 0x00                       | EPx_SIZE_L_B  | 0x08                           | 0x08                       |
| wLength_H             | 0x00                           | 0x00                       | EPx_SIZE_H_A  | 0x00                           | 0x00                       |
| Current_Config        | 0x00                           | 0x00                       | EPx_SIZE_H_B  | 0x00                           | 0x00                       |
| Standard request      | 0x00                           | 0x00                       | FRAME_L       | 0x00                           | 0x00                       |
| Request               | 0x00                           | 0x00                       | FRAME_H       | 0x02                           | 0x02                       |
| DATASET               | 0x00                           | 0x00                       | ADRESS        | 0x00                           | 0x00                       |
| Port Status           | 0x18                           | Hold                       | EPx_SINGLE    | 0x00                           | Hold                       |
| Standard request mode | 0x00                           | Hold                       | EPx_BCS       | 0x00                           | Hold                       |
| Request mode          | 0x00                           | Hold                       | ID_STATE      | 0x01                           | 0x00                       |

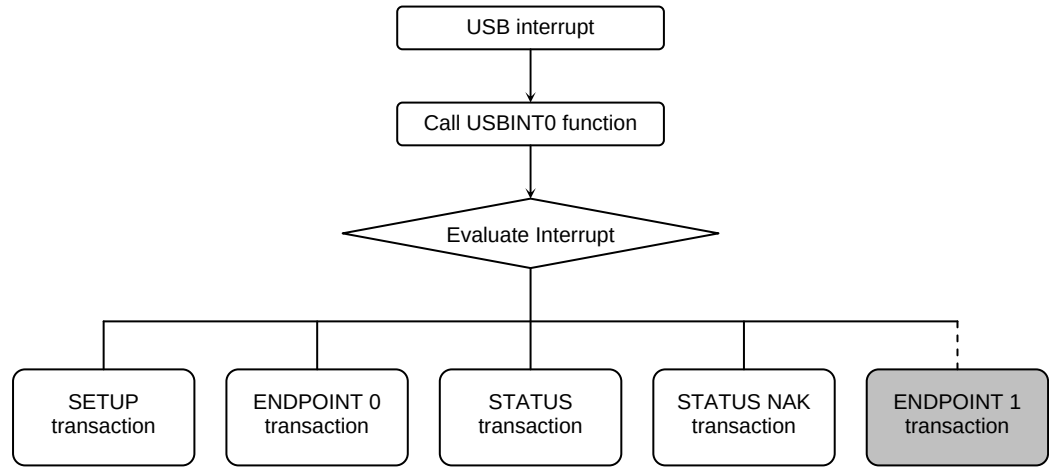
Note 1: The above initial value is the value that is initialized by external reset, USB\_RESET. This value may differ from that displayed depending on conditions.

Please refer to register configure in chapter 2.

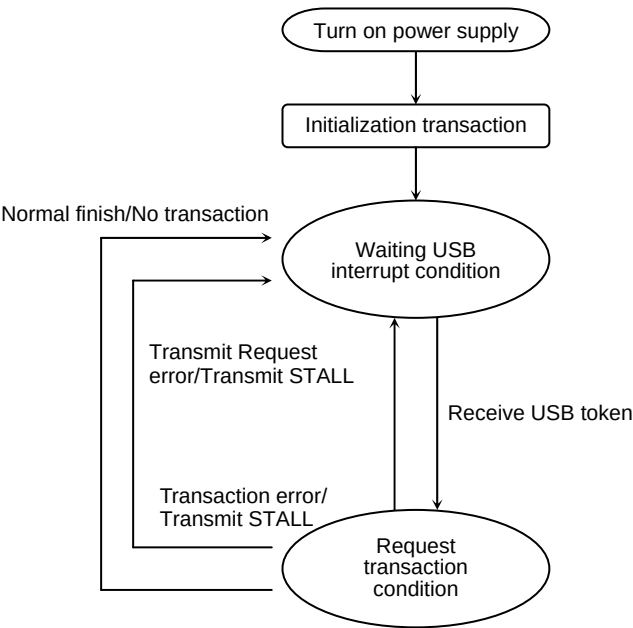
Note 2: EP0\_STATUS register is initialized to 0x00 after USB\_RESET is received.

Note 3: Initial value of ID\_STATE register is initialized by external reset, BRESET. When USB\_RESET signal is received from host, it is initialized to 0x00.

- (3) USB control flow chart
- (a) Transaction for standard request (Outline flowchart (Example))

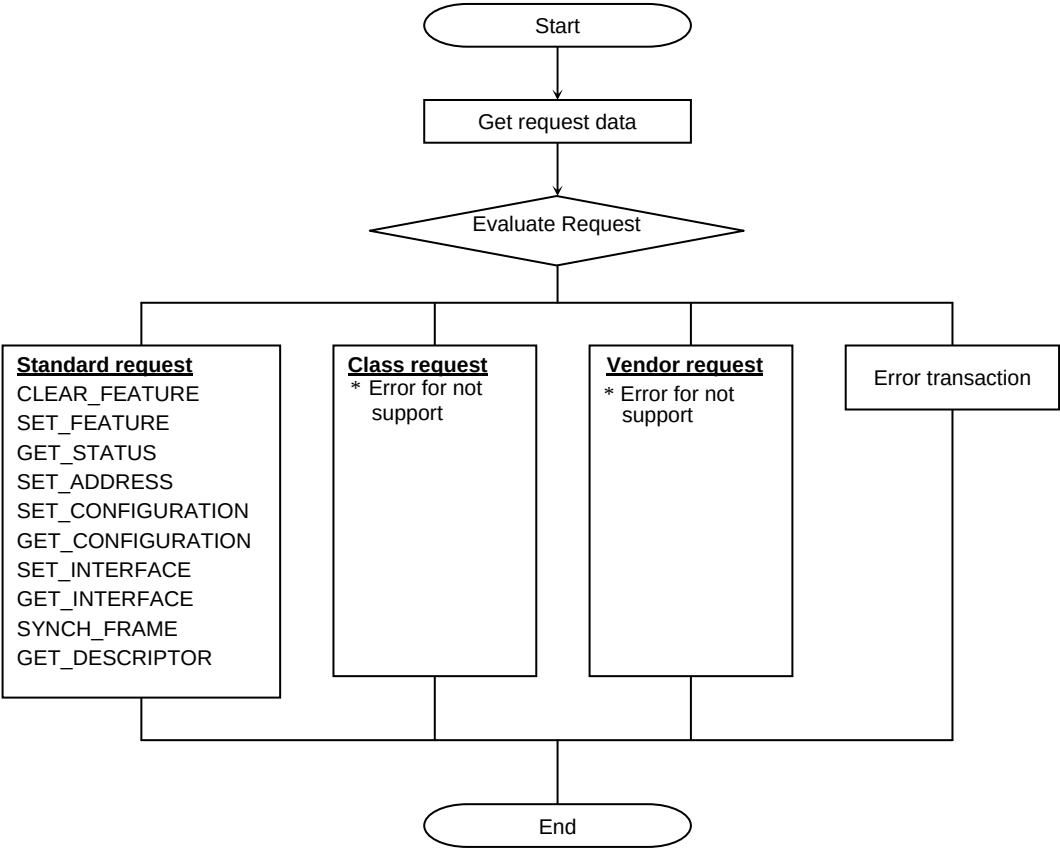


(b) Condition change

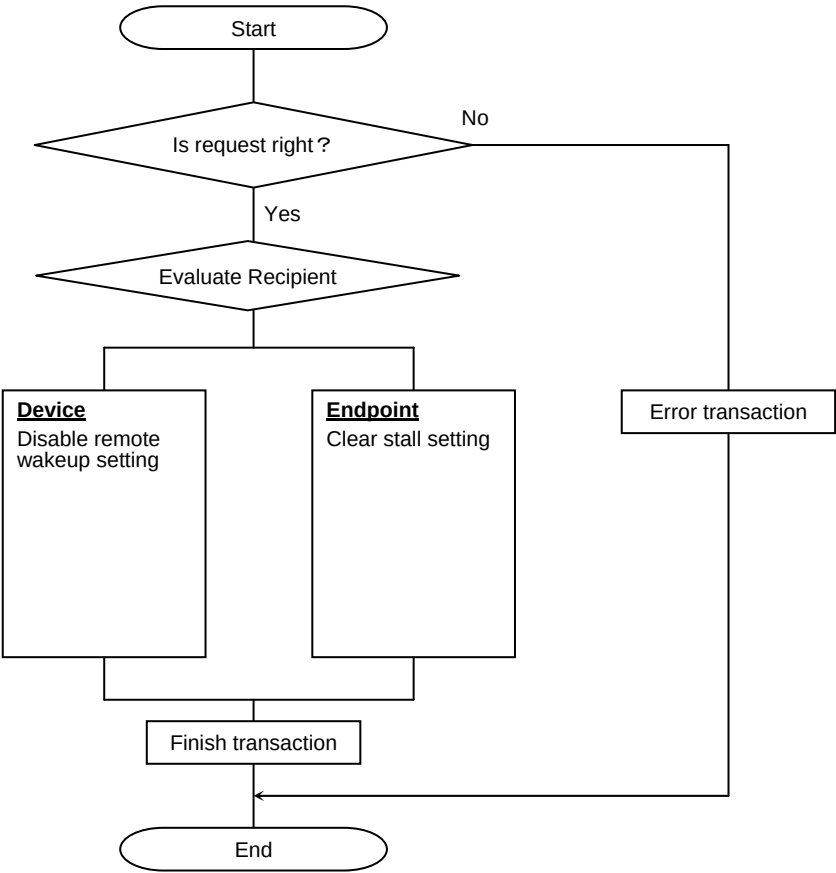




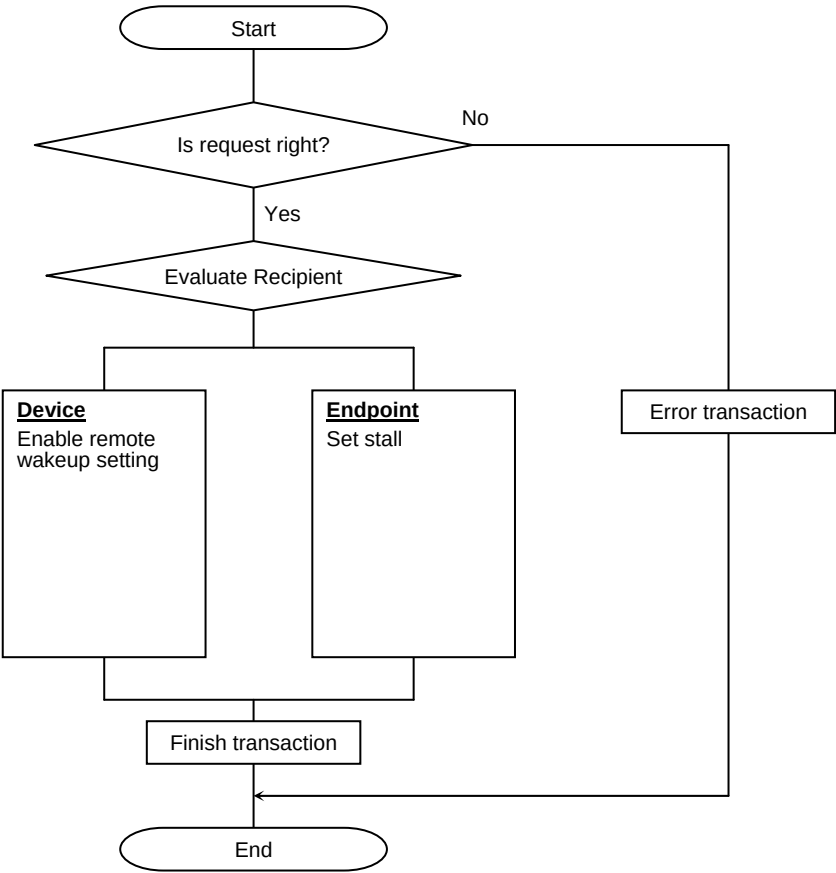
(c) Device request and evaluation of various requests



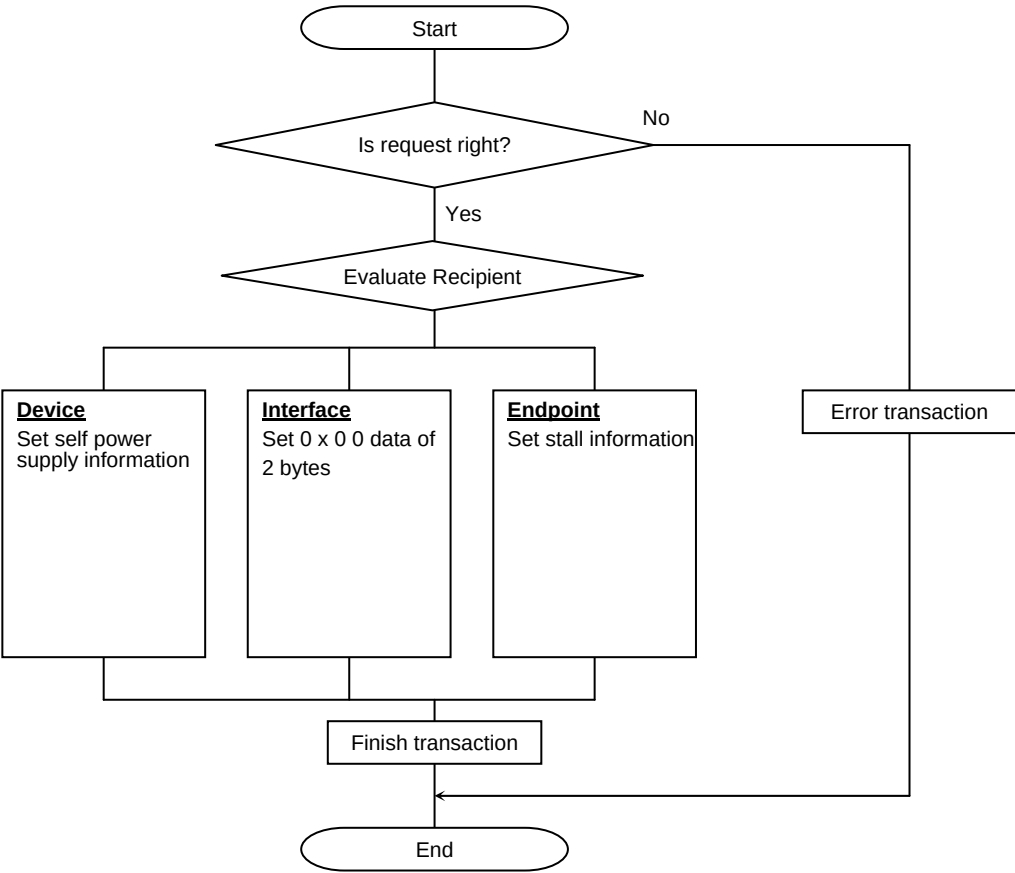
(c-1) CLEAR\_FEATURE request transaction



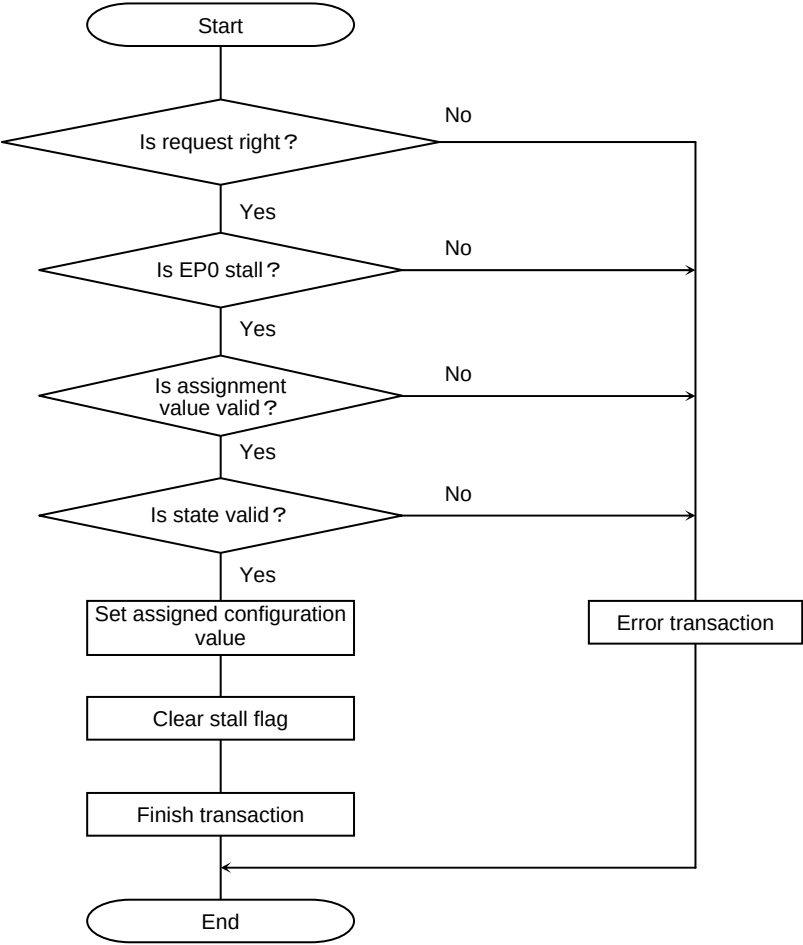
(c-2) SET\_FEATURE request transaction



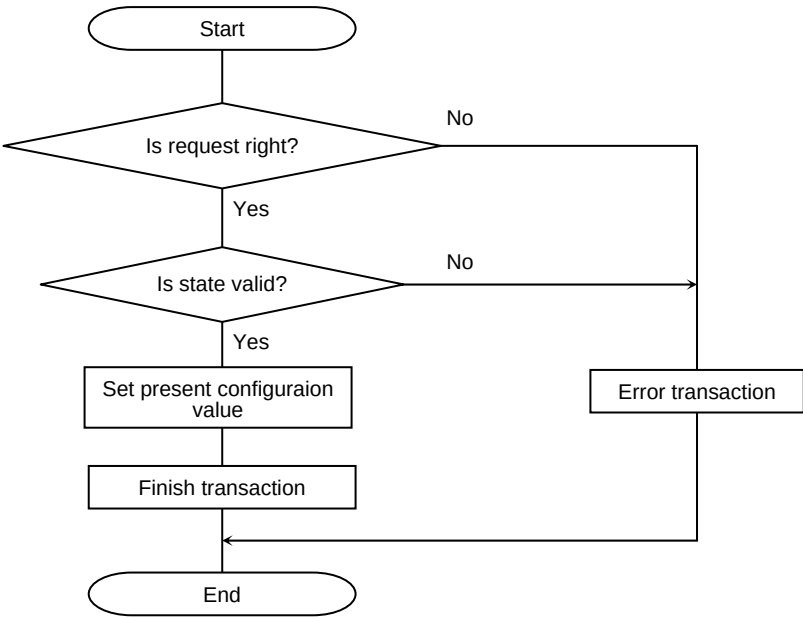
(c-3) GET\_STATUS request transaction



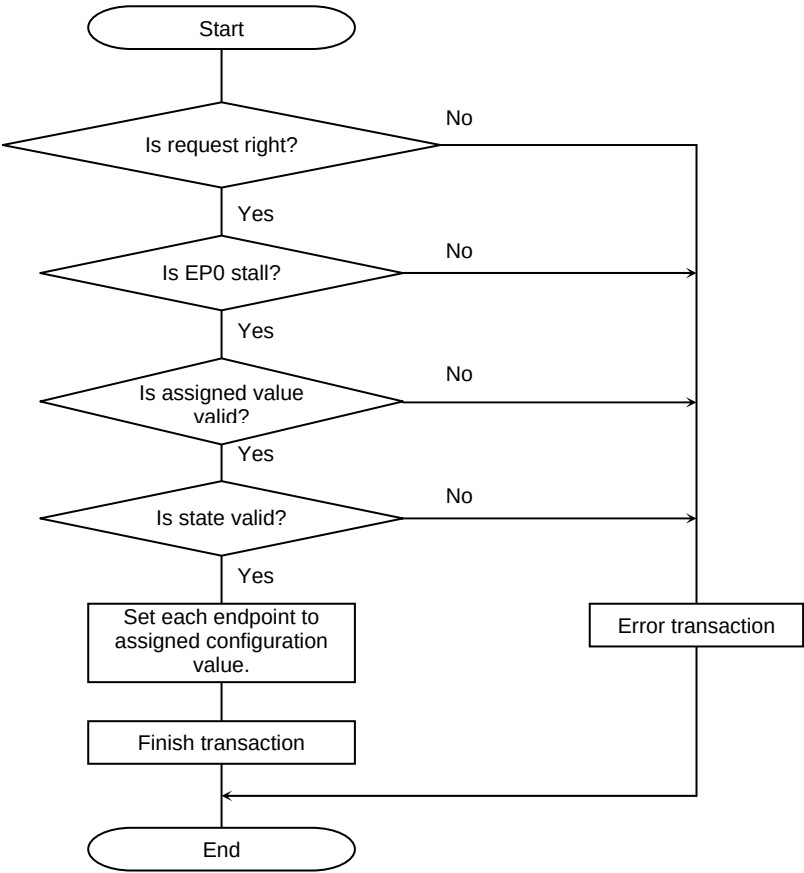
(c-4) SET\_CONFIGURATION request transaction



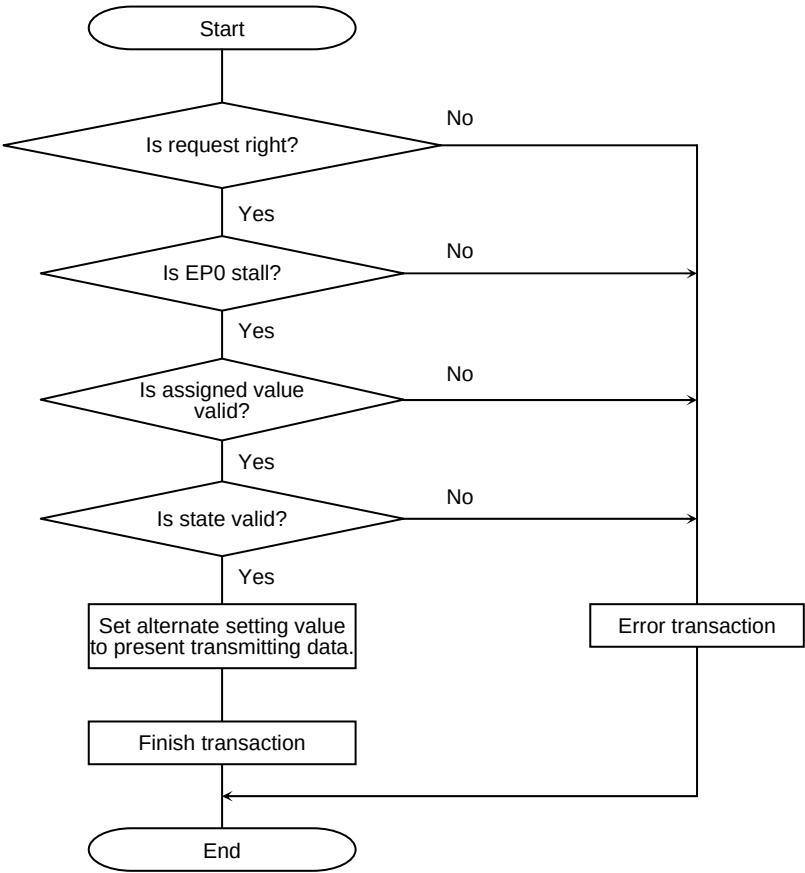
(c-5) GET\_CONFIGURATION request transaction



(c-6) SET\_INTERFACE request transaction

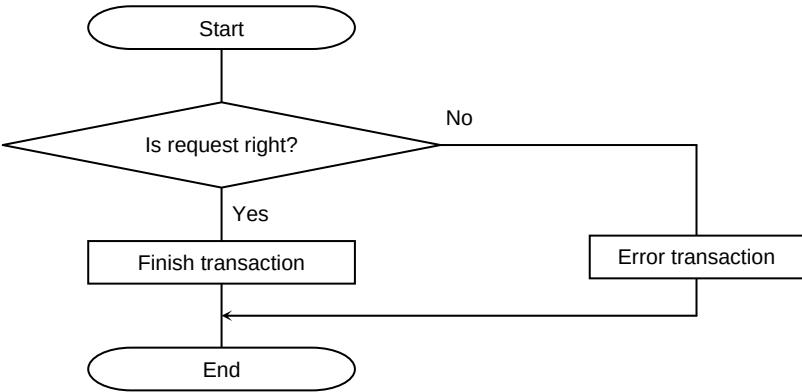


(c-7) SYNCH\_FRAME request transaction

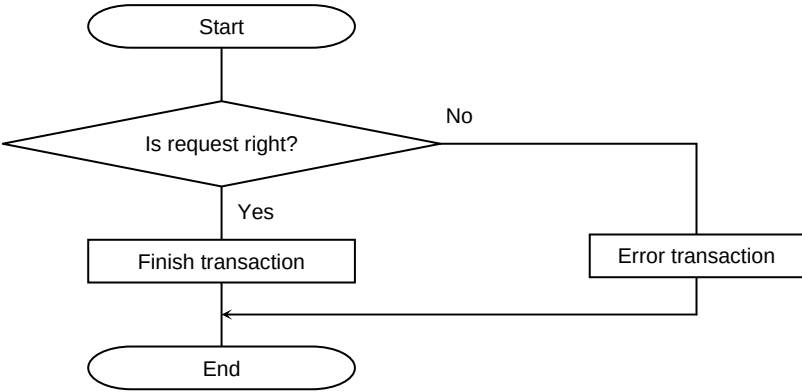




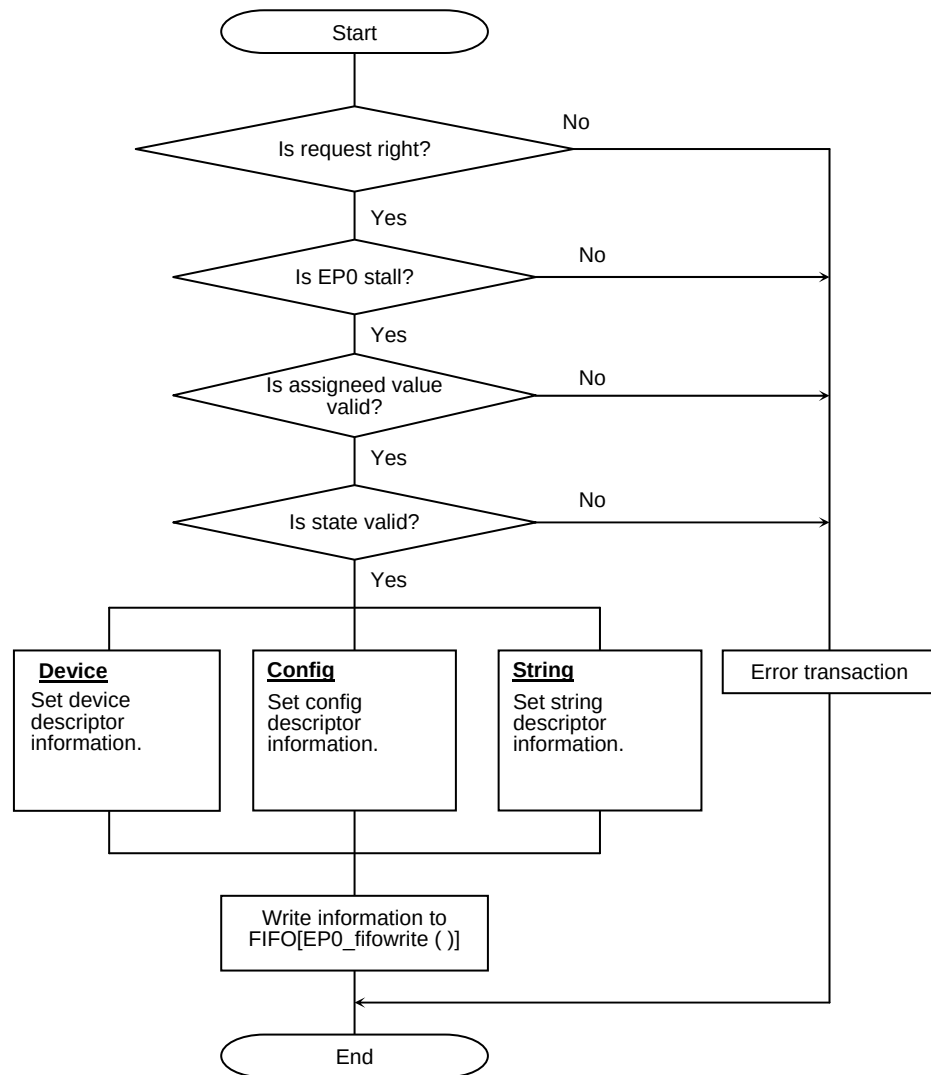
(c-8) SYNCH\_FRAME request transaction



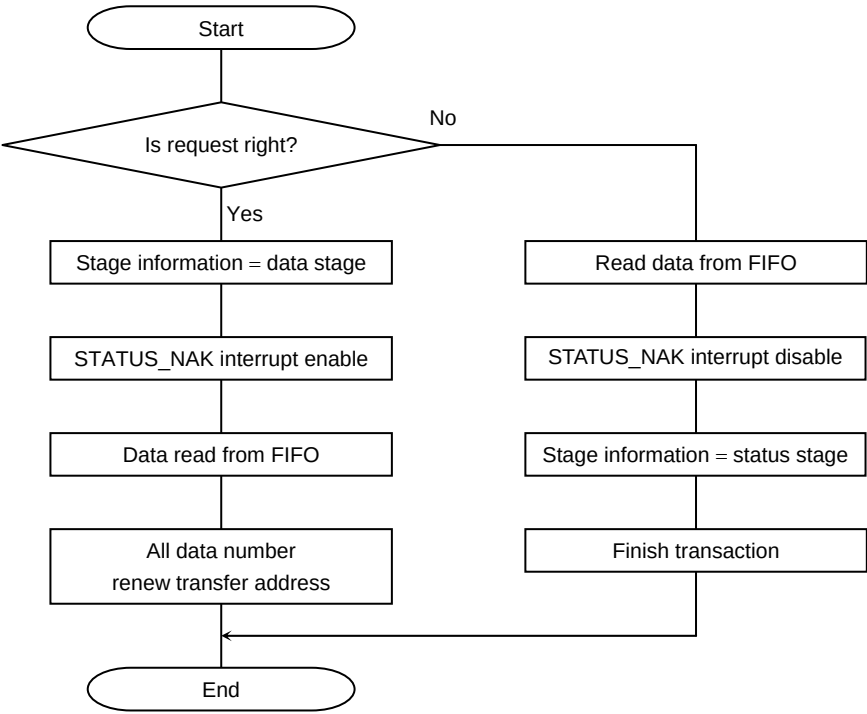
(c-9) SET\_DESCRIPTOR request transaction



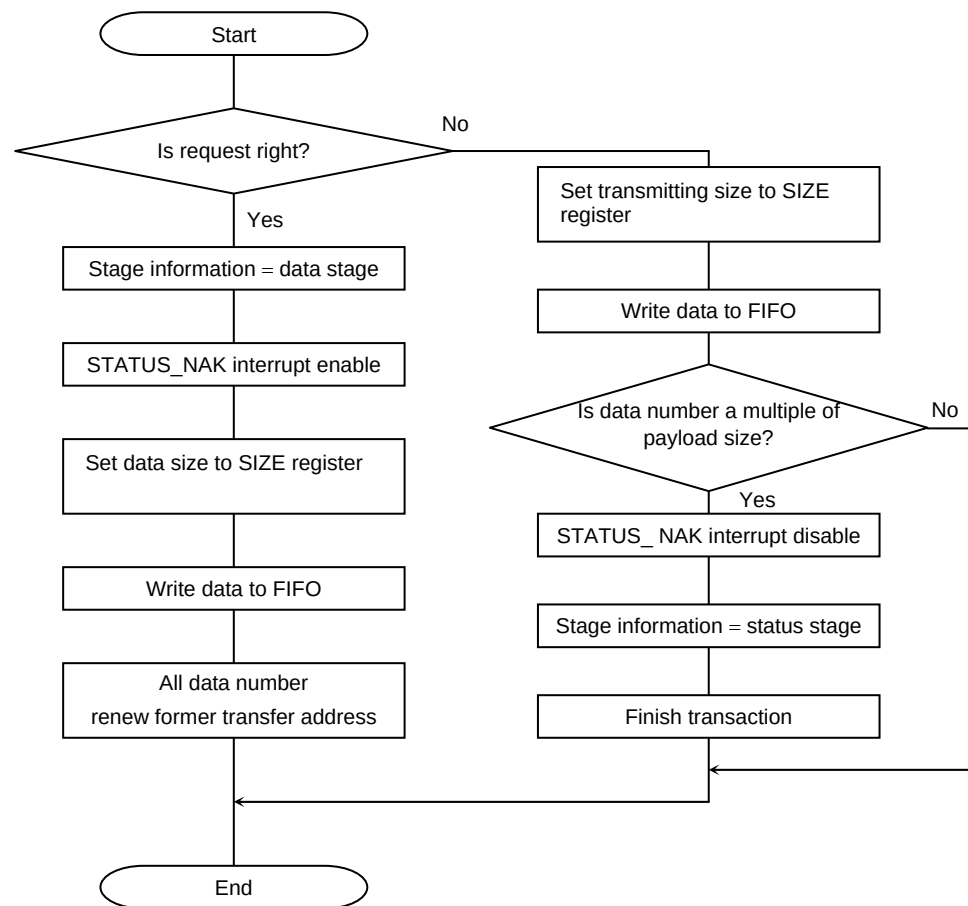
(c-10) GET\_DESCRIPTOR request transaction



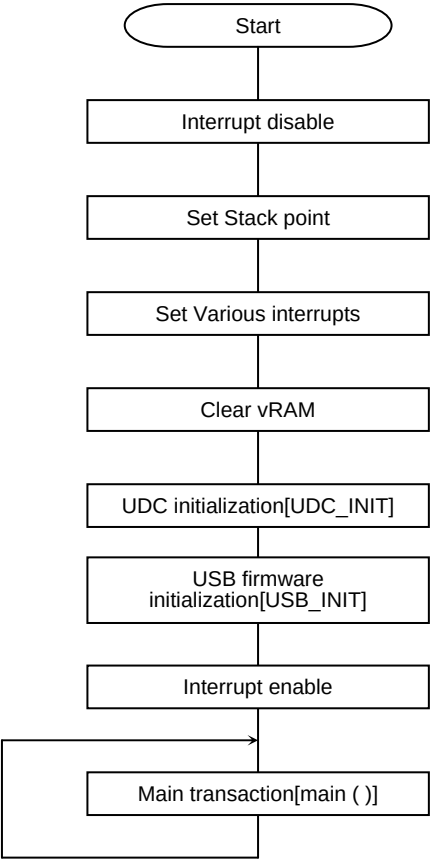
(c-11)Data read transaction to FIFO by EP0



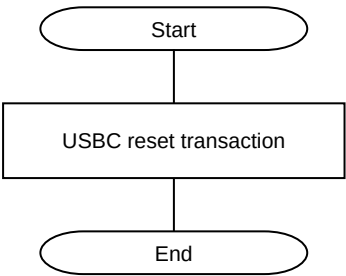
(c-12)Data write transaction to FIFO by EP0



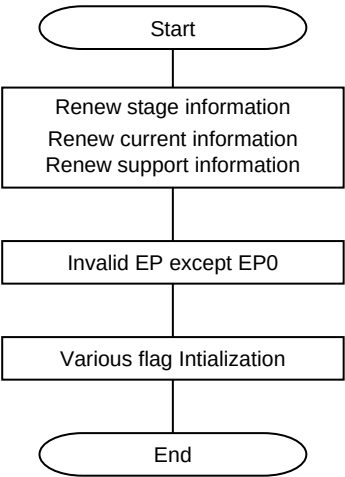
(c-13)Initial setting transaction of microcontroller



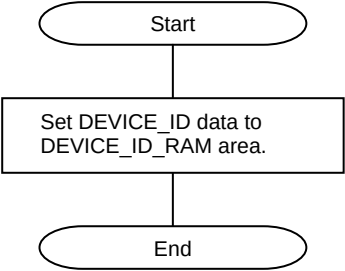
(c-14)Initial setting transaction of UDC



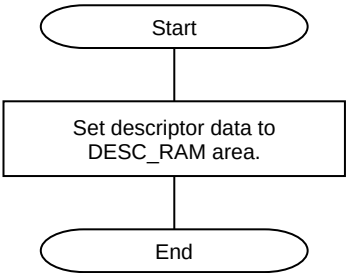
(c-15)Initial transaction of USB number changing firmware



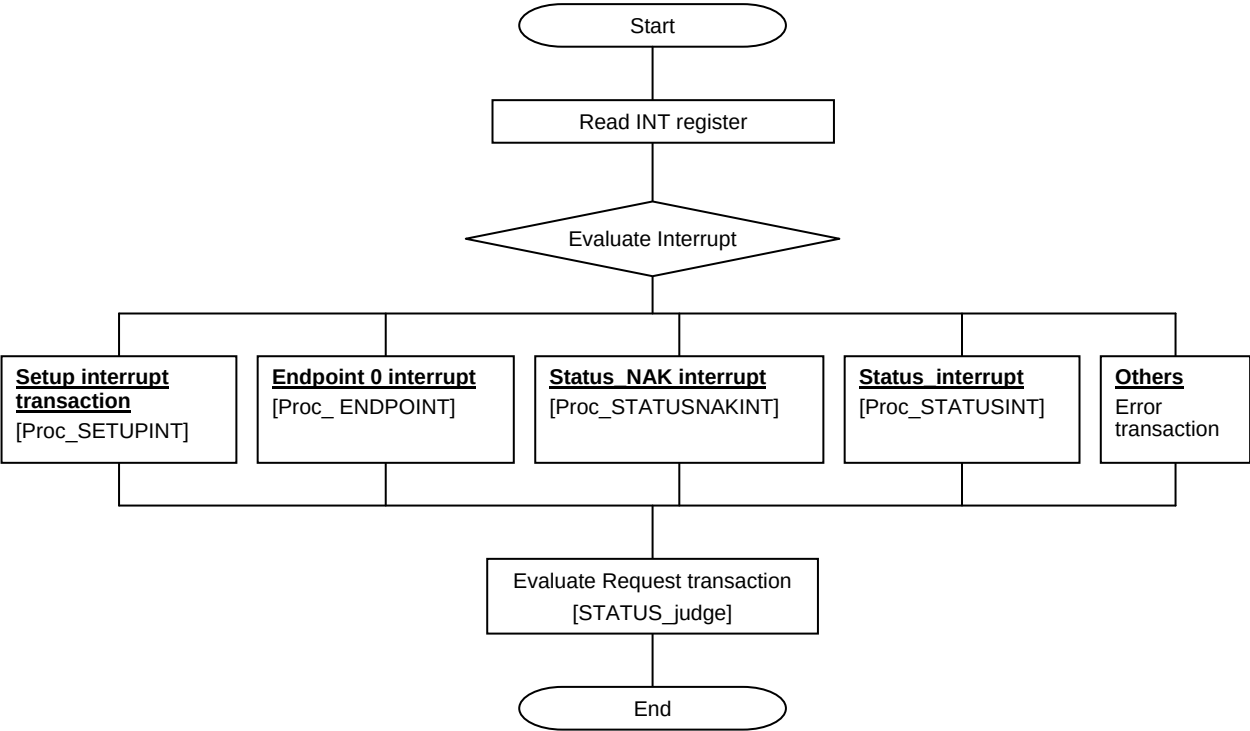
(c-16)Set DEVICE\_ID data to DEVICE\_ID of UDC



(c-17)Descriptor data set transaction



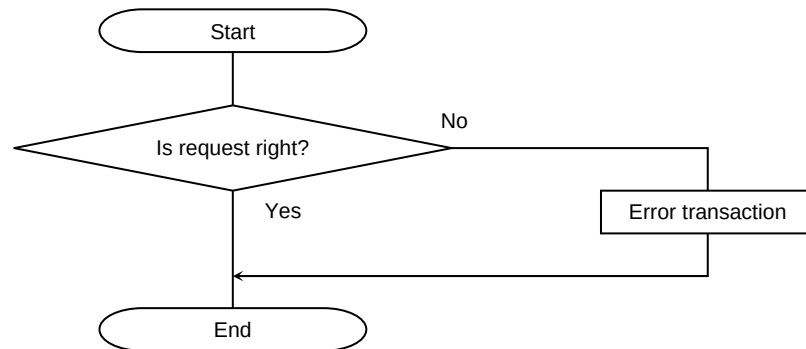
(c-18)USB interrupt transaction



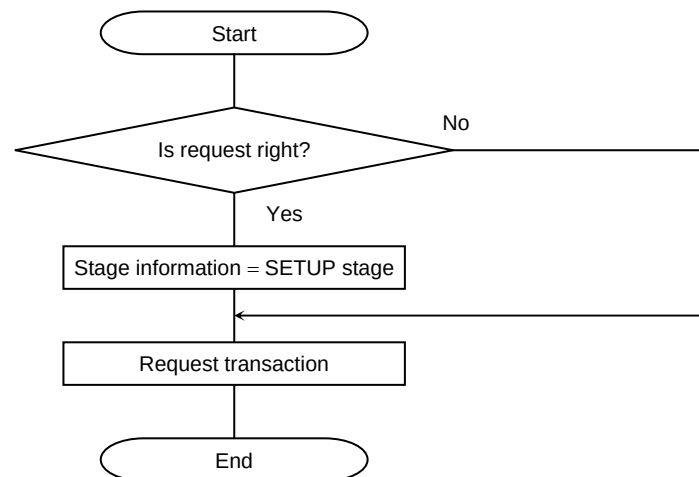
(c-19) Dummy function for not using maskable interrupts.

- Transaction performs nothing, therefore outline flow is skipped.

(c-20) Request evaluation transaction. If transaction result is error, it initiates STALL command.

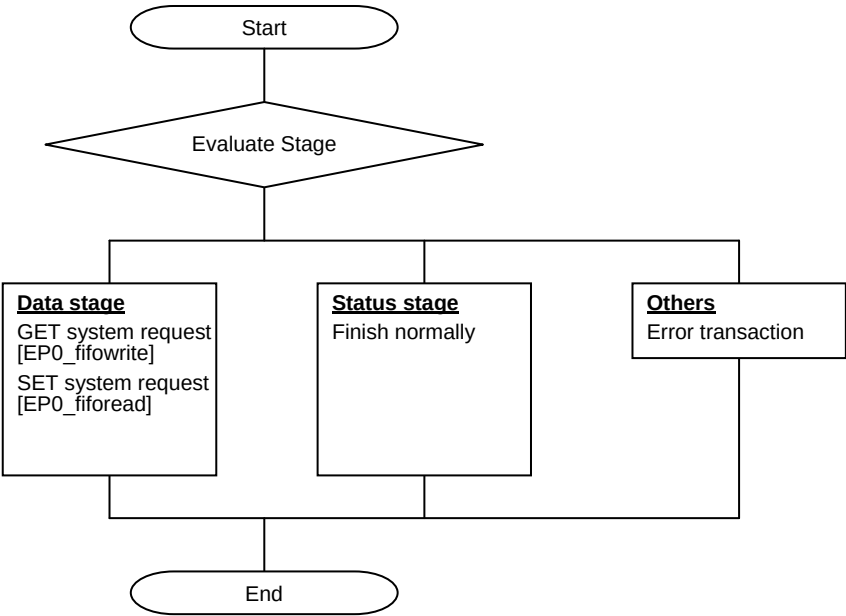


(c-21) SETUP stage transaction

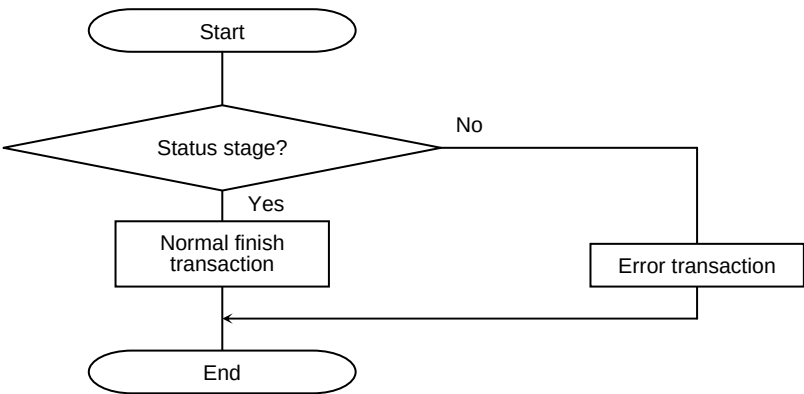




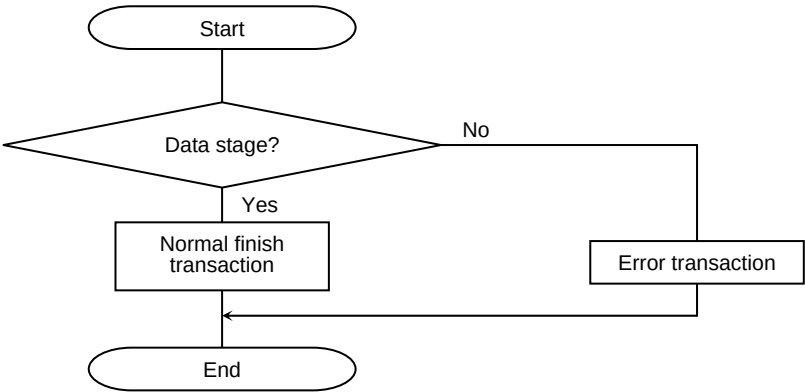
(c-22)Perform endpoint 0 transaction except in SETUP stage.



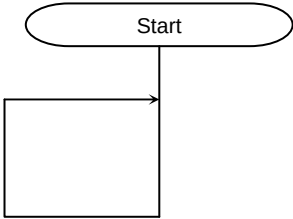
(c-23)Status stage interrupt transaction



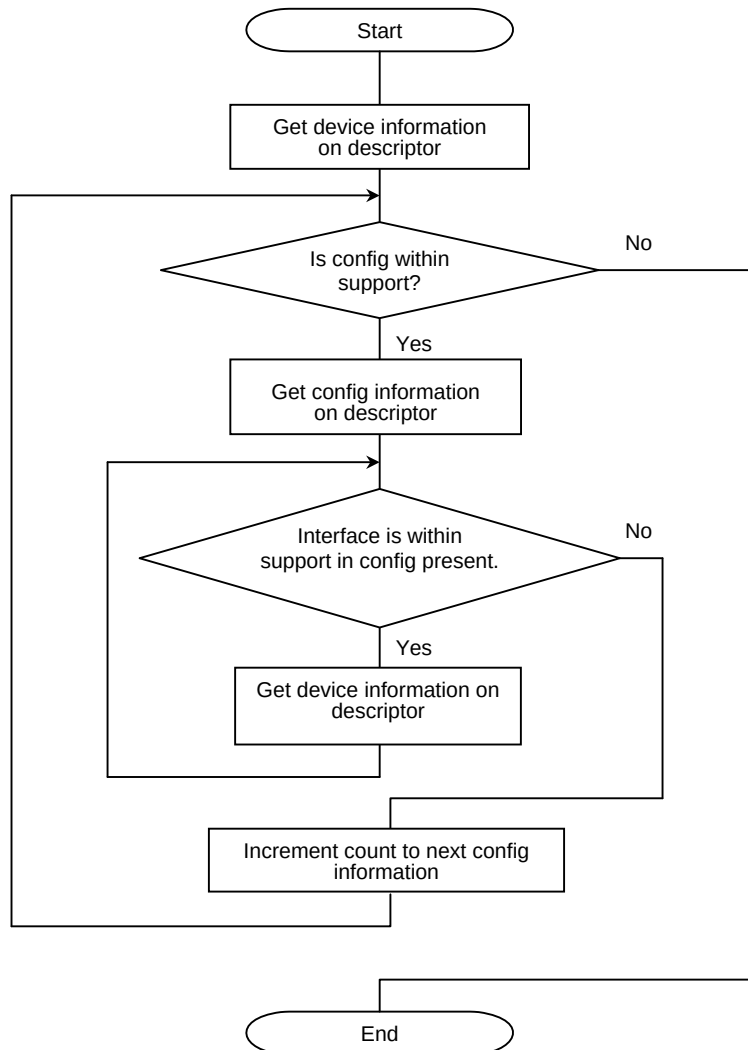
(c-24)STATUS\_NAK interrupt transaction



(c-25)This transaction is a non-transaction for USB interrupts.



## (c-26) Getting descriptor information (related to standard request)



### 3.16.11 Notice and Restrictions

1. When using the USB device controller in the TMP92CF30, a crystal oscillator is recommended (USB standard  $\leq 10 \text{ MHz} \pm 2500\text{ppm}$ ). In this case, a maximum of 3 stages of external hub can be due to the precision of this USB device controller and the internal clock. If USB compliance (USB logo) is needed, the 5 stages connection is needed for external hub. And it is needed that input 48MHz clock from X1USB pin (USB standard  $\leq \pm 2500\text{ppm}$ .)
2. Precaution for using the USB dual packet mode in the TMP92CF30

In the dual packet mode, each FIFO is divided into two independent packets (A and B) to be controlled alternately by hardware.

When reading data from a receive FIFO, it is necessary to check the state of the two packets to determine which packet should be processed first. At this time, the following precaution is required.

The EPx\_SIZE register that indicates the presence of valid data is provided separately for packets A and B. The CPU is required to check the respective PKT\_ACTIVE bits to determine which packet was accessed first and then to know the number of data in this packet. The packet with its PKT\_ACTIVE bit set to "1" is the packet which was received first.

In determining whether only packet A is active, only packet B is active, or both packets A and B are active, if the respective PKT\_ACTIVE bits are read sequentially, the state of each bit may change between each read. If this happens, the packets may not be processed in proper order.

Therefore, the PKT\_ACTIVE bit information in the EPx\_SIZE register should be captured and saved in another location such as RAM by using an interrupt request. Then, use this saved information to perform branch processing.

### 3.17 SPI Controller (SPIC)

The SPIC is a Serial Peripheral Interface Controller that supports only master mode.

It can be connected to the SD card, MMC (Multi Media Card) etc. in SPI mode.

Its features are summarized as follows:

- 1) On-chip 32-byte FIFOs for both transmission and reception
- 2) Generates the CRC-7 and CRC-16 values for transmission and reception
- 3) Baud Rate: 20 Mbps (max)
- 4) Can be connected to multiple SD cards and the MMC. (Since there is only on chip select signal preassigned as  $\overline{\text{SPCS}}$ , use other output ports to allow for more than two connections.)

This device has 1 channel SPI circuit. It shared with PR0~PR3 pins. However, it is possible also that it assign SPI function to PC4 ~PC6 pins.

- 5) Operates as the general synchronous SIO

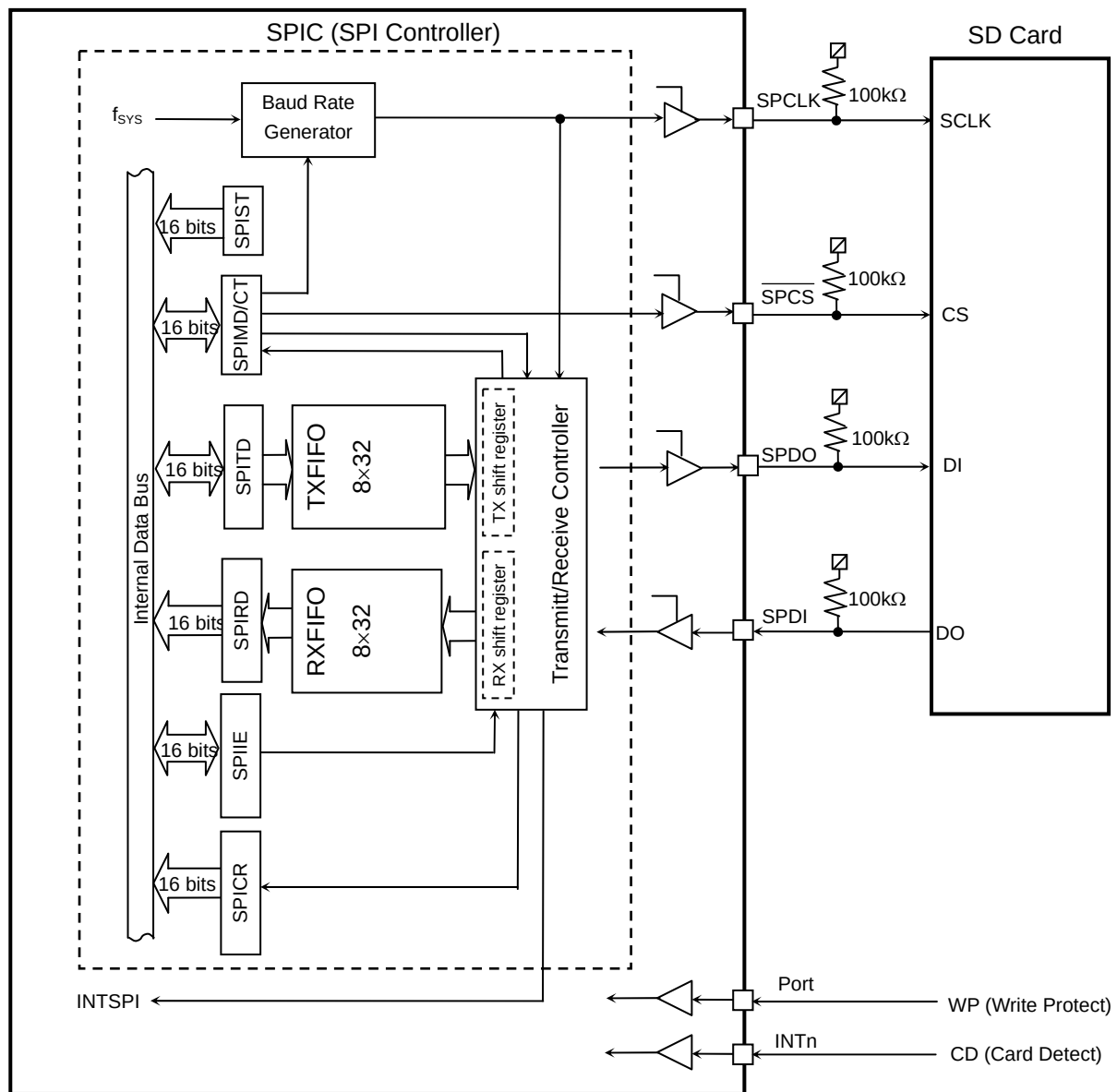
Selects the followings: MSB/LSB-first, 8/16-bit data length, rising/falling edge

- 6) Two types of interrupts: INTSPITX (Transmit interrupt), INTSPIRX (receive interrupt)

Select Read/Mask for interrupts: RFUL, TEMP, REND and TEND

## 3.17.1 Block Diagram

Figure 3.17.1 shows a block diagram of the SPIC and its connections with a SD card.



Note 1: The SPCLK,  $\overline{\text{SPCS}}$ , SPDO and SPDI pins are configured as input ports (Ports PR3, PR2, PR1 and PR0) upon reset.

Thus, these pins require pull-up resistors to fix their voltage levels. The pull-up resistor values should be adjusted under real-world conditions.

Note 2: Any one of general inputs and interrupt should be used as the WP (Write Protect) and CD (Card Detect) inputs, respectively.

Figure 3.17.1 Block Diagram and Connection Example

### 3.17.2 Special Function Registers (SFRs)

This section describes the SFRs of the SPIC. These are connected to the CPU with 16 bit data buses.

#### (1) SPIMD (SPI Mode Select register)

The SPIMD register specifies the operating mode, clock operation, etc.

| SPIMD Register                                                            |             |                                             |                                                            |                                                                           |             |                                                                                          |                                                                                                                                                                                                                                                                      |                                                            |                                                             |
|---------------------------------------------------------------------------|-------------|---------------------------------------------|------------------------------------------------------------|---------------------------------------------------------------------------|-------------|------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------|-------------------------------------------------------------|
| SPIMD<br>(0820H)<br><br>A read-modify-write operation cannot be performed | <div></div> | 7                                           | 6                                                          | 5                                                                         | 4           | 3                                                                                        | 2                                                                                                                                                                                                                                                                    | 1                                                          | 0                                                           |
|                                                                           | Bit Symbol  | SWRST                                       | XEN                                                        | <div></div>                                                               | <div></div> | <div></div>                                                                              | CLKSEL2                                                                                                                                                                                                                                                              | CLKSEL1                                                    | CLKSEL0                                                     |
|                                                                           | Read/Write  | W                                           | R/W                                                        | <div></div>                                                               | <div></div> | <div></div>                                                                              | R/W                                                                                                                                                                                                                                                                  |                                                            |                                                             |
|                                                                           | Reset State | 0                                           | 0                                                          | <div></div>                                                               | <div></div> | <div></div>                                                                              | 1                                                                                                                                                                                                                                                                    | 0                                                          | 0                                                           |
|                                                                           | Function    | Software Reset<br>0: Don't care<br>1: Reset | SYSCK<br>0: Disable<br>1: Enable                           |                                                                           |             |                                                                                          | Select Baud Rate(Note1)<br>000: Reserved      100: f <sub>sys</sub> /8<br>001: f <sub>sys</sub> /2          101: f <sub>sys</sub> /16<br>010: f <sub>sys</sub> /3          110: f <sub>sys</sub> /64<br>011: f <sub>sys</sub> /4          111: f <sub>sys</sub> /256 |                                                            |                                                             |
| (0821H)                                                                   | <div></div> | 15                                          | 14                                                         | 13                                                                        | 12          | 11                                                                                       | 10                                                                                                                                                                                                                                                                   | 9                                                          | 8                                                           |
|                                                                           | Bit Symbol  | LOOPBACK                                    | MSB1ST                                                     | DOSTAT                                                                    | <div></div> | TCPOL                                                                                    | RCPOL                                                                                                                                                                                                                                                                | TDINV                                                      | RDINV                                                       |
|                                                                           | Read/Write  | R/W                                         |                                                            |                                                                           | <div></div> | R/W                                                                                      |                                                                                                                                                                                                                                                                      |                                                            |                                                             |
|                                                                           | Reset State | 0                                           | 1                                                          | 1                                                                         | <div></div> | 0                                                                                        | 0                                                                                                                                                                                                                                                                    | 0                                                          | 0                                                           |
|                                                                           | Function    | LOOPBACK Test Mode<br>0:Disable<br>1:Enable | Start Bit for Transmission / Reception<br>0: LSB<br>1: MSB | SPDO Pin State When Not Transmitting<br>0: Fixed to “0”<br>1:Fixed to “1” |             | Synchronizati-on Clock Edge Select for Transmission<br>0: Falling edge<br>1: Rising edge | Synchronizat-ion Clock Edge Select for Reception<br>0: fall<br>1: rise                                                                                                                                                                                               | Data Inversion for Transmissio<br>n0: Disable<br>1: Enable | Data Inversio<br>n for Reception<br>0: Disable<br>1: Enable |

Note: The SD card of the TMP92CF30 supports a baud rate of up to 20 Mbps in SPI mode. The baud rate should be adjusted with the operating frequency of the CPU (f<sub>sys</sub>) so that it does not exceed 20 MHz.

Figure 3.17.2 SPIMD Register

#### (a) LOOPBACK

Setting the XEN and LOOPBACK bits to 1 enables the internal SPDO output to be internally connected to the SPDI input. This setup can be used for testing.

Also, a clock signal is generated from the SPCLK pin, regardless of whether data transmission or reception is in progress.

Data transmission or reception must not be performed while changing the state of this bit.

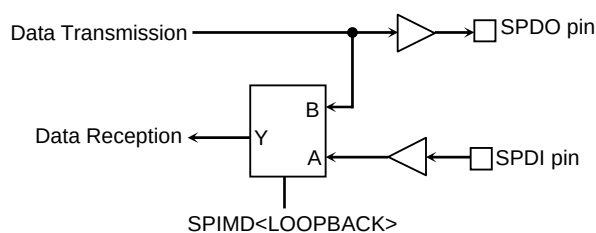


Figure 3.17.3 LOOPBACK Bit Configuration

## (b) MSB1ST

This bit specifies whether to transmit/receive byte with the MSB first or with the LSB first. Data transmission or reception must not be performed while changing the state of this bit.

## (c) DOSTAT

This bit specifies the status of the SPDO pin of when data transmission is not performed (i.e., after completing data transmission or during data reception). Data transmission or reception must not be performed while changing the state of this bit.

## (d) TCPOL

This bit specifies the polarity of the active edge of the synchronization clock for data transmission.

The XEN bit should be cleared to “0” for changing the state of this bit. At the same time, RCPOL should also be cleared to “0”.

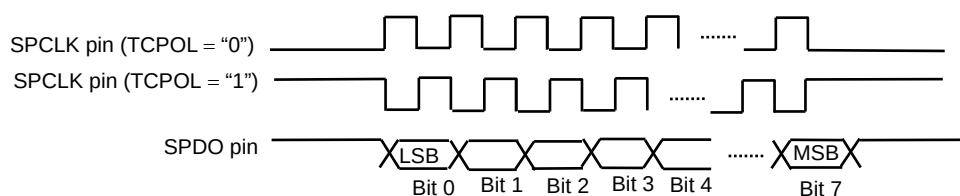


Figure 3.17.4 Timing Diagram of Data Transmissions Controlled by the TCPOL Bit

## (e) RCPOL

This bit specifies the polarity of the active edge of the synchronization clock for data reception.

The SPIMD<XEN> bit should be cleared to “0” for changing the state of this bit. TCPOL should also be cleared to “0”.

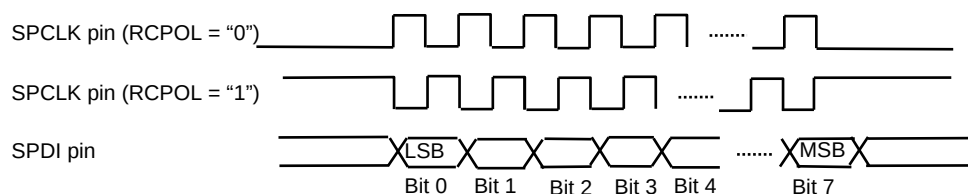


Figure 3.17.5 Timing Diagram of Data Receptions Controlled by the RCPOL Bit

## (f) TDINV

This bit specifies whether to logically invert the data transmitted from the SPDO pin or not. Data transmission or reception must not be performed while changing the state of this bit.

## (g) RDINV

This bit specifies whether to logically invert the data received from the SPDI pin or not. Data transmission or reception must not be performed while changing the state of this bit.



## (h) SWRST

This bit is used to performs a software reset of the read and write pointers for data transmission and reception. Stop the data transmission after writing a “0” to the SPICT<TXE> bit where XEN = “1”. Then, write a “1” to the SWRST bit to initialize the read and write pointers of transmit and receive FIFO buffers.

Writing a “0” to the SPICT<TXE> bit stops data transmission after transmitting the UNIT data that is currently being transmitted. Then, writing a “1” to the SWRST bit invalidate the data in the transmit FIFO buffer. Therefore, the data is not output even if the data transmission is restarted after performing a software reset. Do not write a “1” to the SWRST bit in the middle of data transmission.

In case of performing data reception, the received data contained in the receive FIFO buffer becomes invalid.

However, when performing Sequential-mode data reception, data reception continues even if the data in the receive FIFO buffer becomes invalid. Therefore, stop data reception by writing a “0” to the SPICT<RXE> bit after receiving the data that is currently being received. Then, (after confirming there is no UNIT data currently being received, or ) the receive operation can be stopped completely by writing a “1” to the SWRST bit after checking no UNIT data in receiving (namely after REND interrupt or the time to receive 1UNIT).

Do not write a “1” to the SWRST bit during a data reception. Software reset can be performed in a single-shot operation, which is to write a “1” to the SWRST bit (it is not required to write a “0” to the SWRST bit). Simultaneous writing of 1s to the XEN and SWRST bits is also supported.

## (i) XEN

This bit enables or disables the internal clock signal. Always set this bit to “1” when using the SPI controller.

## (j) CLKSEL2:0

This bit selects the baud rate. The baud rate is generated using the system clock  $f_{SYS}$  and is programmable as shown below according to the system clock settings.

Data transmission or reception must not be performed while changing the state of these bits

Note: The SD card of the TMP92CF30 supports a baud rate of up to 20 Mbps. This field should be programmed so that SPCLK signal does not exceed 20 MHz When setting the baud rates, select less than 20 Mbps according to the operation speed of CPU ( $f_{SYS}$ ).

Table 3.17.1 Example of Baud Rate

| <CLKSEL2:0>   | Baud Rate [Mbps]           |                            |
|---------------|----------------------------|----------------------------|
|               | $f_{SYS} = 60 \text{ MHz}$ | $f_{SYS} = 80 \text{ MHz}$ |
| $f_{SYS}/2$   | –                          | –                          |
| $f_{SYS}/3$   | 20                         | –                          |
| $f_{SYS}/4$   | 15                         | 20                         |
| $f_{SYS}/8$   | 7.5                        | 10                         |
| $f_{SYS}/16$  | 3.75                       | 5                          |
| $f_{SYS}/64$  | 0.9375                     | 1.25                       |
| $f_{SYS}/256$ | 0.234375                   | 0.3125                     |

## (2) SPI Control Register (SPICT)

The SPICT register specifies data length, CRC, etc.

| SPICT Register   |             |                                                  |                                                    |                                                                 |                                                  |                                                |                                                                 |                                                 |                                           |
|------------------|-------------|--------------------------------------------------|----------------------------------------------------|-----------------------------------------------------------------|--------------------------------------------------|------------------------------------------------|-----------------------------------------------------------------|-------------------------------------------------|-------------------------------------------|
| SPICT<br>(0822H) | <div></div> | 7                                                | 6                                                  | 5                                                               | 4                                                | 3                                              | 2                                                               | 1                                               | 0                                         |
|                  | Bit Symbol  | CEN                                              | SPCS_B                                             | UNIT16                                                          | TXMOD                                            | TXE                                            | FDPXE                                                           | RXMOD                                           | RXE                                       |
|                  | Read/Write  | R/W                                              |                                                    |                                                                 |                                                  |                                                |                                                                 |                                                 |                                           |
|                  | Reset State | 0                                                | 1                                                  | 0                                                               | 0                                                | 0                                              | 0                                                               | 0                                               | 0                                         |
|                  | Function    | Communication Control<br>0: Disable<br>1: Enable | SPCS Pin Control<br>0: Set to "0"<br>1: Set to "1" | Data Length Select<br>0: 8 bits<br>1: 16 bits                   | Transmit Mode Select<br>0: UNIT<br>1: Sequential | Transmission Enable<br>0: Disable<br>1: Enable | Alignment Enable in Full duplex mode<br>0: Disable<br>1: Enable | Receive Mode Select<br>0: UNIT<br>1: Sequential | Receive Enable<br>0: Disable<br>1: Enable |
| (0823H)          | <div></div> | 15                                               | 14                                                 | 13                                                              | 12                                               | 11                                             | 10                                                              | 9                                               | 8                                         |
|                  | Bit Symbol  | CRC16_7_B                                        | CRCRX_TX_B                                         | CRCRESET_B                                                      | <div></div>                                      | <div></div>                                    | <div></div>                                                     | <div></div>                                     | <div></div>                               |
|                  | Read/Write  | R/W                                              |                                                    |                                                                 | <div></div>                                      | <div></div>                                    | <div></div>                                                     | <div></div>                                     | <div></div>                               |
|                  | Reset State | 0                                                | 0                                                  | 0                                                               | <div></div>                                      | <div></div>                                    | <div></div>                                                     | <div></div>                                     | <div></div>                               |
|                  | Function    | CRC Select<br>0: CRC7<br>1: CRC16                | CRC Data<br>0: Transmit<br>1: Receive              | CRC Calculation Register Control<br>0: Reset<br>1:Reset Release |                                                  |                                                |                                                                 |                                                 |                                           |

Figure 3.17.6 SPICT Register

## (a) CRC16\_7\_B

This bit selects the CRC calculation algorithm from the CRC7 and CRC16.

## (b) CRCRX\_TX\_B

This bit selects the data to be sent to the CRC generator. When CRCRX\_TX\_B = "0", the CRC calculation is performed on the transmit data. Otherwise, it is performed on the received data.

## (c) CRCRESET\_B

This bit is used to initialize the CRC calculation register.

This section describes how to calculate the CRC16 of the transmit data and to append the calculated CRC value at the end of the transmit data. Figure 3.17.7 below illustrates the flow chart of the CRC calculation procedures.

- (1) Program the SPICT<CRC16\_7\_B> bit to select the CRC algorithm from CRC7 and CRC16. Then, also program the CRCRX\_TX\_B bit to specify the data on which the CRC calculation is performed.
- (2) To reset the SPICR register, write a “0” to the CRCRESET\_B bit and then write a “1” to the same bit.
- (3) Load the SPITD register with the transmit data, and wait until transmission of all data is completed.
- (4) Read the SPICR register and obtain the result of the CRC calculation.
- (5) Transmit the CRC obtained in step (4) in the same way as step (3).

The CRC calculation on the receive data can be performed in the same procedures.

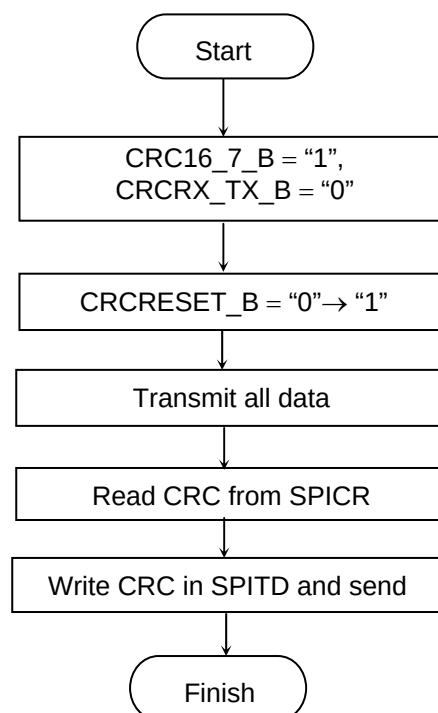


Figure 3.17.7 Flow Chart of the CRC Calculation Procedures

## (d) CEN

This bit enables or disables the pins for the SD card and MMC connections.

When the card is not inserted or when it is not powered on, a shoot through current might flow in the SPDI pin, for it enters the floating state. Also, currents may unintentionally flow into the card from the  $\overline{\text{SPCS}}$ , SPCLK and SPDO pins when they generate a logic 1. This bit can be used to avoid these problems.

If write <CEN> to “0” with PRCR and PRFC selecting  $\overline{\text{SPCS}}$ , SPCLK, SPDO and SPDI signal, SPDI pin is prohibited to input (avoiding penetrated current) and  $\overline{\text{SPCS}}$ , SPCLK, SPDO pin become high impedance.

When writing a “1” to the CEN bit, ensure that a card is properly inserted and powered on, as well as that the clock signal is supplied to the SPIC (SPIMD<XEN> = “1”).

## (e) SPCS\_B

This bit specified the logic state of the  $\overline{\text{SPCS}}$  output.

## (f) UNIT16

This bit selects the data length for transmission and reception. The data length is hereafter referred to as the UNIT. Data transmission or reception must not be performed while changing the state of this bit

## (g) FDPXE

This bit should be set to “1” when performing the full-duplex communication. This bit specifies whether to align the transmit and receive data on the UNIT-size boundaries.

Data transmission or reception must not be performed while changing the state of this bit.

## (h) TXMOD

This bit selects the data transmission mode from UNIT and Sequential modes. During transmission, it is prohibited to change the transmission mode from Sequential to UNIT, or vice versa.

For UNIT-mode transmission, the transmit FIFO buffer is disabled. The TEMP interrupt is generated when the data is loaded from the transmit data register (SPITD) to the transmit shift register.

For sequential-mode transmission, the 32-byte FIFO is enabled. The TEMP interrupt is generated when the empty space of the FIFO becomes 16 bytes or 32 bytes.

## (i) TXE

This bit enables or disables data transmission. Data transmission is started when this bit set to “1” after loading the transmit data into the transmit FIFO, or when loading the transmit data to the transmit FIFO when this bit is already set to “1”. The state of this bit can be changed even during data transmission. If this bit is cleared to 0 during a data transmission, the transmission is stopped after completing the transmission of the UNIT data currently being transmitted.

Important Note:

When in UNIT mode (TXMOD = "0"), the following restriction is imposed on the system operation.

**When the SPICT<TEX> bit is set to "1", the state of any bits must not be changed until the data transmission is completed.**

## Sample Program 1:

```
LD      (SPITDx), A      ; Load the transmit data
DI                      ; Disable the interrupt
SET 3,   (SPICT)         ; Start transmission by setting the TXE bit to "1"

Wait:   BIT 1,   (SPIST)   ; Wait for the completion of the transmission
        JPZ,     Wait
RES 3,   (SPICT)         ; Disable the transmission by clearing the TXE bit to "0"
EI                      ; Enable the interrupt
```

## Sample Program 2 (Recommend):

Check the transmission end flag. (SPIST<TEND> = "1")

```
LD      (SPITDx), A      ; Load "A" the transmit data
DI                      ; Disable the interrupt
SET 3,   (SPICT)         ; Start transmission by setting the TXE bit to "1"
RES 3,   (SPICT)         ; Disable the transmission by clearing the TXE bit to "0"
EI                      ; Enable the interrupt
```

## (j) RXMOD

This bit selects the data reception mode from UNIT and Sequential modes. During reception, it is prohibited to change the reception mode from Sequential to UNIT, or vice versa.

For UNIT-mode reception, the receive FIFO buffer is disabled and the RFUL interrupt is generated when the received data is loaded from the receive shift register to the receive data register (SPIRD).

For sequential-mode reception, the 32-byte receive FIFO is enabled and the RFUL interrupt is generated when the size of received data stored in the receive FIFO reaches 16 or 32 bytes.

## (k) RXE

In the UNIT-mode reception, writing a “1” to this bit enables the reception of only one UNIT-size data.

When reading the receive data register (SPIRD) while this bit is kept enabled, one more UNIT data is additionally received.

In Sequential mode, writing a “1” to this bit enables the sequential data reception until the 32-byte FIFO buffer becomes full. The state of this bit can be changed even during the data reception. If this bit is cleared to “0” during a data reception, the reception is stopped after completing the reception of the UNIT data currently being received.

## [Data Transmission/Reception Modes]

This SPI Controller supports six operating modes as listed below.

These are specified by the FDPXE, RXMOD, RXE, TXMOD, TXE bits.

Table 3.17.2 Data Transmission Reception Modes

| Operating Mode                            | Bit Settings |         |       |         |       | Description                                                                                                     |
|-------------------------------------------|--------------|---------|-------|---------|-------|-----------------------------------------------------------------------------------------------------------------|
|                                           | <FDPXE>      | <TXMOD> | <TXE> | <RXMOD> | <RXE> |                                                                                                                 |
| (1) UNIT transmission                     | 0            | 0       | 1     | x       | x     | Transmit the SPITD data per UNIT                                                                                |
| (2) Sequential transmission               | 0            | 1       | 1     | x       | x     | Transmit the FIFO data sequentially                                                                             |
| (3) UNIT reception                        | 0            | x       | x     | 0       | 1     | Receive only one UNIT-size data                                                                                 |
| (4) Sequential reception                  | 0            | x       | x     | 1       | 1     | Automatically receive data if FIFO buffer has any empty space                                                   |
| (5) UNIT transmission and reception       | 1            | 0       | 1     | 0       | 1     | Transmit/receive one UNIT-size data with the addresses of transmit/receive data aligned on UNIT-size boundaries |
| (6) Sequential transmission and reception | 1            | 1       | 1     | 1       | 1     | Transmit/receive data sequentially with the addresses of transmit/receive data aligned on UNIT-size boundaries  |

x: Don't care

### Differences Between the UNIT-mode and Sequential-mode transmissions

The UNIT mode for the data transmission can be selected by writing a “0” to the SPICT<TXMOD> bit.

The transmit FIFO buffer is disabled in UNIT mode. The UNIT-mode transmission starts when the UNIT-size data is loaded into the SPITD register where SPICT<TXE> = “1”, or when the SPICT<TXE> is set to “1” after loading one UNIT-size data into the SPITD register. During the data transmission, it is prohibited to change the transmission mode from Sequential to UNIT, or vice versa.

In the UNIT-mode transmission, the TEMP interrupt is generated when the transmit data is loaded from the transmit data register (SPITD) to the transmit shift register. Also, the TEND interrupt is generated upon completion of the transmission of the last UNIT data.

#### Important Note:

When in UNIT mode (TXMOD = “0”), the following restriction is imposed on the system operation.

**When the SPICT<TEX> bit is set to “1”, the state of any bits must not be changed until the data transmission is completed.**

#### Sample Program 1:

```
LD      (SPITDx), A      ; Load the transmit data
DI      ; Disable the interrupt
SET 3,   (SPICT)         ; Start transmission by setting the TXE bit to “1”

Wait:   BIT 1,   (SPIST)   ; Wait for the completion of the transmission
        JPZ,     Wait
RES 3,   (SPICT)         ; Disable the transmission by clearing the TXE bit to “0”
EI      ; Enable the interrupt
```

#### Sample Program 2 (Recommend):

Check the transmission end flag. (SPIST<TEND> = “1”)

```
LD      (SPITDx), A      ; Load “A” the transmit data
DI      ; Disable the interrupt
SET 3,   (SPICT)         ; Start transmission by setting the TXE bit to “1”
RES 3,   (SPICT)         ; Disable the transmission by clearing the TXE bit to “0”
EI      ; Enable the interrupt
```

The Sequential mode for the data transmission can be selected by writing a “1” to the SPICT<TXMOD> bit. The 32-byte FIFO is enabled in Sequential mode.

In this mode, the data writes to the transmit FIFO must be performed in 16-byte units. Otherwise, the TEMP interrupt is not properly generated.

In the Sequential-mode transmission, transmit data written into the SPITD is loaded sequentially when SPICT<TXE> = “1”. The transmission in this mode can also be started by setting the SPICT<TXE> bit to “1” after writing the transmit data into the transmit FIFO. The transmit data is transmitted in the same order as they were written into the FIFO.

This mode of transmission keeps transmitting data as long as the transmit data exists. Therefore, the Sequential-mode transmission continues as long as the transmit FIFO (32 bytes) has any valid data. During the data transmission, it is prohibited to change the transmission mode from Sequential to UNIT, or vice versa.

The state of the SPICT<TXE> bit can be changed even during the data transmission. Writing a “0” to the SPICT<TXE> bit during a transmission stops the transmission after completing the transmission of the UNIT data currently being transmitted.

The TEMP interrupt is generated when the empty space size of the FIFO becomes 16 or 32 bytes. The TEND interrupt is generated upon completion of the transmission of the last UNIT data.



### Differences Between the UNIT-mode and Sequential-mode Reception

The UNIT-mode reception receives only one UNIT-size data. The UNIT mode for the data reception can be selected by writing a “0” to the SPICT<RXMOD> bit.

The receive FIFO is disabled in UNIT mode. Writing a “1” to the SPICT<RXE> bit initiates a receive operation of one UNIT data. Then, the transmission is terminated after storing the received data into the receive data register (SPIRD). To perform one-UNIT data reception, read the SPIRD register after writing a “0” to the SPICT<RXE> bit. If the SPIRD register is read again when the SPICT<RXE> bit is set to “1”, one-UNIT data is additionally received. During the data reception, it is prohibited to change the reception mode from Sequential to UNIT, or vice versa.

In this mode, the RFUL and REND interrupts are generated when the receive data is loaded into the SPIRD register from the receive shift register.

The Sequential-mode reception automatically receives the data as long as the receive FIFO has any empty space. The Sequential mode is selected by writing a “1” to the SPICT<RXMOD> bit. The 32-byte receive FIFO is disabled in this mode. In this reception mode, the data reads from the receive FIFO must be performed in 16-byteunits. Otherwise, the RFUL interrupt is not properly generated.

Received data is stored into the receive FIFO by writing a “1” to the SPICT<RXE> bit.

This mode of reception keeps receiving the next data automatically unless the data receive FIFO becomes full (32 bytes). Therefore, the reception continues sequentially without stopping at every UNIT-sized reception. During the data reception, it is prohibited to change the reception mode from Sequential to UNIT, or vice versa.

Writing a “0” to the SPICT<RXE> bit during a reception stops the data reception after completing the reception of the UNIT data currently being received.

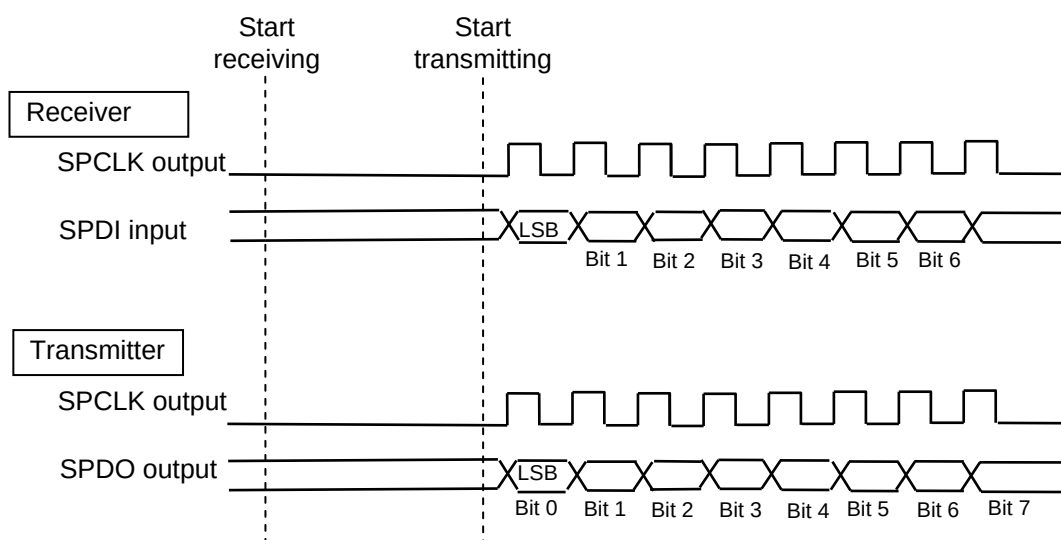
The RFUL interrupt is generated when the size of data stored into the FIFO reaches 16 or 32 bytes. The REND interrupt is generated when the 32-byte receive FIFO becomes full.

### Transmit and Receive Operation

When performing a data transmission and reception simultaneously, the FDPXE bit must be set to "1".

Write a "1" to the SPICT<RXE> bit after writing a "1" to the FDPXE bit to put the receiver into standby mode for the UNIT-mode reception. Writing a "1" to the SPICT<RXE> bit after writing a "1" to the <FDPXE> bit does not immediately initiate the receive operation. This is because the data to be transmitted at the same time has not been prepared. Transmit and receive operation is started only after the transmit data is written into the SPITD register where SPICT<TXE> = "1".

The figure below shows the operations of the receiver and transmitter for the simultaneous transmit and receive operation. :



Note: If the data transmission and reception are not performed simultaneously, data communication should be performed with the FDPXE bit cleared to "0".

Figure 3.17.8 Transmit and Receive Operation

### (3) Interrupts

The SPIC generates two types of interrupt requests to the Interrupt Controller (INTC), which are the transmit interrupt (INTSPITX) and receive interrupt (INTSPIRX) requests. Also, the SPIC has four types of interrupts; two for transmission and two for reception.

#### (a) Transmit interrupts

TEMP (Transmit FIFO Empty interrupt) and TEND (Transmit End interrupt)

As for the TEMP interrupt, the timing of the interrupt generation differs depending on the transmission mode, which is UNIT or Sequential.

In the Sequential-mode transmission, the data writes to the transmit FIFO must be performed in 16-byte units. Otherwise, the TEMP interrupt is not properly generated.

##### UNIT-mode transmission

Since the transmit FIFO is disabled in this mode, the TEMP interrupt is generated when the data written in the transmit data register (SPITD) is loaded into the transmit shift register.

The TEND interrupt is generated when the transmission of the last UNIT data is completed with the FIFO being empty (i.e., after the falling edge of the last bit clock where  $SPIMD<TCPOL> = "0"$ ).

##### Sequential-mode transmission

The TEMP interrupt is generated by the following two conditions: One is when the empty space size of the transmit FIFO reaches 16 bytes, and the other is when it reaches 32 bytes.

The TEND interrupt is generated when the transmission of the last UNIT data is completed with the FIFO being empty (i.e., after the falling edge of the last bit clock where  $SPIMD<TCPOL> = "0"$ ).

#### (b) Receive interrupts

RFUL (Receive FIFO interrupt) and REND (Receive End interrupt).

As for the RFUL interrupt, the timing of the interrupt generation differs depending on the reception mode; which is UNIT or Sequential.

In the Sequential-mode transmission, the data reads from the receive FIFO must be performed in 16-byte units. Otherwise, the RFUL interrupt is not properly generated.

##### UNIT-mode reception

Since the receive FIFO is disabled in this mode, the RFUL interrupt is generated at the same timing as the REND interrupt is generated.

The RFUL and REND interrupts are generated when the data is loaded from the receive shift register into the receive data register (SPIRD).

##### Sequential-mode reception

The RFUL interrupt is generated by the following two conditions: One is when the size of data stored into the receive FIFO reaches 16 bytes, and the other is when it reaches 32 bytes.

The REND interrupt is generated when the 32-byte receive FIFO becomes full.

## (3-1) SPI Status Register (SPIST)

The SPIST register contains three bits that indicates the status of data communication.

| SPIST Register   |             |    |    |    |                                                                                |    |                                                                                                                    |                                                                                                                              |
|------------------|-------------|----|----|----|--------------------------------------------------------------------------------|----|--------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------|
| SPIST<br>(0824H) | 7           | 6  | 5  | 4  | 3                                                                              | 2  | 1                                                                                                                  | 0                                                                                                                            |
|                  | Bit Symbol  |    |    |    | TEMP                                                                           |    | TEND                                                                                                               | REND                                                                                                                         |
|                  | Read/Write  |    |    |    | R                                                                              |    | R                                                                                                                  |                                                                                                                              |
|                  | Reset State |    |    |    | 1                                                                              |    | 1                                                                                                                  | 0                                                                                                                            |
| (0825H)          | Function    |    |    |    | Transmit<br>FIFO<br>Status<br>0: No empty<br>space<br>1: Has an<br>empty space |    | Transmission<br>Status<br>0: Transmission<br>in progress<br>or having<br>transmit data<br>1: Transmission<br>ended | Reception<br>Status<br>0: Reception<br>in progress<br>or not having<br>receive data<br>1: Reception<br>Ended or<br>FIFO full |
|                  | 15          | 14 | 13 | 12 | 11                                                                             | 10 | 9                                                                                                                  | 8                                                                                                                            |
|                  | Bit Symbol  |    |    |    |                                                                                |    |                                                                                                                    |                                                                                                                              |
|                  | Read/Write  |    |    |    |                                                                                |    |                                                                                                                    |                                                                                                                              |
| (0825H)          | Reset State |    |    |    |                                                                                |    |                                                                                                                    |                                                                                                                              |
|                  | Function    |    |    |    |                                                                                |    |                                                                                                                    |                                                                                                                              |

Figure 3.17.9 SPIST Register

## (a) TEMP

For UNIT-mode transmission, this bit is cleared to “0” when the transmit register (SPITD) contains valid data; otherwise, it is set to “1”.

For Sequential-mode transmission, this bit is set to “1” when the transmit FIFO buffer contains no valid data.

## (b) TEND

This bit is cleared to “0” when the SPITD register or the transmit FIFO contains valid transmit data, and also when the transmission is in progress. This bit is set to “1” after completing the data transmission where the SPITD register and the transmit FIFO contain no valid data.

## (c) REND

For UNIT-mode reception, this bit is set to “1” when completing the data reception and valid data is stored into the receive data register (if there is any valid data). This bit is cleared to “0” when the receive register (SPIRD) contains no valid data, or when the reception is in progress.

For Sequential-mode reception, this bit is set to “1” when the 32-byte receive FIFO is full with the valid data after completing the reception of the last data. This bit is cleared to “0” when there is still an empty space of one byte or more in the FIFO.

The RFUL flag does not exist because its function is exactly the same as the REND flag.

## (3-2) SPI Interrupt Enable Register (SPIE)

The SPIE register enables or disables the generation of four types of interrupts.

| SPIE Register   |             |    |    |    |                                            |                                            |                                            |                                            |
|-----------------|-------------|----|----|----|--------------------------------------------|--------------------------------------------|--------------------------------------------|--------------------------------------------|
| SPIE<br>(082CH) | 7           | 6  | 5  | 4  | 3                                          | 2                                          | 1                                          | 0                                          |
|                 | Bit Symbol  |    |    |    | TEMPIE                                     | RFULIE                                     | TENDIE                                     | RENDIE                                     |
|                 | Read/Write  |    |    |    | R/W                                        |                                            |                                            |                                            |
|                 | Reset State |    |    |    | 0                                          | 0                                          | 0                                          | 0                                          |
| (082DH)         | Function    |    |    |    | TEMP<br>interrupt<br>0:Disable<br>1:Enable | RFUL<br>interrupt<br>0:Disable<br>1:Enable | TEND<br>interrupt<br>0:Disable<br>1:Enable | REND<br>interrupt<br>0:Disable<br>1:Enable |
|                 |             | 15 | 14 | 13 | 12                                         | 11                                         | 10                                         | 9                                          |
|                 | Bit Symbol  |    |    |    |                                            |                                            |                                            |                                            |
|                 | Read/Write  |    |    |    |                                            |                                            |                                            |                                            |
|                 | Reset State |    |    |    |                                            |                                            |                                            |                                            |
|                 | Function    |    |    |    |                                            |                                            |                                            |                                            |
|                 |             |    |    |    |                                            |                                            |                                            |                                            |
|                 |             |    |    |    |                                            |                                            |                                            |                                            |

Figure 3.17.10 SPIE Register

## (a) TEMPIE

This bit enables or disables the TEMP interrupt.

## (b) RFULIE

This bit enables or disables the RFUL interrupt.

## (c) TENDIE

This bit enables or disables the TEND interrupt.

## (d) RENDIE

This bit enables disables the REND interrupt.

Note: The SPIC supports four types of interrupts; two transmit interrupts (TEMP, and TEND, both of which causes the generation of the INTSPITX interrupt request) and two receive interrupts (RFUL and REND, both of which causes the generation of the INTSPIRX interrupt request). However, for the proper operation, select either one of the TEMP and TEND interrupts and also select either one of the RFUL and REND interrupts. (Simultaneous use of the TEMP and TEND interrupts is prohibited, as well as the simultaneous usage of the RFUL and REND interrupts.)

## (4) SPI CRC Register (SPICR)

The SPICR register contains the CRC calculation result for transmit/receive data.

| SPICR Register   |             |                        |        |        |        |        |        |       |
|------------------|-------------|------------------------|--------|--------|--------|--------|--------|-------|
| SPICR<br>(0826H) | Bit Symbol  | CRCD7                  | CRCD6  | CRCD5  | CRCD4  | CRCD3  | CRCD2  | CRCD1 |
|                  | Read/Write  | R                      |        |        |        |        |        |       |
|                  | Reset State | 0                      | 0      | 0      | 0      | 0      | 0      | 0     |
|                  | Function    | CRC result bits [7:0]  |        |        |        |        |        |       |
| (0827H)          |             | 15                     | 14     | 13     | 12     | 11     | 10     | 9     |
|                  | Bit Symbol  | CRCD15                 | CRCD14 | CRCD13 | CRCD12 | CRCD11 | CRCD10 | CRCD9 |
|                  | Read/Write  | R                      |        |        |        |        |        |       |
|                  | Reset State | 0                      | 0      | 0      | 0      | 0      | 0      | 0     |
|                  | Function    | CRC result bits [15:8] |        |        |        |        |        |       |

Figure 3.17.11 SPICR Register

## (a) CRCD15:0

The CRC result which is calculated according to the settings of the CRC16\_7\_b, CRCRX\_TX\_B and CRCRESET\_B bits in the SPICR register are loaded into this register. When using the CRC16 algorithm, all the bits participate in the CRC generation. When using the CRC7 algorithm, only the lower seven bits participate in the CRC generation. The following describes the steps required to calculate the CRC16 for the transmit data.

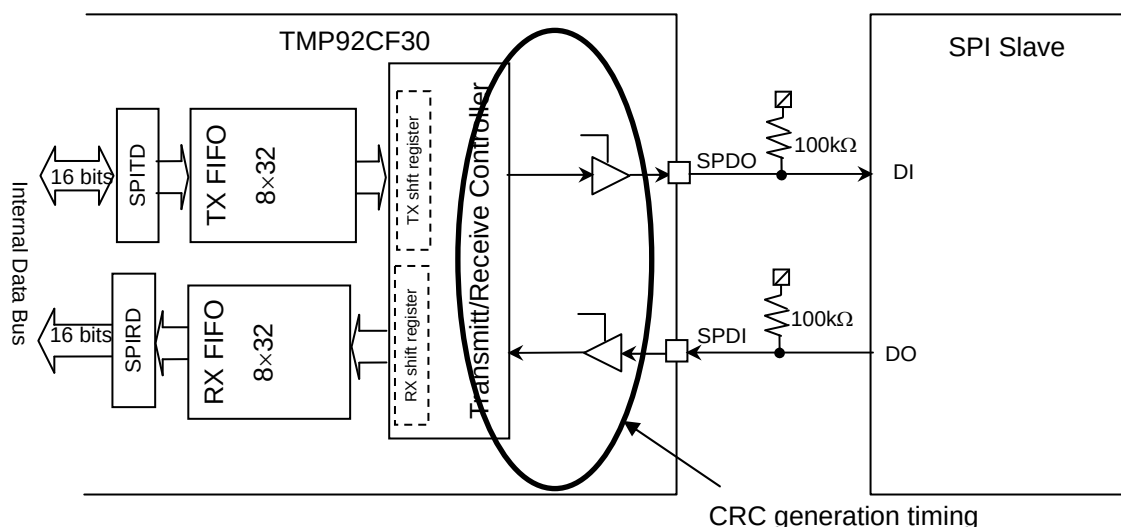
First, initialize the CRC calculation register by writing a “1” to the CRCRESET\_B bit after programming three bits as follows: CRC16\_7\_b = “1”, CRCRX\_TX\_B = “0”, and CRCRESET\_B = “0”.

Then, by writing the transmit data into the SPITD register, complete the transmission of all bits, for which the CRC should be calculated.

The SPIST<TEND> bit should be checked to confirm whether the reception is completed.

By reading the SPICR register after the transmission is completed, the CRC16 for the transmit data can be obtained.

Note: The CRC is generated upon data input and output of the TMP92CF30 as illustrated below. The timing of the CRC comparison should be fully considered when performing Sequential-mode transmit and receive operation using the FIFOs.



## (5) SPI Transmit Data Register (SPITD)

The SPITD0 and SPITD1 registers are used for writing the transmit data.

SPITD0 Register

|                   |             |                           |       |       |       |       |       |      |      |
|-------------------|-------------|---------------------------|-------|-------|-------|-------|-------|------|------|
| SPITD0<br>(0830H) |             | 7                         | 6     | 5     | 4     | 3     | 2     | 1    | 0    |
|                   | Bit Symbol  | TXD7                      | TXD6  | TXD5  | TXD4  | TXD3  | TXD2  | TXD1 | TXD0 |
|                   | Read/Write  | R/W                       |       |       |       |       |       |      |      |
|                   | Reset State | 0                         | 0     | 0     | 0     | 0     | 0     | 0    | 0    |
|                   | Function    | Transmit data bits [7:0]  |       |       |       |       |       |      |      |
| (0831H)           |             | 15                        | 14    | 13    | 12    | 11    | 10    | 9    | 8    |
|                   | Bit Symbol  | TXD15                     | TXD14 | TXD13 | TXD12 | TXD11 | TXD10 | TXD9 | TXD8 |
|                   | Read/Write  | R/W                       |       |       |       |       |       |      |      |
|                   | Reset State | 0                         | 0     | 0     | 0     | 0     | 0     | 0    | 0    |
|                   | Function    | Transmit data bits [15:8] |       |       |       |       |       |      |      |

SPITD1 Register

|                   |             |                           |       |       |       |       |       |      |      |
|-------------------|-------------|---------------------------|-------|-------|-------|-------|-------|------|------|
| SPITD1<br>(0832H) |             | 7                         | 6     | 5     | 4     | 3     | 2     | 1    | 0    |
|                   | Bit Symbol  | TXD7                      | TXD6  | TXD5  | TXD4  | TXD3  | TXD2  | TXD1 | TXD0 |
|                   | Read/Write  | R/W                       |       |       |       |       |       |      |      |
|                   | Reset State | 0                         | 0     | 0     | 0     | 0     | 0     | 0    | 0    |
|                   | Function    | Transmit data bits [7:0]  |       |       |       |       |       |      |      |
| (0833H)           |             | 15                        | 14    | 13    | 12    | 11    | 10    | 9    | 8    |
|                   | Bit Symbol  | TXD15                     | TXD14 | TXD13 | TXD12 | TXD11 | TXD10 | TXD9 | TXD8 |
|                   | Read/Write  | R/W                       |       |       |       |       |       |      |      |
|                   | Reset State | 0                         | 0     | 0     | 0     | 0     | 0     | 0    | 0    |
|                   | Function    | Transmit data bits [15:8] |       |       |       |       |       |      |      |

Figure 3.17.12 SPITD Register

This register is used for writing the transmit data. When this register is read, the last-written data is read out. This register is overwritten if the next data is written with the transmit FIFO being full.

Since the transmit data registers can contain data of up to four bytes, it can support write operations that are performed by using four-byte instructions, such as the parallel operation of the SPI and DMA.

When writing the data, the transmit data at the address 830 must always be the first to be written.

There are several restrictions of the data writing methods (i.e., instructions to be used). For more details, please refer to the following table.

| Transmit Data Write Size | Instruction Example | UNIT-mode Transmission (FIFO Disabled) |                                   | Sequential-mode Transmission (FIFO Enabled) |                                   |
|--------------------------|---------------------|----------------------------------------|-----------------------------------|---------------------------------------------|-----------------------------------|
|                          |                     | 1-byte transmission<br>unit16 = 0      | 2-byte transmission<br>unit16 = 1 | 1-byte transmission<br>unit16 = 0           | 2-byte transmission<br>unit16 = 1 |
| 1-byte write             | ld (0x830),a        | ○                                      | ●                                 | Prohibited                                  | ●                                 |
| 2-byte write             | ld (0x830),wa       | ●                                      | ○                                 | ○                                           | ○                                 |
| 4-byte write             | ld (0x830),xwa      | ●                                      | ●                                 | ○                                           | ○                                 |

○: All data that are written by the CPU are transmitted.

●: Invalid data are also transmitted along with the data written by the CPU.

## (6) SPI Receive Data Register (SPIRD)

The SPIRD0 and SPIRD1 registers are used for reading the received data.

| SPIRD0 Register   |             |                          |       |       |       |       |       |      |
|-------------------|-------------|--------------------------|-------|-------|-------|-------|-------|------|
| SPIRD0<br>(0834H) | Bit Symbol  | RXD7                     | RXD6  | RXD5  | RXD4  | RXD3  | RXD2  | RXD1 |
|                   | Read/Write  | R                        |       |       |       |       |       |      |
|                   | Reset State | 0                        | 0     | 0     | 0     | 0     | 0     | 0    |
|                   | Function    | Receive data bits [7:0]  |       |       |       |       |       |      |
| (0835H)           | Bit Symbol  | RXD15                    | RXD14 | RXD13 | RXD12 | RXD11 | RXD10 | RXD9 |
|                   | Read/Write  | R                        |       |       |       |       |       |      |
|                   | Reset State | 0                        | 0     | 0     | 0     | 0     | 0     | 0    |
|                   | Function    | Receive data bits [15:8] |       |       |       |       |       |      |

| SPIRD1 Register   |             |                          |       |       |       |       |       |      |
|-------------------|-------------|--------------------------|-------|-------|-------|-------|-------|------|
| SPIRD1<br>(0836H) | Bit Symbol  | RXD7                     | RXD6  | RXD5  | RXD4  | RXD3  | RXD2  | RXD1 |
|                   | Read/Write  | R                        |       |       |       |       |       |      |
|                   | Reset State | 0                        | 0     | 0     | 0     | 0     | 0     | 0    |
|                   | Function    | Receive data bits [7:0]  |       |       |       |       |       |      |
| (0837H)           | Bit Symbol  | RXD15                    | RXD14 | RXD13 | RXD12 | RXD11 | RXD10 | RXD9 |
|                   | Read/Write  | R                        |       |       |       |       |       |      |
|                   | Reset State | 0                        | 0     | 0     | 0     | 0     | 0     | 0    |
|                   | Function    | Receive data bits [15:8] |       |       |       |       |       |      |

Figure 3.17.13 SPIRD Register

This register is used for reading the received data. Please check the state of the RFUL or REND bit before starting a read operation.

Since the receive data registers can contain data of up to four bytes, it can support read operations that are performed by using four-byte instructions, such as the parallel operation of the SPI and DMA.

When reading the data, the receive data at the address 834 should be the first to be read. (There are some exceptions.)

There are several restrictions of the data reading methods (i.e., instructions to be used). For mode details, please refer to the following table.

| Receive Data Read Size | Instruction Example | UNIT-mode Reception (FIFO Disabled) |                                | Sequential-mode Reception (FIFO Enabled) |                                |
|------------------------|---------------------|-------------------------------------|--------------------------------|------------------------------------------|--------------------------------|
|                        |                     | 1-byte reception<br>unit16 = 0      | 2-byte reception<br>unit16 = 1 | 1-byte reception<br>unit16 = 0           | 2-byte reception<br>unit16 = 1 |
| 1-byte read            | ld a,(0x834)        | ○                                   | ○                              | Prohibited                               | Prohibited                     |
|                        | ld a,(0x835)        | ●                                   | ○                              | Prohibited                               | Prohibited                     |
| 2-byte read            | ld wa,(0x834)       | ◆*1                                 | ○                              | ○                                        | ○                              |
| 4-byte read            | ld xwa,(0x834)      | ◆*2                                 | ◆*3                            | ○                                        | ○                              |

○: Only the valid data are read when the CPU is reading.

◆: Valid data + invalid data are read when the CPU is reading. Invalid data must be deleted later.

●: Only the invalid data are read when the CPU is reading.

\*1: Address 834 = Valid data, address 835 = Invalid data,

\*2: Address 834 = Valid data, address 835 = Invalid data, address 836 = Invalid data, address 837 = Invalid data

\*3: Address 834 = Valid data, address 835 = Valid data, address 836 = Invalid data, address 837 = Invalid data



### 3.17.3 Notes on the Operations Using the FIFO Buffers

Things to be noted when using the SPIC are as follows:

#### 1) Transmission

The transmit FIFO buffer is overwritten if the new data is written with the transmit FIFO buffer being full. Also, since the FIFO write pointer does not point to the correct write position, interrupts and transmissions are not properly executed. Therefore, the number of writes should be controlled by using software.

In the Sequential-mode transmission, the data writes to the transmit FIFO must be performed in 16-byte units. Otherwise, the TEMP interrupt is not properly generated.

Note: For data transmission in units of other than 16 bytes, UNIT mode must be selected.

#### 2) Reception

If a read operation is performed when the receive FIFO is empty, undefined data is read. Also, since the FIFO read pointer does not point to the correct read position, interrupts and receptions are not properly executed. Therefore, the number of reads should be controlled by using software.

In the Sequential-mode reception, the data reads from the receive FIFO must be performed in 16-byte units. Otherwise, the RFUL interrupt is not properly generated.

Note: For data reception in units of other than 16 bytes, UNIT mode must be selected.

#### 3) CRC

The CRC is generated upon transmission and reception to/from the SPI slave device. (Refer to the section on the SPICRC register for more details.) The timing of the CRC comparison should be fully considered when performing Sequential-mode transmit and receive operation using the FIFOs.

Example: Sequential-mode reception

1. Start Sequential-mode reception
2. finish valid data receive (FIFO\_Full)
3. Stop data reception
4. Read valid data from the FIFO to a temporary buffer (internal RAM, etc.)
5. Read CRC1 from the CRC generator in the SPIC
6. Start CRC2 reception (upon UNIT-mode reception from the SD-CARD)
7. Compare CRC1 and CRC2

Note: The steps 2 to 4 of the above sequence can be used DMAC. However, to perform the CRC comparison, the receive operation must be stopped once as described in step 3. Otherwise, the CRC1 value obtained from the internal CRC generator unintentionally contains CRC2 as well as the valid data, which leads to an incorrect CRC comparison.

### 3.18 I<sup>2</sup>S (Inter-IC Sound)

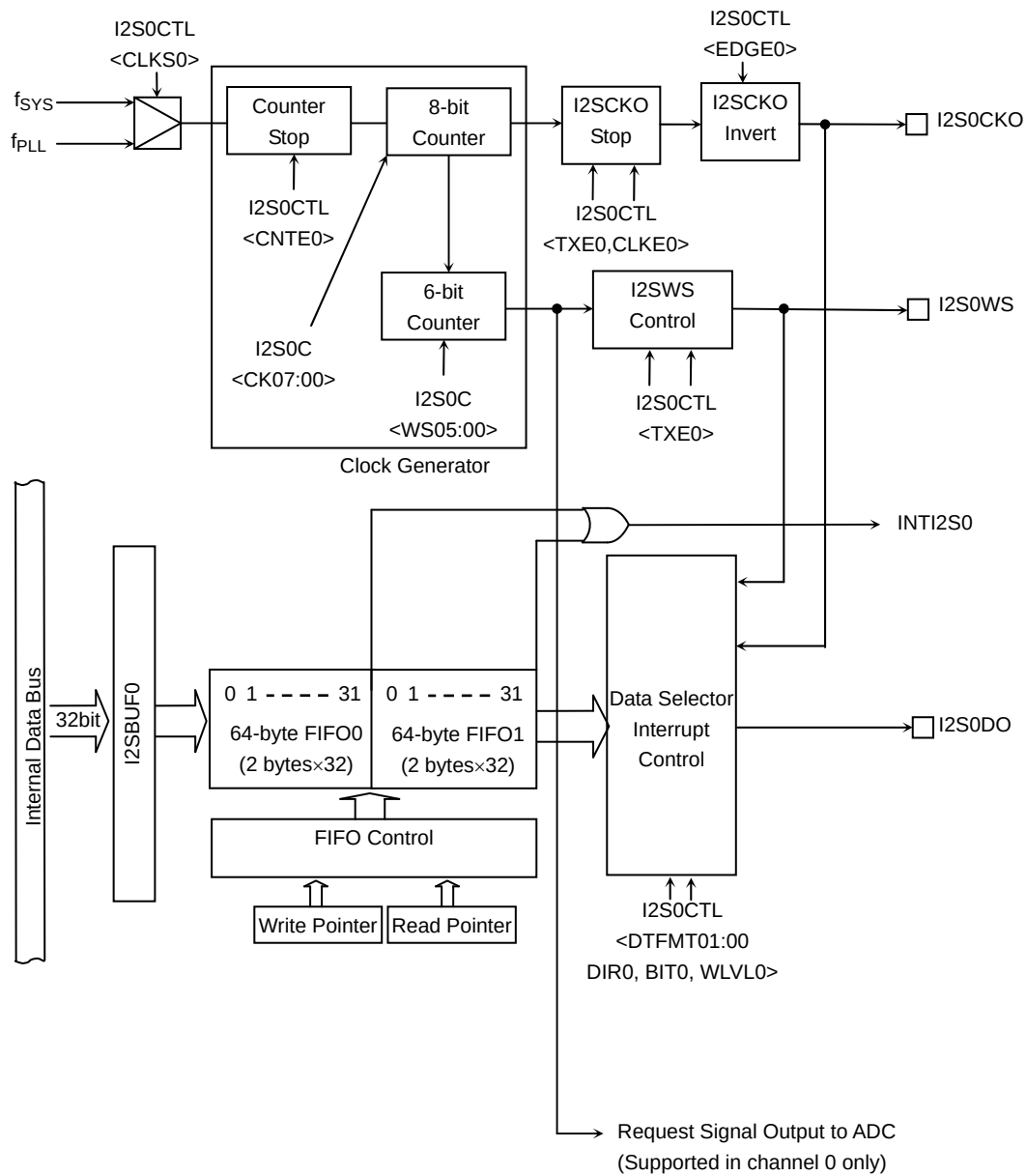
The TMP92CF30 incorporates serial output circuitry that is compliant with the I<sup>2</sup>S format. This function enables the TMP92CF30 to be used for digital audio systems by connecting an LSI for audio output such as a DA converter.

The I<sup>2</sup>S unit has the following features:

Table 3.18.1 I<sup>2</sup>S Operation Features

| Item                | Description                                                                                                                                |
|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------|
| Number of Channels  | 1 channel                                                                                                                                  |
| Format              | I <sup>2</sup> S-format compliant<br>Right-justified and left-justified formats supported<br>Stereo / monaural<br>Master transmission only |
| Pins used           | 1. I2S0CKO (clock output)<br>2. I2S0DO (output)<br>3. I2S0WS (Word Select output)                                                          |
| WS frequency        | Refer to "Setting the transfer clock generator and Word Select signal".                                                                    |
| Data transfer rate  |                                                                                                                                            |
| Transmission buffer | 64 bytes × 2                                                                                                                               |
| Direction of data   | MSB-first or LSB-first selectable                                                                                                          |
| Data length         | 8 bits or 16 bits                                                                                                                          |
| Clock edge          | Rising edge or falling edge                                                                                                                |
| Interrupt           | INTI2S0<br>(64-byte FIFO empty interrupt)                                                                                                  |

## 3.18.1 Block Diagram

Figure 3.18.1 I<sup>2</sup>S Block Diagram

## 3.18.2 SFRs

The I<sup>2</sup>S unit is provided with the following registers. These registers are connected to the CPU via a 32-bit data bus. The transmission buffers I2S0BUF must be accessed using 4-byte load instructions.

I<sup>2</sup>S0 Control Register

|                    | 7           | 6                                                             | 5                                          | 4                                               | 3                                                   | 2                                                                        | 1                                                    | 0                                                                          |
|--------------------|-------------|---------------------------------------------------------------|--------------------------------------------|-------------------------------------------------|-----------------------------------------------------|--------------------------------------------------------------------------|------------------------------------------------------|----------------------------------------------------------------------------|
| I2S0CTL<br>(1808H) | bit Symbol  | TXE0                                                          | *CNTE0                                     | DIR0                                            | BIT0                                                | DTFMT01                                                                  | DTFMT00                                              | SYSCKE0                                                                    |
|                    | Read/Write  | R/W                                                           |                                            | R/W                                             |                                                     |                                                                          |                                                      |                                                                            |
|                    | Reset State | 0                                                             | 0                                          | 0                                               | 0                                                   | 0                                                                        | 0                                                    | 0                                                                          |
|                    | Function    | Transmission<br>0: Stop<br>1: Start                           | Counter<br>control<br>0: Clear<br>1: Start | Transmission<br>start bit<br>0: MSB<br>1: LSB   | Bit length<br>0: 8 bits<br>1: 16 bits               | Output format<br>00: I <sup>2</sup> S 10: Right<br>01: Left 11: Reserved |                                                      | System<br>clock<br>0: Disable<br>1: Enable                                 |
|                    | 15          | 14                                                            | 13                                         | 12                                              | 11                                                  | 10                                                                       | 9                                                    | 8                                                                          |
| (1809H)            | bit Symbol  | CLKS0                                                         |                                            | FSEL0                                           | TEMP0                                               | WLVLO                                                                    | EDGE0                                                | CLKE0                                                                      |
|                    | Read/Write  | R/W                                                           |                                            | R/W                                             | R                                                   | R/W                                                                      |                                                      |                                                                            |
|                    | Reset State | 0                                                             |                                            | 0                                               | 1                                                   | 0                                                                        | 0                                                    | 0                                                                          |
|                    | Function    | Source<br>clock<br>0: f <sub>SYS</sub><br>1: f <sub>PLL</sub> |                                            | Stereo<br>/monaural<br>0: Stereo<br>1: Monaural | Transmission<br>FIFO state<br>0: Data<br>1: No data | WS level<br>0: Low left<br>1: High left                                  | Data output<br>clock edge<br>0: Falling<br>1: Rising | Clock<br>operation<br>(after trans-<br>mission)<br>0: Enable<br>1: Disable |

I<sup>2</sup>S0 Divider Value Setting Register

|                  | 7           | 6                                           | 5    | 4                                           | 3    | 2    | 1    | 0    |
|------------------|-------------|---------------------------------------------|------|---------------------------------------------|------|------|------|------|
| I2S0C<br>(180AH) | bit Symbol  | CK07                                        | CK06 | CK05                                        | CK04 | CK03 | CK02 | CK01 |
|                  | Read/Write  | R/W                                         |      |                                             |      |      |      |      |
|                  | Reset State | 0                                           | 0    | 0                                           | 0    | 0    | 0    | 0    |
|                  | Function    | Divider value for CK signal (8-bit counter) |      |                                             |      |      |      |      |
|                  | 15          | 14                                          | 13   | 12                                          | 11   | 10   | 9    | 8    |
| (180BH)          | Bit symbol  |                                             |      | WS05                                        | WS04 | WS03 | WS02 | WS01 |
|                  | Read/Write  |                                             |      | R/W                                         |      |      |      |      |
|                  | Reset State |                                             |      | 0                                           | 0    | 0    | 0    | 0    |
|                  | Function    |                                             |      | Divider value for WS signal (6-bit counter) |      |      |      |      |

I<sup>2</sup>S0 Buffer Register

|                                                                    | 15          | 14                                  | 13   | 12   | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|--------------------------------------------------------------------|-------------|-------------------------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| I2S0BUF<br>(1800H)                                                 | bit Symbol  | B015                                | B014 | B013 | B012 | B011 | B010 | B009 | B008 | B007 | B006 | B005 | B004 | B003 | B002 | B001 |
|                                                                    | Read/Write  | W                                   |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|                                                                    | Reset State | Undefined                           |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|                                                                    | Function    | Transmission buffer register (FIFO) |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|                                                                    | 31          | 30                                  | 29   | 28   | 27   | 26   | 25   | 24   | 23   | 22   | 21   | 20   | 19   | 18   | 17   | 16   |
| A read-<br>modify-<br>write<br>operation<br>cannot be<br>performed | bit Symbol  | B031                                | B030 | B029 | B028 | B027 | B026 | B025 | B024 | B023 | B022 | B021 | B020 | B019 | B018 | B017 |
|                                                                    | Read/Write  | W                                   |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|                                                                    | Reset State | Undefined                           |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|                                                                    | Function    | Transmission buffer register (FIFO) |      |      |      |      |      |      |      |      |      |      |      |      |      |      |

Figure 3.18.2 I<sup>2</sup>S Channel 0 Control Registers

## (a) &lt;SYSCKE0&gt;

This bit controls to connect source clock to I<sup>2</sup>S circuit.

In case of this circuit is operated, it must enable: <SYSCKE0>= "1". And except operating, for reduce the power consumption, we recommends to disable: <SYSCKE0>= "0".

## (b) &lt;DTFMT01:00&gt;

This bit controls data format: I<sup>2</sup>S, right justify and left justify.

It is not possible to change data format during data transmission. Before changing the data format, set <SYSCKE0>= "1", <CNTE0>= "0" and <TXE0>= "0".

## (c) &lt;BIT0&gt;

This bit controls data length: 8/16 bits.

It is not possible to change data length during data transmission. Before changing the data format, set <SYSCKE0>= "1", <CNTE0>= "0" and <TXE0>= "0".

## (d) &lt;DIR0&gt;

This bit controls direction: LSB\_Fast or MSB\_Fast

It is not possible to change data direction during data transmission. Before changing the data format, set <SYSCKE0>= "1", <CNTE0>= "0" and <TXE0>= "0".

## (e) &lt;CNTE0&gt;

This bit controls clock generator counter: Clear/Start.

When this circuit is used, always set to the start condition.

Clock generator counter will clear by <TXE0>= "0" and <CNTE0>= "0", However, Clock generator counter will not clear by <TXE0>= "0" and <CNTE0>= "1"

## (f) &lt;TXE0&gt;

This bit controls data transmission and FIFO buffer clear: Trans/Stop and Clear Transmission is stopped by <TXE0>= "0", started by <TXE0>= "1".

Output FIFO buffer is cleared by <TXE0>= "0".

## (g) &lt;CLKE0&gt;

This bit controls CLK out period.

<CLKE0>= "0": always out I2S0CKO clock, <CLKE0>= "1": I2S0CKO clock out during effective data out period.

Note: In case of I<sup>2</sup>S format, firstly I2S0WS signal change and after 1clock period, effective data out. If set to <CLKE0>= "1" with I<sup>2</sup>S format, 1 clock pulse after I2S0WS don't out. It is not possible <CLKE0>= "0" setting with I<sup>2</sup>S format.

## (h) &lt;EDGE0&gt;

This bit controls relation of phase between I2S0CKO and data.

<EDGE0>="0": the data is changed in the falling of clock, and the data is latched in the rising edge of clock.

<EDGE0>="1": the data is changed in the rising of clock, and the data is latched the falling edge of clock.

It is not possible to change phase during data transmission. Before changing the data format, set <SYSCKE0>="1", <CNTE0>="0" and <TXE0>="0".

## (i) &lt;WLVL0&gt;

This bit controls phase of Word Select signal: I2S0WS

I2S0WS signal always out "1" level first. The order of data output changes by <WLVL0>. Refer the "FIFO buffer and data format" in details.

It is not possible to change phase of Word Select signal during data transmission. Before changing the data format, set <SYSCKE0>="1", <CNTE0>="0" and <TXE0>="0".

## (j) &lt;TEMP0&gt;

This bit is empty flag of output FIFO buffer.

<TEMP0>="1": FIFO buffer is empty, <TEMP0>="0": remain data in FIFO buffer.

This bit is read only. FIFO buffer is cleared by <TXE0>="0"

## (k) &lt;FSEL0&gt;

This bit controls sound mode: Stereo / Monaural

<FSEL0>="0": Stereo, <FSEL0>="1": Monaural. Refer the chapter of "Data format" in details.

It is not possible to change sound mode during data transmission. Before changing the data format, set <SYSCKE0>="1", <CNTE0>="0" and <TXE0>="0".

## (l) &lt;CLKS0&gt;

This bit controls source clock to I<sup>2</sup>S circuit: f<sub>SYS</sub> / f<sub>PLL</sub>.

<CLKS0>="0": f<sub>SYS</sub> is supplied, <CLKS0>="1": f<sub>PLL</sub> is supplied.

In case of using f<sub>PLL</sub>, before set f<sub>PLL</sub> clock, please take care set-up time: Lock-Up time. In details, refer the chapter of PLL, please.

## (m) &lt;CK07:00&gt;

These bits are set counter value of clock generator. [I2S0CK]

It is not possible to change these counter value during data transmission. Before changing the counter value, set <SYSCKE0>="1", <CNTE0>="0" and <TXE0>="0".

## (n) &lt;WS05:00&gt;

These bits are set counter value of clock generator. [I2S0WS]

It is not possible to change these counter value during data transmission. Before changing the counter value, set <SYSCKE0>="1", <CNTE0>="0" and <TXE0>="0".

### 3.18.3 Description of Operation

#### (1) Settings the transfer clock generator and Word Select signal

In the I<sup>2</sup>S unit, the clock frequencies for the I2S0CKO and I2S0WS signals are generated using the system clock ( $f_{\text{SYS}}$ ) as a source clock. The system clock is divided by a prescaler and a dedicated clock generator to set the transfer clock and sampling frequency.

The counters are started by setting I2S0CTL<CNTE0> to “1” and are stopped and cleared by setting <CNTE0> to “0”.

##### A) Clock generator

- 8-bit counter

This is an 8-bit counter that generates the I2S0CKO signal by dividing the clock selected by I2S0CTL<CLKS0>.

- 6-bit counter

This is a 6-bit counter that generates the I2S0WS signal by dividing the I2S0CKO signal.

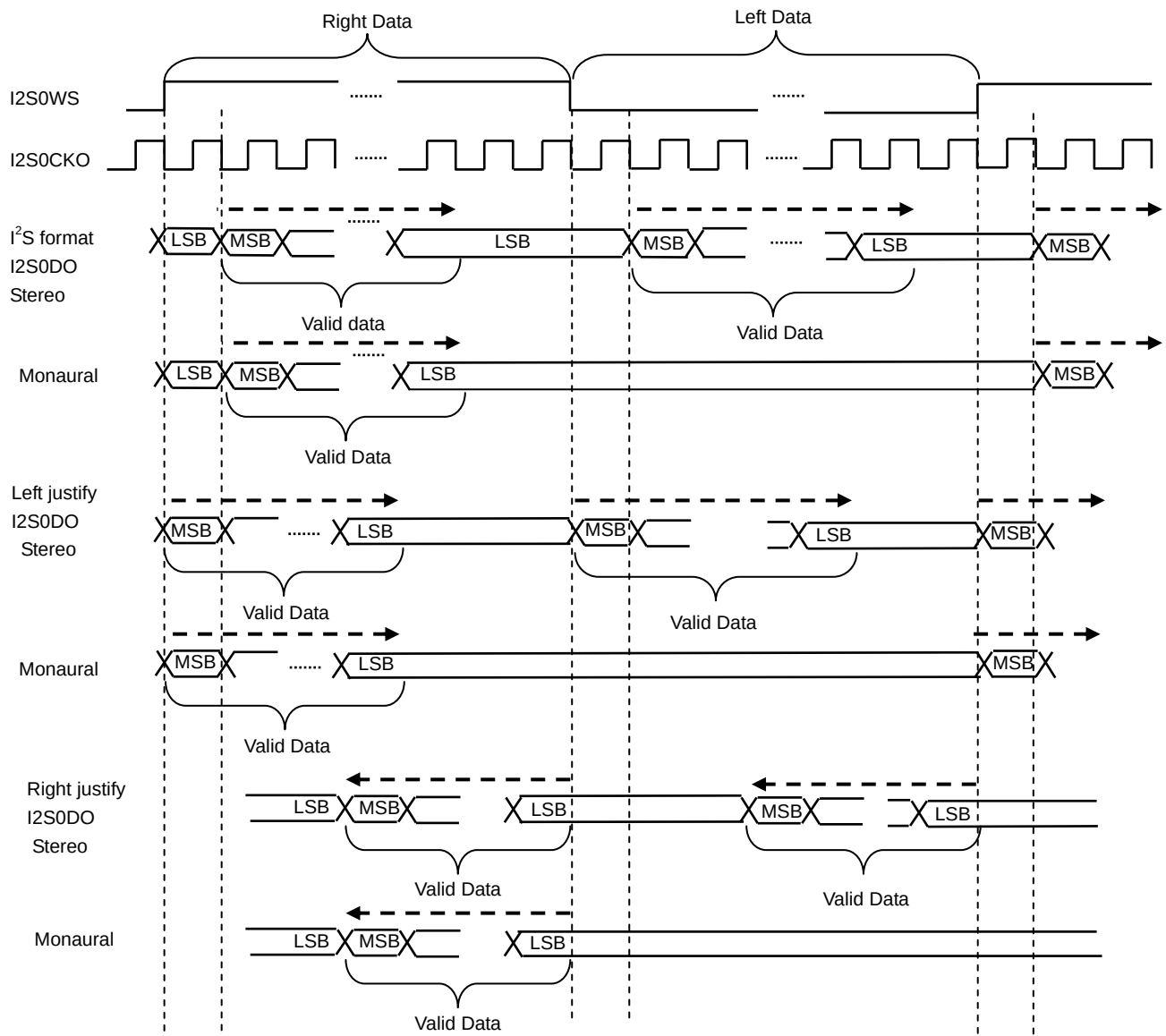
##### B) Word Select

- Word Select signal (I2S0WS)

The I2S0WS signal is used to distinguish the position of valid data and whether left data or right data is being transmitted in the I<sup>2</sup>S format. This signal is clocked out in synchronization with the data transfer clock. In only channel 0, this signal can be used as an AD conversion trigger signal for the ADC. How valid data is to be output in relation to the WS signal can be specified as I<sup>2</sup>S format, left-justified, or right-justified. In only channel 0, an interrupt request can be output to the ADC on the rising edge of the WS signal. (This is controlled by the ADC's control register.)

#### (2) Data format

This circuit support I<sup>2</sup>S format, left justify and right justify format by setting I2S0CTL<DTFMT01:00> register. And support stereo and monaural both, controlled by I2S0CTL<FSEL0> register.



Note: When Monaural is set, Right data and Left data output the same-signal. When Stereo is set, the data of FIFO buffer is renewed every one-word. However, when Monaural is set, it is renewed to the next data after the same-data is transmitted two times.

When Monaural is set, it output the same-data to Right and Left, without the same-data written to the FIFO buffer.

The Monaural function of TMP92CZ26A/CF26A and TMP92CF30 is different.

The Monaural function of TMP92CZ26A/CF26A is one of channels only.

Figure3.18.3 Output Format



## (3) Setting example for the clock generator (8-bit counter/6-bit counter)

The clock generator generates the reference clock for setting the data transfer speed and sampling frequency.

|                  |             | 7                                           | 6    | 5                                           | 4    | 3    | 2    | 1    | 0    |
|------------------|-------------|---------------------------------------------|------|---------------------------------------------|------|------|------|------|------|
| I2S0C<br>(180AH) | bit Symbol  | CK07                                        | CK06 | CK05                                        | CK04 | CK03 | CK02 | CK01 | CK00 |
|                  | Read/Write  | R/W                                         |      |                                             |      |      |      |      |      |
|                  | Reset State | 0                                           | 0    | 0                                           | 0    | 0    | 0    | 0    | 0    |
|                  | Function    | Divider value for CK signal (8-bit counter) |      |                                             |      |      |      |      |      |
|                  |             | 15                                          | 14   | 13                                          | 12   | 11   | 10   | 9    | 8    |
| (180BH)          | Bit symbol  |                                             |      | WS05                                        | WS04 | WS03 | WS02 | WS01 | WS00 |
|                  | Read/Write  |                                             |      | R/W                                         |      |      |      |      |      |
|                  | Reset State |                                             |      | 0                                           | 0    | 0    | 0    | 0    | 0    |
|                  | Function    |                                             |      | Divider value for WS signal (6-bit counter) |      |      |      |      |      |

- Setting the transfer clock I2S0CKO

The transfer clock is generated by dividing the clock selected by I2S0CTL <CLKS0>. An 8-bit counter is provided to divide the source clock by 3 to 256. (The divider value cannot be set to 1 or 2.)

The transfer clock must not exceed 10 MHz. Make sure that the transfer clock is set to within 10 MHz by an appropriate combination of source clock frequency and divider value.

| 8-bit counter set value | Divider value |
|-------------------------|---------------|
| 00000000                | 256           |
| 00000001                | 1             |
| 11111111                | 255           |

When  $f_{\text{SYS}} = 60 \text{ MHz}$  and I2S0C<CK07:00> = 150, the data transfer speed is set as follows:

$$\begin{aligned}
 \text{I2S0CKO} &= f_{\text{SYS}}/150 \\
 &= 60 [\text{MHz}]/150 = 400 [\text{kbps}]
 \end{aligned}$$

Note: It is recommended that the value to be set in I2S0C<CK07:00> be an even number. Although it is possible to set an odd number, the clock duty of the CK signal does not become 50%. Setting an odd number causes the High width of the I2S0CKO signal to become longer by one  $f_{\text{SYS}}$  or  $f_{\text{PLL}}$  pulse than the Low width. (When <EDGE0> = 0, the Low width becomes longer than the High width.)

- Setting the sampling frequency WS

The sampling frequency is set by dividing the transfer clock (CK) described above. A 6-bit counter is provided to divide the transfer clock by 16 to 64. (The divider value cannot be set to 1 to 15.)

| <u>6-bit counter set value</u> | <u>Divider value</u> |
|--------------------------------|----------------------|
| 000000                         | 64                   |
| 000001                         | 1                    |
| 111111                         | 63                   |

When  $f_{\text{SYS}} = 60 \text{ MHz}$ ,  $\text{I2S0C<CK07:00>} = 150$ , and  $\text{I2SnC<WS05:00>} = 50$ , the sampling frequency is set as follows:

$$\begin{aligned} \text{I2S0CKO} &= f_{\text{SYS}} / 150 / 50 \\ &= 60 [\text{MHz}] / 150 / 50 = 8 [\text{kHz}] \end{aligned}$$

Based on the above, the transfer clock is set to 400 kbps, and the sampling frequency is set to 8 kHz in this example.

Note 1: The value to be set in  $\text{I2S0C<WS05:00>}$  must be 16 or larger (18 or larger for  $\text{I}^2\text{S}$  transfer) when the data length is 8 bits and 32 or larger (34 or larger for  $\text{I}^2\text{S}$  transfer) when the data length is 16 bits.

Note 2: It is recommended that the value to be set in  $\text{I2S0C<WS05:00>}$  be an even number. Although it is possible to set an odd number, the clock duty of the WS signal does not become 50%. Setting an odd number causes the High width of the WS signal to become longer by one  $\text{I2S0CKO}$  pulse than the Low width.

- Special function

As a special function available only in channel 0, the rising edge of the WS signal can be used as an AD conversion start trigger for the AD converter in this LSI. Setting  $\text{I2S0CTL<SYSKE0>}=1$  and  $\text{I2S0CTL<CNTE0>}=1$  enables the WS signal to be sent to the AD converter. This can be done regardless of the setting of  $\text{I2S0CTL<TXE0>}$ .

For details about AD conversion using the WS signal, refer to the chapter on the AD converter.

## (4) FIFO buffer and data format

The I<sup>2</sup>S unit is provided with a 128-byte FIFO buffer (32-bit wide × 32-entry). The data written to the 4 bytes (32 bits) of the I2S0BUF register is written to this FIFO buffer. This FIFO must be written in units of 4 bytes. It is also necessary to consider the output order and to distinguish between right data and left data.

To write data to the I2S0BUF register, be sure to use a 4-byte load instruction. If a 1-byte load instruction is used, invalid data will be transmitted. In case of using 1-byte or 2-byte transmission instruction, FIFO buffer isn't renewed and transmission isn't started.

And window addresses are 1800H (channel 0) and 1810H (channel1).

| Write Data Size | Example instruction | 8-bit width | 16-bit width |
|-----------------|---------------------|-------------|--------------|
| 1-byte access   | ld (0x1800),a       | Not allowed | Not allowed  |
| 2-byte access   | ld (0x1800),wa      | Not allowed | Not allowed  |
| 4-byte access   | ld (0x1800),xwa     | OK          | OK           |

Also note that data must be written in units of 64 bytes using the following sequence:

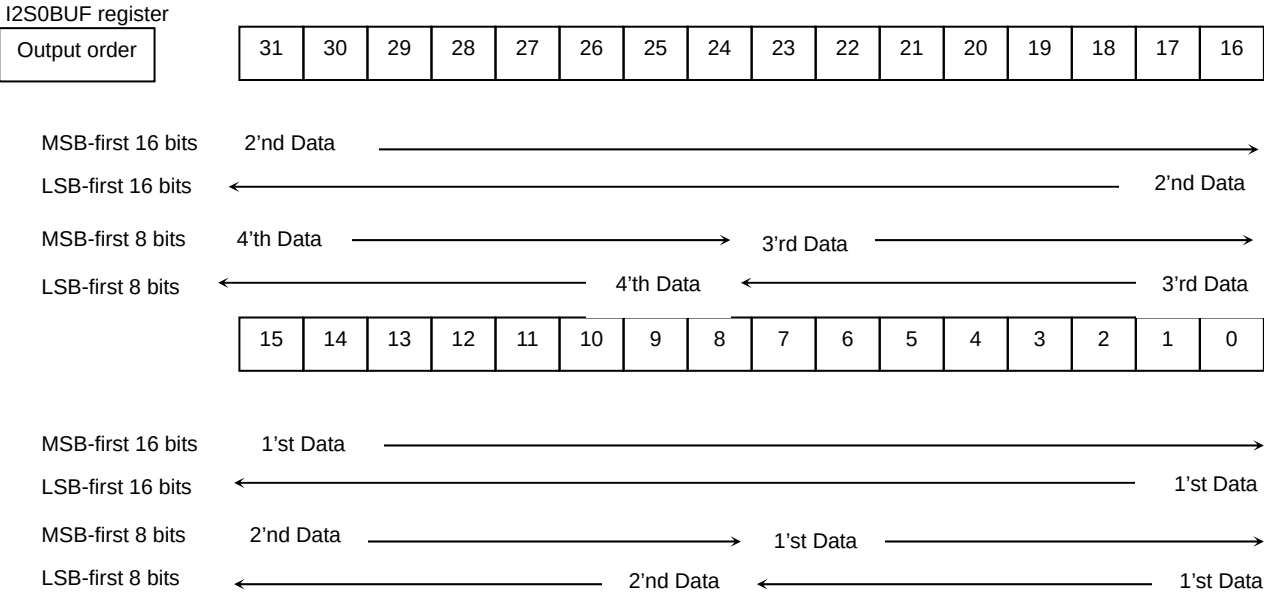
4-byte load instruction × 16 times = 64-byte data write

If data is not written in units of 64 bytes, interrupts cannot be generated at the normal timing.

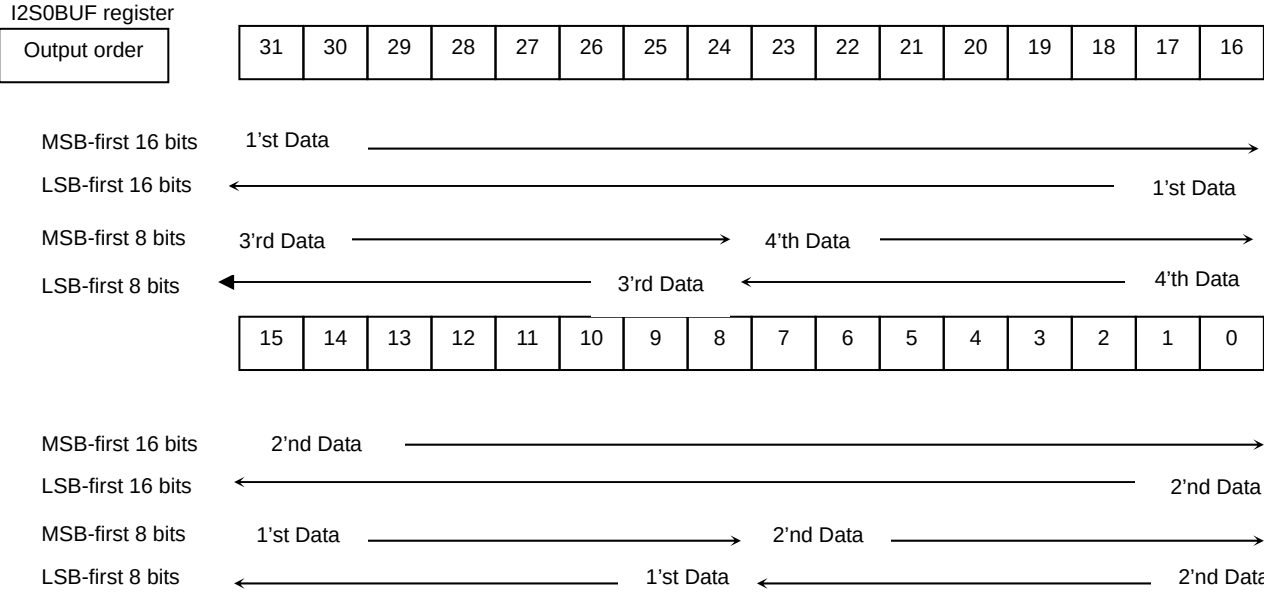
The I2S0CTL<TEMP0> flag is set to “1” when the FIFO buffer for each channel contains no valid data. If there is even one byte of valid data in the FIFO, the flag is cleared to “0”. (The <TEMP0> flag is set to “1” as soon as the last valid data in the FIFO is sent to the transmission shift register.)

The following shows how written data is output under various conditions.

When I2S0CTL<WLVL0> = “0”



When I2S0CTL<WLVL0> = “1”

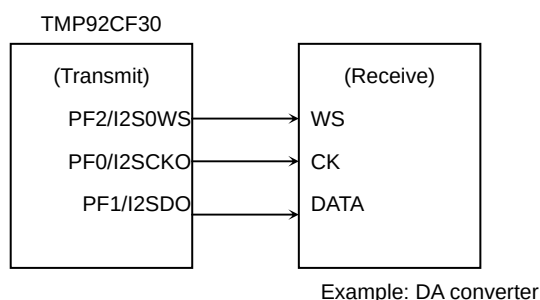


Note: In case of using monaural setting, and change right / left: I2S0CTL<WLVL0>, data output order change off 1'st data and 2'nd data. when Monaural is set, it is renewed to the next data after the same-data is transmitted two times.

### 3.18.4 Detailed Description of Operation

#### (1) Connection example

Figure3.18.4 shows an example of connections between the TMP92CF30 and an external LSI (DA converter) using channel 0.



Note: After reset, PF0 to PF2 are placed in a high-impedance state. Connect each pin with a pull-up or pull-down resistor as necessary.

Figure3.18.4 Connection Example between the TMP92CF30 and an External LSI

#### (2) Operation procedure

The I<sup>2</sup>S unit incorporates a 128-byte FIFO buffer that is divided into two 64-byte units. Whenever each 64-byte buffer space becomes empty, an INTI2S0 interrupt is generated. The next data to be transmitted should be written to the FIFO in the interrupt routine.

Example settings and timing diagram are shown below.

(Example settings) I2S0WS = 8kHz, I2S0CKO = 400kHz, data transmission on the rising edge (at  $f_{SYS} = 60$  MHz)

(Main routine)

|           | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                               |
|-----------|---|---|---|---|---|---|---|---|---------------------------------------------------------------|
| INTEI2S01 | X | – | – | – | X | 0 | 0 | 1 | Set interrupt level.                                          |
| PFCR      | X | X | – | – | – | – | – | – | Set pins: PF0 (I2S0CKO), PF1 (I2S0DO), PF2 (I2S0WS)           |
| PFFC      | – | X | – | – | – | 1 | 1 | 1 |                                                               |
| I2S0C     | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | Divider value N=150                                           |
|           | X | X | 1 | 1 | 0 | 0 | 1 | 0 | Divider value K=50                                            |
| I2S0CTL   | 0 | 0 | X | 0 | 1 | 0 | 0 | 1 | Set transmit mode (I2S mode, MSB-first, 16-bit).              |
|           | 0 | X | X | X | X | 0 | 0 | 0 | Falling edge, WS=0 Left, clock stop.                          |
| I2S0BUF   | * | * | * | * | * | * | * | * | Write left and right data to FIFO (4 bytes × 32 = 128 bytes). |
|           | * | * | * | * | * | * | * | * |                                                               |
|           | * | * | * | * | * | * | * | * |                                                               |
|           | * | * | * | * | * | * | * | * |                                                               |
| I2S0CTL   | 1 | 1 | X | 0 | 1 | 0 | 0 | 1 | Start transmission.                                           |
|           | 0 | X | X | 0 | X | 0 | 0 | 0 |                                                               |

(INTI2S Interrupt Routine)

|         |   |   |   |   |   |   |   |   |                                                              |
|---------|---|---|---|---|---|---|---|---|--------------------------------------------------------------|
| I2S0BUF | * | * | * | * | * | * | * | * | Write left and right data to FIFO (4 bytes × 16 = 64 bytes). |
|         | * | * | * | * | * | * | * | * |                                                              |
|         | * | * | * | * | * | * | * | * |                                                              |
|         | * | * | * | * | * | * | * | * |                                                              |

X: Don't care, –: No change

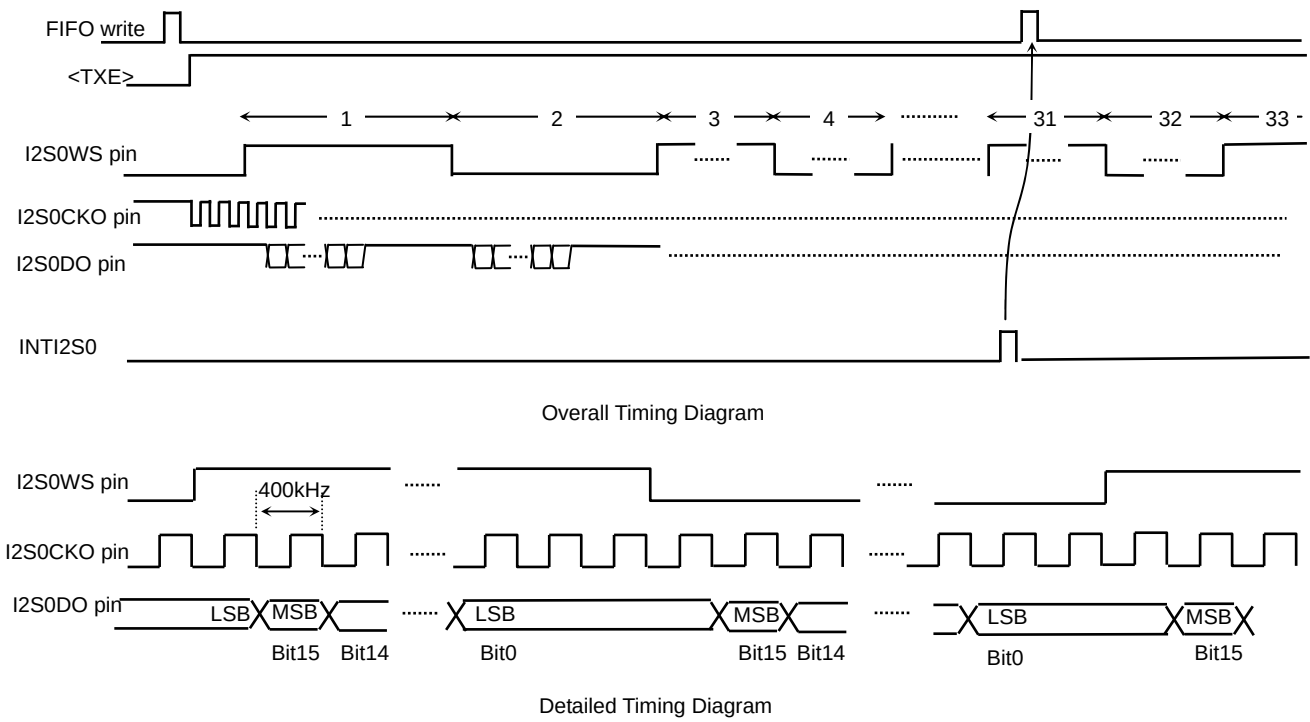


Figure3.18.5 Timing Diagrams (I<sup>2</sup>S FMT/Stereo/16bit/MSB first)

(3) Considerations for using the I<sup>2</sup>S unit

## 1) INTI2S0 generation timing

Every 4bytes data trance from FIFO buffer to shift register per one time.

An INTI2S0 interrupt is generated under two conditions. One is when there are 64 bytes of empty space in the FIFO (after 61- 64th byte has been transferred to the shift register). The other is when the FIFO becomes completely empty (after 125-128th byte has been transferred to the shift register). Therefore, INTI2S0 indicates that there are 64 bytes or 128 bytes of empty space in the FIFO, enabling the next data to be written.

The FIFO must be written in units of 64 bytes. Since the FIFO can contain 128 bytes of data, I<sup>2</sup>S output can be performed continuously as long as there are 64 bytes of data in the FIFO. It is also possible to check the FIFO state by using the I2S0CTL<TEMP0> flag.

## 2) I2S0CTL&lt;TXE0&gt;

Transmission is started by setting I2S0CTL <TXE0> to “1”. Once <TXE0> is set to “1”, transmission is continued automatically as long as the FIFO contains the data to be transmitted. While <TXE0> is set to “1” (transmission in progress), the other bits in the I2S0CTL register must not be changed.

To stop transmission, make sure that the FIFO is empty by checking the I2S0CTL<TEMP0> flag. Then, after waiting for two periods of the I2S0WS signal (after all the data has been transmitted), set <TXE0> to “0”. In case monaural setting, make sure that the FIFO is empty by checking the I2S0CTL<TEMP0> flag. Then, after waiting for four periods of the I2SWS signal (after all the data has been transmitted), set <TXE0> to “0”.

If <TXE0> is set to “0” while data is being transmitted, the transmission is stopped immediately. At the same time, the read and write pointers of the FIFO, the data in the output shift register and the clock generator are all cleared. (However, when I2S0CTL<CNTE0>=1, the clock generator is not cleared. To clear the clock generator, I2S0CTL<CNTE0> must be set to “0”). Therefore, if transmission is stopped and then resumed, no data will be output.

The WS signal stops at Low level and the CK signal stops at Low level when the rising edge is selected and at High level when the falling edge is selected.

## 3) I2S0CTL&lt;CNTE0&gt;

I2S0CTL<CNTE0> is used to control the clock generator (8-bit counter, 6-bit counter) for generating the I2S0CKO and I2S0WS signals.

Setting I2S0CTL<CNTE0> to “1” starts the counters, and setting this bit to “0” stops the counters. Normally, I<sup>2</sup>S data transmission is executed by setting both I2S0CTL<TXE0> and <CNTE0> to “1”. When transmission is stopped by setting I2S0CTL<TXE0> to “0” with I2S0CTL<CNTE0>= “1”, the clock generator is not cleared. To clear the clock generator, I2S0CTL<CNTE0> must be set to “0”.

## 4) FIFO buffer

The I<sup>2</sup>S unit is provided with a 128-byte FIFO. Although it is not necessary to use all 128 bytes in the FIFO, data should basically be written in units of 64 bytes using an INTI2S0 interrupt as a trigger. If data is written to the FIFO without waiting for an INTI2S0 interrupt or in units other than 64 bytes, interrupts cannot be generated properly.

If the last set of data, for which an interrupt is not needed, contains less than 64 bytes, set I2S0CTL<TXE0> to “0” to stop the transmission after writing the data, then checking that the <TEMP0> flag is set to “1”, and waiting for two I2S0WS periods (i.e., after all the data has been transmitted). In case monaural setting, make sure that the FIFO is empty by checking the I2S0CTL<TEMP0> flag. Then, after waiting for four periods of the I2S0WS signal (after all the data has been transmitted), set <TXE0> to “0”.

## 5) I2S0BUF

When writing data to the I2S0BUF register, be sure to use long-word data load instructions. Word data load or byte data load instructions cannot be used.

Examples)

```
ld      (I2S0BUF), xwa;  OK
ld      (I2S0BUF), wa;   NG
ld      (I2S0BUF), a;    NG
```

## 6) Share with HALT instruction

I<sup>2</sup>S circuit is not operated at IDLE1/STOP modes. Therefore, maybe PLL clock that operate at IDLE1 mode affects to this circuits. If mode is shifted to HALT mode, set it after I<sup>2</sup>S circuit is stopped.

When the CPU is shifted to the HALT mode after transmission is stopped, the time to stop completely is necessary before execution of HALT instruction.

It's time is NOP×10.

```
Example:  ld      (I2S0CTL), 0x00 ; Stop transmission
          NOP×10
          HALT
```



### 3.19 Touch Screen Interface (TSI)

An interface for 4-terminal resistor network touch-screen is built in.

The TSI easily supports two procedures: touch detection and X/Y position measurement.

Each procedure is performed by setting the TSI control register (TSICR0 and TSICR1) and using an internal AD converter.

#### 3.19.1 Touch-Screen Interface Module Internal/External Connection

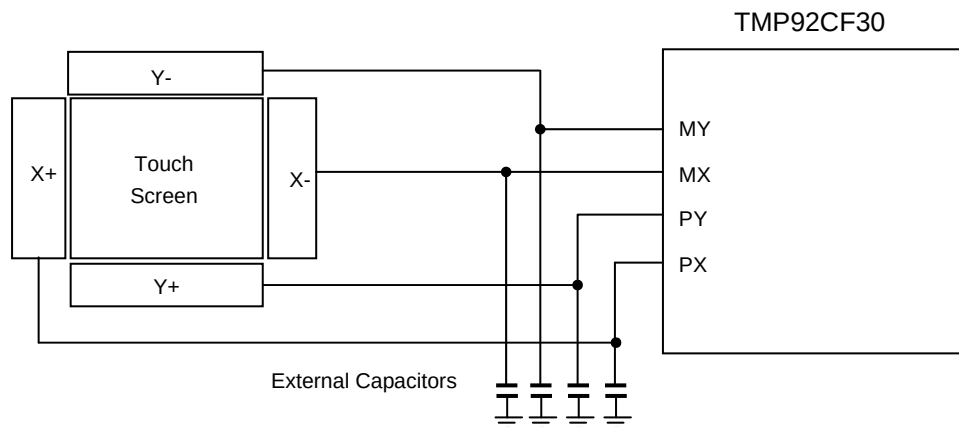


Figure 3.19.1 External connection of TSI

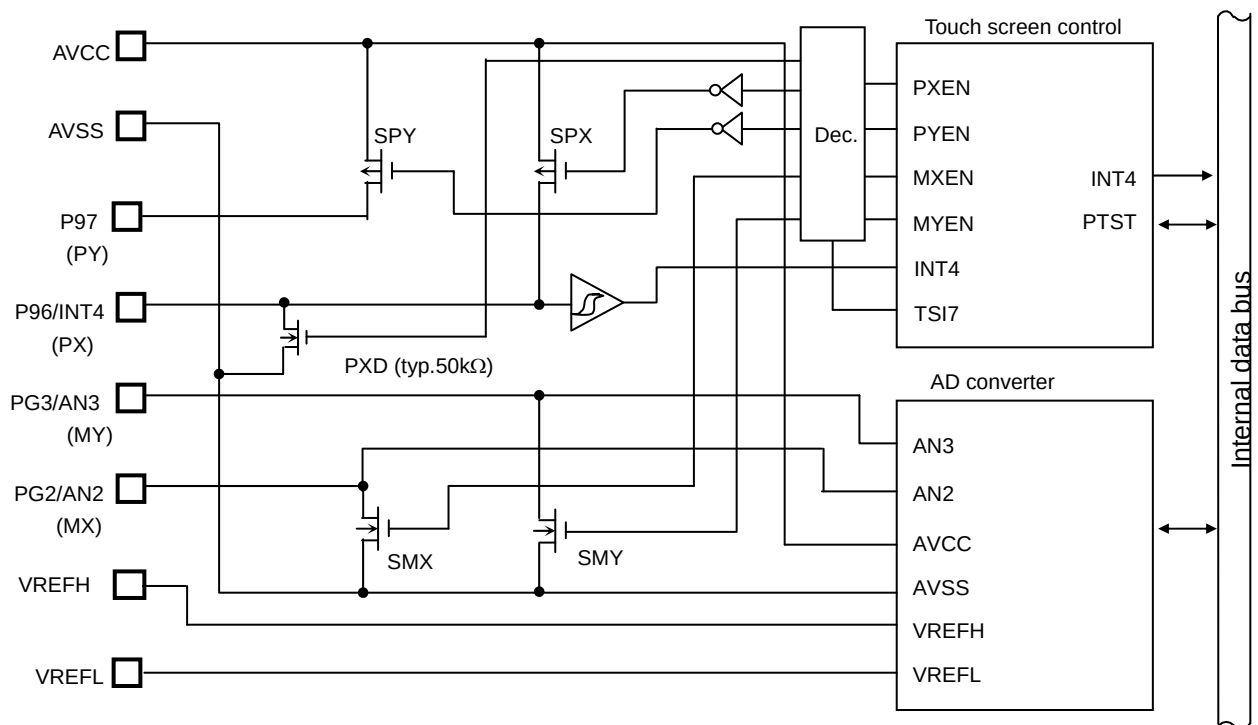


Figure 3.19.2 Internal block diagram of TSI

## 3.19.2 Touch Screen Interface (TSI) Control Register

TSI control register

|                   |             |                         |                                                                   |                                                   |                                                         |                          |                          |                          |                          |
|-------------------|-------------|-------------------------|-------------------------------------------------------------------|---------------------------------------------------|---------------------------------------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| TSICR0<br>(01F0H) |             | 7                       | 6                                                                 | 5                                                 | 4                                                       | 3                        | 2                        | 1                        | 0                        |
|                   | bit Symbol  | TSI7                    | INGE                                                              | PTST                                              | TWIEN                                                   | PYEN                     | PXEN                     | MYEN                     | MXEN                     |
|                   | Read/Write  | R/W                     |                                                                   | R                                                 | R/W                                                     |                          |                          |                          |                          |
|                   | Reset State | 0                       | 0                                                                 | 0                                                 | 0                                                       | 0                        | 0                        | 0                        | 0                        |
|                   | Function    | 0: Disable<br>1: Enable | Input gate<br>control of<br>Port 96,97<br>0: Enable<br>1: Disable | Detection<br>condition<br>0: no touch<br>1: touch | INT4<br>interrupt<br>control<br>0: Disable<br>1: Enable | SPY<br>0 : OFF<br>1 : ON | SPX<br>0 : OFF<br>1 : ON | SMY<br>0 : OFF<br>1 : ON | SMX<br>0 : OFF<br>1 : ON |

PXD (internal pull-down resistor) ON/OFF setting

| <PXEN><br><TSI7> | 0   | 1   |
|------------------|-----|-----|
| 0                | OFF | OFF |
| 1                | ON  | OFF |

Debounce time setting register

| Debounce time setting register                                                                                                          |             |                         |        |       |      |     |     |     |     |
|-----------------------------------------------------------------------------------------------------------------------------------------|-------------|-------------------------|--------|-------|------|-----|-----|-----|-----|
|                                                                                                                                         | 7           | 6                       | 5      | 4     | 3    | 2   | 1   | 0   |     |
| TSICR1<br>(01F1H)                                                                                                                       | bit Symbol  | DBC7                    | DB1024 | DB256 | DB64 | DB8 | DB4 | DB2 | DB1 |
|                                                                                                                                         | Read/Write  | R/W                     |        |       |      |     |     |     |     |
|                                                                                                                                         | Reset State | 0                       | 0      | 0     | 0    | 0   | 0   | 0   | 0   |
|                                                                                                                                         | Function    | 0: Disable<br>1: Enable | 1024   | 256   | 64   | 8   | 4   | 2   | 1   |
| Debounce time is set by the formula “(N*64-16) / fsys”.<br>“N” is the number of bits between bit6 and bit0 which are set to “1”. Note3: |             |                         |        |       |      |     |     |     |     |

Note1: Since the CPU clock is used for the debounce circuit, the debounce circuit does not operate and also no interrupts that bypass the debounce circuit are generated during IDLE1 and STOP mode. During IDLE1 or STOP mode, set this circuit to disable (Write "0" in TSICR1<DBC7>) before entering the HALT state. If debounce time is set to "0", the signal is captured into the inside after a count of 6 system clocks ( $f_{SYS}$ ) from the point when this circuit is set to disable.

Note2: To avoid a flow-through current to the normal C-MOS input gate when converting analog input data by using the AD converter, TSICR0<INGE> can be controlled. If the intermediate voltage is input, cut the input signal to the C-MOS logic (P96,P97) by setting this bit. TSICR0<PTST> is to confirm the initial pen-touch. Note that, when the input to the C-MOS logic is blocked by TSICR0<INGE>, this bit is always "1".

Note3: For example:

TSICR1=95H →  $N = 64 + 4 + 1 = 69$ , if set to (TSICR1) = 95H

### 3.19.3 Touch detection procedure

The touch detection procedure includes the procedure starting from when the pen is touched onto the touch screen and until the pen-touch is detected.

Touching the screen generates the interrupt (INT4) and terminates this procedure. After an X/Y position measuring procedure is terminated, return to this procedure to wait for the next touch.

When waiting for a touch with no contact, set only the SPY switch to ON and set all other three switches (SMY, SPX, SMX) to OFF. At this time, the pull-down resistor built in the P96/INT4/PX pin is set ON.

In this state, because the internal X- and Y-direction resistors in the touch screen are not connected, the P96/INT4/PX pin is set to Low by the internal pull-down resistor (PXD), generating no INT4 interrupt.

When a next pen-touch is given, the X- and Y-direction internal resistors in the touch screen are connected, which sets the P96/INT4/PX pin to High and generates an INT4 interrupt.

To avoid generating more than one INT4 interrupt by one pen-touch, the debounce circuit as shown below is provided. Setting debounce time in the TSICR1 register ignores pulses whose time equals to or is below the set time.

The debounce circuit detects a rising of signal to count up a set debounce counter time and then captures the signal into the inside after counting. When the signal turns to “L” during counting, the counter is cleared, starting to wait for a rising edge again.

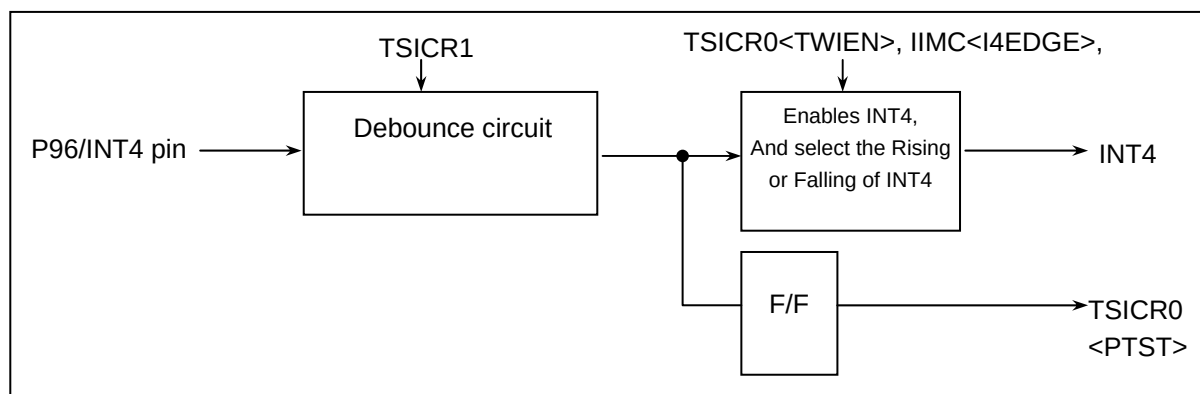


Figure 3.19.3 Block diagram of debounce circuit

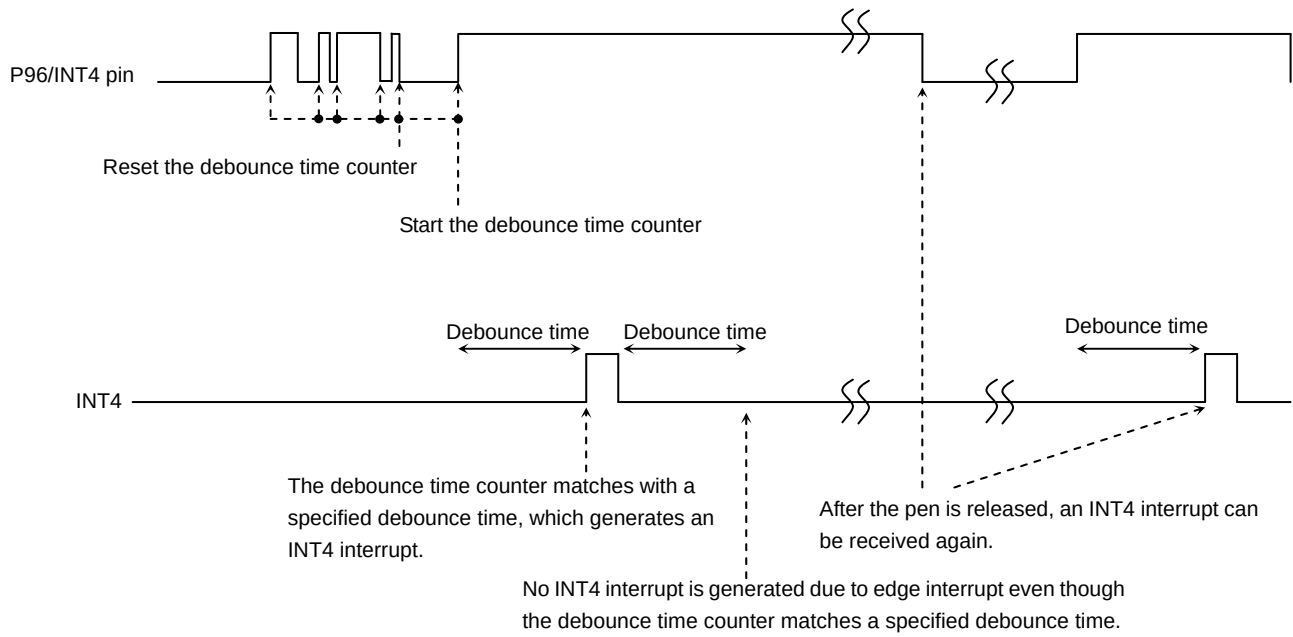


Figure 3.19.4 Timing diagram of debounce circuit

### 3.19.4 X/Y position measuring procedure

During the routine of pen-touch and INT4 interrupt generation, execute a pen position measuring following the procedure below:

#### <X position coordinate measurement>

Make the SPX and SMX switches ON, and the SPY and SMY switches OFF.

With this setting, an analog-voltage that shows the X position will be input to the PG3/MY/AN3 pin.

The X-position coordinate can be measured by converting this voltage to digital code using the AD converter.

#### <Y position coordinate measurement>

Make the SPY and SMY-switches ON, and the SPX and SMX switches OFF.

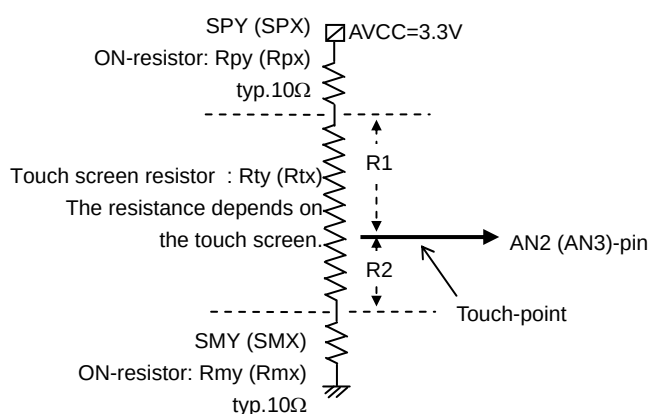
With this setting, an analog voltage that shows the Y position will be input to the PG2/MX/AN2 pin.

The Y position can be measured by converting this voltage to digital code using the AD converter.

The above analog voltage which is input to AN3 and AN2 pins during the X and Y position measurement above can be determined with the ratio between the ON resistance value of the switch in the TMP92CF30 and the resistance value in the touch screen as shown in Figure 3.19.5.

Therefore, even when touching an end area on the touch screen, the analog input voltage will be neither 3.3V nor 0.0V.

Note that the rate of each resistance varies. Remember to take this into consideration during designing. It is also recommended that an average taken from several AD conversions performed if required be adopted as the final correct value.



[Analog input voltage to the AN2 and AN3 pins: Formula to calculate E1]

$$E1 = ((R2 + Rmy) / (Rpy + Rty + Rmy)) \times AVCC [V]$$

Ex.) Where  $AVCC=3.3V$ ,  $Rpy=Rmy=10\Omega$ ,  $R1=400\Omega$  and  $R2=100\Omega$

$$E1 = ((100+10) / (10+400+100+10)) \times 3.3$$

$$= 0.698V$$

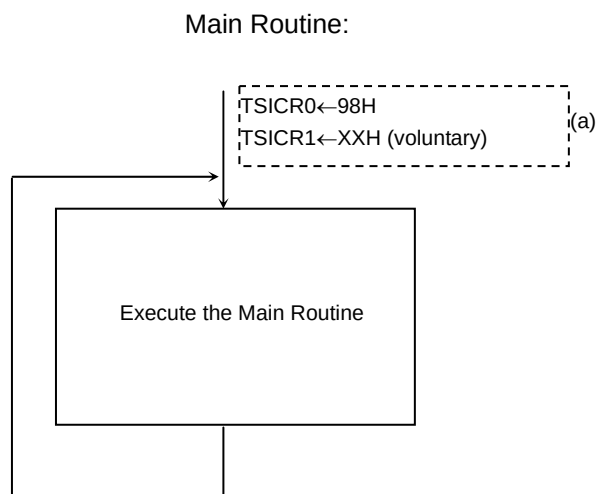
Note1: An X-coordinate position can be calculated in the same way though above formula is for Y-coordinate position.

Note2:  $Rty = R1 + R2$ .

Figure 3.19.5 Calculation analog voltage

## 3.19.5 Flow chart for TSI

## (1) Touch Detection Procedure



## (2) X/Y Position Measuring Procedure

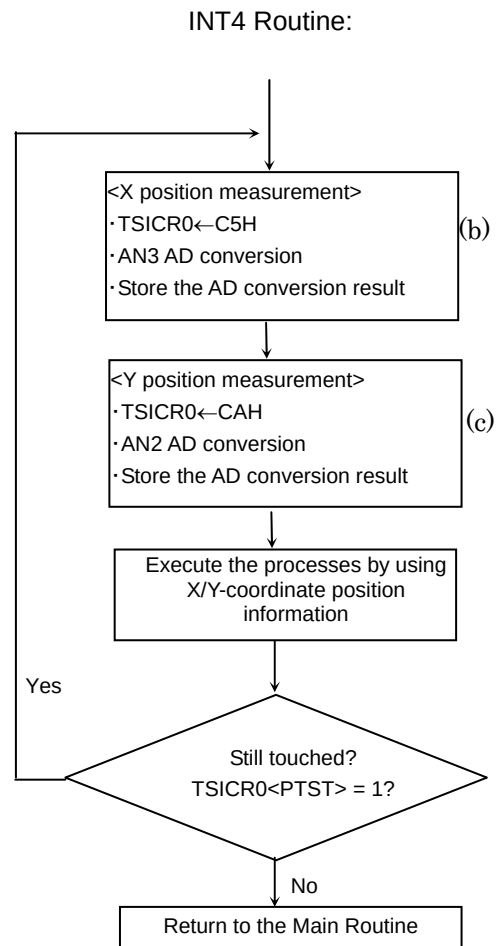
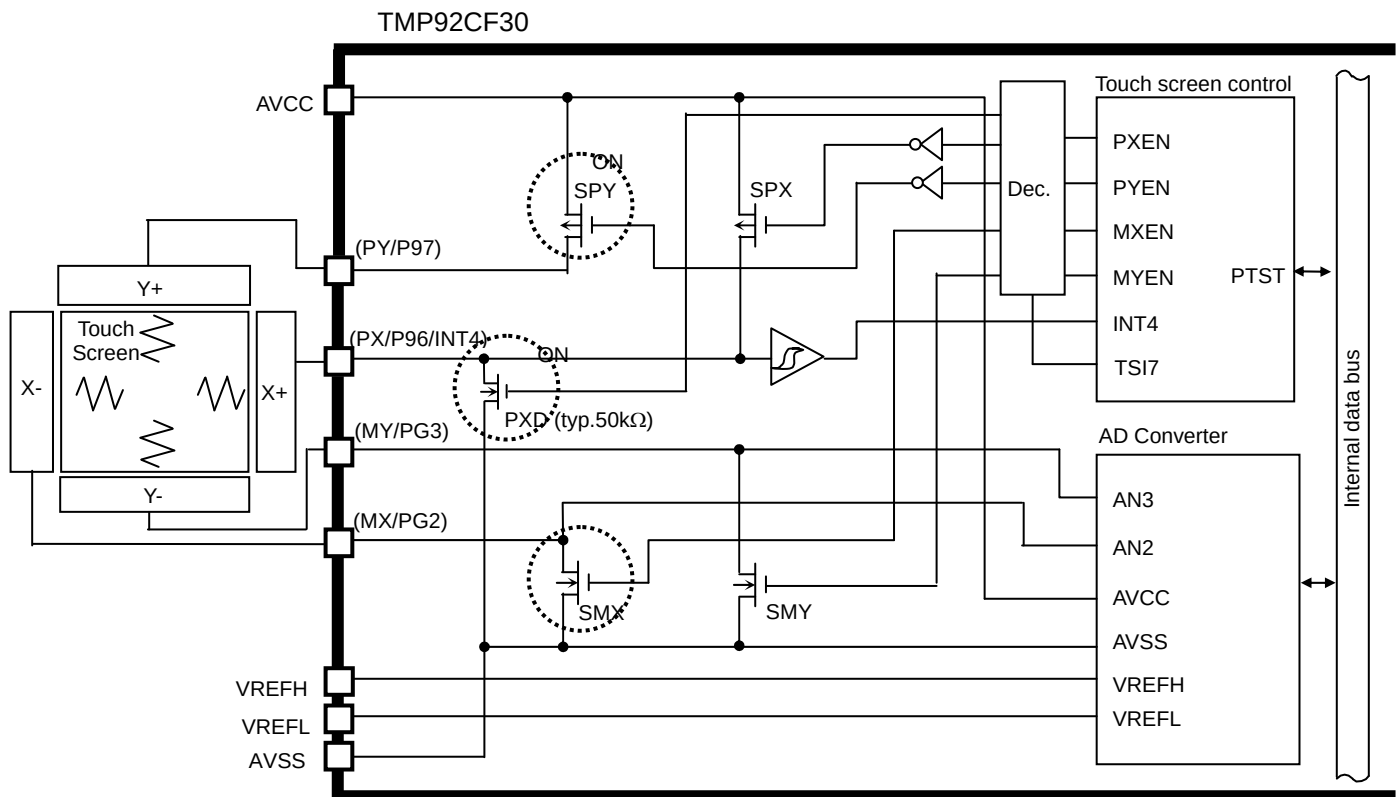


Figure 3.19.6 Flow chart for TSI

The following pages explain each circuit condition (a), (b) and (c) in the flow chart above:

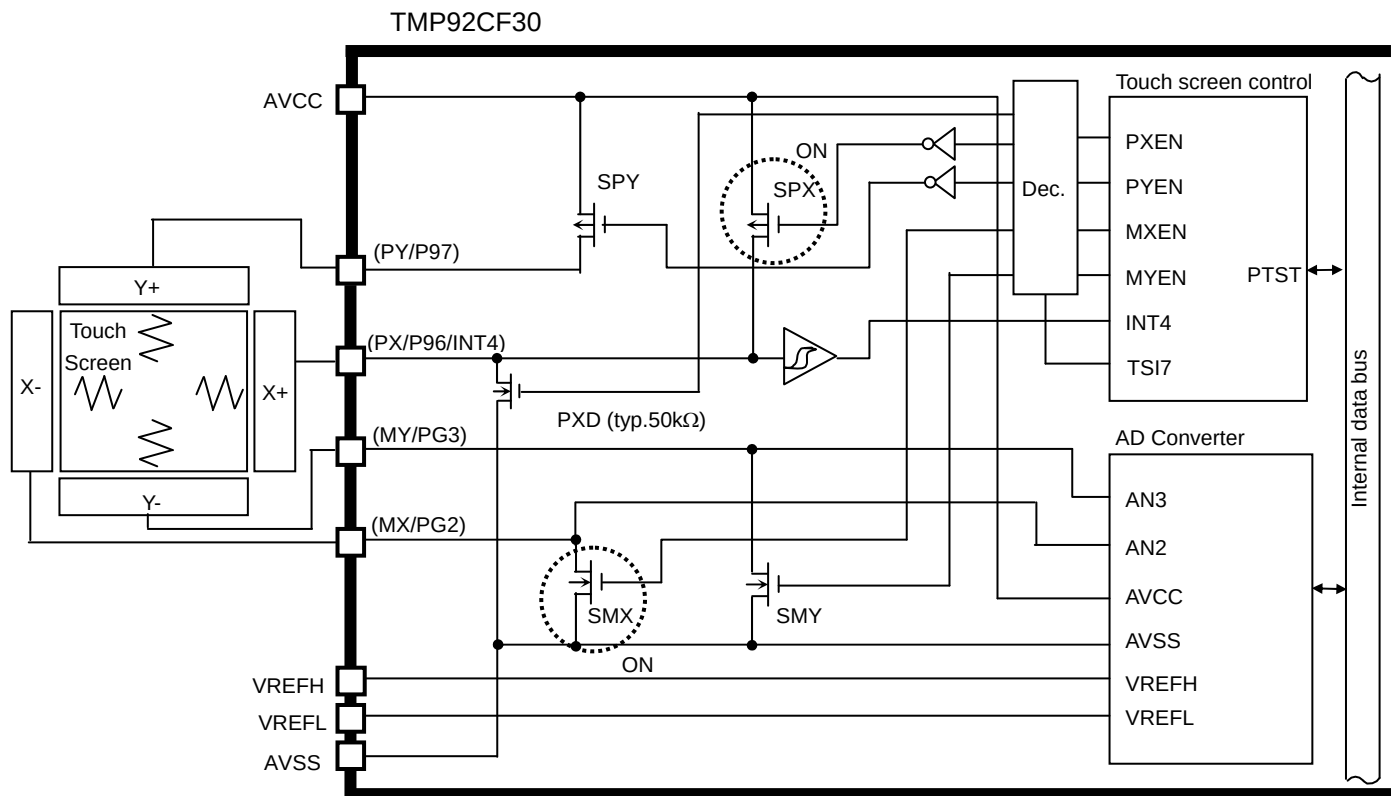
## (a) Main routine (condition of waiting INT4 interrupt)

(p9fc)<P96F>, <P97F>= "1" : Set P96 to int4/PX, set P97 to PY  
 (inte34) : Set interrupt level of INT4  
 (tsicr0)=98h : Pull-down resistor on, SPY on, Interrupt-set<TWIEN>  
 ei : Enable interrupt



## (b) INT4 routine: X-position coordinate measurement (AD conversion start)

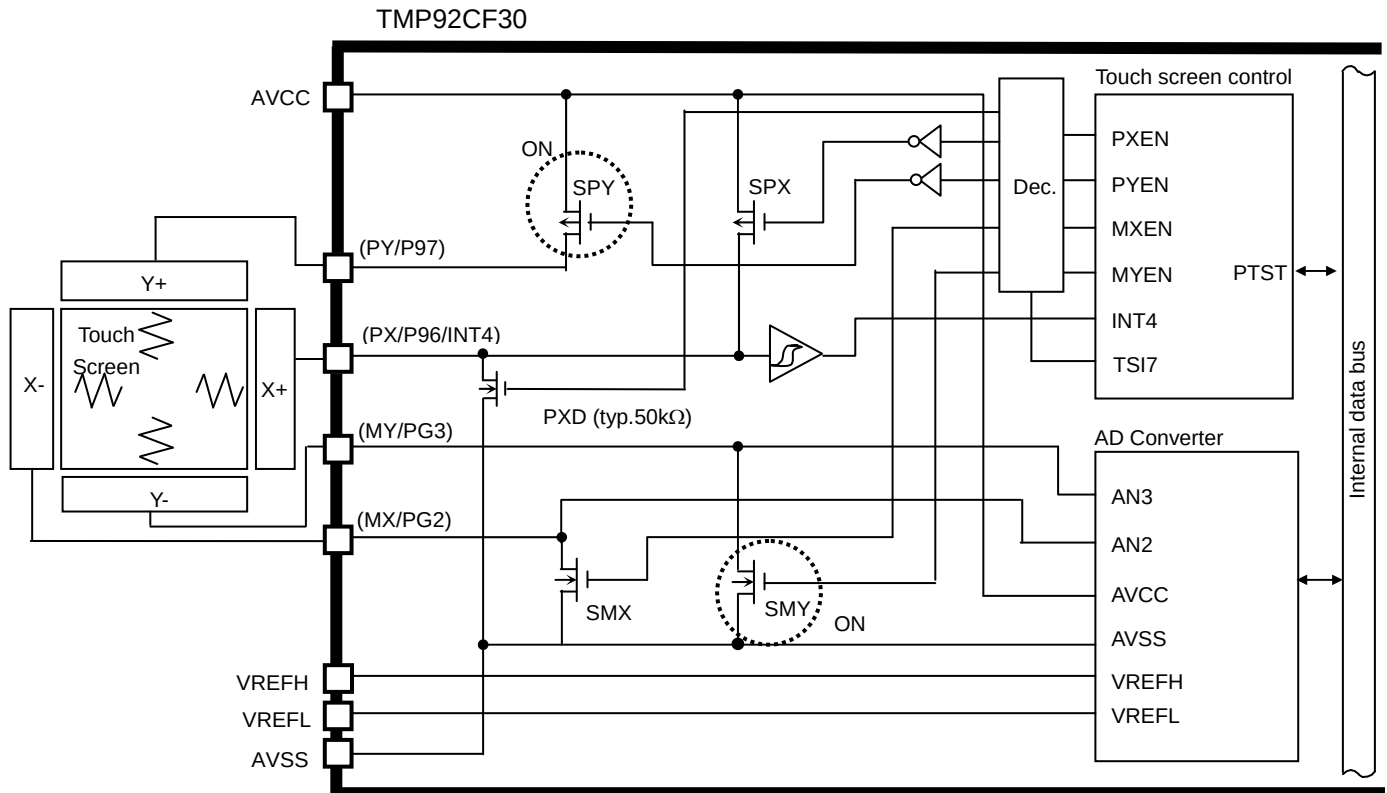
(tsicr0)=c5h : Set SMX, SPX to ON. Set the input gate of P97, P96 to OFF.  
 (admod1)=b0h : Set to AN3.  
 (admod0)=08h : Start AD conversion.





## (c) INT4 routine: Y-position coordinate measurement (AD conversion start)

(tsicr0)=cah : Set SMX, SPX to ON. Set the input gate of P97, P96 to OFF.  
 (admod1)=a0h : Set to AN2.  
 (admod0)=08h : Start AD conversion.



### 3.19.6 Use Cautions

#### 1. Debounce circuit

The CPU system clock is used in debounce circuit. Therefore, when no clock is supplied to the CPU (during IDLE1 and STOP modes), the debounce circuit does not operate. Because of this, interrupts bypassing the debounce circuit are not generated either.

When using a startup that uses the TSI starting from the state during IDLE1 and STOP modes, set the debounce circuit to disable before entering the HALT state. (TSICR1<DBC7>= "0")

#### 2. Port setting

When an intermediate voltage of 0 V to AVcc is converted using the AD converter, the intermediate voltage is also applied to the normal C-MOS input gates (P96 and P97) due to the circuit structure.

Take measures against the flow-through current to Port 96 and 97 by using TSICR0<INGE>. At this time (TSICR0<INGE>= "1"). Note that blocking the input to the C-MOS logics sets "1" at all times in TSICR0<PTST> that confirms a first pen-touch.

## 3.20 Real time clock (RTC)

### 3.20.1 Function description for RTC

- 1) Clock function (hour, minute, second)
- 2) Calendar function (month and day, day of the week, and leap year)
- 3) 24 or 12-hour (AM/PM) clock function
- 4) +/- 30 second adjustment function (by software)
- 5) Alarm function (Alarm output)
- 6) Alarm interrupt generate

### 3.20.2 Block diagram

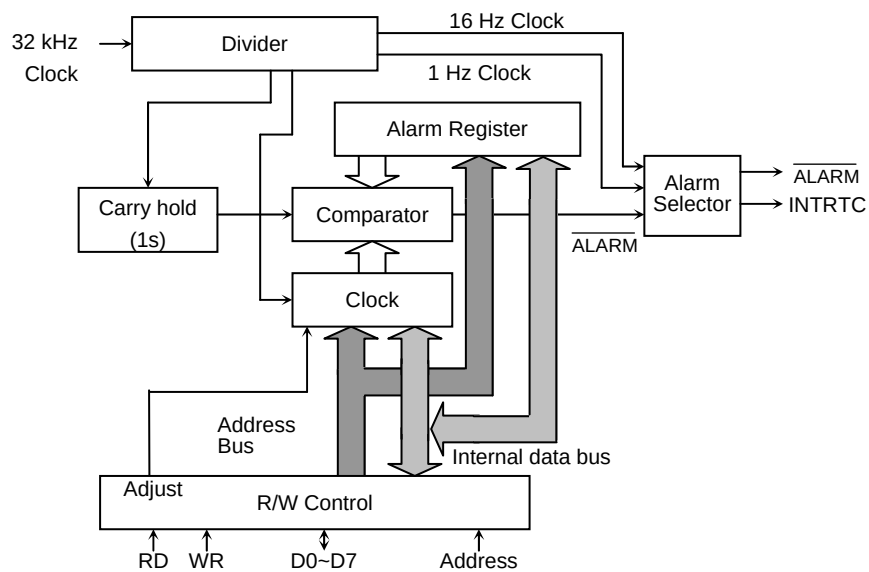


Figure 3.20.1 RTC block diagram

Note 1: Western calendar year column:

This product uses only the final two digits of the year. Therefore, the year following 99 is 00 years. In use, please take into account the first two digits when handling years in the western calendar.

Note 2: Leap year:

A leap year is divisible by 4, but the exception is any leap year which is divisible by 100; this is not considered a leap year. However, any year which is divisible by 400, is a leap year. This product does not take into account the above exceptions. Since this product accounts only for leap years divisible by 4, please adjust the system for any problems.

## 3.20.3 Control registers

Table 3.20.1 PAGE 0 (Clock function) registers

| Symbol | Address | Bit7                | Bit6           | Bit5               | Bit4                   | Bit3             | Bit2            | Bit1    | Bit0            | Function                           | Read/Write |
|--------|---------|---------------------|----------------|--------------------|------------------------|------------------|-----------------|---------|-----------------|------------------------------------|------------|
| SECR   | 1320H   |                     | 40 sec         | 20 sec             | 10 sec                 | 8 sec            | 4 sec           | 2 sec   | 1 sec           | Second column                      | R/W        |
| MINR   | 1321H   |                     | 40 min         | 20 min             | 10 min                 | 8 min            | 4 min           | 2 min   | 1 min           | Minute column                      | R/W        |
| HOURR  | 1322H   |                     |                | 20 hours/<br>PM/AM | 10 hours               | 8 hours          | 4 hours         | 2 hours | 1 hour          | Hour column                        | R/W        |
| DAYR   | 1323H   |                     |                |                    |                        |                  | W2              | W1      | W0              | Day of the week column             | R/W        |
| DATER  | 1324H   |                     |                | Day 20             | Day 10                 | Day 8            | Day 4           | Day 2   | Day 1           | Day column                         | R/W        |
| MONTHR | 1325H   |                     |                |                    | Oct.                   | Aug.             | Apr.            | Feb.    | Jan.            | Month column                       | R/W        |
| YEARR  | 1326H   | Year 80             | Year 40        | Year 20            | Year 10                | Year 8           | Year 4          | Year 2  | Year 1          | Year column<br>(Lower two columns) | R/W        |
| PAGER  | 1327H   | Interrupt<br>enable |                |                    | Adjustment<br>function | Clock<br>enable  | Alarm<br>enable |         | PAGE<br>setting | PAGE register                      | W, R/W     |
| RESTR  | 1328H   | 1Hz<br>enable       | 16Hz<br>enable | Clock<br>reset     | Alarm<br>reset         | Always write "0" |                 |         |                 | Reset register                     | W only     |

Note: When reading SECR, MINR, HOURR, DAYR, DATER, MONTHR, YEARR of PAGE0, the current state is read.

Table 3.20.2 PAGE1 (Alarm function) registers

| Symbol | Address | Bit7                | Bit6           | Bit5               | Bit4                   | Bit3             | Bit2            | Bit1    | Bit0            | Function               | Read/Write |
|--------|---------|---------------------|----------------|--------------------|------------------------|------------------|-----------------|---------|-----------------|------------------------|------------|
| SECR   | 1320H   |                     |                |                    |                        |                  |                 |         |                 |                        | R/W        |
| MINR   | 1321H   |                     | 40 min         | 20 min             | 10 min                 | 8 min            | 4 min           | 2 min   | 1 min           | Minute column          | R/W        |
| HOURR  | 1322H   |                     |                | 20 hours/<br>PM/AM | 10 hours               | 8 hours          | 4 hours         | 2 hours | 1 hour          | Hour column            | R/W        |
| DAYR   | 1323H   |                     |                |                    |                        |                  | W2              | W1      | W0              | Day of the week column | R/W        |
| DATER  | 1324H   |                     |                | Day 20             | Day 10                 | Day 8            | Day 4           | Day 2   | Day 1           | Day column             | R/W        |
| MONTHR | 1325H   |                     |                |                    |                        |                  |                 |         | 24/12           | 24-hour clock mode     | R/W        |
| YEARR  | 1326H   |                     |                |                    |                        |                  |                 | LEAP1   | LEAP0           | Leap-year mode         | R/W        |
| PAGER  | 1327H   | Interrupt<br>enable |                |                    | Adjustment<br>function | Clock<br>enable  | Alarm<br>enable |         | PAGE<br>setting | PAGE register          | W, R/W     |
| RESTR  | 1328H   | 1Hz<br>enable       | 16Hz<br>enable | Clock<br>reset     | Alarm<br>reset         | Always write "0" |                 |         |                 | Reset register         | W only     |

Note: When reading SECR, MINR, HOURR, DAYR, DATER, MONTHR, YEARR of PAGE1, the current state is read.

## 3.20.4 Detailed explanation of control register

RTC is not initialized by system reset. Therefore, all registers must be initialized at the beginning of the program.

## (1) Second column register (for PAGE0 only)

|                 |             |              |                   |                   |                   |                  |                  |                  |                  |
|-----------------|-------------|--------------|-------------------|-------------------|-------------------|------------------|------------------|------------------|------------------|
| SECR<br>(1320H) | <div></div> | 7            | 6                 | 5                 | 4                 | 3                | 2                | 1                | 0                |
|                 | Bit symbol  | <div></div>  | SE6               | SE5               | SE4               | SE3              | SE2              | SE1              | SE0              |
|                 | Read/Write  | <div></div>  | R/W               |                   |                   |                  |                  |                  |                  |
|                 | Reset State | <div></div>  | Undefined         |                   |                   |                  |                  |                  |                  |
|                 | Function    | "0" is read. | 40 sec.<br>column | 20 sec.<br>column | 10 sec.<br>column | 8 sec.<br>column | 4 sec.<br>column | 2 sec.<br>column | 1 sec.<br>column |

|   |   |   |   |   |   |   |        |
|---|---|---|---|---|---|---|--------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 sec  |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 sec  |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 sec  |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3 sec  |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4 sec  |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 5 sec  |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 6 sec  |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 7 sec  |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 8 sec  |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 9 sec  |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 sec |

:

|   |   |   |   |   |   |   |        |
|---|---|---|---|---|---|---|--------|
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 19 sec |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 sec |

:

|   |   |   |   |   |   |   |        |
|---|---|---|---|---|---|---|--------|
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 29 sec |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30 sec |

:

|   |   |   |   |   |   |   |        |
|---|---|---|---|---|---|---|--------|
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 39 sec |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40 sec |

:

|   |   |   |   |   |   |   |        |
|---|---|---|---|---|---|---|--------|
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 49 sec |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 50 sec |

:

|   |   |   |   |   |   |   |        |
|---|---|---|---|---|---|---|--------|
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 59 sec |
|---|---|---|---|---|---|---|--------|

Note: Do not set data other than as shown above.

## (2) Minute column register (for PAGE0/1)

MINR  
(1321H)

|             | 7            | 6                 | 5                 | 4                 | 3                | 2                | 1                | 0                |
|-------------|--------------|-------------------|-------------------|-------------------|------------------|------------------|------------------|------------------|
| Bit symbol  |              | MI6               | MI5               | MI4               | MI3              | MI2              | MI1              | MI0              |
| Read/Write  |              | R/W               |                   |                   |                  |                  |                  |                  |
| Reset State |              | Undefined         |                   |                   |                  |                  |                  |                  |
| Function    | "0" is read. | 40 min,<br>column | 20 min,<br>column | 10 min,<br>column | 8 min,<br>column | 4 min,<br>column | 2 min,<br>column | 1 min,<br>column |

|   |   |   |   |   |   |   |        |
|---|---|---|---|---|---|---|--------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 min  |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 min  |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 min  |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3 min  |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4 min  |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 5 min  |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 6 min  |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 7 min  |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 8 min  |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 9 min  |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 min |

:

|   |   |   |   |   |   |   |        |
|---|---|---|---|---|---|---|--------|
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 19 min |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 min |

:

|   |   |   |   |   |   |   |        |
|---|---|---|---|---|---|---|--------|
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 29 min |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30 min |

:

|   |   |   |   |   |   |   |        |
|---|---|---|---|---|---|---|--------|
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 39 min |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40 min |

:

|   |   |   |   |   |   |   |        |
|---|---|---|---|---|---|---|--------|
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 49 min |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 50 min |

:

|   |   |   |   |   |   |   |        |
|---|---|---|---|---|---|---|--------|
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 59 min |
|---|---|---|---|---|---|---|--------|

Note: Do not set data other than as shown above.

## (3) Hour column register (for PAGE0/1)

## 1. In case of 24-hour clock mode (MONTHR&lt;MO0&gt;= "1")

|               | 7            | 6 | 5              | 4              | 3             | 2             | 1             | 0             |
|---------------|--------------|---|----------------|----------------|---------------|---------------|---------------|---------------|
| HOURR (1322H) |              |   |                |                |               |               |               |               |
| Bit symbol    |              |   | HO5            | HO4            | HO3           | HO2           | HO1           | HO0           |
| Read/Write    |              |   | R/W            |                |               |               |               |               |
| Reset State   |              |   | Undefined      |                |               |               |               |               |
| Function      | "0" is read. |   | 20 hour column | 10 hour column | 8 hour column | 4 hour column | 2 hour column | 1 hour column |

|   |   |   |   |   |   |           |
|---|---|---|---|---|---|-----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 o'clock |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 o'clock |
| 0 | 0 | 0 | 0 | 1 | 0 | 2 o'clock |

:

|   |   |   |   |   |   |            |
|---|---|---|---|---|---|------------|
| 0 | 0 | 1 | 0 | 0 | 0 | 8 o'clock  |
| 0 | 0 | 1 | 0 | 0 | 1 | 9 o'clock  |
| 0 | 1 | 0 | 0 | 0 | 0 | 10 o'clock |

:

|   |   |   |   |   |   |            |
|---|---|---|---|---|---|------------|
| 0 | 1 | 1 | 0 | 0 | 1 | 19 o'clock |
| 1 | 0 | 0 | 0 | 0 | 0 | 20 o'clock |

:

|   |   |   |   |   |   |            |
|---|---|---|---|---|---|------------|
| 1 | 0 | 0 | 0 | 1 | 1 | 23 o'clock |
|---|---|---|---|---|---|------------|

Note: Do not set data other than as shown above.

## 2. In case of 12-hour clock mode (MONTHR&lt;MO0&gt;= "0")

|               | 7            | 6 | 5         | 4              | 3             | 2             | 1             | 0             |
|---------------|--------------|---|-----------|----------------|---------------|---------------|---------------|---------------|
| HOURR (1322H) |              |   |           |                |               |               |               |               |
| Bit symbol    |              |   | HO5       | HO4            | HO3           | HO2           | HO1           | HO0           |
| Read/Write    |              |   | R/W       |                |               |               |               |               |
| Reset State   |              |   | Undefined |                |               |               |               |               |
| Function      | "0" is read. |   | PM/AM     | 10 hour column | 8 hour column | 4 hour column | 2 hour column | 1 hour column |

|   |   |   |   |   |   |                |
|---|---|---|---|---|---|----------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 o'clock (AM) |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 o'clock      |
| 0 | 0 | 0 | 0 | 1 | 0 | 2 o'clock      |

:

|   |   |   |   |   |   |                |
|---|---|---|---|---|---|----------------|
| 0 | 0 | 1 | 0 | 0 | 1 | 9 o'clock      |
| 0 | 1 | 0 | 0 | 0 | 0 | 10 o'clock     |
| 0 | 1 | 0 | 0 | 0 | 1 | 11 o'clock     |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 o'clock (PM) |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 o'clock      |

Note: Do not set data other than as shown above.

## (4) Day of the week column register (for PAGE0/1)

|                 |             |              |             |             |             |             |           |     |     |
|-----------------|-------------|--------------|-------------|-------------|-------------|-------------|-----------|-----|-----|
|                 | <div></div> | 7            | 6           | 5           | 4           | 3           | 2         | 1   | 0   |
| DAYR<br>(1323H) | Bit symbol  | <div></div>  | <div></div> | <div></div> | <div></div> | <div></div> | WE2       | WE1 | WE0 |
|                 | Read/Write  | <div></div>  | <div></div> | <div></div> | <div></div> | <div></div> | R/W       |     |     |
|                 | Reset State | <div></div>  | <div></div> | <div></div> | <div></div> | <div></div> | Undefined |     |     |
|                 | Function    | "0" is read. |             |             |             |             | W2        | W1  | W0  |

|   |   |   |           |
|---|---|---|-----------|
| 0 | 0 | 0 | Sunday    |
| 0 | 0 | 1 | Monday    |
| 0 | 1 | 0 | Tuesday   |
| 0 | 1 | 1 | Wednesday |
| 1 | 0 | 0 | Thursday  |
| 1 | 0 | 1 | Friday    |
| 1 | 1 | 0 | Saturday  |

Note: Do not set data other than as shown above.

## (5) Day column register (PAGE0/1)

|                  |             |              |   |           |        |       |       |       |       |
|------------------|-------------|--------------|---|-----------|--------|-------|-------|-------|-------|
| DATER<br>(1324H) |             | 7            | 6 | 5         | 4      | 3     | 2     | 1     | 0     |
|                  | Bit symbol  |              |   | DA5       | DA4    | DA3   | DA2   | DA1   | DA0   |
|                  | Read/Write  |              |   | R/W       |        |       |       |       |       |
|                  | Reset State |              |   | Undefined |        |       |       |       |       |
|                  | Function    | "0" is read. |   | Day 20    | Day 10 | Day 8 | Day 4 | Day 2 | Day 1 |

|   |   |   |   |   |   |         |
|---|---|---|---|---|---|---------|
| 0 | 0 | 0 | 0 | 0 | 1 | 1st day |
| 0 | 0 | 0 | 0 | 1 | 0 | 2nd day |
| 0 | 0 | 0 | 0 | 1 | 1 | 3rd day |
| 0 | 0 | 0 | 1 | 0 | 0 | 4th day |

:

|   |   |   |   |   |   |          |
|---|---|---|---|---|---|----------|
| 0 | 0 | 1 | 0 | 0 | 1 | 9th day  |
| 0 | 1 | 0 | 0 | 0 | 0 | 10th day |
| 0 | 1 | 0 | 0 | 0 | 1 | 11th day |

:

|   |   |   |   |   |   |          |
|---|---|---|---|---|---|----------|
| 0 | 1 | 1 | 0 | 0 | 1 | 19th day |
| 1 | 0 | 0 | 0 | 0 | 0 | 20th day |

:

|   |   |   |   |   |   |          |
|---|---|---|---|---|---|----------|
| 1 | 0 | 1 | 0 | 0 | 1 | 29th day |
| 1 | 1 | 0 | 0 | 0 | 0 | 30th day |
| 1 | 1 | 0 | 0 | 0 | 1 | 31st day |

Note1: Do not set data other than as shown above.

Note2: Do not set for non-existent days (e.g.: 30<sup>th</sup> Feb)



## (6) Month column register (for PAGE0 only)

|                   | 7            | 6 | 5 | 4         | 3        | 2        | 1        | 0       |
|-------------------|--------------|---|---|-----------|----------|----------|----------|---------|
| MONTHR<br>(1325H) |              |   |   | MO4       | MO4      | MO2      | MO1      | MO0     |
| Bit symbol        |              |   |   | R/W       |          |          |          |         |
| Read/Write        |              |   |   | Undefined |          |          |          |         |
| Reset State       |              |   |   |           |          |          |          |         |
| Function          | "0" is read. |   |   | 10 months | 8 months | 4 months | 2 months | 1 month |

|   |   |   |   |   |           |
|---|---|---|---|---|-----------|
| 0 | 0 | 0 | 0 | 1 | January   |
| 0 | 0 | 0 | 1 | 0 | February  |
| 0 | 0 | 0 | 1 | 1 | March     |
| 0 | 0 | 1 | 0 | 0 | April     |
| 0 | 0 | 1 | 0 | 1 | May       |
| 0 | 0 | 1 | 1 | 0 | June      |
| 0 | 0 | 1 | 1 | 1 | July      |
| 0 | 1 | 0 | 0 | 0 | August    |
| 0 | 1 | 0 | 0 | 1 | September |
| 1 | 0 | 0 | 0 | 0 | October   |
| 1 | 0 | 0 | 0 | 1 | November  |
| 1 | 0 | 0 | 1 | 0 | December  |

Note: Do not set data other than as shown above.

## (7) Select 24-hour clock or 12-hour clock (for PAGE1 only)

|                   | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0                        |
|-------------------|--------------|---|---|---|---|---|---|--------------------------|
| MONTHR<br>(1325H) |              |   |   |   |   |   |   | MO0                      |
| Bit symbol        |              |   |   |   |   |   |   | R/W                      |
| Read/Write        |              |   |   |   |   |   |   | Undefined                |
| Reset State       |              |   |   |   |   |   |   |                          |
| Function          | "0" is read. |   |   |   |   |   |   | 1: 24-hour<br>0: 12-hour |

## (8) Year column register (for PAGE0 only)

|                  |             |           |          |          |          |         |         |         |        |
|------------------|-------------|-----------|----------|----------|----------|---------|---------|---------|--------|
| YEARR<br>(1326H) | <div></div> | 7         | 6        | 5        | 4        | 3       | 2       | 1       | 0      |
|                  | Bit symbol  | YE7       | YE6      | YE5      | YE4      | YE3     | YE2     | YE1     | YE0    |
|                  | Read/Write  | R/W       |          |          |          |         |         |         |        |
|                  | Reset State | Undefined |          |          |          |         |         |         |        |
|                  | Function    | 80 Years  | 40 Years | 20 Years | 10 Years | 8 Years | 4 Years | 2 Years | 1 Year |

|   |   |   |   |   |   |   |   |          |
|---|---|---|---|---|---|---|---|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 years |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 years |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02 years |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03 years |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 years |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05 years |

:

|   |   |   |   |   |   |   |   |          |
|---|---|---|---|---|---|---|---|----------|
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 99 years |
|---|---|---|---|---|---|---|---|----------|

Note: Do not set data other than as shown above.

## (9) Leap-year register (for PAGE1 only)

|                  | 7           | 6            | 5 | 4 | 3 | 2 | 1                               | 0     |
|------------------|-------------|--------------|---|---|---|---|---------------------------------|-------|
| YEARR<br>(1326H) | Bit symbol  |              |   |   |   |   | LEAP1                           | LEAP0 |
|                  | Read/Write  |              |   |   |   |   | R/W                             |       |
|                  | Reset State |              |   |   |   |   | Undefined                       |       |
|                  | Function    | "0" is read. |   |   |   |   | 00: leap-year                   |       |
|                  |             |              |   |   |   |   | 01: one year after leap-year    |       |
|                  |             |              |   |   |   |   | 10: two years after leap-year   |       |
|                  |             |              |   |   |   |   | 11: three years after leap-year |       |

|   |   |                                                |
|---|---|------------------------------------------------|
| 0 | 0 | Current year is a leap-year                    |
| 0 | 1 | Current year is the year following a leap year |
| 1 | 0 | Current year is two years after a leap year    |
| 1 | 1 | Current year is three years after a leap year  |

## (10)PAGE register (for PAGE0/1)

|                                                                 | 7           | 6                                    | 5            | 4                             | 3                                | 2                                | 1            | 0                 |
|-----------------------------------------------------------------|-------------|--------------------------------------|--------------|-------------------------------|----------------------------------|----------------------------------|--------------|-------------------|
| PAGER<br>(1327H)                                                | Bit symbol  | INTENA                               |              | ADJUST                        | ENATMR                           | ENAALM                           |              | PAGE              |
|                                                                 | Read/Write  | R/W                                  |              | W                             | R/W                              |                                  |              | R/W               |
|                                                                 | Reset State | 0                                    |              | Undefined                     | Undefined                        |                                  |              | Undefined         |
| A Read-<br>modify- write<br>operation<br>cannot be<br>performed | Function    | Interrupt<br>0: Disable<br>1: Enable | "0" is read. | 0: Don't<br>care<br>1: Adjust | Clock<br>0: Disable<br>1: Enable | ALARM<br>0: Disable<br>1: Enable | "0" is read. | PAGE<br>selection |

Note: Please keep the setting order below of <ENATMR>, <ENAAML> and <INTENA>. Set difference time for Clock/Alarm setting and interrupt setting.

Example: Clock setting/Alarm setting

Id (pager), 0ch : Clock, Alarm enable

Id (pager), 8ch : Interrupt enable

|      |   |              |
|------|---|--------------|
| PAGE | 0 | Select Page0 |
|      | 1 | Select Page1 |

|        |   |                                                                                                                                                                                                                                                                                                                                                                        |
|--------|---|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ADJUST | 0 | Don't care                                                                                                                                                                                                                                                                                                                                                             |
|        | 1 | Adjust sec. counter.<br>When this bit is set to "1" the sec. counter becomes to "0" when the value of the sec. counter is 0-29. When the value of the sec. counter is 30-59, the min. counter is carried and sec. counter becomes "0". Output Adjust signal during 1 cycle of $f_{SYS}$ . After being adjusted once, Adjust is released automatically.<br>(PAGE0 only) |

## (11) Reset register (for PAGE0/1)

|                                                                 | 7           | 6                              | 5                               | 4                | 3                | 2                | 1 | 0 |
|-----------------------------------------------------------------|-------------|--------------------------------|---------------------------------|------------------|------------------|------------------|---|---|
| RESTR<br>(1328H)                                                | Bit symbol  | DIS1HZ                         | DIS16HZ                         | RSTTMR           | RSTALM           | -                | - | - |
|                                                                 | Read/Write  | W                              |                                 |                  |                  |                  |   |   |
|                                                                 | Reset State | Undefined                      |                                 |                  |                  |                  |   |   |
| A Read-<br>modify- write<br>operation<br>cannot be<br>performed | Function    | 1Hz<br>0: Enable<br>1: Disable | 16Hz<br>0: Enable<br>1: Disable | 1:Clock<br>reset | 1:Alarm<br>reset | Always write "0" |   |   |

|        |   |                      |
|--------|---|----------------------|
| RSTALM | 0 | Unused               |
|        | 1 | Reset alarm register |

|        |   |               |
|--------|---|---------------|
| RSTTMR | 0 | Unused        |
|        | 1 | Reset Counter |

| <DIS1HZ> | <DIS16HZ> | PAGER<ENAALM> | Interrupt source signal |
|----------|-----------|---------------|-------------------------|
| 1        | 1         | 1             | Alarm                   |
| 0        | 1         | 0             | 1Hz                     |
| 1        | 0         | 0             | 16Hz                    |
| Others   |           |               | Output "0"              |

### 3.20.5 Operational description

#### (1) Reading clock data

##### 1. Using 1Hz interrupt

1Hz interrupt and the count up of internal data synchronize. Therefore, data can read correctly if reading data after 1Hz interrupt occurred.

##### 2. Using two times reading

There is a possibility of incorrect clock data reading when the internal counter carries over. To ensure correct data reading, please read twice, as follows:

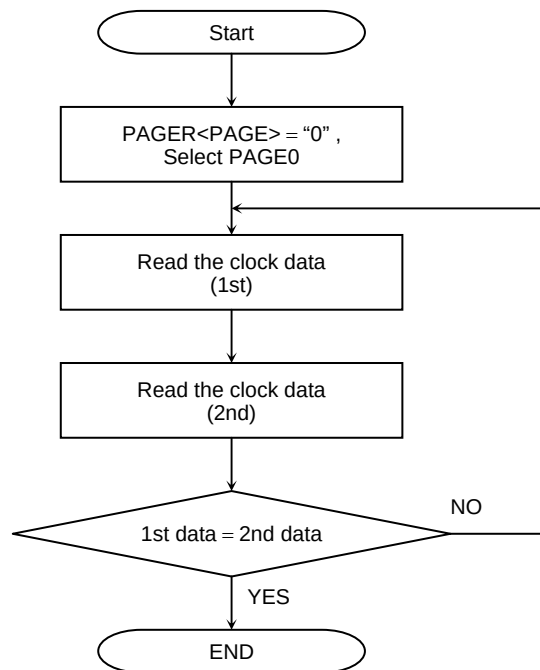


Figure 3.20.2 Flowchart of clock data read

## (2) Writing clock data

When a carry over occurs during a write operation, the data cannot be written correctly. Please use the following method to ensure data is written correctly.

## 1. Using 1Hz interrupt

1Hz interrupt and the count up of internal data synchronize. Therefore, data can write correctly if writing data after 1Hz interrupt occurred.

## 2. Resets counter

There are 15-stage counter inside the RTC, which generate a 1Hz clock from 32,768 kHz. The data is written after reset this counter.

However, if clearing the counter, it is counted up only first writing at half of the setting time, first writing only. Therefore, if setting the clock counter correctly, after clearing the counter, set the 1Hz-interrupt to enable. And set the time after the first interrupt (occurs at 0.5s) is occurred.

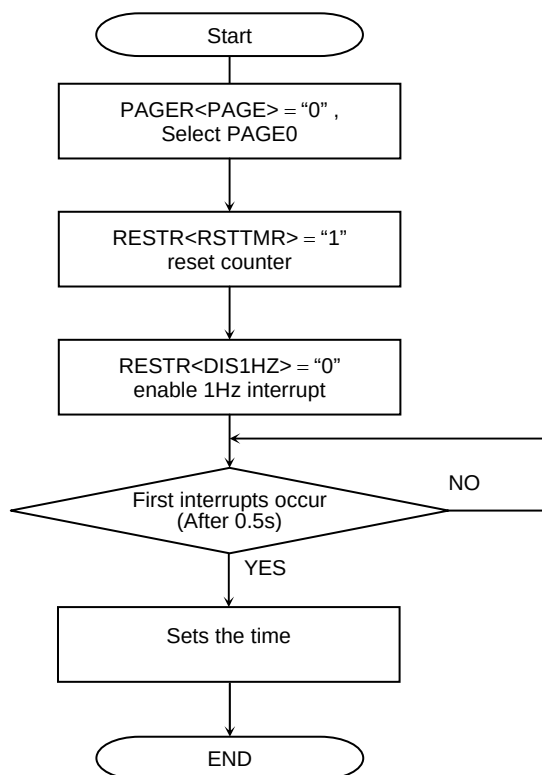


Figure 3.20.3 Flowchart of clock data read

### 3. Disabling the clock

A clock carry over is prohibited when “0” is written to `PAGER<ENATMR>` in order to prevent malfunction caused by the Carry hold circuit. While the clock is prohibited, the Carry hold circuit holds a one sec. carry signal from a divider. When the clock becomes enabled, the carry signal is output to the clock, the time is revised and operation continues. However, the clock is delayed when clock-disabled state continues for one second or more. Note that at this time system power is down while the clock is disabled. In this case the clock is stopped and clock is delayed.

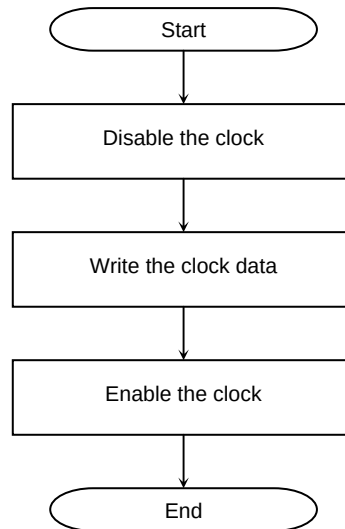


Figure 3.20.4 Flowchart of Clock disable

### 3.20.6 Explanation of the interrupt signal and alarm signal

The alarm function used by setting the PAGE1 register and outputting either of the following three signals from  $\overline{\text{ALARM}}$  pin by writing "1" to  $\text{PAGER<PAGE>}$ . INTRTC outputs a 1-shot pulse when the falling edge is detected. RTC is not initialized by RESET. Therefore, when the clock or alarm function is used, clear interrupt request flag in INTC (interrupt controller).

- (1) When the alarm register and the clock correspond, output "0".
- (2) 1Hz Output clock.
- (3) 16Hz Output clock.

- (1) When the alarm register and the clock correspond, output "0"

When  $\text{PAGER<ENAALM>} = "1"$ , and the value of PAGE0 clock corresponds with PAGE1 alarm register output "0" to  $\overline{\text{ALARM}}$  pin and generate INTRTC.

The methods for using the alarm are as follows:

Initialization of alarm is done by writing in "1" to  $\text{RESTR<RSTALM>}$ . All alarm settings become Don't care. In this case, the alarm always corresponds with value of the clock, and if  $\text{PAGER<ENAALM>} = "1"$ , INTRTC interrupt request is generated.

Setting alarm min., alarm hour, alarm date and alarm day is done by writing data to the relevant PAGE1 register.

When all setting contents correspond, RTC generates an INTRTC interrupt, if  $\text{PAGER<INTENA><ENAALM>} = "1"$ . However, contents which have not been set up (don't care state) are always considered to correspond.

Contents which have already been set up, cannot be returned independently to the Don't care state. In this case, the alarm must be initialized and alarm register reset.

The following is an example program for outputting an alarm from  $\overline{\text{ALARM}}$  -pin at noon (PM12:00) every day.

```
LD      (PAGER), 09H      ; Alarm disable, setting PAGE1
LD      (RESTR), D0H      ; Alarm initialize
LD      (DAYR), 01H       ; W0
LD      (DATER), 01H      ; 1 day
LD      (HOURR), 12H      ; Setting 12 o'clock
LD      (MINR), 00H       ; Setting 00 min
                          ; Set up time 31 μs (Note)
LD      (PAGER), 0CH      ; Alarm enable
( LD    (PAGER), 8CH      ; Interrupt enable )
```

When the CPU is operating at high frequency oscillation, it may take a maximum of one clock at 32 kHz (about 30μs) for the time register setting to become valid. In the above example, it is necessary to set 31μs of set up time between setting the time register and enabling the alarm register.

Note: This set up time is unnecessary when you use only internal interruption.

## (2) With 1Hz output clock

RTC outputs a clock of 1Hz to  $\overline{\text{ALARM}}$  pin by setting up  $\text{PAGER}<\text{ENAALM}>= "0"$ ,  $\text{RESTR}<\text{DIS1HZ}>= "0"$ ,  $<\text{DIS16HZ}>= "1"$ . RTC also generates an INTRTC interrupt on the falling edge of the clock.

## (3) With 16Hz output clock

RTC outputs a clock of 16Hz to  $\overline{\text{ALARM}}$  pin by setting up  $\text{PAGER}<\text{ENAALM}>= "0"$ ,  $\text{RESTR}<\text{DIS1HZ}>= "1"$ ,  $<\text{DIS16HZ}>= "0"$ . RTC also generates INTRTC an interrupt on the falling edge of the clock.



### 3.21 Melody / Alarm generator (MLD)

The TMP92CF30 contains a melody function and alarm function, both of which are output from the MLDALM pin. Five kind of fixed cycle interrupt are generated by using a 15bit counter for use as the alarm generator.

The features are as follows.

#### 1) Melody generator

The Melody function generates signals of any frequency (4Hz- 5461Hz) based on a low-speed clock (32.768 kHz) and outputs the signals from the MLDALM pin.

The melody tone can easily be heard by connecting an external loud speaker.

#### 2) Alarm generator

The Alarm function generates eight kinds of alarm waveform having a modulation frequency (4096Hz) determined by the low-speed clock (32.768 kHz). This waveform can be inverted by setting a value to a register.

The alarm tone can easily be heard by connecting an external loud speaker.

Five kinds of fixed cycle interrupts are generated (1Hz, 2Hz, 64Hz, 512Hz, 8192Hz) by using a counter that is used for the alarm generator.

## 3.21.1 Block Diagram

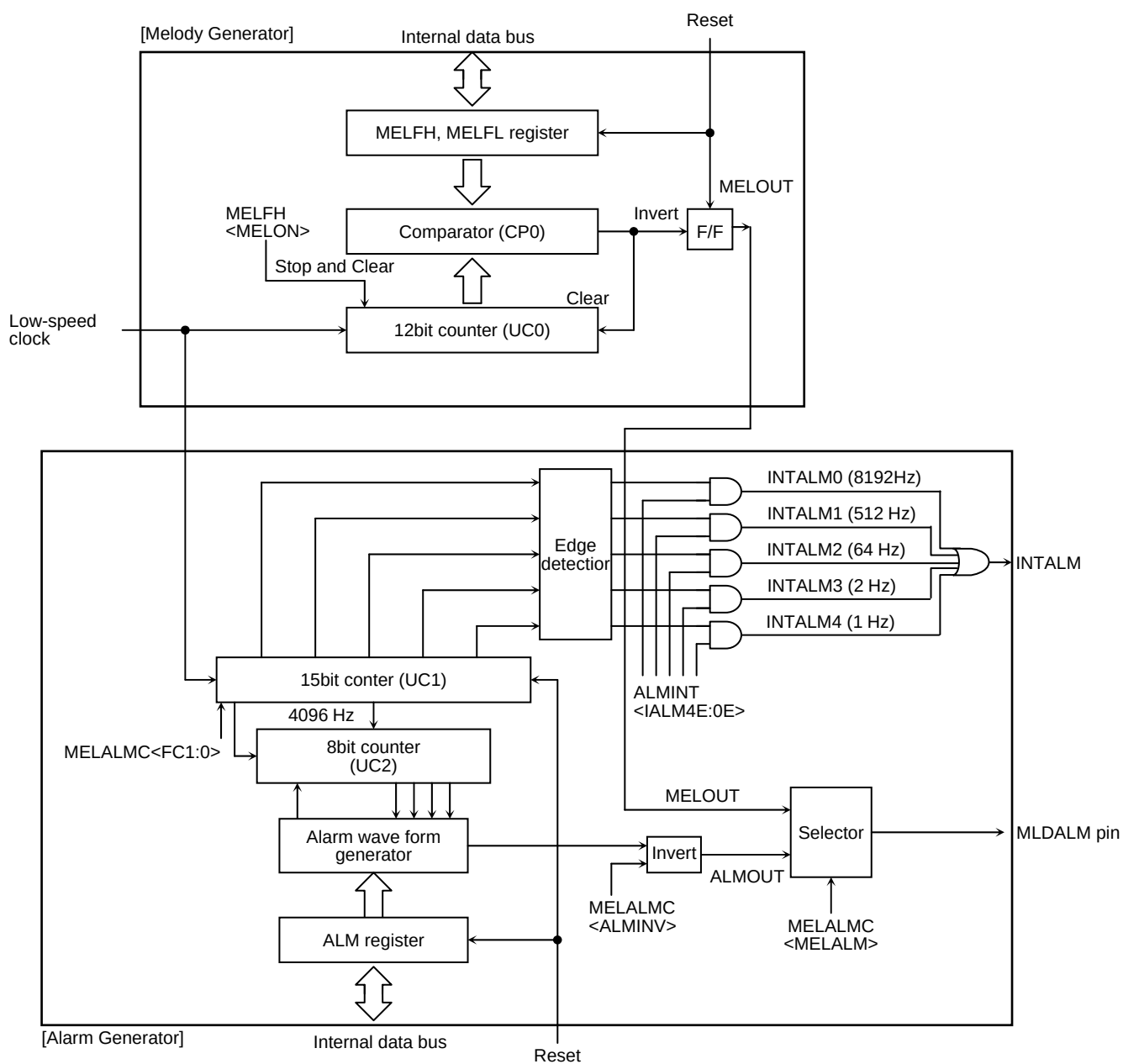


Figure 3.21.1MLD Block Diagram

## 3.21.2 Control registers

ALM register

|             | 7                     | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-------------|-----------------------|-----|-----|-----|-----|-----|-----|-----|
| bit Symbol  | AL8                   | AL7 | AL6 | AL5 | AL4 | AL3 | AL2 | AL1 |
| Read/Write  | R/W                   |     |     |     |     |     |     |     |
| Reset State | 0                     | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Function    | Setting alarm pattern |     |     |     |     |     |     |     |

ALM  
(1330H)

MELALMC register

|             | 7                                                                                            | 6   | 5                                        | 4                | 3 | 2 | 1 | 0                                                     |
|-------------|----------------------------------------------------------------------------------------------|-----|------------------------------------------|------------------|---|---|---|-------------------------------------------------------|
| bit Symbol  | FC1                                                                                          | FC0 | ALMINV                                   | –                | – | – | – | MELALM                                                |
| Read/Write  | R/W                                                                                          |     |                                          |                  |   |   |   |                                                       |
| Reset State | 0                                                                                            | 0   | 0                                        | 0                | 0 | 0 | 0 | 0                                                     |
| Function    | Free-run counter control<br>00: Hold<br>01: Restart<br>10: Clear & Stop<br>11: Clear & Start |     | Alarm<br>Waveform<br>invert<br>1: Invert | Always write "0" |   |   |   | Select<br>Output<br>Waveform<br>0: Alarm<br>1: Melody |

MELALMC  
(1331H)

Note1: MELALMC&lt;FC1&gt; is always read "0".

Note2: When setting MELALMC register except &lt;FC1:0&gt; while the free-run counter is running, &lt;FC1:0&gt; is kept "01".

MELFL register

|             | 7                                     | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-------------|---------------------------------------|-----|-----|-----|-----|-----|-----|-----|
| bit Symbol  | ML7                                   | ML6 | ML5 | ML4 | ML3 | ML2 | ML1 | ML0 |
| Read/Write  | R/W                                   |     |     |     |     |     |     |     |
| Reset State | 0                                     | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Function    | Setting melody frequency (lower 8bit) |     |     |     |     |     |     |     |

MELFL  
(1332H)

MELFH register

|             | 7                                                              | 6 | 5 | 4 | 3                                    | 2    | 1   | 0   |
|-------------|----------------------------------------------------------------|---|---|---|--------------------------------------|------|-----|-----|
| bit Symbol  | MELON                                                          |   |   |   | ML11                                 | ML10 | ML9 | ML8 |
| Read/Write  | R/W                                                            |   |   |   | R/W                                  |      |     |     |
| Reset State | 0                                                              |   |   |   | 0                                    | 0    | 0   | 0   |
| Function    | Control<br>melody<br>counter<br>0: Stop &<br>Clear<br>1: Start |   |   |   | Setting melody frequency(upper 4bit) |      |     |     |

MELFH  
(1333H)

ALMINT register

|             | 7 | 6 | 5                   | 4                            | 3                            | 2                             | 1                              | 0                               |
|-------------|---|---|---------------------|------------------------------|------------------------------|-------------------------------|--------------------------------|---------------------------------|
| bit Symbol  |   |   | –                   | IALM4E                       | IALM3E                       | IALM2E                        | IALM1E                         | IALM0E                          |
| Read/Write  |   |   |                     | R/W                          |                              |                               |                                |                                 |
| Reset State |   |   | 0                   | 0                            | 0                            | 0                             | 0                              | 0                               |
| Function    |   |   | Always<br>write "0" | 1:INTALM4<br>(1Hz)<br>enable | 1:INTALM3<br>(2Hz)<br>enable | 1:INTALM2<br>(64Hz)<br>enable | 1:INTALM1<br>(512Hz)<br>enable | 1:INTALM0<br>(8192Hz)<br>enable |

ALMINT  
(1334H)

Note: INTALM0 to INTALM4 prohibit that set to enable at same time. If setting to enable, set only 1.

### 3.21.3 Operational Description

#### 3.21.3.1 Melody generator

The Melody function generates signals of any frequency (4Hz-5461Hz) based on a low-speed clock (32.768kHz) and outputs the signals from the MLDALM pin.

The melody tone can easily be heard by connecting an external loud speaker.

(Operation)

MELALMC<MELALM> must first be set as 1 in order to select the melody waveform to be output from MLDALM. The melody output frequency must then be set to 12-bit register MELFH, MELFL.

The following are examples of settings and calculations of melody output frequency.

(Formula for calculating melody waveform frequency)

$$\begin{aligned} & \text{Melody output waveform} & f_{\text{MLD}}[\text{Hz}] &= 32768 / (2 \times N + 4) & @f_s = 32.768 [\text{kHz}] \\ & \text{Setting value for melody} & N &= (16384 / f_{\text{MLD}}) - 2 \\ & \text{(Note: } N = 1 \sim 4095 \text{ (001H} \sim \text{FFFH), 0 is not acceptable)} \end{aligned}$$

(Example program)

When outputting an "A" musical note (440Hz)

```
LD      (MELALMC), --XXXXX1B    ; Select melody waveform
LD      (MELFL), 23H              ; N = 16384/440 - 2 = 35.2 = 023H
LD      (MELFH), 80H              ; Start to generate waveform
```

(Refer: Basic musical scale setting table)

| Scale | Frequency<br>[Hz] | Register<br>Value: N |
|-------|-------------------|----------------------|
| C     | 264               | 03CH                 |
| D     | 297               | 035H                 |
| E     | 330               | 030H                 |
| F     | 352               | 02DH                 |
| G     | 396               | 027H                 |
| A     | 440               | 023H                 |
| B     | 495               | 01FH                 |
| C     | 528               | 01DH                 |

### 3.21.3.2 Alarm generator

The Alarm function generates eight kinds of alarm waveform having a modulation frequency of 4096Hz determined by the low-speed clock (32.768 kHz). This waveform is reversible by setting a value to a register.

The alarm tone can easily be heard by connecting an external loud speaker.

Five kind of fixed cycle (interrupts can be generated 1Hz, 2Hz, 64Hz, 512Hz, 8192Hz) by using a counter which is used for the alarm generator.

#### (Operation)

MELALMC<MELALM> must first be set as 0 in order to select the alarm waveform to be output from MLDALMC. The “10” must be set on the MELALMC <FC1:0> register, and clear internal counter. Alarm pattern must then be set on the 8-bit register of ALM. If it is inverted output data, set <ALMINV> as invert.

Then set the MELAMC<FC1:0> to “11” to start the free-run counter.

To stop the alarm output, write “00H” to the ALM register.

The following are examples of program, setting value of alarm pattern and waveform of each setting value.

#### (Setting value of alarm pattern)

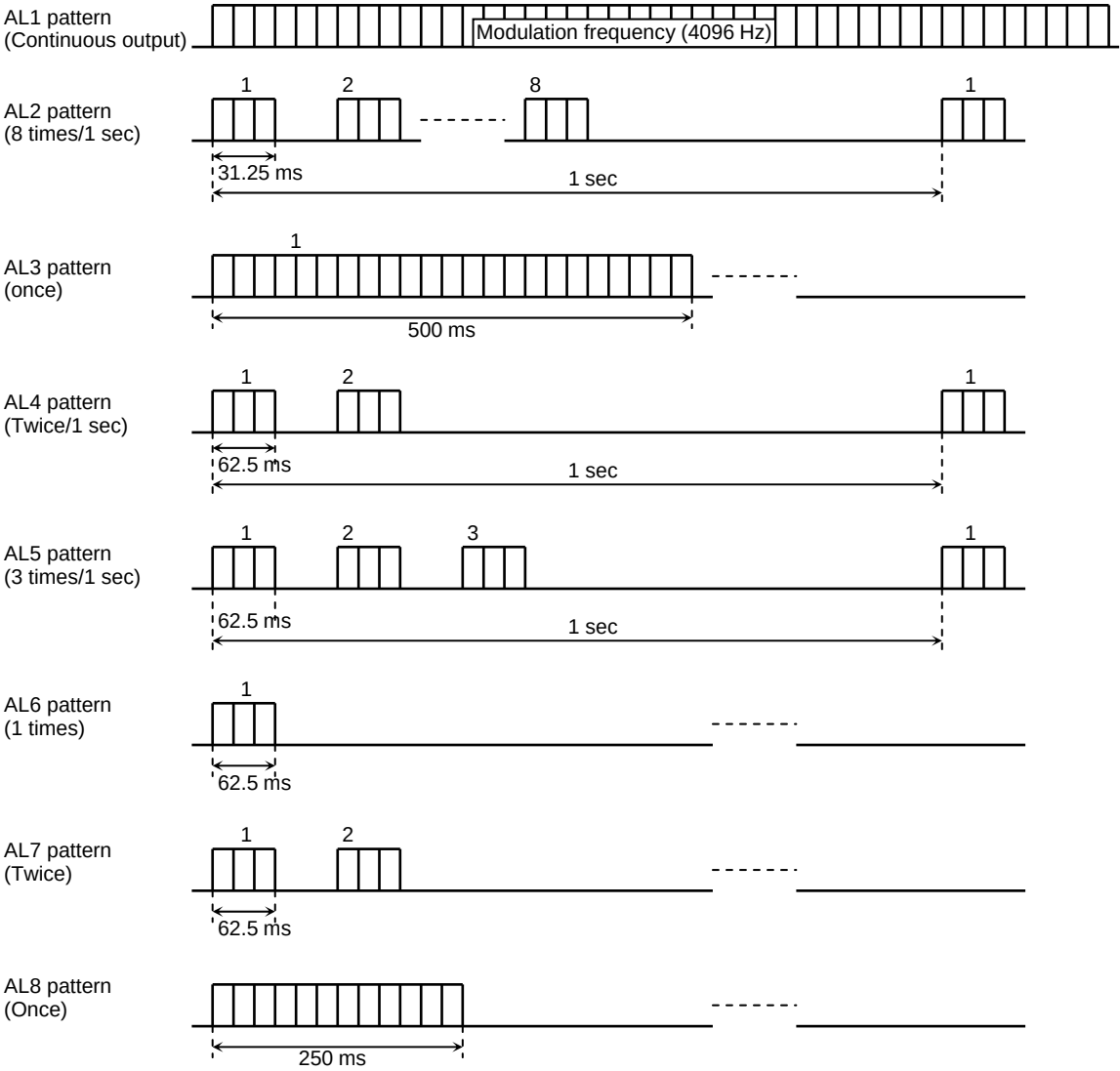
| Setting value<br>for ALM<br>register | Alarm waveform            |
|--------------------------------------|---------------------------|
| 00H                                  | “0” fixed                 |
| 01H                                  | AL1 pattern               |
| 02H                                  | AL2 pattern               |
| 04H                                  | AL3 pattern               |
| 08H                                  | AL4 pattern               |
| 10H                                  | AL5 pattern               |
| 20H                                  | AL6 pattern               |
| 40H                                  | AL7 pattern               |
| 80H                                  | AL8 pattern               |
| Other                                | Undefined<br>(Do not set) |

#### (Example program)

When outputting AL2 pattern (31.25ms/8 times/1sec)

```
LD    (MELALMC), 80H      ; Clear counter, set output alarm waveform
LD    (ALM), 02H          ; Set AL2 pattern
LD    (MELALMC), C0H      ; Free-run counter start
```

Example: Waveform of alarm pattern for each setting value: not inverted)



### 3.22 Analog-Digital Converter (ADC)

A 10-bit serial conversion analog/digital converter (AD converter) having six channels of analog input is built in.

Figure 3.22.1 shows the block diagram of the AD converter.

The 6-analog input channels (AN0-AN5) can be used as general-purpose inputs.

Note1: To reduce the power supply current by IDLE2, IDLE1 and STOP mode, the standby state may be maintained with the internal comparator still being enabled, depending on the timing. Check that the AD converter operation is in a stop before executing HALT instruction. In IDLE2 mode it operates only the case of  $ADMOD0 < I2AD \leq 0$ .

Note2: Setting  $ADMOD1 < DACON = 0$  while the AD converter is in a stop can reduce current consumption.

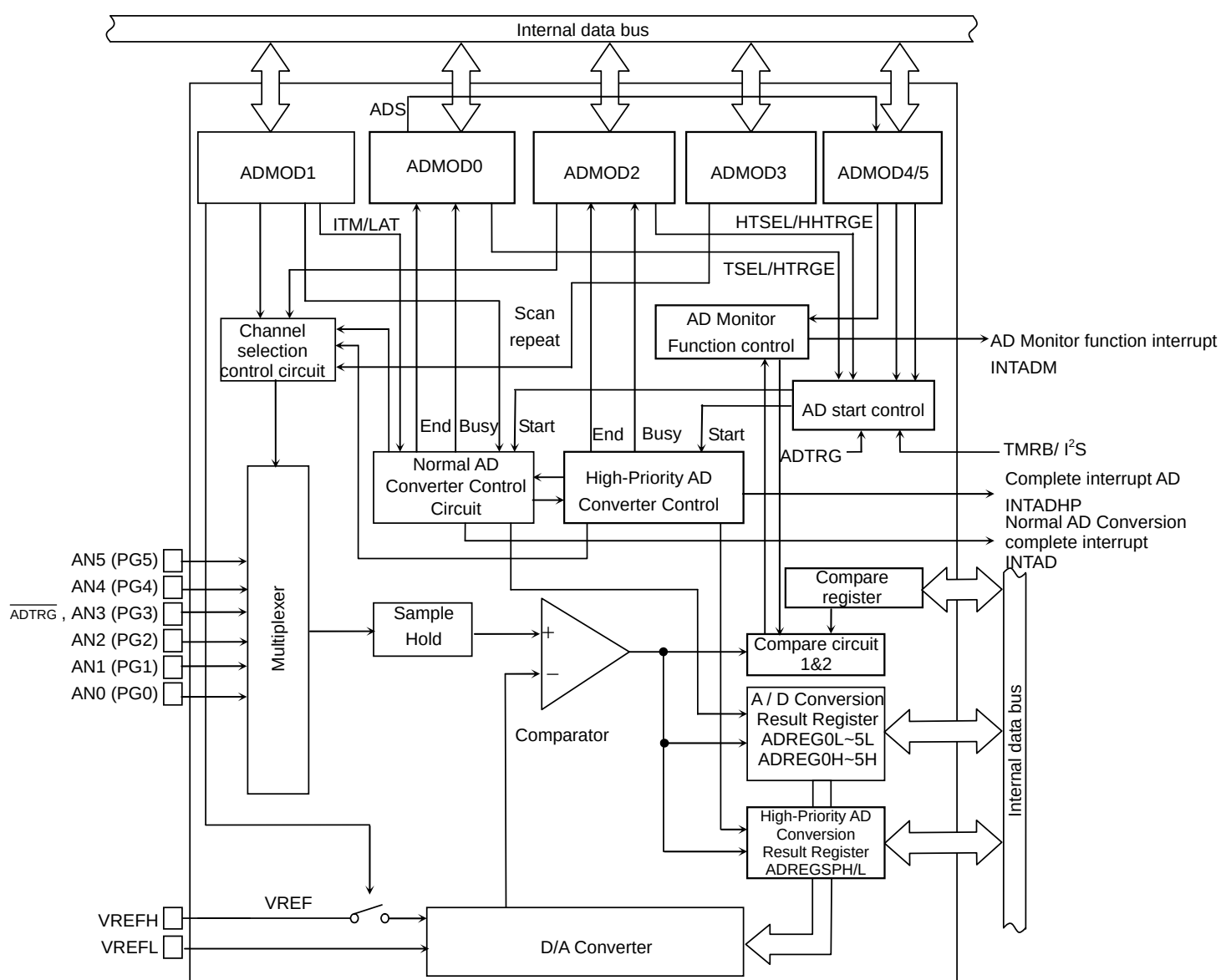


Figure 3.22.1 ADC Block Diagram

### 3.22.1 Control register

The AD converter is controlled by the AD mode control registers (ADMOD0, ADMOD1, ADMOD2, ADMOD3, ADMOD4 and ADMOD5). AD conversion results are stored in the six registers of AD conversion result higher-order/lower-order registers ADREG0H/L to ADREG5H/L. Top-priority conversion results are stored in ADREGSPH/L.

Figure 3.22.2 to Figure 3.22.11 show the registers available in the AD converter.

| AD Mode Control Register 0 (Normal conversion control) |             |                                                                                                                      |                                                                              |   |                                                        |                                                                                                  |                                                                      |                                                                                                                    |
|--------------------------------------------------------|-------------|----------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------|---|--------------------------------------------------------|--------------------------------------------------------------------------------------------------|----------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|
|                                                        | 7           | 6                                                                                                                    | 5                                                                            | 4 | 3                                                      | 2                                                                                                | 1                                                                    | 0                                                                                                                  |
| ADMOD0<br>(12B8H)                                      | bit Symbol  | EOS                                                                                                                  | BUSY                                                                         |   | I2AD                                                   | ADS                                                                                              | HTRGE                                                                | TSEL1<br>TSEL0                                                                                                     |
|                                                        | Read/Write  | R                                                                                                                    |                                                                              |   | R/W                                                    |                                                                                                  |                                                                      |                                                                                                                    |
|                                                        | Reset State | 0                                                                                                                    | 0                                                                            |   | 0                                                      | 0                                                                                                | 0                                                                    | 0                                                                                                                  |
|                                                        | Function    | Normal AD conversion end flag<br>0: During conversion sequence or before starting<br>1: Complete conversion sequence | Normal AD conversion BUSY Flag<br>0: Stop conversion<br>1: During conversion |   | AD conversion when IDLE2 mode<br>0: Stop<br>1: Operate | Start Normal AD conversion<br>0: Don't Care<br>1: Start AD conversion<br><br>Always read as "0". | Normal AD conversion at Hard ware trigger<br>0: Disable<br>1: Enable | Select Hard ware trigger<br>00: INTTB00 interrupt<br>01: Reserved<br>10: $\overline{\text{ADTRG}}$<br>11: Reserved |

Figure 3.22.2 AD Conversion Registers



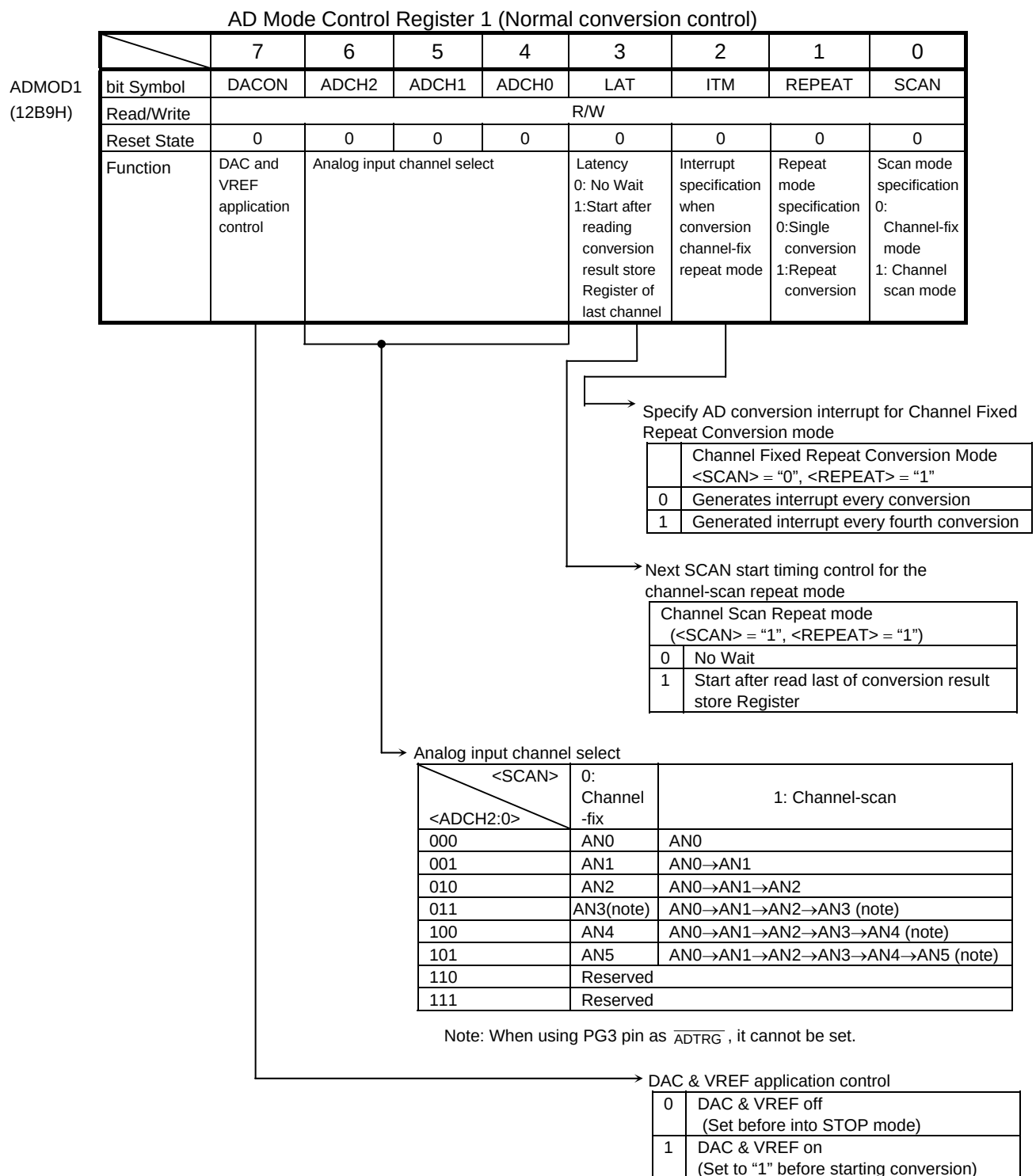


Figure 3.22.3 AD Converter Related Register

| AD Mode Control Register 2 (Top-priority conversion control) |             |                                                                                                                                 |                                                                                    |   |   |                                                                                                        |                                                                            |                                                                                                                                          |
|--------------------------------------------------------------|-------------|---------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|---|---|--------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|
| ADMOD2<br>(12BAH)                                            |             | 7                                                                                                                               | 6                                                                                  | 5 | 4 | 3                                                                                                      | 2                                                                          | 1 0                                                                                                                                      |
|                                                              | bit Symbol  | HEOS                                                                                                                            | HBUSY                                                                              |   |   | HADS                                                                                                   | HHTRGE                                                                     | HTSEL1 HTSEL0                                                                                                                            |
|                                                              | Read/Write  | R                                                                                                                               |                                                                                    |   |   | R/W                                                                                                    |                                                                            |                                                                                                                                          |
|                                                              | Reset State | 0                                                                                                                               | 0                                                                                  |   |   | 0                                                                                                      | 0                                                                          | 0 0                                                                                                                                      |
|                                                              | Function    | Top-priority AD conversion sequence FLAG<br>0: During conversion sequence or before starting<br>1: Complete conversion sequence | Top-priority AD conversion BUSY Flag<br>0: Stop conversion<br>1: During conversion |   |   | Start Top-priority AD conversion<br>0: Don't Care<br>1: Start AD conversion<br><br>Always read as "0". | Top-priority AD conversion at Hard ware trigger<br>0: Disable<br>1: Enable | Select Hard ware trigger<br>00: INTTB10 interrupt<br>01: Reserved<br>10: $\overline{\text{ADTRG}}$<br>11: $I^2S$ Sampling Counter Output |

| AD Mode Control Register 3 (Top-priority conversion control) |             |                   |                                          |        |        |   |   |                   |
|--------------------------------------------------------------|-------------|-------------------|------------------------------------------|--------|--------|---|---|-------------------|
| ADMOD3<br>(12BBH)                                            |             | 7                 | 6                                        | 5      | 4      | 3 | 2 | 1 0               |
|                                                              | bit Symbol  | –                 | HADCH2                                   | HADCH1 | HADCH0 |   |   | –                 |
|                                                              | Read/Write  | R/W               |                                          |        |        |   |   | R/W               |
|                                                              | Reset State | 0                 | 0                                        | 0      | 0      |   |   | 0                 |
|                                                              | Function    | Always write "0". | Top-priority analog input channel select |        |        |   |   | Always write "0". |

→ Analog input channel select

| <HADCH2:0> | Analog input channel when High-priority conversion |
|------------|----------------------------------------------------|
| 000        | AN0                                                |
| 001        | AN1                                                |
| 010        | AN2                                                |
| 011        | AN3(Note)                                          |
| 100        | AN4                                                |
| 101        | AN5                                                |
| 110        | Reserved                                           |
| 111        | Reserved                                           |

Note: When using PG3 pin as  $\overline{\text{ADTRG}}$ , it cannot be set.

Figure 3.22.4 AD Conversion Registers

AD Mode Control Register 4 (AD Monitor function control)

|                   |             |                                                    |                                                    |                                                                                                                       |                                                                                                                       |                                                                            |                                                                            |                                                                                            |                                                                                            |
|-------------------|-------------|----------------------------------------------------|----------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------|----------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|
| ADMOD4<br>(12BCH) |             | 7                                                  | 6                                                  | 5                                                                                                                     | 4                                                                                                                     | 3                                                                          | 2                                                                          | 1                                                                                          | 0                                                                                          |
|                   | bit Symbol  | CMEN1                                              | CMEN0                                              | CMP1C                                                                                                                 | CMP0C                                                                                                                 | IRQEN1                                                                     | IRQEN0                                                                     | CMPINT1                                                                                    | CMPINT0                                                                                    |
|                   | Read/Write  | R/W                                                |                                                    |                                                                                                                       |                                                                                                                       |                                                                            |                                                                            | R                                                                                          |                                                                                            |
|                   | Reset State | 0                                                  | 0                                                  | 0                                                                                                                     | 0                                                                                                                     | 0                                                                          | 0                                                                          | 0                                                                                          | 0                                                                                          |
|                   | Function    | AD Monitor<br>function1<br>0: Disable<br>1: Enable | AD Monitor<br>function0<br>0: Disable<br>1: Enable | Generation<br>condition of<br>AD monitor<br>function<br>interrupt 1<br>0: less than<br>1: Greater<br>than or<br>Equal | Generation<br>condition of<br>AD monitor<br>function<br>interrupt 0<br>0: less than<br>1: Greater<br>than or<br>Equal | AD monitor<br>function<br>interrupt 1<br>0: Disable<br>1: Enable<br>(Note) | AD monitor<br>function<br>interrupt 0<br>0: Disable<br>1: Enable<br>(Note) | Status of<br>AD monitor<br>function<br>interrupt 1<br>0: No<br>generation<br>1: Generation | Status of<br>AD monitor<br>function<br>interrupt 0<br>0: No<br>generation<br>1: Generation |

Note: When AD monitor function interrupts generate, it is cleared automatically and it is set to disable condition.

AD Mode Control Register 5 (AD Monitor function control)

| AD Mode Control Register 5 (AD Monitor function control) |             |   |                                                                                                                                                                      |        |        |   |        |                                                                                                                                                                      |        |
|----------------------------------------------------------|-------------|---|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|---|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|
|                                                          |             | 7 | 6                                                                                                                                                                    | 5      | 4      | 3 | 2      | 1                                                                                                                                                                    | 0      |
| ADMOD5<br>(12BDH)                                        | bit Symbol  |   | CM1CH2                                                                                                                                                               | CM1CH1 | CM1CH0 |   | CM0CH2 | CM0CH1                                                                                                                                                               | CM0CH0 |
|                                                          | Read/Write  |   | R/W                                                                                                                                                                  |        |        |   | R/W    |                                                                                                                                                                      |        |
|                                                          | Reset State |   | 0                                                                                                                                                                    | 0      | 0      |   | 0      | 0                                                                                                                                                                    | 0      |
|                                                          | Function    |   | Select analog channel for AD monitor<br>function 1<br>000: AN0      100: AN4<br>001: AN1      101: AN5<br>010: AN2      110: Reserved<br>011: AN3      111: Reserved |        |        |   |        | Select analog channel for AD monitor<br>function 0<br>000: AN0      100: AN4<br>001: AN1      101: AN5<br>010: AN2      110: Reserved<br>011: AN3      111: Reserved |        |

Note1: When converting AD in hard ware trigger by setting <HHTRGE> and <HTRGE> to "1", set PGFC<PG3F> to "1" (as ADTRG) in case of external TRG before enabling it. When using an INTTBx0 of 16-bit timer, first set the <TSEL1:0> or <HTSEL1:0> bit to "00" when the timer is not operating. Then, set the <HHTRGE> and <HTRGE> to "1" and enable trigger operation. Finally, operate the timer so that AD conversion will be initiated at constant intervals.

Note 2: When disabling an external trigger ( $\overline{\text{ADTRG}}$ ) for AD conversion, first clear the <HHTRGE> or <HTRGE> bit to "0", and clear the PGFC<PG3F> to "0", thus configuring port G as a general-purpose port.

Note 3: When starting AD by using external trigger (ADTRG), it can be started after enabling (<HHTRGE> = "1" or <HTRGE> = "1") and 3 clock at  $f_{\text{SYS}}$  was executed. AD is not started when before that time.

Note 4: When chaging compare register value of AD Monitor function, change it after setting AD Monitor function to disable(ADMOD4<CMEN1:0> = "0").

Figure 3.22.5 AD Conversion Registers

AD Conversion Result Register 0 Low

|                    | 7           | 6                                              | 5     | 4 | 3 | 2 | 1                                             | 0                                            |
|--------------------|-------------|------------------------------------------------|-------|---|---|---|-----------------------------------------------|----------------------------------------------|
| ADREG0L<br>(12A0H) | bit Symbol  | ADR01                                          | ADR00 |   |   |   | OVR0                                          | ADR0RF                                       |
|                    | Read/Write  | R                                              |       |   |   |   | R                                             |                                              |
|                    | Reset State | 0                                              | 0     |   |   |   | 0                                             | 0                                            |
|                    | Function    | Store Lower 2 bits of AN0 AD conversion result |       |   |   |   | Overrun flag<br>0: No generate<br>1: Generate | AD conversion result store flag<br>1: Stored |

AD Conversion Result Register 0 High

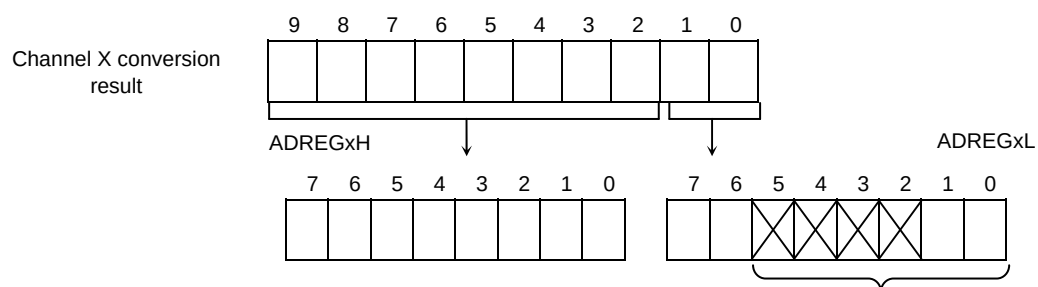
|                    | 7           | 6                                              | 5     | 4     | 3     | 2     | 1     | 0     |
|--------------------|-------------|------------------------------------------------|-------|-------|-------|-------|-------|-------|
| ADREG0H<br>(12A1H) | bit Symbol  | ADR09                                          | ADR08 | ADR07 | ADR06 | ADR05 | ADR04 | ADR03 |
|                    | Read/Write  | R                                              |       |       |       |       |       |       |
|                    | Reset State | 0                                              | 0     | 0     | 0     | 0     | 0     | 0     |
|                    | Function    | Store Upper 8 bits of AN0 AD conversion result |       |       |       |       |       |       |

AD Conversion Result Register 1 Low

|                    | 7           | 6                                              | 5     | 4 | 3 | 2 | 1                                             | 0                                            |
|--------------------|-------------|------------------------------------------------|-------|---|---|---|-----------------------------------------------|----------------------------------------------|
| ADREG1L<br>(12A2H) | bit Symbol  | ADR11                                          | ADR10 |   |   |   | OVR1                                          | ADR1RF                                       |
|                    | Read/Write  | R                                              |       |   |   |   | R                                             |                                              |
|                    | Reset State | 0                                              | 0     |   |   |   | 0                                             | 0                                            |
|                    | Function    | Store Lower 2 bits of AN1 AD conversion result |       |   |   |   | Overrun flag<br>0: No generate<br>1: Generate | AD conversion result store flag<br>1: Stored |

AD Conversion Result Register 1 High

|                    | 7           | 6                                              | 5     | 4     | 3     | 2     | 1     | 0     |
|--------------------|-------------|------------------------------------------------|-------|-------|-------|-------|-------|-------|
| ADREG1H<br>(12A3H) | bit Symbol  | ADR19                                          | ADR18 | ADR17 | ADR16 | ADR15 | ADR14 | ADR13 |
|                    | Read/Write  | R                                              |       |       |       |       |       |       |
|                    | Reset State | 0                                              | 0     | 0     | 0     | 0     | 0     | 0     |
|                    | Function    | Store Upper 8 bits of AN1 AD conversion result |       |       |       |       |       |       |



- Bits 5 ~ 2 are always read as "0".
- Bit 0 is the AD conversion result store flag <ADRxRF>. When AD conversion result is stored, the flag is set to "1". When Lower register (ADRECL) is read, this bit is cleared to "0".
- Bit 1 is the Overrun flag <OVRx>. This bit is set to "1" if a next conversion result is written to the ADREGxH/L before both the ADREGxH and ADREGxL are read. This bit is cleared to "0" by reading Flag.

Figure 3.22.6 AD Conversion Registers

AD Conversion Result Register 2 Low

|                    | 7           | 6                                              | 5     | 4 | 3 | 2 | 1                                             | 0                                            |
|--------------------|-------------|------------------------------------------------|-------|---|---|---|-----------------------------------------------|----------------------------------------------|
| ADREG2L<br>(12A4H) | bit Symbol  | ADR21                                          | ADR20 |   |   |   | OVR2                                          | ADR2RF                                       |
|                    | Read/Write  | R                                              |       |   |   |   | R                                             |                                              |
|                    | Reset State | 0                                              | 0     |   |   |   | 0                                             | 0                                            |
|                    | Function    | Store Lower 2 bits of AN2 AD conversion result |       |   |   |   | Overrun flag<br>0: No generate<br>1: Generate | AD conversion result store flag<br>1: Stored |

AD Conversion Result Register 1 High

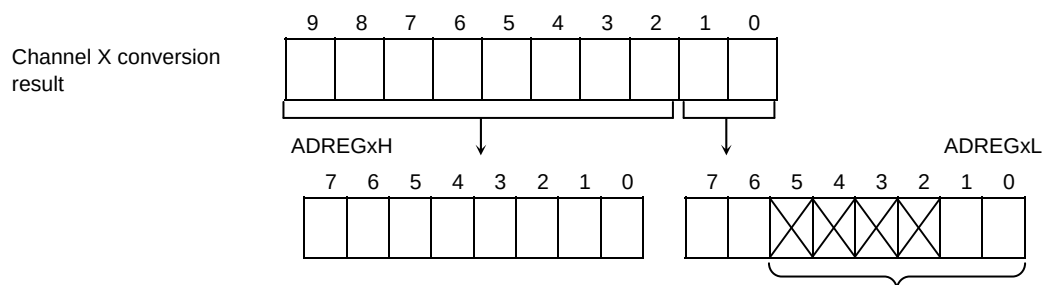
|                    | 7           | 6                                              | 5     | 4     | 3     | 2     | 1     | 0     |
|--------------------|-------------|------------------------------------------------|-------|-------|-------|-------|-------|-------|
| ADREG2H<br>(12A5H) | bit Symbol  | ADR29                                          | ADR28 | ADR27 | ADR26 | ADR25 | ADR24 | ADR23 |
|                    | Read/Write  | R                                              |       |       |       |       |       |       |
|                    | Reset State | 0                                              | 0     | 0     | 0     | 0     | 0     | 0     |
|                    | Function    | Store Upper 8 bits of AN2 AD conversion result |       |       |       |       |       |       |

AD Conversion Result Register 3 Low

|                    | 7           | 6                                              | 5     | 4 | 3 | 2 | 1                                             | 0                                            |
|--------------------|-------------|------------------------------------------------|-------|---|---|---|-----------------------------------------------|----------------------------------------------|
| ADREG3L<br>(12A6H) | bit Symbol  | ADR31                                          | ADR30 |   |   |   | OVR3                                          | ADR3RF                                       |
|                    | Read/Write  | R                                              |       |   |   |   | R                                             |                                              |
|                    | Reset State | 0                                              | 0     |   |   |   | 0                                             | 0                                            |
|                    | Function    | Store Lower 2 bits of AN3 AD conversion result |       |   |   |   | Overrun flag<br>0: No generate<br>1: Generate | AD conversion result store flag<br>1: Stored |

AD Conversion Result Register 3 High

|                    | 7           | 6                                              | 5     | 4     | 3     | 2     | 1     | 0     |
|--------------------|-------------|------------------------------------------------|-------|-------|-------|-------|-------|-------|
| ADREG3H<br>(12A7H) | bit Symbol  | ADR39                                          | ADR38 | ADR37 | ADR36 | ADR35 | ADR34 | ADR33 |
|                    | Read/Write  | R                                              |       |       |       |       |       |       |
|                    | Reset State | 0                                              | 0     | 0     | 0     | 0     | 0     | 0     |
|                    | Function    | Store Upper 8 bits of AN3 AD conversion result |       |       |       |       |       |       |



- Bits 5 ~ 2 are always read as “0”.
- Bit 0 is the AD conversion result store flag <ADR<sub>x</sub>RF>. When AD conversion result is stored, the flag is set to “1”. When Lower register (ADREC<sub>x</sub>L) is read, this bit is cleared to “0”.
- Bit 1 is the Overrun flag <OVR<sub>x</sub>>. This bit is set to “1” if a next conversion result is written to the ADREG<sub>x</sub>H/L before both the ADREG<sub>x</sub>H and ADREG<sub>x</sub>L are read. This bit is cleared to “0” by reading Flag.

Figure 3.22.7 AD Conversion Registers

AD Conversion Result Register 4 Low

|                 | 7           | 6                                              | 5     | 4 | 3 | 2 | 1                                             | 0                                            |
|-----------------|-------------|------------------------------------------------|-------|---|---|---|-----------------------------------------------|----------------------------------------------|
| ADREG4L (12A8H) | bit Symbol  | ADR41                                          | ADR40 |   |   |   | OVR4                                          | ADR4RF                                       |
|                 | Read/Write  | R                                              |       |   |   |   | R                                             |                                              |
|                 | Reset State | 0                                              | 0     |   |   |   | 0                                             | 0                                            |
|                 | Function    | Store Lower 2 bits of AN4 AD conversion result |       |   |   |   | Overrun flag<br>0: No generate<br>1: Generate | AD conversion result store flag<br>1: Stored |

AD Conversion Result Register 4 High

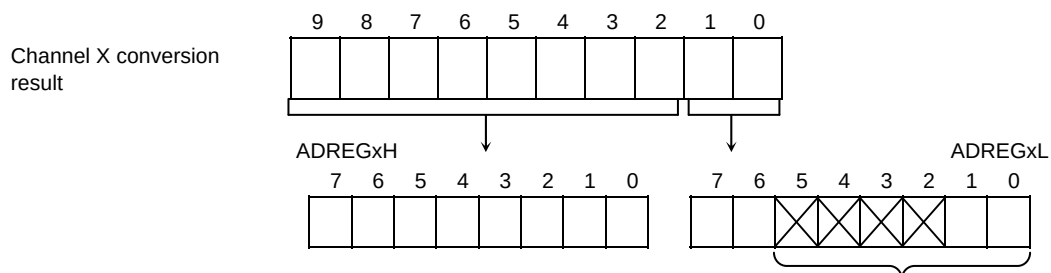
|                 | 7           | 6                                              | 5     | 4     | 3     | 2     | 1     | 0     |
|-----------------|-------------|------------------------------------------------|-------|-------|-------|-------|-------|-------|
| ADREG4H (12A9H) | bit Symbol  | ADR49                                          | ADR48 | ADR47 | ADR46 | ADR45 | ADR44 | ADR43 |
|                 | Read/Write  | R                                              |       |       |       |       |       |       |
|                 | Reset State | 0                                              | 0     | 0     | 0     | 0     | 0     | 0     |
|                 | Function    | Store Upper 8 bits of AN4 AD conversion result |       |       |       |       |       |       |

AD Conversion Result Register 5 Low

|                 | 7           | 6                                              | 5     | 4 | 3 | 2 | 1                                             | 0                                            |
|-----------------|-------------|------------------------------------------------|-------|---|---|---|-----------------------------------------------|----------------------------------------------|
| ADREG5L (12AAH) | bit Symbol  | ADR51                                          | ADR50 |   |   |   | OVR5                                          | ADR5RF                                       |
|                 | Read/Write  | R                                              |       |   |   |   | R                                             |                                              |
|                 | Reset State | 0                                              | 0     |   |   |   | 0                                             | 0                                            |
|                 | Function    | Store Lower 2 bits of AN5 AD conversion result |       |   |   |   | Overrun flag<br>0: No generate<br>1: Generate | AD conversion result store flag<br>1: Stored |

AD Conversion Result Register 5 High

|                 | 7           | 6                                              | 5     | 4     | 3     | 2     | 1     | 0     |
|-----------------|-------------|------------------------------------------------|-------|-------|-------|-------|-------|-------|
| ADREG5H (12ABH) | bit Symbol  | ADR59                                          | ADR58 | ADR57 | ADR56 | ADR55 | ADR54 | ADR53 |
|                 | Read/Write  | R                                              |       |       |       |       |       |       |
|                 | Reset State | 0                                              | 0     | 0     | 0     | 0     | 0     | 0     |
|                 | Function    | Store Upper 8 bits of AN5 AD conversion result |       |       |       |       |       |       |

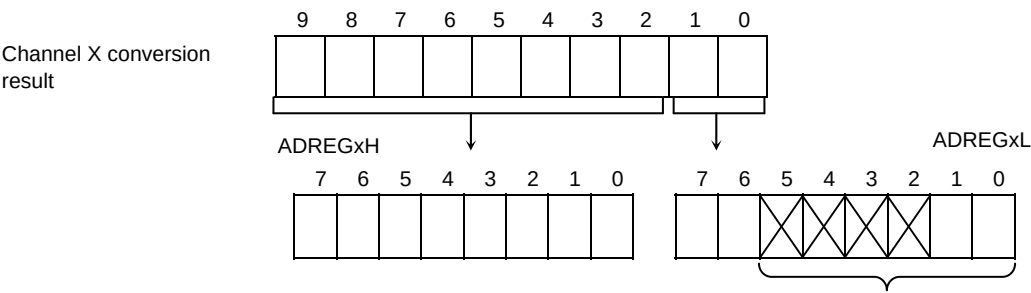


- Bits 5 ~ 2 are always read as “0”.
- Bit 0 is the AD conversion result store flag <ADRxRF>. When AD conversion result is stored, the flag is set to “1”. When Lower register (ADRECL) is read, this bit is cleared to “0”.
- Bit 1 is the Overrun flag <OVRx>. This bit is set to “1” if a next conversion result is written to the ADREGxH/L before both the ADREGxH and ADREGxL are read. This bit is cleared to “0” by reading Flag.

Figure 3.22.8 AD Conversion Registers

| Top-priority AD Conversion Result Register SP Low |             |                                               |        |   |   |   |                                               |                                              |
|---------------------------------------------------|-------------|-----------------------------------------------|--------|---|---|---|-----------------------------------------------|----------------------------------------------|
|                                                   | 7           | 6                                             | 5      | 4 | 3 | 2 | 1                                             | 0                                            |
| ADREGSPL<br>(12B0H)                               | bit Symbol  | ADRSP1                                        | ADRSP0 |   |   |   | OVSRP                                         | ADRSPRF                                      |
|                                                   | Read/Write  | R                                             |        |   |   |   | R                                             |                                              |
|                                                   | Reset State | 0                                             | 0      |   |   |   | 0                                             | 0                                            |
|                                                   | Function    | Store Lower 2 bits of an AD conversion result |        |   |   |   | Overrun flag<br>0: No generate<br>1: Generate | AD conversion result store flag<br>1: Stored |

| Top-priority AD Conversion Result Register SP High |             |                                               |        |        |        |        |        |        |
|----------------------------------------------------|-------------|-----------------------------------------------|--------|--------|--------|--------|--------|--------|
|                                                    | 7           | 6                                             | 5      | 4      | 3      | 2      | 1      | 0      |
| ADREGSPH<br>(12B1H)                                | bit Symbol  | ADRSP9                                        | ADRSP8 | ADRSP7 | ADRSP6 | ADRSP5 | ADRSP4 | ADRSP3 |
|                                                    | Read/Write  | R                                             |        |        |        |        |        |        |
|                                                    | Reset State | 0                                             | 0      | 0      | 0      | 0      | 0      | 0      |
|                                                    | Function    | Store Upper 8 bits of an AD conversion result |        |        |        |        |        |        |



- Bits 5 ~ 2 are always read as “0”.
- Bit 0 is the AD conversion result store flag <ADRxRF>. When AD conversion result is stored, the flag is set to “1”. When Lower register (ADRECL) is read, this bit is cleared to “0”.
- Bit 1 is the Overrun flag <OVRx>. This bit is set to “1” if a next conversion result is written to the ADREGxH/L before both the ADREGxH and ADREGxL are read. This bit is cleared to “0” by reading Flag.

Figure 3.22.9 AD Conversion Registers

AD Conversion Result Compare Criterion Register 0 Low

|                      | 7           | 6                                                               | 5     | 4 | 3 | 2 | 1 | 0 |
|----------------------|-------------|-----------------------------------------------------------------|-------|---|---|---|---|---|
| ADCM0REGL<br>(12B4H) | bit Symbol  | ADR21                                                           | ADR20 |   |   |   |   |   |
|                      | Read/Write  | R/W                                                             |       |   |   |   |   |   |
|                      | Reset State | 0                                                               | 0     |   |   |   |   |   |
|                      | Function    | Store Lower 2 bits of an AD conversion result compare criterion |       |   |   |   |   |   |

AD Conversion Result Compare Criterion Register 0 High

|                      | 7           | 6                                                               | 5     | 4     | 3     | 2     | 1     | 0     |
|----------------------|-------------|-----------------------------------------------------------------|-------|-------|-------|-------|-------|-------|
| ADCM0REGH<br>(12B5H) | bit Symbol  | ADR29                                                           | ADR28 | ADR27 | ADR26 | ADR25 | ADR24 | ADR23 |
|                      | Read/Write  | R/W                                                             |       |       |       |       |       |       |
|                      | Reset State | 0                                                               | 0     | 0     | 0     | 0     | 0     | 0     |
|                      | Function    | Store Upper 8 bits of an AD conversion result compare criterion |       |       |       |       |       |       |

AD Conversion Result Compare Criterion Register 1 Low

|                      | 7           | 6                                                               | 5     | 4 | 3 | 2 | 1 | 0 |
|----------------------|-------------|-----------------------------------------------------------------|-------|---|---|---|---|---|
| ADCM1REGL<br>(12B6H) | bit Symbol  | ADR21                                                           | ADR20 |   |   |   |   |   |
|                      | Read/Write  | R/W                                                             |       |   |   |   |   |   |
|                      | Reset State | 0                                                               | 0     |   |   |   |   |   |
|                      | Function    | Store Lower 2 bits of an AD conversion result compare criterion |       |   |   |   |   |   |

AD Conversion Result Compare Criterion Register 1 High

|                      | 7           | 6                                                               | 5     | 4     | 3     | 2     | 1     | 0     |
|----------------------|-------------|-----------------------------------------------------------------|-------|-------|-------|-------|-------|-------|
| ADCM1REGH<br>(12B7H) | bit Symbol  | ADR29                                                           | ADR28 | ADR27 | ADR26 | ADR25 | ADR24 | ADR23 |
|                      | Read/Write  | R/W                                                             |       |       |       |       |       |       |
|                      | Reset State | 0                                                               | 0     | 0     | 0     | 0     | 0     | 0     |
|                      | Function    | Store Upper 8 bits of an AD conversion result compare criterion |       |       |       |       |       |       |

Note: Disable the AD monitor function (ADMOD4<CMEN1:0> = "0") before attempting to set or modify the value of these registers.

Figure 3.22.10 AD Conversion Registers

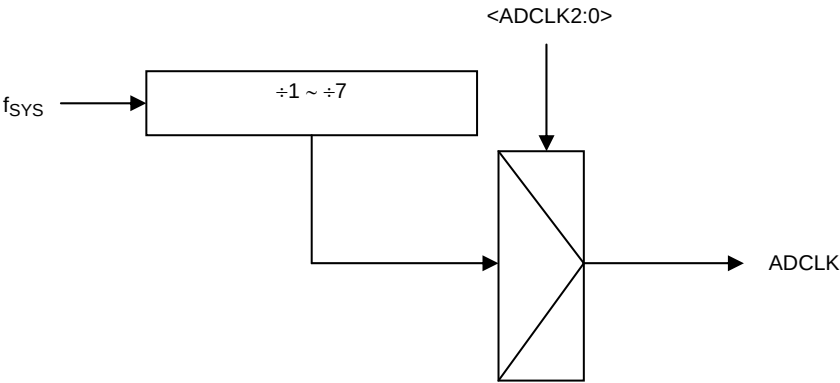


| AD Conversion Clock Setting Register |             |   |   |   |   |                     |                                |                 |
|--------------------------------------|-------------|---|---|---|---|---------------------|--------------------------------|-----------------|
| ADCCLK<br>(12BFH)                    |             | 7 | 6 | 5 | 4 | 3                   | 2                              | 1 0             |
|                                      | bit Symbol  |   |   |   |   | –                   | ADCLK2                         | ADCLK1 ADCLK0   |
|                                      | Read/Write  |   |   |   |   | R/W                 |                                |                 |
|                                      | Reset State |   |   |   |   | 0                   | 0                              | 0 0             |
|                                      | Function    |   |   |   |   | Always<br>write “0” | Select clock for AD conversion |                 |
|                                      |             |   |   |   |   |                     | 000: Reserved                  | 100: $f_{IO}/4$ |
|                                      |             |   |   |   |   |                     | 001: $f_{IO}/1$                | 101: $f_{IO}/5$ |
|                                      |             |   |   |   |   |                     | 010: $f_{IO}/2$                | 110: $f_{IO}/6$ |
|                                      |             |   |   |   |   |                     | 011: $f_{IO}/3$                | 111: $f_{IO}/7$ |

Note1: AD conversion is executed at the clock frequency selected in the above register. To assure conversion accuracy, however, the conversion clock frequency must not exceed 12MHz.

Note2: Don 't change the clock frequency while AD conversion is in progress.

Figure 3.22.11 AD Conversion Registers



| $f_{IO}(f_{sys}/2)$ | $\langle ADCLK2:0 \rangle$ | ADCLK   | AD conversion speed |
|---------------------|----------------------------|---------|---------------------|
| 40MHz               | 100( $f_{IO}/4$ )          | 10.0MHZ | 12 $\mu$ sec        |
|                     | 101( $f_{IO}/5$ )          | 8MHZ    | 15 $\mu$ sec        |
| 30MHz               | 011( $f_{IO}/3$ )          | 10.0MHZ | 12 $\mu$ sec        |
|                     | 100( $f_{IO}/4$ )          | 7.5MHZ  | 16 $\mu$ sec        |

AD conversion speed can be calculated by following.

Conversion speed =  $120 \times (1/ADCLK)$

### 3.22.2 Operation

#### 3.22.2.1 Analog Reference Voltages

Apply the analog reference voltage's "H" level side to the VREFH pin and the "L" level side to the VREFL pin.

#### 3.22.2.2 Selecting Analog Input Channels

Selecting an analog input channel depends on the operation mode of the AC converter.

##### (1) For normal AD conversion

When using an analog input channel in fix mode, select one channel from the AN0 to AN5 pins by setting (ADMOD1<SCAN> = "0") ADMOD1<ADCH2:0>.

When using an analog input channel in scan mode, select one scan mode from the six scan modes by setting (ADMOD1<SCAN> = "1") ADMOD1 <ADCH2:0>.

##### (2) For top-priority AD conversion

Select one channel from the analog input pins AN0 to AN5 by setting ADMOD3<HADCH2:0>.

After reset, ADMOD1<SCAN> is initialized to "0" and ADMOD1<ADCH2:0> to "000". Since these settings are used for channel selection, the channel fixed input with the AN0 pin will be selected. Pins not used as analog input channels can be used as normal ports.

### 3.22.2.3 Starting an AD Conversion

The AD conversion has the two types of normal AD conversion and top-priority AD conversion.

Normal AD conversion can be started up by setting ADMOD0<ADS> to “1.” Top-priority AD conversion can be started up by software by setting ADMOD2<HADS> to “1.”

For normal AD conversion, one operation mode is selected from the four types of operation modes specified by ADMOD1<REPEAT, SCAN>. The operation mode for top-priority AD conversion is only single conversion by channel-fix mode.

The ADC supports two types of AD conversion: normal AD conversion and Top-priority AD conversion. The ADC initiates a normal AD conversion by software when the ADMOD0<ADS> is set to “1”. It initiates a Top-priority AD conversion by software when the ADMOD2<HADS> is set to “1”. For a normal AD conversion, ADMOD1<REPEAT, SCAN> select one of four conversion modes. For a Top-priority AD conversion, the ADC only supports Fixed-Channel Single Conversion mode.

The ADMOD0<TSEL1:0> and ADMOD2<HTSEL1:0> enable a hardware trigger for a normal and Top-priority AD conversion, respectively. When these bits are set to “10”, a normal or Top-priority AD conversion is triggered by a falling edge applied to  $\overline{\text{ADTRG}}$  pin. When ADMOD0<TSEL1:0> is set to “00”, a normal AD conversion is triggered by INTTB00 of 16-Bit Timer interrupt. When ADMOD2<HTSEL1:0> is set to “00”, a Top-priority AD conversion is triggered by INTTB10 of 16-Bit Timer interrupt. If this bit is “11”, it is triggered by I<sup>2</sup>S sampling block. Even when a hardware trigger is enabled, software starting can be used.

Note: If changing HTSEL at HHTRGE is “ON”, maybe unexpected interrupts occurs. If changing HTSEL, once set HHTRGE to “OFF”.

When normal AD conversion is started, the AD conversion BUSY flag (ADMOD0<BUSY>) that shows the state for AD being converted is set to “1.”

When top-priority AD conversion is started, the AD conversion BUSY flag (ADMOD2<HBUSY>) that shows the state for AD being converted is set to “1.”

In addition, when top-priority conversion is started during normal AD conversion, ADMOD0<BUSY> is kept to “1.”

<HEOS> and <EOS> are set to “1” after conversion is completed. This flag is cleared to “0” only when read.

During a normal AD conversion, writing a “1” to ADMOD0<ADS> causes the ADC to abort any ongoing conversion immediately, and restart.

During a normal AD conversion, if normal AD conversion starting is enabled by hard ware trigger, normal AD conversion is restarted when start condition from hard ware trigger is satisfied. When restart is set, normal AD conversion is aborted immediately.

During a normal AD conversion, if a Top-priority AD conversion starts (writing a “1” to ADMOD2<HADS> or a hard ware trigger occurs), the ADC aborts any ongoing conversion immediately, and then start a Top-priority AD conversion for the channel specified by ADMOD3<HADCH2:0>. Upon the completion of the Top-priority conversion, the ADC stores the conversion result to ADREGSPH/L, and then resumes the suspended normal conversion with that channel.

Note: It cannot overlap with three or more AD conversions.

Prohibition example 1: In FIRST normal AD conversion

- (Before finished FIRST normal AD conversion) Started SECOND normal AD conversion
- (Before finished SECOND normal AD conversion) Started THIRD normal AD conversion

Prohibition example 2: In FIRST normal AD conversion

- (Before finished FIRST normal AD conversion) Started SECOND normal AD conversion
- (Before finished SECOND normal AD conversion) Started THIRD high-priority AD conversion

### 3.22.2.4 AD Conversion Modes and AD Conversion-End Interrupts

For AD conversion, the following four operation modes are provided: For normal AD conversion, selection is available by setting ADMOD1<REPEAT and SCAN>. As for top-priority AD conversion, only single conversion mode by channel-fix mode is available.

- a. Channel-fix single conversion mode
- b. Channel-scan single conversion mode
- c. Channel-fix repeat conversion mode
- d. Channel-scan repeat conversion mode

#### (1) Normal AD conversion

To select operation modes, use ADMOD1<REPEAT, SCAN>. After AD conversion is started, ADMOD0<BUSY> is set to “1.” When a specified AD conversion ends, the Normal AD conversion end interrupt (INTAD) is generated, which sets “1” in ADMOD0<EOS> is set “1”, that shows the end of the AD conversion sequence.

##### a. Channel-fix single conversion mode

Setting ADMOD1<REPEAT, SCAN> to “00” selects the channel-fix single conversion mode.

This mode performs a conversion only one time at one channel selected. After conversion ends, ADMOD0<EOS> is set to “1,” generating Normal AD conversion End an INTAD interrupt request. <EOS> is cleared to “0” only by being read.

##### b. Channel-scan single conversion mode

Setting ADMOD1<REPEAT, SCAN> to “01” selects the channel-scan single conversion mode.

This mode performs a conversion only one time at each scan channel selected. After scan conversion ends, ADMOD0<EOS> is set to “1,” generating Normal AD conversion End interrupt request. <EOS> is cleared to “0” only by being read.

##### c. Channel-fix repeat conversion mode

Setting ADMOD1<REPEAT, SCAN> to “10” selects the channel-fix repeat conversion mode.

This mode performs a conversion at one channel selected repeatedly. After conversion ends, ADMOD0<EOS> is set to “1.” The timing of Normal AD conversion End INTAD interrupt request generation can be selected by setting ADMOD1 <ITM>. The timing of <EOS> being set is also linked to the interrupt timing.

ADMOD0<EOS> is cleared to “0” only by being read.

Setting <ITM> to “0” generates an interrupt request each time an AD conversion ends. In this case, conversion results are always stored into the storage register of ADREGxH/L. At the point of storage, <EOS> is set to 1.

Setting <ITM> to “1” generates an interrupt request each time four AD conversions end. In this case, conversion results are stored into the storage registers of ADREG0H/L to ADREG3H/L one after another. After stored into ADREG3, <EOS> is set to “1,” restarting storage from ADREG0. ADMOD0<EOS> is set to “1” after a fourth conversion result is stored. <EOS> is cleared to “0” only by being read.

## d. Channel-scan repeat conversion mode

Setting ADMOD1<REPEAT, SCAN> to “11” selects the channel-scan repeat conversion mode.

This mode performs a conversion at selected scan channels repeatedly. Each time after the conversion at a final channel ends, ADMOD0<EOS> is set to “1,” generating Normal AD conversion End interrupt request. <EOS> is cleared to “0” only by being read.

To stop the repeat conversion mode (mode of c and d) operation, write “0” in ADMOD1<REPEAT>. At the point when a scan conversion being executed ends, the repeat conversion mode ends.

Shift to a standby mode (IDLE2 Mode with ADMOD0<I2AD> = “0”, IDLE1 Mode or STOP Mode) immediately stops operation of the AD converter even if AD conversion is still in progress. Therefore, ADC may consume current even if operation is stopped, depending on stop condition of ADC that switches to standby mode. For avoiding this problem, Stop ADC before switching to standby mode.

## (2) Top-priority AD conversion

The operation mode is only single conversion by channel-fix mode. The settings in ADMOD1<REPEAT, SCAN> are not involved.

When startup conditions are established, a conversion at a channel specified by ADMOD3<HADCH2:0> is performed only one time. When conversion ends, the top-priority AD conversion end interrupt (INTADHP) is generated, which sets “1” in ADMOD2<HEOS>. The HEOS flag is cleared to “0” only by being read.

Table 3.22.1 Interrupt Generation Timing and Flag Setting in Each AD Conversion Mode

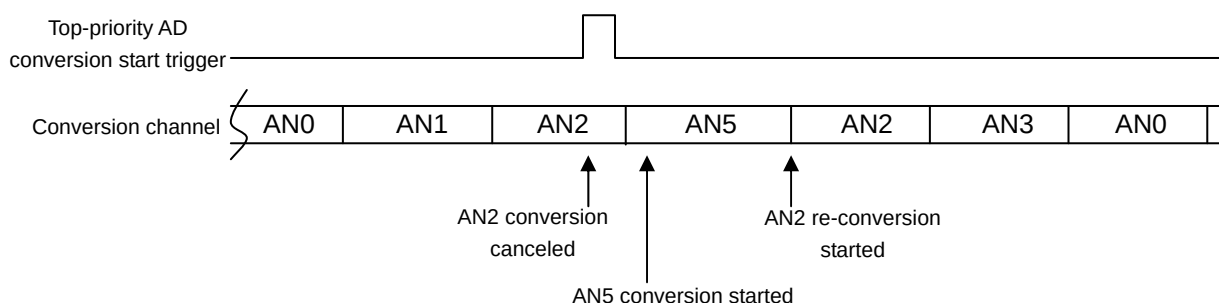
| Conversion mode                | Interrupt Generation Timing              | EOS set timing (Note)                    | ADMOD1 |        |      |
|--------------------------------|------------------------------------------|------------------------------------------|--------|--------|------|
|                                |                                          |                                          | ITM    | REPEAT | SCAN |
| Channel-fix Single conversion  | After conversion end                     | After conversion end                     | –      | 0      | 0    |
| Channel-fix Repeat conversion  | Per one conversion                       | Each time after one conversion ends      | 0      | 1      | 0    |
|                                | Per four conversions                     | Each time after four conversions end     | 1      |        |      |
| Channel-scan Single conversion | After scan conversion end                | After scan conversion end                | –      | 0      | 1    |
| Channel-scan Repeat conversion | Each time after one scan conversion ends | Each time after one scan conversion ends | –      | 1      | 1    |

Note: EOS is cleared to “0” only by reading this bit.

### 3.22.2.5 Top-Priority Conversion Mode

The ADC can perform a Top-priority AD conversion while it is performing a normal AD conversion sequence. A Top-priority AD conversion can be started at software by setting the ADMOD2<HADS> to “1”. It is also triggered by a hardware trigger if so enabled using ADMOD2<HTSEL1:0>. If a Top-priority AD conversion is triggered during a normal AD conversion, the ADC aborts any ongoing conversion immediately, and then begins a single Top-priority AD conversion for the channel specified with the ADMOD3<HADC2:0>. Upon the completion of the Top-priority AD conversion, the ADC stores the results of the conversion in the ADREGSPH/L, generates the Top-priority AD conversion interrupt (INTADHP), and then resumes the suspended normal conversion with that channel. While a Top-priority conversion is being performed, a trigger for another Top-priority conversion is ignored.

Example: When AN5 top-priority AD conversion is started up with ADMOD3<HADC2:0> = “101” during repeat scan conversion at channels AN0 to AN3 with ADMOD1<REPEAT, SCAN> = “11” and ADMOD1<ADCH2:0> = “011”



### 3.22.2.6 AD Monitor Function

Setting ADMOD4<CMEN1:0> to “1” enables the AD monitoring function.

The value of Result storage register that is appointed by ADMOD5 is compared with the value of AD conversion result register (H/L), ADMOD4<CMP1C:0C> can select greater or smaller of comparison format. As register ADMOD4<IRQEN1:0> is Enable,

This comparison operation is performed each time when a result is stored in the corresponding conversion result storage register. When conditions are met, the interrupt is generated. Be careful that the storage registers assigned for the AD monitoring function are usually not ready by software, which means that the overrun flag <OVRx> is always set and the conversion result storage flag <ADRxRF> is also set.

If each of them is assigned to separate channels, the monitoring of greater or smaller is possible in the two analog channels. In addition, if assigned to the same channels, the monitoring with the voltage range set is possible.

### 3.22.2.7 AD Conversion Time

One AD conversion takes 120 clocks including sampling clocks. The AD conversion clock is selected from 1/1 to 1/7  $f_{IO}$  by ADCLK <ADCLK2:0>. To meet the guaranteed accuracy, the AD conversion clock needs to be set to 12 MHz or less; or equivalently 10  $\mu$ s or more of AD conversion time.

### 3.22.2.8 Storing and Read of AD Conversion Results

AD conversion results are stored in the AD conversion result higher-order/lower-order registers (ADREG0H/L~ ADREG5H/L) for the normal AD conversion (ADREG0H/L to ADREG5H/L are read-only registers)

In the channel-fix repeat conversion mode, AD conversion results are stored into ADREG0H/L to ADREG3H/L one after another. In other modes, the conversion results of channels AN0, AN1, AN2, AN3, AN4, and AN5 are each stored into ADREG0H/L, ADREG1H/L, ADREG2H/L, ADREG3H/L, ADREG4H/L, and ADREG5H/L.

Table 3.22.2 shows the correspondence between analog input channels and AD conversion result registers.

Table 3.22.2 Correspondence between analog input channels and AD conversion result registers

| Analog input channel<br>(Port G) | AD Conversion result registers                       |                                                        |
|----------------------------------|------------------------------------------------------|--------------------------------------------------------|
|                                  | Other conversion<br>modes than shown in<br>the right | Channel-fix repeat<br>conversion mode<br>(per 4 times) |
| AN0                              | ADREG0H/L                                            |                                                        |
| AN1                              | ADREG1H/L                                            |                                                        |
| AN2                              | ADREG2H/L                                            |                                                        |
| AN3                              | ADREG3H/L                                            |                                                        |
| AN4                              | ADREG4H/L                                            |                                                        |
| AN5                              | ADREG5H/L                                            |                                                        |

Note: In order to detect overruns without omission, read the conversion result storage register's higher-order bits first, and then read the lower-order bits next. As this result, receiving the result of OVRn = "0" and ADnRF = "1" for overruns existing in the lower-order bits means that a correct conversion result has been obtained.

### 3.22.2.9 Data Polling

To process AD conversion results by using data polling without using interrupts, perform a polling on ADMOD0<EOS>. After confirming that ADMOD0<EOS> is set to "1," read the AD conversion storage register.



Setting example:

1. Convert the analog input voltage on the AN3 pin and write the result to memory address 2800H using the AD interrupt(INTAD) processing routine.

Main routine

|        | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                         |
|--------|---|---|---|---|---|---|---|---|---------------------------------------------------------|
| INTEAD | ← | 1 | 1 | 0 | 0 | — | — | — | Enable INTAD and set it to interrupt level 4.           |
| ADMOD1 | ← | 1 | 1 | 0 | 0 | 0 | 0 | 1 | Set pin AN3 to be the analog input channel.             |
| ADMOD0 | ← | X | X | 0 | 0 | 0 | 0 | 0 | Start conversion in channel-fix single conversion mode. |

Interrupt routine processing example

|         |   |        |                                                                             |
|---------|---|--------|-----------------------------------------------------------------------------|
| WA      | ← | ADREG3 | Read value of ADREG3L and ADREG3H into 16-bits general-purpose register WA. |
| WA      | ← | >> 6   | Shift contents read into WA six times to right and zero fill upper bits.    |
| (2800H) | ← | WA     | Write contents of WA to memory address 2800H.                               |

2. This example repeatedly converts the analog input voltages on the three pins AN0, AN1 and AN2, using channel-scan repeat conversion mode.

|        |   |   |   |   |   |   |   |   |                                                          |
|--------|---|---|---|---|---|---|---|---|----------------------------------------------------------|
| INTEAD | ← | 1 | 0 | 0 | 0 | — | — | — | Disable INTAD.                                           |
| ADMOD1 | ← | 1 | 1 | 0 | 0 | 0 | 0 | 1 | Set pins AN0 to AN2 to be the analog input channels.     |
| ADMOD0 | ← | X | X | 0 | 0 | 0 | 1 | 1 | Start conversion in channel-scan repeat conversion mode. |

3. Convert the analog input voltage on the AN2 pin as a Top-priority AD conversion, and write the result to memory address 2A00H using the Top-priority AD interrupt (INTADHP) processing routine.

Main routine

|        |   |   |   |   |   |   |   |   |                                                 |
|--------|---|---|---|---|---|---|---|---|-------------------------------------------------|
| INTEAD | ← | 1 | 1 | 0 | 1 | — | — | — | Enable INTADHP and set it to interrupt level 6. |
| ADMOD1 | ← | 1 | 0 | 0 | 0 | 0 | 0 | 0 | DAC On.                                         |
| ADMOD3 | ← | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Set pin AN2 to be the analog input channel.     |
| ADMOD2 | ← | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Start a Top-priority AD conversion by software. |

Interrupt routine processing example

|         |   |         |                                                                               |
|---------|---|---------|-------------------------------------------------------------------------------|
| WA      | ← | ADREGSP | Read value of ADREGSPL and ADREGSPH into 16-bits general-purpose register WA. |
| WA      | ← | >> 6    | Shift contents read into WA six times to right and zero fill upper bits.      |
| (2A00H) | ← | WA      | Write contents of WA to memory address 2A00H.                                 |

4. Convert the analog input voltage on the AN4 pin as a normal AD conversion of a channel-fix single conversion mode. And then if its conversion result is greater or equal than the value of (ADCM0REGL/H), write the result to memory address 2C00H using the AD monitor function interrupt (INTADM) processing routine.

Main routine

|        |   |   |   |   |   |   |   |   |   |                                                                                                                                                                                                            |
|--------|---|---|---|---|---|---|---|---|---|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| INTEAD | ← | — | — | — | — | 1 | 0 | 1 | 1 | Enable INTAD and set it to interrupt level 3.                                                                                                                                                              |
| ADMOD5 | ← | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Set the analog input channel AN4 for AD monitor function 0.                                                                                                                                                |
| ADMOD4 | ← | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Enable the AD monitor function0 and AD monitor function interrupt 0. Set "a conversion result ≥ AD conversion result compare criterion register" for generation condition of monitor function interrupt 0. |
| ADMOD1 | ← | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Set pin AN4 to be the analog input channel.                                                                                                                                                                |
| ADMOD0 | ← | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Start a normal AD conversion by software.                                                                                                                                                                  |

Interrupt routine processing example

|         |   |        |                                                                             |
|---------|---|--------|-----------------------------------------------------------------------------|
| WA      | ← | ADREG4 | Read value of ADREG4L and ADREG4H into 16-bits general-purpose register WA. |
| WA      | ← | >> 6   | Shift contents read into WA six times to right and zero fill upper bits.    |
| (2C00H) | ← | WA     | Write contents of WA to memory address 2C00H.                               |

X : Don't care, —: No change

### 3.23 Watchdog Timer (Runaway detection timer)

The TMP92CF30 contains a watchdog timer of runaway detecting.

The watchdog timer (WDT) is used to return the CPU to the normal state when it detects that the CPU has started to malfunction (runaway) due to causes such as noise. When the watchdog timer detects a malfunction, it generates a non-maskable interrupt INTWD to notify the CPU of the malfunction.

Connecting the watchdog timer output to the reset pin internally forces a reset.

(The level of external  $\overline{\text{RESET}}$  pin is not changed.)

#### 3.23.1 Configuration

Figure 3.23.1 is a block diagram of the watchdog timer (WDT).

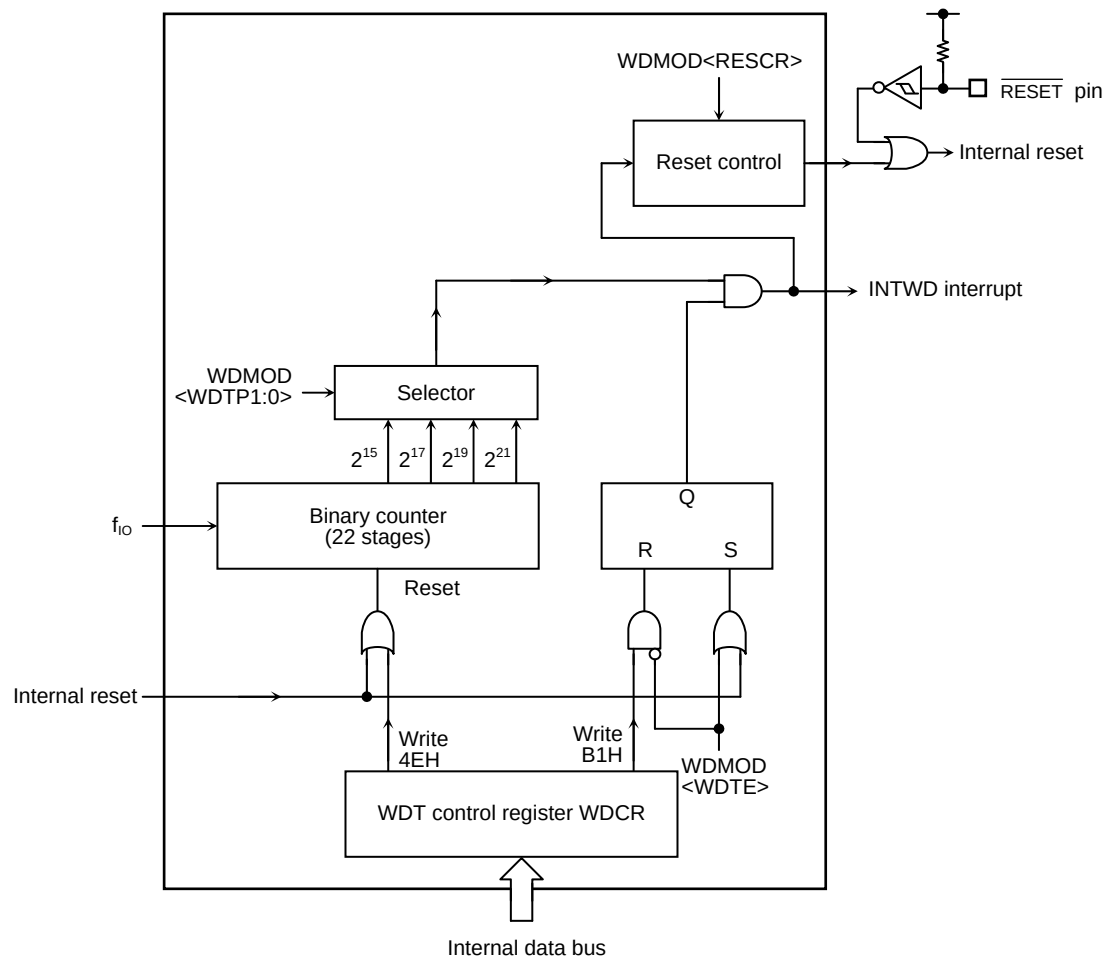


Figure 3.23.1 Block Diagram of Watchdog Timer

Note: Care must be exercised in the overall design of the apparatus since the watchdog timer may fail to function correctly due to external noise, etc.

### 3.23.2 Operation

The watchdog timer generates an INTWD interrupt when the detection time set in the WDMOD<WDTP1:0> has elapsed. The watchdog timer must be cleared “0” in software before an INTWD interrupt will be generated. If the CPU malfunctions (e.g., if runaway occurs) due to causes such as noise, but does not execute the instruction used to clear the binary counter, the binary counter will overflow and an INTWD interrupt will be generated. The CPU will detect malfunction (runaway) due to the INTWD interrupt and in this case it is possible to return to the CPU to normal operation by means of an anti-malfunction program.

The watchdog timer begins operating immediately on release of the watchdog timer reset.

The watchdog timer is halted in IDLE1 or STOP mode. The watchdog timer counter continues counting during bus release (when  $\overline{\text{BUSAK}}$  goes low).

When the device is in IDLE2 mode, the operation of WDT depends on the WDMOD<I2WDT> setting. Ensure that WDMOD<I2WDT> is set before the device enters IDLE2 mode.

The watchdog timer consists of a 22-stage binary counter which uses the clock ( $f_{\text{IO}}$ ) as the input clock. The binary counter can output  $2^{15}/f_{\text{IO}}$ ,  $2^{17}/f_{\text{IO}}$ ,  $2^{19}/f_{\text{IO}}$  and  $2^{21}/f_{\text{IO}}$ .

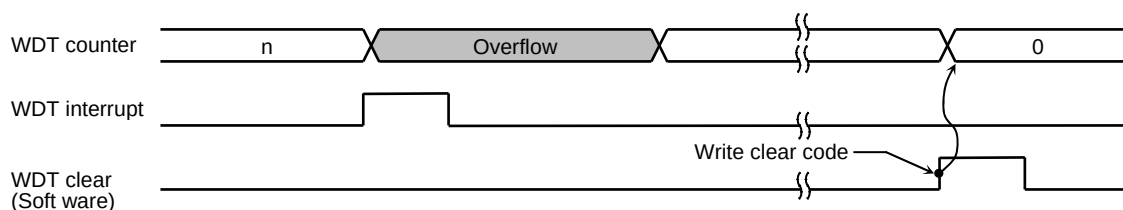


Figure 3.23.2 Normal Mode

The runaway detection result can also be connected to the reset pin internally.

In this case, the reset time will be 32 clocks ( $102.4 \mu\text{s}$  at  $f_{\text{OSCH}} = 10 \text{ MHz}$ ) as shown in Figure 3.23.3. After a reset, the clock  $f_{\text{IO}}$  is divided  $f_{\text{SYS}}$  by two, where  $f_{\text{SYS}}$  is generated by dividing the high-speed oscillator clock ( $f_{\text{OSCH}}$ ) by sixteen through the clock gear function.

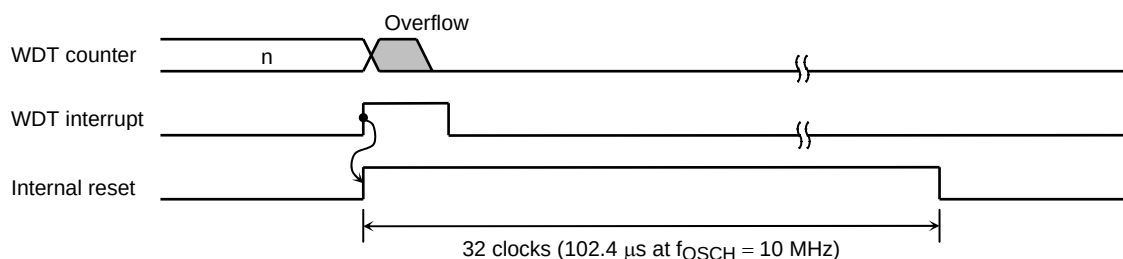


Figure 3.23.3 Reset Mode

### 3.23.3 Control Registers

The watchdog timer (WDT) is controlled by two control registers WDMOD and WDCR.

#### (1) Watchdog timer mode registers (WDMOD)

##### 1. Setting the detection time for the watchdog timer in <WDTP1:0>

This 2-bit register is used for setting the watchdog timer interrupt time used when detecting runaway.

On a reset this register is initialized to WDMOD<WDTP1:0> = "00".

The detection time for WDT is  $2^{15}/f_{IO}$  [s]. (The number of system clocks is approximately 65,536.)

##### 2. Watchdog timer enable/disable control register <WDTE>

At reset, the WDMOD<WDTE> is initialized to "1", enabling the watchdog timer.

To disable the watchdog timer, it is necessary to clear this bit to "0" and to write the disable code (B1H) to the watchdog timer control register (WDCR). This makes it difficult for the watchdog timer to be disabled by runaway.

However, it is possible to return the watchdog timer from the disabled state to the enabled state merely by setting <WDTE> to "1".

##### 3. Watchdog timer out reset connection <RESCR>

This register is used to connect the output of the watchdog timer with the RESET terminal internally. Since WDMOD<RESCR> is initialized to "0" at reset, a reset by the watchdog timer will not be performed.

#### (2) Watchdog timer control register (WDCR)

This register is used to disable and clear the binary counter for the watchdog timer.

##### • Disable control

The watchdog timer can be disabled by clearing WDMOD<WDTE> to "0" and then writing the disable code (B1H) to the WDCR register.

|       |   |   |   |   |   |   |   |   |   |                               |
|-------|---|---|---|---|---|---|---|---|---|-------------------------------|
| WDCR  | ← | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | Write the clear code (4EH).   |
| WDMOD | ← | 0 | – | – | X | X | – | – | 0 | Clear WDMOD <WDTE> to "0".    |
| WDCR  | ← | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | Write the disable code (B1H). |

##### • Enable control

Set WDMOD<WDTE> to "1".

##### • Watchdog timer clear control

To clear the binary counter and cause counting to resume, write the clear code (4EH) to the WDCR register.

|      |   |   |   |   |   |   |   |   |   |                             |
|------|---|---|---|---|---|---|---|---|---|-----------------------------|
| WDCR | ← | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | Write the clear code (4EH). |
|------|---|---|---|---|---|---|---|---|---|-----------------------------|

Note1: If the disable control is used, set the disable code (B1H) to WDCR after write the clear code (4EH) once.

(Please refer to setting example.)

Note2: If the watchdog timer setting is changed, change setting after setting to disable condition once.

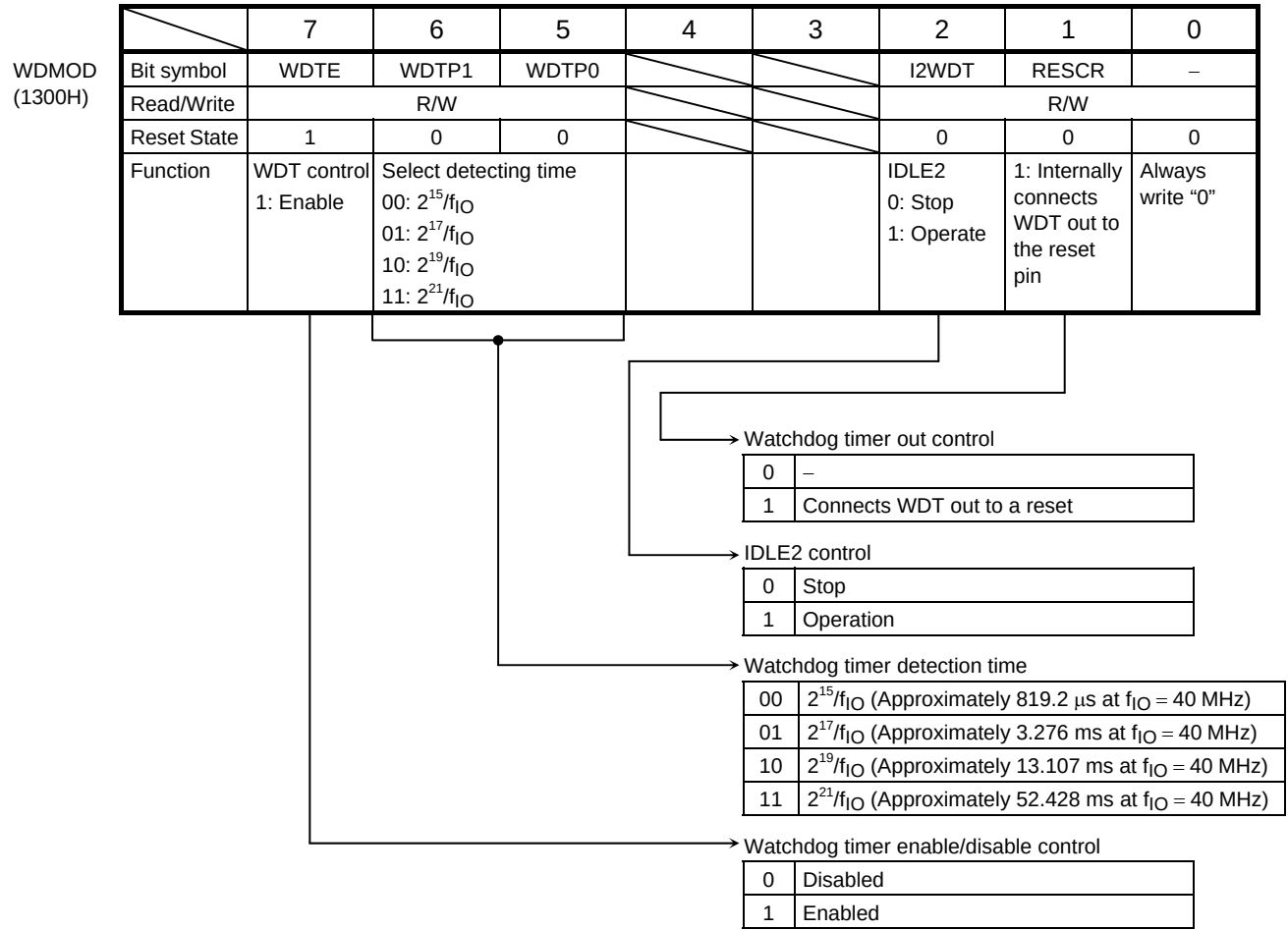


Figure 3.23.4 Watchdog Timer Mode Register

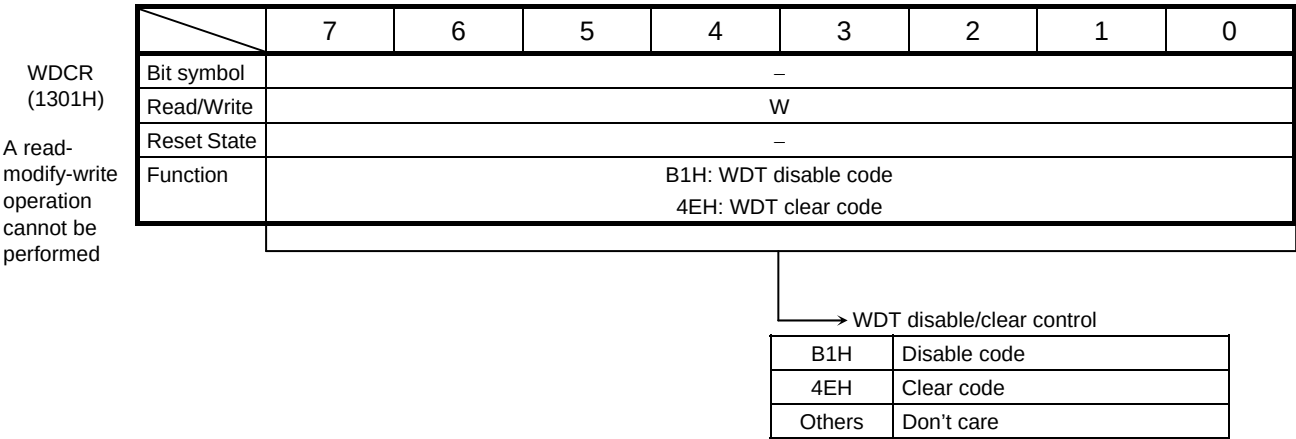


Figure 3.23.5 Watchdog Timer Control Register

### 3.24 Multiply and Accumulate Calculation Unit (MAC)

The TMP92CF30 includes a multiply-accumulate unit (MAC) capable of 32-bit  $\times$  32-bit + 64-bit arithmetic operations at high speed. The MAC has the following features:

- One-cycle execution for all MAC operations (excluding register access time)
- Three operation modes : 1) 64-bit + 32-bit  $\times$  32-bit  
2) 64-bit – 32-bit  $\times$  32-bit  
3) 32-bit  $\times$  32-bit – 64-bit
- Support for signed/unsigned operations
- Support for integer operations only

#### 3.24.1 Registers

The MAC in the TMP92CF30 has one control register and three data registers. These registers are connected to the CPU via a 32-bit bus and can be accessed in one system clock ( $f_{SYS}$ ).

##### 3.24.1.1 Control Register

The control register is used to control the operation of the MAC.

| MAC Control Register                              |             |                                                         |                                                                 |                                                                                                                                                                               |        |        |                                       |                                                                                        |        |
|---------------------------------------------------|-------------|---------------------------------------------------------|-----------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|---------------------------------------|----------------------------------------------------------------------------------------|--------|
|                                                   | 7           | 6                                                       | 5                                                               | 4                                                                                                                                                                             | 3      | 2      | 1                                     | 0                                                                                      |        |
| MACCR<br>(1BFCH)                                  | bit Symbol  | MOVF                                                    | MOPST                                                           | MSTTG2                                                                                                                                                                        | MSTTG1 | MSTTG0 | MSGMD                                 | MOPMD1                                                                                 | MOPMD0 |
|                                                   | Read/Write  | R/W                                                     | W                                                               | R/W                                                                                                                                                                           |        |        |                                       |                                                                                        |        |
| A read-modify-write operation cannot be performed | Reset State | 0                                                       | 0                                                               | 0                                                                                                                                                                             | 0      | 0      | 0                                     | 0                                                                                      | 0      |
|                                                   | Function    | Overflow flag<br>0: No overflow<br>1: Overflow occurred | Calculation soft start<br>0: Don't care<br>1: Start calculation | Calculation start trigger<br>000: Write to MACMA<7:0><br>001: Write to MACMB<7:0><br>010: Write to MACMOR<7:0><br>011: Write to MACMOR<39:32><br>1xx: Write of "1" to <MOPST> |        |        | Sign mode<br>0: Unsigned<br>1: Signed | Calculation mode<br>00: 64 + 32×32<br>01: 64 – 32×32<br>10: 32×32 – 64<br>11: Reserved |        |

Note 1: <MOPST> is write-only and it is read as "0".

Note 2: Writing "1xx" to <MSTTG2:0> and writing "1" to <MOPST> can be executed in the same write cycle.

Note 3: <MOVF> is fixed two system clocks ( $f_{SYS}$ ) after calculation is started.

## 3.24.1.2 Data Registers

The data registers are arranged as shown below.

|                       | Data Registers |             |             |                |             |             |            |                |
|-----------------------|----------------|-------------|-------------|----------------|-------------|-------------|------------|----------------|
|                       | Bits<63:56>    | Bits<55:48> | Bits<47:40> | Bits<39:32>    | Bits<31:24> | Bits<23:16> | Bits<15:8> | Bits<7:0>      |
| Multiplier A Register |                |             |             |                | (1BE3H)     | (1BE2H)     | (1BE1H)    | MACMA (1BE0H)  |
| Multiplier B Register |                |             |             |                | (1BE7H)     | (1BE6H)     | (1BE5H)    | MACMB (1BE4H)  |
| MAC Register          | (1BEFH)        | (1BEEH)     | (1BEDH)     | MACORH (1BECH) | (1BEBH)     | (1BEAH)     | (1BE9H)    | MACORL (1BE8H) |

Note 1: After reset, all the registers are cleared to "0".

Note 2: Read-modify-write instructions can be used on all the registers.

Note 3: All the registers can be accessed in long word, word, or byte units. (In case of using "sign mode", it can be accessed in long word only)

Note 4: When MACCR<MSTTG2:0> is set to "0", "001", "010" or "011" and the registers are written in word or byte units, the <7:0> bits of each register must be written last.

Note 5: The MACORL register is fixed one system clock ( $f_{SYS}$ ) after calculation is started, and the MACORH register is fixed two system clocks ( $f_{SYS}$ ) after calculation is started. Therefore, to read the MACOR register immediately after calculation, be sure to read the MACORL register first.

Note 6: In case of using "sign mode", MACCR<MSGMD> = "1", it must need to write to MACMA and MACMB register with longword (32bit).

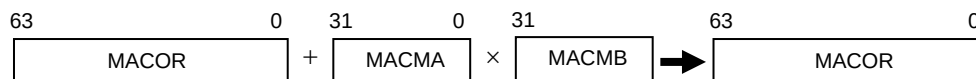
## 3.24.2 Description of Operation

## (1) Calculation mode

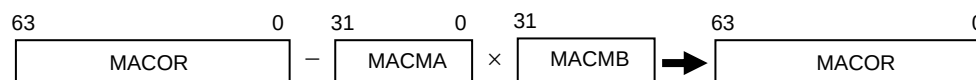
The MAC has the following three types of calculation mode. The calculation mode to be used is specified in MACCR<MOPMD1:0>. MACCR<MSGMD> is used to select unsigned or signed mode. The operation of each calculation mode is explained below.

(a)  $64 + 32 \times 32$  mode

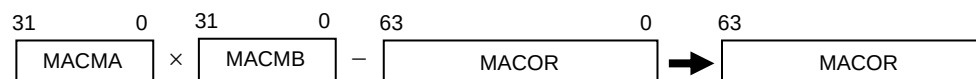
In this mode, the contents of the MACMA register and the MACMB register are multiplied and the result is added to the contents of the MACOR register. Then, the result is stored back in the MACOR register.

(b)  $64 - 32 \times 32$  mode

In this mode, the contents of the MACMA register and the MACMB register are multiplied and the result is subtracted from the contents of the MACOR register. Then, the result is stored back in the MACOR register.

(c)  $32 \times 32 - 64$  mode

In this mode, the contents of the MACMA register and the MACMB register are multiplied and the contents of the MACOR register are subtracted from the result. Then, the result is stored back in the MACOR register.





## (d) Sign mode

Both multiply-accumulate and multiply-subtract operations can be executed in unsigned or signed mode.

In signed mode, the MACMA, MACMB, and MACOR registers become signed registers, and the most significant bit is treated as the sign bit and the data set in each register is treated as a two's complement value. Table 3.24.1 shows the range of values that can be represented in each sign mode.

Table 3.24.1 Data Range in Unsigned/Signed Mode

|          | MACMA, MACMB Registers   | MACOR Register           |
|----------|--------------------------|--------------------------|
| Unsigned | $0 \sim 2^{32}-1$        | $0 \sim 2^{64}-1$        |
| Signed   | $-2^{31} \sim +2^{31}-1$ | $-2^{63} \sim +2^{63}-1$ |

Use signed mode when the values to be set in the MACMA and MACMB registers are signed (two's complement) data. Even in unsigned mode it is possible to set signed (two's complement) data in the MACOR register to perform additions and subtractions in signed mode.

**In case of using "sign mode", MACCR<MSGMD> = "1", it must need to write to MACMA and MACMB register with longword (32bit).**

## (2) Calculation start trigger

As a trigger to start calculation, writing to the MACMA, MACMB or MACOR register or soft start (MACCR<MOPST>= "1") can be selected in MACCR<MSTTG2:0>.

## (3) Overflow flag

When an overflow occurs in the calculation result (see Table 3.24.2), MACCR<MOVF> is set to "1". Once an overflow occurs, MACCR<MOVF> is held at "1" regardless of subsequent calculation results. Since the overflow flag is not automatically cleared by a read operation, it is necessary to write "0" to clear this flag.

Table 3.24.2 Overflow Definitions

| Sign Mode | Calculation Result<br>(MACOR register value) | MACCR<MOVF> |
|-----------|----------------------------------------------|-------------|
| Signed    | $MACOR > 2^{64}-1$                           | 1           |
|           | $0 \leq MACOR \leq 2^{64}-1$                 | 0           |
|           | $MACOR < 0$                                  | 1           |
| Unsigned  | $MACOR > 2^{63}-1$                           | 1           |
|           | $-2^{63} \leq MACOR \leq 2^{63}-1$           | 0           |
|           | $MACOR < -2^{63}$                            | 1           |

### 3.24.3 Operation Examples

#### (1) Unsigned multiply-accumulate operation

The following shows a setting example for calculating “33333333 + 11111111 × 22222222”:

|     |                 |                                                    |                     |
|-----|-----------------|----------------------------------------------------|---------------------|
| ld  | (MACCR), 0x08   | ; Unsigned multiply-accumulate mode                |                     |
|     |                 | Start calculation by write to MACMB.               |                     |
| ld  | xde, 0x00000000 |                                                    |                     |
| ld  | xhl, 0x33333333 |                                                    |                     |
| ld  | xix, 0x11111111 |                                                    |                     |
| ld  | xiy, 0x22222222 |                                                    |                     |
| ld  | (MACORL), xhl   | ; Write 33333333 to MACORL.                        |                     |
| ld  | (MACORH), xde   | ; Clear MACORH.                                    |                     |
| ld  | (MACMA), xix    | ; Write 11111111 to MACMA.                         |                     |
| ld  | (MACMB), xiy    | ; Write 22222222 to MACMB.                         | ← Calculation start |
| ld  | xhl, (MACORL)   | ; Read lower result 0x41FDB975.                    |                     |
| bit | 7, (MACCR)      | ; Check over-flow error                            |                     |
| jp  | nz, ERROR       | ; Go to error routine, if there is over-flow error |                     |
| ld  | xde, (MACORH)   | ; Read upper result 0x02468ACF.                    |                     |

#### (2) Signed multiply-subtract operation

The following shows a setting example for calculating “33333333 – 11111111 × –22222222”:

|     |                 |                                                    |                     |
|-----|-----------------|----------------------------------------------------|---------------------|
| ld  | (MACCR), 0x25   | ; Signed multiply-subtract mode                    |                     |
|     |                 | Start calculation by write of “1” to <MOPST>.      |                     |
| ld  | xde, 0x00000000 |                                                    |                     |
| ld  | xhl, 0x33333333 |                                                    |                     |
| ld  | xix, 0x11111111 |                                                    |                     |
| ld  | xiy, 0xDDDDDDDE | ; –22222222                                        |                     |
| ld  | (MACORL), xhl   | ; Write 33333333 to MACORL.                        |                     |
| ld  | (MACORH), xde   | ; Clear MACORH.                                    |                     |
| ld  | (MACMA), xix    | ; Write 11111111 to MACMA.                         |                     |
| ld  | (MACMB), xiy    | ; Write –22222222 to MACMB.                        |                     |
| set | 5, (MACCR)      |                                                    | ← Calculation start |
| ld  | xhl, (MACORL)   | ; Read lower result 0x41FDB975.                    |                     |
| bit | 7, (MACCR)      | ; Check over-flow error                            |                     |
| jp  | nz, ERROR       | ; Go to error routine, if there is over-flow error |                     |
| ld  | xde, (MACORH)   | ; Read upper result 0x02468ACF.                    |                     |

#### (3) Unsigned multiply-accumulate operation (two multiply-accumulate operations)

The following shows a setting example for calculating “(33333333 + 11111111 × 22222222) + (11111111 × 44444444)”:

|     |                 |                                                    |                     |
|-----|-----------------|----------------------------------------------------|---------------------|
| ld  | (MACCR), 0x08   | ; Unsigned multiply-accumulate mode                |                     |
|     |                 | Start calculation by write to MACMB.               |                     |
| ld  | xde, 0x00000000 |                                                    |                     |
| ld  | xhl, 0x33333333 |                                                    |                     |
| ld  | xix, 0x11111111 |                                                    |                     |
| ld  | xiy, 0x22222222 |                                                    |                     |
| ld  | xiz, 0x44444444 |                                                    |                     |
| ld  | (MACORL), xhl   | ; Write 33333333 to MACORL.                        |                     |
| ld  | (MACORH), xde   | ; Clear MACORH.                                    |                     |
| ld  | (MACMA), xix    | ; Write 11111111 to MACMA.                         |                     |
| ld  | (MACMB), xiy    | ; Write 22222222 to MACMB.                         | ← Calculation start |
| ld  | (MACMB), xiz    | ; Write 44444444 to MACMB.                         | ← Calculation start |
| ld  | xhl, (MACORL)   | ; Read lower result 0x5F92C5F9.                    |                     |
| bit | 7, (MACCR)      | ; Check over-flow error                            |                     |
| jp  | nz, ERROR       | ; Go to error routine, if there is over-flow error |                     |
| ld  | xde, (MACORH)   | ; Read upper result 0x06D3A06D.                    |                     |

## 4. Electrical Characteristics

### 4.1 Absolute Maximum Ratings

| Symbol              | Contents                      | Rating                                                  | Unit |
|---------------------|-------------------------------|---------------------------------------------------------|------|
| DVCC3A              | Power Supply Voltage          | -0.3 to 3.9                                             | V    |
| DVCC1A              |                               | -0.3 to 3.0                                             |      |
| DVCC1B              |                               |                                                         |      |
| DVCC1C              |                               |                                                         |      |
| AVCC                |                               | -0.3 to 3.9                                             |      |
| V <sub>IN</sub>     | Input Voltage                 | -0.3 to DVCC3A+0.3 (Note1)<br>-0.3 to AVCC+0.3 (Note 2) | V    |
| I <sub>OL</sub>     | Output Current (1pin)         | 15                                                      | mA   |
| I <sub>OH</sub>     | Output Current (1pin)         | -15                                                     | mA   |
| Σ I <sub>OL</sub>   | Output Current (total)        | 80                                                      | mA   |
| Σ I <sub>OH</sub>   | Output Current (total)        | -50                                                     | mA   |
| P <sub>D</sub>      | Power Dissipation (Ta = 85°C) | 600                                                     | mW   |
| T <sub>SOLDER</sub> | Soldering Temperature (10s)   | 260                                                     | °C   |
| T <sub>STG</sub>    | Storage Temperature           | -65 to 150                                              | °C   |
| T <sub>OPR</sub>    | Operation Temperature         | -0 to 70                                                | °C   |

Note1: If setting it, don't exceed the Maximum Ratings of DVCC3A.

Note2: In PG0 to PG5, P96,P97,VREFH,VREFL maximum ratings for AVCC is applied.

Note3: The absolute maximum ratings are rated values that must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products that include this device, ensure that no absolute maximum rating value will ever be exceeded.

#### Solderability

| Test parameter | Test condition                                                                                                                                                  | Note                                                  |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------|
| Solderability  | Use of Sn-37Pb solder Bath<br>Solder bath temperature = 230 $^\circ\text{C}$ , Dipping time = 5 seconds<br>The number of times = one, Use of R-type flux        | Pass:<br>solderability rate until forming $\geq 95\%$ |
|                | Use of Sn-3.0Ag-0.5Cu solder bath<br>Solder bath temperature = 245 $^\circ\text{C}$ , Dipping time = 5 seconds<br>The number of times = one, Use of R-type flux |                                                       |

## 4.2 DC Electrical Characteristics

| Symbol    | Parameter                                                                                                                                                                                    | Min  | Typ. | Max                  | Unit | Condition                           |                 |
|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|----------------------|------|-------------------------------------|-----------------|
| DVCC3A    | General I/O<br>Power Supply Voltage<br>(DVCC=AVCC)<br>(DVSSCOM=AVSS=0V)                                                                                                                      | 3.0  | 3.3  | 3.6                  | V    | X1=6 to 10MHz<br>CPU CLK<br>(80MHz) | XT1=30 to 34kHz |
| DVCC1A    | Internal Power A                                                                                                                                                                             | 1.4  | 1.5  | 1.6                  | V    |                                     |                 |
| DVCC1B    | Internal Power B                                                                                                                                                                             |      |      |                      |      |                                     |                 |
| DVCC1C    | High CLK oscillator and PLL Power                                                                                                                                                            |      |      |                      |      |                                     |                 |
| $V_{IL0}$ | Input Low Voltage for<br>D0 to D7<br>P10 to P17 (D8 to 15), P60 to P67<br>P71 to P76, P90<br>PC4 to PC7, PF0 to PF5<br>PG0 to PG5, PJ5 to PJ6<br>PN0 to PN7, PR0 to PR3,<br>PT0 to PT7, PX5, | -0.3 | —    | $0.3 \times DVCC3A$  | V    | $3.0 \leq DVCC3A \leq 3.6$          |                 |
| $V_{IL1}$ | Input Low Voltage for<br>PV6 to PV7                                                                                                                                                          |      | —    | $0.3 \times DVCC3A$  |      | $3.0 \leq DVCC3A \leq 3.6$          |                 |
| $V_{IL2}$ | Input Low Voltage for<br>P91 to P92, P96 to P97, PA0 to<br>PA7<br>PC0 to PC3, PP3 to PP5, $\overline{RESET}$                                                                                 |      | —    | $0.25 \times DVCC3A$ |      | $3.0 \leq DVCC3A \leq 3.6$          |                 |
| $V_{IL3}$ | Input Low Voltage for<br>AM0 to AM1                                                                                                                                                          |      | —    | $0.1 \times DVCC3A$  |      | $3.0 \leq DVCC3A \leq 3.6$          |                 |
| $V_{IL4}$ | Input Low Voltage for X1                                                                                                                                                                     |      | —    | $0.1 \times DVCC1C$  |      | $1.4 \leq DVCC1C \leq 1.6$          |                 |
| $V_{IL5}$ | Input Low Voltage for XT1                                                                                                                                                                    |      | —    | $0.15 \times DVCC3A$ |      | $3.0 \leq DVCC3A \leq 3.6$          |                 |

Note: Above power supply range is premised that all power supply of same system is equal.

(DVCC1A = DVCC1B = DVCC1C or DVCC3A = AVCC)

| Symbol    | Parameter                                                                                                                                                                                                 | Min                  | Typ. | Max            | Unit | Condition                  |
|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------|----------------|------|----------------------------|
| $V_{IH0}$ | Input High Voltage for<br>D0 to D7<br>P10 to P17 (D8 to 15), P60 to P67<br>P71 to P76, P90<br>PC4 to PC7, PF0 to PF5<br>PG0 to PG5, PJ5 to PJ6<br>PN0 to PN7, PP1 to PP2<br>PR0 to PR3, PT0 to PT7<br>PX5 | $0.7 \times DVCC3A$  | –    | $DVCC3A + 0.3$ | V    | $3.0 \leq DVCC3A \leq 3.6$ |
| $V_{IH1}$ | Input High Voltage for<br>PV6 to PV7                                                                                                                                                                      | $0.7 \times DVCC3A$  | –    | $DVCC3A + 0.3$ |      | $3.0 \leq DVCC3A \leq 3.6$ |
| $V_{IH2}$ | Input High Voltage for<br>P91 to P92, P96 to P97,<br>PA0 to PA7, PC0 to PC3,<br>PP3 to PP5, $\overline{RESET}$                                                                                            | $0.75 \times DVCC3A$ | –    | $DVCC3A + 0.3$ |      | $3.0 \leq DVCC3A \leq 3.6$ |
| $V_{IH3}$ | Input High Voltage for AM0 to AM1                                                                                                                                                                         | $0.9 \times DVCC3A$  | –    | $DVCC3A + 0.3$ |      | $3.0 \leq DVCC3A \leq 3.6$ |
| $V_{IH4}$ | Input High Voltage for X1                                                                                                                                                                                 | $0.9 \times DVCC1C$  | –    | $DVCC1C + 0.3$ |      | $1.4 \leq DVCC1C \leq 1.6$ |
| $V_{IH5}$ | Input High Voltage for XT1                                                                                                                                                                                | $0.85 \times DVCC3A$ | –    | $DVCC3A + 0.3$ |      | $3.0 \leq DVCC3A \leq 3.6$ |

| Symbol           | Parameter                                                                                                                                        | Min | Typ. | Max | Unit | Condition                                |                                |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----|------|------------------------------------------|--------------------------------|
| V <sub>OL1</sub> | Output Low Voltage1<br>P90 to P92,<br>PC0 to PC3, PC7<br>PF0 to PF5, PK1 to PK7<br>PM1 to PM2, PM7<br>PN0 to PN7, PP3 to PP6<br>PV6 to PV7, PX5  | –   | –    | 0.4 | V    | I <sub>OL</sub> = 0.5mA, 3.0 ≤ DVCC3A    |                                |
| V <sub>OL2</sub> | Output Low Voltage2<br>Except VOL1 output pin                                                                                                    |     |      |     |      | I <sub>OL</sub> = 2mA, 3.0 ≤ DVCC3A      |                                |
| V <sub>OH1</sub> | Output High Voltage1<br>P90 to P92,<br>PC0 to PC3, PC7<br>PF0 to PF7, PK1 to PK7<br>PM1 to PM2, PM7<br>PN0 to PN7, PP3 to PP6<br>PV6 to PV7, PX5 | 2.4 | –    | –   |      | I <sub>OH</sub> = -0.5mA, 3.0 ≤ DVCC3A   |                                |
| V <sub>OH2</sub> | Output High Voltage2<br>Except VOL1 output pin                                                                                                   |     |      |     |      | I <sub>OH</sub> = -2mA, 3.0 ≤ DVCC3A     |                                |
| I <sub>Mon</sub> | Internal resistor (ON)<br>MX, MY pins                                                                                                            | –   | –    | 30  | Ω    | V <sub>OL</sub> = 0.2V                   | V <sub>CC</sub> = 3.0 to 3.6 V |
| I <sub>Mon</sub> | Internal resistor (ON)<br>PX, PY pins                                                                                                            | –   | –    | 30  |      | V <sub>OH</sub> = V <sub>CC</sub> – 0.2V |                                |
| I <sub>LI</sub>  | Input Leakage Current                                                                                                                            | –   | 0.02 | ±5  | μA   | 0.0 ≤ Vin ≤ DVCC3A                       |                                |
| I <sub>LO</sub>  | Output Leakage Current                                                                                                                           | –   | 0.05 | ±10 | μA   | 0.2 ≤ Vin ≤ DVCC3A-0.2V                  |                                |
| R <sub>RST</sub> | Pull Up/Down Resistor for<br>RESET , PA0 to PA7, P96                                                                                             | 30  | 50   | 70  | kΩ   |                                          |                                |
| C <sub>IO</sub>  | Pin Capacitance                                                                                                                                  | –   | –    | 10  | pF   | fc=1MHz                                  |                                |
| V <sub>TH</sub>  | Schmitt Width for<br>P91 to P92, P96 to P97,<br>PA0 to PA7, PC0 to PC3,<br>PP3 to PP5, RESET                                                     | 0.6 | 0.8  | 1.0 | V    | 3.0 ≤ DVCC3A ≤ 3.6                       |                                |

Note: Typical values are value that when  $T_a = 25^\circ\text{C}$  and  $V_{CC} = 3.3 \text{ V}$  unless otherwise noted.

| Symbol          | Parameter      | Min | Typ. | Max  | Unit | Condition                          |                     |
|-----------------|----------------|-----|------|------|------|------------------------------------|---------------------|
| I <sub>CC</sub> | NORMAL (note2) | —   | 15   | 30   | mA   | PLL_ON<br>f <sub>SYS</sub> =80MHZ  | DVCC3A= 3.6V        |
|                 |                |     | 37   | 52   |      |                                    | DVCC1A,1B,1C = 1.6V |
|                 | IDLE2          | —   | 0.5  | 1    |      |                                    | DVCC3A = 3.6V       |
|                 |                |     | 20   | 35   |      |                                    | DVCC1A,1B,1C = 1.6V |
|                 | NORMAL (note2) | —   | 12   | 23   |      | PLL_ON<br>f <sub>SYS</sub> =60MHZ  | DVCC3A = 3.6V       |
|                 |                |     | 28   | 39   |      |                                    | DVCC1A,1B,1C = 1.6V |
|                 | IDLE2          | —   | 0.4  | 0.8  |      |                                    | DVCC3A = 3.6V       |
|                 |                |     | 15   | 26   |      |                                    | DVCC1A,1B,1C = 1.6V |
|                 | IDLE1          | —   | 12   | 45   | μA   | PLL_OFF<br>f <sub>SYS</sub> =10MHZ | DVCC3A = 3.6V       |
|                 |                |     | 200  | 3200 |      |                                    | DVCC1A,1B,1C = 1.6V |
|                 | STOP           | —   | 6    | 35   |      | Ta ≤ 70°C                          | DVCC3A = 3.6V       |
|                 |                |     |      | 30   |      | AVCC = 3.6V                        |                     |
|                 |                |     | 200  | 800  |      | Ta ≤ 70°C                          | DVCC1A =1.6V        |
|                 |                |     |      | 600  |      | Ta ≤ 50°C                          | DVCC1B =1.6V        |
|                 |                |     |      |      |      |                                    | DVCC1C =1.6V        |
|                 |                |     |      |      |      |                                    | XT = OFF<br>X = OFF |

Note1: Typical values are value that when Ta = 25°C and V<sub>CC</sub> = 3.3 V, DVCC1A,1B,1C = 1.5V unless otherwise noted.

Note2: I<sub>CC</sub> measurement conditions (NORMAL, SLOW):

All functions are operational; output pins except bus pin are open, and input pins are fixed. Bus pin C<sub>L</sub> = 50pF  
(Access to external memory at 8-wait setting )

Note3: Above I<sub>CC</sub> measurement value is a data when 16 bit external bus starting.

### 4.3 AC Characteristics

The Following all AC regulation is the measurement result in following condition, if unless otherwise noted.

#### AC measuring condition

- Clock of top column in above table shows system clock frequency, and “T” shows system clock period [ns].
- Output level: High =  $0.7 \times DVCC3A$ , Low =  $0.3 \times DVCC3A$
- Input level: High =  $0.9 \times DVCC3A$ , Low =  $0.1 \times DVCC3A$

Note: In table, “Variable” shows the regulation at  $DVCC3A=3.0V$  to  $3.6V$ ,  $DVCC1A=DVCC1B=DVCC1C=1.4$  to  $1.6V$ .

#### 4.3.1 Basic Bus Cycle

##### Read cycle

| No.  | Parameter                                                       | Symbol     | Variable    |               | 80 MHz | 60 MHz | Unit |
|------|-----------------------------------------------------------------|------------|-------------|---------------|--------|--------|------|
|      |                                                                 |            | Min         | Max           |        |        |      |
| 1    | OSC period (X1/X2)                                              | $t_{OSC}$  | 100         | 166.6         | –      | –      | ns   |
| 2    | System clock period (= T)                                       | $t_{CYC}$  | 12.5        | 2666          | 12.5   | 16.6   |      |
| 3    | SDCLK low width                                                 | $t_{CL}$   | $0.5T - 3$  |               | 3.25   | 5.3    |      |
| 4    | SDCLK high width                                                | $t_{CH}$   | $0.5T - 3$  |               | 3.25   | 5.3    |      |
| 5-1  | A0 to A23 valid<br>→ D0 to D31 input at 0 waits                 | $t_{AD}$   |             | $2.0T - 18.0$ | 7      | 15.3   |      |
| 5-2  | A0 to A23 valid<br>→ D0 to D31 input at 4 waits/6 waits         | $t_{AD4}$  |             | $6.0T - 18.0$ | 57     | 82     |      |
|      |                                                                 | $t_{AD6}$  |             | $8.0T - 18.0$ | 82     | 115    |      |
| 6-1  | $\overline{RD}$ falling → D0 to D31 input at 0 waits            | $t_{RD}$   |             | $1.5T - 18.0$ | 0.75   | 7      |      |
| 6-2  | $\overline{RD}$ falling<br>→ D0 to D31 input at 4 waits/6 waits | $t_{RD4}$  |             | $5.5T - 18.0$ | 50.75  | 73.6   |      |
|      |                                                                 | $t_{RD6}$  |             | $7.5T - 18.0$ | 75.75  | 106.5  |      |
| 7-1  | $\overline{RD}$ low width at 0 waits                            | $t_{RR}$   | $1.5T - 10$ |               | 8.75   | 14.9   |      |
| 7-2  | $\overline{RD}$ low width at 4 waits/6 waits                    | $t_{RR4}$  | $5.5T - 10$ |               | 58.75  | 81.3   |      |
|      |                                                                 | $t_{RR6}$  | $7.5T - 10$ |               | 83.75  | 114.5  |      |
| 8    | A0 to A23 valid → $\overline{RD}$ falling                       | $t_{AR}$   | $0.5T - 5$  |               | 1.25   | 3.3    |      |
| 9    | $\overline{RD}$ falling → SDCLK rising                          | $t_{RK}$   | $0.5T - 5$  |               | 1.25   | 3.3    |      |
| 10   | A0 to A23 valid → D0 to D31 hold                                | $t_{HA}$   | 0           |               | 0      | 0      |      |
| 11   | $\overline{RD}$ rising → D0 to D31 hold                         | $t_{HR}$   | 0           |               | 0      | 0      |      |
| 12   | $\overline{WAIT}$ setup time                                    | $t_{TK}$   | 20          |               | 20     | 20     |      |
| 13   | $\overline{WAIT}$ hold time                                     | $t_{KT}$   | 2           |               | 2      | 2      |      |
| 14-1 | Data byte control access time for SRAM<br>at 0 waits            | $t_{SBA}$  |             | $1.5T - 18.0$ | 0.75   | 7      |      |
| 14-2 | Data byte control access time for SRAM<br>at 4 waits/6waits     | $t_{SBA4}$ |             | $5.5T - 18.0$ | 50.75  | 73.6   |      |
|      |                                                                 | $t_{SBA6}$ |             | $7.5T - 18.0$ | 75.75  | 107.0  |      |
| 15   | $\overline{RD}$ high width                                      | $t_{RRH}$  | $0.5T - 5$  |               | 1.25   | 3.3    |      |

#### AC measuring condition

- Data\_bus, Address\_bus, various function control signal capacitance  $C_L = 50$  pF



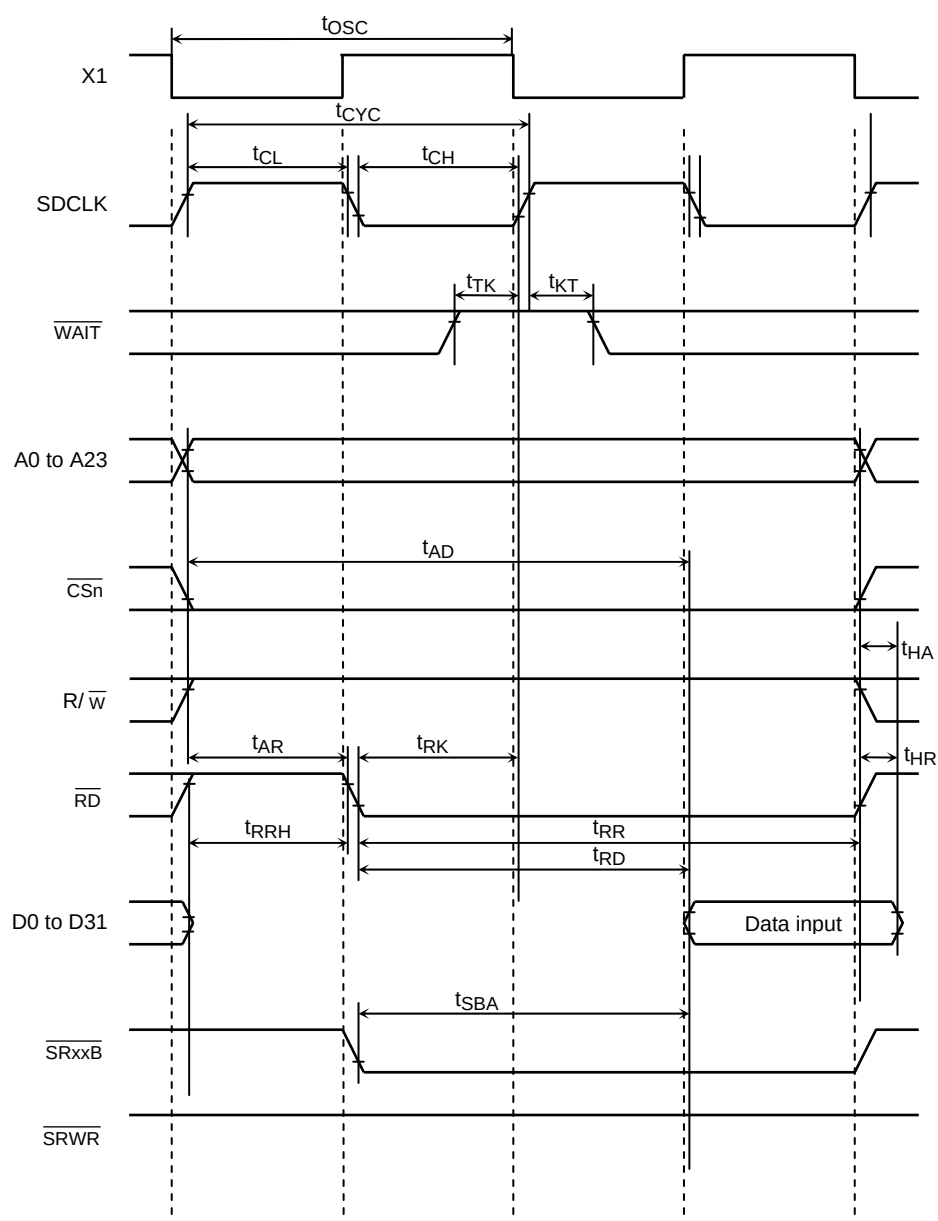
## Write cycle

| No.  | Parameter                                                         | Symbol     | Variable   |     | 80MHz | 60MHz | Unit |
|------|-------------------------------------------------------------------|------------|------------|-----|-------|-------|------|
|      |                                                                   |            | Min        | Max |       |       |      |
| 16-1 | D0 to D31 valid<br>→ $\overline{WR}$ xx rising at 0 waits         | $t_{DW}$   | 1.0T – 6.0 |     | 6.5   | 10.6  | ns   |
| 16-2 | D0 to D31 valid<br>→ $\overline{WR}$ xx rising at 2 waits/4 waits | $t_{DW2}$  | 3.0T – 6.0 |     | 31.5  | 43.8  |      |
|      |                                                                   | $t_{DW4}$  | 5.0T – 6.0 |     | 56.5  | 77.0  |      |
| 17-1 | $\overline{WR}$ xx low width at 0 waits                           | $t_{WW}$   | 1.0T – 4.0 |     | 8.5   | 12.6  |      |
| 17-2 | $\overline{WR}$ xx low width at 2 waits/4 waits                   | $t_{WW2}$  | 3.0T – 4.0 |     | 33.5  | 45.8  |      |
|      |                                                                   | $t_{WW4}$  | 5.0T – 4.0 |     | 58.5  | 79.0  |      |
| 18   | A0 to A23 valid → $\overline{WR}$ falling                         | $t_{AW}$   | 0.5T – 5.0 |     | 1.25  | 3.3   |      |
| 19   | $\overline{WR}$ xx falling → SDCLK rising                         | $t_{WK}$   | 0.5T – 5.0 |     | 1.25  | 3.3   |      |
| 20   | $\overline{WR}$ xx rising → A0 to A23 hold                        | $t_{WA}$   | 0.5T – 5.0 |     | 1.25  | 3.3   |      |
| 21   | $\overline{WR}$ xx rising → D0 to D31 hold                        | $t_{WD}$   | 0.5T – 5.0 |     | 1.25  | 3.3   |      |
| 22   | $\overline{RD}$ rising → D0 to D31 output                         | $t_{RDO}$  | 0.5T – 1.0 |     | 5.25  | 7.3   |      |
| 23-1 | Write width for SRAM at 0 waits                                   | $t_{SWP}$  | 1.0T – 4.0 |     | 8.5   | 12.6  |      |
| 23-2 | Write width for SRAM at 2 waits/4 waits                           | $t_{SWP2}$ | 3.0T – 4.0 |     | 33.5  | 45.8  |      |
|      |                                                                   | $t_{SWP4}$ | 5.0T – 4.0 |     | 58.5  | 79.0  |      |
| 24-1 | Data byte control ~ end of write<br>for SRAM at 0 waits           | $t_{SBW}$  | 1.0T – 4.0 |     | 8.5   | 12.6  |      |
| 24-2 | Data byte control ~ end of write<br>for SRAM at 2 waits/4 waits   | $t_{SBW2}$ | 3.0T – 4.0 |     | 33.5  | 45.8  |      |
|      |                                                                   | $t_{SBW4}$ | 5.0T – 4.0 |     | 58.5  | 79.0  |      |
| 25   | Address setup time for SRAM                                       | $t_{SAS}$  | 0.5T – 5.0 |     | 1.25  | 3.3   |      |
| 26   | Write recovery time for SRAM                                      | $t_{SWR}$  | 0.5T – 5.0 |     | 1.25  | 3.3   |      |
| 27-1 | Data setup time for SRAM at 0 waits                               | $t_{SDS}$  | 1.0T – 6.0 |     | 6.5   | 10.6  |      |
| 27-2 | Data setup time for SRAM<br>at 2 waits/4 waits                    | $t_{SDS2}$ | 3.0T – 6.0 |     | 31.5  | 43.8  |      |
|      |                                                                   | $t_{SDS4}$ | 5.0T – 6.0 |     | 56.5  | 77.0  |      |
| 28   | Data hold time for SRAM                                           | $t_{SDH}$  | 0.5T – 5.0 |     | 1.25  | 3.3   |      |

AC measuring condition

- Data\_bus, Address\_bus, various function control signal capacitance  $C_L = 50 \text{ pF}$

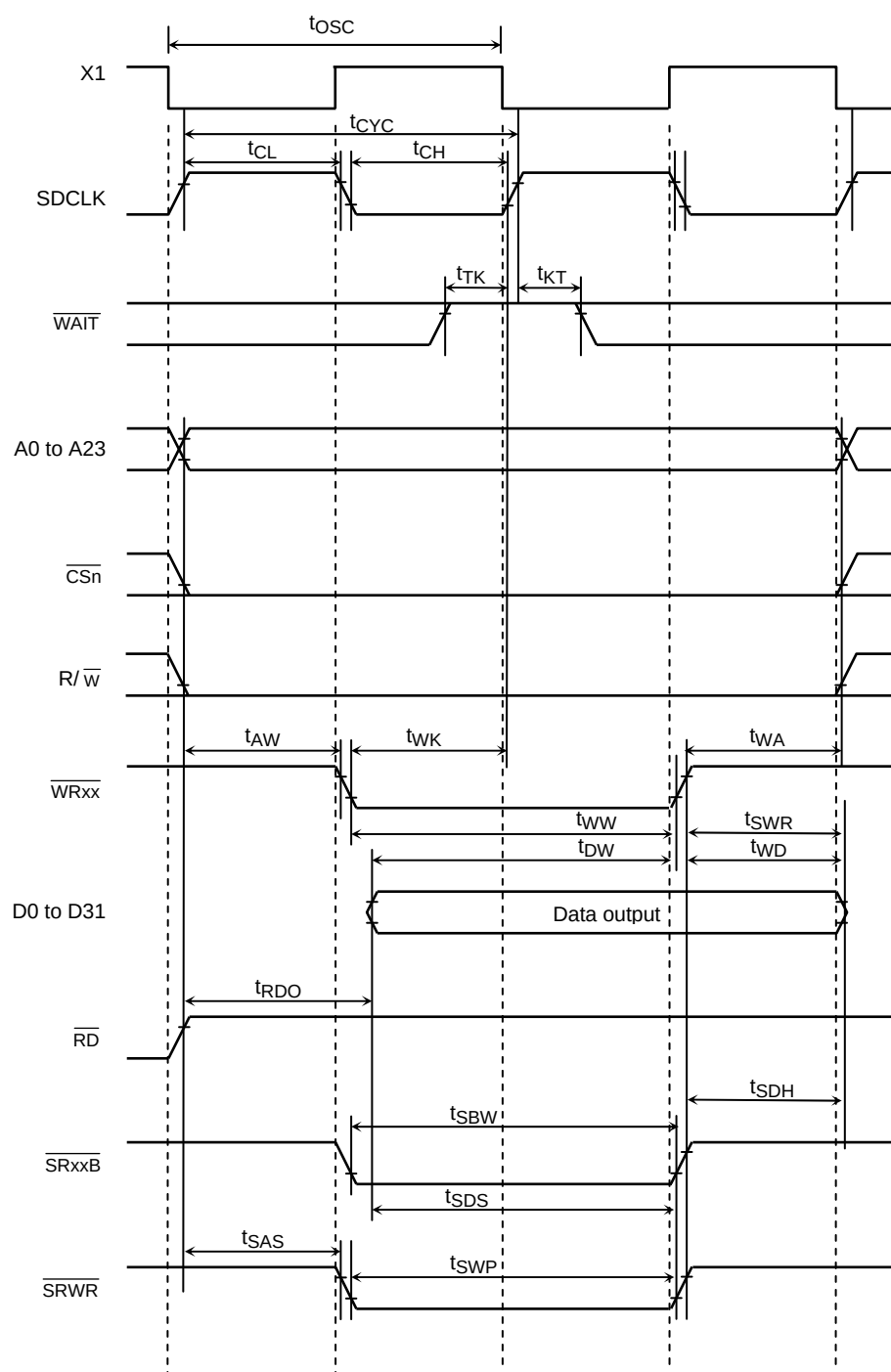
## (1) Read cycle (0 waits)



Note1: The phase relation between X1 input signal and the other signals is undefined.

Note2: The above timing chart show an example of basic bus timing. The  $\overline{CSn}$ ,  $R/\overline{W}$ ,  $\overline{RD}$ ,  $\overline{WRxx}$ ,  $\overline{SRxxB}$ ,  $\overline{SRWR}$  pins timing can be adjusted by memory controller timing adjust function.

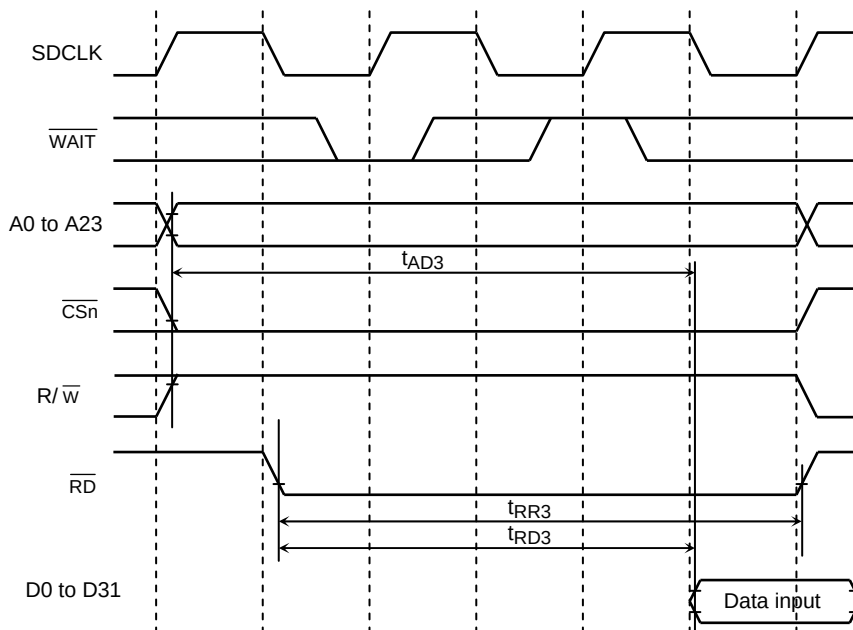
## (2) Write cycle (0 waits)



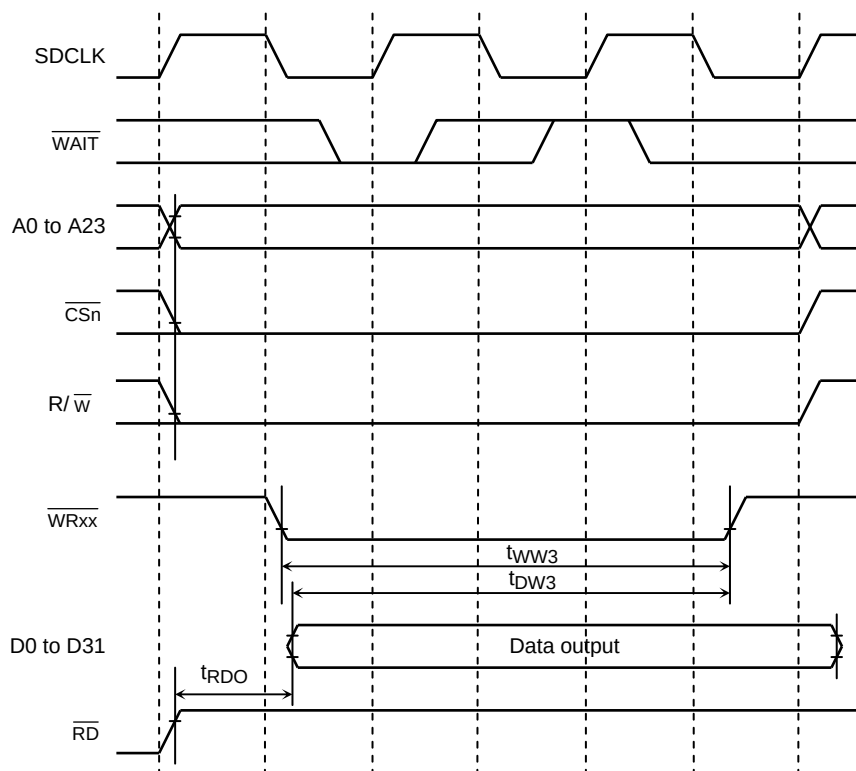
Note1: The phase relation between X1 input signal and the other signals is undefined.

Note2: The above timing chart show an example of basic bus timing. The  $\overline{CSn}$ ,  $\overline{R/\overline{W}}$ ,  $\overline{RD}$ ,  $\overline{WRxx}$ ,  $\overline{SRxxB}$ ,  $\overline{SRWR}$  pins timing can be adjusted by memory controller timing adjust function.

## (3) Read cycle (1 wait)



## (4) Write cycle (1 wait)



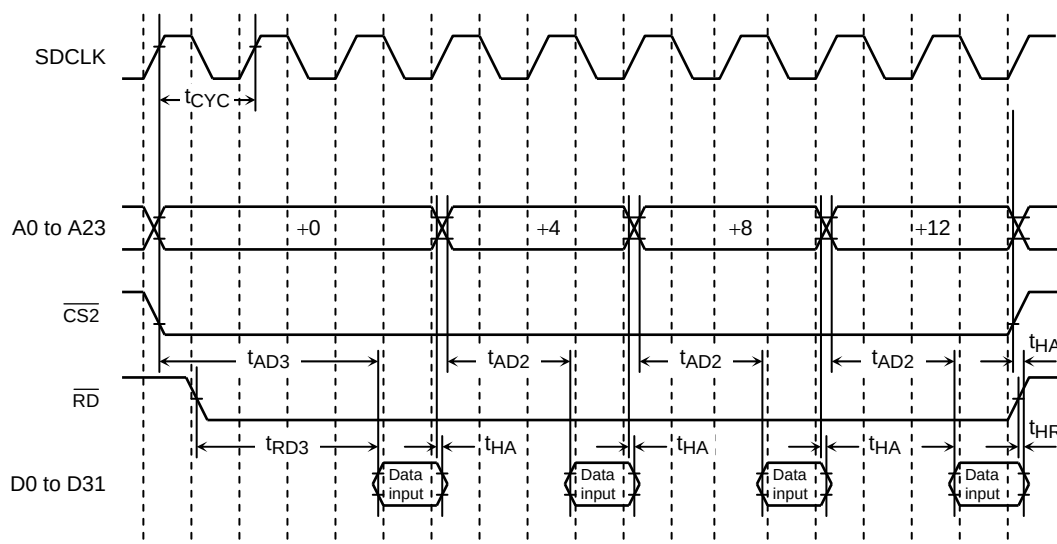
## 4.3.2 Page ROM Read Cycle

## (1) 3-2-2-2 mode

| No. | Parameter                                 | Symbol    | Variable |             | 80 MHz | 60 MHz | Unit |
|-----|-------------------------------------------|-----------|----------|-------------|--------|--------|------|
|     |                                           |           | Min      | Max         |        |        |      |
| 1   | System clock period (= T)                 | $t_{CYC}$ | 12.5     | 2666        | 12.5   | 16.6   | ns   |
| 2   | A0, A1 → D0 to D31 input                  | $t_{AD2}$ |          | $2.0T - 18$ | 7      | 15.2   |      |
| 3   | A2 to A23 → D0 to D31 input               | $t_{AD3}$ |          | $3.0T - 18$ | 19.5   | 31.8   |      |
| 4   | $\overline{RD}$ falling → D0 to D31 input | $t_{RD3}$ |          | $2.5T - 18$ | 13     | 24     |      |
| 5   | A0 to A23 Invalid → D0 to D31 hold        | $t_{HA}$  | 0        |             | 0      | 0      |      |
| 6   | $\overline{RD}$ rising → D0 to D31 hold   | $t_{HR}$  | 0        |             | 0      | 0      |      |

AC measuring condition

Note: The (a), (b) and (c) of "Symbol" in above table depend on the falling timing of  $\overline{RD}$  pin. The falling timing of  $\overline{RD}$  pin is set by MEMCR0<RDTMG1:0> in memory controller. If MEMCR0<RDTMG1:0> is set to "00", it correspond with (a) in above table, and "01" is (b), "10" is (c).



Page Mode Access Timing (when using a 16-byte page size example)

## 4.3.3 SDRAM controller AC Characteristics

| No.  | Parameter                                                        |                    | Symbol    | Variable   |         | 80 MHz | 60 MHz | Unit |
|------|------------------------------------------------------------------|--------------------|-----------|------------|---------|--------|--------|------|
|      |                                                                  |                    |           | Min        | Max     |        |        |      |
| 1    | Ref/Active to ref/active command period                          | <STRC[2:0]>= "000" | $t_{RC}$  | T          |         | 12.5   | 16.6   | ns   |
|      |                                                                  | <STRC[2:0]>= "110" |           | 7T         |         | 87.5   | 116.2  |      |
| 2    | Active to precharge command period                               | <STRC[2:0]>= "000" | $t_{RAS}$ | 2T (Note1) |         | 25.0   | 33.2   |      |
|      |                                                                  | <STRC[2:0]>= "110" |           | 7T         |         | 87.5   | 116.2  |      |
| 3    | Active to read/write command delay time                          | <STRCD>= "0"       | $t_{RCD}$ | T          |         | 12.5   | 16.6   |      |
|      |                                                                  | <STRCD>= "1"       |           | 2T         |         | 25.0   | 33.2   |      |
| 4    | Precharge to active command period                               | <STRP>= "0"        | $t_{RP}$  | T          |         | 12.5   | 16.6   |      |
|      |                                                                  | <STRP>= "1"        |           | 2T         |         | 25.0   | 33.2   |      |
| 5    | Active to active command period                                  | <STRC[2:0]>= "000" | $t_{RRD}$ | 3T (Note2) |         | 37.5   | 49.8   |      |
|      |                                                                  | <STRC[2:0]>= "110" |           | 7T         |         | 87.5   | 116.2  |      |
| 6    | Write recovery time                                              | <STWR>= "0"        | $t_{WR}$  | T          |         | 12.5   | 16.6   |      |
|      |                                                                  | <STWR>= "1"        |           | 2T         |         | 25.0   | 33.2   |      |
| 7    | CLK cycle time                                                   |                    | $t_{CK}$  | T          |         | 12.5   | 16.6   |      |
| 8    | CLK high level width                                             |                    | $t_{CH}$  | 0.5T – 3   |         | 3.25   | 5.3    |      |
| 9    | CLK low level width                                              |                    | $t_{CL}$  | 0.5T – 3   |         | 3.25   | 5.3    |      |
| 10-1 | Access time from CLK(CL* =2)<br><SRDS>= "0"(Read data shift OFF) |                    | $t_{AC}$  |            | T – 16  | - 3.5  | 0.6    |      |
| 10-2 | Access time from CLK(CL* =2)<br><SRDS>= "1"(Read data shift ON)  |                    | $t_{AC}$  |            | T – 6.5 | 6      | 10.1   |      |
| 11   | Data hold time from internal read                                |                    | $t_{HR}$  | 0          |         | 0      | 0      |      |
| 12   | Data set-up time                                                 | 1Word/Single       | $t_{DS}$  | 0.5T – 4   |         | 2.25   | 4.3    |      |
|      |                                                                  | Burst              | $t_{DS}$  | 0.5T – 4   |         | 2.25   | 4.3    |      |
| 13   | Data hold time                                                   | 1Word/Single       | $t_{DH}$  | T – 10     |         | 2.5    | 6.6    |      |
|      |                                                                  | Burst              | $t_{DH}$  | 0.5T – 4   |         | 2.25   | 4.3    |      |
| 14   | Address set-up time                                              |                    | $t_{AS}$  | 0.5T – 4   |         | 2.25   | 4.3    |      |
| 15   | Address hold time                                                |                    | $t_{AH}$  | 0.5T – 4   |         | 2.25   | 4.3    |      |
| 16   | CKE set-up time                                                  |                    | $t_{CKS}$ | 0.5T – 3   |         | 3.25   | 5.3    |      |
| 17   | Command set-up time                                              |                    | $t_{CMS}$ | 0.5T – 3   |         | 3.25   | 5.3    |      |
| 18   | Command hold time                                                |                    | $t_{CMH}$ | 0.5T – 4   |         | 2.25   | 4.3    |      |
| 19   | Mode register set cycle time                                     |                    | $t_{RSC}$ | T          |         | 12.5   | 16.6   |      |

\*CL: CAS latency

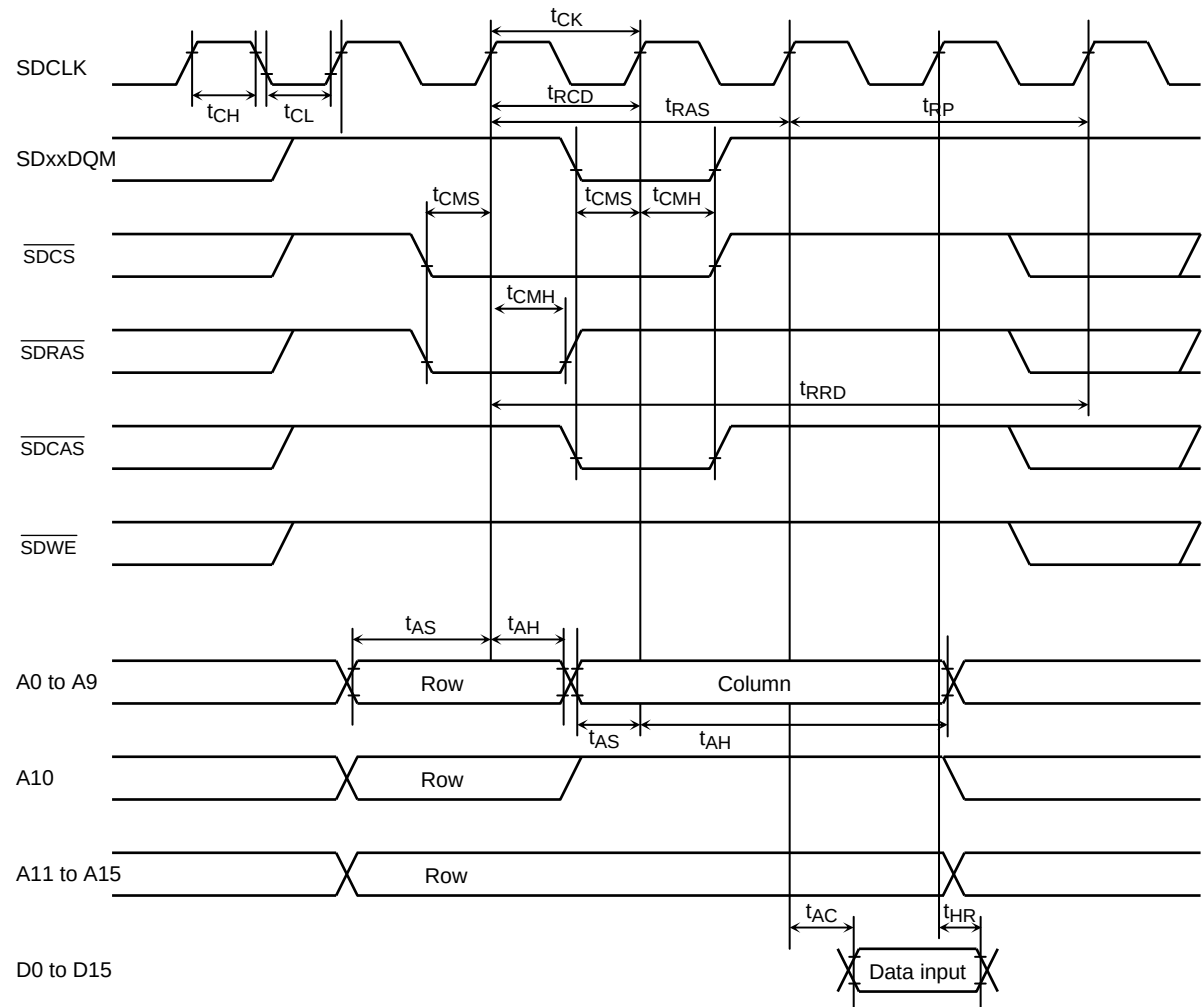
AC measuring condition

- SDCLK pin  $C_L = 30$  pF, Other pins  $C_L = 50$  pF

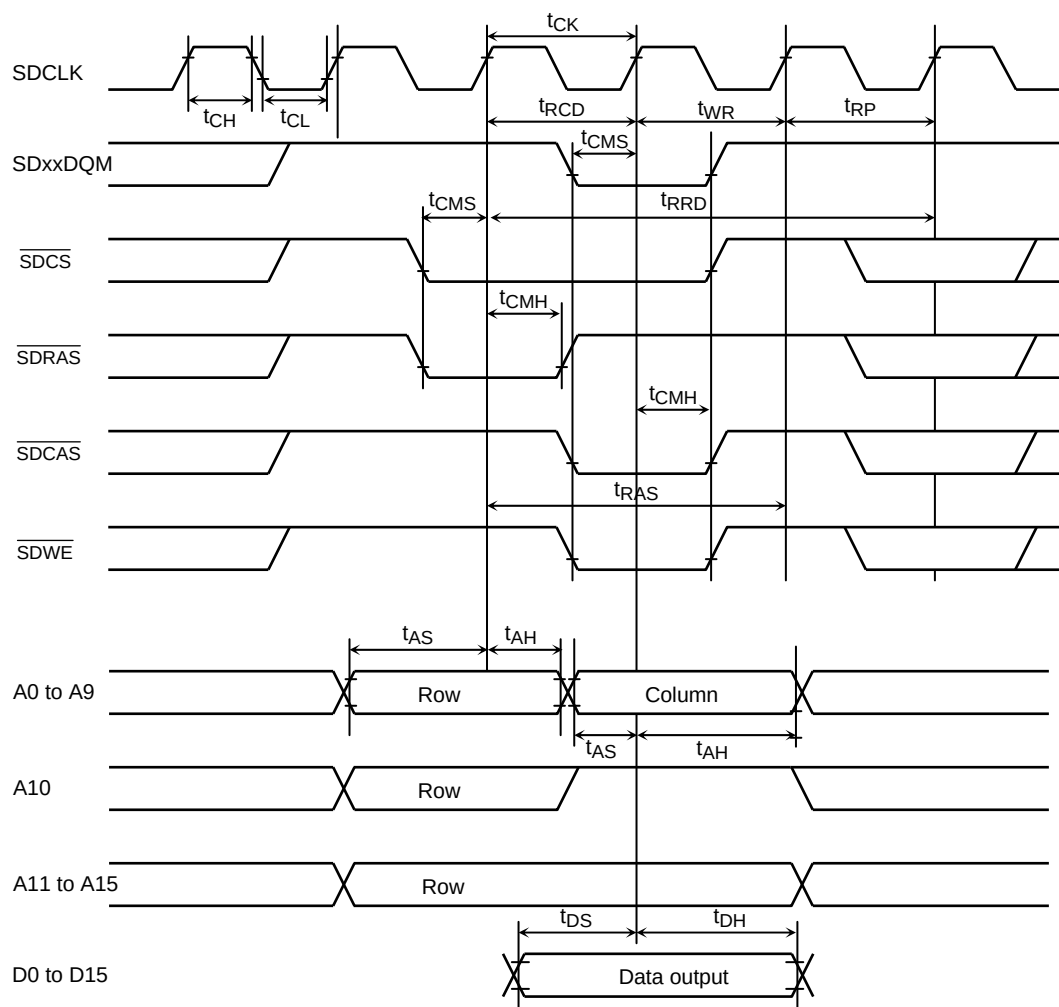
Note1: The Minimum cycle of "Active to pre-charge command period" is 2T (2 clocks) because the cycle of "READ/WRITE + PRECHARGE" occur by SDCISR<STRC2:0>="000", "001" and "010". If other settings the above setting, the clock is value of "Register setting value +1". (ex. if "010" setting, the clock is 3clocks.)

Note 2: The Minimum cycle of "Active to active command period" is 3T (3 clocks) because the cycle of "READ/WRITE + PRECHARGE + ACTIVE" occur by SDCISR<STRC2:0>="000", "001" and "010". If other settings the above setting, the clock is value of "Register setting value +1". (ex. if "011" setting, the clock is 4 clocks.)

(1) SDRAM read timing (1Word length read mode, <SPRE>= “1”)

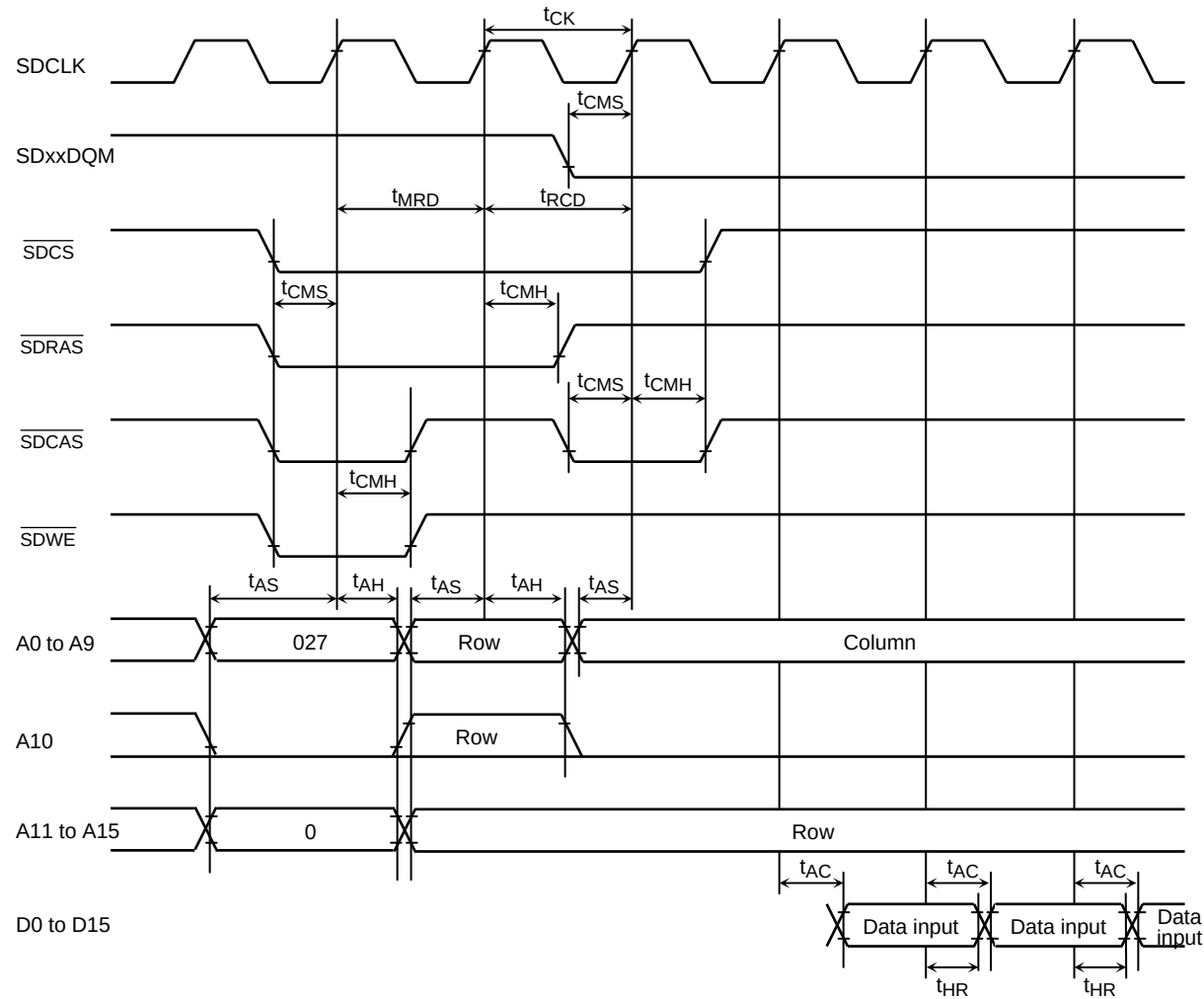


## (2) SDRAM write timing (Single write mode, &lt;SPRE&gt;= "1")

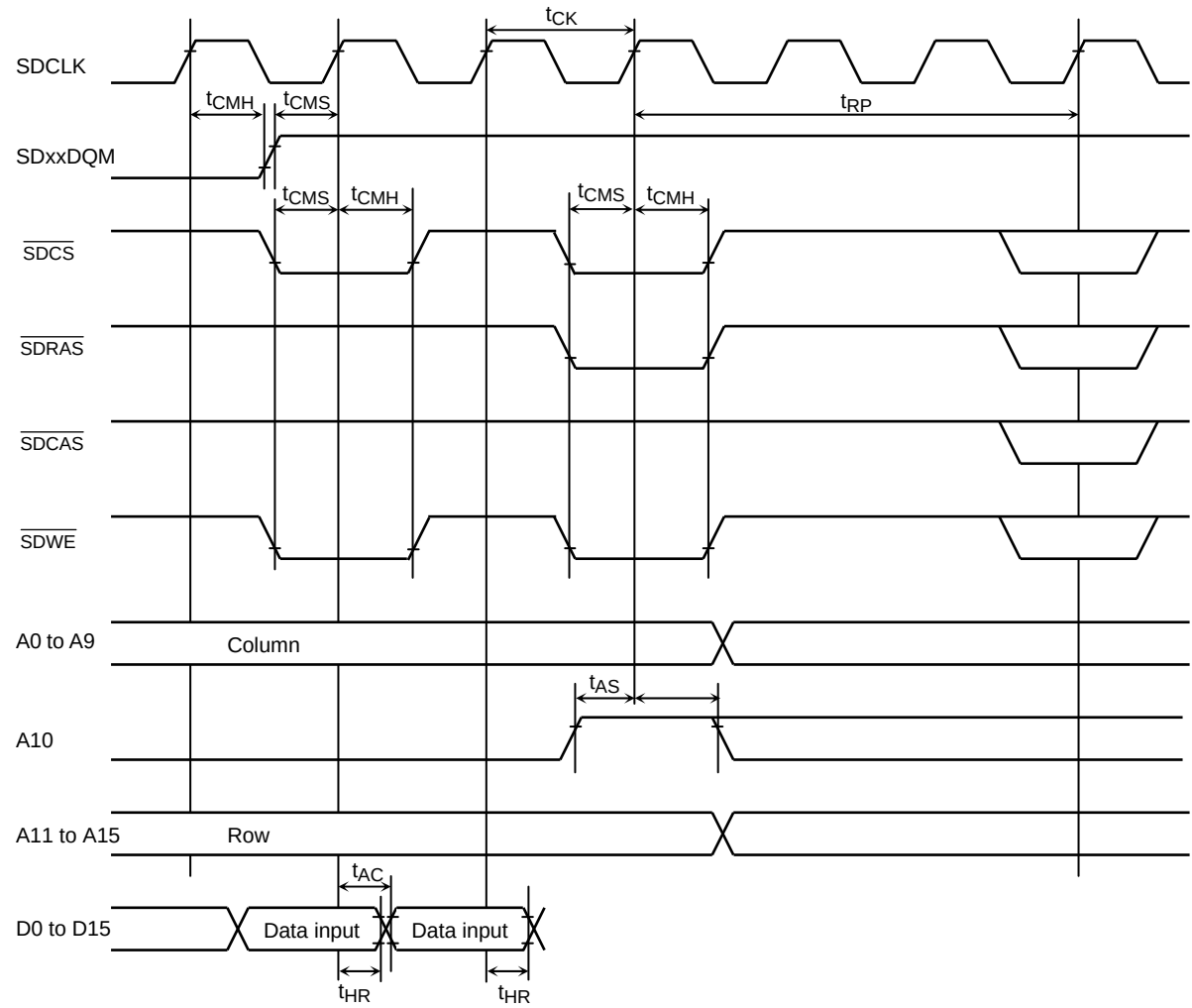




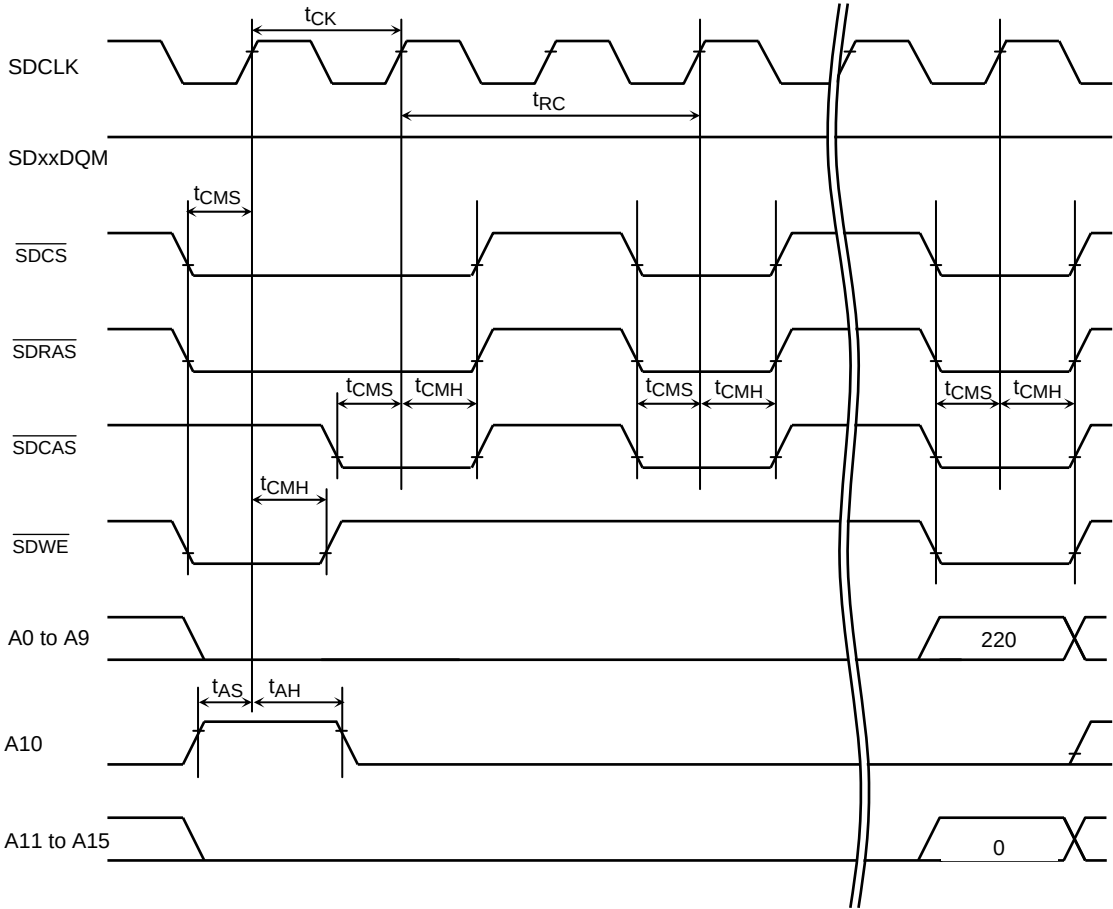
(3) SDRAM burst read timing (Start burst cycle)



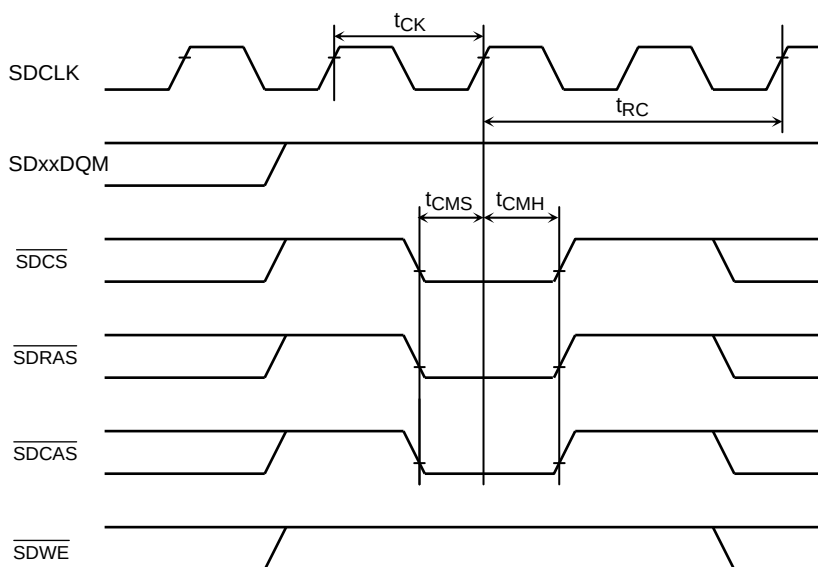
(4) SDRAM burst read timing (End burst timing)



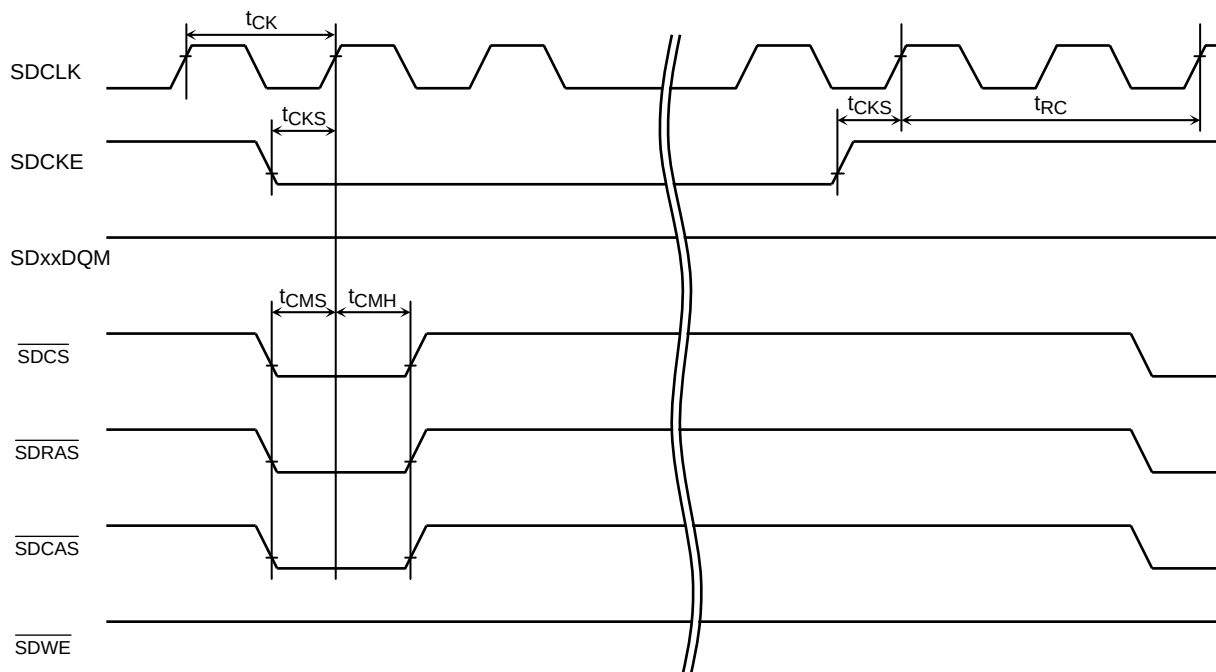
(5) SDRAM initializes timing



## (6) SDRAM refreshes timing



## (7) SDRAM self refresh timing



## 4.3.4 NAND Flash Controller AC Characteristics

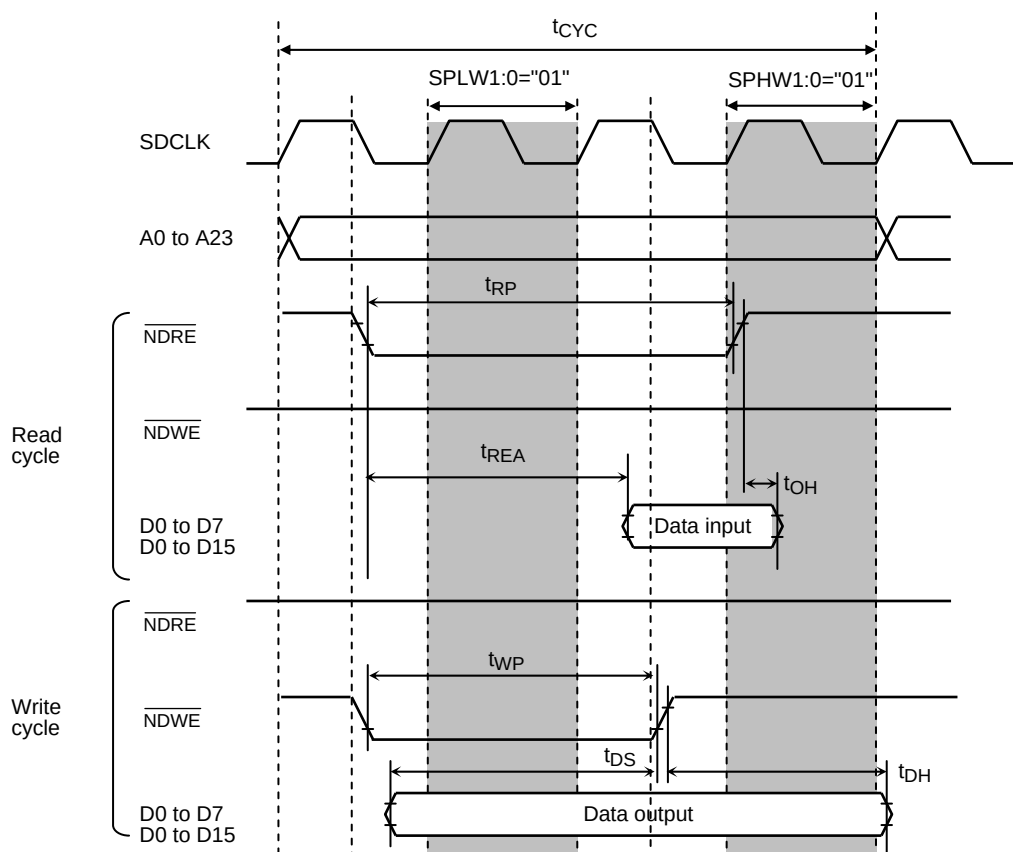
| No. | Symbol    | Parameter                          | Variable          |                   | 80 MHz         | 60 MHz         | Unit |
|-----|-----------|------------------------------------|-------------------|-------------------|----------------|----------------|------|
|     |           |                                    | Min               | Max               | (n=3)<br>(m=3) | (n=3)<br>(m=3) |      |
| 1   | $t_{NC}$  | Access cycle                       | $(2 + n + m)T$    |                   | 100            | 132            | ns   |
| 2   | $t_{RP}$  | $\overline{NDRE}$ low level width  | $(1.5 + n)T - 12$ |                   | 45             | 63             |      |
| 3   | $t_{REA}$ | $\overline{NDRE}$ data access time |                   | $(1.5 + n)T - 15$ | 41             | 60             |      |
| 4   | $t_{OH}$  | Read data hold time                | 0                 |                   | 0              | 0              |      |
| 5   | $t_{WP}$  | $\overline{NDWE}$ low level width  | $(1.0 + n)T - 20$ |                   | 30             | 47             |      |
| 6   | $t_{DS}$  | Write data setup time              | $(1.0 + n)T - 20$ |                   | 30             | 47             |      |
| 7   | $t_{DH}$  | Write data hold time               | $(0.5 + m)T - 2$  |                   | 42             | 56             |      |

AC measuring condition

Note1: The “n” in “Variable” means wait-number which is set to NDFMCR0<SPLW1:0>, and “m” means number which is set to NDFMCR0<SPHW1:0>.

Example: If NDFMCR0<SPLW1:0> is set to “01”,  $n = 1$ ,  $t_{RP} = (1.5 + n)T - 12 = 2.5T - 12$

Note2: In above variable, the setting that result is minus can not use.



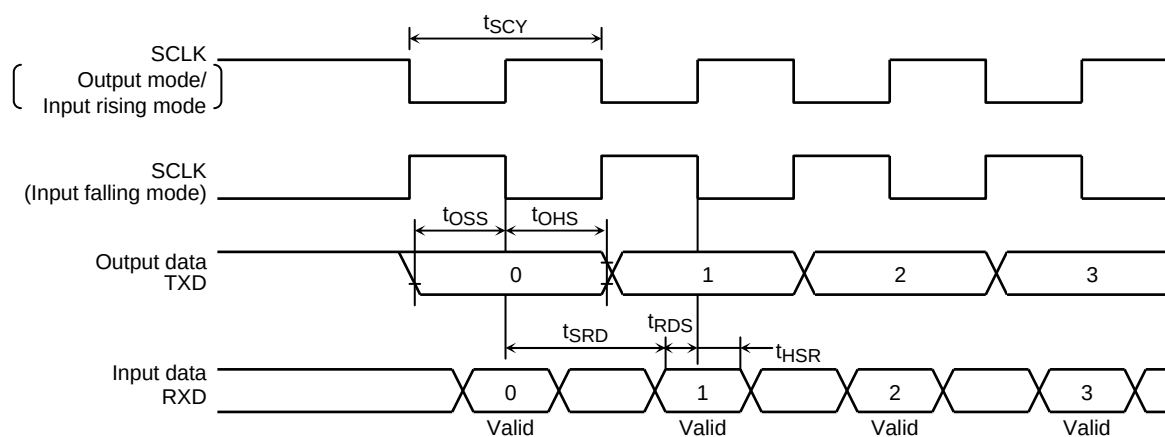
## 4.3.5 Serial channel timing

## (1) SCLK input mode (I/O interface mode)

| Parameter                               | Symbol    | Variable              |                | 80 MHz | 60 MHz | Unit |
|-----------------------------------------|-----------|-----------------------|----------------|--------|--------|------|
|                                         |           | Min                   | Max            |        |        |      |
| SCLK cycle                              | $t_{SCY}$ | 16T                   |                | 200    | 266    | ns   |
| Output data → SCLK rising/ falling      | $t_{OSS}$ | $t_{SCY}/2 - 4T - 30$ |                | 20     | 36.4   |      |
| SCLK rising/ falling → Output data hold | $t_{OHS}$ | $t_{SCY}/2 + 2T - 20$ |                | 105    | 146    |      |
| SCLK rising/ falling → Input data hold  | $t_{HSR}$ | $2T + 10$             |                | 35     | 43     |      |
| SCLK rising/ falling → Input data valid | $t_{SRD}$ |                       | $t_{SCY} - 20$ | 180    | 246    |      |
| Input data valid → SCLK rising/ falling | $t_{RDS}$ | 20                    |                | 20     | 20     |      |

## (2) SCLK output mode (I/O interface mode)

| Parameter                               | Symbol    | Variable         |                     | 80 MHz | 60 MHz | Unit |
|-----------------------------------------|-----------|------------------|---------------------|--------|--------|------|
|                                         |           | Min              | Max                 |        |        |      |
| SCLK cycle (Programmable)               | $t_{SCY}$ | 16T              | 8192T               | 200    | 266    | ns   |
| Output data → SCLK rising/ falling      | $t_{OSS}$ | $t_{SCY}/2 - 40$ |                     | 60     | 93     |      |
| SCLK rising/ falling → Output data hold | $t_{OHS}$ | $t_{SCY}/2 - 40$ |                     | 60     | 93     |      |
| SCLK rising/ falling → Input data hold  | $t_{HSR}$ | 0                |                     | 0      | 0      |      |
| SCLK rising/ falling → Input data valid | $t_{SRD}$ |                  | $t_{SCY} - 1T - 50$ | 137.5  | 199    |      |
| Input data valid → SCLK rising/ falling | $t_{RDS}$ | $1T + 50$        |                     | 62.5   | 66     |      |



4.3.6 Timer input pulse (TA0IN,TA2IN,TB0IN0,TB1IN0)

| Parameter              | Symbol     | Variable  |     | 80 MHz | 60 MHz | Unit |
|------------------------|------------|-----------|-----|--------|--------|------|
|                        |            | Min       | Max |        |        |      |
| Clock cycle            | $t_{VCK}$  | $8T+100$  |     | 200    | 234    | ns   |
| Low level pulse width  | $t_{VCKL}$ | $4T + 40$ |     | 90     | 107    |      |
| High level pulse width | $t_{VCKH}$ | $4T + 40$ |     | 90     | 107    |      |

4.3.7 Interrupt operation

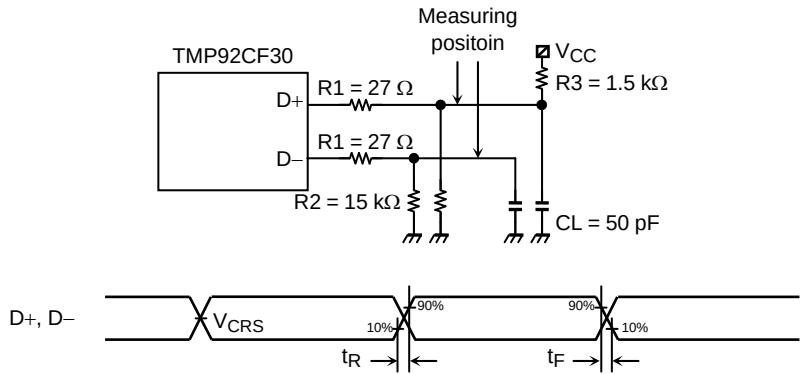
| Parameter            | Symbol      | Variable  |     | 80 MHz | 60 MHz | Unit |
|----------------------|-------------|-----------|-----|--------|--------|------|
|                      |             | Min       | Max |        |        |      |
| INT0~INT7 low width  | $t_{INTAL}$ | $2T + 40$ |     | 65     | 74     | ns   |
| INT0~INT7 high width | $t_{INTAH}$ | $2T + 40$ |     | 65     | 74     |      |

4.3.8 USB Timing (Full-speed)

$DVCCA = 3.3 \pm 0.3 \text{ V}/f_{USB} = 48 \text{ MHz}$

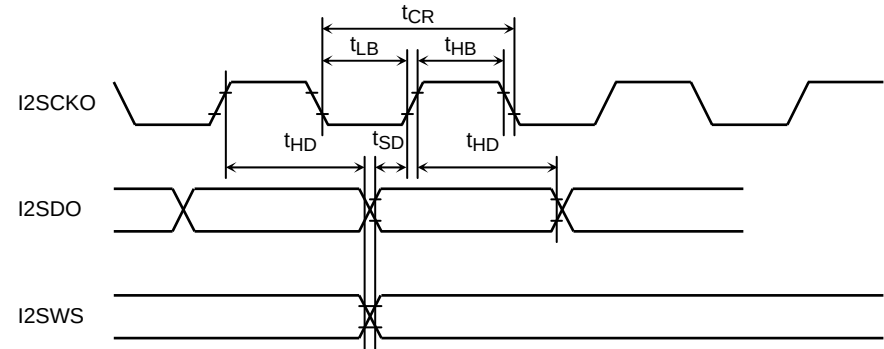
| Parameter                       | Symbol    | Min | Max | Unit |
|---------------------------------|-----------|-----|-----|------|
| D+, D- rising time              | $t_R$     | 4   | 20  | ns   |
| D+, D- falling time             | $t_F$     | 4   | 20  |      |
| Output signal crossover voltage | $V_{CRS}$ | 1.3 | 2.0 | V    |

AC measuring condition



4.3.9 I<sup>2</sup>S Timing

| Parameter               | Symbol          | Variable                 |     | 80 MHz | 60 MHz | Unit |
|-------------------------|-----------------|--------------------------|-----|--------|--------|------|
|                         |                 | Min                      | Max |        |        |      |
| I2SCKO clock period     | t <sub>CR</sub> | t <sub>IC</sub>          |     | 100    | 100    | ns   |
| I2SCKO high width       | t <sub>HB</sub> | 0.5 t <sub>CR</sub> – 15 |     | 35     | 35     |      |
| I2SCKO low width        | t <sub>LB</sub> | 0.5 t <sub>CR</sub> – 15 |     | 35     | 35     |      |
| I2SDO, I2SWS setup time | t <sub>SD</sub> | 0.5 t <sub>CR</sub> – 15 |     | 35     | 35     |      |
| I2SDO, I2SWS hold time  | t <sub>HD</sub> | 0.5 t <sub>CR</sub> – 8  |     | 42     | 42     |      |



Note: The Maximum operation frequency of I2SCKO in I<sup>2</sup>S circuit is 10MHz. Don't set I2SCKO to value more than 10MHz.

AC measuring condition

- I2SCKO, I2SDO and I2SWS pins C<sub>L</sub> = 30 pF

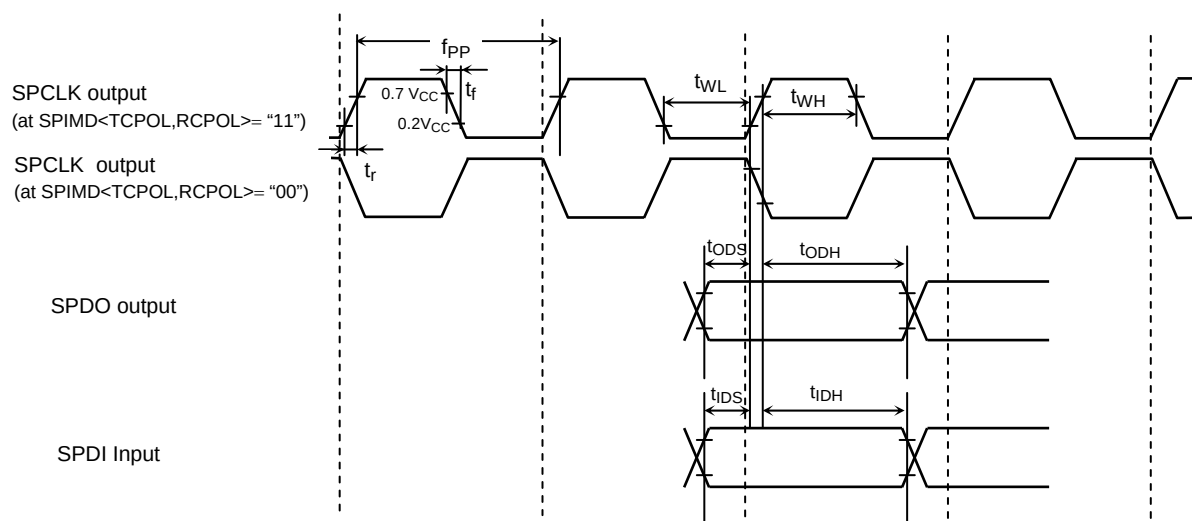


## 4.3.10 SPI Controller

| Parameter                                   | Symbol    | Variable  |     | 80 MHz | 60 MHz | Unit |
|---------------------------------------------|-----------|-----------|-----|--------|--------|------|
|                                             |           | Min       | Max |        |        |      |
| SPCLK frequency ( = 1/S)                    | $f_{PP}$  |           | 20  | 20     | 15     | MHz  |
| SPCLK rising time                           | $t_r$     |           | 6   | 6      | 6      | ns   |
| SPCLK falling time                          | $t_f$     |           | 6   | 6      | 6      |      |
| SPCLK low width                             | $t_{WL}$  | 0.5S – 6  |     | 19     | 28     |      |
| SPCLK high width                            | $t_{WH}$  | 0.5S – 6  |     | 19     | 28     |      |
| Output data valid<br>→ SPCLK rising/falling | $t_{ODS}$ | 0.5S – 18 |     | 7      | 15     |      |
| SPCLK rising/ falling<br>→ Output data hold | $t_{ODH}$ | 0.5S – 10 |     | 15     | 23.4   |      |
| Input data valid<br>→ SPCLK rising/ falling | $t_{IDS}$ | 5         |     | 5      | 5      |      |
| SPCLK rising/ falling<br>→ Input data valid | $t_{IDH}$ | 5         |     | 5      | 5      |      |

AC measuring condition

- Clock of top column in above table shows system clock frequency, and “S” in “Variable” show SPCLK clock cycle [ns].
- $C_L = 25$  pF



## 4.4 AD Conversion Characteristics

| Parameter                                               | Symbol         | Condition                | Min        | Typ.   | Max        | Unit |
|---------------------------------------------------------|----------------|--------------------------|------------|--------|------------|------|
| Analog reference voltage (+)                            | VREFH          |                          | AVCC – 0.2 | AVCC   | AVCC       | V    |
| Analog reference voltage (–)                            | VREFL          |                          | DVSS       | DVSS   | DVSS + 0.2 |      |
| AD converter power supply voltage                       | AVCC           |                          | DVCC3A     | DVCC3A | DVCC3A     |      |
| AD converter ground                                     | AVSS           |                          | DVSS       | DVSS   | DVSS       |      |
| Analog input voltage                                    | AVIN           |                          | VREFL      |        | VREFH      |      |
| Analog current for analog reference voltage             | IREFON         | <VREFON> = "1"           |            | 0.38   | 0.45       | mA   |
|                                                         | IREFOFF        | <VREFON> = "0"           |            | 1      | 5          | μA   |
| Total error<br>(Quantize error of ±0.5 LSB is included) | E <sub>T</sub> | Conversion speed at 12μs |            | ±2.0   | ±4.0       | LSB  |

Note1: 1 LSB = (VREFH–VREFL)/1024[V]

Note2: Minimum frequency for operation

Minimum clock for AD converter operate is 3MHz. (Clock frequency that is selected by Clock gear ≥ f<sub>sys</sub> = 3MHz)

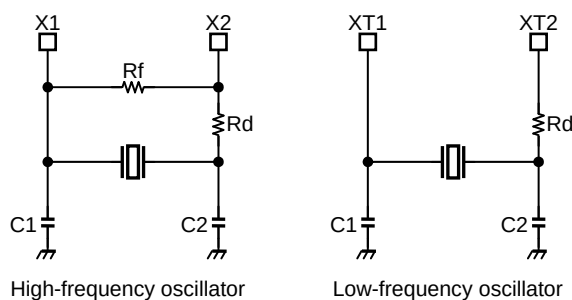
Note3: The power supply current from AVCC pin is included in the power supply current of V<sub>CC</sub> pin (I<sub>CC</sub>).

## 4.5 Recommended Oscillation Circuit

The TMP92CF30 has been evaluated by the oscillator vender below. Use this information when selecting external parts.

Note: The total load value of the oscillator is the sum of external loads (C1 and C2) and the floating load of the actual assembled board. There is a possibility of operating error when using C1 and C2 values in the table below. When designing the board, design the minimum length pattern around the oscillator. We also recommend that oscillator evaluation be carried out using the actual board.

### (1) Connection example



### (2) Recommended ceramic oscillator

TMP92CF30 recommends the high-frequency oscillator by Murata Manufacturing Co., Ltd.

Please refer to the following URL;

<http://www.murata.com/>

## 5. Table of Special function registers (SFRs)

The SFRs include the I/O ports and peripheral control registers allocated to the 8-Kbyte address space from 000000H to 001FF0H.

- |                           |                                  |
|---------------------------|----------------------------------|
| (1) I/O Port              | (11) Clock gear, PLL             |
| (2) Interrupt control     | (12) 8-bit timer                 |
| (3) Memory controller     | (13) 16-bit timer                |
| (4) TSI(Touch screen I/F) | (14) SIO                         |
| (5) SDRAM controller      | (15) SBI                         |
| (6) USB controller        | (16) AD converter                |
| (7) SPI controller        | (17) Watchdog timer              |
| (8) MMU                   | (18) RTC(Real time clock)        |
| (9) NAND-Flash controller | (19) MLD(Melody/alarm generator) |
| (10) DMA controller       | (20) I <sup>2</sup> S            |
|                           | (21) MAC                         |

Table layout

| Symbol | Name | Address | 7 | 6 |  |  | 1 | 0 |                                  |
|--------|------|---------|---|---|--|--|---|---|----------------------------------|
|        |      |         |   |   |  |  |   |   | Bit Symbol                       |
|        |      |         |   |   |  |  |   |   | Read/Write                       |
|        |      |         |   |   |  |  |   |   | Initial value after system reset |
|        |      |         |   |   |  |  |   |   | Remarks                          |

Note: "Prohibit RMW" in the table means that you cannot use RMW instructions on these register.

Example: When setting bit0 only of the register PxCR, the instruction "SET 0, (PxCR)" cannot be used. The LD (transfer) instruction must be used to write all eight bits.

### Read/Write

- R/W: Both read and write are possible.
- R: Only read is possible.
- W: Only write is possible.
- W\*: Both read and write are possible (when this bit is read as 1)
- Prohibit RMW: Read modify write instructions are prohibited. (The EX, ADD, ADC, BUS, SBC, INC, DEC, AND, OR, XOR, STCF, RES, SET, CHG, TSET, RLC, RRC, RL, RR, SLA, SRA, SLL, SRL, RLD and RRD instruction are read modify write instructions.)
- R/W\*: Read modify write is prohibited when controlling the pull-up resistor.

Table 5.1 I/O Register Address Map

[1] Port (1/2)

| Address | Name | Address | Name | Address | Name  | Address | Name  |
|---------|------|---------|------|---------|-------|---------|-------|
| 0000H   |      | 0010H   | P4   | 0020H   | P8    | 0030H   | PC    |
| 1H      |      | 1H      |      | 1H      | P8FC2 | 1H      | PCFC2 |
| 2H      |      | 2H      |      | 2H      |       | 2H      | PCCR  |
| 3H      |      | 3H      | P4FC | 3H      | P8FC  | 3H      | PCFC  |
| 4H      | P1   | 4H      | P5   | 4H      | P9    | 4H      |       |
| 5H      |      | 5H      |      | 5H      | P9FC2 | 5H      |       |
| 6H      | P1CR | 6H      |      | 6H      | P9CR  | 6H      |       |
| 7H      | P1FC | 7H      | P5FC | 7H      | P9FC  | 7H      |       |
| 8H      |      | 8H      | P6   | 8H      | PA    | 8H      |       |
| 9H      |      | 9H      |      | 9H      |       | 9H      |       |
| AH      |      | AH      | P6CR | AH      |       | AH      |       |
| BH      |      | BH      | P6FC | BH      | PAFC  | BH      |       |
| CH      |      | CH      | P7   | CH      |       | CH      | PF    |
| DH      |      | DH      |      | DH      |       | DH      |       |
| EH      |      | EH      | P7CR | EH      |       | EH      | PFCR  |
| FH      |      | FH      | P7FC | FH      |       | FH      | PFFC  |

| Address | Name | Address | Name     | Address | Name  | Address | Name     |
|---------|------|---------|----------|---------|-------|---------|----------|
| 0040H   | PG   | 0050H   | PK       | 0060H   | PP    | 0070H   | Reserved |
| 1H      |      | 1H      |          | 1H      | PPFC2 | 1H      | Reserved |
| 2H      |      | 2H      |          | 2H      | PPCR  | 2H      | Reserved |
| 3H      | PGFC | 3H      | Reserved | 3H      | PPFC  | 3H      | Reserved |
| 4H      |      | 4H      | PL       | 4H      | PR    | 4H      | Reserved |
| 5H      |      | 5H      | PLFC2    | 5H      |       | 5H      | Reserved |
| 6H      |      | 6H      | PLCR     | 6H      | PRCR  | 6H      | Reserved |
| 7H      |      | 7H      | PLFC     | 7H      | PRFC  | 7H      | Reserved |
| 8H      |      | 8H      | PM       | 8H      |       | 8H      | Reserved |
| 9H      |      | 9H      |          | 9H      |       | 9H      | Reserved |
| AH      |      | AH      |          | AH      |       | AH      | Reserved |
| BH      |      | BH      | PMFC     | BH      |       | BH      | Reserved |
| CH      | PJ   | CH      | PN       | CH      |       | CH      | Reserved |
| DH      |      | DH      |          | DH      |       | DH      | Reserved |
| EH      | PJCR | EH      | PNCR     | EH      |       | EH      | Reserved |
| FH      | PJFC | FH      | PNFC     | FH      |       | FH      | Reserved |

## [1] Port (2/2)

| Address | Name | Address | Name | Address | Name  | Address | Name  |
|---------|------|---------|------|---------|-------|---------|-------|
| 0080H   |      | 0090H   | PGDR | 00A0H   | PT    | 00B0H   | PX    |
| 1H      | P1DR | 1H      |      | 1H      | PTFC2 | 1H      | PXFC2 |
| 2H      |      | 2H      |      | 2H      | PTCR  | 2H      | PXCR  |
| 3H      |      | 3H      | PJDR | 3H      | PTFC  | 3H      | PXFC  |
| 4H      | P4DR | 4H      | PKDR | 4H      |       | 4H      |       |
| 5H      | P5DR | 5H      | PLDR | 5H      |       | 5H      |       |
| 6H      | P6DR | 6H      | PMDR | 6H      |       | 6H      |       |
| 7H      | P7DR | 7H      | PNDR | 7H      |       | 7H      |       |
| 8H      | P8DR | 8H      | PPDR | 8H      | PV    | 8H      |       |
| 9H      | P9DR | 9H      | PRDR | 9H      | PVFC2 | 9H      |       |
| AH      | PADR | AH      |      | AH      | PVCR  | AH      |       |
| BH      |      | BH      | PTDR | BH      | PVFC  | BH      |       |
| CH      | PCDR | CH      |      | CH      |       | CH      |       |
| DH      |      | DH      | PVDR | DH      |       | DH      |       |
| EH      |      | EH      |      | EH      |       | EH      |       |
| FH      | PFDR | FH      | PXDR | FH      |       | FH      |       |

Note: Do not access no allocated name address.

## [2] INTC

| Address | Name     | Address | Name       | Address | Name                   | Address | Name   |
|---------|----------|---------|------------|---------|------------------------|---------|--------|
| 00D0H   | INTE12   | 00E0H   | INTESBIADM | 00F0H   | INTE0                  | 0100H   | DMA0V  |
| 1H      | INTE34   | 1H      | INTESPI    | 1H      | INTETC01<br>/INTEDMA01 | 1H      | DMA1V  |
| 2H      | INTE56   | 2H      | Reserved   | 2H      | INTETC23<br>/INTEDMA23 | 2H      | DMA2V  |
| 3H      | INTE7    | 3H      | INTEUSB    | 3H      | INTETC45<br>/INTEDMA45 | 3H      | DMA3V  |
| 4H      | INTETA01 | 4H      | Reserved   | 4H      | INTETC67               | 4H      | DMA4V  |
| 5H      | INTETA23 | 5H      | INTEALM    | 5H      | SIMC                   | 5H      | DMA5V  |
| 6H      | INTETA45 | 6H      | Reserved   | 6H      | IIMC0                  | 6H      | DMA6V  |
| 7H      | INTETA67 | 7H      |            | 7H      | INTWDT/NMI             | 7H      | DMA7V  |
| 8H      | INTETB0  | 8H      | INTERTC    | 8H      | INTCLR                 | 8H      | DMAB   |
| 9H      | INTETB1  | 9H      | INTEKEY    | 9H      |                        | 9H      | DMAR   |
| AH      |          | AH      | Reserved   | AH      | IIMC1                  | AH      | DMASEL |
| BH      | INTES0   | BH      | INTEI2S0   | BH      |                        | BH      |        |
| CH      | INTES1   | CH      | INTENDFC   | CH      |                        | CH      |        |
| DH      |          | DH      | Reserved   | DH      |                        | DH      |        |
| EH      |          | EH      | INTEP0     | EH      |                        | EH      |        |
| FH      |          | FH      | INTEAD     | FH      | Reserved               | FH      |        |

## [3] MEMC

| Address | Name  | Address | Name   | Address | Name     | Address | Name     |
|---------|-------|---------|--------|---------|----------|---------|----------|
| 0140H   | B0CSL | 0150H   |        | 0160H   |          | 01F0H   | TSICR0   |
| 1H      | B0CSH | 1H      |        | 1H      |          | 1H      | TSICR1   |
| 2H      | MAMR0 | 2H      |        | 2H      |          | 2H      | Reserved |
| 3H      | MSAR0 | 3H      |        | 3H      |          | 3H      |          |
| 4H      | B1CSL | 4H      |        | 4H      |          | 4H      |          |
| 5H      | B1CSH | 5H      |        | 5H      |          | 5H      |          |
| 6H      | MAMR1 | 6H      |        | 6H      | PMEMCR   | 6H      |          |
| 7H      | MSAR1 | 7H      |        | 7H      |          | 7H      |          |
| 8H      | B2CSL | 8H      | BEXCSL | 8H      | CSTMGCR  | 8H      |          |
| 9H      | B2CSH | 9H      | BEXCSH | 9H      | WRTMGCR  | 9H      |          |
| AH      | MAMR2 | AH      |        | AH      | RDTMGCR0 | AH      |          |
| BH      | MSAR2 | BH      |        | BH      | RDTMGCR1 | BH      |          |
| CH      | B3CSL | CH      |        | CH      | BROMCR   | CH      |          |
| DH      | B3CSH | DH      |        | DH      | RAMCR    | DH      |          |
| EH      | MAMR3 | EH      |        | EH      |          | EH      |          |
| FH      | MSAR3 | FH      |        | FH      |          | FH      |          |

## [4] TSI

Note: Do not access no allocated name address.

[5] SDRAMC

| Address | Name   |
|---------|--------|
| 0250H   | SDACR  |
| 1H      | SDCISR |
| 2H      | SDRCR  |
| 3H      | SDCMM  |
| 4H      | SDBLS  |
| 5H      |        |
| 6H      |        |
| 7H      |        |
| 8H      |        |
| 9H      |        |
| AH      |        |
| BH      |        |
| CH      |        |
| DH      |        |
| EH      |        |
| FH      |        |

| Address | Name     | Address | Name     | Address | Name     | Address | Name     |
|---------|----------|---------|----------|---------|----------|---------|----------|
| 0280H   | Reserved | 0290H   | Reserved | 02A0H   | Reserved | 02F0H   | Reserved |
| 1H      | Reserved | 1H      | Reserved | 1H      | Reserved | 1H      |          |
| 2H      | Reserved | 2H      | Reserved | 2H      | Reserved | 2H      |          |
| 3H      | Reserved | 3H      | Reserved | 3H      |          | 3H      |          |
| 4H      | Reserved | 4H      | Reserved | 4H      | Reserved | 4H      |          |
| 5H      | Reserved | 5H      | Reserved | 5H      | Reserved | 5H      |          |
| 6H      | Reserved | 6H      | Reserved | 6H      | Reserved | 6H      |          |
| 7H      | Reserved | 7H      | Reserved | 7H      |          | 7H      |          |
| 8H      | Reserved | 8H      | Reserved | 8H      | Reserved | 8H      |          |
| 9H      | Reserved | 9H      | Reserved | 9H      | Reserved | 9H      |          |
| AH      | Reserved | AH      |          | AH      | Reserved | AH      |          |
| BH      | Reserved | BH      |          | BH      | Reserved | BH      |          |
| CH      | Reserved | CH      |          | CH      | Reserved | CH      |          |
| DH      | Reserved | DH      |          | DH      | Reserved | DH      |          |
| EH      | Reserved | EH      |          | EH      | Reserved | EH      |          |
| FH      | Reserved | FH      |          | FH      | Reserved | FH      |          |

Note: Do not access no allocated name address.



## [6] USBC (1/2)

| Address              | Name                            | Address | Name      | Address | Name         | Address | Name         |
|----------------------|---------------------------------|---------|-----------|---------|--------------|---------|--------------|
| 0500H<br>to<br>067FH | Descriptor<br>RAM<br>(384 byte) | 0780H   | ENDPOINT0 | 0790H   | EP0_STATUS   | 07A0H   |              |
|                      |                                 | 1H      | ENDPOINT1 | 1H      | EP1_STATUS   | 1H      | EP1_SIZE_L_B |
|                      |                                 | 2H      | ENDPOINT2 | 2H      | EP2_STATUS   | 2H      | EP2_SIZE_L_B |
|                      |                                 | 3H      | ENDPOINT3 | 3H      | EP3_STATUS   | 3H      | EP3_SIZE_L_B |
|                      |                                 | 4H      |           | 4H      |              | 4H      |              |
|                      |                                 | 5H      |           | 5H      |              | 5H      |              |
|                      |                                 | 6H      |           | 6H      |              | 6H      |              |
|                      |                                 | 7H      |           | 7H      |              | 7H      |              |
|                      |                                 | 8H      | Reserved  | 8H      | EP0_SIZE_L_A | 8H      | Reserved     |
|                      |                                 | 9H      | EP1_MODE  | 9H      | EP1_SIZE_L_A | 9H      | EP1_SIZE_H_A |
|                      |                                 | AH      | EP2_MODE  | AH      | EP2_SIZE_L_A | AH      | EP2_SIZE_H_A |
|                      |                                 | BH      | EP3_MODE  | BH      | EP3_SIZE_L_A | BH      | EP3_SIZE_H_A |
|                      |                                 | CH      |           | CH      |              | CH      |              |
|                      |                                 | DH      |           | DH      |              | DH      |              |
|                      |                                 | EH      |           | EH      |              | EH      |              |
|                      |                                 | FH      |           | FH      |              | FH      |              |

| Address | Name         | Address | Name             | Address | Name                  |
|---------|--------------|---------|------------------|---------|-----------------------|
| 07B0H   |              | 07C0H   | bmRequestType    | 07D0H   | COMMAND               |
| 1H      | EP1_SIZE_H_B | 1H      | bRequest         | 1H      | EPx_SINGLE1           |
| 2H      | EP2_SIZE_H_B | 2H      | wValue_L         | 2H      | Reserved              |
| 3H      | EP3_SIZE_H_B | 3H      | wValue_H         | 3H      | EPx_BCS1              |
| 4H      |              | 4H      | wIndex_L         | 4H      | Reserved              |
| 5H      |              | 5H      | wIndex_H         | 5H      | Reserved              |
| 6H      |              | 6H      | wLength_L        | 6H      | INT_Control           |
| 7H      |              | 7H      | wLength_H        | 7H      | Reserved              |
| 8H      |              | 8H      | SetupReceived    | 8H      | Standard Request Mode |
| 9H      |              | 9H      | Current_Config   | 9H      | Request Mode          |
| AH      |              | AH      | Standard Request | AH      | Reserved              |
| BH      |              | BH      | Request          | BH      | Reserved              |
| CH      |              | CH      | DATASET1         | CH      | Reserved              |
| DH      |              | DH      | DATASET2         | DH      | Reserved              |
| EH      |              | EH      | USB STATE        | EH      | ID_CONTROL            |
| FH      |              | FH      | EOP              | FH      | ID_STATE              |

Note: Do not access no allocated name address.

[6] USBC (2/2)

| Address | Name                 | Address | Name      |
|---------|----------------------|---------|-----------|
| 07E0H   | Port Status          | 07F0H   | USBINTFR1 |
| 1H      | FRAME_L              | 1H      | USBINTFR2 |
| 2H      | FRAME_H              | 2H      | USBINTFR3 |
| 3H      | ADDRESS              | 3H      | USBINTFR4 |
| 4H      | Reserved             | 4H      | USBINTMR1 |
| 5H      | Reserved             | 5H      | USBINTMR2 |
| 6H      | USBREADY             | 6H      | USBINTMR3 |
| 7H      | Reserved             | 7H      | USBINTMR4 |
| 8H      | Set Descriptor STALL | 8H      | USBCR1    |
| 9H      |                      | 9H      |           |
| AH      |                      | AH      |           |
| BH      |                      | BH      |           |
| CH      |                      | CH      |           |
| DH      |                      | DH      |           |
| EH      |                      | EH      |           |
| FH      |                      | FH      |           |

Note: Do not access no allocated name address.

## [7] SPIC

| Address | Name  | Address | Name   |
|---------|-------|---------|--------|
| 0820H   | SPIMD | 0830H   | SPITD0 |
| 1H      | SPIMD | 1H      | SPITD0 |
| 2H      | SPICT | 2H      | SPITD1 |
| 3H      | SPICT | 3H      | SPITD1 |
| 4H      | SPIST | 4H      | SPIRD0 |
| 5H      | SPIST | 5H      | SPIRD0 |
| 6H      | SPICR | 6H      | SPIRD1 |
| 7H      | SPICR | 7H      | SPIRD1 |
| 8H      |       | 8H      |        |
| 9H      |       | 9H      |        |
| AH      |       | AH      |        |
| BH      |       | BH      |        |
| CH      | SPIIE | CH      |        |
| DH      | SPIIE | DH      |        |
| EH      |       | EH      |        |
| FH      |       | FH      |        |

## [8] MMU

| Address | Name     | Address | Name    | Address | Name     | Address | Name     |
|---------|----------|---------|---------|---------|----------|---------|----------|
| 0880H   | LOCALPX  | 0890H   | LOCALRX | 08A0H   | LOCALESX | 08B0H   | LOCALOSX |
| 1H      | LOCALPX  | 1H      | LOCALRX | 1H      | LOCALESX | 1H      | LOCALOSX |
| 2H      | LOCALPY  | 2H      | LOCALRY | 2H      | LOCALESY | 2H      | LOCALOSY |
| 3H      | LOCALPY  | 3H      | LOCALRY | 3H      | LOCALESY | 3H      | LOCALOSY |
| 4H      | LOCALPZ  | 4H      | LOCALRZ | 4H      | LOCALESZ | 4H      | LOCALOSZ |
| 5H      | LOCALPZ  | 5H      | LOCALRZ | 5H      | LOCALESZ | 5H      | LOCALOSZ |
| 6H      |          | 6H      |         | 6H      |          | 6H      |          |
| 7H      |          | 7H      |         | 7H      |          | 7H      |          |
| 8H      | Reserved | 8H      | LOCALWX | 8H      | LOCALEDX | 8H      | LOCALODX |
| 9H      | Reserved | 9H      | LOCALWX | 9H      | LOCALEDX | 9H      | LOCALODX |
| AH      | Reserved | AH      | LOCALWY | AH      | LOCALEDY | AH      | LOCALODY |
| BH      | Reserved | BH      | LOCALWY | BH      | LOCALEDY | BH      | LOCALODY |
| CH      | Reserved | CH      | LOCALWZ | CH      | LOCALEDZ | CH      | LOCALODZ |
| DH      | Reserved | DH      | LOCALWZ | DH      | LOCALEDZ | DH      | LOCALODZ |
| EH      |          | EH      |         | EH      |          | EH      |          |
| FH      |          | FH      |         | FH      |          | FH      |          |

Note: Do not access no allocated name address.

[9] NAND-Flash controller

| Address | Name     | Address | Name    | Address | Name    |
|---------|----------|---------|---------|---------|---------|
| 08C0H   | NDFMCR0  | 08D0H   | NDRSCA0 | 1FF0H   | NDFDTR0 |
| 1H      | NDFMCR0  | 1H      | NDRSCA0 | 1H      | NDFDTR0 |
| 2H      | NDFMCR1  | 2H      | NDRSCD0 | 2H      | NDFDTR1 |
| 3H      | NDFMCR1  | 3H      |         | 3H      | NDFDTR1 |
| 4H      | NDECARD0 | 4H      | NDRSCA1 | 4H      |         |
| 5H      | NDECARD0 | 5H      | NDRSCA1 | 5H      |         |
| 6H      | NDECARD1 | 6H      | NDRSCD1 | 6H      |         |
| 7H      | NDECARD1 | 7H      |         | 7H      |         |
| 8H      | NDECARD2 | 8H      | NDRSCA2 | 8H      |         |
| 9H      | NDECARD2 | 9H      | NDRSCA2 | 9H      |         |
| AH      | NDECARD3 | AH      | NDRSCD2 | AH      |         |
| BH      | NDECARD3 | BH      |         | BH      |         |
| CH      | NDECARD4 | CH      | NDRSCA3 | CH      |         |
| DH      | NDECARD4 | DH      | NDRSCA3 | DH      |         |
| EH      |          | EH      | NDRSCD3 | EH      |         |
| FH      |          | FH      |         | FH      |         |

Note: Do not access no allocated name address.

## [10] DMAC

| Address | Name    | Address | Name    | Address | Name    | Address | Name    |
|---------|---------|---------|---------|---------|---------|---------|---------|
| 0900H   | HDMAS0  | 0910H   | HDMAS1  | 0920H   | HDMAS2  | 0930H   | HDMAS3  |
| 1H      | HDMAS0  | 1H      | HDMAS1  | 1H      | HDMAS2  | 1H      | HDMAS3  |
| 2H      | HDMAS0  | 2H      | HDMAS1  | 2H      | HDMAS2  | 2H      | HDMAS3  |
| 3H      |         | 3H      |         | 3H      |         | 3H      |         |
| 4H      | HDMAD0  | 4H      | HDMAD1  | 4H      | HDMAD2  | 4H      | HDMAD3  |
| 5H      | HDMAD0  | 5H      | HDMAD1  | 5H      | HDMAD2  | 5H      | HDMAD3  |
| 6H      | HDMAD0  | 6H      | HDMAD1  | 6H      | HDMAD2  | 6H      | HDMAD3  |
| 7H      |         | 7H      |         | 7H      |         | 7H      |         |
| 8H      | HDMACA0 | 8H      | HDMACA1 | 8H      | HDMACA2 | 8H      | HDMACA3 |
| 9H      | HDMACA0 | 9H      | HDMACA1 | 9H      | HDMACA2 | 9H      | HDMACA3 |
| AH      | HDMACB0 | AH      | HDMACB1 | AH      | HDMACB2 | AH      | HDMACB3 |
| BH      | HDMACB0 | BH      | HDMACB1 | BH      | HDMACB2 | BH      | HDMACB3 |
| CH      | HDMAM0  | CH      | HDMAM1  | CH      | HDMAM2  | CH      | HDMAM3  |
| DH      |         | DH      |         | DH      |         | DH      |         |
| EH      |         | EH      |         | EH      |         | EH      |         |
| FH      |         | FH      |         | FH      |         | FH      |         |

| Address | Name    | Address | Name    | Address | Name     |
|---------|---------|---------|---------|---------|----------|
| 0940H   | HDMAS4  | 0950H   | HDMAS5  | 0970H   |          |
| 1H      | HDMAS4  | 1H      | HDMAS5  | 1H      |          |
| 2H      | HDMAS4  | 2H      | HDMAS5  | 2H      |          |
| 3H      |         | 3H      |         | 3H      |          |
| 4H      | HDMAD4  | 4H      | HDMAD5  | 4H      |          |
| 5H      | HDMAD4  | 5H      | HDMAD5  | 5H      |          |
| 6H      | HDMAD4  | 6H      | HDMAD5  | 6H      |          |
| 7H      |         | 7H      |         | 7H      |          |
| 8H      | HDMACA4 | 8H      | HDMACA5 | 8H      |          |
| 9H      | HDMACA4 | 9H      | HDMACA5 | 9H      |          |
| AH      | HDMACB4 | AH      | HDMACB5 | AH      |          |
| BH      | HDMACB4 | BH      | HDMACB5 | BH      |          |
| CH      | HDMAM4  | CH      | HDMAM5  | CH      | Reserved |
| DH      |         | DH      |         | DH      | Reserved |
| EH      |         | EH      |         | EH      | HDMAE    |
| FH      |         | FH      |         | FH      | HDMATR   |

Note: Do not access no allocated name address.

[11] CGEAR, PLL

| Address | Name     |
|---------|----------|
| 10E0H   | SYSCR0   |
| 1H      | SYSCR1   |
| 2H      | SYSCR2   |
| 3H      | EMCCR0   |
| 4H      | EMCCR1   |
| 5H      | EMCCR2   |
| 6H      | Reserved |
| 7H      |          |
| 8H      | PLLCR0   |
| 9H      | PLLCR1   |
| AH      |          |
| BH      |          |
| CH      |          |
| DH      |          |
| EH      |          |
| FH      |          |

[12] 8-bit timer

| Address | Name    |
|---------|---------|
| 1100H   | TA01RUN |
| 1H      |         |
| 2H      | TA0REG  |
| 3H      | TA1REG  |
| 4H      | TA01MOD |
| 5H      | TA1FFCR |
| 6H      |         |
| 7H      |         |
| 8H      | TA23RUN |
| 9H      |         |
| AH      | TA2REG  |
| BH      | TA3REG  |
| CH      | TA23MOD |
| DH      | TA3FFCR |
| EH      |         |
| FH      |         |

| Address | Name     |
|---------|----------|
| 1110H   | TA45RUN  |
| 1H      |          |
| 2H      | TA4REG   |
| 3H      | TA5REG   |
| 4H      | TA45MOD  |
| 5H      | Reserved |
| 6H      |          |
| 7H      |          |
| 8H      | TA67RUN  |
| 9H      |          |
| AH      | TA6REG   |
| BH      | TA7REG   |
| CH      | TA67MOD  |
| DH      | TA7FFCR  |
| EH      |          |
| FH      |          |

[13] 16-bit timer

| Address | Name    |
|---------|---------|
| 1180H   | TB0RUN  |
| 1H      |         |
| 2H      | TB0MOD  |
| 3H      | TB0FFCR |
| 4H      |         |
| 5H      |         |
| 6H      |         |
| 7H      |         |
| 8H      | TB0RG0L |
| 9H      | TB0RG0H |
| AH      | TB0RG1L |
| BH      | TB0RG1H |
| CH      | TB0CP0L |
| DH      | TB0CP0H |
| EH      | TB0CP1L |
| FH      | TB0CP1H |

| Address | Name     |
|---------|----------|
| 1190H   | TB1RUN   |
| 1H      |          |
| 2H      | TB1MOD   |
| 3H      | Reserved |
| 4H      |          |
| 5H      |          |
| 6H      |          |
| 7H      |          |
| 8H      | TB1RG0L  |
| 9H      | TB1RG0H  |
| AH      | TB1RG1L  |
| BH      | TB1RG1H  |
| CH      | TB1CP0L  |
| DH      | TB1CP0H  |
| EH      | TB1CP1L  |
| FH      | TB1CP1H  |

[14] SIO

| Address | Name    |
|---------|---------|
| 1200H   | SC0BUF  |
| 1H      | SC0CR   |
| 2H      | SC0MOD0 |
| 3H      | BR0CR   |
| 4H      | BR0ADD  |
| 5H      | SC0MOD1 |
| 6H      |         |
| 7H      | SIR0CR  |
| 8H      | SC1BUF  |
| 9H      | SC1CR   |
| AH      | SC1MOD0 |
| BH      | BR1CR   |
| CH      | BR1ADD  |
| DH      | SC1MOD1 |
| EH      |         |
| FH      | SIR1CR  |

[15] SBI

| Address | Name         |
|---------|--------------|
| 1240H   | SBICR1       |
| 1H      | SBIDBR       |
| 2H      | I2CAR        |
| 3H      | SBICR2/SBISR |
| 4H      | SBIBR0       |
| 5H      |              |
| 6H      |              |
| 7H      | SBICR0       |
| 8H      |              |
| 9H      |              |
| AH      |              |
| BH      |              |
| CH      |              |
| DH      |              |
| EH      |              |
| FH      |              |

Note: Do not access no allocated name address.

[16] 10-bit ADC

| Address | Name     |
|---------|----------|
| 12A0H   | ADREG0L  |
| 1H      | ADREG0H  |
| 2H      | ADREG1L  |
| 3H      | ADREG1H  |
| 4H      | ADREG2L  |
| 5H      | ADREG2H  |
| 6H      | ADREG3L  |
| 7H      | ADREG3H  |
| 8H      | ADREG4L  |
| 9H      | ADREG4H  |
| AH      | ADREG5L  |
| BH      | ADREG5H  |
| CH      | Reserved |
| DH      | Reserved |
| EH      | Reserved |
| FH      | Reserved |

[17] WDT

| Address | Name      |
|---------|-----------|
| 12B0H   | ADREGSPL  |
| 1H      | ADREGSPH  |
| 2H      | Reserved  |
| 3H      | Reserved  |
| 4H      | ADCM0REGL |
| 5H      | ADCM0REGH |
| 6H      | ADCM1REGL |
| 7H      | ADCM1REGH |
| 8H      | ADMOD0    |
| 9H      | ADMOD1    |
| AH      | ADMOD2    |
| BH      | ADMOD3    |
| CH      | ADMOD4    |
| DH      | ADMOD5    |
| EH      |           |
| FH      | ADCCLK    |

| Address | Name  |
|---------|-------|
| 1300H   | WDMOD |
| 1H      | WDCR  |
| 2H      |       |
| 3H      |       |
| 4H      |       |
| 5H      |       |
| 6H      |       |
| 7H      |       |
| 8H      |       |
| 9H      |       |
| AH      |       |
| BH      |       |
| CH      |       |
| DH      |       |
| EH      |       |
| FH      |       |

[18] RTC

| Address | Name   |
|---------|--------|
| 1320H   | SECR   |
| 1H      | MINR   |
| 2H      | HOURR  |
| 3H      | DAYR   |
| 4H      | DATER  |
| 5H      | MONTHR |
| 6H      | YEARR  |
| 7H      | PAGER  |
| 8H      | RESTR  |
| 9H      |        |
| AH      |        |
| BH      |        |
| CH      |        |
| DH      |        |
| EH      |        |
| FH      |        |

[19] MLD

| Address | Name    |
|---------|---------|
| 1330H   | ALM     |
| 1H      | MELALMC |
| 2H      | MELFL   |
| 3H      | MELFH   |
| 4H      | ALMINT  |
| 5H      |         |
| 6H      |         |
| 7H      |         |
| 8H      |         |
| 9H      |         |
| AH      |         |
| BH      |         |
| CH      |         |
| DH      |         |
| EH      |         |
| FH      |         |

Note: Do not access no allocated name address.

[20] I<sup>2</sup>S

| Address | Name    |
|---------|---------|
| 1800H   | I2S0BUF |
| 1H      |         |
| 2H      |         |
| 3H      |         |
| 4H      |         |
| 5H      |         |
| 6H      |         |
| 7H      |         |
| 8H      | I2S0CTL |
| 9H      | I2S0CTL |
| AH      | I2S0C   |
| BH      | I2S0C   |
| CH      |         |
| DH      |         |
| EH      |         |
| FH      |         |

| Address | Name     |
|---------|----------|
| 1810H   | Reserved |
| 1H      |          |
| 2H      |          |
| 3H      |          |
| 4H      |          |
| 5H      |          |
| 6H      |          |
| 7H      |          |
| 8H      | Reserved |
| 9H      | Reserved |
| AH      | Reserved |
| BH      | Reserved |
| CH      |          |
| DH      |          |
| EH      |          |
| FH      |          |

[21] MAC

| Address | Name   |
|---------|--------|
| 1BE0H   | MACMA  |
| 1H      | MACMA  |
| 2H      | MACMA  |
| 3H      | MACMA  |
| 4H      | MACMB  |
| 5H      | MACMB  |
| 6H      | MACMB  |
| 7H      | MACMB  |
| 8H      | MACORL |
| 9H      | MACORL |
| AH      | MACORL |
| BH      | MACORL |
| CH      | MACORH |
| DH      | MACORH |
| EH      | MACORH |
| FH      | MACORH |

| Address | Name  |
|---------|-------|
| 1BF0H   |       |
| 1H      |       |
| 2H      |       |
| 3H      |       |
| 4H      |       |
| 5H      |       |
| 6H      |       |
| 7H      |       |
| 8H      |       |
| 9H      |       |
| AH      |       |
| BH      |       |
| CH      | MACCR |
| DH      |       |
| EH      |       |
| FH      |       |

Note: Do not access no allocated name address.



## (1) I/O ports (1/10)

| Symbol | Name  | Address | 7                                                                 | 6                                                             | 5                       | 4                                                                 | 3   | 2                                                             | 1   | 0   |  |
|--------|-------|---------|-------------------------------------------------------------------|---------------------------------------------------------------|-------------------------|-------------------------------------------------------------------|-----|---------------------------------------------------------------|-----|-----|--|
| P1     | PORT1 | 0004H   | P17                                                               | P16                                                           | P15                     | P14                                                               | P13 | P12                                                           | P11 | P10 |  |
|        |       |         | R/W                                                               |                                                               |                         |                                                                   |     |                                                               |     |     |  |
|        |       |         | Data from external port (Output latch register is cleared to “0”) |                                                               |                         |                                                                   |     |                                                               |     |     |  |
| P4     | PORT4 | 0010H   | P47                                                               | P46                                                           | P45                     | P44                                                               | P43 | P42                                                           | P41 | P40 |  |
|        |       |         | R/W                                                               |                                                               |                         |                                                                   |     |                                                               |     |     |  |
|        |       |         | 0                                                                 | 0                                                             | 0                       | 0                                                                 | 0   | 0                                                             | 0   | 0   |  |
| P5     | PORT5 | 0014H   | P57                                                               | P56                                                           | P55                     | P54                                                               | P53 | P52                                                           | P51 | P50 |  |
|        |       |         | R/W                                                               |                                                               |                         |                                                                   |     |                                                               |     |     |  |
|        |       |         | 0                                                                 | 0                                                             | 0                       | 0                                                                 | 0   | 0                                                             | 0   | 0   |  |
| P6     | PORT6 | 0018H   | P67                                                               | P66                                                           | P65                     | P64                                                               | P63 | P62                                                           | P61 | P60 |  |
|        |       |         | R/W                                                               |                                                               |                         |                                                                   |     |                                                               |     |     |  |
|        |       |         | Data from external port (Output latch register is cleared to “0”) |                                                               |                         |                                                                   |     |                                                               |     |     |  |
| P7     | PORT7 | 001CH   |                                                                   | P76                                                           | P75                     | P74                                                               | P73 | P72                                                           | P71 | P70 |  |
|        |       |         |                                                                   | R/W                                                           |                         |                                                                   |     |                                                               |     |     |  |
|        |       |         |                                                                   | Data from external port (Output latch register is set to “1”) |                         | Data from external port (Output latch register is cleared to “0”) |     | Data from external port (Output latch register is set to “1”) |     | 1   |  |
| P8     | PORT8 | 0020H   | P87                                                               | P86                                                           |                         |                                                                   | P83 | P82                                                           | P81 | P80 |  |
|        |       |         | R/W                                                               |                                                               |                         |                                                                   | R/W |                                                               |     |     |  |
|        |       |         | 1                                                                 | 1                                                             |                         |                                                                   | 1   | 0 (Note)                                                      | 1   | 1   |  |
| P9     | PORT9 | 0024H   | P97                                                               | P96                                                           |                         |                                                                   |     | P92                                                           | P91 | P90 |  |
|        |       |         | R                                                                 |                                                               |                         |                                                                   |     | R/W                                                           |     |     |  |
|        |       |         | Data from external port                                           |                                                               |                         |                                                                   |     | Data from external port (Output latch register is set to “1”) |     |     |  |
| PA     | PORTA | 0028H   | PA7                                                               | PA6                                                           | PA5                     | PA4                                                               | PA3 | PA2                                                           | PA1 | PA0 |  |
|        |       |         | R                                                                 |                                                               |                         |                                                                   |     |                                                               |     |     |  |
|        |       |         | Data from external port                                           |                                                               |                         |                                                                   |     |                                                               |     |     |  |
| PC     | PORTC | 0030H   | PC7                                                               | PC6                                                           | PC5                     | PC4                                                               | PC3 | PC2                                                           | PC1 | PC0 |  |
|        |       |         | R/W                                                               |                                                               |                         |                                                                   |     |                                                               |     |     |  |
|        |       |         | Data from external port (Output latch register is set to “1”)     |                                                               |                         |                                                                   |     |                                                               |     |     |  |
| PF     | PORTF | 003CH   | PF7                                                               |                                                               |                         |                                                                   |     | PF2                                                           | PF1 | PF0 |  |
|        |       |         | R/W                                                               |                                                               |                         |                                                                   |     | R/W                                                           |     |     |  |
|        |       |         | 1                                                                 |                                                               |                         |                                                                   |     | Data from external port (Output latch register is set to “1”) |     |     |  |
| PG     | PORTG | 0040H   |                                                                   |                                                               | PG5                     | PG4                                                               | PG3 | PG2                                                           | PG1 | PG0 |  |
|        |       |         |                                                                   |                                                               | R                       |                                                                   |     |                                                               |     |     |  |
|        |       |         |                                                                   |                                                               | Data from external port |                                                                   |     |                                                               |     |     |  |
| PJ     | PORTJ | 004CH   | PJ7                                                               | PJ6                                                           | PJ5                     | PJ4                                                               | PJ3 | PJ2                                                           | PJ1 | PJ0 |  |
|        |       |         | R/W                                                               |                                                               |                         |                                                                   |     |                                                               |     |     |  |
|        |       |         | 1                                                                 | Data from external port (Output latch register is set to “1”) |                         | 1                                                                 | 1   | 1                                                             | 1   | 1   |  |
| PK     | PORTK | 0050H   | PK7                                                               | PK6                                                           | PK5                     | PK4                                                               | PK3 | PK2                                                           | PK1 | PK0 |  |
|        |       |         | R/W                                                               |                                                               |                         |                                                                   |     |                                                               |     |     |  |
|        |       |         | 0                                                                 | 0                                                             | 0                       | 0                                                                 | 0   | 0                                                             | 0   | 0   |  |
| PL     | PORTL | 0054H   | PL7                                                               | PL6                                                           | PL5                     | PL4                                                               | PL3 | PL2                                                           | PL1 | PL0 |  |
|        |       |         | R/W                                                               |                                                               |                         |                                                                   |     |                                                               |     |     |  |
|        |       |         | 0                                                                 | 0                                                             | 0                       | 0                                                                 | 0   | 0                                                             | 0   | 0   |  |

## (1) I/O ports (2/10)

| Symbol | Name  | Address | 7                                                                    | 6   | 5                                                                    | 4   | 3                                                                    | 2   | 1   | 0   |
|--------|-------|---------|----------------------------------------------------------------------|-----|----------------------------------------------------------------------|-----|----------------------------------------------------------------------|-----|-----|-----|
| PM     | PORTM | 0058H   | PM7                                                                  |     |                                                                      |     |                                                                      | PM2 | PM1 |     |
|        |       |         | R/W                                                                  |     |                                                                      |     |                                                                      | R/W |     |     |
|        |       |         | 1                                                                    |     |                                                                      |     |                                                                      | 1   | 1   |     |
| PN     | PORTN | 005CH   | PN7                                                                  | PN6 | PN5                                                                  | PN4 | PN3                                                                  | PN2 | PN1 | PN0 |
|        |       |         | R/W                                                                  |     |                                                                      |     |                                                                      |     |     |     |
|        |       |         | Data from external port (Output latch register is cleared to "1")    |     |                                                                      |     |                                                                      |     |     |     |
| PP     | PORTP | 0060H   |                                                                      | PP6 | PP5                                                                  | PP4 | PP3                                                                  |     |     |     |
|        |       |         |                                                                      | R/W |                                                                      |     |                                                                      |     |     |     |
|        |       |         |                                                                      | 0   | Data from external port<br>(Output latch register is cleared to "0") |     |                                                                      |     |     |     |
| PR     | PORTR | 0064H   |                                                                      |     |                                                                      |     | PR3                                                                  | PR2 | PR1 | PR0 |
|        |       |         |                                                                      |     |                                                                      |     | R/W                                                                  |     |     |     |
|        |       |         |                                                                      |     |                                                                      |     | Data from external port<br>(Output latch register is cleared to "0") |     |     |     |
| PT     | PORTT | 00A0H   | PT7                                                                  | PT6 | PT5                                                                  | PT4 | PT3                                                                  | PT2 | PT1 | PT0 |
|        |       |         | R/W                                                                  |     |                                                                      |     |                                                                      |     |     |     |
|        |       |         | Data from external port (Output latch register is cleared to "0")    |     |                                                                      |     |                                                                      |     |     |     |
| PV     | PORTV | 00A8H   | PV7                                                                  | PV6 |                                                                      |     |                                                                      |     |     |     |
|        |       |         | R/W                                                                  |     |                                                                      |     |                                                                      |     |     |     |
|        |       |         | Data from external port<br>(Output latch register is cleared to "0") |     |                                                                      |     |                                                                      |     |     |     |
| PX     | PORTX | 00B0H   |                                                                      |     | PX5                                                                  | PX4 |                                                                      |     |     |     |
|        |       |         |                                                                      |     | R/W                                                                  |     |                                                                      |     |     |     |
|        |       |         |                                                                      |     | Data from external port<br>(Output latch register is cleared to "0") |     |                                                                      |     |     |     |

## (1) I/O ports (3/10)

| Symbol | Name                    | Address                 | 7                                | 6                                                            | 5                                                                                           | 4                                        | 3                                        | 2                                                                                                                                                    | 1                                                                                                                                                    | 0                                  |
|--------|-------------------------|-------------------------|----------------------------------|--------------------------------------------------------------|---------------------------------------------------------------------------------------------|------------------------------------------|------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------|
| P1CR   | PORT1 control register  | 0006H<br>(Prohibit RMW) | P17C                             | P16C                                                         | P15C                                                                                        | P14C                                     | P13C                                     | P12C                                                                                                                                                 | P11C                                                                                                                                                 | P10C                               |
|        |                         |                         | W                                |                                                              |                                                                                             |                                          |                                          |                                                                                                                                                      |                                                                                                                                                      |                                    |
|        |                         |                         | 0                                | 0                                                            | 0                                                                                           | 0                                        | 0                                        | 0                                                                                                                                                    | 0                                                                                                                                                    | 0                                  |
|        |                         |                         | 0: Input 1: Output               |                                                              |                                                                                             |                                          |                                          |                                                                                                                                                      |                                                                                                                                                      |                                    |
| P1FC   | PORT1 function register | 0007H<br>(Prohibit RMW) |                                  |                                                              |                                                                                             |                                          |                                          |                                                                                                                                                      |                                                                                                                                                      | P1F                                |
|        |                         |                         |                                  |                                                              |                                                                                             |                                          |                                          |                                                                                                                                                      |                                                                                                                                                      | W                                  |
|        |                         |                         |                                  |                                                              |                                                                                             |                                          |                                          |                                                                                                                                                      |                                                                                                                                                      | 0/1                                |
|        |                         |                         |                                  |                                                              |                                                                                             |                                          |                                          |                                                                                                                                                      |                                                                                                                                                      | 0: Port<br>1: Data bus<br>(D8~D15) |
| P4FC   | PORT4 function register | 0013H<br>(Prohibit RMW) | P47F                             | P46F                                                         | P45F                                                                                        | P44F                                     | P43F                                     | P42F                                                                                                                                                 | P41F                                                                                                                                                 | P40F                               |
|        |                         |                         | W                                |                                                              |                                                                                             |                                          |                                          |                                                                                                                                                      |                                                                                                                                                      |                                    |
|        |                         |                         | 1                                | 1                                                            | 1                                                                                           | 1                                        | 1                                        | 1                                                                                                                                                    | 1                                                                                                                                                    | 1                                  |
|        |                         |                         | 0: Port 1: Address bus (A0~A7)   |                                                              |                                                                                             |                                          |                                          |                                                                                                                                                      |                                                                                                                                                      |                                    |
| P5FC   | PORT5 function register | 0017H<br>(Prohibit RMW) | P57F                             | P56F                                                         | P55F                                                                                        | P54F                                     | P53F                                     | P52F                                                                                                                                                 | P51F                                                                                                                                                 | P50F                               |
|        |                         |                         | W                                |                                                              |                                                                                             |                                          |                                          |                                                                                                                                                      |                                                                                                                                                      |                                    |
|        |                         |                         | 1                                | 1                                                            | 1                                                                                           | 1                                        | 1                                        | 1                                                                                                                                                    | 1                                                                                                                                                    | 1                                  |
|        |                         |                         | 0: Port 1: Address bus (A8~A15)  |                                                              |                                                                                             |                                          |                                          |                                                                                                                                                      |                                                                                                                                                      |                                    |
| P6CR   | PORT6 control register  | 001AH<br>(Prohibit RMW) | P67C                             | P66C                                                         | P65C                                                                                        | P64C                                     | P63C                                     | P62C                                                                                                                                                 | P61C                                                                                                                                                 | P60C                               |
|        |                         |                         | W                                |                                                              |                                                                                             |                                          |                                          |                                                                                                                                                      |                                                                                                                                                      |                                    |
|        |                         |                         | 0                                | 0                                                            | 0                                                                                           | 0                                        | 0                                        | 0                                                                                                                                                    | 0                                                                                                                                                    | 0                                  |
|        |                         |                         | 0: Input 1: Output               |                                                              |                                                                                             |                                          |                                          |                                                                                                                                                      |                                                                                                                                                      |                                    |
| P6FC   | PORT6 function register | 001BH<br>(Prohibit RMW) | P67F                             | P66F                                                         | P65F                                                                                        | P64F                                     | P63F                                     | P62F                                                                                                                                                 | P61F                                                                                                                                                 | P60F                               |
|        |                         |                         | W                                |                                                              |                                                                                             |                                          |                                          |                                                                                                                                                      |                                                                                                                                                      |                                    |
|        |                         |                         | 1                                | 1                                                            | 1                                                                                           | 1                                        | 1                                        | 1                                                                                                                                                    | 1                                                                                                                                                    | 1                                  |
|        |                         |                         | 0: Port 1: Address bus (A16~A23) |                                                              |                                                                                             |                                          |                                          |                                                                                                                                                      |                                                                                                                                                      |                                    |
| P7CR   | PORT7 control register  | 001EH<br>(Prohibit RMW) |                                  | P76C                                                         | P75C                                                                                        | P74C                                     | P73C                                     | P72C                                                                                                                                                 | P71C                                                                                                                                                 |                                    |
|        |                         |                         |                                  | W                                                            |                                                                                             |                                          |                                          |                                                                                                                                                      |                                                                                                                                                      |                                    |
|        |                         |                         |                                  | 0                                                            | 0                                                                                           | 0                                        | 0                                        | 0                                                                                                                                                    | 0                                                                                                                                                    |                                    |
|        |                         |                         |                                  | 0: Input port,<br>$\overline{\text{WAIT}}$<br>1: Output port | 0: Input port,<br>NDR/ $\overline{\text{B}}$<br>1: Output port,<br>R/ $\overline{\text{W}}$ | 0: Input port<br>1: Output port,<br>EA25 | 0: Input port<br>1: Output port,<br>EA24 | 0: Input port<br>1: Output port,<br>NDWE at<br>$\langle \text{P72} \rangle = 0$ ,<br>$\overline{\text{WRLU}}$ at<br>$\langle \text{P72} \rangle = 1$ | 0: Input port<br>1: Output port,<br>NDRE at<br>$\langle \text{P71} \rangle = 0$ ,<br>$\overline{\text{WRLU}}$ at<br>$\langle \text{P71} \rangle = 1$ |                                    |
| P7FC   | PORT7 function register | 001FH<br>(Prohibit RMW) |                                  | P76F                                                         | P75F                                                                                        | P74F                                     | P73F                                     | P72F                                                                                                                                                 | P71F                                                                                                                                                 | P70F                               |
|        |                         |                         |                                  | W                                                            |                                                                                             |                                          |                                          |                                                                                                                                                      |                                                                                                                                                      |                                    |
|        |                         |                         |                                  | 0                                                            | 0                                                                                           | 0                                        | 0                                        | 0                                                                                                                                                    | 0                                                                                                                                                    | 0                                  |
|        |                         |                         |                                  | 0: Port<br>1: $\overline{\text{WAIT}}$                       | 0: Port<br>1: NDR/ $\overline{\text{B}}$ ,<br>R/ $\overline{\text{W}}$                      | 0: Port<br>1: EA25                       | 0: Port<br>1: EA24                       | 0: Port<br>1: NDWE at<br>$\langle \text{P72} \rangle = 0$ ,<br>$\overline{\text{WRLU}}$ at<br>$\langle \text{P72} \rangle = 1$                       | 0: Port<br>1: NDRE at<br>$\langle \text{P71} \rangle = 0$ ,<br>$\overline{\text{WRLU}}$ at<br>$\langle \text{P71} \rangle = 1$                       | 0: Port<br>1: RD                   |

## (1) I/O ports (4/10)

| Symbol | Name                           | Address                    | 7                                                           | 6                                                           | 5                                                                                                                                                                                  | 4                                            | 3                                                                                     | 2                                                                                                                                    | 1                                                                     | 0                                                                     |
|--------|--------------------------------|----------------------------|-------------------------------------------------------------|-------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------|---------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------|-----------------------------------------------------------------------|
| P8FC   | PORT8<br>function<br>register  | 0023H<br>(Prohibit<br>RMW) | P87F                                                        | P86F                                                        |                                                                                                                                                                                    |                                              | P83F                                                                                  | P82F                                                                                                                                 | P81F                                                                  | P80F                                                                  |
|        |                                |                            | W                                                           |                                                             |                                                                                                                                                                                    |                                              | W                                                                                     |                                                                                                                                      |                                                                       |                                                                       |
|        |                                |                            | 0                                                           | 0                                                           |                                                                                                                                                                                    |                                              | 0                                                                                     | 0                                                                                                                                    | 0                                                                     | 0                                                                     |
|        |                                |                            | 0: Port<br>1: <P87F2>                                       | 0: Port<br>1: <P86F2>                                       |                                                                                                                                                                                    |                                              | 0: Port<br>1: $\overline{\text{CS3}}$ ,<br>$\overline{\text{CSXA}}$                   | 0: Port,<br>$\overline{\text{CSZA}}$ ,<br>1: $\overline{\text{CS2}}$ ,<br>$\overline{\text{SDCS}}$                                   | 0: Port<br>1: $\overline{\text{CS1}}$                                 | 0: Port<br>1: $\overline{\text{CS0}}$                                 |
| P8FC2  | PORT8<br>function<br>register2 | 0021H<br>(Prohibit<br>RMW) | P87F2                                                       | P86F2                                                       |                                                                                                                                                                                    |                                              | P83F2                                                                                 | P82F2                                                                                                                                | P81F2                                                                 |                                                                       |
|        |                                |                            | W                                                           |                                                             |                                                                                                                                                                                    |                                              | W                                                                                     |                                                                                                                                      |                                                                       |                                                                       |
|        |                                |                            | 0                                                           | 0                                                           |                                                                                                                                                                                    |                                              | 0                                                                                     | 0                                                                                                                                    | 0                                                                     |                                                                       |
|        |                                |                            | 0: $\overline{\text{CSXB}}$<br>1: $\overline{\text{ND1CE}}$ | 0: $\overline{\text{CSZD}}$<br>1: $\overline{\text{ND0CE}}$ |                                                                                                                                                                                    |                                              | 0: Port,<br>$\overline{\text{CS3}}$<br>1: $\overline{\text{CSXA}}$                    | 0: Output<br>port,<br>$\overline{\text{CS2}}$<br>1: $\overline{\text{CSZA}}$ ,<br>$\overline{\text{SDCS}}$                           | 0: <P81F><br>1: $\overline{\text{SDCS}}$                              |                                                                       |
| P9CR   | PORT9<br>control<br>register   | 0026H<br>(Prohibit<br>RMW) |                                                             |                                                             |                                                                                                                                                                                    |                                              |                                                                                       | P92C                                                                                                                                 | P91C                                                                  | P90C                                                                  |
|        |                                |                            |                                                             |                                                             |                                                                                                                                                                                    |                                              |                                                                                       | W                                                                                                                                    |                                                                       |                                                                       |
|        |                                |                            |                                                             |                                                             |                                                                                                                                                                                    |                                              |                                                                                       | 0                                                                                                                                    | 0                                                                     | 0                                                                     |
|        |                                |                            |                                                             |                                                             |                                                                                                                                                                                    |                                              |                                                                                       | 0 Input<br>port,<br>$\overline{\text{CTS0/1}}$ ,<br>$\overline{\text{SCLK0/1}}$<br>1: Output<br>port,<br>$\overline{\text{SCLK0/1}}$ | 0: Input<br>port,<br>$\overline{\text{RXD0/1}}$<br>1: Output<br>port, | 0: Input<br>port,<br>1: Output<br>port,<br>$\overline{\text{TXD0/1}}$ |
| P9FC   | PORT9<br>function<br>register  | 0027H<br>(Prohibit<br>RMW) |                                                             | P96F                                                        |                                                                                                                                                                                    |                                              |                                                                                       | P92F                                                                                                                                 |                                                                       | P90F                                                                  |
|        |                                |                            |                                                             | W                                                           |                                                                                                                                                                                    |                                              |                                                                                       | W                                                                                                                                    |                                                                       | W                                                                     |
|        |                                |                            |                                                             | 0                                                           |                                                                                                                                                                                    |                                              |                                                                                       | 0                                                                                                                                    |                                                                       | 0                                                                     |
|        |                                |                            |                                                             | 0: Input<br>port,<br>1: $\overline{\text{INT4}}$            |                                                                                                                                                                                    |                                              |                                                                                       | 0: Port,<br>$\overline{\text{CTS0/1}}$<br>1: $\overline{\text{SCLK0}}$                                                               |                                                                       | 0: Port<br>1: $\overline{\text{TXD0/1}}$                              |
| P9FC2  | PORT9<br>function<br>register2 | 0025H<br>(Prohibit<br>RMW) | -                                                           |                                                             | P95F2                                                                                                                                                                              | P94F2                                        | P93F2                                                                                 | -                                                                                                                                    |                                                                       | P90FC2                                                                |
|        |                                |                            | W                                                           |                                                             | W                                                                                                                                                                                  |                                              |                                                                                       | W                                                                                                                                    |                                                                       | W                                                                     |
|        |                                |                            | 0                                                           |                                                             | 0                                                                                                                                                                                  | 0                                            | 0                                                                                     | 0                                                                                                                                    |                                                                       | 0                                                                     |
|        |                                |                            | Always<br>write "0"                                         |                                                             | P92<br>SCLK<br>selection<br>0: $\overline{\text{SCLK0}}$<br>1: $\overline{\text{SCLK1}}$<br><br>SIO0<br>SCLK,<br>$\overline{\text{CTS}}$<br>input<br>selection<br>0: P92<br>1: PP5 | SIO0<br>RXD<br>selection<br>0: P91<br>1: PP4 | P90<br>TXD<br>selection<br>0: $\overline{\text{TXD0}}$<br>1: $\overline{\text{TXD1}}$ | Always<br>write "0"                                                                                                                  |                                                                       | 0: CMOS<br>1: Open<br>-Drain                                          |
| PAFC   | PORTA<br>function<br>register  | 002BH<br>(Prohibit<br>RMW) | PA7F                                                        | PA6F                                                        | PA5F                                                                                                                                                                               | PA4F                                         | PA3F                                                                                  | PA2F                                                                                                                                 | PA1F                                                                  | PA0F                                                                  |
|        |                                |                            | W                                                           |                                                             |                                                                                                                                                                                    |                                              |                                                                                       |                                                                                                                                      |                                                                       |                                                                       |
|        |                                |                            | 0                                                           | 0                                                           | 0                                                                                                                                                                                  | 0                                            | 0                                                                                     | 0                                                                                                                                    | 0                                                                     | 0                                                                     |
|        |                                |                            | 0: Key-in disable                                           |                                                             |                                                                                                                                                                                    |                                              | 1: Key-in enable                                                                      |                                                                                                                                      |                                                                       |                                                                       |

## (1) I/O ports (5/10)

| Symbol | Name                      | Address              | 7                                                            | 6                                                                | 5                                                                | 4                                                       | 3                                                     | 2                                         | 1                                                  | 0                                         |
|--------|---------------------------|----------------------|--------------------------------------------------------------|------------------------------------------------------------------|------------------------------------------------------------------|---------------------------------------------------------|-------------------------------------------------------|-------------------------------------------|----------------------------------------------------|-------------------------------------------|
| PCCR   | PORTC control register    | 0032H (Prohibit RMW) | PC7C                                                         | PC6C                                                             | PC5C                                                             | PC4C                                                    | PC3C                                                  | PC2C                                      | PC1C                                               | PC0C                                      |
|        |                           |                      | W                                                            |                                                                  |                                                                  |                                                         |                                                       |                                           |                                                    |                                           |
|        |                           |                      | 0                                                            | 0                                                                | 0                                                                | 0                                                       | 0                                                     | 0                                         | 0                                                  | 0                                         |
|        |                           |                      | 0: Input port,<br>1: Output port,<br>KO output (Open -drain) | 0: Input port,<br>EA28<br>1: Output port,<br>SPCLK output        | 0: Input port,<br>EA27<br>1: Output port,<br>SPDO output         | 0: Input port,<br>EA26<br>1: Output port,<br>SPDI input | 0: Input port,<br>INT3<br>1: Output port,<br>TA2IN    | 0: Input port,<br>INT2<br>1: Output port, | 0: Input port,<br>INT1<br>1: Output port,<br>TA0IN | 0: Input port,<br>INT0<br>1: Output port, |
| PCFC   | PORTC function register   | 0033H (Prohibit RMW) | PC7F                                                         | PC6F                                                             | PC5F                                                             | PC4F                                                    | PC3F                                                  | PC2F                                      | PC1F                                               | PC0F                                      |
|        |                           |                      | W                                                            |                                                                  |                                                                  |                                                         |                                                       |                                           |                                                    |                                           |
|        |                           |                      | 0                                                            | 0                                                                | 0                                                                | 0                                                       | 0                                                     | 0                                         | 0                                                  | 0                                         |
|        |                           |                      | 0: Port<br>1: KO output (Open -Drain)                        | 0: Port<br>1: EA28, SPCLK output                                 | 0: Port<br>1: EA27, SPDO output                                  | 0: Port<br>1: EA26, SPDI input                          | 0: Port<br>1: INT3, TA2IN                             | 0: Port<br>1: INT2                        | 0: Port<br>1: INT1, TA0IN                          | 0: Port<br>1: INT0                        |
| PCFC2  | PORTC function 2 register | 0031H (Prohibit RMW) |                                                              |                                                                  |                                                                  | PC4F2                                                   |                                                       |                                           |                                                    |                                           |
|        |                           |                      |                                                              |                                                                  |                                                                  | W                                                       |                                                       |                                           |                                                    |                                           |
|        |                           |                      |                                                              |                                                                  |                                                                  | 0                                                       |                                                       |                                           |                                                    |                                           |
|        |                           |                      |                                                              |                                                                  |                                                                  | SPDI selection<br>0: PR0<br>1: PC4                      |                                                       |                                           |                                                    |                                           |
| PFCR   | PORTF control register    | 003EH (Prohibit RMW) |                                                              |                                                                  |                                                                  |                                                         |                                                       | PF2C                                      | PF1C                                               | PF0C                                      |
|        |                           |                      |                                                              |                                                                  |                                                                  |                                                         |                                                       | W                                         |                                                    |                                           |
|        |                           |                      |                                                              |                                                                  |                                                                  |                                                         |                                                       | 0                                         | 0                                                  | 0                                         |
|        |                           |                      |                                                              |                                                                  |                                                                  |                                                         |                                                       | 0: Input, 1: Output                       |                                                    |                                           |
| PFFC   | PORTF function register   | 003FH (Prohibit RMW) | PF7F                                                         |                                                                  |                                                                  |                                                         |                                                       | PF2F                                      | PF1F                                               | PF0F                                      |
|        |                           |                      | W                                                            |                                                                  |                                                                  |                                                         |                                                       | W                                         |                                                    |                                           |
|        |                           |                      | 1                                                            |                                                                  |                                                                  |                                                         |                                                       | 0                                         | 0                                                  | 0                                         |
|        |                           |                      | 0: Output port,<br>1: SDCLK                                  |                                                                  |                                                                  |                                                         |                                                       | 0: Port<br>1: I2S0WS                      | 0: Port<br>1: I2S0DO                               | 0: Port<br>1: I2S1CKO                     |
| PGFC   | PORTG function register   | 0043H (Prohibit RMW) |                                                              |                                                                  |                                                                  |                                                         | PG3F                                                  |                                           |                                                    |                                           |
|        |                           |                      |                                                              |                                                                  |                                                                  |                                                         | W                                                     |                                           |                                                    |                                           |
|        |                           |                      |                                                              |                                                                  |                                                                  |                                                         | 0                                                     |                                           |                                                    |                                           |
|        |                           |                      |                                                              |                                                                  |                                                                  |                                                         | -                                                     |                                           |                                                    |                                           |
| PJCR   | PORTJ control register    | 004EH (Prohibit RMW) |                                                              |                                                                  |                                                                  |                                                         | 0: Input port,<br>AN3<br>1: $\overline{\text{ADTRG}}$ |                                           |                                                    |                                           |
|        |                           |                      |                                                              |                                                                  |                                                                  |                                                         |                                                       |                                           |                                                    |                                           |
|        |                           |                      |                                                              |                                                                  |                                                                  |                                                         |                                                       |                                           |                                                    |                                           |
|        |                           |                      |                                                              |                                                                  |                                                                  |                                                         |                                                       |                                           |                                                    |                                           |
|        |                           |                      |                                                              | PJ6C                                                             | PJ5C                                                             |                                                         |                                                       |                                           |                                                    |                                           |
|        |                           |                      |                                                              | W                                                                |                                                                  |                                                         |                                                       |                                           |                                                    |                                           |
|        |                           |                      |                                                              | 0                                                                | 0                                                                |                                                         |                                                       |                                           |                                                    |                                           |
|        |                           |                      |                                                              | -                                                                | -                                                                |                                                         |                                                       |                                           |                                                    |                                           |
|        |                           |                      |                                                              | 0: Input port<br>SRUUB output<br>1: output port,<br>NDCLE output | 0: Input port<br>SRULB output<br>1: output port,<br>NDALE output |                                                         |                                                       |                                           |                                                    |                                           |

## (1) I/O ports (6/10)

| Symbol | Name                          | Address                    | 7                                   | 6                                                            | 5                                                            | 4                                         | 3                                         | 2                                                                    | 1                                                                      | 0                                                                      |
|--------|-------------------------------|----------------------------|-------------------------------------|--------------------------------------------------------------|--------------------------------------------------------------|-------------------------------------------|-------------------------------------------|----------------------------------------------------------------------|------------------------------------------------------------------------|------------------------------------------------------------------------|
| PJFC   | PORTJ<br>function<br>register | 004FH<br>(Prohibit<br>RMW) | PJ7F                                | PJ6F                                                         | PJ5F                                                         | PJ4F                                      | PJ3F                                      | PJ2F                                                                 | PJ1F                                                                   | PJ0F                                                                   |
|        |                               |                            | W                                   |                                                              |                                                              |                                           |                                           |                                                                      |                                                                        |                                                                        |
|        |                               |                            | 0                                   | 0                                                            | 0                                                            | 0                                         | 0                                         | 0                                                                    | 0                                                                      | 0                                                                      |
|        |                               |                            | 0: Port<br>1: SDCKE                 | 0: Port<br>1: $\overline{\text{SRUUB}}$ ,<br>NDCLE<br>output | 0: Port<br>1: $\overline{\text{SRULB}}$ ,<br>NDALE<br>output | 0: Port<br>1: $\overline{\text{SDLUDQM}}$ | 0: Port<br>1: $\overline{\text{SDLLDQM}}$ | 0: Port<br>1: $\overline{\text{SDWE}}$ ,<br>$\overline{\text{SRWR}}$ | 0: Port<br>1: $\overline{\text{SDCAS}}$ ,<br>$\overline{\text{SRLUB}}$ | 0: Port<br>1: $\overline{\text{SDRAS}}$ ,<br>$\overline{\text{SRLLB}}$ |
| PKFC   | PORTK<br>function<br>register | 0053H<br>(Prohibit<br>RMW) | PK7F                                | PK6F                                                         | PK5F                                                         | PK4F                                      | PK3F                                      | PK2F                                                                 | PK1F                                                                   | PK0F                                                                   |
|        |                               |                            | W                                   |                                                              |                                                              |                                           |                                           |                                                                      |                                                                        |                                                                        |
|        |                               |                            | 0                                   | 0                                                            | 0                                                            | 0                                         | 0                                         | 0                                                                    | 0                                                                      | 0                                                                      |
|        |                               |                            | 0: Port 1: Don't setting            |                                                              |                                                              |                                           |                                           |                                                                      |                                                                        |                                                                        |
| PLCR   | PORTL<br>control<br>register  | 0056H<br>(Prohibit<br>RMW) | PL7C                                | PL6FC                                                        | PL5C                                                         | PL4C                                      | PL3C                                      | PL2C                                                                 | PL1C                                                                   | PL0C                                                                   |
|        |                               |                            | W                                   |                                                              |                                                              |                                           |                                           |                                                                      |                                                                        |                                                                        |
|        |                               |                            | 0                                   | 0                                                            | 0                                                            | 0                                         | 0                                         | 0                                                                    | 0                                                                      | 0                                                                      |
|        |                               |                            | 0: Input 1: Output                  |                                                              |                                                              |                                           |                                           |                                                                      |                                                                        |                                                                        |
| PLFC   | PORTL<br>function<br>register | 0057H<br>(Prohibit<br>RMW) | PL7F                                | PL6F                                                         | PL5F                                                         | PL4F                                      | PL3F                                      | PL2F                                                                 | PL1F                                                                   | PL0F                                                                   |
|        |                               |                            | W                                   |                                                              |                                                              |                                           |                                           |                                                                      |                                                                        |                                                                        |
|        |                               |                            | 0                                   | 0                                                            | 0                                                            | 0                                         | 0                                         | 0                                                                    | 0                                                                      | 0                                                                      |
|        |                               |                            | 0: Port 1: Don't setting            |                                                              |                                                              |                                           |                                           |                                                                      |                                                                        |                                                                        |
| PLFC2  | PORTL<br>register 2           | 0055H<br>(Prohibit<br>RMW) |                                     |                                                              |                                                              |                                           |                                           |                                                                      |                                                                        | PL0F2                                                                  |
|        |                               |                            |                                     |                                                              |                                                              |                                           |                                           |                                                                      |                                                                        | W                                                                      |
|        |                               |                            |                                     |                                                              |                                                              |                                           |                                           |                                                                      |                                                                        | 0/1                                                                    |
|        |                               |                            |                                     |                                                              |                                                              |                                           |                                           |                                                                      |                                                                        | 0: Port<br>1: Data bus<br>(D16 to D23)                                 |
| PMFC   | PORTM<br>function<br>register | 005BH<br>(Prohibit<br>RMW) | PM7F                                |                                                              |                                                              |                                           |                                           | PM2F                                                                 | PM1F                                                                   |                                                                        |
|        |                               |                            | W                                   |                                                              |                                                              |                                           |                                           | W                                                                    |                                                                        |                                                                        |
|        |                               |                            | 0                                   |                                                              |                                                              |                                           |                                           | 0                                                                    | 0                                                                      |                                                                        |
|        |                               |                            | 0: Port<br>1: Don't<br>setting      |                                                              |                                                              |                                           |                                           | 0: Port<br>1: ALARM at<br><PM2>=1<br>MLDALM at<br><PM2>=0            | 0: Port<br>1: MLDALM<br>at<br><PM1>=1,<br>TA1OUT at<br><PM1>=0         |                                                                        |
| PNCR   | PORTN<br>control<br>register  | 005EH<br>(Prohibit<br>RMW) | PN7C                                | PN6C                                                         | PN5C                                                         | PN4C                                      | PN3C                                      | PN2C                                                                 | PN1C                                                                   | PN0C                                                                   |
|        |                               |                            | W                                   |                                                              |                                                              |                                           |                                           |                                                                      |                                                                        |                                                                        |
|        |                               |                            | 0                                   | 0                                                            | 0                                                            | 0                                         | 0                                         | 0                                                                    | 0                                                                      | 0                                                                      |
|        |                               |                            | 0: Input 1: Output                  |                                                              |                                                              |                                           |                                           |                                                                      |                                                                        |                                                                        |
| PNFC   | PORTN<br>function<br>register | 005FH<br>(Prohibit<br>RMW) | PN7F                                | PN6F                                                         | PN5F                                                         | PN4F                                      | PN3F                                      | PN2F                                                                 | PN1F                                                                   | PN0F                                                                   |
|        |                               |                            | W                                   |                                                              |                                                              |                                           |                                           |                                                                      |                                                                        |                                                                        |
|        |                               |                            | 0                                   | 0                                                            | 0                                                            | 0                                         | 0                                         | 0                                                                    | 0                                                                      | 0                                                                      |
|        |                               |                            | 0: CMOS output 1: Open-Drain output |                                                              |                                                              |                                           |                                           |                                                                      |                                                                        |                                                                        |
| PPCR   | PORTP<br>control<br>register  | 0062H<br>(Prohibit<br>RMW) |                                     |                                                              | PP5C                                                         | PP4C                                      | PP3C                                      |                                                                      |                                                                        |                                                                        |
|        |                               |                            |                                     |                                                              | W                                                            |                                           |                                           |                                                                      |                                                                        |                                                                        |
|        |                               |                            |                                     |                                                              | 0                                                            | 0                                         | 0                                         |                                                                      |                                                                        |                                                                        |
|        |                               |                            |                                     |                                                              | 0: Input 1: Output                                           |                                           |                                           |                                                                      |                                                                        |                                                                        |

## (1) I/O ports (7/10)

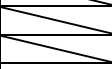
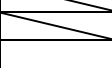
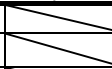
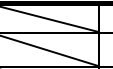
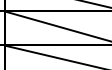
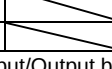
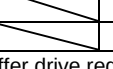
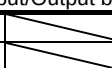
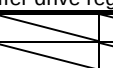
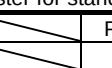
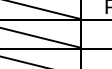
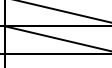
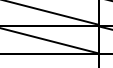
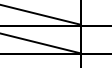
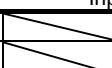
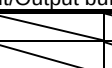
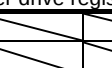
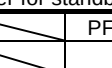
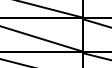
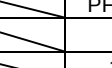
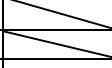
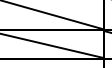
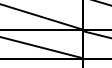
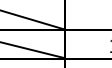
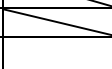
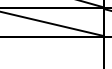
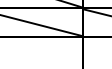
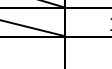
| Symbol | Name                            | Address                    | 7    | 6                                                                                               | 5                                                 | 4                                                 | 3                                                                           | 2                                                | 1                                                 | 0                                                |
|--------|---------------------------------|----------------------------|------|-------------------------------------------------------------------------------------------------|---------------------------------------------------|---------------------------------------------------|-----------------------------------------------------------------------------|--------------------------------------------------|---------------------------------------------------|--------------------------------------------------|
| PPFC   | PORTP<br>function<br>register   | 0063H<br>(Prohibit<br>RMW) |      | PP6F                                                                                            | PP5F                                              | PP4F                                              | PP3F                                                                        |                                                  |                                                   |                                                  |
|        |                                 |                            |      | W                                                                                               |                                                   |                                                   |                                                                             |                                                  |                                                   |                                                  |
|        |                                 |                            |      | 0                                                                                               | 0                                                 | 0                                                 | 0                                                                           |                                                  |                                                   |                                                  |
|        |                                 |                            |      | 0: Port<br>1: TB0OUT0                                                                           | 0: Port<br>1: INT7,<br>TB1IN0 at<br><PP3F2>=<br>0 | 0: Port<br>1: INT6,<br>TB0IN0 at<br><PP2F2>=<br>0 | 0: Port<br>1: INT5,<br>TA7OUT<br>at<PP1F2><br>= 0                           |                                                  |                                                   |                                                  |
| PPFC2  | PORTP<br>function 2<br>register | 0061H<br>(Prohibit<br>RMW) |      | PP6F2                                                                                           | PP5F2                                             | PP4F2                                             | PP3F2                                                                       | PP2F2                                            | PP1F2                                             | PP0F2                                            |
|        |                                 |                            |      | W                                                                                               |                                                   |                                                   |                                                                             |                                                  |                                                   |                                                  |
|        |                                 |                            |      | 0                                                                                               | 0                                                 | 0                                                 | 0                                                                           | 0                                                | 0                                                 | 0                                                |
|        |                                 |                            |      | PP5<br>SCLK<br>output<br>0: SCLK1<br>1: SCLK0<br>SIO1<br>SCLK,<br>CTS input<br>0: PP5<br>1: P92 | SIO1<br>RXD<br>selection<br>0: PP4<br>1: P91      | PP3<br>selection<br>0: TXD1<br>1: TXD0            | PP5<br>selection<br>0: Others<br>1: SCLK,<br>CTS input<br>or SCLK<br>output | PP4<br>selection<br>0: Others<br>1: RXD<br>input | PP3<br>selection<br>0: Others<br>1: TXD<br>output | PP3<br>selection<br>0: CMOS<br>1: Open<br>-drain |
| PRCR   | PORTR<br>control<br>register    | 0066H<br>(Prohibit<br>RMW) |      |                                                                                                 |                                                   |                                                   | PR3C                                                                        | PR2C                                             | PR1C                                              | PR0C                                             |
|        |                                 |                            |      |                                                                                                 |                                                   |                                                   | W                                                                           |                                                  |                                                   |                                                  |
|        |                                 |                            |      |                                                                                                 |                                                   |                                                   | 0                                                                           | 0                                                | 0                                                 | 0                                                |
|        |                                 |                            |      |                                                                                                 |                                                   |                                                   | 0: Input, 1: Output                                                         |                                                  |                                                   |                                                  |
| PRFC   | PORTR<br>function<br>register   | 0067H<br>(Prohibit<br>RMW) |      |                                                                                                 |                                                   |                                                   | PR3F                                                                        | PR2F                                             | PR1F                                              | PR0F                                             |
|        |                                 |                            |      |                                                                                                 |                                                   |                                                   | W                                                                           |                                                  |                                                   |                                                  |
|        |                                 |                            |      |                                                                                                 |                                                   |                                                   | 0                                                                           | 0                                                | 0                                                 | 0                                                |
|        |                                 |                            |      |                                                                                                 |                                                   |                                                   | 0: Port<br>1: SPCLK                                                         | 0: Port<br>1: SPCS                               | 0: Port<br>1: SPDO                                | 0: Port<br>1: SPD1                               |
| PTCR   | PORTT<br>control<br>register    | 00A2H<br>(Prohibit<br>RMW) | PT7C | PT6C                                                                                            | PT5C                                              | PT4C                                              | PT3C                                                                        | PT2C                                             | PT1C                                              | PT0C                                             |
|        |                                 |                            |      | W                                                                                               |                                                   |                                                   |                                                                             |                                                  |                                                   |                                                  |
|        |                                 |                            | 0    | 0                                                                                               | 0                                                 | 0                                                 | 0                                                                           | 0                                                | 0                                                 | 0                                                |
|        |                                 |                            |      | 0: Input 1: Output                                                                              |                                                   |                                                   |                                                                             |                                                  |                                                   |                                                  |
| PTFC   | PORTT<br>function<br>register   | 00A3H<br>(Prohibit<br>RMW) | PT7F | PT6F                                                                                            | PT5F                                              | PT4F                                              | PT3F                                                                        | PT2F                                             | PT1F                                              | PT0F                                             |
|        |                                 |                            |      | W                                                                                               |                                                   |                                                   |                                                                             |                                                  |                                                   |                                                  |
|        |                                 |                            | 0    | 0                                                                                               | 0                                                 | 0                                                 | 0                                                                           | 0                                                | 0                                                 | 0                                                |
|        |                                 |                            |      | 0: Port 1: Don't setting                                                                        |                                                   |                                                   |                                                                             |                                                  |                                                   |                                                  |
| PTFC2  | PORTL<br>function<br>register 2 | 00A1H<br>(Prohibit<br>RMW) |      |                                                                                                 |                                                   |                                                   |                                                                             |                                                  |                                                   | PT0F2                                            |
|        |                                 |                            |      |                                                                                                 |                                                   |                                                   |                                                                             |                                                  |                                                   | W                                                |
|        |                                 |                            |      |                                                                                                 |                                                   |                                                   |                                                                             |                                                  |                                                   | 0/1                                              |
|        |                                 |                            |      |                                                                                                 |                                                   |                                                   |                                                                             |                                                  |                                                   | 0: Port<br>1: Data bus<br>(D24 to D31)           |

## (1) I/O ports (8/10)

| Symbol | Name                       | Address                 | 7                            | 6                            | 5                                                                                                       | 4                               | 3 | 2 | 1 | 0 |
|--------|----------------------------|-------------------------|------------------------------|------------------------------|---------------------------------------------------------------------------------------------------------|---------------------------------|---|---|---|---|
| PVCR   | PORTV control register     | 00AAH<br>(Prohibit RMW) | PV7C                         | PV6C                         |                                                                                                         |                                 |   |   |   |   |
|        |                            |                         | W                            |                              |                                                                                                         |                                 |   |   |   |   |
|        |                            |                         | 0                            | 0                            |                                                                                                         |                                 |   |   |   |   |
|        |                            |                         | 0: Input                     | 1: Output                    |                                                                                                         |                                 |   |   |   |   |
| PVFC   | PORTV function register    | 00ABH<br>(Prohibit RMW) | PV7F                         | PV6F                         |                                                                                                         |                                 |   |   |   |   |
|        |                            |                         | W                            |                              |                                                                                                         |                                 |   |   |   |   |
|        |                            |                         | 0                            | 0                            |                                                                                                         |                                 |   |   |   |   |
|        |                            |                         | 0: Port<br>1: SCL            | 0: Port<br>1: SDA            |                                                                                                         |                                 |   |   |   |   |
| PVFC2  | PORTV function register 2  | 00A9H<br>(Prohibit RMW) | PV7F2                        | PV6F2                        |                                                                                                         |                                 |   |   |   |   |
|        |                            |                         | W                            |                              |                                                                                                         |                                 |   |   |   |   |
|        |                            |                         | 0                            | 0                            |                                                                                                         |                                 |   |   |   |   |
|        |                            |                         | 0: CMOS<br>1: Open<br>-drain | 0: CMOS<br>1: Open<br>-drain |                                                                                                         |                                 |   |   |   |   |
| PXCR   | PORT X control register    | 00B2H<br>(Prohibit RMW) |                              |                              | PX5C                                                                                                    |                                 |   |   |   |   |
|        |                            |                         |                              |                              | W                                                                                                       |                                 |   |   |   |   |
|        |                            |                         |                              |                              | 0                                                                                                       |                                 |   |   |   |   |
|        |                            |                         |                              |                              | 0: Input<br>1: Output                                                                                   |                                 |   |   |   |   |
| PXFC   | PORT X function register   | 00B3H<br>(Prohibit RMW) |                              |                              | PX5F                                                                                                    | PX4F                            |   |   |   |   |
|        |                            |                         |                              |                              | W                                                                                                       |                                 |   |   |   |   |
|        |                            |                         |                              |                              | 0                                                                                                       | 0                               |   |   |   |   |
|        |                            |                         |                              |                              | 0: Port<br>1: X1USB input at <PX5C>=0, X1D4 output at <PX5C>=1, <PX5>=1                                 | 0: Port<br>1: CLKOUT at <PX4>=0 |   |   |   |   |
| PXFC2  | PORT X function register 2 | 00B1H<br>(Prohibit RMW) |                              |                              | PX5F2                                                                                                   | PX4F2                           |   |   |   |   |
|        |                            |                         |                              |                              | W                                                                                                       |                                 |   |   |   |   |
|        |                            |                         |                              |                              | 0                                                                                                       | 0                               |   |   |   |   |
|        |                            |                         |                              |                              | –                                                                                                       | –                               |   |   |   |   |
|        |                            |                         |                              |                              | X1D4 output clock selection<br>00: X1 pin ×1/8<br>01: X1 pin ×1/4<br>10: X1 pin ×1/2<br>11: X1 pin ×1/1 |                                 |   |   |   |   |



## (1) I/O ports (9/10)

| Symbol | Name                       | Address | 7                                                                                   | 6                                                                                   | 5                                                                                   | 4                                                                                    | 3                                                                                     | 2                                                   | 1    | 0    |
|--------|----------------------------|---------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|-----------------------------------------------------|------|------|
| P1DR   | PORT1<br>drive<br>register | 0081H   | P17D                                                                                | P16D                                                                                | P15D                                                                                | P14D                                                                                 | P13D                                                                                  | P12D                                                | P11D | P10D |
|        |                            |         | R/W                                                                                 |                                                                                     |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
|        |                            |         | 1                                                                                   | 1                                                                                   | 1                                                                                   | 1                                                                                    | 1                                                                                     | 1                                                   | 1    | 1    |
|        |                            |         | Input/Output buffer drive register for standby mode                                 |                                                                                     |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
| P2DR   | PORT2<br>drive<br>register | 0082H   | P27D                                                                                | P26D                                                                                | P25D                                                                                | P24D                                                                                 | P23D                                                                                  | P22D                                                | P21D | P20D |
|        |                            |         | R/W                                                                                 |                                                                                     |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
|        |                            |         | 1                                                                                   | 1                                                                                   | 1                                                                                   | 1                                                                                    | 1                                                                                     | 1                                                   | 1    | 1    |
|        |                            |         | Input/Output buffer drive register for standby mode                                 |                                                                                     |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
| P3DR   | PORT3<br>drive<br>register | 0083H   | P37D                                                                                | P36D                                                                                | P35D                                                                                | P34D                                                                                 | P33D                                                                                  | P32D                                                | P31D | P30D |
|        |                            |         | R/W                                                                                 |                                                                                     |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
|        |                            |         | 1                                                                                   | 1                                                                                   | 1                                                                                   | 1                                                                                    | 1                                                                                     | 1                                                   | 1    | 1    |
|        |                            |         | Input/Output buffer drive register for standby mode                                 |                                                                                     |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
| P4DR   | PORT4<br>drive<br>register | 0084H   | P47D                                                                                | P46D                                                                                | P45D                                                                                | P44D                                                                                 | P43D                                                                                  | P42D                                                | P41D | P40D |
|        |                            |         | R/W                                                                                 |                                                                                     |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
|        |                            |         | 1                                                                                   | 1                                                                                   | 1                                                                                   | 1                                                                                    | 1                                                                                     | 1                                                   | 1    | 1    |
|        |                            |         | Input/Output buffer drive register for standby mode                                 |                                                                                     |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
| P5DR   | PORT5<br>drive<br>register | 0085H   | P57D                                                                                | P56D                                                                                | P55D                                                                                | P54D                                                                                 | P53D                                                                                  | P52D                                                | P51D | P50D |
|        |                            |         | R/W                                                                                 |                                                                                     |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
|        |                            |         | 1                                                                                   | 1                                                                                   | 1                                                                                   | 1                                                                                    | 1                                                                                     | 1                                                   | 1    | 1    |
|        |                            |         | Input/Output buffer drive register for standby mode                                 |                                                                                     |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
| P6DR   | PORT6<br>drive<br>register | 0086H   | P67D                                                                                | P66D                                                                                | P65D                                                                                | P64D                                                                                 | P63D                                                                                  | P62D                                                | P61D | P60D |
|        |                            |         | R/W                                                                                 |                                                                                     |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
|        |                            |         | 1                                                                                   | 1                                                                                   | 1                                                                                   | 1                                                                                    | 1                                                                                     | 1                                                   | 1    | 1    |
|        |                            |         | Input/Output buffer drive register for standby mode                                 |                                                                                     |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
| P7DR   | PORT7<br>drive<br>register | 0087H   |   | P76D                                                                                | P75D                                                                                | P74D                                                                                 | P73D                                                                                  | P72D                                                | P71D | P70D |
|        |                            |         |   | R/W                                                                                 |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
|        |                            |         |   | 1                                                                                   | 1                                                                                   | 1                                                                                    | 1                                                                                     | 1                                                   | 1    | 1    |
|        |                            |         |  | Input/Output buffer drive register for standby mode                                 |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
| P8DR   | PORT8<br>drive<br>register | 0088H   | P87D                                                                                | P86D                                                                                |  |   | P83D                                                                                  | P82D                                                | P81D | P80D |
|        |                            |         | R/W                                                                                 |                                                                                     |  |   | R/W                                                                                   |                                                     |      |      |
|        |                            |         | 1                                                                                   | 1                                                                                   |  |   | 1                                                                                     | 1                                                   | 1    | 1    |
|        |                            |         | Input/Output buffer drive register for standby mode                                 |                                                                                     |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
| P9DR   | PORT9<br>drive<br>register | 0089H   | P97D                                                                                | P96D                                                                                |  |   |  | P92D                                                | P91D | P90D |
|        |                            |         | R/W                                                                                 |                                                                                     |  |   |  | R/W                                                 |      |      |
|        |                            |         | 1                                                                                   | 1                                                                                   |  |   |  | 1                                                   | 1    | 1    |
|        |                            |         | Input/Output buffer drive register for standby mode                                 |                                                                                     |                                                                                     |                                                                                      | Input/Output buffer drive register for standby mode                                   |                                                     |      |      |
| PADR   | PORTA<br>drive<br>register | 008AH   | PA7D                                                                                | PA6D                                                                                | PA5D                                                                                | PA4D                                                                                 | PA3D                                                                                  | PA2D                                                | PA1D | PA0D |
|        |                            |         | R/W                                                                                 |                                                                                     |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
|        |                            |         | 1                                                                                   | 1                                                                                   | 1                                                                                   | 1                                                                                    | 1                                                                                     | 1                                                   | 1    | 1    |
|        |                            |         | Input/Output buffer drive register for standby mode                                 |                                                                                     |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
| PCDR   | PORTC<br>drive<br>register | 008CH   | PC7D                                                                                | PC6D                                                                                | PC5D                                                                                | PC4D                                                                                 | PC3D                                                                                  | PC2D                                                | PC1D | PC0D |
|        |                            |         | R/W                                                                                 |                                                                                     |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
|        |                            |         | 1                                                                                   | 1                                                                                   | 1                                                                                   | 1                                                                                    | 1                                                                                     | 1                                                   | 1    | 1    |
|        |                            |         | Input/Output buffer drive register for standby mode                                 |                                                                                     |                                                                                     |                                                                                      |                                                                                       |                                                     |      |      |
| PFDR   | PORTF<br>drive<br>register | 008FH   | PF7D                                                                                |  |  |  |  | PF2D                                                | PF1D | PF0D |
|        |                            |         | R/W                                                                                 |  |  |  |  | R/W                                                 |      |      |
|        |                            |         | 1                                                                                   |  |  |  |  | 1                                                   | 1    | 1    |
|        |                            |         | Input/<br>Output<br>buffer<br>drive<br>register for<br>standby<br>mode              |  |  |  |  | Input/Output buffer drive register for standby mode |      |      |

## (1) I/O ports (10/10)

| Symbol | Name                       | Address | 7                                                   | 6                                                   | 5                                                   | 4    | 3                                                         | 2    | 1    | 0    |
|--------|----------------------------|---------|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|------|-----------------------------------------------------------|------|------|------|
| PGDR   | PORTG<br>drive<br>register | 0090H   |                                                     |                                                     |                                                     |      | PG3D                                                      | PG2D |      |      |
|        |                            |         |                                                     |                                                     |                                                     |      | R/W                                                       |      |      |      |
|        |                            |         |                                                     |                                                     |                                                     |      | 1                                                         | 1    |      |      |
|        |                            |         |                                                     |                                                     |                                                     |      | Input/Output buffer<br>drive register for<br>standby mode |      |      |      |
| PJDR   | PORTJ<br>drive<br>register | 0093H   | PJ7D                                                | PJ6D                                                | PJ5D                                                | PJ4D | PJ3D                                                      | PJ2D | PJ1D | PJ0D |
|        |                            |         | R/W                                                 |                                                     |                                                     |      |                                                           |      |      |      |
|        |                            |         | 1                                                   | 1                                                   | 1                                                   | 1    | 1                                                         | 1    | 1    | 1    |
|        |                            |         | Input/Output buffer drive register for standby mode |                                                     |                                                     |      |                                                           |      |      |      |
| PKDR   | PORTK<br>drive<br>register | 0094H   | PK7D                                                | PK6D                                                | PK5D                                                | PK4D | PK3D                                                      | PK2D | PK1D | PK0D |
|        |                            |         | R/W                                                 |                                                     |                                                     |      |                                                           |      |      |      |
|        |                            |         | 1                                                   | 1                                                   | 1                                                   | 1    | 1                                                         | 1    | 1    | 1    |
|        |                            |         | Input/Output buffer drive register for standby mode |                                                     |                                                     |      |                                                           |      |      |      |
| PLDR   | PORTL<br>drive<br>register | 0095H   | PL7D                                                | PL6D                                                | PL5D                                                | PL4D | PL3D                                                      | PL2D | PL1D | PL0D |
|        |                            |         | R/W                                                 |                                                     |                                                     |      |                                                           |      |      |      |
|        |                            |         | 1                                                   | 1                                                   | 1                                                   | 1    | 1                                                         | 1    | 1    | 1    |
|        |                            |         | Input/Output buffer drive register for standby mode |                                                     |                                                     |      |                                                           |      |      |      |
| PMDR   | PORTM<br>drive<br>register | 0096H   | PM7D                                                |                                                     |                                                     |      |                                                           | PM2D | PM1D |      |
|        |                            |         | R/W                                                 |                                                     |                                                     |      |                                                           | R/W  |      |      |
|        |                            |         | 1                                                   |                                                     |                                                     |      |                                                           | 1    | 1    |      |
|        |                            |         | Input/Output buffer drive register for standby mode |                                                     |                                                     |      |                                                           |      |      |      |
| PNDR   | PORTN<br>drive<br>register | 0097H   | PN7D                                                | PN6D                                                | PN5D                                                | PN4D | PN3D                                                      | PN2D | PN1D | PN0D |
|        |                            |         | R/W                                                 |                                                     |                                                     |      |                                                           |      |      |      |
|        |                            |         | 1                                                   | 1                                                   | 1                                                   | 1    | 1                                                         | 1    | 1    | 1    |
|        |                            |         | Input/Output buffer drive register for standby mode |                                                     |                                                     |      |                                                           |      |      |      |
| PPDR   | PORTP<br>drive<br>register | 0098H   |                                                     | PP6D                                                | PP5D                                                | PP4D | PP3D                                                      |      |      |      |
|        |                            |         |                                                     | R/W                                                 |                                                     |      |                                                           |      |      |      |
|        |                            |         |                                                     | 1                                                   | 1                                                   | 1    | 1                                                         |      |      |      |
|        |                            |         |                                                     | Input/Output buffer drive register for standby mode |                                                     |      |                                                           |      |      |      |
| PRDR   | PORTR<br>drive<br>register | 0099H   |                                                     |                                                     |                                                     |      | PR3D                                                      | PR2D | PR1D | PR0D |
|        |                            |         |                                                     |                                                     |                                                     |      | R/W                                                       |      |      |      |
|        |                            |         |                                                     |                                                     |                                                     |      | 1                                                         | 1    | 1    | 1    |
|        |                            |         |                                                     |                                                     |                                                     |      | Input/Output buffer drive register for standby mode       |      |      |      |
| PTDR   | PORTT<br>drive<br>register | 009BH   | PT7D                                                | PT6D                                                | PT5D                                                | PT4D | PT3D                                                      | PT2D | PT1D | PT0D |
|        |                            |         | R/W                                                 |                                                     |                                                     |      |                                                           |      |      |      |
|        |                            |         | 1                                                   | 1                                                   | 1                                                   | 1    | 1                                                         | 1    | 1    | 1    |
|        |                            |         | Input/Output buffer drive register for standby mode |                                                     |                                                     |      |                                                           |      |      |      |
| PVDR   | PORTV<br>drive<br>register | 009DH   | PV7D                                                | PV6D                                                |                                                     |      |                                                           |      |      |      |
|        |                            |         | R/W                                                 |                                                     |                                                     |      |                                                           |      |      |      |
|        |                            |         | 1                                                   | 1                                                   |                                                     |      |                                                           |      |      |      |
|        |                            |         | Input/Output buffer drive register for standby mode |                                                     |                                                     |      |                                                           |      |      |      |
| PXDR   | PORTX<br>drive<br>register | 009FH   |                                                     |                                                     | PX5D                                                | PX4D |                                                           |      |      |      |
|        |                            |         |                                                     |                                                     | R/W                                                 |      |                                                           |      |      |      |
|        |                            |         |                                                     |                                                     | 1                                                   | 1    |                                                           |      |      |      |
|        |                            |         |                                                     |                                                     | Input/Output buffer drive register for standby mode |      |                                                           |      |      |      |

## (2) Interrupt control (1/4)

| Symbol     | Name                     | Address | 7                | 6       | 5       | 4       | 3               | 2       | 1       | 0       |
|------------|--------------------------|---------|------------------|---------|---------|---------|-----------------|---------|---------|---------|
| INTE0      | INT0 enable              | 00F0H   | –                |         |         |         | INT0            |         |         |         |
|            |                          |         | –                | –       | –       | –       | I0C             | I0M2    | I0M1    | I0M0    |
|            |                          |         | –                | –       |         |         | R               | R/W     |         |         |
|            |                          |         | Always write “0” |         |         |         | 0               | 0       | 0       | 0       |
| INTE12     | INT1 & INT2 enable       | 00D0H   | INT2             |         |         |         | INT1            |         |         |         |
|            |                          |         | I2C              | I2M2    | I2M1    | I2M0    | I1C             | I1M2    | I1M1    | I1M0    |
|            |                          |         | R                | R/W     |         |         | R               | R/W     |         |         |
|            |                          |         | 0                | 0       | 0       | 0       | 0               | 0       | 0       | 0       |
| INTE34     | INT3 & INT4 enable       | 00D1H   | INT4             |         |         |         | INT3            |         |         |         |
|            |                          |         | I4C              | I4M2    | I4M1    | I4M0    | I3C             | I3M2    | I3M1    | I3M0    |
|            |                          |         | R                | R/W     |         |         | R               | R/W     |         |         |
|            |                          |         | 0                | 0       | 0       | 0       | 0               | 0       | 0       | 0       |
| INTE56     | INT5 & INT6 enable       | 00D2H   | INT6             |         |         |         | INT5            |         |         |         |
|            |                          |         | I6C              | I6M2    | I6M1    | I6M0    | I5C             | I5M2    | I5M1    | I5M0    |
|            |                          |         | R                | R/W     |         |         | R               | R/W     |         |         |
|            |                          |         | 0                | 0       | 0       | 0       | 0               | 0       | 0       | 0       |
| INTE7      | INT7 enable              | 00D3H   | –                |         |         |         | INT7            |         |         |         |
|            |                          |         | –                | –       | –       | –       | I7C             | I7M2    | I7M1    | I7M0    |
|            |                          |         | –                | –       |         |         | R               | R/W     |         |         |
|            |                          |         | Always write “0” |         |         |         | 0               | 0       | 0       | 0       |
| INTETA01   | INTTA0 & INTTA1 enable   | 00D4H   | INTTA1 (TMRA1)   |         |         |         | INTTA0 (TMRA0)  |         |         |         |
|            |                          |         | ITA1C            | ITA1M2  | ITA1M1  | ITA1M0  | ITA0C           | ITA0M2  | ITA0M1  | ITA0M0  |
|            |                          |         | R                | R/W     |         |         | R               | R/W     |         |         |
|            |                          |         | 0                | 0       | 0       | 0       | 0               | 0       | 0       | 0       |
| INTETA23   | INTTA2 & INTTA3 enable   | 00D5H   | INTTA3 (TMRA3)   |         |         |         | INTTA2 (TMRA2)  |         |         |         |
|            |                          |         | ITA3C            | ITA3M2  | ITA3M1  | ITA3M0  | ITA2C           | ITA2M2  | ITA2M1  | ITA2M0  |
|            |                          |         | R                | R/W     |         |         | R               | R/W     |         |         |
|            |                          |         | 0                | 0       | 0       | 0       | 0               | 0       | 0       | 0       |
| INTETA45   | INTTA4 & INTTA5 enable   | 00D6H   | INTTA5 (TMRA5)   |         |         |         | INTTA4 (TMRA4)  |         |         |         |
|            |                          |         | ITA5C            | ITA5M2  | ITA5M1  | ITA5M0  | ITA4C           | ITA4M2  | ITA4M1  | ITA4M0  |
|            |                          |         | R                | R/W     |         |         | R               | R/W     |         |         |
|            |                          |         | 0                | 0       | 0       | 0       | 0               | 0       | 0       | 0       |
| INTETA67   | INTTA6 & INTTA7 enable   | 00D7H   | INTTA7 (TMRA7)   |         |         |         | INTTA6 (TMRA6)  |         |         |         |
|            |                          |         | ITA7C            | ITA7M2  | ITA7M1  | ITA7M0  | ITA6C           | ITA6M2  | ITA6M1  | ITA6M0  |
|            |                          |         | R                | R/W     |         |         | R               | R/W     |         |         |
|            |                          |         | 0                | 0       | 0       | 0       | 0               | 0       | 0       | 0       |
| INTETB0    | INTTB00 & INTTB01 enable | 00D8H   | INTTB01 (TMRB0)  |         |         |         | INTTB00 (TMRB0) |         |         |         |
|            |                          |         | ITB01C           | ITB01M2 | ITB01M1 | ITB01M0 | ITB00C          | ITB00M2 | ITB00M1 | ITB00M0 |
|            |                          |         | R                | R/W     |         |         | R               | R/W     |         |         |
|            |                          |         | 0                | 0       | 0       | 0       | 0               | 0       | 0       | 0       |
| INTETB1    | INTTB10 & INTTB11 enable | 00D9H   | INTTB11 (TMRB1)  |         |         |         | INTTB10 (TMRB1) |         |         |         |
|            |                          |         | ITB11C           | ITB11M2 | ITB11M1 | ITB11M0 | ITB10C          | ITB10M2 | ITB10M1 | ITB10M0 |
|            |                          |         | R                | R/W     |         |         | R               | R/W     |         |         |
|            |                          |         | 0                | 0       | 0       | 0       | 0               | 0       | 0       | 0       |
| INTES0     | INTRX0 & INTTX0 enable   | 00DBH   | INTTX0           |         |         |         | INTRX0          |         |         |         |
|            |                          |         | ITX0C            | ITX0M2  | ITX0M1  | ITX0M0  | IRX0C           | IRX0M2  | IRX0M1  | IRX0M0  |
|            |                          |         | R                | R/W     |         |         | R               | R/W     |         |         |
|            |                          |         | 0                | 0       | 0       | 0       | 0               | 0       | 0       | 0       |
| INTES1     | INTRX1 & INTTX1 enable   | 00DCH   | INTTX1           |         |         |         | INTRX1          |         |         |         |
|            |                          |         | ITX1C            | ITX1M2  | ITX1M1  | ITX1M0  | IRX1C           | IRX1M2  | IRX1M1  | IRX1M0  |
|            |                          |         | R                | R/W     |         |         | R               | R/W     |         |         |
|            |                          |         | 0                | 0       | 0       | 0       | 0               | 0       | 0       | 0       |
| INTESBIADM | INTSBI & INTADM enable   | 00E0H   | INTADM           |         |         |         | INTSBI          |         |         |         |
|            |                          |         | IADM0C           | IADMM2  | IADMM1  | IADMM0  | ISBI0C          | ISBIM2  | ISBIM1  | ISBIM0  |
|            |                          |         | R                | R/W     |         |         | R               | R/W     |         |         |
|            |                          |         | 0                | 0       | 0       | 0       | 0               | 0       | 0       | 0       |

## (2) Interrupt control (2/4)

| Symbol   | Name                   | Address | 7                | 6       | 5       | 4       | 3        | 2       | 1       | 0       |
|----------|------------------------|---------|------------------|---------|---------|---------|----------|---------|---------|---------|
| INTESPI  | INTSPI enable          | 00E1H   | INTSPITX         |         |         |         | INTSPIRX |         |         |         |
|          |                        |         | ISPITC           | ISPITM2 | ISPITM1 | ISPITM0 | ISPIRC   | ISPIRM2 | ISPIRM1 | ISPIRM0 |
|          |                        |         | R                | R/W     |         |         | R        | R/W     |         |         |
|          |                        |         | 0                | 0       | 0       | 0       | 0        | 0       | 0       | 0       |
| INTEUSB  | INTUSB enable          | 00E3H   | —                |         |         |         | INTUSB   |         |         |         |
|          |                        |         | —                | —       | —       | —       | IUSBC    | IUSBM2  | IUSBM1  | IUSBM0  |
|          |                        |         | —                | —       |         |         | R        | R/W     |         |         |
|          |                        |         | Always write “0” |         |         |         | 0        | 0       | 0       | 0       |
| INTEALM  | INTALM enable          | 00E5H   | —                |         |         |         | INTALM   |         |         |         |
|          |                        |         | —                | —       | —       | —       | IALMC    | IALMM2  | IALMM1  | IALMM0  |
|          |                        |         | —                | —       |         |         | R        | R/W     |         |         |
|          |                        |         | Always write “0” |         |         |         | 0        | 0       | 0       | 0       |
| INTERTC  | INTRTC enable          | 00E8H   | —                |         |         |         | INTRTC   |         |         |         |
|          |                        |         | —                | —       | —       | —       | IRC      | IRM2    | IRM1    | IRM0    |
|          |                        |         | —                | —       |         |         | R        | R/W     |         |         |
|          |                        |         | Always write “0” |         |         |         | 0        | 0       | 0       | 0       |
| INTEKEY  | INTKEY enable          | 00E9H   | —                |         |         |         | INTKEY   |         |         |         |
|          |                        |         | —                | —       | —       | —       | IKC      | IKM2    | IKM1    | IKM0    |
|          |                        |         | —                | —       |         |         | R        | R/W     |         |         |
|          |                        |         | Always write “0” |         |         |         | 0        | 0       | 0       | 0       |
| INTEI2S0 | INTI2S0 enable         | 00EBH   | —                |         |         |         | INTI2S0  |         |         |         |
|          |                        |         | —                | —       | —       | —       | I2S0C    | I2S0M2  | I2S0M1  | I2S0M0  |
|          |                        |         | —                | —       |         |         | R        | R/W     |         |         |
|          |                        |         | Always write “0” |         |         |         | 0        | 0       | 0       | 0       |
| INTENDFC | INTRSC & INTRDY enable | 00ECH   | INTRSC           |         |         |         | INTRDY   |         |         |         |
|          |                        |         | IRSCC            | IRSCM2  | IRSCM1  | IRSCM0  | IRDYC    | IRDYM2  | IRDYM1  | IRDYM0  |
|          |                        |         | R                | R/W     |         |         | R        | R/W     |         |         |
|          |                        |         | 0                | 0       | 0       | 0       | 0        | 0       | 0       | 0       |
| INTEP0   | INTP0 enable           | 00EEH   | —                |         |         |         | INTP0    |         |         |         |
|          |                        |         | —                | —       | —       | —       | IP0C     | IP0M2   | IP0M1   | IP0M0   |
|          |                        |         | —                | —       |         |         | R        | R/W     |         |         |
|          |                        |         | Always write “0” |         |         |         | 0        | 0       | 0       | 0       |
| INTEAD   | INTAD & INTADHP enable | 00EFH   | INTADHP          |         |         |         | INTAD    |         |         |         |
|          |                        |         | IADHPC           | IADHPM2 | IADHPM1 | IADHPM0 | IADC     | IADM2   | IADM1   | IADM0   |
|          |                        |         | R                | R/W     |         |         | R        | R/W     |         |         |
|          |                        |         | 0                | 0       | 0       | 0       | 0        | 0       | 0       | 0       |

## (2) Interrupt control (3/4)

| Symbol                | Name                                         | Address                    | 7                                       | 6                                       | 5                                       | 4                                       | 3                                       | 2                                       | 1                                                       | 0                                                                 |
|-----------------------|----------------------------------------------|----------------------------|-----------------------------------------|-----------------------------------------|-----------------------------------------|-----------------------------------------|-----------------------------------------|-----------------------------------------|---------------------------------------------------------|-------------------------------------------------------------------|
| INTETC01<br>/INTDMA01 | INTTC0/INTDMA0 &<br>INTTC1/INTDMA1<br>enable | 00F1H                      | INTTC1/INTDMA1                          |                                         |                                         |                                         | INTTC0/INTDMA0                          |                                         |                                                         |                                                                   |
|                       |                                              |                            | ITC1C<br>/IDMA1C                        | ITC1M2<br>/IDMA1M2                      | ITC1M1<br>/IDMA1M1                      | ITC1M0<br>/IDMA1M0                      | ITC0C<br>/IDMA0C                        | ITC0M2<br>/IDMA0M2                      | ITC0M1<br>/IDMA0M1                                      | ITC0M0<br>/IDMA0M0                                                |
|                       |                                              |                            | R                                       | R/W                                     |                                         |                                         | R                                       | R/W                                     |                                                         |                                                                   |
|                       |                                              |                            | 0                                       | 0                                       | 0                                       | 0                                       | 0                                       | 0                                       | 0                                                       | 0                                                                 |
| INTETC23<br>/INTDMA23 | INTTC2/INTDMA2 &<br>INTTC3/INTDMA3<br>enable | 00F2H                      | INTTC3/INTDMA3                          |                                         |                                         |                                         | INTTC2/INTDMA2                          |                                         |                                                         |                                                                   |
|                       |                                              |                            | ITC3C<br>/IDMA3C                        | ITC3M2<br>/IDMA3M2                      | ITC3M1<br>/IDMA3M1                      | ITC3M0<br>/IDMA3M0                      | ITC2C<br>/IDMA2C                        | ITC2M2<br>/IDMA2M2                      | ITC2M1<br>/IDMA2M1                                      | ITC2M0<br>/IDMA2M0                                                |
|                       |                                              |                            | R                                       | R/W                                     |                                         |                                         | R                                       | R/W                                     |                                                         |                                                                   |
|                       |                                              |                            | 0                                       | 0                                       | 0                                       | 0                                       | 0                                       | 0                                       | 0                                                       | 0                                                                 |
| INTETC45<br>/INTDMA45 | INTTC4/INTDMA4 &<br>INTTC5/INTDMA5<br>enable | 00F3H                      | INTTC5/INTDMA5                          |                                         |                                         |                                         | INTTC4/INTDMA4                          |                                         |                                                         |                                                                   |
|                       |                                              |                            | ITC5C<br>/IDMA5C                        | ITC5M2<br>/IDMA5M2                      | ITC5M1<br>/IDMA5M1                      | ITC5M0<br>/IDMA5M0                      | ITC4C<br>/IDMA4C                        | ITC4M2<br>/IDMA4M2                      | ITC4M1<br>/IDMA4M1                                      | ITC4M0<br>/IDMA4M0                                                |
|                       |                                              |                            | R                                       | R/W                                     |                                         |                                         | R                                       | R/W                                     |                                                         |                                                                   |
|                       |                                              |                            | 0                                       | 0                                       | 0                                       | 0                                       | 0                                       | 0                                       | 0                                                       | 0                                                                 |
| INTETC67              | INTTC6 & INTTC7<br>enable                    | 00F4H                      | INTTC7 (DMA7)                           |                                         |                                         |                                         | INTTC6 (DMA6)                           |                                         |                                                         |                                                                   |
|                       |                                              |                            | ITC7C                                   | ITC7M2                                  | ITC7M1                                  | ITC7M0                                  | ITC6C                                   | ITC6M2                                  | ITC6M1                                                  | ITC6M0                                                            |
|                       |                                              |                            | R                                       | R/W                                     |                                         |                                         | R                                       | R/W                                     |                                                         |                                                                   |
|                       |                                              |                            | 0                                       | 0                                       | 0                                       | 0                                       | 0                                       | 0                                       | 0                                                       | 0                                                                 |
| SIMC                  | SIO<br>interrupt mode<br>control             | 00F5H<br>(Prohibit<br>RMW) | –                                       | –                                       |                                         |                                         |                                         |                                         | IR1LE                                                   | IR0LE                                                             |
|                       |                                              |                            | W                                       |                                         |                                         |                                         |                                         |                                         | W                                                       |                                                                   |
|                       |                                              |                            | 0                                       | 0                                       |                                         |                                         |                                         |                                         | 1                                                       | 1                                                                 |
|                       |                                              |                            | Always<br>write “0”                     | Always<br>write “0”                     |                                         |                                         |                                         |                                         | 0: INTRX1<br>edge<br>mode<br>1: INTRX1<br>level<br>mode | 0: INTRX0<br>edge mode<br>1: INTRX0<br>level mode                 |
| IIMC0                 | Interrupt<br>input mode control 0            | 00F6H<br>(Prohibit<br>RMW) | I5EDGE                                  | I4EDGE                                  | I3EDGE                                  | I2EDGE                                  | I1EDGE                                  | I0EDGE                                  | I0LE                                                    | NMIREE                                                            |
|                       |                                              |                            | W                                       |                                         |                                         |                                         |                                         |                                         | R/W                                                     | R/W                                                               |
|                       |                                              |                            | 0                                       | 0                                       | 0                                       | 0                                       | 0                                       | 0                                       | 0                                                       | 0                                                                 |
|                       |                                              |                            | INT5<br>edge<br>0: Rising<br>1: Falling | INT4<br>edge<br>0: Rising<br>1: Falling | INT3<br>edge<br>0: Rising<br>1: Falling | INT2<br>edge<br>0: Rising<br>1: Falling | INT1<br>edge<br>0: Rising<br>1: Falling | INT0<br>edge<br>0: Rising<br>1: Falling | 0: INT0<br>edge mode<br>1: INT0<br>level mode           | NMI EDGE<br>0: Falling<br>1: Both edge<br>(Falling and<br>Rising) |
| INTWDT/NMI            | INTWD & NMI<br>enable                        | 00F7H                      | –                                       |                                         |                                         |                                         | INTWD                                   |                                         |                                                         |                                                                   |
|                       |                                              |                            | ITCNMI                                  | –                                       | –                                       | –                                       | ITCWD                                   | –                                       | –                                                       | –                                                                 |
|                       |                                              |                            | R                                       | –                                       |                                         |                                         | R                                       | –                                       | –                                                       | –                                                                 |
|                       |                                              |                            | Always write “0”                        |                                         |                                         |                                         | 0                                       | –                                       | –                                                       | –                                                                 |
| INTCLR                | Interrupt<br>clear control                   | 00F8H<br>(Prohibit<br>RMW) | CLR7                                    | CLR6                                    | CLR5                                    | CLR4                                    | CLR3                                    | CLR2                                    | CLR1                                                    | CLR0                                                              |
|                       |                                              |                            | W                                       |                                         |                                         |                                         |                                         |                                         |                                                         |                                                                   |
|                       |                                              |                            | 0                                       | 0                                       | 0                                       | 0                                       | 0                                       | 0                                       | 0                                                       | 0                                                                 |
|                       |                                              |                            | Interrupt vector                        |                                         |                                         |                                         |                                         |                                         |                                                         |                                                                   |
| IIMC1                 | Interrupt<br>input mode control 1            | 00FAH<br>(Prohibit<br>RMW) |                                         |                                         |                                         |                                         |                                         |                                         | I7EDGE                                                  | I6EDGE                                                            |
|                       |                                              |                            |                                         |                                         |                                         |                                         |                                         |                                         | W                                                       | W                                                                 |
|                       |                                              |                            |                                         |                                         |                                         |                                         |                                         |                                         | 0                                                       | 0                                                                 |
|                       |                                              |                            |                                         |                                         |                                         |                                         |                                         |                                         | INT7<br>edge<br>0: Rising<br>1: Falling                 | INT6<br>edge<br>0: Rising<br>1: Falling                           |

## (2) Interrupt control (4/4)

| Symbol | Name                  | Address                 | 7                            | 6     | 5                         | 4                         | 3                         | 2                         | 1                         | 0                         |
|--------|-----------------------|-------------------------|------------------------------|-------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| DMA0V  | DMA0 start vector     | 0100H                   |                              |       | DMA0V5                    | DMA0V4                    | DMA0V3                    | DMA0V2                    | DMA0V1                    | DMA0V0                    |
|        |                       |                         |                              |       | R/W                       |                           |                           |                           |                           |                           |
|        |                       |                         |                              |       | 0                         | 0                         | 0                         | 0                         | 0                         | 0                         |
|        |                       |                         |                              |       | DMA0 start vector         |                           |                           |                           |                           |                           |
| DMA1V  | DMA1 start vector     | 0101H                   |                              |       | DMA1V5                    | DMA1V4                    | DMA1V3                    | DMA1V2                    | DMA1V1                    | DMA1V0                    |
|        |                       |                         |                              |       | R/W                       |                           |                           |                           |                           |                           |
|        |                       |                         |                              |       | 0                         | 0                         | 0                         | 0                         | 0                         | 0                         |
|        |                       |                         |                              |       | DMA1 start vector         |                           |                           |                           |                           |                           |
| DMA2V  | DMA2 start vector     | 0102H                   |                              |       | DMA2V5                    | DMA2V4                    | DMA2V3                    | DMA2V2                    | DMA2V1                    | DMA2V0                    |
|        |                       |                         |                              |       | R/W                       |                           |                           |                           |                           |                           |
|        |                       |                         |                              |       | 0                         | 0                         | 0                         | 0                         | 0                         | 0                         |
|        |                       |                         |                              |       | DMA2 start vector         |                           |                           |                           |                           |                           |
| DMA3V  | DMA3 start vector     | 0103H                   |                              |       | DMA3V5                    | DMA3V4                    | DMA3V3                    | DMA3V2                    | DMA3V1                    | DMA3V0                    |
|        |                       |                         |                              |       | R/W                       |                           |                           |                           |                           |                           |
|        |                       |                         |                              |       | 0                         | 0                         | 0                         | 0                         | 0                         | 0                         |
|        |                       |                         |                              |       | DMA3 start vector         |                           |                           |                           |                           |                           |
| DMA4V  | DMA4 start vector     | 0104H                   |                              |       | DMA4V5                    | DMA4V4                    | DMA4V3                    | DMA4V2                    | DMA4V1                    | DMA4V0                    |
|        |                       |                         |                              |       | R/W                       |                           |                           |                           |                           |                           |
|        |                       |                         |                              |       | 0                         | 0                         | 0                         | 0                         | 0                         | 0                         |
|        |                       |                         |                              |       | DMA4 start vector         |                           |                           |                           |                           |                           |
| DMA5V  | DMA5 start vector     | 0105H                   |                              |       | DMA5V5                    | DMA5V4                    | DMA5V3                    | DMA5V2                    | DMA5V1                    | DMA5V0                    |
|        |                       |                         |                              |       | R/W                       |                           |                           |                           |                           |                           |
|        |                       |                         |                              |       | 0                         | 0                         | 0                         | 0                         | 0                         | 0                         |
|        |                       |                         |                              |       | DMA5 start vector         |                           |                           |                           |                           |                           |
| DMA6V  | DMA6 start vector     | 0106H                   |                              |       | DMA6V5                    | DMA6V4                    | DMA6V3                    | DMA6V2                    | DMA6V1                    | DMA6V0                    |
|        |                       |                         |                              |       | R/W                       |                           |                           |                           |                           |                           |
|        |                       |                         |                              |       | 0                         | 0                         | 0                         | 0                         | 0                         | 0                         |
|        |                       |                         |                              |       | DMA6 start vector         |                           |                           |                           |                           |                           |
| DMA7V  | DMA7 start vector     | 0107H                   |                              |       | DMA7V5                    | DMA7V4                    | DMA7V3                    | DMA7V2                    | DMA7V1                    | DMA7V0                    |
|        |                       |                         |                              |       | R/W                       |                           |                           |                           |                           |                           |
|        |                       |                         |                              |       | 0                         | 0                         | 0                         | 0                         | 0                         | 0                         |
|        |                       |                         |                              |       | DMA7 start vector         |                           |                           |                           |                           |                           |
| DMAB   | DMA burst             | 0108H                   | DBST7                        | DBST6 | DBST5                     | DBST4                     | DBST3                     | DBST2                     | DBST1                     | DBST0                     |
|        |                       |                         | R/W                          |       |                           |                           |                           |                           |                           |                           |
|        |                       |                         | 0                            | 0     | 0                         | 0                         | 0                         | 0                         | 0                         | 0                         |
|        |                       |                         | 1: DMA request on burst mode |       |                           |                           |                           |                           |                           |                           |
| DMAR   | DMA request           | 0109H<br>(Prohibit RMW) | DREQ7                        | DREQ6 | DREQ5                     | DREQ4                     | DREQ3                     | DREQ2                     | DREQ1                     |                           |
|        |                       |                         | R/W                          |       |                           |                           |                           |                           |                           |                           |
|        |                       |                         | 0                            | 0     | 0                         | 0                         | 0                         | 0                         | 0                         | 0                         |
|        |                       |                         | 1: DMA request in software   |       |                           |                           |                           |                           |                           |                           |
| DMASEL | Micro DMA/HDMA Select | 010AH                   |                              |       | DMASEL5                   | DMASEL4                   | DMASEL3                   | DMASEL2                   | DMASEL1                   | DMASEL0                   |
|        |                       |                         |                              |       | R/W                       |                           |                           |                           |                           |                           |
|        |                       |                         |                              |       | 0                         | 0                         | 0                         | 0                         | 0                         | 0                         |
|        |                       |                         |                              |       | 0: Micro DMA5<br>1: HDMA5 | 0: Micro DMA4<br>1: HDMA4 | 0: Micro DMA3<br>1: HDMA3 | 0: Micro DMA2<br>1: HDMA2 | 0: Micro DMA1<br>1: HDMA1 | 0: Micro DMA0<br>1: HDMA0 |

## (3) Memory controller (1/4)

| Symbol | Name                                 | Address | 7                                                                                                                                                                                                                                                                                     | 6                        | 5     | 4                                        | 3                                                                                                                                                                                                                                                                                     | 2     | 1                                                                            | 0      |
|--------|--------------------------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|-------|------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------------------------------------------------------------------------------|--------|
| B0CSL  | BLOCK0 CS/WAIT control register low  | 0140H   | B0WW3                                                                                                                                                                                                                                                                                 | B0WW2                    | B0WW1 | B0WW0                                    | B0WR3                                                                                                                                                                                                                                                                                 | B0WR2 | B0WR1                                                                        | B0WR0  |
|        |                                      |         | R/W                                                                                                                                                                                                                                                                                   |                          |       |                                          |                                                                                                                                                                                                                                                                                       |       |                                                                              |        |
|        |                                      |         | 0                                                                                                                                                                                                                                                                                     | 0                        | 1     | 0                                        | 0                                                                                                                                                                                                                                                                                     | 0     | 1                                                                            | 0      |
|        |                                      |         | Write waits                                                                                                                                                                                                                                                                           |                          |       |                                          | Read waits                                                                                                                                                                                                                                                                            |       |                                                                              |        |
|        |                                      |         | 0001: 0 waits 0010: 1 wait<br>0101: 2 waits 0110: 3 waits<br>0111: 4 waits 1000: 5 waits<br>1001: 6 waits 1010: 7 waits<br>1011: 8 waits 1100: 9 waits<br>1101: 10 waits 1110: 12 waits<br>1111: 16 waits 0100: 20 waits<br>0011: 6 states + WAIT pin input mode<br>Others: Reserved  |                          |       |                                          | 0001: 0 waits 0010: 1 wait<br>0101: 2 waits 0110: 3 waits<br>0111: 4 waits 1000: 5 waits<br>1001: 6 waits 1010: 7 waits<br>1011: 8 waits 1100: 9 waits<br>1101: 10 waits 1110: 12 waits<br>1111: 16 waits 0100: 20 waits<br>0011: 6 states + WAIT pin input mode<br>Others: Reserved  |       |                                                                              |        |
| B0CSH  | BLOCK0 CS/WAIT control register high | 0141H   | B0E                                                                                                                                                                                                                                                                                   |                          |       | B0REC                                    | B0OM1                                                                                                                                                                                                                                                                                 | B0OM0 | B0BUS1                                                                       | B0BUS0 |
|        |                                      |         | R/W                                                                                                                                                                                                                                                                                   |                          |       | R/W                                      |                                                                                                                                                                                                                                                                                       |       |                                                                              |        |
|        |                                      |         | 0                                                                                                                                                                                                                                                                                     |                          |       | 0                                        | 0                                                                                                                                                                                                                                                                                     | 0     | 0                                                                            | 0      |
|        |                                      |         | CS select<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                  |                          |       | Dummy cycle<br>0: No insert<br>1: Insert | 00: ROM/SRAM<br>01: Reserved<br>10: Reserved<br>11: Reserved                                                                                                                                                                                                                          |       | Data bus width<br>00: 8 bits<br>01: 16 bits<br>10: Reserved<br>11: Don't set |        |
|        |                                      |         |                                                                                                                                                                                                                                                                                       |                          |       |                                          |                                                                                                                                                                                                                                                                                       |       |                                                                              |        |
| B1CSL  | BLOCK1 CS/WAIT control register low  | 0144H   | B1WW3                                                                                                                                                                                                                                                                                 | B1WW2                    | B1WW1 | B1WW0                                    | B1WR3                                                                                                                                                                                                                                                                                 | B1WR2 | B1WR1                                                                        | B1WR0  |
|        |                                      |         | R/W                                                                                                                                                                                                                                                                                   |                          |       |                                          |                                                                                                                                                                                                                                                                                       |       |                                                                              |        |
|        |                                      |         | 0                                                                                                                                                                                                                                                                                     | 0                        | 1     | 0                                        | 0                                                                                                                                                                                                                                                                                     | 0     | 1                                                                            | 0      |
|        |                                      |         | Write waits                                                                                                                                                                                                                                                                           |                          |       |                                          | Read waits                                                                                                                                                                                                                                                                            |       |                                                                              |        |
|        |                                      |         | 0001: 0 waits 0010: 1 waits<br>0101: 2 waits 0110: 3 waits<br>0111: 4 waits 1000: 5 waits<br>1001: 6 waits 1010: 7 waits<br>1011: 8 waits 1100: 9 waits<br>1101: 10 waits 1110: 12 waits<br>1111: 16 waits 0100: 20 waits<br>0011: 6 states + WAIT pin input mode<br>Others: Reserved |                          |       |                                          | 0001: 0 waits 0010: 1 waits<br>0101: 2 waits 0110: 3 waits<br>0111: 4 waits 1000: 5 waits<br>1001: 6 waits 1010: 7 waits<br>1011: 8 waits 1100: 9 waits<br>1101: 10 waits 1110: 12 waits<br>1111: 16 waits 0100: 20 waits<br>0011: 6 states + WAIT pin input mode<br>Others: Reserved |       |                                                                              |        |
| B1CSH  | BLOCK1 CS/WAIT control register high | 0145H   | B1E                                                                                                                                                                                                                                                                                   |                          |       | B1REC                                    | B1OM1                                                                                                                                                                                                                                                                                 | B1OM0 | B1BUS1                                                                       | B1BUS0 |
|        |                                      |         | R/W                                                                                                                                                                                                                                                                                   |                          |       | R/W                                      |                                                                                                                                                                                                                                                                                       |       |                                                                              |        |
|        |                                      |         | 0                                                                                                                                                                                                                                                                                     |                          |       | 0                                        | 0                                                                                                                                                                                                                                                                                     | 0     | 0                                                                            | 0      |
|        |                                      |         | CS select<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                  |                          |       | Dummy cycle<br>0: No insert<br>1: Insert | 00: ROM/SRAM<br>01: Reserved<br>10: Reserved<br>11: SDRAM                                                                                                                                                                                                                             |       | Data bus width<br>00: 8 bits<br>01: 16 bits<br>10: Reserved<br>11: Don't set |        |
|        |                                      |         |                                                                                                                                                                                                                                                                                       |                          |       |                                          |                                                                                                                                                                                                                                                                                       |       |                                                                              |        |
| B2CSL  | BLOCK2 CS/WAIT control register low  | 0148H   | B2WW3                                                                                                                                                                                                                                                                                 | B2WW2                    | B2WW1 | B2WW0                                    | B2WR3                                                                                                                                                                                                                                                                                 | B2WR2 | B2WR1                                                                        | B2WR0  |
|        |                                      |         | R/W                                                                                                                                                                                                                                                                                   |                          |       |                                          |                                                                                                                                                                                                                                                                                       |       |                                                                              |        |
|        |                                      |         | 0                                                                                                                                                                                                                                                                                     | 0                        | 1     | 0                                        | 0                                                                                                                                                                                                                                                                                     | 0     | 1                                                                            | 0      |
|        |                                      |         | Write waits                                                                                                                                                                                                                                                                           |                          |       |                                          | Read waits                                                                                                                                                                                                                                                                            |       |                                                                              |        |
|        |                                      |         | 0001: 0 waits 0010: 1 waits<br>0101: 2 waits 0110: 3 waits<br>0111: 4 waits 1000: 5 waits<br>1001: 6 waits 1010: 7 waits<br>1011: 8 waits 1100: 9 waits<br>1101: 10 waits 1110: 12 waits<br>1111: 16 waits 0100: 20 waits<br>0011: 6 states + WAIT pin input mode<br>Others: Reserved |                          |       |                                          | 0001: 0 waits 0010: 1 waits<br>0101: 2 waits 0110: 3 waits<br>0111: 4 waits 1000: 5 waits<br>1001: 6 waits 1010: 7 waits<br>1011: 8 waits 1100: 9 waits<br>1101: 10 waits 1110: 12 waits<br>1111: 16 waits 0100: 20 waits<br>0011: 6 states + WAIT pin input mode<br>Others: Reserved |       |                                                                              |        |
| B2CSH  | BLOCK2 CS/WAIT control register high | 0149H   | B2E                                                                                                                                                                                                                                                                                   | B2M                      |       | B2REC                                    | B2OM1                                                                                                                                                                                                                                                                                 | B2OM0 | B2BUS1                                                                       | B2BUS0 |
|        |                                      |         | R/W                                                                                                                                                                                                                                                                                   |                          |       | R/W                                      |                                                                                                                                                                                                                                                                                       |       |                                                                              |        |
|        |                                      |         | 1                                                                                                                                                                                                                                                                                     | 0                        |       | 0                                        | 0                                                                                                                                                                                                                                                                                     | 0     | 0                                                                            | 1      |
|        |                                      |         | CS select<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                  | 0: 16 MB<br>1: Sets area |       | Dummy cycle<br>0: No insert<br>1: Insert | 00: ROM/SRAM<br>01: Reserved<br>10: Reserved<br>11: SDRAM                                                                                                                                                                                                                             |       | Data bus width<br>00: 8 bits<br>01: 16 bits<br>10: Reserved<br>11: Don't set |        |
|        |                                      |         |                                                                                                                                                                                                                                                                                       |                          |       |                                          |                                                                                                                                                                                                                                                                                       |       |                                                                              |        |

## (3) Memory controller (2/4)

| Symbol | Name                                               | Address | 7                                                                                                                                                                                                                                                                                                         | 6      | 5      | 4                                              | 3                                                                                                                                                                                                                                                                                                         | 2      | 1                                                                            | 0       |
|--------|----------------------------------------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------------------------------------------------------------------------------|---------|
| B3CSL  | BLOCK3<br>CS/WAIT<br>control<br>register<br>low    | 014CH   | B3WW3                                                                                                                                                                                                                                                                                                     | B3WW2  | B3WW1  | B3WW0                                          | B3WR3                                                                                                                                                                                                                                                                                                     | B3WR2  | B3WR1                                                                        | B3WR0   |
|        |                                                    |         | R/W                                                                                                                                                                                                                                                                                                       |        |        |                                                |                                                                                                                                                                                                                                                                                                           |        |                                                                              |         |
|        |                                                    |         | 0                                                                                                                                                                                                                                                                                                         | 0      | 1      | 0                                              | 0                                                                                                                                                                                                                                                                                                         | 0      | 1                                                                            | 0       |
|        |                                                    |         | Write waits                                                                                                                                                                                                                                                                                               |        |        |                                                | Read waits                                                                                                                                                                                                                                                                                                |        |                                                                              |         |
|        |                                                    |         | 0001: 0 waits 0010: 1 waits<br>0101: 2 waits 0110: 3 waits<br>0111: 4 waits 1000: 5 waits<br>1001: 6 waits 1010: 7 waits<br>1011: 8 waits 1100: 9 waits<br>1101: 10 waits 1110: 12 waits<br>1111: 16 waits 0100: 20 waits<br>0011: 6 states + $\overline{\text{WAIT}}$ pin input mode<br>Others: Reserved |        |        |                                                | 0001: 0 waits 0010: 1 waits<br>0101: 2 waits 0110: 3 waits<br>0111: 4 waits 1000: 5 waits<br>1001: 6 waits 1010: 7 waits<br>1011: 8 waits 1100: 9 waits<br>1101: 10 waits 1110: 12 waits<br>1111: 16 waits 0100: 20 waits<br>0011: 6 states + $\overline{\text{WAIT}}$ pin input mode<br>Others: Reserved |        |                                                                              |         |
| B3CSH  | BLOCK3<br>CS/WAIT<br>control<br>register<br>high   | 014DH   | B3E                                                                                                                                                                                                                                                                                                       |        |        | B3REC                                          | B3OM1                                                                                                                                                                                                                                                                                                     | B3OM0  | B3BUS1                                                                       | B3BUS0  |
|        |                                                    |         | R/W                                                                                                                                                                                                                                                                                                       |        |        | R/W                                            |                                                                                                                                                                                                                                                                                                           |        |                                                                              |         |
|        |                                                    |         | 0                                                                                                                                                                                                                                                                                                         |        |        | 0                                              | 0                                                                                                                                                                                                                                                                                                         | 0      | 0                                                                            | 0       |
|        |                                                    |         | CS select<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                      |        |        | Dummy<br>cycle<br>0: No<br>insert<br>1: Insert | 00: ROM/SRAM<br>01: Reserved<br>10: Reserved<br>11: Reserved                                                                                                                                                                                                                                              |        | Data bus width<br>00: 8 bits<br>01: 16 bits<br>10: Reserved<br>11: Don't set |         |
| BEXCSL | BLOCK EX<br>CS/WAIT<br>control<br>register<br>low  | 0158H   | BEXWW3                                                                                                                                                                                                                                                                                                    | BEXWW2 | BEXWW1 | BEXWW0                                         | BEXWR3                                                                                                                                                                                                                                                                                                    | BEXWR2 | BEXWR1                                                                       | BEXWR0  |
|        |                                                    |         | R/W                                                                                                                                                                                                                                                                                                       |        |        |                                                |                                                                                                                                                                                                                                                                                                           |        |                                                                              |         |
|        |                                                    |         | 0                                                                                                                                                                                                                                                                                                         | 0      | 1      | 0                                              | 0                                                                                                                                                                                                                                                                                                         | 0      | 1                                                                            | 0       |
|        |                                                    |         | Write waits                                                                                                                                                                                                                                                                                               |        |        |                                                | Read waits                                                                                                                                                                                                                                                                                                |        |                                                                              |         |
|        |                                                    |         | 0001: 0 waits 0010: 1 waits<br>0101: 2 waits 0110: 3 waits<br>0111: 4 waits 1000: 5 waits<br>1001: 6 waits 1010: 7 waits<br>1011: 8 waits 1100: 9 waits<br>1101: 10 waits 1110: 12 waits<br>1111: 16 waits 0100: 20 waits<br>0011: 6 states + $\overline{\text{WAIT}}$ pin input mode<br>Others: Reserved |        |        |                                                | 0001: 0 waits 0010: 1 waits<br>0101: 2 waits 0110: 3 waits<br>0111: 4 waits 1000: 5 waits<br>1001: 6 waits 1010: 7 waits<br>1011: 8 waits 1100: 9 waits<br>1101: 10 waits 1110: 12 waits<br>1111: 16 waits 0100: 20 waits<br>0011: 6 states + $\overline{\text{WAIT}}$ pin input mode<br>Others: Reserved |        |                                                                              |         |
| BEXCSH | BLOCK EX<br>CS/WAIT<br>control<br>register<br>high | 0159H   |                                                                                                                                                                                                                                                                                                           |        |        | BEXREC                                         | BEXOM1                                                                                                                                                                                                                                                                                                    | BEXOM0 | BEXBUS1                                                                      | BEXBUS0 |
|        |                                                    |         |                                                                                                                                                                                                                                                                                                           |        |        | R/W                                            |                                                                                                                                                                                                                                                                                                           |        |                                                                              |         |
|        |                                                    |         |                                                                                                                                                                                                                                                                                                           |        |        | 0                                              | 0                                                                                                                                                                                                                                                                                                         | 0      | 0                                                                            | 0       |
|        |                                                    |         |                                                                                                                                                                                                                                                                                                           |        |        | Dummy<br>cycle<br>0: No<br>insert<br>1: Insert | 00: ROM/SRAM<br>01: Reserved<br>10: Reserved<br>11: Reserved                                                                                                                                                                                                                                              |        | Data bus width<br>00: 8 bits<br>01: 16 bits<br>10: Reserved<br>11: Don't set |         |



## (3) Memory controller (3/4)

| Symbol | Name                            | Address | 7                                    | 6     | 5     | 4     | 3     | 2     | 1       | 0     |
|--------|---------------------------------|---------|--------------------------------------|-------|-------|-------|-------|-------|---------|-------|
| MAMR0  | Memory address mask register 0  | 0142H   | M0V20                                | M0V19 | M0V18 | M0V17 | M0V16 | M0V15 | M0V14-9 | M0V8  |
|        |                                 |         | R/W                                  |       |       |       |       |       |         |       |
|        |                                 |         | 1                                    | 1     | 1     | 1     | 1     | 1     | 1       | 1     |
|        |                                 |         | 0: Compare enable 1: Compare disable |       |       |       |       |       |         |       |
| MSAR0  | Memory start address register 0 | 0143H   | M0S23                                | M0S22 | M0S21 | M0S20 | M0S19 | M0S18 | M0S17   | M0S16 |
|        |                                 |         | R/W                                  |       |       |       |       |       |         |       |
|        |                                 |         | 1                                    | 1     | 1     | 1     | 1     | 1     | 1       | 1     |
|        |                                 |         | Set start address A23 to A16         |       |       |       |       |       |         |       |
| MAMR1  | Memory address mask register 1  | 0146H   | M1V21                                | M1V20 | M1V19 | M1V18 | M1V17 | M1V16 | M1V15-9 | M1V8  |
|        |                                 |         | R/W                                  |       |       |       |       |       |         |       |
|        |                                 |         | 1                                    | 1     | 1     | 1     | 1     | 1     | 1       | 1     |
|        |                                 |         | 0: Compare enable 1: Compare disable |       |       |       |       |       |         |       |
| MSAR1  | Memory start address register 1 | 0147H   | M1S23                                | M1S22 | M1S21 | M1S20 | M1S19 | M1S18 | M1S17   | M1S16 |
|        |                                 |         | R/W                                  |       |       |       |       |       |         |       |
|        |                                 |         | 1                                    | 1     | 1     | 1     | 1     | 1     | 1       | 1     |
|        |                                 |         | Set start address A23 to A16         |       |       |       |       |       |         |       |
| MAMR2  | Memory address mask register 2  | 014AH   | M2V22                                | M2V21 | M2V20 | M2V19 | M2V18 | M2V17 | M2V16   | M2V15 |
|        |                                 |         | R/W                                  |       |       |       |       |       |         |       |
|        |                                 |         | 1                                    | 1     | 1     | 1     | 1     | 1     | 1       | 1     |
|        |                                 |         | 0: Compare enable 1: Compare disable |       |       |       |       |       |         |       |
| MSAR2  | Memory start address register 2 | 014BH   | M2S23                                | M2S22 | M2S21 | M2S20 | M2S19 | M2S18 | M2S17   | M2S16 |
|        |                                 |         | R/W                                  |       |       |       |       |       |         |       |
|        |                                 |         | 1                                    | 1     | 1     | 1     | 1     | 1     | 1       | 1     |
|        |                                 |         | Set start address A23 to A16         |       |       |       |       |       |         |       |
| MAMR3  | Memory address mask register 3  | 014EH   | M3V22                                | M3V21 | M3V20 | M3V19 | M3V18 | M3V17 | M3V16   | M3V15 |
|        |                                 |         | R/W                                  |       |       |       |       |       |         |       |
|        |                                 |         | 1                                    | 1     | 1     | 1     | 1     | 1     | 1       | 1     |
|        |                                 |         | 0: Compare enable 1: Compare disable |       |       |       |       |       |         |       |
| MSAR3  | Memory start address register 3 | 014FH   | M3S23                                | M3S22 | M3S21 | M3S20 | M3S19 | M3S18 | M3S17   | M3S16 |
|        |                                 |         | R/W                                  |       |       |       |       |       |         |       |
|        |                                 |         | 1                                    | 1     | 1     | 1     | 1     | 1     | 1       | 1     |
|        |                                 |         | Set start address A23 to A16         |       |       |       |       |       |         |       |

## (3) Memory controller (4/4)

| Symbol   | Name                                | Address | 7                                                                                                                                                   | 6       | 5                                                                                                                                           | 4                                          | 3                                                                                                                                                   | 2                                                                                    | 1                                                                                                                                                   | 0                |
|----------|-------------------------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| PMEMCR   | Page ROM control register           | 0166H   |                                                                                                                                                     |         |                                                                                                                                             | OPGE                                       | OPWR1                                                                                                                                               | OPWR0                                                                                | PR1                                                                                                                                                 | PR0              |
|          |                                     |         |                                                                                                                                                     |         |                                                                                                                                             | R/W                                        |                                                                                                                                                     |                                                                                      |                                                                                                                                                     |                  |
|          |                                     |         |                                                                                                                                                     |         |                                                                                                                                             | 0                                          | 0                                                                                                                                                   | 0                                                                                    | 1                                                                                                                                                   | 0                |
|          |                                     |         |                                                                                                                                                     |         |                                                                                                                                             | ROM page access<br>0: Disable<br>1: Enable | Wait number on page<br>00: 1 CLK (n-1-1-1 mode)<br>01: 2 CLK (n-2-2-2 mode)<br>10: 3 CLK (n-3-3-3 mode)<br>11: Reserved                             | Byte number in a page<br>00: 64 bytes<br>01: 32 bytes<br>10: 16 bytes<br>11: 8 bytes |                                                                                                                                                     |                  |
| CSTMGCR  | Adjust for Timing of control signal | 0168H   |                                                                                                                                                     |         | TACSEL1                                                                                                                                     | TACSEL0                                    |                                                                                                                                                     |                                                                                      | TAC1                                                                                                                                                | TAC0             |
|          |                                     |         |                                                                                                                                                     |         | R/W                                                                                                                                         |                                            |                                                                                                                                                     |                                                                                      | R/W                                                                                                                                                 |                  |
|          |                                     |         |                                                                                                                                                     |         | 0                                                                                                                                           | 0                                          |                                                                                                                                                     |                                                                                      | 0                                                                                                                                                   | 0                |
|          |                                     |         |                                                                                                                                                     |         | Select area to change timing<br>00:CS0 01:CS1<br>10:CS2 11:CS3                                                                              |                                            |                                                                                                                                                     |                                                                                      | Select delay time(TAC)<br>00:0 × 1/f <sub>sys</sub><br>01:1 × 1/f <sub>sys</sub><br>10:2 × 1/f <sub>sys</sub><br>11:Reserved                        |                  |
| WRTMGCR  | Adjust for Timing of control signal | 0169H   |                                                                                                                                                     |         | TCWSEL1                                                                                                                                     | TCWSEL0                                    | TCWS1                                                                                                                                               | TCWS0                                                                                | TCWH1                                                                                                                                               | TCWH0            |
|          |                                     |         |                                                                                                                                                     |         | R/W                                                                                                                                         |                                            |                                                                                                                                                     |                                                                                      |                                                                                                                                                     |                  |
|          |                                     |         |                                                                                                                                                     |         | 0                                                                                                                                           | 0                                          | 0                                                                                                                                                   | 0                                                                                    | 0                                                                                                                                                   | 0                |
|          |                                     |         |                                                                                                                                                     |         | Select area to change timing<br>00:CS0 01:CS1<br>10:CS2 11:CS3                                                                              |                                            | Select delay time(TCWS)<br>00:0.5 × 1/f <sub>sys</sub><br>01:1.5 × 1/f <sub>sys</sub><br>10:2.5 × 1/f <sub>sys</sub><br>11:3.5 × 1/f <sub>sys</sub> |                                                                                      | Select delay time(TCWH)<br>00:0.5 × 1/f <sub>sys</sub><br>01:1.5 × 1/f <sub>sys</sub><br>10:2.5 × 1/f <sub>sys</sub><br>11:3.5 × 1/f <sub>sys</sub> |                  |
| RDTMGCR0 | Adjust for Timing of control signal | 016AH   | B1TCRS1                                                                                                                                             | B1TCRS0 | B1TCRH1                                                                                                                                     | B1TCRH0                                    | B0TCRS1                                                                                                                                             | B0TCRS0                                                                              | B0TCRH1                                                                                                                                             | B0TCRH0          |
|          |                                     |         | R/W                                                                                                                                                 |         |                                                                                                                                             |                                            |                                                                                                                                                     |                                                                                      |                                                                                                                                                     |                  |
|          |                                     |         | 0                                                                                                                                                   | 0       | 0                                                                                                                                           | 0                                          | 0                                                                                                                                                   | 0                                                                                    | 0                                                                                                                                                   | 0                |
|          |                                     |         | Select delay time(TCRS)<br>00:0.5 × 1/f <sub>sys</sub><br>01:1.5 × 1/f <sub>sys</sub><br>10:2.5 × 1/f <sub>sys</sub><br>11:3.5 × 1/f <sub>sys</sub> |         | Select delay time(TCRH)<br>00:0 × 1/f <sub>sys</sub><br>01:1 × 1/f <sub>sys</sub><br>10:2 × 1/f <sub>sys</sub><br>11:3 × 1/f <sub>sys</sub> |                                            | Select delay time(TCRS)<br>00:0.5 × 1/f <sub>sys</sub><br>01:1.5 × 1/f <sub>sys</sub><br>10:2.5 × 1/f <sub>sys</sub><br>11:3.5 × 1/f <sub>sys</sub> |                                                                                      | Select delay time(TCRH)<br>00:0 × 1/f <sub>sys</sub><br>01:1 × 1/f <sub>sys</sub><br>10:2 × 1/f <sub>sys</sub><br>11:3 × 1/f <sub>sys</sub>         |                  |
| RDTMGCR1 | Adjust for Timing of control signal | 016BH   | B3TCRS1                                                                                                                                             | B3TCRS0 | B3TCRH1                                                                                                                                     | B3TCRH0                                    | B2TCRS1                                                                                                                                             | B2TCRS0                                                                              | B2TCRH1                                                                                                                                             | B2TCRH0          |
|          |                                     |         | R/W                                                                                                                                                 |         |                                                                                                                                             |                                            |                                                                                                                                                     |                                                                                      |                                                                                                                                                     |                  |
|          |                                     |         | 0                                                                                                                                                   | 0       | 0                                                                                                                                           | 0                                          | 0                                                                                                                                                   | 0                                                                                    | 0                                                                                                                                                   | 0                |
|          |                                     |         | Select delay time(TCRS)<br>00:0.5 × 1/f <sub>sys</sub><br>01:1.5 × 1/f <sub>sys</sub><br>10:2.5 × 1/f <sub>sys</sub><br>11:3.5 × 1/f <sub>sys</sub> |         | Select delay time(TCRH)<br>00:0 × 1/f <sub>sys</sub><br>01:1 × 1/f <sub>sys</sub><br>10:2 × 1/f <sub>sys</sub><br>11:3 × 1/f <sub>sys</sub> |                                            | Select delay time(TCRS)<br>00:0.5 × 1/f <sub>sys</sub><br>01:1.5 × 1/f <sub>sys</sub><br>10:2.5 × 1/f <sub>sys</sub><br>11:3.5 × 1/f <sub>sys</sub> |                                                                                      | Select delay time(TCRH)<br>00:0 × 1/f <sub>sys</sub><br>01:1 × 1/f <sub>sys</sub><br>10:2 × 1/f <sub>sys</sub><br>11:3 × 1/f <sub>sys</sub>         |                  |
| BROMCR   | Boot Rom Control register           | 016CH   |                                                                                                                                                     |         |                                                                                                                                             |                                            |                                                                                                                                                     | CSDIS                                                                                | –                                                                                                                                                   | –                |
|          |                                     |         |                                                                                                                                                     |         |                                                                                                                                             |                                            |                                                                                                                                                     | R/W                                                                                  |                                                                                                                                                     |                  |
|          |                                     |         |                                                                                                                                                     |         |                                                                                                                                             |                                            |                                                                                                                                                     | 1                                                                                    | 1                                                                                                                                                   | 0                |
|          |                                     |         |                                                                                                                                                     |         |                                                                                                                                             |                                            |                                                                                                                                                     | Nand-Flash Area CS Output<br>0:enable<br>1:disable                                   | Always write "1"                                                                                                                                    | Always write "0" |
| RAMCR    | RAM Control register                | 016DH   |                                                                                                                                                     |         |                                                                                                                                             |                                            |                                                                                                                                                     |                                                                                      |                                                                                                                                                     | –                |
|          |                                     |         |                                                                                                                                                     |         |                                                                                                                                             |                                            |                                                                                                                                                     |                                                                                      |                                                                                                                                                     | R/W              |
|          |                                     |         |                                                                                                                                                     |         |                                                                                                                                             |                                            |                                                                                                                                                     |                                                                                      |                                                                                                                                                     | 1                |
|          |                                     |         |                                                                                                                                                     |         |                                                                                                                                             |                                            |                                                                                                                                                     |                                                                                      |                                                                                                                                                     | Always write "1" |

## (4) TSI

| Symbol | Name                  | Address | 7                                                                                                                               | 6                                                           | 5                                              | 4                                                 | 3                      | 2                      | 1                      | 0                      |
|--------|-----------------------|---------|---------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------|------------------------------------------------|---------------------------------------------------|------------------------|------------------------|------------------------|------------------------|
| TSICR0 | TSI control register0 | 01F0H   | TSI7                                                                                                                            | INGE                                                        | PTST                                           | TWIEN                                             | PYEN                   | PXEN                   | MYEN                   | MXEN                   |
|        |                       |         | R/W                                                                                                                             |                                                             | R                                              | R/W                                               |                        |                        |                        |                        |
|        |                       |         | 0                                                                                                                               | 0                                                           | 0                                              | 0                                                 | 0                      | 0                      | 0                      | 0                      |
|        |                       |         | 0: Disable<br>1: Enable                                                                                                         | Input gate control of Port 96,97<br>0: Enable<br>1: Disable | Detection condition<br>0: no touch<br>1: touch | INT4 interrupt control<br>0: Disable<br>1: Enable | SPY<br>0: OFF<br>1: ON | SPX<br>0: OFF<br>1: ON | SMY<br>0: OFF<br>1: ON | SMX<br>0: OFF<br>1: ON |
|        |                       |         |                                                                                                                                 |                                                             |                                                |                                                   |                        |                        |                        |                        |
| TSICR1 | TSI control register1 | 01F1H   | DBC7                                                                                                                            | DB1024                                                      | DB256                                          | DB64                                              | DB8                    | DB4                    | DB2                    | DB1                    |
|        |                       |         | R/W                                                                                                                             |                                                             |                                                |                                                   |                        |                        |                        |                        |
|        |                       |         | 0                                                                                                                               | 0                                                           | 0                                              | 0                                                 | 0                      | 0                      | 0                      | 0                      |
|        |                       |         | 0: Disable<br>1: Enable                                                                                                         | 1024                                                        | 256                                            | 64                                                | 8                      | 4                      | 2                      | 1                      |
|        |                       |         | De-bounce time is set by "(N*64-16) / f <sub>sys</sub> "-formula.<br>"N" is sum of number which is set to "1" in bit6 to bit 0. |                                                             |                                                |                                                   |                        |                        |                        |                        |

## (5) SDRAM controller

| Symbol | Name                                    | Address | 7                                                   | 6                            | 5                                                                                                       | 4                                                          | 3                                                                                                                                                                       | 2                                                                                                                                                                                                                                                                                                      | 1         | 0                                               |
|--------|-----------------------------------------|---------|-----------------------------------------------------|------------------------------|---------------------------------------------------------------------------------------------------------|------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------------------------------------------------|
| SDACR  | SDRAM access control register           | 0250H   | SRDS                                                | –                            | SMUXW1                                                                                                  | SMUXW0                                                     | SPRE                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                        |           | SMAC                                            |
|        |                                         |         | R/W                                                 |                              |                                                                                                         |                                                            |                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                        |           | R/W                                             |
|        |                                         |         | 1                                                   | 0                            | 0                                                                                                       | 0                                                          | 0                                                                                                                                                                       |                                                                                                                                                                                                                                                                                                        |           | 0                                               |
|        |                                         |         | Read data shift function<br>0: Disable<br>1: Enable | Always write "0"             | Address multiplex type<br>00: Type A (A9- )<br>01: Type B (A10- )<br>10: Type C (A11- )<br>11: Reserved |                                                            | Read/Write commands<br><br>0: Without auto pre-charge<br>1: With auto precharge                                                                                         |                                                                                                                                                                                                                                                                                                        |           | SDRAM controller<br><br>0: Disable<br>1: Enable |
| SDCISR | SDRAM Command Interval Setting Register | 0251H   |                                                     | STMRD                        | STWR                                                                                                    | STRP                                                       | STRCD                                                                                                                                                                   | STRC2                                                                                                                                                                                                                                                                                                  | STRC1     | STRC0                                           |
|        |                                         |         |                                                     | R/W                          |                                                                                                         |                                                            |                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                        |           |                                                 |
|        |                                         |         |                                                     | 1                            | 1                                                                                                       | 1                                                          | 1                                                                                                                                                                       | 1                                                                                                                                                                                                                                                                                                      | 0         | 0                                               |
|        |                                         |         |                                                     | TMRD<br>0: 1 CLK<br>1: 2 CLK | TWR<br>0: 1 CLK<br>1: 2 CLK                                                                             | TRP<br>0: 1 CLK<br>1: 2 CLK                                | TRCD<br>0: 1 CLK<br>1: 2 CLK                                                                                                                                            | TRC<br>000: 1 CLK    100: 5 CLK<br>001: 2 CLK    101: 6 CLK<br>010: 3 CLK    110: 7 CLK<br>011: 4 CLK    111: 8 CLK                                                                                                                                                                                    |           |                                                 |
| SDRCR  | SDRAM refresh control register          | 0252H   | –                                                   |                              |                                                                                                         | SSAE                                                       | SRS2                                                                                                                                                                    | SRS1                                                                                                                                                                                                                                                                                                   | SRS0      | SRC                                             |
|        |                                         |         | R/W                                                 |                              |                                                                                                         | R/W                                                        |                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                        |           |                                                 |
|        |                                         |         | 0                                                   |                              |                                                                                                         | 1                                                          | 0                                                                                                                                                                       | 0                                                                                                                                                                                                                                                                                                      | 0         | 0                                               |
|        |                                         |         | Always write "0"                                    |                              |                                                                                                         | Self Refresh auto exit function<br>0: Disable<br>1: Enable | Refresh interval<br>000: 47 states    100: 468 states<br>001: 78 states    101: 624 states<br>010: 156 states    110: 936 states<br>011: 312 states    111: 1248 states |                                                                                                                                                                                                                                                                                                        |           | Auto Refresh<br><br>0: Disable<br>1: Enable     |
| SDCMM  | SDRAM command register                  | 0253H   |                                                     |                              |                                                                                                         |                                                            |                                                                                                                                                                         | SCMM2                                                                                                                                                                                                                                                                                                  | SCMM1     | SCMM0                                           |
|        |                                         |         |                                                     |                              |                                                                                                         |                                                            |                                                                                                                                                                         | R/W                                                                                                                                                                                                                                                                                                    |           |                                                 |
|        |                                         |         |                                                     |                              |                                                                                                         |                                                            |                                                                                                                                                                         | 0                                                                                                                                                                                                                                                                                                      | 0         | 0                                               |
|        |                                         |         |                                                     |                              |                                                                                                         |                                                            |                                                                                                                                                                         | Command issue<br>000: Don't care<br>001: Initialization sequence<br>a. Precharge All command<br>b. Eight Auto Refresh commands<br>c. Mode Register Set command<br>010: Precharge All command<br>100: Reserved<br>101: Self Refresh Entry command<br>110: Self Refresh Exit command<br>Others: Reserved |           |                                                 |
| SDBLS  | SDRAM HDRAM burst length register       | 0254H   |                                                     |                              | SDBL5                                                                                                   | SDBL4                                                      | SDBL3                                                                                                                                                                   | SDBL2                                                                                                                                                                                                                                                                                                  | SDBL1     | SDBL0                                           |
|        |                                         |         |                                                     |                              |                                                                                                         |                                                            |                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                        |           |                                                 |
|        |                                         |         |                                                     |                              | 0                                                                                                       | 0                                                          | 0                                                                                                                                                                       | 0                                                                                                                                                                                                                                                                                                      | 0         | 0                                               |
|        |                                         |         |                                                     |                              | For HDMA5                                                                                               | For HDMA4                                                  | For HDMA3                                                                                                                                                               | For HDMA2                                                                                                                                                                                                                                                                                              | For HDMA1 | For HDMA0                                       |
|        |                                         |         |                                                     |                              | HDMA burst length<br>0: 1 Word Read / Single Write<br>1: Full Page Read / Burst Write                   |                                                            |                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                        |           |                                                 |

## (6) USB controller (1/6)

| Symbol            | Name                        | Address | 7         | 6         | 5          | 4          | 3          | 2         | 1         | 0         |
|-------------------|-----------------------------|---------|-----------|-----------|------------|------------|------------|-----------|-----------|-----------|
| Descriptor RAM0   | Descriptor RAM 0 register   | 0500H   | D7        | D6        | D5         | D4         | D3         | D2        | D1        | D0        |
|                   |                             |         | R/W       |           |            |            |            |           |           |           |
|                   |                             |         | Undefined | Undefined | Undefined  | Undefined  | Undefined  | Undefined | Undefined | Undefined |
| Descriptor RAM1   | Descriptor RAM 1 register   | 0501H   | D7        | D6        | D5         | D4         | D3         | D2        | D1        | D0        |
|                   |                             |         | R/W       |           |            |            |            |           |           |           |
|                   |                             |         | Undefined | Undefined | Undefined  | Undefined  | Undefined  | Undefined | Undefined | Undefined |
| Descriptor RAM2   | Descriptor RAM 2 register   | 0502H   | D7        | D6        | D5         | D4         | D3         | D2        | D1        | D0        |
|                   |                             |         | R/W       |           |            |            |            |           |           |           |
|                   |                             |         | Undefined | Undefined | Undefined  | Undefined  | Undefined  | Undefined | Undefined | Undefined |
| Descriptor RAM3   | Descriptor RAM 3 register   | 0503H   | D7        | D6        | D5         | D4         | D3         | D2        | D1        | D0        |
|                   |                             |         | R/W       |           |            |            |            |           |           |           |
|                   |                             |         | Undefined | Undefined | Undefined  | Undefined  | Undefined  | Undefined | Undefined | Undefined |
| :                 | :                           | :       | :         |           |            |            |            |           |           |           |
| Descriptor RAM381 | Descriptor RAM 381 register | 067DH   | D7        | D6        | D5         | D4         | D3         | D2        | D1        | D0        |
|                   |                             |         | R/W       |           |            |            |            |           |           |           |
|                   |                             |         | Undefined | Undefined | Undefined  | Undefined  | Undefined  | Undefined | Undefined | Undefined |
| Descriptor RAM382 | Descriptor RAM 382 register | 067EH   | D7        | D6        | D5         | D4         | D3         | D2        | D1        | D0        |
|                   |                             |         | R/W       |           |            |            |            |           |           |           |
|                   |                             |         | Undefined | Undefined | Undefined  | Undefined  | Undefined  | Undefined | Undefined | Undefined |
| Descriptor RAM383 | Descriptor RAM 383 register | 067FH   | D7        | D6        | D5         | D4         | D3         | D2        | D1        | D0        |
|                   |                             |         | R/W       |           |            |            |            |           |           |           |
|                   |                             |         | Undefined | Undefined | Undefined  | Undefined  | Undefined  | Undefined | Undefined | Undefined |
| Endpoint0         | Endpoint 0 register         | 0780H   | EP0_DATA7 | EP0_DATA6 | EP0_DATA5  | EP0_DATA4  | EP0_DATA3  | EP0_DATA2 | EP0_DATA1 | EP0_DATA0 |
|                   |                             |         | R/W       |           |            |            |            |           |           |           |
|                   |                             |         | Undefined | Undefined | Undefined  | Undefined  | Undefined  | Undefined | Undefined | Undefined |
| Endpoint1         | Endpoint 1 register         | 0781H   | EP1_DATA7 | EP1_DATA6 | EP1_DATA5  | EP1_DATA4  | EP1_DATA3  | EP1_DATA2 | EP1_DATA1 | EP1_DATA0 |
|                   |                             |         | R/W       |           |            |            |            |           |           |           |
|                   |                             |         | Undefined | Undefined | Undefined  | Undefined  | Undefined  | Undefined | Undefined | Undefined |
| Endpoint2         | Endpoint 2 register         | 0782H   | EP2_DATA7 | EP2_DATA6 | EP2_DATA5  | EP2_DATA4  | EP2_DATA3  | EP2_DATA2 | EP2_DATA1 | EP2_DATA0 |
|                   |                             |         | R/W       |           |            |            |            |           |           |           |
|                   |                             |         | Undefined | Undefined | Undefined  | Undefined  | Undefined  | Undefined | Undefined | Undefined |
| Endpoint3         | Endpoint 3 register         | 0783H   | EP3_DATA7 | EP3_DATA6 | EP3_DATA5  | EP3_DATA4  | EP3_DATA3  | EP3_DATA2 | EP3_DATA1 | EP3_DATA0 |
|                   |                             |         | R/W       |           |            |            |            |           |           |           |
|                   |                             |         | Undefined | Undefined | Undefined  | Undefined  | Undefined  | Undefined | Undefined | Undefined |
| EP1_MODE          | Endpoint 1 mode register    | 0789H   |           |           | Payload[2] | Payload[1] | Payload[0] | Mode[1]   | Mode[0]   | Direction |
|                   |                             |         | R/W       |           |            |            |            |           |           |           |
|                   |                             |         |           |           | 0          | 0          | 0          | 0         | 0         | 0         |
| EP2_MODE          | Endpoint 2 mode register    | 078AH   |           |           | Payload[2] | Payload[1] | Payload[0] | Mode[1]   | Mode[0]   | Direction |
|                   |                             |         | R/W       |           |            |            |            |           |           |           |
|                   |                             |         |           |           | 0          | 0          | 0          | 0         | 0         | 0         |
| EP3_MODE          | Endpoint 3 mode register    | 078BH   |           |           | Payload[2] | Payload[1] | Payload[0] | Mode[1]   | Mode[0]   | Direction |
|                   |                             |         | R/W       |           |            |            |            |           |           |           |
|                   |                             |         |           |           | 0          | 0          | 0          | 0         | 0         | 0         |

## (6) USB controller (2/6)

| Symbol       | Name                            | Address | 7          | 6         | 5         | 4         | 3         | 2         | 1            | 0         |
|--------------|---------------------------------|---------|------------|-----------|-----------|-----------|-----------|-----------|--------------|-----------|
| EP0_STATUS   | Endpoint 0 status register      | 0790H   |            | TOGGLE    | SUSPEND   | STATUS[2] | STATUS[1] | STATUS[0] | FIFO_DISABLE | STAGE_ERR |
|              |                                 |         |            | R         |           |           |           |           |              |           |
|              |                                 |         |            | 0         | 0         | 1         | 1         | 1         | 0            | 0         |
| EP1_STATUS   | Endpoint 1 status register      | 0791H   |            | TOGGLE    | SUSPEND   | STATUS[2] | STATUS[1] | STATUS[0] | FIFO_DISABLE | STAGE_ERR |
|              |                                 |         |            | R         |           |           |           |           |              |           |
|              |                                 |         |            | 0         | 0         | 1         | 1         | 1         | 0            | 0         |
| EP2_STATUS   | Endpoint 2 status register      | 0792H   |            | TOGGLE    | SUSPEND   | STATUS[2] | STATUS[1] | STATUS[0] | FIFO_DISABLE | STAGE_ERR |
|              |                                 |         |            | R         |           |           |           |           |              |           |
|              |                                 |         |            | 0         | 0         | 1         | 1         | 1         | 0            | 0         |
| EP3_STATUS   | Endpoint 3 status register      | 0793H   |            | TOGGLE    | SUSPEND   | STATUS[2] | STATUS[1] | STATUS[0] | FIFO_DISABLE | STAGE_ERR |
|              |                                 |         |            | R         |           |           |           |           |              |           |
|              |                                 |         |            | 0         | 0         | 1         | 1         | 1         | 0            | 0         |
| EP0_SIZE_L_A | Endpoint 0 size register Low A  | 0798H   | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1    | DATASIZE0 |
|              |                                 |         |            | R         |           |           |           |           |              |           |
|              |                                 |         | 1          | 0         | 0         | 0         | 1         | 0         | 0            | 0         |
| EP1_SIZE_L_A | Endpoint 0 size register Low A  | 0799H   | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1    | DATASIZE0 |
|              |                                 |         |            | R         |           |           |           |           |              |           |
|              |                                 |         | 1          | 0         | 0         | 0         | 1         | 0         | 0            | 0         |
| EP2_SIZE_L_A | Endpoint 2 size register Low A  | 079AH   | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1    | DATASIZE0 |
|              |                                 |         |            | R         |           |           |           |           |              |           |
|              |                                 |         | 1          | 0         | 0         | 0         | 1         | 0         | 0            | 0         |
| EP3_SIZE_L_A | Endpoint 3 size register Low A  | 079BH   | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1    | DATASIZE0 |
|              |                                 |         |            | R         |           |           |           |           |              |           |
|              |                                 |         | 1          | 0         | 0         | 0         | 1         | 0         | 0            | 0         |
| EP1_SIZE_L_B | Endpoint 1 size register Low B  | 07A1H   | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1    | DATASIZE0 |
|              |                                 |         |            | R         |           |           |           |           |              |           |
|              |                                 |         | 0          | 0         | 0         | 0         | 1         | 0         | 0            | 0         |
| EP2_SIZE_L_B | Endpoint 2 size register Low B  | 07A2H   | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1    | DATASIZE0 |
|              |                                 |         |            | R         |           |           |           |           |              |           |
|              |                                 |         | 0          | 0         | 0         | 0         | 1         | 0         | 0            | 0         |
| EP3_SIZE_L_B | Endpoint 3 size register Low B  | 07A3H   | PKT_ACTIVE | DATASIZE6 | DATASIZE5 | DATASIZE4 | DATASIZE3 | DATASIZE2 | DATASIZE1    | DATASIZE0 |
|              |                                 |         |            | R         |           |           |           |           |              |           |
|              |                                 |         | 0          | 0         | 0         | 0         | 1         | 0         | 0            | 0         |
| EP1_SIZE_H_A | Endpoint 1 size register High A | 07A9H   |            |           |           |           |           | DATASIZE9 | DATASIZE8    | DATASIZE7 |
|              |                                 |         |            |           |           |           |           | R         |              |           |
|              |                                 |         |            |           |           |           |           | 0         | 0            | 0         |
| EP2_SIZE_H_A | Endpoint 2 size register High A | 07AAH   |            |           |           |           |           | DATASIZE9 | DATASIZE8    | DATASIZE7 |
|              |                                 |         |            |           |           |           |           | R         |              |           |
|              |                                 |         |            |           |           |           |           | 0         | 0            | 0         |
| EP3_SIZE_H_A | Endpoint 3 size register HighA  | 07ABH   |            |           |           |           |           | DATASIZE9 | DATASIZE8    | DATASIZE7 |
|              |                                 |         |            |           |           |           |           | R         |              |           |
|              |                                 |         |            |           |           |           |           | 0         | 0            | 0         |

## (6) USB controller (3/6)

| Symbol        | Name                            | Address | 7         | 6         | 5         | 4          | 3          | 2          | 1          | 0          |
|---------------|---------------------------------|---------|-----------|-----------|-----------|------------|------------|------------|------------|------------|
| EP1_SIZE_H_B  | Endpoint 1 size register High B | 07B1H   |           |           |           |            |            | DATASIZE9  | DATASIZE8  | DATASIZE7  |
|               |                                 |         |           |           |           |            |            | R          |            |            |
|               |                                 |         |           |           |           |            |            | 0          | 0          | 0          |
| EP2_SIZE_H_B  | Endpoint 2 size register High B | 07B2H   |           |           |           |            |            | DATASIZE9  | DATASIZE8  | DATASIZE7  |
|               |                                 |         |           |           |           |            |            | R          |            |            |
|               |                                 |         |           |           |           |            |            | 0          | 0          | 0          |
| EP3_SIZE_H_B  | Endpoint 0 size register High B | 07B3H   |           |           |           |            |            | DATASIZE9  | DATASIZE8  | DATASIZE7  |
|               |                                 |         |           |           |           |            |            | R          |            |            |
|               |                                 |         |           |           |           |            |            | 0          | 0          | 0          |
| bmRequestType | bmRequest-Type register         | 07C0H   | DIRECTION | REQ_TYPE1 | REQ_TYPE0 | RECIPIENT4 | RECIPIENT3 | RECIPIENT2 | RECIPIENT1 | RECIPIENT0 |
|               |                                 |         | R         |           |           |            |            |            |            |            |
|               |                                 |         | 0         | 0         | 0         | 0          | 0          | 0          | 0          | 0          |
| bRequest      | bRequest register               | 07C1H   | REQUEST7  | REQUEST6  | REQUEST5  | REQUEST4   | REQUEST3   | REQUEST2   | REQUEST1   | REQUEST0   |
|               |                                 |         | R         |           |           |            |            |            |            |            |
|               |                                 |         | 0         | 0         | 0         | 0          | 0          | 0          | 0          | 0          |
| wValue_L      | wValue register Low             | 07C2H   | VALUE_L7  | VALUE_L6  | VALUE_L5  | VALUE_L4   | VALUE_L3   | VALUE_L2   | VALUE_L1   | VALUE_L0   |
|               |                                 |         | R         |           |           |            |            |            |            |            |
|               |                                 |         | 0         | 0         | 0         | 0          | 0          | 0          | 0          | 0          |
| wValue_H      | wValue register High            | 07C3H   | VALUE_H7  | VALUE_H6  | VALUE_H5  | VALUE_H4   | VALUE_H3   | VALUE_H2   | VALUE_H1   | VALUE_H0   |
|               |                                 |         | R         |           |           |            |            |            |            |            |
|               |                                 |         | 0         | 0         | 0         | 0          | 0          | 0          | 0          | 0          |
| wIndex_L      | wIndex register Low             | 07C4H   | INDEX_L7  | INDEX_L6  | INDEX_L5  | INDEX_L4   | INDEX_L3   | INDEX_L2   | INDEX_L1   | INDEX_L0   |
|               |                                 |         | R         |           |           |            |            |            |            |            |
|               |                                 |         | 0         | 0         | 0         | 0          | 0          | 0          | 0          | 0          |
| wIndex_H      | wIndex register High            | 07C5H   | INDEX_H7  | INDEX_H6  | INDEX_H5  | INDEX_H4   | INDEX_H3   | INDEX_H2   | INDEX_H1   | INDEX_H0   |
|               |                                 |         | R         |           |           |            |            |            |            |            |
|               |                                 |         | 0         | 0         | 0         | 0          | 0          | 0          | 0          | 0          |
| wLength_L     | wLength register Low            | 07C6H   | LENGTH_L7 | LENGTH_L6 | LENGTH_L5 | LENGTH_L4  | LENGTH_L3  | LENGTH_L2  | LENGTH_L1  | LENGTH_L0  |
|               |                                 |         | R         |           |           |            |            |            |            |            |
|               |                                 |         | 0         | 0         | 0         | 0          | 0          | 0          | 0          | 0          |
| wLength_H     | wLength register High           | 07C7H   | LENGTH_H7 | LENGTH_H6 | LENGTH_H5 | LENGTH_H4  | LENGTH_H3  | LENGTH_H2  | LENGTH_H1  | LENGTH_H0  |
|               |                                 |         | R         |           |           |            |            |            |            |            |
|               |                                 |         | 0         | 0         | 0         | 0          | 0          | 0          | 0          | 0          |

## (6) USB controller (4/6)

| Symbol                | Name                           | Address | 7            | 6           | 5            | 4            | 3            | 2            | 1          | 0          |
|-----------------------|--------------------------------|---------|--------------|-------------|--------------|--------------|--------------|--------------|------------|------------|
| SetupReceived         | SetupReceived register         | 07C8H   | D7           | D6          | D5           | D4           | D3           | D2           | D1         | D0         |
|                       |                                |         | W            |             |              |              |              |              |            |            |
|                       |                                |         | 0            | 0           | 0            | 0            | 0            | 0            | 0          | 0          |
| Current_Config        | Current_Config register        | 07C9H   | REMOTEWAKEUP |             | ALTERNATE[1] | ALTERNATE[0] | INTERFACE[1] | INTERFACE[0] | CONFIG[1]  | CONFIG[0]  |
|                       |                                |         | R            |             | R            |              |              |              |            |            |
|                       |                                |         | 0            |             | 0            | 0            | 0            | 0            | 0          | 0          |
| Standard Request      | Standard-Request register      | 07CAH   | S_INTERFACE  | G_INTERFACE | S_CONFIG     | G_CONFIG     | G_DESCRIPTOR | S_FEATURE    | C_FEATURE  | G_STATUS   |
|                       |                                |         | R            |             |              |              |              |              |            |            |
|                       |                                |         | 0            | 0           | 0            | 0            | 0            | 0            | 0          | 0          |
| Request               | Request register               | 07CBH   |              | SOFT_RESET  | G_PORT_STS   | G_DEVICE_ID  | VENDOR       | CLASS        | EXSTANDARD | STANDARD   |
|                       |                                |         |              | R           |              |              |              |              |            |            |
|                       |                                |         |              | 0           | 0            | 0            | 0            | 0            | 0          | 0          |
| DATASET1              | DATASET 1 register             | 07CCH   | EP3_DSET_B   | EP3_DSET_A  | EP2_DSET_B   | EP2_DSET_A   | EP1_DSET_B   | EP1_DSET_A   |            | EP0_DSET_A |
|                       |                                |         | R            |             |              |              |              |              |            | R          |
|                       |                                |         | 0            | 0           | 0            | 0            | 0            | 0            |            | 0          |
| DATASET2              | DATASET 2 register             | 07CDH   | EP7_DSET_B   | EP7_DSET_A  | EP6_DSET_B   | EP6_DSET_A   | EP5_DSET_B   | EP5_DSET_A   | EP4_DSET_B | EP4_DSET_A |
|                       |                                |         | R            |             |              |              |              |              |            |            |
|                       |                                |         | 0            | 0           | 0            | 0            | 0            | 0            | 0          | 0          |
| USB_STATE             | USB state register             | 07CEH   |              |             |              |              |              | Configured   | Addressed  | Default    |
|                       |                                |         |              |             |              |              |              | R/W          | R          |            |
|                       |                                |         |              |             |              |              |              | 0            | 0          | 1          |
| EOP                   | EOP register                   | 07CFH   | EP7_EOPB     | EP6_EOPB    | EP5_EOPB     | EP4_EOPB     | EP3_EOPB     | EP2_EOPB     | EP1_EOPB   | EP0_EOPB   |
|                       |                                |         | W            |             |              |              |              |              |            |            |
|                       |                                |         | 1            | 1           | 1            | 1            | 1            | 1            | 1          | 1          |
| COMMAND               | Command register               | 07D0H   |              | EP[2]       | EP[1]        | EP[0]        | Command[3]   | Command[2]   | Command[1] | Command[0] |
|                       |                                |         |              | W           |              |              |              |              |            |            |
|                       |                                |         |              | 0           | 0            | 0            | 0            | 0            | 0          | 0          |
| EPx_SINGLE1           | Endpoint 1 single register     | 07D1H   | EP3_SELECT   | EP2_SELECT  | EP1_SELECT   |              | EP3_SINGLE   | EP2_SINGLE   | EP1_SINGLE |            |
|                       |                                |         | R/W          |             |              |              | R/W          |              |            |            |
|                       |                                |         | 0            | 0           | 0            |              | 0            | 0            | 0          |            |
| EPx_BCS1              | Endpoint 1 BCS register        | 07D3H   | EP3_SELECT   | EP2_SELECT  | EP1_SELECT   |              | EP3_BCS      | EP2_BCS      | EP1_BCS    |            |
|                       |                                |         | R/W          |             |              |              | R/W          |              |            |            |
|                       |                                |         | 0            | 0           | 0            |              | 0            | 0            | 0          |            |
| INT_Control           | Interrupt control register     | 07D6H   |              |             |              |              |              |              |            | Status_nak |
|                       |                                |         |              |             |              |              |              |              |            | R/W        |
|                       |                                |         |              |             |              |              |              |              |            | 0          |
| Standard Request Mode | Standard Request mode register | 07D8H   | S_Interface  | G_Interface | S_Config     | G_Config     | G_Descript   | S_Feature    | C_Feature  | G_Status   |
|                       |                                |         | R/W          |             |              |              |              |              |            |            |
|                       |                                |         | 0            | 0           | 0            | 0            | 0            | 0            | 0          | 0          |
| Request Mode          | Request mode register          | 07D9H   |              | Soft_Reset  | G_Port_Sts   | G_DeviceId   |              |              |            |            |
|                       |                                |         |              | R/W         |              |              |              |              |            |            |
|                       |                                |         |              | 0           | 0            | 0            |              |              |            |            |



## (6) USB controller (5/6)

| Symbol               | Name                          | Address                 | 7                                                                                        | 6            | 5           | 4           | 3           | 2           | 1           | 0           |             |
|----------------------|-------------------------------|-------------------------|------------------------------------------------------------------------------------------|--------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Port Status          | Port status register          | 07E0H                   | Reserved7                                                                                | Reserved6    | PaperError  | Select      | NotError    | Reserved2   | Reserved1   | Reserved0   |             |
|                      |                               |                         | W                                                                                        |              |             |             |             |             |             |             |             |
|                      |                               |                         | 0                                                                                        | 0            | 0           | 1           | 1           | 0           | 0           | 0           |             |
| FRAME_L              | Frame register Low            | 07E1H                   | –                                                                                        | T[6]         | T[5]        | T[4]        | T[3]        | T[2]        | T[1]        | T[0]        |             |
|                      |                               |                         | R                                                                                        |              |             |             |             |             |             |             |             |
|                      |                               |                         | 0                                                                                        | 0            | 0           | 0           | 0           | 0           | 0           | 0           |             |
| FRAME_H              | Frame register H              | 07E2H                   | T[10]                                                                                    | T[9]         | T[8]        | T[7]        | <div></div> | CREATE      | FRAME_STS1  | FRAME_STS0  |             |
|                      |                               |                         | R                                                                                        |              |             |             | <div></div> | R           |             |             |             |
|                      |                               |                         | 0                                                                                        | 0            | 0           | 0           | <div></div> | 0           | 1           | 0           |             |
| ADDRESS              | Address register              | 07E3H                   | <div></div>                                                                              | A6           | A5          | A4          | A3          | A2          | A1          | A0          |             |
|                      |                               |                         | R                                                                                        |              |             |             |             |             |             |             |             |
|                      |                               |                         | 0                                                                                        | 0            | 0           | 0           | 0           | 0           | 0           | 0           |             |
| USBREADY             | USB ready register            | 07E6H                   | <div></div>                                                                              | <div></div>  | <div></div> | <div></div> | <div></div> | <div></div> | <div></div> | USBREADY    |             |
|                      |                               |                         | <div></div>                                                                              | <div></div>  | <div></div> | <div></div> | <div></div> | <div></div> | <div></div> | R/W         |             |
|                      |                               |                         | <div></div>                                                                              | <div></div>  | <div></div> | <div></div> | <div></div> | <div></div> | <div></div> | 0           |             |
| Set Descriptor STALL | Set-Descriptor stall register | 07E8H                   | <div></div>                                                                              | <div></div>  | <div></div> | <div></div> | <div></div> | <div></div> | <div></div> | S_D_STALL   |             |
|                      |                               |                         | <div></div>                                                                              | <div></div>  | <div></div> | <div></div> | <div></div> | <div></div> | <div></div> | W           |             |
|                      |                               |                         | <div></div>                                                                              | <div></div>  | <div></div> | <div></div> | <div></div> | <div></div> | <div></div> | 0           |             |
| USBINTFR1            | USB interrupt flag register 1 | 07F0H<br>(Prohibit RMW) | INT_URST_STR                                                                             | INT_URST_END | INT_SUS     | INT_RESUME  | INT_CLKSTOP | INT_CLKON   | <div></div> | <div></div> |             |
|                      |                               |                         | R/W                                                                                      |              |             |             |             |             |             | <div></div> | <div></div> |
|                      |                               |                         | 0                                                                                        | 0            | 0           | 0           | 0           | 0           | <div></div> | <div></div> |             |
|                      |                               |                         | When read 0: Not generate interrupt    When write 0: Clear flag<br>1: Generate interrupt |              |             |             |             |             |             |             |             |

## (6) USB controller (6/6)

| Symbol    | Name                          | Address | 7                                    | 6                          | 5          | 4          | 3           | 2          | 1          | 0          |
|-----------|-------------------------------|---------|--------------------------------------|----------------------------|------------|------------|-------------|------------|------------|------------|
| USBINTMR1 | USB interrupt mask register 1 | 07F4H   | MSK_URST_STR                         | MSK_URST_END               | MSK_SUS    | MSK_RESUME | MSK_CLKSTOP | MSK_CLKON  |            |            |
|           |                               |         | R/W                                  |                            |            |            |             |            |            |            |
|           |                               |         | 1                                    | 1                          | 1          | 1          | 1           | 1          |            |            |
|           |                               |         | 0: Be not masked 1: Be masked        |                            |            |            |             |            |            |            |
| USBINTMR2 | USB interrupt mask register 2 | 07F5H   | EP1_MSK_FA                           | EP1_MSK_EA                 | EP1_MSK_FB | EP1_MSK_EB | EP2_MSK_FA  | EP2_MSK_EA | EP2_MSK_FB | EP2_MSK_EB |
|           |                               |         | R/W                                  |                            |            |            |             |            |            |            |
|           |                               |         | 1                                    | 1                          | 1          | 1          | 1           | 1          | 1          | 1          |
|           |                               |         | 0: Be not masked 1: Be masked        |                            |            |            |             |            |            |            |
| USBINTMR3 | USB interrupt mask register 3 | 07F6H   | EP3_MSK_FA                           | EP3_MSK_EA                 |            |            |             |            |            |            |
|           |                               |         | R/W                                  |                            |            |            |             |            |            |            |
|           |                               |         | 1                                    | 1                          |            |            |             |            |            |            |
|           |                               |         | 0: Be not masked<br>1: Be masked     |                            |            |            |             |            |            |            |
| USBINTMR4 | USB interrupt mask register 4 | 07F7H   | MSK_SETUP                            | MSK_EP0                    | MSK_STAS   | MSK_STASN  | MSK_EP1N    | MSK_EP2N   | MSK_EP3N   |            |
|           |                               |         | R/W                                  |                            |            |            |             |            |            |            |
|           |                               |         | 1                                    | 1                          | 1          | 1          | 1           | 1          | 1          |            |
|           |                               |         | 0: Be not masked 1: Be masked        |                            |            |            |             |            |            |            |
| USBCR1    | USB control register 1        | 07F8H   | TRNS_USE                             | WAKEUP                     |            |            |             |            | SPEED      | USBCLKE    |
|           |                               |         | R/W                                  |                            |            |            |             |            | R/W        |            |
|           |                               |         | 0                                    | 0                          |            |            |             |            | 1          | 0          |
|           |                               |         | Transceiver<br>0:disable<br>1:enable | Wake up<br>0: –<br>1:Start |            |            |             |            |            |            |

## (7) SPIC (1/2)

| Symbol | Name                          | Address                 | 7                                                | 6                                                  | 5                                                                | 4                                         | 3                                                                | 2                                                                                                                                                                                                                            | 1                                                                                  | 0                                                                                                   |
|--------|-------------------------------|-------------------------|--------------------------------------------------|----------------------------------------------------|------------------------------------------------------------------|-------------------------------------------|------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|
| SPIMD  | SPI Mode Setting register     | 0820H<br>(Prohibit RMW) | SWRST                                            | XEN                                                |                                                                  |                                           |                                                                  | CLKSEL2                                                                                                                                                                                                                      | CLKSEL1                                                                            | CLKSEL0                                                                                             |
|        |                               |                         | W                                                | R/W                                                |                                                                  |                                           |                                                                  | R/W                                                                                                                                                                                                                          |                                                                                    |                                                                                                     |
|        |                               |                         | 0                                                | 0                                                  |                                                                  |                                           |                                                                  | 1                                                                                                                                                                                                                            | 0                                                                                  | 0                                                                                                   |
|        |                               |                         | Software reset<br>0: don't care<br>1: Reset      | SYSCK<br>0: disable<br>1: enable                   |                                                                  |                                           |                                                                  | Select Baud Rate<br>000:Reserved 100: f <sub>sys</sub> /8<br>001: f <sub>sys</sub> /2 101: f <sub>sys</sub> /16<br>010: f <sub>sys</sub> /3 110: f <sub>sys</sub> /64<br>011: f <sub>sys</sub> /4 111: f <sub>sys</sub> /256 |                                                                                    |                                                                                                     |
|        |                               | 0821H<br>(Prohibit RMW) | LOOPBACK                                         | MSB1ST                                             | DOSTAT                                                           |                                           | TCPOL                                                            | RCPOL                                                                                                                                                                                                                        | TDINV                                                                              | RDINV                                                                                               |
|        |                               |                         | R/W                                              |                                                    |                                                                  |                                           | R/W                                                              |                                                                                                                                                                                                                              |                                                                                    |                                                                                                     |
|        |                               |                         | 0                                                | 1                                                  | 1                                                                |                                           | 0                                                                | 0                                                                                                                                                                                                                            | 0                                                                                  | 0                                                                                                   |
|        |                               |                         | LOOPBACK Test mode<br>0:disable<br>1:enable      | Start bit for Transmit / Receive<br>0:LSB<br>1:MSB | SPDO pin state (no transmit)<br>0:fixed to "0"<br>1:fixed to "1" |                                           | Synchronous clock edge during transmitting<br>0: fall<br>1: rise | Synchronous clock edge during receiving<br>0: fall<br>1: rise                                                                                                                                                                | Invert data During transmitting<br>0: disable<br>1: enable                         | Invert data During receiving<br>0: disable<br>1: enable                                             |
| SPICT  | SPI Control register          | 0822H                   | CEN                                              | SPCS_B                                             | UNIT16                                                           | TXMOD                                     | TXE                                                              | FDPXE                                                                                                                                                                                                                        | RXMOD                                                                              | RXE                                                                                                 |
|        |                               |                         | R/W                                              |                                                    |                                                                  |                                           |                                                                  |                                                                                                                                                                                                                              |                                                                                    |                                                                                                     |
|        |                               |                         | 0                                                | 1                                                  | 0                                                                | 0                                         | 0                                                                | 0                                                                                                                                                                                                                            | 0                                                                                  | 0                                                                                                   |
|        |                               |                         | communication control<br>0: disable<br>1: enable | SPCS pin<br>0: output "0"<br>1: output "1"         | Data length<br>0: 8bit<br>1: 16bit                               | Transmit mode<br>0: UNIT<br>1: Sequential | Transmit control<br>0: disable<br>1: enable                      | Alignment in Full duplex<br>0: disable<br>1: enable                                                                                                                                                                          | Receive Mode<br>0: UNIT<br>1: Sequential                                           | Receive control<br>0: disable<br>1: enable                                                          |
|        |                               | 0823H                   | CRC16_7_B                                        | CRCRX_TX_B                                         | CRCRESET_B                                                       |                                           |                                                                  |                                                                                                                                                                                                                              |                                                                                    |                                                                                                     |
|        |                               |                         | R/W                                              |                                                    |                                                                  |                                           |                                                                  |                                                                                                                                                                                                                              |                                                                                    |                                                                                                     |
|        |                               |                         | 0                                                | 0                                                  | 0                                                                |                                           |                                                                  |                                                                                                                                                                                                                              |                                                                                    |                                                                                                     |
|        |                               |                         | CRC select<br>0: CRC7<br>1: CRC16                | CRC data<br>0: Transmit<br>1: receive              | CRC calculate register<br>0:Reset<br>1:Release Reset             |                                           |                                                                  |                                                                                                                                                                                                                              |                                                                                    |                                                                                                     |
| SPIST  | SPI Status register           | 0824H                   |                                                  |                                                    |                                                                  |                                           | TEMP                                                             |                                                                                                                                                                                                                              | TEND                                                                               | REND                                                                                                |
|        |                               |                         |                                                  |                                                    |                                                                  |                                           | R                                                                |                                                                                                                                                                                                                              | R                                                                                  |                                                                                                     |
|        |                               |                         |                                                  |                                                    |                                                                  |                                           | 1                                                                |                                                                                                                                                                                                                              | 1                                                                                  | 0                                                                                                   |
|        |                               |                         |                                                  |                                                    |                                                                  |                                           | Transmit FIFO Status<br>0: no space<br>1: having space           |                                                                                                                                                                                                                              | Transmit Status<br>0: during transmission or having transmission data<br>1: finish | Receive Status<br>0: during receiving or not having receiving data<br>1: finish or not having space |
|        |                               | 0825H                   |                                                  |                                                    |                                                                  |                                           |                                                                  |                                                                                                                                                                                                                              |                                                                                    |                                                                                                     |
|        |                               |                         |                                                  |                                                    |                                                                  |                                           |                                                                  |                                                                                                                                                                                                                              |                                                                                    |                                                                                                     |
|        |                               |                         |                                                  |                                                    |                                                                  |                                           |                                                                  |                                                                                                                                                                                                                              |                                                                                    |                                                                                                     |
|        |                               |                         |                                                  |                                                    |                                                                  |                                           |                                                                  |                                                                                                                                                                                                                              |                                                                                    |                                                                                                     |
| SPIIE  | SPI Interrupt enable register | 082CH                   |                                                  |                                                    |                                                                  |                                           | TEMPIE                                                           | RFULIE                                                                                                                                                                                                                       | TENDIE                                                                             | RENDIE                                                                                              |
|        |                               |                         |                                                  |                                                    |                                                                  |                                           | R/W                                                              |                                                                                                                                                                                                                              |                                                                                    |                                                                                                     |
|        |                               |                         |                                                  |                                                    |                                                                  |                                           | 0                                                                | 0                                                                                                                                                                                                                            | 0                                                                                  | 0                                                                                                   |
|        |                               |                         |                                                  |                                                    |                                                                  |                                           | TEMP interrupt<br>0:enable<br>1:disable                          | RFUL interrupt<br>0:enable<br>1:disable                                                                                                                                                                                      | TEND interrupt<br>0:enable<br>1:disable                                            | REND interrupt<br>0:enable<br>1:disable                                                             |
|        |                               | 082DH                   |                                                  |                                                    |                                                                  |                                           |                                                                  |                                                                                                                                                                                                                              |                                                                                    |                                                                                                     |
|        |                               |                         |                                                  |                                                    |                                                                  |                                           |                                                                  |                                                                                                                                                                                                                              |                                                                                    |                                                                                                     |
|        |                               |                         |                                                  |                                                    |                                                                  |                                           |                                                                  |                                                                                                                                                                                                                              |                                                                                    |                                                                                                     |
|        |                               |                         |                                                  |                                                    |                                                                  |                                           |                                                                  |                                                                                                                                                                                                                              |                                                                                    |                                                                                                     |

## (7) SPIC (2/2)

| Symbol | Name                                     | Address | 7                             | 6      | 5      | 4      | 3      | 2      | 1     | 0     |
|--------|------------------------------------------|---------|-------------------------------|--------|--------|--------|--------|--------|-------|-------|
| SPICR  | SPI<br>CRC<br>register                   | 0826H   | CRCD7                         | CRCD6  | CRCD5  | CRCD4  | CRCD3  | CRCD2  | CRCD1 | CRCD0 |
|        |                                          |         | R                             |        |        |        |        |        |       |       |
|        |                                          |         | 0                             | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|        |                                          |         | CRC result register [7:0]     |        |        |        |        |        |       |       |
|        |                                          | 0827H   | CRCD15                        | CRCD14 | CRCD13 | CRCD12 | CRCD11 | CRCD10 | CRCD9 | CRCD8 |
|        |                                          |         | R                             |        |        |        |        |        |       |       |
|        |                                          |         | 0                             | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|        |                                          |         | CRC result register [15:8]    |        |        |        |        |        |       |       |
| SPITD0 | SPI<br>transmission<br>data0<br>register | 0830H   | TXD7                          | TXD6   | TXD5   | TXD4   | TXD3   | TXD2   | TXD1  | TXD0  |
|        |                                          |         | R/W                           |        |        |        |        |        |       |       |
|        |                                          |         | 0                             | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|        |                                          |         | Transmit data register [7:0]  |        |        |        |        |        |       |       |
|        |                                          | 0831H   | TXD15                         | TXD14  | TXD13  | TXD12  | TXD11  | TXD10  | TXD9  | TXD8  |
|        |                                          |         | R/W                           |        |        |        |        |        |       |       |
|        |                                          |         | 0                             | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|        |                                          |         | Transmit data register [15:8] |        |        |        |        |        |       |       |
| SPITD1 | SPI<br>transmission<br>data1<br>register | 0832H   | TXD7                          | TXD6   | TXD5   | TXD4   | TXD3   | TXD2   | TXD1  | TXD0  |
|        |                                          |         | R/W                           |        |        |        |        |        |       |       |
|        |                                          |         | 0                             | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|        |                                          |         | Transmit data register [7:0]  |        |        |        |        |        |       |       |
|        |                                          | 0833H   | TXD15                         | TXD14  | TXD13  | TXD12  | TXD11  | TXD10  | TXD9  | TXD8  |
|        |                                          |         | R/W                           |        |        |        |        |        |       |       |
|        |                                          |         | 0                             | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|        |                                          |         | Transmit data register [15:8] |        |        |        |        |        |       |       |
| SPIRD0 | SPI<br>receive<br>data0<br>register      | 0834H   | RXD7                          | RXD6   | RXD5   | RXD4   | RXD3   | RXD2   | RXD1  | RXD0  |
|        |                                          |         | R                             |        |        |        |        |        |       |       |
|        |                                          |         | 0                             | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|        |                                          |         | Receive data register [7:0]   |        |        |        |        |        |       |       |
|        |                                          | 0835H   | RXD15                         | RXD14  | RXD13  | RXD12  | RXD11  | RXD10  | RXD9  | RXD8  |
|        |                                          |         | R                             |        |        |        |        |        |       |       |
|        |                                          |         | 0                             | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|        |                                          |         | Receive data register [15:8]  |        |        |        |        |        |       |       |
| SPIRD1 | SPI<br>receive<br>data1<br>register      | 0836H   | RXD7                          | RXD6   | RXD5   | RXD4   | RXD3   | RXD2   | RXD1  | RXD0  |
|        |                                          |         | R                             |        |        |        |        |        |       |       |
|        |                                          |         | 0                             | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|        |                                          |         | Receive data register [7:0]   |        |        |        |        |        |       |       |
|        |                                          | 0837H   | RXD15                         | RXD14  | RXD13  | RXD12  | RXD11  | RXD10  | RXD9  | RXD8  |
|        |                                          |         | R                             |        |        |        |        |        |       |       |
|        |                                          |         | 0                             | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|        |                                          |         | Receive data register [15:8]  |        |        |        |        |        |       |       |

## (8) MMU (1/7)

| Symbol                                         | Name                                                                                                                                                                                                                                                                             | Address | 7                                                                                                                                          | 6  | 5                                                                                                                                          | 4  | 3  | 2  | 1  | 0   |  |
|------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------|----|--------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|-----|--|
| LOCALPX                                        | LOCALX<br>register<br>for<br>program                                                                                                                                                                                                                                             | 0880H   | X7                                                                                                                                         | X6 | X5                                                                                                                                         | X4 | X3 | X2 | X1 | X0  |  |
|                                                |                                                                                                                                                                                                                                                                                  |         | R/W                                                                                                                                        |    |                                                                                                                                            |    |    |    |    |     |  |
|                                                |                                                                                                                                                                                                                                                                                  |         | 0                                                                                                                                          | 0  | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0   |  |
|                                                |                                                                                                                                                                                                                                                                                  |         | Specify the bank number for the LOCAL-X area<br>(Since bank 0 is overlapping with the COMMON area, this filed must not be specified as 0.) |    |                                                                                                                                            |    |    |    |    |     |  |
|                                                |                                                                                                                                                                                                                                                                                  | 0881H   | LXE                                                                                                                                        |    |                                                                                                                                            |    |    |    |    | X8  |  |
|                                                |                                                                                                                                                                                                                                                                                  |         | R/W                                                                                                                                        |    |                                                                                                                                            |    |    |    |    | R/W |  |
|                                                |                                                                                                                                                                                                                                                                                  |         | 0                                                                                                                                          |    |                                                                                                                                            |    |    |    |    | 0   |  |
| Bank for<br>LOCAL-X<br>0: Disable<br>1: Enable | Specify the bank number for the LOCAL-X area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>000000000 to 011111111 CSXA<br>100000000 to 111111111 CSXB                                                                                     |         |                                                                                                                                            |    |                                                                                                                                            |    |    |    |    |     |  |
| LOCALPY                                        | LOCALY<br>register<br>for<br>program                                                                                                                                                                                                                                             | 0882H   |                                                                                                                                            |    | Y5                                                                                                                                         | Y4 | Y3 | Y2 | Y1 | Y0  |  |
|                                                |                                                                                                                                                                                                                                                                                  |         |                                                                                                                                            |    | R/W                                                                                                                                        |    |    |    |    |     |  |
|                                                |                                                                                                                                                                                                                                                                                  |         |                                                                                                                                            |    | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0   |  |
|                                                |                                                                                                                                                                                                                                                                                  |         |                                                                                                                                            |    | Specify the bank number for the LOCAL-Y area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |    |    |    |    |     |  |
|                                                |                                                                                                                                                                                                                                                                                  | 0883H   | LYE                                                                                                                                        |    |                                                                                                                                            |    |    |    |    |     |  |
|                                                |                                                                                                                                                                                                                                                                                  |         | R/W                                                                                                                                        |    |                                                                                                                                            |    |    |    |    |     |  |
|                                                |                                                                                                                                                                                                                                                                                  |         | 0                                                                                                                                          |    |                                                                                                                                            |    |    |    |    |     |  |
| Bank for<br>LOCAL-Y<br>0: Disable<br>1: Enable |                                                                                                                                                                                                                                                                                  |         |                                                                                                                                            |    |                                                                                                                                            |    |    |    |    |     |  |
| LOCALPZ                                        | LOCALZ<br>register<br>for<br>program                                                                                                                                                                                                                                             | 0884H   | Z7                                                                                                                                         | Z6 | Z5                                                                                                                                         | Z4 | Z3 | Z2 | Z1 | Z0  |  |
|                                                |                                                                                                                                                                                                                                                                                  |         | R/W                                                                                                                                        |    |                                                                                                                                            |    |    |    |    |     |  |
|                                                |                                                                                                                                                                                                                                                                                  |         | 0                                                                                                                                          | 0  | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0   |  |
|                                                |                                                                                                                                                                                                                                                                                  |         | Specify the bank number for the LOCAL-Z area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |    |                                                                                                                                            |    |    |    |    |     |  |
|                                                |                                                                                                                                                                                                                                                                                  | 0885H   | LZE                                                                                                                                        |    |                                                                                                                                            |    |    |    |    | Z8  |  |
|                                                |                                                                                                                                                                                                                                                                                  |         | R/W                                                                                                                                        |    |                                                                                                                                            |    |    |    |    | R/W |  |
|                                                |                                                                                                                                                                                                                                                                                  |         | 0                                                                                                                                          |    |                                                                                                                                            |    |    |    |    | 0   |  |
| Bank for<br>LOCAL-Z<br>0: Disable<br>1: Enable | Specify the bank number for the LOCAL-Z area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>000000000 to 001111111 CSZA 100000000 to 101111111 Setting prohibited<br>010000000 to 011111111 Setting prohibited 110000000 to 111111111 CSZD |         |                                                                                                                                            |    |                                                                                                                                            |    |    |    |    |     |  |

## (8) MMU (2/7)

| Symbol  | Name                     | Address | 7                                                                                                                                          | 6                                                                                                                                                                                                                                                                                      | 5   | 4  | 3  | 2  | 1  | 0   |
|---------|--------------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|----|----|----|----|-----|
| LOCALRX | LOCALX register for read | 0890H   | X7                                                                                                                                         | X6                                                                                                                                                                                                                                                                                     | X5  | X4 | X3 | X2 | X1 | X0  |
|         |                          |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                        |     |    |    |    |    |     |
|         |                          |         | 0                                                                                                                                          | 0                                                                                                                                                                                                                                                                                      | 0   | 0  | 0  | 0  | 0  | 0   |
|         |                          |         | Specify the bank number for the LOCAL-X area<br>(Since bank 0 is overlapping with the COMMON area, this filed must not be specified as 0.) |                                                                                                                                                                                                                                                                                        |     |    |    |    |    |     |
|         |                          | 0891H   | LXE                                                                                                                                        |                                                                                                                                                                                                                                                                                        |     |    |    |    |    | X8  |
|         |                          |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                        |     |    |    |    |    | R/W |
|         |                          |         | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                        |     |    |    |    |    | 0   |
|         |                          |         | Bank for LOCAL-X<br>0: Disable<br>1: Enable                                                                                                | Specify the bank number for the LOCAL-X area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>000000000 to 011111111 CSXA<br>100000000 to 111111111 CSXB                                                                                           |     |    |    |    |    |     |
| LOCALRY | LOCALY register for read | 0892H   |                                                                                                                                            |                                                                                                                                                                                                                                                                                        | Y5  | Y4 | Y3 | Y2 | Y1 | Y0  |
|         |                          |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                        | R/W |    |    |    |    |     |
|         |                          |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                        | 0   | 0  | 0  | 0  | 0  | 0   |
|         |                          |         | Specify the bank number for the LOCAL-Y area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |                                                                                                                                                                                                                                                                                        |     |    |    |    |    |     |
|         |                          | 0893H   | LYE                                                                                                                                        |                                                                                                                                                                                                                                                                                        |     |    |    |    |    |     |
|         |                          |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                        |     |    |    |    |    |     |
|         |                          |         | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                        |     |    |    |    |    |     |
|         |                          |         | Bank for LOCAL-Y<br>0: Disable<br>1: Enable                                                                                                |                                                                                                                                                                                                                                                                                        |     |    |    |    |    |     |
| LOCALRZ | LOCALZ register for read | 0894H   | Z7                                                                                                                                         | Z6                                                                                                                                                                                                                                                                                     | Z5  | Z4 | Z3 | Z2 | Z1 | Z0  |
|         |                          |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                        |     |    |    |    |    |     |
|         |                          |         | 0                                                                                                                                          | 0                                                                                                                                                                                                                                                                                      | 0   | 0  | 0  | 0  | 0  | 0   |
|         |                          |         | Specify the bank number for the LOCAL-Z area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |                                                                                                                                                                                                                                                                                        |     |    |    |    |    |     |
|         |                          | 0895H   | LZE                                                                                                                                        |                                                                                                                                                                                                                                                                                        |     |    |    |    |    | Z8  |
|         |                          |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                        |     |    |    |    |    | R/W |
|         |                          |         | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                        |     |    |    |    |    | 0   |
|         |                          |         | Bank for LOCAL-Z<br>0: Disable<br>1: Enable                                                                                                | Specify the bank number for the LOCAL-Z area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>000000000 to 001111111 CSZA<br>010000000 to 011111111 Setting prohibited<br>100000000 to 101111111 Setting prohibited<br>110000000 to 111111111 CSZD |     |    |    |    |    |     |

## (8) MMU (3/7)

| Symbol  | Name                               | Address | 7                                                                                                                                          | 6                                                                                                                                                                                                                                                                                          | 5   | 4  | 3  | 2  | 1  | 0   |
|---------|------------------------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|----|----|----|----|-----|
| LOCALWX | LOCALX<br>register<br>for<br>write | 0898H   | X7                                                                                                                                         | X6                                                                                                                                                                                                                                                                                         | X5  | X4 | X3 | X2 | X1 | X0  |
|         |                                    |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                            |     |    |    |    |    |     |
|         |                                    |         | 0                                                                                                                                          | 0                                                                                                                                                                                                                                                                                          | 0   | 0  | 0  | 0  | 0  | 0   |
|         |                                    |         | Specify the bank number for the LOCAL-X area<br>(Since bank 0 is overlapping with the COMMON area, this filed must not be specified as 0.) |                                                                                                                                                                                                                                                                                            |     |    |    |    |    |     |
|         |                                    | 0899H   | LXE                                                                                                                                        |                                                                                                                                                                                                                                                                                            |     |    |    |    |    | X8  |
|         |                                    |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                            |     |    |    |    |    | R/W |
|         |                                    |         | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                            |     |    |    |    |    | 0   |
|         |                                    |         | Bank for<br>LOCAL-X<br>0: Disable<br>1: Enable                                                                                             | Specify the bank number for the LOCAL-X area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>000000000 to 011111111 CSXA<br>100000000 to 111111111 CSXB                                                                                               |     |    |    |    |    |     |
| LOCALWY | LOCALY<br>register<br>for<br>write | 089AH   |                                                                                                                                            |                                                                                                                                                                                                                                                                                            | Y5  | Y4 | Y3 | Y2 | Y1 | Y0  |
|         |                                    |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                            | R/W |    |    |    |    |     |
|         |                                    |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                            | 0   | 0  | 0  | 0  | 0  | 0   |
|         |                                    |         | Specify the bank number for the LOCAL-Y area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |                                                                                                                                                                                                                                                                                            |     |    |    |    |    |     |
|         |                                    | 089BH   | LYE                                                                                                                                        |                                                                                                                                                                                                                                                                                            |     |    |    |    |    |     |
|         |                                    |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                            |     |    |    |    |    |     |
|         |                                    |         | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                            |     |    |    |    |    |     |
|         |                                    |         | Bank for<br>LOCAL-Y<br>0: Disable<br>1: Enable                                                                                             |                                                                                                                                                                                                                                                                                            |     |    |    |    |    |     |
| LOCALWZ | LOCALZ<br>register<br>for<br>write | 089CH   | Z7                                                                                                                                         | Z6                                                                                                                                                                                                                                                                                         | Z5  | Z4 | Z3 | Z2 | Z1 | Z0  |
|         |                                    |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                            |     |    |    |    |    |     |
|         |                                    |         | 0                                                                                                                                          | 0                                                                                                                                                                                                                                                                                          | 0   | 0  | 0  | 0  | 0  | 0   |
|         |                                    |         | Specify the bank number for the LOCAL-Z area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |                                                                                                                                                                                                                                                                                            |     |    |    |    |    |     |
|         |                                    | 089DH   | LZE                                                                                                                                        |                                                                                                                                                                                                                                                                                            |     |    |    |    |    | Z8  |
|         |                                    |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                            |     |    |    |    |    | R/W |
|         |                                    |         | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                            |     |    |    |    |    | 0   |
|         |                                    |         | Bank for<br>LOCAL-Z<br>0: Disable<br>1: Enable                                                                                             | Specify the bank number for the LOCAL-Z area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>000000000 to 001111111 CSZA      100000000 to 101111111 Setting prohibited<br>010000000 to 011111111 Setting prohibited      110000000 to 111111111 CSZD |     |    |    |    |    |     |

## (8) MMU (4/7)

| Symbol   | Name                                    | Address | 7                                                                                                                                          | 6                                                                                                                                                                                                                                                                                      | 5   | 4  | 3  | 2  | 1  | 0   |
|----------|-----------------------------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|----|----|----|----|-----|
| LOCALESX | LOCALX<br>register<br>for DMA<br>source | 08A0H   | X7                                                                                                                                         | X6                                                                                                                                                                                                                                                                                     | X5  | X4 | X3 | X2 | X1 | X0  |
|          |                                         |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                        |     |    |    |    |    |     |
|          |                                         |         | 0                                                                                                                                          | 0                                                                                                                                                                                                                                                                                      | 0   | 0  | 0  | 0  | 0  | 0   |
|          |                                         |         | Specify the bank number for the LOCAL-X area<br>(Since bank 0 is overlapping with the COMMON area, this filed must not be specified as 0.) |                                                                                                                                                                                                                                                                                        |     |    |    |    |    |     |
|          |                                         | 08A1H   | LXE                                                                                                                                        |                                                                                                                                                                                                                                                                                        |     |    |    |    |    | X8  |
|          |                                         |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                        |     |    |    |    |    | R/W |
|          |                                         |         | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                        |     |    |    |    |    | 0   |
|          |                                         |         | Bank for<br>LOCAL-X<br>0: Disable<br>1: Enable                                                                                             | Specify the bank number for the LOCAL-X area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>000000000 to 011111111 CSXA<br>100000000 to 111111111 CSXB                                                                                           |     |    |    |    |    |     |
| LOCALESY | LOCALY<br>register<br>for DMA<br>source | 08A2H   |                                                                                                                                            |                                                                                                                                                                                                                                                                                        | Y5  | Y4 | Y3 | Y2 | Y1 | Y0  |
|          |                                         |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                        | R/W |    |    |    |    |     |
|          |                                         |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                        | 0   | 0  | 0  | 0  | 0  | 0   |
|          |                                         |         | Specify the bank number for the LOCAL-Y area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |                                                                                                                                                                                                                                                                                        |     |    |    |    |    |     |
|          |                                         | 08A3H   | LYE                                                                                                                                        |                                                                                                                                                                                                                                                                                        |     |    |    |    |    |     |
|          |                                         |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                        |     |    |    |    |    |     |
|          |                                         |         | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                        |     |    |    |    |    |     |
|          |                                         |         | Bank for<br>LOCAL-Y<br>0: Disable<br>1: Enable                                                                                             |                                                                                                                                                                                                                                                                                        |     |    |    |    |    |     |
| LOCALESZ | LOCALZ<br>register<br>for DMA<br>source | 08A4H   | Z7                                                                                                                                         | Z6                                                                                                                                                                                                                                                                                     | Z5  | Z4 | Z3 | Z2 | Z1 | Z0  |
|          |                                         |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                        |     |    |    |    |    |     |
|          |                                         |         | 0                                                                                                                                          | 0                                                                                                                                                                                                                                                                                      | 0   | 0  | 0  | 0  | 0  | 0   |
|          |                                         |         | Specify the bank number for the LOCAL-Z area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3)  |                                                                                                                                                                                                                                                                                        |     |    |    |    |    |     |
|          |                                         | 08A5H   | LZE                                                                                                                                        |                                                                                                                                                                                                                                                                                        |     |    |    |    |    | Z8  |
|          |                                         |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                        |     |    |    |    |    | R/W |
|          |                                         |         | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                        |     |    |    |    |    | 0   |
|          |                                         |         | BANK for<br>LOCAL-Z<br>0: Disable<br>1: Enable                                                                                             | Specify the bank number for the LOCAL-Z area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>000000000 to 001111111 CSZA<br>010000000 to 011111111 Setting prohibited<br>100000000 to 101111111 Setting prohibited<br>110000000 to 111111111 CSZD |     |    |    |    |    |     |



## (8) MMU (5/7)

| Symbol   | Name                                | Address | 7                                                                                                                                          | 6                                                                                                                                                                                                                                                                                                    | 5                                                                                                                                          | 4  | 3  | 2  | 1  | 0  |     |
|----------|-------------------------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|-----|
| LOCALEDX | LOCALX register for DMA destination | 08A8H   | X7                                                                                                                                         | X6                                                                                                                                                                                                                                                                                                   | X5                                                                                                                                         | X4 | X3 | X2 | X1 | X0 |     |
|          |                                     |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                                      |                                                                                                                                            |    |    |    |    |    |     |
|          |                                     |         | 0                                                                                                                                          | 0                                                                                                                                                                                                                                                                                                    | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0  |     |
|          |                                     |         | Specify the bank number for the LOCAL-X area<br>(Since bank 0 is overlapping with the COMMON area, this filed must not be specified as 0.) |                                                                                                                                                                                                                                                                                                      |                                                                                                                                            |    |    |    |    |    |     |
|          |                                     | 08A9H   | LXE                                                                                                                                        |                                                                                                                                                                                                                                                                                                      |                                                                                                                                            |    |    |    |    |    | X8  |
|          |                                     |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                                      |                                                                                                                                            |    |    |    |    |    | R/W |
|          |                                     |         | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                                      |                                                                                                                                            |    |    |    |    |    | 0   |
|          |                                     |         | Bank for LOCAL-X<br>0: Disable<br>1: Enable                                                                                                | Specify the bank number for the LOCAL-X area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>000000000 to 011111111 CSXA<br>100000000 to 111111111 CSXB                                                                                                         |                                                                                                                                            |    |    |    |    |    |     |
|          |                                     |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                                      |                                                                                                                                            |    |    |    |    |    |     |
| LOCALEDY | LOCALY register for DMA destination | 08AAH   |                                                                                                                                            |                                                                                                                                                                                                                                                                                                      | Y5                                                                                                                                         | Y4 | Y3 | Y2 | Y1 | Y0 |     |
|          |                                     |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                                      | R/W                                                                                                                                        |    |    |    |    |    |     |
|          |                                     |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                                      | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0  |     |
|          |                                     |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                                      | Specify the bank number for the LOCAL-Y area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |    |    |    |    |    |     |
|          |                                     | 08ABH   | LYE                                                                                                                                        |                                                                                                                                                                                                                                                                                                      |                                                                                                                                            |    |    |    |    |    |     |
|          |                                     |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                                      |                                                                                                                                            |    |    |    |    |    |     |
|          |                                     |         | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                                      |                                                                                                                                            |    |    |    |    |    |     |
|          |                                     |         | Bank for LOCAL-Y<br>0: Disable<br>1: Enable                                                                                                |                                                                                                                                                                                                                                                                                                      |                                                                                                                                            |    |    |    |    |    |     |
|          |                                     |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                                      |                                                                                                                                            |    |    |    |    |    |     |
| LOCALEDZ | LOCALZ register for DMA destination | 08ACH   | Z7                                                                                                                                         | Z6                                                                                                                                                                                                                                                                                                   | Z5                                                                                                                                         | Z4 | Z3 | Z2 | Z1 | Z0 |     |
|          |                                     |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                                      |                                                                                                                                            |    |    |    |    |    |     |
|          |                                     |         | 0                                                                                                                                          | 0                                                                                                                                                                                                                                                                                                    | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0  |     |
|          |                                     |         | Specify the bank number for the LOCAL-Z area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |                                                                                                                                                                                                                                                                                                      |                                                                                                                                            |    |    |    |    |    |     |
|          |                                     | 08ADH   | LZE                                                                                                                                        |                                                                                                                                                                                                                                                                                                      |                                                                                                                                            |    |    |    |    |    | Z8  |
|          |                                     |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                                      |                                                                                                                                            |    |    |    |    |    | R/W |
|          |                                     |         | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                                      |                                                                                                                                            |    |    |    |    |    | 0   |
|          |                                     |         | Bank for LOCAL-Z<br>0: Disable<br>1: Enable                                                                                                | Specify the bank number for the LOCAL-Z area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>000000000 to 001111111 CSZA                      100000000 to 101111111 Setting prohibited<br>010000000 to 011111111 Setting prohibited110000000 to 111111111 CSZD |                                                                                                                                            |    |    |    |    |    |     |
|          |                                     |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                                      |                                                                                                                                            |    |    |    |    |    |     |

## (8) MMU (6/7)

| Symbol   | Name                                    | Address | 7                                                                                                                                          | 6                                                                                                                                                                                                                                                                                | 5                                                                                                                                          | 4  | 3  | 2  | 1  | 0   |
|----------|-----------------------------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|-----|
| LOCALOSX | LOCALX<br>register<br>for DMA<br>source | 08B0H   | X7                                                                                                                                         | X6                                                                                                                                                                                                                                                                               | X5                                                                                                                                         | X4 | X3 | X2 | X1 | X0  |
|          |                                         |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    |     |
|          |                                         |         | 0                                                                                                                                          | 0                                                                                                                                                                                                                                                                                | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0   |
|          |                                         |         | Specify the bank number for the LOCAL-X area<br>(Since bank 0 is overlapping with the COMMON area, this filed must not be specified as 0.) |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    |     |
|          |                                         | 08B1H   | LXE                                                                                                                                        |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    | X8  |
|          |                                         |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    | R/W |
|          |                                         |         | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    | 0   |
|          |                                         |         | Bank for<br>LOCAL-X<br>0: Disable<br>1: Enable                                                                                             | Specify the bank number for the LOCAL-X area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>000000000 to 011111111 CSXA<br>100000000 to 111111111 CSXB                                                                                     |                                                                                                                                            |    |    |    |    |     |
|          |                                         |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    |     |
|          |                                         |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    |     |
| LOCALOSY | LOCALY<br>register<br>for DMA<br>source | 08B2H   |                                                                                                                                            |                                                                                                                                                                                                                                                                                  | Y5                                                                                                                                         | Y4 | Y3 | Y2 | Y1 | Y0  |
|          |                                         |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                  | R/W                                                                                                                                        |    |    |    |    |     |
|          |                                         |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                  | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0   |
|          |                                         |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                  | Specify the bank number for the LOCAL-Y area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |    |    |    |    |     |
|          |                                         | 08B3H   | LYE                                                                                                                                        |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    |     |
|          |                                         |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    |     |
|          |                                         |         | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    |     |
|          |                                         |         | Bank for<br>LOCAL-Y<br>0: Disable<br>1: Enable                                                                                             |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    |     |
|          |                                         |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    |     |
|          |                                         |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    |     |
| LOCALOSZ | LOCALZ<br>register<br>for DMA<br>source | 08B4H   | Z7                                                                                                                                         | Z6                                                                                                                                                                                                                                                                               | Z5                                                                                                                                         | Z4 | Z3 | Z2 | Z1 | Z0  |
|          |                                         |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    |     |
|          |                                         |         | 0                                                                                                                                          | 0                                                                                                                                                                                                                                                                                | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0   |
|          |                                         |         | Specify the bank number for the LOCAL-Z area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    |     |
|          |                                         | 08B5H   | LZE                                                                                                                                        |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    | Z8  |
|          |                                         |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    | R/W |
|          |                                         |         | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    | 0   |
|          |                                         |         | Bank for<br>LOCAL-Z<br>0: Disable<br>1: Enable                                                                                             | Specify the bank number for the LOCAL-Z area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>000000000 to 001111111 CSZA 100000000 to 101111111 Setting prohibited<br>010000000 to 011111111 Setting prohibited 110000000 to 111111111 CSZD |                                                                                                                                            |    |    |    |    |     |
|          |                                         |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    |     |
|          |                                         |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                  |                                                                                                                                            |    |    |    |    |     |

## (10) MMU (7/7)

| Symbol  | Name                                | Address | 7                                                                                                                                          | 6                                                                                                                                                                                                                                                                                     | 5                                                                                                                                          | 4  | 3  | 2  | 1  | 0   |
|---------|-------------------------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|-----|
| LOCALDX | LOCALX register for DMA destination | 08B8H   | X7                                                                                                                                         | X6                                                                                                                                                                                                                                                                                    | X5                                                                                                                                         | X4 | X3 | X2 | X1 | X0  |
|         |                                     |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                       |                                                                                                                                            |    |    |    |    |     |
|         |                                     |         | 0                                                                                                                                          | 0                                                                                                                                                                                                                                                                                     | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0   |
|         |                                     |         | Specify the bank number for the LOCAL-X area<br>(Since bank 0 is overlapping with the COMMON area, this filed must not be specified as 0.) |                                                                                                                                                                                                                                                                                       |                                                                                                                                            |    |    |    |    |     |
|         |                                     | 08B9H   | LXE                                                                                                                                        |                                                                                                                                                                                                                                                                                       |                                                                                                                                            |    |    |    |    | X8  |
|         |                                     |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                       |                                                                                                                                            |    |    |    |    | R/W |
|         |                                     |         | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                       |                                                                                                                                            |    |    |    |    | 0   |
|         |                                     |         | Bank for LOCAL-X<br>0: Disable<br>1: Enable                                                                                                | Specify the bank number for the LOCAL-X area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>000000000 to 011111111 CSXA<br>100000000 to 111111111 CSXB                                                                                          |                                                                                                                                            |    |    |    |    |     |
| LOCALDY | LOCALY register for DMA destination | 08BAH   |                                                                                                                                            |                                                                                                                                                                                                                                                                                       | Y5                                                                                                                                         | Y4 | Y3 | Y2 | Y1 | Y0  |
|         |                                     |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                       | R/W                                                                                                                                        |    |    |    |    |     |
|         |                                     |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                       | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0   |
|         |                                     |         |                                                                                                                                            |                                                                                                                                                                                                                                                                                       | Specify the bank number for the LOCAL-Y area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |    |    |    |    |     |
|         |                                     | 08BBH   | LYE                                                                                                                                        |                                                                                                                                                                                                                                                                                       |                                                                                                                                            |    |    |    |    |     |
|         |                                     |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                       |                                                                                                                                            |    |    |    |    |     |
|         |                                     |         | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                       |                                                                                                                                            |    |    |    |    |     |
|         |                                     |         | BANK for LOCAL-Y<br>0: Disable<br>1: Enable                                                                                                |                                                                                                                                                                                                                                                                                       |                                                                                                                                            |    |    |    |    |     |
| LOCALDZ | LOCALZ register for DMA destination | 08BCH   | Z7                                                                                                                                         | Z6                                                                                                                                                                                                                                                                                    | Z5                                                                                                                                         | Z4 | Z3 | Z2 | Z1 | Z0  |
|         |                                     |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                       |                                                                                                                                            |    |    |    |    |     |
|         |                                     |         | 0                                                                                                                                          | 0                                                                                                                                                                                                                                                                                     | 0                                                                                                                                          | 0  | 0  | 0  | 0  | 0   |
|         |                                     |         | Specify the bank number for the LOCAL-Z area<br>(Since bank 3 is overlapping with the COMMON area, this filed must not be specified as 3.) |                                                                                                                                                                                                                                                                                       |                                                                                                                                            |    |    |    |    |     |
|         |                                     | 08BDH   | LZE                                                                                                                                        |                                                                                                                                                                                                                                                                                       |                                                                                                                                            |    |    |    |    | Z8  |
|         |                                     |         | R/W                                                                                                                                        |                                                                                                                                                                                                                                                                                       |                                                                                                                                            |    |    |    |    | R/W |
|         |                                     |         | 0                                                                                                                                          |                                                                                                                                                                                                                                                                                       |                                                                                                                                            |    |    |    |    | 0   |
|         |                                     |         | Bank for LOCAL-Z<br>0: Disable<br>1: Enable                                                                                                | Specify the bank number for the LOCAL-Z area<br>Settings of the X8 through X0 bits and their corresponding chip select signals<br>000000000 to 001111111 CSZA      100000000 to 101111111 Setting prohibited<br>010000000 to 011111111 Setting prohibited 110000000 to 111111111 CSZD |                                                                                                                                            |    |    |    |    |     |

## (9) NAND-Flash controller (1/4)

| Symbol                               | Name                     | Address                                                                  | 7                                              | 6                                                                         | 5                                       | 4                                                        | 3                                                                  | 2                                                                                   | 1                                                                      | 0                                                             |  |
|--------------------------------------|--------------------------|--------------------------------------------------------------------------|------------------------------------------------|---------------------------------------------------------------------------|-----------------------------------------|----------------------------------------------------------|--------------------------------------------------------------------|-------------------------------------------------------------------------------------|------------------------------------------------------------------------|---------------------------------------------------------------|--|
| NDFMCR0                              | NANDF Control0 Register  | 08C0H<br>(Prohibit RMW)                                                  | WE                                             | ALE                                                                       | CLE                                     | CE0                                                      | CE1                                                                | ECCE                                                                                | BUSY                                                                   | ECCRST                                                        |  |
|                                      |                          |                                                                          | R/W                                            |                                                                           |                                         |                                                          |                                                                    |                                                                                     |                                                                        |                                                               |  |
|                                      |                          |                                                                          | 0                                              | 0                                                                         | 0                                       | 0                                                        | 0                                                                  | 0                                                                                   | 0                                                                      | 0                                                             |  |
|                                      |                          |                                                                          | WE enable<br>0: Disable<br>1: Enable           | ALE control<br>0: "L" out<br>1: "H" out                                   | CLE control<br>0: "L" out<br>1: "H" out | CE0 control<br>0: "H" out<br>1: "L" out                  | CE1 control<br>0: "H" out<br>1: "L" out                            | ECC circuit control<br>0: Disable<br>1: Enable                                      | NAND Flash state<br>1: Busy<br>0: Ready                                | ECC reset control<br>0: –<br>1: Reset<br>*Always read as "0". |  |
|                                      |                          | 08C1H<br>(Prohibit RMW)                                                  | SPLW1                                          | SPLW0                                                                     | SPHW1                                   | SPHW0                                                    | RSECCL                                                             | RSEDN                                                                               | RSESTA                                                                 | RSECGW                                                        |  |
|                                      |                          |                                                                          | R/W                                            |                                                                           |                                         |                                                          |                                                                    |                                                                                     | W                                                                      | R/W                                                           |  |
|                                      |                          |                                                                          | 0                                              | 0                                                                         | 0                                       | 0                                                        | 0                                                                  | 0                                                                                   | 0                                                                      | 0                                                             |  |
|                                      |                          | Strobe pulse width<br>(Low width of $\overline{\text{NDRE}}$ ,<br>NDWE ) |                                                | Strobe pulse width<br>(High width of $\overline{\text{NDRE}}$ ,<br>NDWE ) |                                         | Reed-Solomon<br>ECC latch<br><br>0: Disable<br>1: Enable | Reed-Solomon<br>operation<br>0: Encode (Write)<br>1: Decode (Read) | Reed-Solomon<br>error calculation start<br>0: –<br>1: Start<br>*Always read as "0". | Reed-Solomon<br>ECC generator write control<br>0: Disable<br>1: Enable |                                                               |  |
|                                      |                          | Inserted width<br>= (f <sub>SYS</sub> ) × (set value)                    |                                                | Inserted width<br>= (f <sub>SYS</sub> ) × (set value)                     |                                         |                                                          |                                                                    |                                                                                     |                                                                        |                                                               |  |
| NDFMCR1                              | NANDF Control1 Register  | 08C2H                                                                    | INTERDY                                        | INTRSC                                                                    |                                         |                                                          |                                                                    | BUSW                                                                                | ECES                                                                   | SYSCKE                                                        |  |
|                                      |                          |                                                                          | R/W                                            | R/W                                                                       |                                         |                                                          |                                                                    | R/W                                                                                 | R/W                                                                    | R/W                                                           |  |
|                                      |                          |                                                                          | 0                                              | 0                                                                         |                                         |                                                          |                                                                    | 0                                                                                   | 0                                                                      | 0                                                             |  |
|                                      |                          |                                                                          | Ready interrupt<br><br>0: Disable<br>1: Enable | Reed-Solomon<br>calculation end interrupt<br>0: Disable<br>1: Enable      |                                         |                                                          |                                                                    | Data bus width<br><br>0: 8-bit<br>1: 16-bit                                         | ECC calculation<br><br>0:Hamming<br>1: Reed-Solomon                    | Clock control<br><br>0: Disable<br>1: Enable                  |  |
|                                      |                          | 08C3H                                                                    | STATE3                                         | STATE2                                                                    | STATE1                                  | STATE0                                                   | SEER1                                                              | SEER0                                                                               |                                                                        |                                                               |  |
|                                      |                          |                                                                          | R                                              |                                                                           |                                         |                                                          |                                                                    |                                                                                     |                                                                        |                                                               |  |
|                                      |                          |                                                                          | 0                                              | 0                                                                         | 0                                       | 0                                                        | Undefined                                                          | Undefined                                                                           |                                                                        |                                                               |  |
| Status read (See the table below.)   |                          |                                                                          |                                                |                                                                           |                                         |                                                          |                                                                    |                                                                                     |                                                                        |                                                               |  |
| NDECCRD0                             | NANDF Code ECC Register0 | 08C4H                                                                    | ECCD7                                          | ECCD6                                                                     | ECCD5                                   | ECCD4                                                    | ECCD3                                                              | ECCD2                                                                               | ECCD1                                                                  | ECCD0                                                         |  |
|                                      |                          |                                                                          | R                                              |                                                                           |                                         |                                                          |                                                                    |                                                                                     |                                                                        |                                                               |  |
|                                      |                          |                                                                          | 0                                              | 0                                                                         | 0                                       | 0                                                        | 0                                                                  | 0                                                                                   | 0                                                                      | 0                                                             |  |
|                                      |                          | NAND Flash ECC Register (7-0) (7-0)                                      |                                                |                                                                           |                                         |                                                          |                                                                    |                                                                                     |                                                                        |                                                               |  |
|                                      |                          | 08C5H                                                                    | ECCD15                                         | ECCD14                                                                    | ECCD13                                  | ECCD12                                                   | ECCD11                                                             | ECCD10                                                                              | ECCD9                                                                  | ECCD8                                                         |  |
|                                      |                          |                                                                          | R                                              |                                                                           |                                         |                                                          |                                                                    |                                                                                     |                                                                        |                                                               |  |
| 0                                    | 0                        |                                                                          | 0                                              | 0                                                                         | 0                                       | 0                                                        | 0                                                                  | 0                                                                                   |                                                                        |                                                               |  |
| NAND Flash ECC Register (7-0) (15-8) |                          |                                                                          |                                                |                                                                           |                                         |                                                          |                                                                    |                                                                                     |                                                                        |                                                               |  |
| NDECCRD1                             | NANDF Code ECC Register1 | 08C6H                                                                    | ECCD7                                          | ECCD6                                                                     | ECCD5                                   | ECCD4                                                    | ECCD3                                                              | ECCD2                                                                               | ECCD1                                                                  | ECCD0                                                         |  |
|                                      |                          |                                                                          | R                                              |                                                                           |                                         |                                                          |                                                                    |                                                                                     |                                                                        |                                                               |  |
|                                      |                          |                                                                          | 0                                              | 0                                                                         | 0                                       | 0                                                        | 0                                                                  | 0                                                                                   | 0                                                                      | 0                                                             |  |
|                                      |                          | NAND Flash ECC Register (7-0) (7-0)                                      |                                                |                                                                           |                                         |                                                          |                                                                    |                                                                                     |                                                                        |                                                               |  |
|                                      |                          | 08C7H                                                                    | ECCD15                                         | ECCD14                                                                    | ECCD13                                  | ECCD12                                                   | ECCD11                                                             | ECCD10                                                                              | ECCD9                                                                  | ECCD8                                                         |  |
|                                      |                          |                                                                          | R                                              |                                                                           |                                         |                                                          |                                                                    |                                                                                     |                                                                        |                                                               |  |
|                                      |                          |                                                                          | 0                                              | 0                                                                         | 0                                       | 0                                                        | 0                                                                  | 0                                                                                   | 0                                                                      | 0                                                             |  |
| NAND Flash ECC Register (7-0) (15-8) |                          |                                                                          |                                                |                                                                           |                                         |                                                          |                                                                    |                                                                                     |                                                                        |                                                               |  |

## (9) NAND-Flash controller (2/4)

| Symbol   | Name                           | Address | 7                              | 6      | 5      | 4      | 3      | 2      | 1     | 0     |
|----------|--------------------------------|---------|--------------------------------|--------|--------|--------|--------|--------|-------|-------|
| NDECCRD2 | NANDF<br>Code ECC<br>Register2 | 08C8H   | ECCD7                          | ECCD6  | ECCD5  | ECCD4  | ECCD3  | ECCD2  | ECCD1 | ECCD0 |
|          |                                |         | R                              |        |        |        |        |        |       |       |
|          |                                |         | 0                              | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|          |                                |         | NAND Flash ECC Register (7-0)  |        |        |        |        |        |       |       |
|          |                                | 08C9H   | ECCD15                         | ECCD14 | ECCD13 | ECCD12 | ECCD11 | ECCD10 | ECCD9 | ECCD8 |
|          |                                |         | R                              |        |        |        |        |        |       |       |
|          |                                |         | 0                              | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|          |                                |         | NAND Flash ECC Register (15-8) |        |        |        |        |        |       |       |
| NDECCRD3 | NANDF<br>Code ECC<br>Register3 | 08CAH   | ECCD7                          | ECCD6  | ECCD5  | ECCD4  | ECCD3  | ECCD2  | ECCD1 | ECCD0 |
|          |                                |         | R                              |        |        |        |        |        |       |       |
|          |                                |         | 0                              | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|          |                                |         | NAND Flash ECC Register (7-0)  |        |        |        |        |        |       |       |
|          |                                | 08CBH   | ECCD15                         | ECCD14 | ECCD13 | ECCD12 | ECCD11 | ECCD10 | ECCD9 | ECCD8 |
|          |                                |         | R                              |        |        |        |        |        |       |       |
|          |                                |         | 0                              | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|          |                                |         | NAND Flash ECC Register (15-8) |        |        |        |        |        |       |       |
| NDECCRD4 | NANDF<br>Code ECC<br>Register4 | 08CCH   | ECCD7                          | ECCD6  | ECCD5  | ECCD4  | ECCD3  | ECCD2  | ECCD1 | ECCD0 |
|          |                                |         | R                              |        |        |        |        |        |       |       |
|          |                                |         | 0                              | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|          |                                |         | NAND Flash ECC Register (7-0)  |        |        |        |        |        |       |       |
|          |                                | 08CDH   | ECCD15                         | ECCD14 | ECCD13 | ECCD12 | ECCD11 | ECCD10 | ECCD9 | ECCD8 |
|          |                                |         | R                              |        |        |        |        |        |       |       |
|          |                                |         | 0                              | 0      | 0      | 0      | 0      | 0      | 0     | 0     |
|          |                                |         | NAND Flash ECC Register (15-8) |        |        |        |        |        |       |       |

## (9) NAND-Flash controller (3/4)

| Symbol  | Name                                                    | Address | 7                                                                 | 6     | 5     | 4     | 3     | 2     | 1                                                                           | 0     |
|---------|---------------------------------------------------------|---------|-------------------------------------------------------------------|-------|-------|-------|-------|-------|-----------------------------------------------------------------------------|-------|
| NDRSCA0 | NANDF<br>read solomon<br>Result<br>address<br>Register0 | 08D0H   | RS0A7                                                             | RS0A6 | RS0A5 | RS0A4 | RS0A3 | RS0A2 | RS0A1                                                                       | RS0A0 |
|         |                                                         |         | R                                                                 |       |       |       |       |       |                                                                             |       |
|         |                                                         |         | 0                                                                 | 0     | 0     | 0     | 0     | 0     | 0                                                                           | 0     |
|         |                                                         |         | NAND Flash Reed-Solomon Calculation Result Address Register (7-0) |       |       |       |       |       |                                                                             |       |
|         |                                                         | 08D1H   |                                                                   |       |       |       |       |       | RS0A9                                                                       | RS0A8 |
|         |                                                         |         |                                                                   |       |       |       |       |       | R                                                                           |       |
|         |                                                         |         |                                                                   |       |       |       |       |       | 0                                                                           | 0     |
|         |                                                         |         |                                                                   |       |       |       |       |       | NAND Flash<br>Reed-Solomon<br>Calculation Result<br>Address Register (9-8)  |       |
| NDRSCD0 | NANDF<br>read solomon<br>Result data<br>Register0       | 08D2H   | RS0D7                                                             | RS0D6 | RS0D5 | RS0D4 | RS0D3 | RS0D2 | RS0D1                                                                       | RS0D0 |
|         |                                                         |         | R                                                                 |       |       |       |       |       |                                                                             |       |
|         |                                                         |         | 0                                                                 | 0     | 0     | 0     | 0     | 0     | 0                                                                           | 0     |
| NDRSCA1 | NANDF<br>read solomon<br>Result<br>address<br>Register1 | 08D4H   | RS1A7                                                             | RS1A6 | RS1A5 | RS1A4 | RS1A3 | RS1A2 | RS1A1                                                                       | RS1A0 |
|         |                                                         |         | R                                                                 |       |       |       |       |       |                                                                             |       |
|         |                                                         |         | 0                                                                 | 0     | 0     | 0     | 0     | 0     | 0                                                                           | 0     |
|         |                                                         |         | NAND Flash Reed-Solomon Calculation Result Address Register (7-0) |       |       |       |       |       |                                                                             |       |
|         |                                                         | 08D5H   |                                                                   |       |       |       |       |       | RS1A9                                                                       | RS1A8 |
|         |                                                         |         |                                                                   |       |       |       |       |       | R                                                                           |       |
|         |                                                         |         |                                                                   |       |       |       |       |       | 0                                                                           | 0     |
|         |                                                         |         |                                                                   |       |       |       |       |       | NAND Flash Reed-<br>Solomon Calculation<br>Result Address<br>Register (9-8) |       |
| NDRSCD1 | NANDF<br>read solomon<br>Result data<br>Register1       | 08D6H   | RS1D7                                                             | RS1D6 | RS1D5 | RS1D4 | RS1D3 | RS1D2 | RS1D1                                                                       | RS1D0 |
|         |                                                         |         | R                                                                 |       |       |       |       |       |                                                                             |       |
|         |                                                         |         | 0                                                                 | 0     | 0     | 0     | 0     | 0     | 0                                                                           | 0     |
| NDRSCA2 | NANDF<br>read solomon<br>Result<br>address<br>Register2 | 08D8H   | RS2A7                                                             | RS2A6 | RS2A5 | RS2A4 | RS2A3 | RS2A2 | RS2A1                                                                       | RS2A0 |
|         |                                                         |         | R                                                                 |       |       |       |       |       |                                                                             |       |
|         |                                                         |         | 0                                                                 | 0     | 0     | 0     | 0     | 0     | 0                                                                           | 0     |
|         |                                                         |         | NAND Flash Reed-Solomon Calculation Result Address Register (7-0) |       |       |       |       |       |                                                                             |       |
|         |                                                         | 08D9H   |                                                                   |       |       |       |       |       | RS2A9                                                                       | RS2A8 |
|         |                                                         |         |                                                                   |       |       |       |       |       | R                                                                           |       |
|         |                                                         |         |                                                                   |       |       |       |       |       | 0                                                                           | 0     |
|         |                                                         |         |                                                                   |       |       |       |       |       | NAND Flash Reed-<br>Solomon Calculation<br>Result Address<br>Register (9-8) |       |
| NDRSCD2 | NANDF<br>read solomon<br>Result data<br>Register2       | 08DAH   | RS2D7                                                             | RS2D6 | RS2D5 | RS2D4 | RS2D3 | RS2D2 | RS2D1                                                                       | RS2D0 |
|         |                                                         |         | R                                                                 |       |       |       |       |       |                                                                             |       |
|         |                                                         |         | 0                                                                 | 0     | 0     | 0     | 0     | 0     | 0                                                                           | 0     |
|         |                                                         |         | NAND Flash Reed-Solomon Calculation Result Data Register (7-0)    |       |       |       |       |       |                                                                             |       |

## (9) NAND-Flash controller (4/4)

| Symbol  | Name                                        | Address | 7                                                                 | 6         | 5         | 4         | 3         | 2         | 1                                                                 | 0         |
|---------|---------------------------------------------|---------|-------------------------------------------------------------------|-----------|-----------|-----------|-----------|-----------|-------------------------------------------------------------------|-----------|
| NDRSCA3 | NANDF read solomon Result address Register3 | 08DCH   | RS3A7                                                             | RS3A6     | RS3A5     | RS3A4     | RS3A3     | RS3A2     | RS3A1                                                             | RS3A0     |
|         |                                             |         | R                                                                 |           |           |           |           |           |                                                                   |           |
|         |                                             |         | 0                                                                 | 0         | 0         | 0         | 0         | 0         | 0                                                                 | 0         |
|         |                                             |         | NAND Flash Reed-Solomon Calculation Result Address Register (7-0) |           |           |           |           |           |                                                                   |           |
|         |                                             | 08DDH   |                                                                   |           |           |           |           |           | RS3A9                                                             | RS3A8     |
|         |                                             |         |                                                                   |           |           |           |           |           | R                                                                 |           |
|         |                                             |         |                                                                   |           |           |           |           |           | 0                                                                 | 0         |
|         |                                             |         |                                                                   |           |           |           |           |           | NAND Flash Reed-Solomon Calculation Result Address Register (9-8) |           |
| NDRSCD3 | NANDF read solomon Result data Register3    | 08DEH   | RS2D7                                                             | RS2D6     | RS2D5     | RS2D4     | RS2D3     | RS2D2     | RS2D1                                                             | RS2D0     |
|         |                                             |         | R                                                                 |           |           |           |           |           |                                                                   |           |
|         |                                             |         | 0                                                                 | 0         | 0         | 0         | 0         | 0         | 0                                                                 | 0         |
|         |                                             |         | NAND Flash Reed-Solomon Calculation Result Data Register (7-0)    |           |           |           |           |           |                                                                   |           |
| NDFDTR0 | NANDF Data Register0                        | 1FF0H   | D7                                                                | D6        | D5        | D4        | D3        | D2        | D1                                                                | D0        |
|         |                                             |         | R/W                                                               |           |           |           |           |           |                                                                   |           |
|         |                                             |         | Undefined                                                         | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined                                                         | Undefined |
|         |                                             |         | NAND-Flash Data Register (7-0)                                    |           |           |           |           |           |                                                                   |           |
|         |                                             | 1FF1H   | D15                                                               | D14       | D13       | D12       | D11       | D10       | D9                                                                | D8        |
|         |                                             |         | R/W                                                               |           |           |           |           |           |                                                                   |           |
|         |                                             |         | Undefined                                                         | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined                                                         | Undefined |
|         |                                             |         | NAND-Flash Data Register (15-8)                                   |           |           |           |           |           |                                                                   |           |
| NDFDTR1 | NANDF Data Register1                        | 1FF2H   | D7                                                                | D6        | D5        | D4        | D3        | D2        | D1                                                                | D0        |
|         |                                             |         | R/W                                                               |           |           |           |           |           |                                                                   |           |
|         |                                             |         | Undefined                                                         | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined                                                         | Undefined |
|         |                                             |         | NAND-Flash Data Register (7-0)                                    |           |           |           |           |           |                                                                   |           |
|         |                                             | 1FF3H   | D15                                                               | D14       | D13       | D12       | D11       | D10       | D9                                                                | D8        |
|         |                                             |         | R/W                                                               |           |           |           |           |           |                                                                   |           |
|         |                                             |         | Undefined                                                         | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined                                                         | Undefined |
|         |                                             |         | NAND-Flash Data Register (15-8)                                   |           |           |           |           |           |                                                                   |           |

## (10) DMAC (1/7)

| Symbol  | Name                                  | Address | 7                                    | 6      | 5      | 4                                                                                                                                                                                                                                                                                                           | 3      | 2      | 1      | 0      |
|---------|---------------------------------------|---------|--------------------------------------|--------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|--------|--------|
| HDMAS0  | DMA source address Register0          | 0900H   | D0SA7                                | D0SA6  | D0SA5  | D0SA4                                                                                                                                                                                                                                                                                                       | D0SA3  | D0SA2  | D0SA1  | D0SA0  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Source address for DMA0 (7:0)        |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0901H   | D0SA15                               | D0SA14 | D0SA13 | D0SA12                                                                                                                                                                                                                                                                                                      | D0SA11 | D0SA10 | D0SA9  | D0SA8  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Source address for DMA0 (15:8)       |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0902H   | D0SA23                               | D0SA22 | D0SA21 | D0SA20                                                                                                                                                                                                                                                                                                      | D0SA19 | D0SA18 | D0SA17 | D0SA16 |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Source address for DMA0 (23:16)      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMAD0  | DMA destination address Register0     | 0904H   | D0DA7                                | D0DA6  | D0DA5  | D0DA4                                                                                                                                                                                                                                                                                                       | D0DA3  | D0DA2  | D0DA1  | D0DA0  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Destination address for DMA0 (7:0)   |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0905H   | D0DA15                               | D0DA14 | D0DA13 | D0DA12                                                                                                                                                                                                                                                                                                      | D0DA11 | D0DA10 | D0DA9  | D0DA8  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Destination address for DMA0 (15:8)  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0906H   | D0DA23                               | D0DA22 | D0DA21 | D0DA20                                                                                                                                                                                                                                                                                                      | D0DA19 | D0DA18 | D0DA17 | D0DA16 |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Destination address for DMA0 (23:16) |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMACA0 | DMA Transfer count number A Register0 | 0908H   | D0CA7                                | D0CA6  | D0CA5  | D0CA4                                                                                                                                                                                                                                                                                                       | D0CA3  | D0CA2  | D0CA1  | D0CA0  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count A [7:0] for DMA0      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0909H   | D0CA15                               | D0CA14 | D0CA13 | D0CA12                                                                                                                                                                                                                                                                                                      | D0CA11 | D0CA10 | D0CA9  | D0CA8  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count A [15:8] for DMA0     |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMACB0 | DMA Transfer count number B Register0 | 090AH   | D0CB7                                | D0CB6  | D0CB5  | D0CB4                                                                                                                                                                                                                                                                                                       | D0CB3  | D0CB2  | D0CB1  | D0CB0  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count B [7:0] for DMA0      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 090BH   | D0CB15                               | D0CB14 | D0CB13 | D0CB12                                                                                                                                                                                                                                                                                                      | D0CB11 | D0CB10 | D0CB9  | D0CB8  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count B [15:8] for DMA0     |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMAM0  | DMA transfer Mode Register0           | 090CH   |                                      |        |        | D0M4                                                                                                                                                                                                                                                                                                        | D0M3   | D0M2   | D0M1   | D0M0   |
|         |                                       |         |                                      |        |        | R/W                                                                                                                                                                                                                                                                                                         |        |        |        |        |
|         |                                       |         |                                      |        |        | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         |                                      |        |        | DMA transfer mode<br>000: Destination INC (I/O → MEM)<br>001: Destination DEC (I/O → MEM)<br>010: Source INC (MEM → I/O)<br>011: Source DEC (MEM → I/O)<br>100: Source/destination INC (MEM → MEM)<br>101: Source/destination DEC (MEM → MEM)<br>110: Source/destination fixed (I/O → I/O)<br>111: Reserved |        |        |        |        |
|         |                                       |         |                                      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         |                                      |        |        | Transfer data size<br>00: 1 byte<br>01: 2 bytes<br>10: 4 bytes<br>11: Reserved                                                                                                                                                                                                                              |        |        |        |        |



## (10) DMAC (2/7)

| Symbol  | Name                                  | Address | 7                                           | 6      | 5      | 4                                                                                                                                                                                                                                                                                                           | 3      | 2      | 1      | 0      |
|---------|---------------------------------------|---------|---------------------------------------------|--------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|--------|--------|
| HDMAS1  | DMA source address Register1          | 0910H   | D1SA7                                       | D1SA6  | D1SA5  | D1SA4                                                                                                                                                                                                                                                                                                       | D1SA3  | D1SA2  | D1SA1  | D1SA0  |
|         |                                       |         | R/W                                         |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                           | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Set source address for DMA1 (7:0)           |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0911H   | D1SA15                                      | D1SA14 | D1SA13 | D1SA12                                                                                                                                                                                                                                                                                                      | D1SA11 | D1SA10 | D1SA9  | D1SA8  |
|         |                                       |         | R/W                                         |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                           | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Set source address for DMA1 (15:8)          |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0912H   | D1SA23                                      | D1SA22 | D1SA21 | D1SA20                                                                                                                                                                                                                                                                                                      | D1SA19 | D1SA18 | D1SA17 | D1SA16 |
|         |                                       |         | R/W                                         |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                           | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Set source address for DMA1 (23:16)         |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMAD1  | DMA destination address Register1     | 0914H   | D1DA7                                       | D1DA6  | D1DA5  | D1DA4                                                                                                                                                                                                                                                                                                       | D1DA3  | D1DA2  | D1DA1  | D1DA0  |
|         |                                       |         | R/W                                         |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                           | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Set destination address for DMA1 (7:0)      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0915H   | D1DA15                                      | D1DA14 | D1DA13 | D1DA12                                                                                                                                                                                                                                                                                                      | D1DA11 | D1DA10 | D1DA9  | D1DA8  |
|         |                                       |         | R/W                                         |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                           | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Set destination address for DMA1 (15:8)     |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0916H   | D1DA23                                      | D1DA22 | D1DA21 | D1DA20                                                                                                                                                                                                                                                                                                      | D1DA19 | D1DA18 | D1DA17 | D1DA16 |
|         |                                       |         | R/W                                         |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                           | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Set destination address for DMA1 (23:16)    |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMACA1 | DMA Transfer count number A Register1 | 0918H   | D1CA7                                       | D1CA6  | D1CA5  | D1CA4                                                                                                                                                                                                                                                                                                       | D1CA3  | D1CA2  | D1CA1  | D1CA0  |
|         |                                       |         | R/W                                         |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                           | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Set transfer-count-number A for DMA1 (7:0)  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0919H   | D1CA15                                      | D1CA14 | D1CA13 | D1CA12                                                                                                                                                                                                                                                                                                      | D1CA11 | D1CA10 | D1CA9  | D1CA8  |
|         |                                       |         | R/W                                         |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                           | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Set transfer-count-number A for DMA1 (15:8) |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMACB1 | DMA Transfer count number B Register1 | 091AH   | D1CB7                                       | D1CB6  | D1CB5  | D1CB4                                                                                                                                                                                                                                                                                                       | D1CB3  | D1CB2  | D1CB1  | D1CB0  |
|         |                                       |         | R/W                                         |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                           | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Set transfer-count-number B for DMA1 (7:0)  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 091BH   | D1CB15                                      | D1CB14 | D1CB13 | D1CB12                                                                                                                                                                                                                                                                                                      | D1CB11 | D1CB10 | D1CB9  | D1CB8  |
|         |                                       |         | R/W                                         |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                           | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Set transfer-count-number B for DMA1 (15:8) |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMAM1  | DMA transfer Mode Register1           | 091CH   |                                             |        |        | D1M4                                                                                                                                                                                                                                                                                                        | D1M3   | D1M2   | D1M1   | D1M0   |
|         |                                       |         |                                             |        |        | R/W                                                                                                                                                                                                                                                                                                         |        |        |        |        |
|         |                                       |         |                                             |        |        | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         |                                             |        |        | DMA transfer mode<br>000: Destination INC (I/O → MEM)<br>001: Destination DEC (I/O → MEM)<br>010: Source INC (MEM → I/O)<br>011: Source DEC (MEM → I/O)<br>100: Source/destination INC (MEM → MEM)<br>101: Source/destination DEC (MEM → MEM)<br>110: Source/destination fixed (I/O → I/O)<br>111: Reserved |        |        |        |        |
|         |                                       |         |                                             |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         |                                             |        |        | Transfer data size<br>00: 1 byte<br>01: 2 bytes<br>10: 4 bytes<br>11: Reserved                                                                                                                                                                                                                              |        |        |        |        |
|         |                                       |         |                                             |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |

## (10) DMAC (3/7)

| Symbol  | Name                                  | Address | 7                                    | 6      | 5      | 4                                                                                                                                                                                                                                                                                                           | 3      | 2      | 1      | 0      |
|---------|---------------------------------------|---------|--------------------------------------|--------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|--------|--------|
| HDMAS2  | DMA source address Register2          | 0920H   | D2SA7                                | D2SA6  | D2SA5  | D2SA4                                                                                                                                                                                                                                                                                                       | D2SA3  | D2SA2  | D2SA1  | D2SA0  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Source address for DMA2 (7:0)        |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0921H   | D2SA15                               | D2SA14 | D2SA13 | D2SA12                                                                                                                                                                                                                                                                                                      | D2SA11 | D2SA10 | D2SA9  | D2SA8  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Source address for DMA2 (15:8)       |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0922H   | D2SA23                               | D2SA22 | D2SA21 | D2SA20                                                                                                                                                                                                                                                                                                      | D2SA19 | D2SA18 | D2SA17 | D2SA16 |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Source address for DMA2 (23:16)      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMAD2  | DMA destination address Register2     | 0924H   | D2DA7                                | D2DA6  | D2DA5  | D2DA4                                                                                                                                                                                                                                                                                                       | D2DA3  | D2DA2  | D2DA1  | D2DA0  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Destination address for DMA2 (7:0)   |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0925H   | D2DA15                               | D2DA14 | D2DA13 | D2DA12                                                                                                                                                                                                                                                                                                      | D2DA11 | D2DA10 | D2DA9  | D2DA8  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Destination address for DMA2 (15:8)  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0926H   | D2DA23                               | D2DA22 | D2DA21 | D2DA20                                                                                                                                                                                                                                                                                                      | D2DA19 | D2DA18 | D2DA17 | D2DA16 |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Destination address for DMA2 (23:16) |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMACA2 | DMA Transfer count number A Register2 | 0928H   | D2CA7                                | D2CA6  | D2CA5  | D2CA4                                                                                                                                                                                                                                                                                                       | D2CA3  | D2CA2  | D2CA1  | D2CA0  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count A [7:0] for DMA2      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0929H   | D2CA15                               | D2CA14 | D2CA13 | D2CA12                                                                                                                                                                                                                                                                                                      | D2CA11 | D2CA10 | D2CA9  | D2CA8  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count A [15:8] for DMA2     |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMACB2 | DMA Transfer count number B Register2 | 092AH   | D2CB7                                | D2CB6  | D2CB5  | D2CB4                                                                                                                                                                                                                                                                                                       | D2CB3  | D2CB2  | D2CB1  | D2CB0  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count B [7:0] for DMA2      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 092BH   | D2CB15                               | D2CB14 | D2CB13 | D2CB12                                                                                                                                                                                                                                                                                                      | D2CB11 | D2CB10 | D2CB9  | D2CB8  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count A [15:8] for DMA2     |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMAM2  | DMA transfer Mode Register2           | 092CH   |                                      |        |        | D2M4                                                                                                                                                                                                                                                                                                        | D2M3   | D2M2   | D2M1   | D2M0   |
|         |                                       |         |                                      |        |        | R/W                                                                                                                                                                                                                                                                                                         |        |        |        |        |
|         |                                       |         |                                      |        |        | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         |                                      |        |        | DMA transfer mode<br>000: Destination INC (I/O → MEM)<br>001: Destination DEC (I/O → MEM)<br>010: Source INC (MEM → I/O)<br>011: Source DEC (MEM → I/O)<br>100: Source/destination INC (MEM → MEM)<br>101: Source/destination DEC (MEM → MEM)<br>110: Source/destination fixed (I/O → I/O)<br>111: Reserved |        |        |        |        |
|         |                                       |         |                                      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         |                                      |        |        | Transfer data size<br>00: 1 byte<br>01: 2 bytes<br>10: 4 bytes<br>11: Reserved                                                                                                                                                                                                                              |        |        |        |        |

## (10) DMAC (4/7)

| Symbol  | Name                                  | Address | 7                                        | 6      | 5      | 4                                                                                                                                                                                                                                                                                                           | 3      | 2      | 1      | 0      |
|---------|---------------------------------------|---------|------------------------------------------|--------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|--------|--------|
| HDMAS3  | DMA source address Register3          | 0930H   | D3SA7                                    | D3SA6  | D3SA5  | D3SA4                                                                                                                                                                                                                                                                                                       | D3SA3  | D3SA2  | D3SA1  | D3SA0  |
|         |                                       |         | R/W                                      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                        | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Set source address for DMA3 (7:0)        |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0931H   | D3SA15                                   | D3SA14 | D3SA13 | D3SA12                                                                                                                                                                                                                                                                                                      | D3SA11 | D3SA10 | D3SA9  | D3SA8  |
|         |                                       |         | R/W                                      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                        | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Set source address for DMA3 (15:8)       |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0932H   | D3SA23                                   | D3SA22 | D3SA21 | D3SA20                                                                                                                                                                                                                                                                                                      | D3SA19 | D3SA18 | D3SA17 | D3SA16 |
|         |                                       |         | R/W                                      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                        | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Set source address for DMA3 (23:16)      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMAD3  | DMA destination address Register3     | 0934H   | D3DA7                                    | D3DA6  | D3DA5  | D3DA4                                                                                                                                                                                                                                                                                                       | D3DA3  | D3DA2  | D3DA1  | D3DA0  |
|         |                                       |         | R/W                                      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                        | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Set destination address for DMA3 (7:0)   |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0935H   | D3DA15                                   | D3DA14 | D3DA13 | D3DA12                                                                                                                                                                                                                                                                                                      | D3DA11 | D3DA10 | D3DA9  | D3DA8  |
|         |                                       |         | R/W                                      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                        | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Set destination address for DMA3 (15:8)  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0936H   | D3DA23                                   | D3DA22 | D3DA21 | D3DA20                                                                                                                                                                                                                                                                                                      | D3DA19 | D3DA18 | D3DA17 | D3DA16 |
|         |                                       |         | R/W                                      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                        | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Set destination address for DMA3 (23:16) |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMACA3 | DMA Transfer count number A Register3 | 0938H   | D3CA7                                    | D3CA6  | D3CA5  | D3CA4                                                                                                                                                                                                                                                                                                       | D3CA3  | D3CA2  | D3CA1  | D3CA0  |
|         |                                       |         | R/W                                      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                        | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count A [7:0] for DMA3          |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0939H   | D3CA15                                   | D3CA14 | D3CA13 | D3CA12                                                                                                                                                                                                                                                                                                      | D3CA11 | D3CA10 | D3CA9  | D3CA8  |
|         |                                       |         | R/W                                      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                        | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count A [15:8] for DMA3         |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMACB3 | DMA Transfer count number B Register3 | 093AH   | D3CB7                                    | D3CB6  | D3CB5  | D3CB4                                                                                                                                                                                                                                                                                                       | D3CB3  | D3CB2  | D3CB1  | D3CB0  |
|         |                                       |         | R/W                                      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                        | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count B [7:0] for DMA3          |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 093BH   | D3CB15                                   | D3CB14 | D3CB13 | D3CB12                                                                                                                                                                                                                                                                                                      | D3CB11 | D3CB10 | D3CB9  | D3CB8  |
|         |                                       |         | R/W                                      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                        | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count B [15:8] for DMA3         |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMAM3  | DMA transfer Mode Register3           | 093CH   |                                          |        |        | D3M4                                                                                                                                                                                                                                                                                                        | D3M3   | D3M2   | D3M1   | D3M0   |
|         |                                       |         |                                          |        |        | R/W                                                                                                                                                                                                                                                                                                         |        |        |        |        |
|         |                                       |         |                                          |        |        | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         |                                          |        |        | DMA transfer mode<br>000: Destination INC (I/O → MEM)<br>001: Destination DEC (I/O → MEM)<br>010: Source INC (MEM → I/O)<br>011: Source DEC (MEM → I/O)<br>100: Source/destination INC (MEM → MEM)<br>101: Source/destination DEC (MEM → MEM)<br>110: Source/destination fixed (I/O → I/O)<br>111: Reserved |        |        |        |        |
|         |                                       |         |                                          |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         |                                          |        |        | Transfer data size<br>00: 1 byte<br>01: 2 bytes<br>10: 4 bytes<br>11: Reserved                                                                                                                                                                                                                              |        |        |        |        |
|         |                                       |         |                                          |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |

## (10) DMAC (5/7)

| Symbol  | Name                                  | Address | 7                                    | 6      | 5      | 4                                                                                                                                                                                                                                                                                                           | 3      | 2      | 1      | 0      |
|---------|---------------------------------------|---------|--------------------------------------|--------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|--------|--------|
| HDMAS4  | DMA source address Register4          | 0940H   | D4SA7                                | D4SA6  | D4SA5  | D4SA4                                                                                                                                                                                                                                                                                                       | D4SA3  | D4SA2  | D4SA1  | D4SA0  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Source address for DMA4 (7:0)        |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0941H   | D4SA15                               | D4SA14 | D4SA13 | D4SA12                                                                                                                                                                                                                                                                                                      | D4SA11 | D4SA10 | D4SA9  | D4SA8  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Source address for DMA4 (15:8)       |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0942H   | D4SA23                               | D4SA22 | D4SA21 | D4SA20                                                                                                                                                                                                                                                                                                      | D4SA19 | D4SA18 | D4SA17 | D4SA16 |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Source address for DMA4 (23:16)      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMAD4  | DMA destination address Register4     | 0944H   | D4DA7                                | D4DA6  | D4DA5  | D4DA4                                                                                                                                                                                                                                                                                                       | D4DA3  | D4DA2  | D4DA1  | D4DA0  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Destination address for DMA4 (7:0)   |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0945H   | D4DA15                               | D4DA14 | D4DA13 | D4DA12                                                                                                                                                                                                                                                                                                      | D4DA11 | D4DA10 | D4DA9  | D4DA8  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Destination address for DMA4 (15:8)  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0946H   | D4DA23                               | D4DA22 | D4DA21 | D4DA20                                                                                                                                                                                                                                                                                                      | D4DA19 | D4DA18 | D4DA17 | D4DA16 |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Destination address for DMA4 (23:16) |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMACA4 | DMA Transfer count number A Register4 | 0948H   | D4CA7                                | D4CA6  | D4CA5  | D4CA4                                                                                                                                                                                                                                                                                                       | D4CA3  | D4CA2  | D4CA1  | D4CA0  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count A [15:8] for DMA4     |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0949H   | D4CA15                               | D4CA14 | D4CA13 | D4CA12                                                                                                                                                                                                                                                                                                      | D4CA11 | D4CA10 | D4CA9  | D4CA8  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count A [15:8] for DMA4     |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMACB4 | DMA Transfer count number B Register4 | 094AH   | D4CB7                                | D4CB6  | D4CB5  | D4CB4                                                                                                                                                                                                                                                                                                       | D4CB3  | D4CB2  | D4CB1  | D4CB0  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count B [7:0] for DMA4      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 094BH   | D4CB15                               | D4CB14 | D4CB13 | D4CB12                                                                                                                                                                                                                                                                                                      | D4CB11 | D4CB10 | D4CB9  | D4CB8  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count B [15:8] for DMA4     |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMAM4  | DMA transfer Mode Register4           | 094CH   |                                      |        |        | D4M4                                                                                                                                                                                                                                                                                                        | D4M3   | D4M2   | D4M1   | D4M0   |
|         |                                       |         |                                      |        |        | R/W                                                                                                                                                                                                                                                                                                         |        |        |        |        |
|         |                                       |         |                                      |        |        | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         |                                      |        |        | DMA transfer mode<br>000: Destination INC (I/O → MEM)<br>001: Destination DEC (I/O → MEM)<br>010: Source INC (MEM → I/O)<br>011: Source DEC (MEM → I/O)<br>100: Source/destination INC (MEM → MEM)<br>101: Source/destination DEC (MEM → MEM)<br>110: Source/destination fixed (I/O → I/O)<br>111: Reserved |        |        |        |        |
|         |                                       |         |                                      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         |                                      |        |        | Transfer data size<br>00: 1 byte<br>01: 2 bytes<br>10: 4 bytes<br>11: Reserved                                                                                                                                                                                                                              |        |        |        |        |

## (10) DMAC (6/7)

| Symbol  | Name                                  | Address | 7                                    | 6      | 5      | 4                                                                                                                                                                                                                                                                                                           | 3      | 2      | 1      | 0      |
|---------|---------------------------------------|---------|--------------------------------------|--------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|--------|--------|
| HDMAS5  | DMA source address Register5          | 0950H   | D5SA7                                | D5SA6  | D5SA5  | D5SA4                                                                                                                                                                                                                                                                                                       | D5SA3  | D5SA2  | D5SA1  | D5SA0  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Source address for DMA5 (7:0)        |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0951H   | D5SA15                               | D5SA14 | D5SA13 | D5SA12                                                                                                                                                                                                                                                                                                      | D5SA11 | D5SA10 | D5SA9  | D5SA8  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Source address for DMA5 (15:8)       |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0952H   | D5SA23                               | D5SA22 | D5SA21 | D5SA20                                                                                                                                                                                                                                                                                                      | D5SA19 | D5SA18 | D5SA17 | D5SA16 |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Source address for DMA5 (23:16)      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMAD5  | DMA destination address Register5     | 0954H   | D5DA7                                | D5DA6  | D5DA5  | D5DA4                                                                                                                                                                                                                                                                                                       | D5DA3  | D5DA2  | D5DA1  | D5DA0  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Destination address for DMA5 (7:0)   |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0955H   | D5DA15                               | D5DA14 | D5DA13 | D5DA12                                                                                                                                                                                                                                                                                                      | D5DA11 | D5DA10 | D5DA9  | D5DA8  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Destination address for DMA5 (15:8)  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0956H   | D5DA23                               | D5DA22 | D5DA21 | D5DA20                                                                                                                                                                                                                                                                                                      | D5DA19 | D5DA18 | D5DA17 | D5DA16 |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Destination address for DMA5 (23:16) |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMACA5 | DMA Transfer count number A Register5 | 0958H   | D5CA7                                | D5CA6  | D5CA5  | D5CA4                                                                                                                                                                                                                                                                                                       | D5CA3  | D5CA2  | D5CA1  | D5CA0  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count A [7:0] for DMA5      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 0959H   | D5CA15                               | D5CA14 | D5CA13 | D5CA12                                                                                                                                                                                                                                                                                                      | D5CA11 | D5CA10 | D5CA9  | D5CA8  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count A [15:8] for DMA5     |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMACB5 | DMA Transfer count number B Register5 | 095AH   | D5CB7                                | D5CB6  | D5CB5  | D5CB4                                                                                                                                                                                                                                                                                                       | D5CB3  | D5CB2  | D5CB1  | D5CB0  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count B [7:0] for DMA5      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       | 095BH   | D5CB15                               | D5CB14 | D5CB13 | D5CB12                                                                                                                                                                                                                                                                                                      | D5CB11 | D5CB10 | D5CB9  | D5CB8  |
|         |                                       |         | R/W                                  |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         | 0                                    | 0      | 0      | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         | Transfer count B [15:8] for DMA5     |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
| HDMAM5  | DMA transfer Mode Register5           | 095CH   |                                      |        |        | D5M4                                                                                                                                                                                                                                                                                                        | D5M3   | D5M2   | D5M1   | D5M0   |
|         |                                       |         |                                      |        |        | R/W                                                                                                                                                                                                                                                                                                         |        |        |        |        |
|         |                                       |         |                                      |        |        | 0                                                                                                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
|         |                                       |         |                                      |        |        | DMA transfer mode<br>000: Destination INC (I/O → MEM)<br>001: Destination DEC (I/O → MEM)<br>010: Source INC (MEM → I/O)<br>011: Source DEC (MEM → I/O)<br>100: Source/destination INC (MEM → MEM)<br>101: Source/destination DEC (MEM → MEM)<br>110: Source/destination fixed (I/O → I/O)<br>111: Reserved |        |        |        |        |
|         |                                       |         |                                      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |
|         |                                       |         |                                      |        |        | Transfer data size<br>00: 1 byte<br>01: 2 bytes<br>10: 4 bytes<br>11: Reserved                                                                                                                                                                                                                              |        |        |        |        |
|         |                                       |         |                                      |        |        |                                                                                                                                                                                                                                                                                                             |        |        |        |        |

## (10) DMAC (7/7)

| Symbol | Name                | Address | 7                                          | 6                                                                                                                                                                                | 5                                             | 4      | 3      | 2      | 1      | 0      |
|--------|---------------------|---------|--------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|--------|--------|--------|--------|--------|
| HDMAE  | DMA enable Register | 097EH   |                                            |                                                                                                                                                                                  | DMAE5                                         | DMAE4  | DMAE3  | DMAE2  | DMAE1  | DMAE0  |
|        |                     |         |                                            |                                                                                                                                                                                  | R/W                                           |        |        |        |        |        |
|        |                     |         |                                            |                                                                                                                                                                                  | 0                                             | 0      | 0      | 0      | 0      | 0      |
|        |                     |         |                                            |                                                                                                                                                                                  | DMA channel operation<br>0: Disable 1: Enable |        |        |        |        |        |
| HDMATR | DMA timer Register  | 097FH   | DMATE                                      | DMATR6                                                                                                                                                                           | DMATR5                                        | DMATR4 | DMATR3 | DMATR2 | DMATR1 | DMATR0 |
|        |                     |         | R/W                                        |                                                                                                                                                                                  |                                               |        |        |        |        |        |
|        |                     |         | 0                                          | 0                                                                                                                                                                                | 0                                             | 0      | 0      | 0      | 0      | 0      |
|        |                     |         | Timer operation<br>0: Disable<br>1: Enable | Maximum bus occupancy time setting<br>The value to be set in <DMATR6:0> should be obtained by<br>"Maximum bus occupancy time / (256/f <sub>SYS</sub> )".<br>"00H" cannot be set. |                                               |        |        |        |        |        |

## (11) Clock gear, PLL

| Symbol | Name                           | Address | 7                                                                                                                                                                                                                                     | 6                                                                   | 5                                                                                                                                                             | 4       | 3                                                                              | 2                                                                                                                                                                   | 1                                                   | 0                                                                          |
|--------|--------------------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|--------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------|----------------------------------------------------------------------------|
| SYSCR0 | System clock control register0 | 10E0H   |                                                                                                                                                                                                                                       | XTEN                                                                | USBCLK1                                                                                                                                                       | USBCLK0 |                                                                                | WUEF                                                                                                                                                                |                                                     | PRCK                                                                       |
|        |                                |         |                                                                                                                                                                                                                                       | R/W                                                                 |                                                                                                                                                               |         |                                                                                | R/W                                                                                                                                                                 |                                                     | R/W                                                                        |
|        |                                |         |                                                                                                                                                                                                                                       | 1                                                                   | 0                                                                                                                                                             | 0       |                                                                                | 0                                                                                                                                                                   |                                                     | 0                                                                          |
|        |                                |         |                                                                                                                                                                                                                                       | Low -frequency oscillator circuit (fs)<br>0: Stop<br>1: Oscillation | Select the clock of USB(f <sub>usb</sub> )<br>00: Disable<br>01: Reserved<br>10: X1USB<br>11: f <sub>PLLUSB</sub>                                             |         |                                                                                | Warm-up timer                                                                                                                                                       |                                                     | Select Prescaler clock<br>0: f <sub>sys</sub> /2<br>1: f <sub>sys</sub> /8 |
| SYSCR1 | System clock control register1 | 10E1H   |                                                                                                                                                                                                                                       |                                                                     |                                                                                                                                                               |         |                                                                                | GEAR2                                                                                                                                                               | GEAR1                                               | GEAR0                                                                      |
|        |                                |         |                                                                                                                                                                                                                                       |                                                                     |                                                                                                                                                               |         |                                                                                | R/W                                                                                                                                                                 |                                                     |                                                                            |
|        |                                |         |                                                                                                                                                                                                                                       |                                                                     |                                                                                                                                                               |         |                                                                                | 1                                                                                                                                                                   | 0                                                   | 0                                                                          |
|        |                                |         |                                                                                                                                                                                                                                       |                                                                     |                                                                                                                                                               |         |                                                                                | Select gear value of high frequency (fc)<br>000: fc      101: (Reserved)<br>001: fc/2    110: (Reserved)<br>010: fc/4    111: (Reserved)<br>011: fc/8    100: fc/16 |                                                     |                                                                            |
| SYSCR2 | System clock control register2 | 10E2H   | –                                                                                                                                                                                                                                     | CKOSEL                                                              | WUPTM1                                                                                                                                                        | WUPTM0  | HALTM1                                                                         | HALTM0                                                                                                                                                              |                                                     |                                                                            |
|        |                                |         |                                                                                                                                                                                                                                       | R/W                                                                 |                                                                                                                                                               |         |                                                                                |                                                                                                                                                                     |                                                     |                                                                            |
|        |                                |         | 0                                                                                                                                                                                                                                     | 0                                                                   | 1                                                                                                                                                             | 0       | 1                                                                              | 1                                                                                                                                                                   |                                                     |                                                                            |
|        |                                |         | Always write "0".                                                                                                                                                                                                                     | Select CLKOUT<br>0: f <sub>sys</sub><br>1: fs                       | Warm-Up Timer<br>00: Reserved<br>01: 2 <sup>8</sup> /inputted frequency<br>10: 2 <sup>14</sup> /inputted frequency<br>11: 2 <sup>16</sup> /inputted frequency |         | HALT mode<br>00: Reserved<br>01: STOP mode<br>10: IDLE1 mode<br>11: IDLE2 mode |                                                                                                                                                                     |                                                     |                                                                            |
| EMCCR0 | EMC control register0          | 10E3H   | PROTECT                                                                                                                                                                                                                               |                                                                     |                                                                                                                                                               |         | –                                                                              | EXTIN                                                                                                                                                               | DRVOSCH                                             | DRVOSCL                                                                    |
|        |                                |         | R                                                                                                                                                                                                                                     |                                                                     |                                                                                                                                                               |         | R/W                                                                            | R/W                                                                                                                                                                 | R/W                                                 | R/W                                                                        |
|        |                                |         | 0                                                                                                                                                                                                                                     |                                                                     |                                                                                                                                                               |         | 0                                                                              | 0                                                                                                                                                                   | 1                                                   | 1                                                                          |
|        |                                |         | Protect flag<br>0: OFF<br>1: ON                                                                                                                                                                                                       |                                                                     |                                                                                                                                                               |         | Always write "0".                                                              | 1: External clock                                                                                                                                                   | fc oscillator drive ability<br>1: NORMAL<br>0: WEAK | fs oscillator drive ability<br>1: NORMAL<br>0: WEAK                        |
| EMCCR1 | EMC control register1          | 10E4H   | Switching the protect ON/OFF by write to following 1 <sup>st</sup> -KEY, 2 <sup>nd</sup> -KEY<br>1 <sup>st</sup> -KEY: EMCCR1=5AH, EMCCR2=A5H in succession write<br>2 <sup>nd</sup> -KEY: EMCCR1=A5H, EMCCR2=5AH in succession write |                                                                     |                                                                                                                                                               |         |                                                                                |                                                                                                                                                                     |                                                     |                                                                            |
| EMCCR2 | EMC control register2          | 10E5H   |                                                                                                                                                                                                                                       |                                                                     |                                                                                                                                                               |         |                                                                                |                                                                                                                                                                     |                                                     |                                                                            |
| PLLCR0 | PLL control register0          | 10E8H   |                                                                                                                                                                                                                                       | FCSEL                                                               | LUPFG                                                                                                                                                         |         |                                                                                |                                                                                                                                                                     |                                                     |                                                                            |
|        |                                |         |                                                                                                                                                                                                                                       | R/W                                                                 | R                                                                                                                                                             |         |                                                                                |                                                                                                                                                                     |                                                     |                                                                            |
|        |                                |         |                                                                                                                                                                                                                                       | 0                                                                   | 0                                                                                                                                                             |         |                                                                                |                                                                                                                                                                     |                                                     |                                                                            |
|        |                                |         |                                                                                                                                                                                                                                       | Select fc clock<br>0 : f <sub>OSCH</sub><br>1 : f <sub>PLL</sub>    | Lock-up timer<br>Status flag<br>0 : not end<br>1 : end                                                                                                        |         |                                                                                |                                                                                                                                                                     |                                                     |                                                                            |
| PLLCR1 | PLL control register1          | 10E9H   | PLL0                                                                                                                                                                                                                                  | PLL1                                                                | LUPSEL                                                                                                                                                        |         |                                                                                |                                                                                                                                                                     |                                                     | PLLTIMES                                                                   |
|        |                                |         |                                                                                                                                                                                                                                       | R/W                                                                 |                                                                                                                                                               |         |                                                                                |                                                                                                                                                                     |                                                     | R/W                                                                        |
|        |                                |         | 0                                                                                                                                                                                                                                     | 0                                                                   | 0                                                                                                                                                             |         |                                                                                |                                                                                                                                                                     |                                                     | 0                                                                          |
|        |                                |         | PLL0 for CPU<br>0: Off<br>1: On                                                                                                                                                                                                       | PLL1 for USB<br>0: Off<br>1: On                                     | Select stage of Lock up counter<br>0: 12 stage (for PLL0)<br>1: 13 stage (for PLL1)                                                                           |         |                                                                                |                                                                                                                                                                     |                                                     | Select the number of PLL<br>0: x12<br>1: x16                               |

## (12) 8-bit timer (1/2)

| Symbol  | Name                                      | Address                    | 7                                                                                                           | 6      | 5                                                                                           | 4     | 3                                                                        | 2                                                             | 1                                                                         | 0                                                    |
|---------|-------------------------------------------|----------------------------|-------------------------------------------------------------------------------------------------------------|--------|---------------------------------------------------------------------------------------------|-------|--------------------------------------------------------------------------|---------------------------------------------------------------|---------------------------------------------------------------------------|------------------------------------------------------|
| TA01RUN | TMRA01<br>RUN<br>register                 | 1100H                      | TA0RDE                                                                                                      |        |                                                                                             |       | I2TA01                                                                   | TA01PRUN                                                      | TA1RUN                                                                    | TA0RUN                                               |
|         |                                           |                            | R/W                                                                                                         |        |                                                                                             |       | R/W                                                                      |                                                               |                                                                           |                                                      |
|         |                                           |                            | 0                                                                                                           |        |                                                                                             |       | 0                                                                        | 0                                                             | 0                                                                         | 0                                                    |
|         |                                           |                            | Double<br>buffer<br>0: Disable<br>1: Enable                                                                 |        |                                                                                             |       | IDLE2<br>0: Stop<br>1: Operate                                           | TMRA01<br>prescaler<br>0: Stop and clear<br>1: Run (Count up) | Up counter<br>(UC1)                                                       | Up counter<br>(UC0)                                  |
| TA0REG  | 8-bit timer<br>register 0                 | 1102H<br>(Prohibit<br>RMW) | —                                                                                                           |        |                                                                                             |       |                                                                          |                                                               |                                                                           |                                                      |
|         |                                           |                            | W                                                                                                           |        |                                                                                             |       |                                                                          |                                                               |                                                                           |                                                      |
|         |                                           |                            | 0                                                                                                           |        |                                                                                             |       |                                                                          |                                                               |                                                                           |                                                      |
| TA1REG  | 8-bit timer<br>register 1                 | 1103H<br>(Prohibit<br>RMW) | —                                                                                                           |        |                                                                                             |       |                                                                          |                                                               |                                                                           |                                                      |
|         |                                           |                            | W                                                                                                           |        |                                                                                             |       |                                                                          |                                                               |                                                                           |                                                      |
|         |                                           |                            | 0                                                                                                           |        |                                                                                             |       |                                                                          |                                                               |                                                                           |                                                      |
| TA01MOD | TMRA01<br>MODE<br>register                | 1104H                      | TA01M1                                                                                                      | TA01M0 | PWM01                                                                                       | PWM00 | TA1CLK1                                                                  | TA1CLK0                                                       | TA0CLK1                                                                   | TA0CLK0                                              |
|         |                                           |                            | R/W                                                                                                         |        |                                                                                             |       |                                                                          |                                                               |                                                                           |                                                      |
|         |                                           |                            | 0                                                                                                           | 0      | 0                                                                                           | 0     | 0                                                                        | 0                                                             | 0                                                                         | 0                                                    |
|         |                                           |                            | Operation mode<br>00: 8-bit timer mode<br>01: 16-bit timer mode<br>10: 8-bit PPG mode<br>11: 8-bit PWM mode |        | PWM cycle<br>00: Reserved<br>01: 2 <sup>6</sup><br>10: 2 <sup>7</sup><br>11: 2 <sup>8</sup> |       | Source clock for TMRA1<br>00: TA0TRG<br>01: φT1<br>10: φT16<br>11: φT256 |                                                               | Source clock for TMRA0<br>00: TA0IN pin<br>01: φT1<br>10: φT4<br>11: φT16 |                                                      |
| TA1FFCR | TMRA1<br>Flip-Flop<br>control<br>register | 1105H<br>(Prohibit<br>RMW) |                                                                                                             |        |                                                                                             |       | TA1FFC1                                                                  | TA1FFC0                                                       | TA1FFIE                                                                   | TA1FFIS                                              |
|         |                                           |                            |                                                                                                             |        |                                                                                             |       | R/W                                                                      |                                                               | R/W                                                                       |                                                      |
|         |                                           |                            |                                                                                                             |        |                                                                                             |       | 1                                                                        | 1                                                             | 0                                                                         | 0                                                    |
|         |                                           |                            |                                                                                                             |        |                                                                                             |       | 00: Invert TA1FF<br>01: Set TA1FF<br>10: Clear TA1FF<br>11: Don't care   |                                                               | TA1FF<br>control for<br>inversion<br>0: Disable<br>1: Enable              | TA1FF<br>inversion<br>select<br>0: TMRA0<br>1: TMRA1 |
| TA23RUN | TMRA23<br>RUN<br>register                 | 1108H                      | TA2RDE                                                                                                      |        |                                                                                             |       | I2TA23                                                                   | TA23PRUN                                                      | TA3RUN                                                                    | TA2RUN                                               |
|         |                                           |                            | R/W                                                                                                         |        |                                                                                             |       | R/W                                                                      |                                                               |                                                                           |                                                      |
|         |                                           |                            | 0                                                                                                           |        |                                                                                             |       | 0                                                                        | 0                                                             | 0                                                                         | 0                                                    |
|         |                                           |                            | Double<br>buffer<br>0: Disable<br>1: Enable                                                                 |        |                                                                                             |       | IDLE2<br>0: Stop<br>1: Operate                                           | TMRA23<br>prescaler<br>0: Stop and clear<br>1: Run (Count up) | Up counter<br>(UC3)                                                       | Up counter<br>(UC2)                                  |
| TA2REG  | 8-bit timer<br>register 2                 | 110AH<br>(Prohibit<br>RMW) | —                                                                                                           |        |                                                                                             |       |                                                                          |                                                               |                                                                           |                                                      |
|         |                                           |                            | W                                                                                                           |        |                                                                                             |       |                                                                          |                                                               |                                                                           |                                                      |
|         |                                           |                            | 0                                                                                                           |        |                                                                                             |       |                                                                          |                                                               |                                                                           |                                                      |
| TA3REG  | 8-bit timer<br>register 3                 | 110BH<br>(Prohibit<br>RMW) | —                                                                                                           |        |                                                                                             |       |                                                                          |                                                               |                                                                           |                                                      |
|         |                                           |                            | W                                                                                                           |        |                                                                                             |       |                                                                          |                                                               |                                                                           |                                                      |
|         |                                           |                            | 0                                                                                                           |        |                                                                                             |       |                                                                          |                                                               |                                                                           |                                                      |
| TA23MOD | TMRA23<br>MODE<br>register                | 110CH                      | TA23M1                                                                                                      | TA23M0 | PWM21                                                                                       | PWM20 | TA3CLK1                                                                  | TA3CLK0                                                       | TA2CLK1                                                                   | TA2CLK0                                              |
|         |                                           |                            | R/W                                                                                                         |        |                                                                                             |       |                                                                          |                                                               |                                                                           |                                                      |
|         |                                           |                            | 0                                                                                                           | 0      | 0                                                                                           | 0     | 0                                                                        | 0                                                             | 0                                                                         | 0                                                    |
|         |                                           |                            | Operation mode<br>00: 8-bit timer mode<br>01: 16-bit timer mode<br>10: 8-bit PPG mode<br>11: 8-bit PWM mode |        | PWM cycle<br>00: Reserved<br>01: 2 <sup>6</sup><br>10: 2 <sup>7</sup><br>11: 2 <sup>8</sup> |       | Source clock for TMRA3<br>00: TA2TRG<br>01: φT1<br>10: φT16<br>11: φT256 |                                                               | Source clock for TMRA2<br>00: Reserved<br>01: φT1<br>10: φT4<br>11: φT16  |                                                      |
| TA3FFCR | TMRA3<br>Flip-Flop<br>control<br>register | 110DH<br>(Prohibit<br>RMW) |                                                                                                             |        |                                                                                             |       | TA3FFC1                                                                  | TA3FFC0                                                       | TA3FFIE                                                                   | TA3FFIS                                              |
|         |                                           |                            |                                                                                                             |        |                                                                                             |       | R/W                                                                      |                                                               | R/W                                                                       |                                                      |
|         |                                           |                            |                                                                                                             |        |                                                                                             |       | 1                                                                        | 1                                                             | 0                                                                         | 0                                                    |
|         |                                           |                            |                                                                                                             |        |                                                                                             |       | 00: Invert TA3FF<br>01: Set TA3FF<br>10: Clear TA3FF<br>11: Don't care   |                                                               | TA3FF<br>control for<br>inversion<br>0: Disable<br>1: Enable              | TA3FF<br>inversion<br>select<br>0: TMRA2<br>1: TMRA3 |



## (12) 8-bit timer (2/2)

| Symbol  | Name                             | Address              | 7                                                                                                           | 6      | 5                                                                                           | 4     | 3                                                                        | 2                                                          | 1                                                                           | 0                                              |
|---------|----------------------------------|----------------------|-------------------------------------------------------------------------------------------------------------|--------|---------------------------------------------------------------------------------------------|-------|--------------------------------------------------------------------------|------------------------------------------------------------|-----------------------------------------------------------------------------|------------------------------------------------|
| TA45RUN | TMRA45 RUN register              | 1110H                | TA4RDE                                                                                                      |        |                                                                                             |       | I2TA45                                                                   | TA45PRUN                                                   | TA5RUN                                                                      | TA4RUN                                         |
|         |                                  |                      | R/W                                                                                                         |        |                                                                                             |       | R/W                                                                      |                                                            |                                                                             |                                                |
|         |                                  |                      | 0                                                                                                           |        |                                                                                             |       | 0                                                                        | 0                                                          | 0                                                                           | 0                                              |
|         |                                  |                      | Double buffer<br>0: Disable<br>1: Enable                                                                    |        |                                                                                             |       | IDLE2<br>0: Stop<br>1: Operate                                           | TMRA45 prescaler<br>0: Stop and clear<br>1: Run (Count up) | Up counter (UC5)                                                            | Up counter (UC4)                               |
| TA4REG  | 8-bit timer register 4           | 1112H (Prohibit RMW) | —                                                                                                           |        |                                                                                             |       |                                                                          |                                                            |                                                                             |                                                |
|         |                                  |                      | W                                                                                                           |        |                                                                                             |       |                                                                          |                                                            |                                                                             |                                                |
|         |                                  |                      | 0                                                                                                           |        |                                                                                             |       |                                                                          |                                                            |                                                                             |                                                |
| TA5REG  | 8-bit timer register 5           | 1113H (Prohibit RMW) | —                                                                                                           |        |                                                                                             |       |                                                                          |                                                            |                                                                             |                                                |
|         |                                  |                      | W                                                                                                           |        |                                                                                             |       |                                                                          |                                                            |                                                                             |                                                |
|         |                                  |                      | 0                                                                                                           |        |                                                                                             |       |                                                                          |                                                            |                                                                             |                                                |
| TA45MOD | TMRA45 MODE register             | 1114H                | TA45M1                                                                                                      | TA45M0 | PWM41                                                                                       | PWM40 | TA5CLK1                                                                  | TA5CLK0                                                    | TA4CLK1                                                                     | TA4CLK0                                        |
|         |                                  |                      | R/W                                                                                                         |        |                                                                                             |       |                                                                          |                                                            |                                                                             |                                                |
|         |                                  |                      | 0                                                                                                           | 0      | 0                                                                                           | 0     | 0                                                                        | 0                                                          | 0                                                                           | 0                                              |
|         |                                  |                      | Operation mode<br>00: 8-bit timer mode<br>01: 16-bit timer mode<br>10: 8-bit PPG mode<br>11: 8-bit PWM mode |        | PWM cycle<br>00: Reserved<br>01: 2 <sup>6</sup><br>10: 2 <sup>7</sup><br>11: 2 <sup>8</sup> |       | Source clock for TMRA5<br>00: TA4TRG<br>01: φT1<br>10: φT16<br>11: φT256 |                                                            | Source clock for TMRA4<br>00: 32kHz clock<br>01: φT1<br>10: φT4<br>11: φT16 |                                                |
| TA67RUN | TMRA67 RUN register              | 1118H                | TA6RDE                                                                                                      |        |                                                                                             |       | I2TA67                                                                   | TA67PRUN                                                   | TA7RUN                                                                      | TA6RUN                                         |
|         |                                  |                      | R/W                                                                                                         |        |                                                                                             |       | R/W                                                                      |                                                            |                                                                             |                                                |
|         |                                  |                      | 0                                                                                                           |        |                                                                                             |       | 0                                                                        | 0                                                          | 0                                                                           | 0                                              |
|         |                                  |                      | Double buffer<br>0: Disable<br>1: Enable                                                                    |        |                                                                                             |       | IDLE2<br>0: Stop<br>1: Operate                                           | TMRA67 prescaler<br>0: Stop and clear<br>1: Run (Count up) | Up counter (UC7)                                                            | Up counter (UC6)                               |
| TA6REG  | 8-bit timer register 2           | 111AH (Prohibit RMW) | —                                                                                                           |        |                                                                                             |       |                                                                          |                                                            |                                                                             |                                                |
|         |                                  |                      | W                                                                                                           |        |                                                                                             |       |                                                                          |                                                            |                                                                             |                                                |
|         |                                  |                      | 0                                                                                                           |        |                                                                                             |       |                                                                          |                                                            |                                                                             |                                                |
| TA7REG  | 8-bit timer register 3           | 111BH (Prohibit RMW) | —                                                                                                           |        |                                                                                             |       |                                                                          |                                                            |                                                                             |                                                |
|         |                                  |                      | W                                                                                                           |        |                                                                                             |       |                                                                          |                                                            |                                                                             |                                                |
|         |                                  |                      | 0                                                                                                           |        |                                                                                             |       |                                                                          |                                                            |                                                                             |                                                |
| TA67MOD | TMRA67 MODE register             | 111CH                | TA67M1                                                                                                      | TA67M0 | PWM61                                                                                       | PWM60 | TA7CLK1                                                                  | TA7CLK0                                                    | TA6CLK1                                                                     | TA6CLK0                                        |
|         |                                  |                      | R/W                                                                                                         |        |                                                                                             |       |                                                                          |                                                            |                                                                             |                                                |
|         |                                  |                      | 0                                                                                                           | 0      | 0                                                                                           | 0     | 0                                                                        | 0                                                          | 0                                                                           | 0                                              |
|         |                                  |                      | Operation mode<br>00: 8-bit timer mode<br>01: 16-bit timer mode<br>10: 8-bit PPG mode<br>11: 8-bit PWM mode |        | PWM cycle<br>00: Reserved<br>01: 2 <sup>6</sup><br>10: 2 <sup>7</sup><br>11: 2 <sup>8</sup> |       | Source clock for TMRA7<br>00: TA6TRG<br>01: φT1<br>10: φT16<br>11: φT256 |                                                            | Source clock for TMRA6<br>00: 32kHz clock<br>01: φT1<br>10: φT4<br>11: φT16 |                                                |
| TA7FFCR | TMRA7 Flip-Flop control register | 111DH (Prohibit RMW) |                                                                                                             |        |                                                                                             |       | TA7FFC1                                                                  | TA7FFC0                                                    | TA7FFIE                                                                     | TA7FFIS                                        |
|         |                                  |                      |                                                                                                             |        |                                                                                             |       | R/W                                                                      |                                                            | R/W                                                                         |                                                |
|         |                                  |                      |                                                                                                             |        |                                                                                             |       | 1                                                                        | 1                                                          | 0                                                                           | 0                                              |
|         |                                  |                      |                                                                                                             |        |                                                                                             |       | 00: Invert TA7FF<br>01: Set TA7FF<br>10: Clear TA7FF<br>11: Don't care   |                                                            | TA7FF control for inversion<br>0: Disable<br>1: Enable                      | TA7FF inversion select<br>0: TMRA6<br>1: TMRA7 |

## (13) 16-bit timer (1/2)

| Symbol  | Name                             | Address              | 7                                               | 6                                                                   | 5                                                                                                                                                                                                                           | 4                                | 3                                                               | 2                                                                        | 1        | 0                 |  |
|---------|----------------------------------|----------------------|-------------------------------------------------|---------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|-----------------------------------------------------------------|--------------------------------------------------------------------------|----------|-------------------|--|
| TB0RUN  | TMRB0 RUN register               | 1180H                | TB0RDE                                          | –                                                                   |                                                                                                                                                                                                                             |                                  | I2TB0                                                           | TB0PRUN                                                                  |          | TB0RUN            |  |
|         |                                  |                      | R/W                                             | R/W                                                                 |                                                                                                                                                                                                                             |                                  | R/W                                                             | R/W                                                                      |          | R/W               |  |
|         |                                  |                      | 0                                               | 0                                                                   |                                                                                                                                                                                                                             |                                  | 0                                                               | 0                                                                        |          | 0                 |  |
|         |                                  |                      | Double buffer<br>0: disable<br>1: enable        | Always write “0”.                                                   |                                                                                                                                                                                                                             |                                  | IDLE2<br>0: Stop<br>1: Operate                                  | TMRB0 prescaler                                                          |          | Up counter (UC10) |  |
|         |                                  |                      | 0: Stop and clear<br>1: Run (Count up)          |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
| TB0MOD  | TMRB0 MODE register              | 1182H (Prohibit RMW) | –                                               | –                                                                   | TB0CP0I                                                                                                                                                                                                                     | TB0CPM1                          | TB0CPM0                                                         | TB0CLE                                                                   | TB0CLK1  | TB0CLK0           |  |
|         |                                  |                      | R/W                                             |                                                                     | W*                                                                                                                                                                                                                          | R/W                              |                                                                 |                                                                          |          |                   |  |
|         |                                  |                      | 0                                               | 0                                                                   | 1                                                                                                                                                                                                                           | 0                                | 0                                                               | 0                                                                        | 0        | 0                 |  |
|         |                                  |                      | Always write “00”.                              | Software capture control<br>0: Execute<br>1: Undefined              | Capture timing<br>00: Disable<br>INT6 occurs at rising edge<br>01: TB0IN0 ↑<br>INT6 occurs at rising edge<br>10: TB0IN0 ↑ TB0IN0 ↓<br>INT6 occurs at falling edge<br>11: TA1OUT ↑<br>TA1OUT ↓<br>INT6 occurs at rising edge |                                  | Control Up counter<br>0: Clear<br>Disable<br>1: Clear<br>Enable | TMRB1 source clock<br>00: TB0IN0 input<br>01: φT1<br>10: φT4<br>11: φT16 |          |                   |  |
|         |                                  |                      |                                                 |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
| TB0FFCR | TMRB0 Flip-Flop control register | 1183H (Prohibit RMW) | –                                               | –                                                                   | TB0CT1                                                                                                                                                                                                                      | TB0C0T1                          | TB0E1T1                                                         | TB0E0T1                                                                  | TB0FF0C1 | TB0FF0C0          |  |
|         |                                  |                      | W*                                              |                                                                     | R/W                                                                                                                                                                                                                         |                                  |                                                                 |                                                                          |          | W*                |  |
|         |                                  |                      | 1                                               | 1                                                                   | 0                                                                                                                                                                                                                           | 0                                | 0                                                               | 0                                                                        | 1        | 1                 |  |
|         |                                  |                      | Always write “11”.<br><br>*Always read as “11”. | TB1FF0 inversion trigger<br>0: Disable trigger<br>1: Enable trigger |                                                                                                                                                                                                                             |                                  |                                                                 | Control TB1FF0<br>00: Invert<br>01: Set<br>10: Clear<br>11: Don't care   |          |                   |  |
|         |                                  |                      | When capture UC10 to TB0CP1H/L                  | When capture UC10 to TB0CP0H/L                                      | When UC10 matches with TB0RG1H/L                                                                                                                                                                                            | When UC10 matches with TB0RG0H/L | * Always read as “11”.                                          |                                                                          |          |                   |  |
| TB0RG0L | 16 bit timer register 0 low      | 1188H (Prohibit RMW) | –                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
|         |                                  |                      | W                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
|         |                                  |                      | 0                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
| TB0RG0H | 16 bit timer register 0 high     | 1189H (Prohibit RMW) | –                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
|         |                                  |                      | W                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
|         |                                  |                      | 0                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
| TB0RG1L | 16 bit timer register low        | 118AH (Prohibit RMW) | –                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
|         |                                  |                      | W                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
|         |                                  |                      | 0                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
| TB0RG1H | 16 bit timer register 1 high     | 118BH (Prohibit RMW) | –                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
|         |                                  |                      | W                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
|         |                                  |                      | 0                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
| TB0CP0L | Capture register 0 low           | 118CH                | –                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
|         |                                  |                      | R                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
|         |                                  |                      | Undefined                                       |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
| TB0CP0H | Capture register 0 high          | 118DH                | –                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
|         |                                  |                      | R                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
|         |                                  |                      | Undefined                                       |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
| TB0CP1L | Capture register 1 low           | 118EH                | –                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
|         |                                  |                      | R                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
|         |                                  |                      | Undefined                                       |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
| TB0CP1H | Capture register 1 high          | 118FH                | –                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
|         |                                  |                      | R                                               |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |
|         |                                  |                      | Undefined                                       |                                                                     |                                                                                                                                                                                                                             |                                  |                                                                 |                                                                          |          |                   |  |

## (15) 16-bit timer (2/2)

| Symbol  | Name                               | Address                    | 7                                           | 6                                                               | 5                                                                                                                                                                                                                                       | 4                                                                   | 3                                                                        | 2                  | 1       | 0                       |
|---------|------------------------------------|----------------------------|---------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|--------------------------------------------------------------------------|--------------------|---------|-------------------------|
| TB1RUN  | TMRB1<br>RUN<br>register           | 1190H                      | TB1RDE                                      | –                                                               |                                                                                                                                                                                                                                         |                                                                     | I2TB1                                                                    | TB1PRUN            |         | TB1RUN                  |
|         |                                    |                            | R/W                                         | R/W                                                             |                                                                                                                                                                                                                                         |                                                                     | R/W                                                                      | R/W                |         | R/W                     |
|         |                                    |                            | 0                                           | 0                                                               |                                                                                                                                                                                                                                         |                                                                     | 0                                                                        | 0                  |         | 0                       |
|         |                                    |                            | Double<br>buffer<br>0: disable<br>1: enable | Always<br>write “0”.                                            |                                                                                                                                                                                                                                         |                                                                     | IDLE2<br>0: Stop<br>1: Operate                                           | TMRB1<br>prescaler |         | Up<br>counter<br>(UC12) |
|         |                                    |                            | 0: Stop and clear<br>1: Run (Count up)      |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
| TB1MOD  | TMRB1<br>MODE<br>register          | 1192H<br>(Prohibit<br>RMW) | –                                           | –                                                               | TB1CP0I                                                                                                                                                                                                                                 | TB1CPM1                                                             | TB1CPM0                                                                  | TB1CLE             | TB1CLK1 | TB1CLK0                 |
|         |                                    |                            | R/W                                         |                                                                 | W*                                                                                                                                                                                                                                      | R/W                                                                 |                                                                          |                    |         |                         |
|         |                                    |                            | 0                                           | 0                                                               | 1                                                                                                                                                                                                                                       | 0                                                                   | 0                                                                        | 0                  | 0       | 0                       |
|         |                                    |                            | Always write “00”.                          | Software<br>capture<br>control<br>0: Execute<br>1:<br>Undefined | Capture timing<br>00: Disable<br>INT7 occurs at rising<br>edge<br>01: TB1IN0 ↑<br>INT7 occurs at rising<br>edge<br>10: TB1IN0 ↑ TB1IN0 ↓<br>INT7 occurs at falling<br>edge<br>11: TA3OUT ↑<br>TA3OUT ↓<br>INT7 occurs at rising<br>edge | Control<br>Up<br>counter<br>0:Clear<br>Disable<br>1:Clear<br>Enable | TMRB1 source clock<br>00: TB1IN0 input<br>01: φT1<br>10: φT4<br>11: φT16 |                    |         |                         |
|         |                                    |                            |                                             |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
| TB1RG0L | 16 bit timer<br>register 0<br>low  | 1198H<br>(Prohibit<br>RMW) | –                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
|         |                                    |                            | W                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
|         |                                    |                            | 0                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
| TB1RG0H | 16 bit timer<br>register 0<br>high | 1199H<br>(Prohibit<br>RMW) | –                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
|         |                                    |                            | W                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
|         |                                    |                            | 0                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
| TB1RG1L | 16 bit timer<br>register low       | 119AH<br>(Prohibit<br>RMW) | –                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
|         |                                    |                            | W                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
|         |                                    |                            | 0                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
| TB1RG1H | 16 bit timer<br>register 1<br>high | 119BH<br>(Prohibit<br>RMW) | –                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
|         |                                    |                            | W                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
|         |                                    |                            | 0                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
| TB1CP0L | Capture<br>register 0<br>low       | 119CH                      | –                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
|         |                                    |                            | R                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
|         |                                    |                            | Undefined                                   |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
| TB1CP0H | Capture<br>register 0<br>high      | 119DH                      | –                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
|         |                                    |                            | R                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
|         |                                    |                            | Undefined                                   |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
| TB1CP1L | Capture<br>register 1<br>low       | 119EH                      | –                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
|         |                                    |                            | R                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
|         |                                    |                            | Undefined                                   |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
| TB1CP1H | Capture<br>register 1<br>high      | 119FH                      | –                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
|         |                                    |                            | R                                           |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |
|         |                                    |                            | Undefined                                   |                                                                 |                                                                                                                                                                                                                                         |                                                                     |                                                                          |                    |         |                         |

## (14) UART/Serial channels (1/2)

| Symbol  | Name                                        | Address                 | 7                                                 | 6                                              | 5                                                           | 4                                    | 3                                                                                                                                                                      | 2          | 1                                                                                                               | 0                                            |
|---------|---------------------------------------------|-------------------------|---------------------------------------------------|------------------------------------------------|-------------------------------------------------------------|--------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----------------------------------------------------------------------------------------------------------------|----------------------------------------------|
| SC0BUF  | Serial channel 0 buffer register            | 1200H<br>(Prohibit RMW) | RB7<br>TB7                                        | RB6<br>TB6                                     | RB5<br>TB5                                                  | RB4<br>TB4                           | RB3<br>TB3                                                                                                                                                             | RB2<br>TB2 | RB1<br>TB1                                                                                                      | RB0<br>TB0                                   |
|         |                                             |                         | R (Receive) /W (Transmission)                     |                                                |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
|         |                                             |                         | Undefined                                         |                                                |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
| SC0CR   | Serial channel 0 control register           | 1201H<br>(Prohibit RMW) | RB8                                               | EVEN                                           | PE                                                          | OERR                                 | PERR                                                                                                                                                                   | FERR       | SCLKS                                                                                                           | IOC                                          |
|         |                                             |                         | R                                                 | R/W                                            |                                                             | R (Cleared to 0 when read)           |                                                                                                                                                                        |            | R/W                                                                                                             |                                              |
|         |                                             |                         | Undefined                                         | 0                                              | 0                                                           | 0                                    | 0                                                                                                                                                                      | 0          | 0                                                                                                               | 0                                            |
|         |                                             |                         | Received data bit8                                | Parity<br>0: Odd<br>1: Even                    | Parity addition<br>0: Disable<br>1: Enable                  | 1: Error                             |                                                                                                                                                                        |            | 0: SCLK0↑<br>1: SCLK0↓                                                                                          | 0: baud rate generator<br>1: SCLK0 pin input |
|         |                                             |                         |                                                   |                                                |                                                             | Overrun                              | Parity                                                                                                                                                                 | Framing    |                                                                                                                 |                                              |
| SC0MOD0 | Serial channel 0 mode 0 register            | 1202H                   | TB8                                               | CTSE                                           | RXE                                                         | WU                                   | SM1                                                                                                                                                                    | SM0        | SC1                                                                                                             | SC0                                          |
|         |                                             |                         | R/W                                               |                                                |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
|         |                                             |                         | 0                                                 | 0                                              | 0                                                           | 0                                    | 0                                                                                                                                                                      | 0          | 0                                                                                                               | 0                                            |
|         |                                             |                         | Transfer data bit 8                               | 0: CTS disable<br>1: CTS enable                | Receive function<br>0: Receive disable<br>1: Receive enable | Wake up<br>0: Disable<br>1: Enable   | 00: I/O interface Mode<br>01: 7-bit UART Mode<br>10: 8-bit UART Mode<br>11: 9-bit UART Mode                                                                            |            | 00: TA0TRG<br>01: Baud rate generator<br>10: Internal clock f <sub>IO</sub><br>11: External clock (SCLK0 input) |                                              |
| BR0CR   | Serial channel 0 baud rate control register | 1203H                   | –                                                 | BR0ADDE                                        | BR0CK1                                                      | BR0CK0                               | BR0S3                                                                                                                                                                  | BR0S2      | BR0S1                                                                                                           | BR0S0                                        |
|         |                                             |                         | R/W                                               |                                                |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
|         |                                             |                         | 0                                                 | 0                                              | 0                                                           | 0                                    | 0                                                                                                                                                                      | 0          | 0                                                                                                               | 0                                            |
|         |                                             |                         | Always write "0".                                 | (16–K) /16 division<br>0: Disable<br>1: Enable | 00: φT0<br>01: φT2<br>10: φT8<br>11: φT32                   | Divided frequency "N" setting<br>0–F |                                                                                                                                                                        |            |                                                                                                                 |                                              |
| BR0ADD  | Serial channel 0 K setting register         | 1204H                   |                                                   |                                                |                                                             |                                      | BR0K3                                                                                                                                                                  | BR0K2      | BR0K1                                                                                                           | BR0K0                                        |
|         |                                             |                         |                                                   |                                                |                                                             |                                      | R/W                                                                                                                                                                    |            |                                                                                                                 |                                              |
|         |                                             |                         |                                                   |                                                |                                                             |                                      | 0                                                                                                                                                                      | 0          | 0                                                                                                               | 0                                            |
| SC0MOD1 | Serial channel 0 mode 1 register            | 1205H                   | Sets frequency divisor "K" (1–F)                  |                                                |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
|         |                                             |                         | I2S0                                              | FDPX0                                          |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
|         |                                             |                         | R/W                                               |                                                |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
|         |                                             |                         | 0                                                 | 0                                              |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
| SIR0CR  | IrDA 0 control register                     | 1207H                   | IDLE2<br>0: Stop<br>1: Run                        | Duplex<br>0: Half<br>1: Full                   |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
|         |                                             |                         | PLSEL                                             | RXSEL                                          | TXEN                                                        | RXEN                                 | SIR0WD3                                                                                                                                                                | SIR0WD2    | SIR0WD1                                                                                                         | SIR0WD0                                      |
|         |                                             |                         | R/W                                               |                                                |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
|         |                                             |                         | 0                                                 | 0                                              | 0                                                           | 0                                    | 0                                                                                                                                                                      | 0          | 0                                                                                                               | 0                                            |
|         |                                             |                         | Select transmit pulse width<br>0: 3/16<br>1: 1/16 | Receive data<br>0: "H" pulse<br>1: "L" pulse   | Transmit<br>0: Disable<br>1: Enable                         | Receive<br>0: Disable<br>1: Enable   | Select receive pulse width<br>Set the valid SIRR×D pulse width for equal or more than<br>2x × (setting value + 1) + 100ns<br>Can be set: 1–14<br>Can not be set: 0, 15 |            |                                                                                                                 |                                              |

## (14) UART/Serial channels (2/2)

| Symbol  | Name                                        | Address              | 7                                                 | 6                                              | 5                                                           | 4                                    | 3                                                                                                                                                                      | 2          | 1                                                                                                               | 0                                            |
|---------|---------------------------------------------|----------------------|---------------------------------------------------|------------------------------------------------|-------------------------------------------------------------|--------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----------------------------------------------------------------------------------------------------------------|----------------------------------------------|
| SC1BUF  | Serial channel 1 buffer register            | 1208H (Prohibit RMW) | RB7<br>TB7                                        | RB6<br>TB6                                     | RB5<br>TB5                                                  | RB4<br>TB4                           | RB3<br>TB3                                                                                                                                                             | RB2<br>TB2 | RB1<br>TB1                                                                                                      | RB0<br>TB0                                   |
|         |                                             |                      | R (Receive) /W (Transmission)                     |                                                |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
|         |                                             |                      | Undefined                                         |                                                |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
| SC1CR   | Serial channel 1 control register           | 1209H (Prohibit RMW) | RB8                                               | EVEN                                           | PE                                                          | OERR                                 | PERR                                                                                                                                                                   | FERR       | SCLKS                                                                                                           | IOC                                          |
|         |                                             |                      | R                                                 | R/W                                            |                                                             | R (Cleared to 0 when read)           |                                                                                                                                                                        |            | R/W                                                                                                             |                                              |
|         |                                             |                      | Undefined                                         | 0                                              | 0                                                           | 0                                    | 0                                                                                                                                                                      | 0          | 0                                                                                                               | 0                                            |
|         |                                             |                      | Received data bit8                                | Parity<br>0: Odd<br>1: Even                    | Parity addition<br>0: Disable<br>1: Enable                  | 1: Error                             |                                                                                                                                                                        |            | 0: SCLK1↑<br>1: SCLK1↓                                                                                          | 0: baud rate generator<br>1: SCLK1 pin input |
|         |                                             |                      |                                                   |                                                |                                                             | Overrun                              | Parity                                                                                                                                                                 | Framing    |                                                                                                                 |                                              |
| SC1MOD0 | Serial channel 1 mode 0 register            | 120AH                | TB8                                               | CTSE                                           | RXE                                                         | WU                                   | SM1                                                                                                                                                                    | SM0        | SC1                                                                                                             | SC0                                          |
|         |                                             |                      | R/W                                               |                                                |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
|         |                                             |                      | 0                                                 | 0                                              | 0                                                           | 0                                    | 0                                                                                                                                                                      | 0          | 0                                                                                                               | 0                                            |
|         |                                             |                      | Transfer data bit 8                               | 0: CTS disable<br>1: CTS enable                | Receive function<br>0: Receive disable<br>1: Receive enable | Wake up<br>0: Disable<br>1: Enable   | 00: I/O interface Mode<br>01: 7-bit UART Mode<br>10: 8-bit UART Mode<br>11: 9-bit UART Mode                                                                            |            | 00: TA0TRG<br>01: Baud rate generator<br>10: Internal clock f <sub>IO</sub><br>11: External clock (SCLK1 input) |                                              |
| BR1CR   | Serial channel 1 baud rate control register | 120CH                | –                                                 | BR1ADDE                                        | BR1CK1                                                      | BR1CK0                               | BR1S3                                                                                                                                                                  | BR1S2      | BR1S1                                                                                                           | BR1S0                                        |
|         |                                             |                      | R/W                                               |                                                |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
|         |                                             |                      | 0                                                 | 0                                              | 0                                                           | 0                                    | 0                                                                                                                                                                      | 0          | 0                                                                                                               | 0                                            |
|         |                                             |                      | Always write "0".                                 | (16–K) /16 division<br>0: Disable<br>1: Enable | 00: φT0<br>01: φT2<br>10: φT8<br>11: φT32                   | Divided frequency "N" setting<br>0–F |                                                                                                                                                                        |            |                                                                                                                 |                                              |
| BR1ADD  | Serial channel 1 K setting register         | 120DH                |                                                   |                                                |                                                             |                                      | BR1K3                                                                                                                                                                  | BR1K2      | BR1K1                                                                                                           | BR1K0                                        |
|         |                                             |                      |                                                   |                                                |                                                             |                                      | R/W                                                                                                                                                                    |            |                                                                                                                 |                                              |
|         |                                             |                      |                                                   |                                                |                                                             |                                      | 0                                                                                                                                                                      | 0          | 0                                                                                                               | 0                                            |
| SC0MOD1 | Serial channel 0 mode 1 register            | 1205H                | Sets frequency divisor "K" (1–F)                  |                                                |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
|         |                                             |                      | I2S1                                              | FDPX1                                          |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
|         |                                             |                      | R/W                                               |                                                |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
|         |                                             |                      | 0                                                 | 0                                              |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
| SIR1CR  | IrDA 1 control register                     | 120FH                | IDLE2<br>0: Stop<br>1: Run                        | Duplex<br>0: Half<br>1: Full                   |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
|         |                                             |                      | PLSEL                                             | RXSEL                                          | TXEN                                                        | RXEN                                 | SIR1WD3                                                                                                                                                                | SIR1WD2    | SIR1WD1                                                                                                         | SIR1WD0                                      |
|         |                                             |                      | R/W                                               |                                                |                                                             |                                      |                                                                                                                                                                        |            |                                                                                                                 |                                              |
|         |                                             |                      | 0                                                 | 0                                              | 0                                                           | 0                                    | 0                                                                                                                                                                      | 0          | 0                                                                                                               | 0                                            |
|         |                                             |                      | Select transmit pulse width<br>0: 3/16<br>1: 1/16 | Receive data<br>0: "H" pulse<br>1: "L" pulse   | Transmit<br>0: Disable<br>1: Enable                         | Receive<br>0: Disable<br>1: Enable   | Select receive pulse width<br>Set the valid SIRR×D pulse width for equal or more than<br>2x × (setting value + 1) + 100ns<br>Can be set: 1–14<br>Can not be set: 0, 15 |            |                                                                                                                 |                                              |

## (15) SBI

| Symbol               | Name                                      | Address                 | 7                                                                                                       | 6                                                                      | 5                                                              | 4                                                                               | 3                                                                                                                                   | 2                                                                                                                                             | 1                                                                                        | 0                                              |
|----------------------|-------------------------------------------|-------------------------|---------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------|----------------------------------------------------------------|---------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------|------------------------------------------------|
| SBICR1               | Serial bus interface control register 1   | 1240H<br>(Prohibit RMW) | BC2                                                                                                     | BC1                                                                    | BC0                                                            | ACK                                                                             | –                                                                                                                                   | SCK2                                                                                                                                          | SCK1                                                                                     | SCK0 /SWRMON                                   |
|                      |                                           |                         | R/W                                                                                                     |                                                                        |                                                                |                                                                                 | R                                                                                                                                   | R/W                                                                                                                                           |                                                                                          | R/W                                            |
|                      |                                           |                         | 0                                                                                                       | 0                                                                      | 0                                                              | 0                                                                               | 1                                                                                                                                   | 0                                                                                                                                             | 0                                                                                        | 0/1                                            |
|                      |                                           |                         | Number of transfer bits<br>000: 8    001: 1    010: 2<br>011: 3    100: 4    101: 5<br>110: 6    111: 7 |                                                                        |                                                                | Acknowledge mode specification<br>0: Disable<br>1: Enable                       | Always read as "1".                                                                                                                 | Setting for the divisor value "n"<br>(When writing)<br>000: 4    001: 5    010: 6<br>011: 7    100: 8    101: 9<br>110: 10    111: (Reserved) |                                                                                          |                                                |
| SBIDBR               | SBI buffer register                       | 1241H<br>(Prohibit RMW) | DB7                                                                                                     | DB6                                                                    | DB5                                                            | DB4                                                                             | DB3                                                                                                                                 | DB2                                                                                                                                           | DB1                                                                                      | DB0                                            |
|                      |                                           |                         | R (receive)/W (Transmit)                                                                                |                                                                        |                                                                |                                                                                 |                                                                                                                                     |                                                                                                                                               |                                                                                          |                                                |
|                      |                                           |                         | Undefined                                                                                               |                                                                        |                                                                |                                                                                 |                                                                                                                                     |                                                                                                                                               |                                                                                          |                                                |
| I2CAR                | I <sup>2</sup> C BUS Address register     | 1242H<br>(Prohibit RMW) | SA6                                                                                                     | SA5                                                                    | SA4                                                            | SA3                                                                             | SA2                                                                                                                                 | SA1                                                                                                                                           | SA0                                                                                      | ALS                                            |
|                      |                                           |                         | R/W                                                                                                     |                                                                        |                                                                |                                                                                 |                                                                                                                                     |                                                                                                                                               |                                                                                          |                                                |
|                      |                                           |                         | 0                                                                                                       | 0                                                                      | 0                                                              | 0                                                                               | 0                                                                                                                                   | 0                                                                                                                                             | 0                                                                                        | 0                                              |
|                      |                                           |                         | Slave Address setting                                                                                   |                                                                        |                                                                |                                                                                 |                                                                                                                                     |                                                                                                                                               |                                                                                          | Address recognition<br>0: Enable<br>1: Disable |
| SBISR<br>When read   | Serial bus interface status register      | 1243H<br>(Prohibit RMW) | MST                                                                                                     | TRX                                                                    | BB                                                             | PIN                                                                             | AL/SBIM1                                                                                                                            | AAS/SBIM0                                                                                                                                     | AD0/SWRST1                                                                               | LRB/SWRST0                                     |
|                      |                                           |                         | R/W                                                                                                     |                                                                        |                                                                |                                                                                 |                                                                                                                                     |                                                                                                                                               |                                                                                          |                                                |
|                      |                                           |                         | 0                                                                                                       | 0                                                                      | 0                                                              | 1                                                                               | 0                                                                                                                                   | 0                                                                                                                                             | 0                                                                                        | 0                                              |
|                      |                                           |                         | Master/Slave status monitor<br>0: Slave<br>1: Master                                                    | Transmitter / Receiver status monitor<br>0: Receiver<br>1: Transmitter | I <sup>2</sup> C bus status monitor<br>0: Free<br>1: Busy      | INTSBI request monitor<br>0: Request<br>1: Cancel                               | Arbitration lost detection monitor<br>0: –<br>1: Detected                                                                           | Slave Address match detection monitor<br>0: Undetected<br>1: Detected                                                                         | General call detection monitor<br>0: Undetected<br>1: Detected                           | Last receive bit monitor<br>0: "0"<br>1: "1"   |
| SBICR2<br>When write | Serial bus interface control register 2   |                         |                                                                                                         |                                                                        | Start/Stop condition<br>0: Stop condition<br>1: Busy condition | Cancel INTSBI interrupt request<br>0: Don't care<br>1: Cancel interrupt request | Serial bus interface operation mode selection<br>00: Port mode<br>01: (Reserved)<br>10: I <sup>2</sup> C bus mode<br>11: (Reserved) |                                                                                                                                               | Software reset generate write "10" and "01", then an internal reset signal is generated. |                                                |
| SBIBR0               | Serial bus interface baud rate register 0 | 1244H<br>(Prohibit RMW) | –                                                                                                       | I2SBI                                                                  | –                                                              | –                                                                               | –                                                                                                                                   | –                                                                                                                                             | –                                                                                        | –                                              |
|                      |                                           |                         | W                                                                                                       | R/W                                                                    | R                                                              |                                                                                 |                                                                                                                                     |                                                                                                                                               |                                                                                          | R/W                                            |
|                      |                                           |                         | 0                                                                                                       | 0                                                                      | 1                                                              | 1                                                                               | 1                                                                                                                                   | 1                                                                                                                                             | 1                                                                                        | 0                                              |
|                      |                                           |                         | Always read "0"                                                                                         | IDLE2<br>0: Stop<br>1: Operate                                         | Always read as "1".                                            |                                                                                 |                                                                                                                                     |                                                                                                                                               |                                                                                          | Always write "0".                              |
| SBICR0               | Serial bus interface control register 0   | 1247H<br>(Prohibit RMW) | SBIEN                                                                                                   | –                                                                      | –                                                              | –                                                                               | –                                                                                                                                   | –                                                                                                                                             | –                                                                                        | –                                              |
|                      |                                           |                         | R/W                                                                                                     | R                                                                      |                                                                |                                                                                 |                                                                                                                                     |                                                                                                                                               |                                                                                          |                                                |
|                      |                                           |                         | 0                                                                                                       | 0                                                                      | 0                                                              | 0                                                                               | 0                                                                                                                                   | 0                                                                                                                                             | 0                                                                                        | 0                                              |
|                      |                                           |                         | SBI operation<br>0: disable<br>1: enable                                                                | Always read as "0".                                                    |                                                                |                                                                                 |                                                                                                                                     |                                                                                                                                               |                                                                                          |                                                |

## (16) AD converter (1/3)

| Symbol  | Name                                 | Address | 7                                              | 6     | 5     | 4     | 3     | 2     | 1                                             | 0                                            |
|---------|--------------------------------------|---------|------------------------------------------------|-------|-------|-------|-------|-------|-----------------------------------------------|----------------------------------------------|
| ADREG0L | AD conversion result register 0 low  | 12A0H   | ADR01                                          | ADR00 |       |       |       |       | OVR0                                          | ADR0RF                                       |
|         |                                      |         | R                                              |       |       |       |       |       | R                                             |                                              |
|         |                                      |         | 0                                              | 0     |       |       |       |       | 0                                             | 0                                            |
|         |                                      |         | Store Lower 2 bits of AN0 AD conversion result |       |       |       |       |       | Overrun flag<br>0: No generate<br>1: Generate | AD conversion result store flag<br>1: Stored |
| ADREG0H | AD conversion result register 0 high | 12A1H   | ADR09                                          | ADR08 | ADR07 | ADR06 | ADR05 | ADR04 | ADR03                                         | ADR02                                        |
|         |                                      |         | R                                              |       |       |       |       |       |                                               |                                              |
|         |                                      |         | 0                                              | 0     | 0     | 0     | 0     | 0     | 0                                             | 0                                            |
|         |                                      |         | Store Upper 8 bits of an AN0 conversion result |       |       |       |       |       |                                               |                                              |
| ADREG1L | AD conversion result register 1 low  | 12A2H   | ADR11                                          | ADR10 |       |       |       |       | OVR1                                          | ADR1RF                                       |
|         |                                      |         | R                                              |       |       |       |       |       | R                                             |                                              |
|         |                                      |         | 0                                              | 0     |       |       |       |       | 0                                             | 0                                            |
|         |                                      |         | Store Lower 2 bits of AN1 AD conversion result |       |       |       |       |       | Overrun flag<br>0: No generate<br>1: Generate | AD conversion result store flag<br>1: Stored |
| ADREG1H | AD conversion result register 1 high | 12A3H   | ADR19                                          | ADR18 | ADR17 | ADR16 | ADR15 | ADR14 | ADR13                                         | ADR12                                        |
|         |                                      |         | R                                              |       |       |       |       |       |                                               |                                              |
|         |                                      |         | 0                                              | 0     | 0     | 0     | 0     | 0     | 0                                             | 0                                            |
|         |                                      |         | Store Upper 8 bits of an AN1 conversion result |       |       |       |       |       |                                               |                                              |
| ADREG2L | AD conversion result register 2 low  | 12A4H   | ADR21                                          | ADR20 |       |       |       |       | OVR2                                          | ADR2RF                                       |
|         |                                      |         | R                                              |       |       |       |       |       | R                                             |                                              |
|         |                                      |         | 0                                              | 0     |       |       |       |       | 0                                             | 0                                            |
|         |                                      |         | Store Lower 2 bits of AN2 AD conversion result |       |       |       |       |       | Overrun flag<br>0: No generate<br>1: Generate | AD conversion result store flag<br>1: Stored |
| ADREG2H | AD conversion result register 2 high | 12A5H   | ADR29                                          | ADR28 | ADR27 | ADR26 | ADR25 | ADR24 | ADR23                                         | ADR22                                        |
|         |                                      |         | R                                              |       |       |       |       |       |                                               |                                              |
|         |                                      |         | 0                                              | 0     | 0     | 0     | 0     | 0     | 0                                             | 0                                            |
|         |                                      |         | Store Upper 8 bits of an AN2 conversion result |       |       |       |       |       |                                               |                                              |
| ADREG3L | AD conversion result register 3 low  | 12A6H   | ADR31                                          | ADR30 |       |       |       |       | OVR3                                          | ADR3RF                                       |
|         |                                      |         | R                                              |       |       |       |       |       | R                                             |                                              |
|         |                                      |         | 0                                              | 0     |       |       |       |       | 0                                             | 0                                            |
|         |                                      |         | Store Lower 2 bits of AN3 AD conversion result |       |       |       |       |       | Overrun flag<br>0: No generate<br>1: Generate | AD conversion result store flag<br>1: Stored |
| ADREG3H | AD conversion result register 3 high | 12A7H   | ADR39                                          | ADR38 | ADR37 | ADR36 | ADR35 | ADR34 | ADR33                                         | ADR32                                        |
|         |                                      |         | R                                              |       |       |       |       |       |                                               |                                              |
|         |                                      |         | 0                                              | 0     | 0     | 0     | 0     | 0     | 0                                             | 0                                            |
|         |                                      |         | Store Upper 8 bits of an AN3 conversion result |       |       |       |       |       |                                               |                                              |
| ADREG4L | AD conversion result register 4 low  | 12A8H   | ADR4                                           | ADR4  |       |       |       |       | OVR4                                          | ADR4F                                        |
|         |                                      |         | R                                              |       |       |       |       |       | R                                             |                                              |
|         |                                      |         | 0                                              | 0     |       |       |       |       | 0                                             | 0                                            |
|         |                                      |         | Store Lower 2 bits of AN4 AD conversion result |       |       |       |       |       | Overrun flag<br>0: No generate<br>1: Generate | AD conversion result store flag<br>1: Stored |
| ADREG4H | AD conversion result register 4 high | 12A9H   | ADR49                                          | ADR48 | ADR47 | ADR46 | ADR45 | ADR44 | ADR43                                         | ADR42                                        |
|         |                                      |         | R                                              |       |       |       |       |       |                                               |                                              |
|         |                                      |         | 0                                              | 0     | 0     | 0     | 0     | 0     | 0                                             | 0                                            |
|         |                                      |         | Store Upper 8 bits of an AN4 conversion result |       |       |       |       |       |                                               |                                              |
| ADREG5L | AD conversion result register 5 low  | 12AAH   | ADR5                                           | ADR5  |       |       |       |       | OVR5                                          | ADR5F                                        |
|         |                                      |         | R                                              |       |       |       |       |       | R                                             |                                              |
|         |                                      |         | 0                                              | 0     |       |       |       |       | 0                                             | 0                                            |
|         |                                      |         | Store Lower 2 bits of AN5 AD conversion result |       |       |       |       |       | Overrun flag<br>0: No generate<br>1: Generate | AD conversion result store flag<br>1: Stored |
| ADREG5H | AD conversion result register 5 high | 12ABH   | ADR59                                          | ADR58 | ADR57 | ADR56 | ADR55 | ADR54 | ADR53                                         | ADR52                                        |
|         |                                      |         | R                                              |       |       |       |       |       |                                               |                                              |
|         |                                      |         | 0                                              | 0     | 0     | 0     | 0     | 0     | 0                                             | 0                                            |
|         |                                      |         | Store Upper 8 bits of an AN5 conversion result |       |       |       |       |       |                                               |                                              |

## (16) AD converter (2/3)

| Symbol    | Name                                                   | Address | 7                                                                                                                    | 6                                                                            | 5      | 4                                                      | 3                                                                                            | 2                                                                    | 1                                                                                              | 0                                            |
|-----------|--------------------------------------------------------|---------|----------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------|--------|--------------------------------------------------------|----------------------------------------------------------------------------------------------|----------------------------------------------------------------------|------------------------------------------------------------------------------------------------|----------------------------------------------|
| ADREGSPL  | High priority Conversion Register SP low               | 12B0H   | ADRSP1                                                                                                               | ADRSP0                                                                       |        |                                                        |                                                                                              |                                                                      | OVS RP                                                                                         | ADRSPRF                                      |
|           |                                                        |         | R                                                                                                                    |                                                                              |        |                                                        |                                                                                              |                                                                      | R                                                                                              |                                              |
|           |                                                        |         | 0                                                                                                                    | 0                                                                            |        |                                                        |                                                                                              |                                                                      | 0                                                                                              | 0                                            |
|           |                                                        |         | Store Lower 2 bits of an AD conversion result                                                                        |                                                                              |        |                                                        |                                                                                              |                                                                      | Overrun<br>1: Generate                                                                         | AD conversion result store flag<br>1: Stored |
| ADREGSPH  | High priority Conversion Register SP high              | 12B1H   | ADRSP9                                                                                                               | ADRSP8                                                                       | ADRSP7 | ADRSP6                                                 | ADRSP5                                                                                       | ADRSP4                                                               | ADRSP3                                                                                         | ADRSP2                                       |
|           |                                                        |         | R                                                                                                                    |                                                                              |        |                                                        |                                                                                              |                                                                      |                                                                                                |                                              |
|           |                                                        |         | 0                                                                                                                    | 0                                                                            | 0      | 0                                                      | 0                                                                                            | 0                                                                    | 0                                                                                              | 0                                            |
|           |                                                        |         | Store Upper 8 bits of an AD conversion result                                                                        |                                                                              |        |                                                        |                                                                                              |                                                                      |                                                                                                |                                              |
| ADCM0REGL | AD Conversion Result Compare Criterion Register 0 Low  | 12B4H   | ADR21                                                                                                                | ADR20                                                                        |        |                                                        |                                                                                              |                                                                      |                                                                                                |                                              |
|           |                                                        |         | R/W                                                                                                                  |                                                                              |        |                                                        |                                                                                              |                                                                      |                                                                                                |                                              |
|           |                                                        |         | 0                                                                                                                    | 0                                                                            |        |                                                        |                                                                                              |                                                                      |                                                                                                |                                              |
|           |                                                        |         | Store Lower 2 bits of an AD conversion result compare criterion                                                      |                                                                              |        |                                                        |                                                                                              |                                                                      |                                                                                                |                                              |
| ADCM0REGH | AD Conversion Result Compare Criterion Register 0 High | 12B5H   | ADR29                                                                                                                | ADR28                                                                        | ADR27  | ADR26                                                  | ADR25                                                                                        | ADR24                                                                | ADR23                                                                                          | ADR22                                        |
|           |                                                        |         | R/W                                                                                                                  |                                                                              |        |                                                        |                                                                                              |                                                                      |                                                                                                |                                              |
|           |                                                        |         | 0                                                                                                                    | 0                                                                            | 0      | 0                                                      | 0                                                                                            | 0                                                                    | 0                                                                                              | 0                                            |
|           |                                                        |         | Store Upper 8 bits of an AD conversion result compare criterion                                                      |                                                                              |        |                                                        |                                                                                              |                                                                      |                                                                                                |                                              |
| ADCM1REGL | AD Conversion Result Compare Criterion Register 1 Low  | 12B6H   | ADR21                                                                                                                | ADR20                                                                        |        |                                                        |                                                                                              |                                                                      |                                                                                                |                                              |
|           |                                                        |         | R/W                                                                                                                  |                                                                              |        |                                                        |                                                                                              |                                                                      |                                                                                                |                                              |
|           |                                                        |         | 0                                                                                                                    | 0                                                                            |        |                                                        |                                                                                              |                                                                      |                                                                                                |                                              |
|           |                                                        |         | Store Lower 2 bits of an AD conversion result compare criterion                                                      |                                                                              |        |                                                        |                                                                                              |                                                                      |                                                                                                |                                              |
| ADCM1REGH | AD Conversion Result Compare Criterion Register 1 High | 12B7H   | ADR29                                                                                                                | ADR28                                                                        | ADR27  | ADR26                                                  | ADR25                                                                                        | ADR24                                                                | ADR23                                                                                          | ADR22                                        |
|           |                                                        |         | R/W                                                                                                                  |                                                                              |        |                                                        |                                                                                              |                                                                      |                                                                                                |                                              |
|           |                                                        |         | 0                                                                                                                    | 0                                                                            | 0      | 0                                                      | 0                                                                                            | 0                                                                    | 0                                                                                              | 0                                            |
|           |                                                        |         | Store Upper 8 bits of an AD conversion result compare criterion                                                      |                                                                              |        |                                                        |                                                                                              |                                                                      |                                                                                                |                                              |
| ADMOD0    | AD mode control register 0                             | 12B8H   | EOS                                                                                                                  | BUSY                                                                         |        | I2AD                                                   | ADS                                                                                          | HTRGE                                                                | TSEL1                                                                                          | TSEL0                                        |
|           |                                                        |         | R                                                                                                                    |                                                                              |        | R/W                                                    |                                                                                              |                                                                      |                                                                                                |                                              |
|           |                                                        |         | 0                                                                                                                    | 0                                                                            |        | 0                                                      | 0                                                                                            | 0                                                                    | 0                                                                                              | 0                                            |
|           |                                                        |         | Normal AD conversion end flag<br>0: During conversion sequence or before starting<br>1: Complete conversion sequence | Normal AD conversion BUSY Flag<br>0: Stop conversion<br>1: During conversion |        | AD conversion when IDLE2 mode<br>0: Stop<br>1: Operate | Start Normal AD conversion<br>0: Don't Care<br>1: Start AD conversion<br>Always read as "0". | Normal AD conversion at Hard ware trigger<br>0: Disable<br>1: Enable | Select Hard ware trigger<br>00: INTTB00 interrupt<br>01: Reserved<br>10: ADTRG<br>11: Reserved |                                              |



## (16) AD converter (3/3)

| Symbol | Name                                 | Address | 7                                                                                                                                | 6                                                                                                                                             | 5                                                                                                   | 4                                                                                                   | 3                                                                                                       | 2                                                                                                                                                                                                                                        | 1                                                                                                                 | 0                                                                              |
|--------|--------------------------------------|---------|----------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------|
| ADMOD1 | AD mode control register 1           | 12B9H   | DACON                                                                                                                            | ADCH2                                                                                                                                         | ADCH1                                                                                               | ADCH0                                                                                               | LAT                                                                                                     | ITM                                                                                                                                                                                                                                      | REPEAT                                                                                                            | SCAN                                                                           |
|        |                                      |         | R/W                                                                                                                              |                                                                                                                                               |                                                                                                     |                                                                                                     |                                                                                                         |                                                                                                                                                                                                                                          |                                                                                                                   |                                                                                |
|        |                                      |         | 0                                                                                                                                | 0                                                                                                                                             | 0                                                                                                   | 0                                                                                                   | 0                                                                                                       | 0                                                                                                                                                                                                                                        | 0                                                                                                                 | 0                                                                              |
|        |                                      |         | DAC and VREF application control                                                                                                 | Analog input channel select                                                                                                                   |                                                                                                     |                                                                                                     | Latency<br>0: No Wait<br>1: Start after reading conversion result store Register of last channel        | Interrupt specification when conversion channel fixed repeat mode                                                                                                                                                                        | Repeat mode specification<br>0: Single conversion<br>1: Repeat conversion                                         | Scan mode specification<br>0: Channel fixed mode<br>1: Channel scan mode       |
| ADMOD2 | AD mode control register 2           | 12BAH   | HEOS                                                                                                                             | HBUSY                                                                                                                                         |                                                                                                     |                                                                                                     | HADS                                                                                                    | HHTRGE                                                                                                                                                                                                                                   | HTSEL1                                                                                                            | HTSEL0                                                                         |
|        |                                      |         | R                                                                                                                                |                                                                                                                                               |                                                                                                     |                                                                                                     | R/W                                                                                                     |                                                                                                                                                                                                                                          |                                                                                                                   |                                                                                |
|        |                                      |         | 0                                                                                                                                | 0                                                                                                                                             |                                                                                                     |                                                                                                     | 0                                                                                                       | 0                                                                                                                                                                                                                                        | 0                                                                                                                 | 0                                                                              |
|        |                                      |         | High-priority AD conversion sequence FLAG<br>0: During conversion sequence or before starting<br>1: Complete conversion sequence | High-priority AD conversion BUSY Flag<br>0: Stop conversion<br>1: During conversion                                                           |                                                                                                     |                                                                                                     | Start High-priority AD conversion<br>0: Don't Care<br>1: Start AD conversion<br><br>Always read as "0". | High-priority AD conversion at Hard ware trigger<br>0: Disable<br>1: Enable                                                                                                                                                              | Select Hard ware trigger<br>00: INTTB10 interrupt<br>01: Reserved<br>10: ADTRG<br>11: I2S Sampling Counter Output |                                                                                |
| ADMOD3 | AD mode control register 3           | 12BBH   | —                                                                                                                                | HADCH2                                                                                                                                        | HADCH1                                                                                              | HADCH0                                                                                              |                                                                                                         |                                                                                                                                                                                                                                          |                                                                                                                   | —                                                                              |
|        |                                      |         | R/W                                                                                                                              |                                                                                                                                               |                                                                                                     |                                                                                                     |                                                                                                         |                                                                                                                                                                                                                                          |                                                                                                                   | R/W                                                                            |
|        |                                      |         | 0                                                                                                                                | 0                                                                                                                                             | 0                                                                                                   | 0                                                                                                   |                                                                                                         |                                                                                                                                                                                                                                          |                                                                                                                   | 0                                                                              |
|        |                                      |         | Always write "0".                                                                                                                | High-priority analog input channel select                                                                                                     |                                                                                                     |                                                                                                     |                                                                                                         |                                                                                                                                                                                                                                          |                                                                                                                   | Always write "0".                                                              |
| ADMOD4 | AD mode control register 4           | 12BCH   | CMEN1                                                                                                                            | CMEN0                                                                                                                                         | CMP1C                                                                                               | CMP0C                                                                                               | IRQEN1                                                                                                  | IRQEN0                                                                                                                                                                                                                                   | CMPINT1                                                                                                           | CMPINT0                                                                        |
|        |                                      |         | R/W                                                                                                                              |                                                                                                                                               |                                                                                                     |                                                                                                     |                                                                                                         |                                                                                                                                                                                                                                          |                                                                                                                   |                                                                                |
|        |                                      |         | 0                                                                                                                                | 0                                                                                                                                             | 0                                                                                                   | 0                                                                                                   | 0                                                                                                       | 0                                                                                                                                                                                                                                        | 0                                                                                                                 | 0                                                                              |
|        |                                      |         | AD Monitor function1<br>0: Disable<br>1: Enable                                                                                  | AD Monitor function0<br>0: Disable<br>1: Enable                                                                                               | Generation condition of AD monitor function interrupt 1<br>0: less than<br>1: Greater than or Equal | Generation condition of AD monitor function interrupt 0<br>0: less than<br>1: Greater than or Equal | AD monitor function interrupt 1<br>0: Disable<br>1: Enable (Note)                                       | AD monitor function interrupt 0<br>0: Disable<br>1: Enable (Note)                                                                                                                                                                        | Status of AD monitor function interrupt 1<br>0: No generation<br>1: Generation                                    | Status of AD monitor function interrupt 0<br>0: No generation<br>1: Generation |
| ADMOD5 | AD mode control register 5           | 12BDH   |                                                                                                                                  | CM1CH2                                                                                                                                        | CM1CH1                                                                                              | CM1CH0                                                                                              |                                                                                                         | CM0CH2                                                                                                                                                                                                                                   | CM0CH1                                                                                                            | CM0CH0                                                                         |
|        |                                      |         |                                                                                                                                  | R/W                                                                                                                                           |                                                                                                     |                                                                                                     |                                                                                                         | R/W                                                                                                                                                                                                                                      |                                                                                                                   |                                                                                |
|        |                                      |         |                                                                                                                                  | 0                                                                                                                                             | 0                                                                                                   | 0                                                                                                   |                                                                                                         | 0                                                                                                                                                                                                                                        | 0                                                                                                                 | 0                                                                              |
|        |                                      |         |                                                                                                                                  | Select analog channel for AD monitor function 1<br>000: AN0 100: AN4<br>001: AN1 101: AN5<br>010: AN2 110: Reserved<br>011: AN3 111: Reserved |                                                                                                     |                                                                                                     |                                                                                                         | Select analog channel for AD monitor function 1<br>000: AN0 100: AN4<br>001: AN1 101: AN5<br>010: AN2 110: Reserved<br>011: AN3 111: Reserved                                                                                            |                                                                                                                   |                                                                                |
| ADCCLK | AD Conversion Clock Setting Register | 12BFH   |                                                                                                                                  |                                                                                                                                               |                                                                                                     |                                                                                                     | —                                                                                                       | ADCLK2                                                                                                                                                                                                                                   | ADCLK1                                                                                                            | ADCLK0                                                                         |
|        |                                      |         |                                                                                                                                  |                                                                                                                                               |                                                                                                     |                                                                                                     | R/W                                                                                                     |                                                                                                                                                                                                                                          |                                                                                                                   |                                                                                |
|        |                                      |         |                                                                                                                                  |                                                                                                                                               |                                                                                                     |                                                                                                     | 0                                                                                                       | 0                                                                                                                                                                                                                                        | 0                                                                                                                 | 0                                                                              |
|        |                                      |         |                                                                                                                                  |                                                                                                                                               |                                                                                                     |                                                                                                     | Always write "0"                                                                                        | Select clock for AD conversion<br>000 : Reserved 100 : f <sub>IO</sub> /4<br>001 : f <sub>IO</sub> /1 101 : f <sub>IO</sub> /5<br>010 : f <sub>IO</sub> /2 110 : f <sub>IO</sub> /6<br>011 : f <sub>IO</sub> /3 111 : f <sub>IO</sub> /7 |                                                                                                                   |                                                                                |

(17) Watchdog timer

| Symbol | Name                 | Address              | 7                        | 6                                                                                                                                                                                     | 5     | 4 | 3                  | 2                              | 1                                                  | 0                 |
|--------|----------------------|----------------------|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|---|--------------------|--------------------------------|----------------------------------------------------|-------------------|
| WDMOD  | WDT mode register    | 1300H                | WDTE                     | WDTP1                                                                                                                                                                                 | WDTP0 |   |                    | I2WDT                          | RESCR                                              | –                 |
|        |                      |                      | R/W                      |                                                                                                                                                                                       |       |   |                    | R/W                            |                                                    |                   |
|        |                      |                      | 1                        | 0                                                                                                                                                                                     | 0     |   |                    | 0                              | 0                                                  | 0                 |
|        |                      |                      | WDT control<br>1: Enable | Select detecting time<br>00: 2 <sup>15</sup> /f <sub>IO</sub><br>01: 2 <sup>17</sup> /f <sub>IO</sub><br>10: 2 <sup>19</sup> /f <sub>IO</sub><br>11: 2 <sup>21</sup> /f <sub>IO</sub> |       |   |                    | IDLE2<br>0: Stop<br>1: Operate | 1: Internally connects<br>WDT out to the reset pin | Always write “0”. |
| WDCR   | WDT control register | 1301H (Prohibit RMW) | –                        |                                                                                                                                                                                       |       |   |                    |                                |                                                    |                   |
|        |                      |                      | W                        |                                                                                                                                                                                       |       |   |                    |                                |                                                    |                   |
|        |                      |                      | –                        |                                                                                                                                                                                       |       |   |                    |                                |                                                    |                   |
|        |                      |                      | B1H: WDT disable code    |                                                                                                                                                                                       |       |   | 4E: WDT clear code |                                |                                                    |                   |

## (18) RTC (Real-Time Clock)

| Symbol | Name            | Address              | 7                                    | 6                               | 5                | 4                          | 3                                | 2                                | 1            | 0              |
|--------|-----------------|----------------------|--------------------------------------|---------------------------------|------------------|----------------------------|----------------------------------|----------------------------------|--------------|----------------|
| SECR   | Second register | 1320H                |                                      | SE6                             | SE5              | SE4                        | SE3                              | SE2                              | SE1          | SE0            |
|        |                 |                      |                                      | R/W                             |                  |                            |                                  |                                  |              |                |
|        |                 |                      |                                      | Undefined                       |                  |                            |                                  |                                  |              |                |
|        |                 |                      | "0" is read                          | 40 sec.                         | 20 sec.          | 10 sec.                    | 8 sec.                           | 4 sec.                           | 2 sec.       | 1 sec.         |
| MINR   | Minute register | 1321H                |                                      | MI6                             | MI5              | MI4                        | MI3                              | MI2                              | MI1          | MI0            |
|        |                 |                      |                                      | R/W                             |                  |                            |                                  |                                  |              |                |
|        |                 |                      |                                      | Undefined                       |                  |                            |                                  |                                  |              |                |
|        |                 |                      | "0" is read                          | 40 min.                         | 20 min.          | 10 min.                    | 8 min.                           | 4 min.                           | 2 min.       | 1 min.         |
| HOURR  | Hour register   | 1322H                |                                      |                                 | HO5              | HO4                        | HO3                              | HO2                              | HO1          | HO0            |
|        |                 |                      |                                      |                                 | R/W              |                            |                                  |                                  |              |                |
|        |                 |                      |                                      |                                 | Undefined        |                            |                                  |                                  |              |                |
|        |                 |                      | "0" is read                          |                                 | 20 hours (PM/AM) | 10 hours                   | 8 hours                          | 4 hours                          | 2 hours      | 1 hour         |
| DAYR   | Day register    | 1323H                |                                      |                                 |                  |                            |                                  | WE2                              | WE1          | WE0            |
|        |                 |                      |                                      |                                 |                  |                            |                                  | R/W                              |              |                |
|        |                 |                      |                                      |                                 |                  |                            |                                  | Undefined                        |              |                |
|        |                 |                      | "0" is read                          |                                 |                  |                            |                                  | W2                               | W1           | W0             |
| DATER  | Date register   | 1324H                |                                      |                                 | DA5              | DA4                        | DA3                              | DA2                              | DA1          | DA0            |
|        |                 |                      |                                      |                                 | R/W              |                            |                                  |                                  |              |                |
|        |                 |                      |                                      |                                 | Undefined        |                            |                                  |                                  |              |                |
|        |                 |                      | "0" is read                          |                                 | 20 days          | 10 days                    | 8 days                           | 4 days                           | 2 days       | 1 day          |
| MONTHR | Month register  | 1325H                |                                      |                                 |                  | MO4                        | MO3                              | MO2                              | MO1          | MO0            |
|        |                 |                      |                                      |                                 |                  | R/W                        |                                  |                                  |              |                |
|        |                 |                      |                                      |                                 |                  | Undefined                  |                                  |                                  |              |                |
|        |                 |                      | "0" is read                          |                                 |                  | 10 month                   | 8 month                          | 4 month                          | 2 month      | 1 month        |
| YEARR  | Year register   | 1326H                |                                      |                                 |                  |                            |                                  |                                  |              |                |
|        |                 |                      |                                      |                                 |                  |                            |                                  |                                  |              |                |
|        |                 |                      |                                      |                                 |                  |                            |                                  |                                  |              |                |
|        |                 |                      | "0" is read                          |                                 |                  |                            |                                  |                                  |              |                |
| PAGER  | Page register   | 1327H (Prohibit RMW) | INTENA                               |                                 |                  | ADJUST                     | ENATMR                           | ENAALM                           |              | PAGE           |
|        |                 |                      | R/W                                  |                                 |                  | W                          |                                  |                                  |              | R/W            |
|        |                 |                      | 0                                    |                                 |                  | Undefined                  |                                  |                                  |              | Undefined      |
|        |                 |                      | Interrupt<br>1: Enable<br>0: Disable | "0" is read                     |                  | 0: Don't care<br>1: Adjust | Clock<br>1: Enable<br>0: Disable | ALARM<br>1: Enable<br>0: Disable | "0" is read. | PAGE selection |
| RESTR  | Reset register  | 1328H (Prohibit RMW) | DIS1HZ                               | DIS16HZ                         | RSTTMR           | RSTALM                     | RE3                              | RE2                              | RE1          | RE0            |
|        |                 |                      |                                      |                                 |                  |                            |                                  |                                  |              |                |
|        |                 |                      |                                      |                                 |                  |                            |                                  |                                  |              |                |
|        |                 |                      | 1Hz<br>0: Enable<br>1: Disable       | 16Hz<br>0: Enable<br>1: Disable | 1: Clock reset   | 1: Alarm reset             | Always write "0"                 |                                  |              |                |

## (19) Melody/alarm generator

| Symbol  | Name                            | Address | 7                                                                                                | 6   | 5                                   | 4                            | 3                                   | 2                             | 1                              | 0                                         |
|---------|---------------------------------|---------|--------------------------------------------------------------------------------------------------|-----|-------------------------------------|------------------------------|-------------------------------------|-------------------------------|--------------------------------|-------------------------------------------|
| ALM     | Alarm-pattern register          | 1330H   | AL8                                                                                              | AL7 | AL6                                 | AL5                          | AL4                                 | AL3                           | AL2                            | AL1                                       |
|         |                                 |         | R/W                                                                                              |     |                                     |                              |                                     |                               |                                |                                           |
|         |                                 |         | 0                                                                                                | 0   | 0                                   | 0                            | 0                                   | 0                             | 0                              | 0                                         |
|         |                                 |         | Alarm pattern setting                                                                            |     |                                     |                              |                                     |                               |                                |                                           |
| MELALMC | Melody/alarm control register   | 1331H   | FC1                                                                                              | FC0 | ALMINV                              | –                            | –                                   | –                             | –                              | MELALM                                    |
|         |                                 |         | R/W                                                                                              |     |                                     |                              |                                     |                               |                                |                                           |
|         |                                 |         | 0                                                                                                | 0   | 0                                   | 0                            | 0                                   | 0                             | 0                              | 0                                         |
|         |                                 |         | Free run counter control<br>00: Hold<br>01: Restart<br>10: Clear and stop<br>11: Clear and start |     | Alarm frequency invert<br>1: Invert | Always write "0".            |                                     |                               |                                | Output frequency<br>0: Alarm<br>1: Melody |
| MELFL   | Melody frequency L-register     | 1332H   | ML7                                                                                              | ML6 | ML5                                 | ML4                          | ML3                                 | ML2                           | ML1                            | ML0                                       |
|         |                                 |         | R/W                                                                                              |     |                                     |                              |                                     |                               |                                |                                           |
|         |                                 |         | 0                                                                                                | 0   | 0                                   | 0                            | 0                                   | 0                             | 0                              | 0                                         |
|         |                                 |         | Melody frequency set (Low 8bit)                                                                  |     |                                     |                              |                                     |                               |                                |                                           |
| MELFH   | Melody frequency H-register     | 1333H   | MELON                                                                                            |     |                                     |                              | ML11                                | ML10                          | ML9                            | ML8                                       |
|         |                                 |         | R/W                                                                                              |     |                                     |                              | R/W                                 |                               |                                |                                           |
|         |                                 |         | 0                                                                                                |     |                                     |                              | 0                                   | 0                             | 0                              | 0                                         |
|         |                                 |         | Melody counter control<br>0: Stop and clear<br>1: Start                                          |     |                                     |                              | Melody frequency set (Upper 4 bits) |                               |                                |                                           |
| ALMINT  | Alarm interrupt enable register | 1334H   |                                                                                                  |     | –                                   | IALM4E                       | IALM3E                              | IALM2E                        | IALM1E                         | IALM0E                                    |
|         |                                 |         |                                                                                                  |     | R/W                                 |                              |                                     |                               |                                |                                           |
|         |                                 |         |                                                                                                  |     | 0                                   | 0                            | 0                                   | 0                             | 0                              | 0                                         |
|         |                                 |         |                                                                                                  |     | Always write "0".                   | 1:INTALM4<br>(1Hz)<br>enable | 1:INTALM3<br>(2Hz)<br>enable        | 1:INTALM2<br>(64Hz)<br>enable | 1:INTALM1<br>(512Hz)<br>enable | 1:INTALM0<br>(8192Hz)<br>enable           |

(20) I<sup>2</sup>S

| Symbol                                      | Name                                                         | Address                                     | 15                                                            | 14   | 13                                         | 12   | 11   | 10   | 9                                                | 8    | 7                                                                  | 6    | 5                                                                             | 4    | 3                                                              | 2    | 1                                                                   | 0    |
|---------------------------------------------|--------------------------------------------------------------|---------------------------------------------|---------------------------------------------------------------|------|--------------------------------------------|------|------|------|--------------------------------------------------|------|--------------------------------------------------------------------|------|-------------------------------------------------------------------------------|------|----------------------------------------------------------------|------|---------------------------------------------------------------------|------|
| I2S0BUF                                     | I <sup>2</sup> S<br>Transmi-<br>ssion<br>Buffer<br>Register0 | 1800H<br>(Prohibit<br>RMW)                  | B015                                                          | B014 | B013                                       | B012 | B011 | B010 | B009                                             | B008 | B007                                                               | B006 | B005                                                                          | B004 | B003                                                           | B002 | B001                                                                | B000 |
|                                             |                                                              |                                             | W                                                             |      |                                            |      |      |      |                                                  |      |                                                                    |      |                                                                               |      |                                                                |      |                                                                     |      |
|                                             |                                                              |                                             | Undefined                                                     |      |                                            |      |      |      |                                                  |      |                                                                    |      |                                                                               |      |                                                                |      |                                                                     |      |
|                                             |                                                              |                                             | Transmission buffer register (FIFO)                           |      |                                            |      |      |      |                                                  |      |                                                                    |      |                                                                               |      |                                                                |      |                                                                     |      |
|                                             |                                                              |                                             | 31                                                            | 30   | 29                                         | 28   | 27   | 26   | 25                                               | 24   | 23                                                                 | 22   | 21                                                                            | 20   | 19                                                             | 18   | 17                                                                  | 16   |
|                                             |                                                              |                                             | B031                                                          | B030 | B09                                        | B028 | B027 | B026 | B025                                             | B024 | B023                                                               | B022 | B021                                                                          | B020 | B019                                                           | B018 | B017                                                                | B016 |
|                                             |                                                              |                                             | W                                                             |      |                                            |      |      |      |                                                  |      |                                                                    |      |                                                                               |      |                                                                |      |                                                                     |      |
|                                             |                                                              |                                             | Undefined                                                     |      |                                            |      |      |      |                                                  |      |                                                                    |      |                                                                               |      |                                                                |      |                                                                     |      |
|                                             |                                                              |                                             | Transmission buffer register (FIFO)                           |      |                                            |      |      |      |                                                  |      |                                                                    |      |                                                                               |      |                                                                |      |                                                                     |      |
| I2S0CTL                                     | I <sup>2</sup> S<br>Control<br>Register0                     | 1808H                                       | TXE0                                                          |      | *CNTE0                                     |      |      |      | DIR0                                             |      | BIT0                                                               |      | DTFMT01                                                                       |      | DTFMT00                                                        |      | SYSCKE0                                                             |      |
|                                             |                                                              |                                             | R/W                                                           |      |                                            |      |      |      | R/W                                              |      |                                                                    |      |                                                                               |      |                                                                |      |                                                                     |      |
|                                             |                                                              |                                             | 0                                                             |      | 0                                          |      |      |      | 0                                                |      | 0                                                                  |      | 0                                                                             |      | 0                                                              |      |                                                                     |      |
|                                             |                                                              |                                             | Transmit<br>0: Stop<br>1: Start                               |      | Counter<br>control<br>0: Clear<br>1: Start |      |      |      | Transmi-<br>ssion start<br>BIT<br>0:MSB<br>1:LSB |      | Bit length<br>0: 8 bits<br>1:16 bits                               |      | Output format<br>00: I <sup>2</sup> S    10: Right<br>01: Left    11:Reserved |      | System<br>clock<br>0:Disable<br>1:Enable                       |      |                                                                     |      |
|                                             |                                                              | 1809H                                       | CLKS0                                                         |      |                                            |      |      |      | FSEL0                                            |      | TEMPO                                                              |      | WLVLO                                                                         |      | EDGE0                                                          |      | CLKE0                                                               |      |
|                                             |                                                              |                                             | R/W                                                           |      |                                            |      |      |      | R/W                                              |      | R                                                                  |      | R/W                                                                           |      |                                                                |      |                                                                     |      |
|                                             |                                                              |                                             | 0                                                             |      |                                            |      |      |      |                                                  |      | 0                                                                  |      | 1                                                                             |      | 0                                                              |      | 0                                                                   |      |
|                                             |                                                              |                                             | Source<br>clock<br>0: f <sub>SYS</sub><br>1: f <sub>PLL</sub> |      |                                            |      |      |      | Stereo<br>/monaural<br>0: Stereo<br>1: Monaural  |      | Condition of<br>transmission<br>FIFO<br>0: data<br>1: None<br>data |      | WS level<br>0:low left<br>1:high left                                         |      | Clock<br>edge for<br>data<br>output<br>0: Falling<br>1: Rising |      | Clock<br>enable<br>(After trans-<br>mission)<br>0:Operate<br>1:Stop |      |
|                                             |                                                              |                                             |                                                               |      |                                            |      |      |      |                                                  |      |                                                                    |      |                                                                               |      |                                                                |      |                                                                     |      |
| I2S0C                                       | I <sup>2</sup> S0<br>Divider<br>Value<br>Setting<br>Register | 180AH                                       | CK07                                                          |      | CK06                                       |      | CK05 |      | CK04                                             |      | CK03                                                               |      | CK02                                                                          |      | CK01                                                           |      | CK00                                                                |      |
|                                             |                                                              |                                             | R/W                                                           |      |                                            |      |      |      |                                                  |      |                                                                    |      |                                                                               |      |                                                                |      |                                                                     |      |
|                                             |                                                              |                                             | 0                                                             |      | 0                                          |      | 0    |      | 0                                                |      | 0                                                                  |      | 0                                                                             |      | 0                                                              |      | 0                                                                   |      |
|                                             |                                                              | Divider value for CK signal (8-bit counter) |                                                               |      |                                            |      |      |      |                                                  |      |                                                                    |      |                                                                               |      |                                                                |      |                                                                     |      |
|                                             |                                                              | 180BH                                       |                                                               |      |                                            |      | WS05 |      | WS04                                             |      | WS03                                                               |      | WS02                                                                          |      | WS01                                                           |      | WS00                                                                |      |
|                                             |                                                              |                                             |                                                               |      |                                            |      | R/W  |      |                                                  |      |                                                                    |      |                                                                               |      |                                                                |      |                                                                     |      |
| 0                                           |                                                              |                                             |                                                               |      |                                            |      | 0    |      | 0                                                |      | 0                                                                  |      | 0                                                                             |      | 0                                                              |      |                                                                     |      |
| Divider value for WS signal (6-bit counter) |                                                              |                                             |                                                               |      |                                            |      |      |      |                                                  |      |                                                                    |      |                                                                               |      |                                                                |      |                                                                     |      |

## (21) MAC (1/2)

| Symbol    | Name                                       | Address | 7                                             | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|-----------|--------------------------------------------|---------|-----------------------------------------------|------|------|------|------|------|------|------|
| MACMA_LL  | Data register Multiplier A-LL              | 1BE0H   | MA7                                           | MA6  | MA5  | MA4  | MA3  | MA2  | MA1  | MA0  |
|           |                                            |         | R/W                                           |      |      |      |      |      |      |      |
|           |                                            |         | Undefined                                     |      |      |      |      |      |      |      |
|           |                                            |         | Multiplier A data register [7:0]              |      |      |      |      |      |      |      |
| MACMA_LH  | Data register Multiplier A-LH              | 1BE1H   | MA15                                          | MA14 | MA13 | MA12 | MA11 | MA10 | MA9  | MA8  |
|           |                                            |         | R/W                                           |      |      |      |      |      |      |      |
|           |                                            |         | Undefined                                     |      |      |      |      |      |      |      |
|           |                                            |         | Multiplier A data register [15:8]             |      |      |      |      |      |      |      |
| MACMA_HL  | Data register Multiplier A-HL              | 1BE2H   | MA23                                          | MA22 | MA21 | MA20 | MA19 | MA18 | MA17 | MA16 |
|           |                                            |         | R/W                                           |      |      |      |      |      |      |      |
|           |                                            |         | Undefined                                     |      |      |      |      |      |      |      |
|           |                                            |         | Multiplier A data register [23:16]            |      |      |      |      |      |      |      |
| MACMA_HH  | Data register Multiplier A-HH              | 1BE3H   | MA31                                          | MA30 | MA29 | MA28 | MA27 | MA26 | MA25 | MA24 |
|           |                                            |         | R/W                                           |      |      |      |      |      |      |      |
|           |                                            |         | Undefined                                     |      |      |      |      |      |      |      |
|           |                                            |         | Multiplier A data register [31:24]            |      |      |      |      |      |      |      |
| MACMB_LL  | Data register Multiplier B-LL              | 1BE4H   | MB7                                           | MB6  | MB5  | MB4  | MB3  | MB2  | MB1  | MB0  |
|           |                                            |         | R/W                                           |      |      |      |      |      |      |      |
|           |                                            |         | Undefined                                     |      |      |      |      |      |      |      |
|           |                                            |         | Multiplier B data register [7:0]              |      |      |      |      |      |      |      |
| MACMB_LH  | Data register Multiplier B-LH              | 1BE5H   | MB15                                          | MB14 | MB13 | MB12 | MB11 | MB10 | MB9  | MB8  |
|           |                                            |         | R/W                                           |      |      |      |      |      |      |      |
|           |                                            |         | Undefined                                     |      |      |      |      |      |      |      |
|           |                                            |         | Multiplier B data register [15:8]             |      |      |      |      |      |      |      |
| MACMB_HL  | Data register Multiplier B-HL              | 1BE6H   | MB23                                          | MB22 | MB21 | MB20 | MB19 | MB18 | MB17 | MB16 |
|           |                                            |         | R/W                                           |      |      |      |      |      |      |      |
|           |                                            |         | Undefined                                     |      |      |      |      |      |      |      |
|           |                                            |         | Multiplier B data register [23:16]            |      |      |      |      |      |      |      |
| MACMB_HH  | Data register Multiplier B-HH              | 1BE7H   | MB31                                          | MB30 | MB29 | MB28 | MB27 | MB26 | MB25 | MB24 |
|           |                                            |         | R/W                                           |      |      |      |      |      |      |      |
|           |                                            |         | Undefined                                     |      |      |      |      |      |      |      |
|           |                                            |         | Multiplier B data register [31:24]            |      |      |      |      |      |      |      |
| MACOR_LLL | Data register Multiply and Accumulate -LLL | 1BE8H   | OR7                                           | OR6  | OR5  | OR4  | OR3  | OR2  | OR1  | OR0  |
|           |                                            |         | R/W                                           |      |      |      |      |      |      |      |
|           |                                            |         | Undefined                                     |      |      |      |      |      |      |      |
|           |                                            |         | Multiply and Accumulate data register [7:0]   |      |      |      |      |      |      |      |
| MACOR_LLH | Data register Multiply and Accumulate -LLH | 1BE9H   | OR15                                          | OR14 | OR13 | OR12 | OR11 | OR10 | OR9  | OR8  |
|           |                                            |         | R/W                                           |      |      |      |      |      |      |      |
|           |                                            |         | Undefined                                     |      |      |      |      |      |      |      |
|           |                                            |         | Multiply and Accumulate data register [15:8]  |      |      |      |      |      |      |      |
| MACOR_LHL | Data register Multiply and Accumulate -LGL | 1BEAH   | OR23                                          | OR22 | OR21 | OR20 | OR19 | OR18 | OR17 | OR16 |
|           |                                            |         | R/W                                           |      |      |      |      |      |      |      |
|           |                                            |         | Undefined                                     |      |      |      |      |      |      |      |
|           |                                            |         | Multiply and Accumulate data register [23:16] |      |      |      |      |      |      |      |
| MACOR_LHH | Data register Multiply and Accumulate -LHH | 1BEBH   | OR31                                          | OR30 | OR29 | OR28 | OR27 | OR26 | OR25 | OR24 |
|           |                                            |         | R/W                                           |      |      |      |      |      |      |      |
|           |                                            |         | Undefined                                     |      |      |      |      |      |      |      |
|           |                                            |         | Multiply and Accumulate data register [31:24] |      |      |      |      |      |      |      |

## (21) MAC (2/2)

| Symbol    | Name                                                | Address | 7                                                                 | 6                                                                          | 5                                                                                                                                                                                        | 4      | 3      | 2                                      | 1                                                                                               | 0      |
|-----------|-----------------------------------------------------|---------|-------------------------------------------------------------------|----------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|----------------------------------------|-------------------------------------------------------------------------------------------------|--------|
| MACOR_HLL | Data register<br>Multiply and<br>Accumulate<br>-HLL | 1BECH   | OR39                                                              | OR38                                                                       | OR37                                                                                                                                                                                     | OR36   | OR35   | OR34                                   | OR33                                                                                            | OR32   |
|           |                                                     |         | R/W                                                               |                                                                            |                                                                                                                                                                                          |        |        |                                        |                                                                                                 |        |
|           |                                                     |         | Undefined                                                         |                                                                            |                                                                                                                                                                                          |        |        |                                        |                                                                                                 |        |
|           |                                                     |         | Multiply and Accumulate data register [39:32]                     |                                                                            |                                                                                                                                                                                          |        |        |                                        |                                                                                                 |        |
| MACOR_HLH | Data register<br>Multiply and<br>Accumulate<br>-HLH | 1BEDH   | OR47                                                              | OR46                                                                       | OR45                                                                                                                                                                                     | OR44   | OR43   | OR42                                   | OR41                                                                                            | OR40   |
|           |                                                     |         | R/W                                                               |                                                                            |                                                                                                                                                                                          |        |        |                                        |                                                                                                 |        |
|           |                                                     |         | Undefined                                                         |                                                                            |                                                                                                                                                                                          |        |        |                                        |                                                                                                 |        |
|           |                                                     |         | Multiply and Accumulate data register [47:40]                     |                                                                            |                                                                                                                                                                                          |        |        |                                        |                                                                                                 |        |
| MACOR_HHL | Data register<br>Multiply and<br>Accumulate<br>-HHL | 1BEEH   | OR55                                                              | OR54                                                                       | OR53                                                                                                                                                                                     | OR52   | OR51   | OR50                                   | OR49                                                                                            | OR48   |
|           |                                                     |         | R/W                                                               |                                                                            |                                                                                                                                                                                          |        |        |                                        |                                                                                                 |        |
|           |                                                     |         | Undefined                                                         |                                                                            |                                                                                                                                                                                          |        |        |                                        |                                                                                                 |        |
|           |                                                     |         | Multiply and Accumulate data register [55:48]                     |                                                                            |                                                                                                                                                                                          |        |        |                                        |                                                                                                 |        |
| MACOR_HHH | Data register<br>Multiply and<br>Accumulate<br>-HHH | 1BEFH   | OR63                                                              | OR62                                                                       | OR61                                                                                                                                                                                     | OR60   | OR59   | OR58                                   | OR57                                                                                            | OR56   |
|           |                                                     |         | R/W                                                               |                                                                            |                                                                                                                                                                                          |        |        |                                        |                                                                                                 |        |
|           |                                                     |         | Undefined                                                         |                                                                            |                                                                                                                                                                                          |        |        |                                        |                                                                                                 |        |
|           |                                                     |         | Multiply and Accumulate data register [63:56]                     |                                                                            |                                                                                                                                                                                          |        |        |                                        |                                                                                                 |        |
| MACCR     | MAC<br>Control<br>Register                          | 1BFCH   | MOVF                                                              | MOPST                                                                      | MSTTG2                                                                                                                                                                                   | MSTTG1 | MSTTG0 | MSGMD                                  | MOPMD1                                                                                          | MOPMD0 |
|           |                                                     |         | R/W                                                               | W                                                                          | R/W                                                                                                                                                                                      |        |        | R/W                                    | R/W                                                                                             |        |
|           |                                                     |         | 0                                                                 | 0                                                                          | 0                                                                                                                                                                                        | 0      | 0      | 0                                      | 0                                                                                               | 0      |
|           |                                                     |         | Over flow<br>flag<br>0:no<br>over flow<br>1:generate<br>over flow | Start<br>calculation<br>control<br>0:don't care<br>1: Start<br>calculation | Select the trigger of start calculation<br>000: Write to MACMA[7:0]<br>001: Write to MACMB[7:0]<br>010: Write to MACMOR[7:0]<br>011: Write to MACMOR[39:32]<br>1xx: Write "1" to <MOPST> |        |        | Sign<br>mode<br>0:Unsigned<br>1:Signed | Calculation<br>Mode<br>00: 64 + 32 × 32<br>01: 64 – 32 × 32<br>10: 32 × 32 – 64<br>11: Reserved |        |
|           |                                                     |         |                                                                   |                                                                            |                                                                                                                                                                                          |        |        |                                        |                                                                                                 |        |

## 6. Notes and Restrictions

### 6.1 Notation

- (1) The notation for built-in I/O registers is as follows: Register symbol <Bit symbol>

Example: TA01RUN<TA0RUN> denotes bit TA0RUN of register TA01RUN.

- (2) Read-modify-write instructions (RMW)

An instruction in which the CPU reads data from memory and writes the data to the same memory location in one instruction.

Example 1: SET 3, (TA01RUN); Set bit3 of TA01RUN.

Example 2: INC 1, (100H); Increment the data at 100H.

- Examples of read-modify-write instructions on the TLCS-900:

Exchange instruction

EX (mem), R

Arithmetic operations

ADD (mem), R/#      ADC (mem), R/#

SUB (mem), R/#      SBC (mem), R/#

INC #3, (mem)      DEC #3, (mem)

Logic operations

AND (mem), R/#      OR (mem), R/#

XOR (mem), R/#

Bit manipulation operations

STCF#3/A, (mem)      RES #3, (mem)

SET #3, (mem)      CHG #3, (mem)

TSET#3, (mem)

Rotate and shift operations

RLC (mem)      RRC (mem)

RL (mem)      RR (mem)

SLA (mem)      SRA (mem)

SLL (mem)      SRL (mem)

RLD (mem)      RRD (mem)

- (3) fOSCH, fc, fSYS, fIO and one state

The clock frequency input on pins X1 and 2 is referred to as fOSCH. The clock selected by PLLCR0<FCSEL> is referred to as fc.

The clock selected by SYSCR1<GEAR2:0> is referred to as system clock fSYS. The clock frequency given by fSYS divided by 2 is referred to as fIO.

One cycle of fSYS is referred to as one state.



## 6.2 Notes

### (1) AM0 and AM1 pins

These pins are connected to the VCC (Power supply level) or the VSS (Ground level) pin. Do not alter the level when the pin is active.

### (2) Reserved address areas

The 144Kbyte area (022000H~045FFFH) and 16 bytes area (FFFFFF0H ~ FFFFFFFH) cannot be used since it is reserved for use as internal area. If using an emulator, an optional 64 Kbytes of the 16M bytes area is used for emulator control. Therefore, if using an emulator, this area cannot be used.

### (3) Standby mode (IDLE1)

When the HALT instruction is executed in IDLE1 mode (in which only the oscillator operates), RTC (Real-time-clock) and MLD (Melody-alarm-generator) operate. When necessary, stop the circuit before the HALT instruction is executed.

### (4) Warm-up timer

The warm-up timer operates when STOP mode is released, even if the system is using an external oscillator. As a result, a time equivalent to the warm-up time elapses between input of the release request and output of the system clock.

### (5) Watchdog timer

The watchdog timer starts operation immediately after a reset is released. Disable the watchdog timer when it is not to be used.

### (6) AD converter

The string resistor between the VREFH and VREFL pins can be cut by program so as to reduce power consumption. When STOP mode is used, disable the resistor using the program before the HALT instruction is executed.

### (7) CPU (Micro DMA)

Only the "LDC cr, r" and "LDC r, cr" instructions can be used to access the control registers in the CPU (e.g., the transfer source address register (DMASn)).

### (8) Undefined SFR

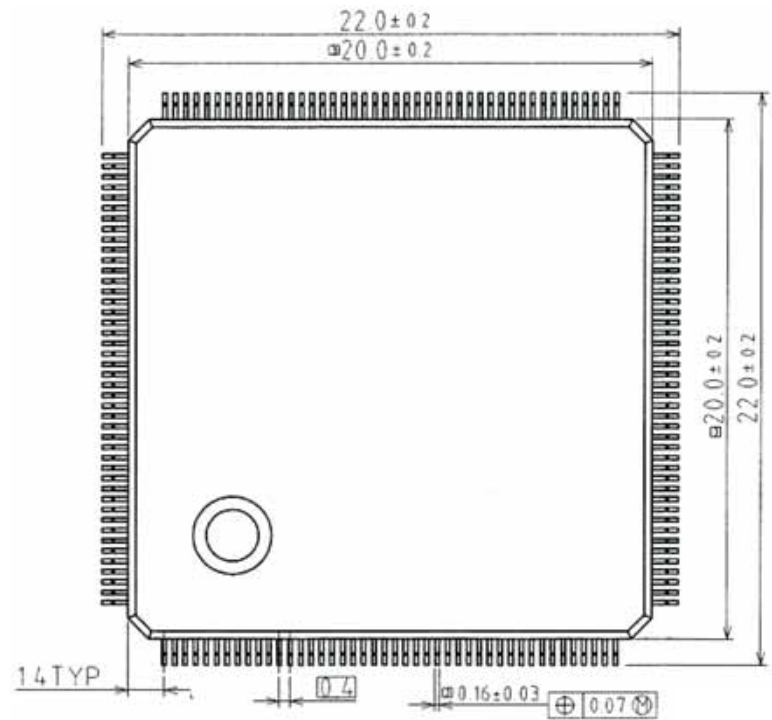
The value of an undefined bit in an SFR is undefined when read.

### (9) POP SR instruction

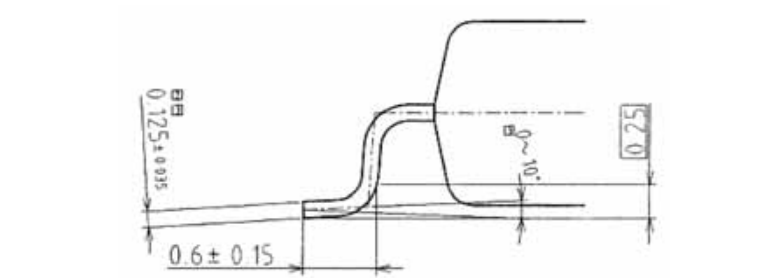
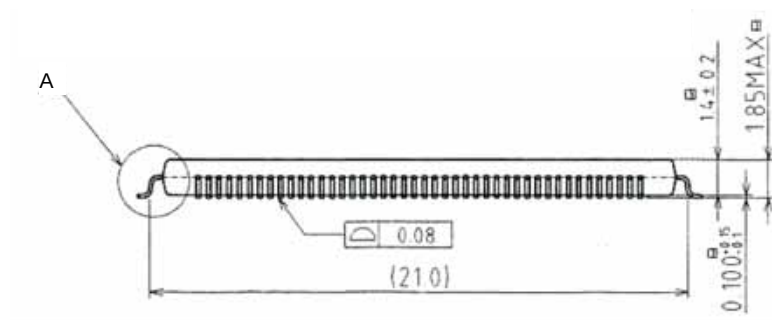
Please execute the POP SR instruction during DI condition.

7. Package Dimensions

LQFP176-P-2020-0.40F



TOP VIEW



Detail view of A (25/1)

BOTTOM VIEW

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