PSMN1R5-30BLE

N-channel 30 V 1.5 mΩ logic level MOSFET in D2PAK

12 October 2012 Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Enhanced forward biased safe operating area for superior linear mode operation
- Very low Rdson for low conduction losses

1.3 Applications

- Electronic fuse
- Hot swap
- Load switch
- Soft start

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	30	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; Fig. 1	[1]	-	-	120	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 2		-	-	401	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 12		-	1.3	1.5	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; Fig. 12		-	1.7	1.85	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	V_{GS} = 4.5 V; I_D = 25 A; V_{DS} = 15 V; Fig. 14; Fig. 15		-	33.2	-	nC
$Q_{G(tot)}$	total gate charge	V_{GS} = 10 V; I_D = 25 A; V_{DS} = 15 V; Fig. 14; Fig. 15		-	228	-	nC

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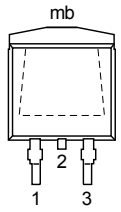
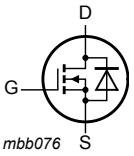
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 120 A; V_{sup} ≤ 30 V; unclamped; R_{GS} = 50 Ω; Fig. 3		-	-	1990	mJ

[1] Capped at 120A due to package

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 D2PAK (SOT404)	
2	D	drain[1]		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R5-30BLE	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R5-30BLE	PSMN1R5-30BLE

5. Limiting values

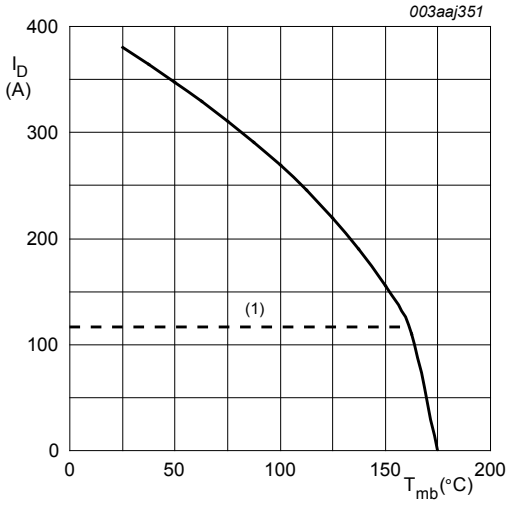
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T_j ≥ 25 °C; T_j ≤ 175 °C		-	30	V
V_{DGR}	drain-gate voltage	T_j ≤ 175 °C; T_j ≥ 25 °C; R_{GS} = 20 kΩ		-	30	V

Symbol	Parameter	Conditions		Min	Max	Unit
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 1	[1]	-	120	A
		V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 1	[1]	-	120	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10$ µs; T_{mb} = 25 °C; Fig. 4		-	1521	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 2		-	401	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[1]	-	120	A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; T_{mb} = 25 °C		-	1521	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 120 A; $V_{sup} \leq 30$ V; unclamped; R_{GS} = 50 Ω; Fig. 3		-	1990	mJ

[1] Capped at 120A due to package



(1) Capped at 120A due to package

Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

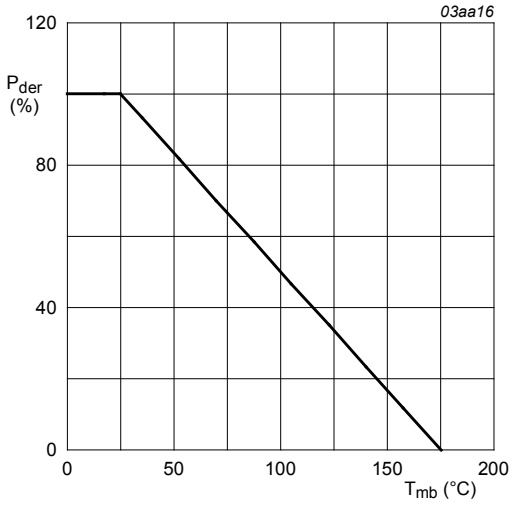


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

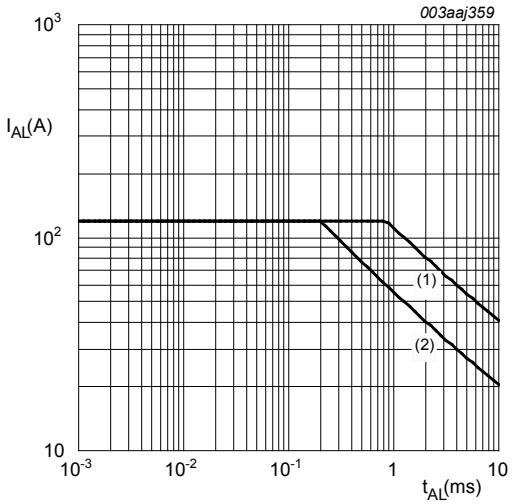


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j\ (init)} = 25°C$; (2) $T_{j\ (init)} = 100°C$

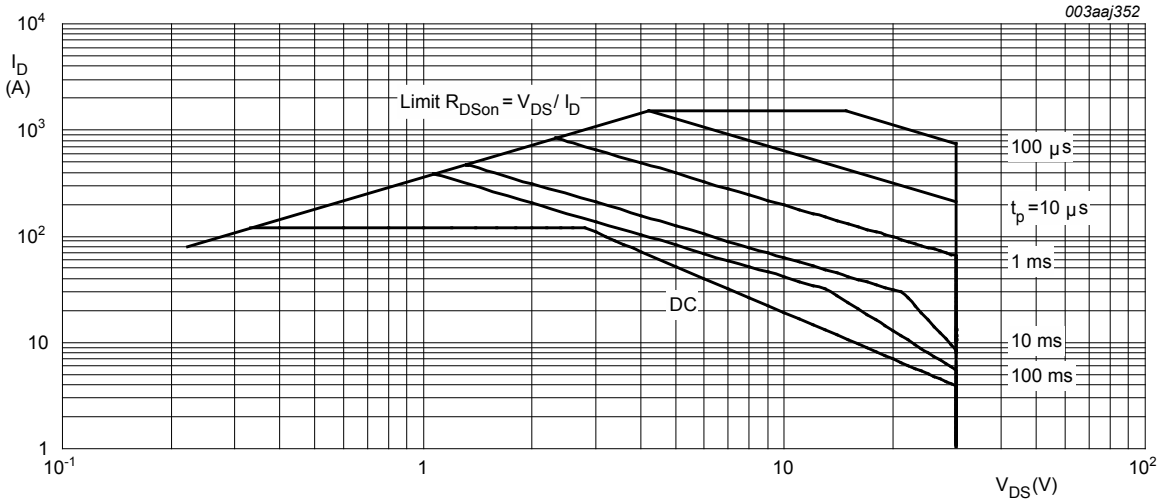


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25°C$; I_{DM} *is a single pulse*

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.3	0.37	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	minimum footprint; FR4 board		-	50	-	K/W

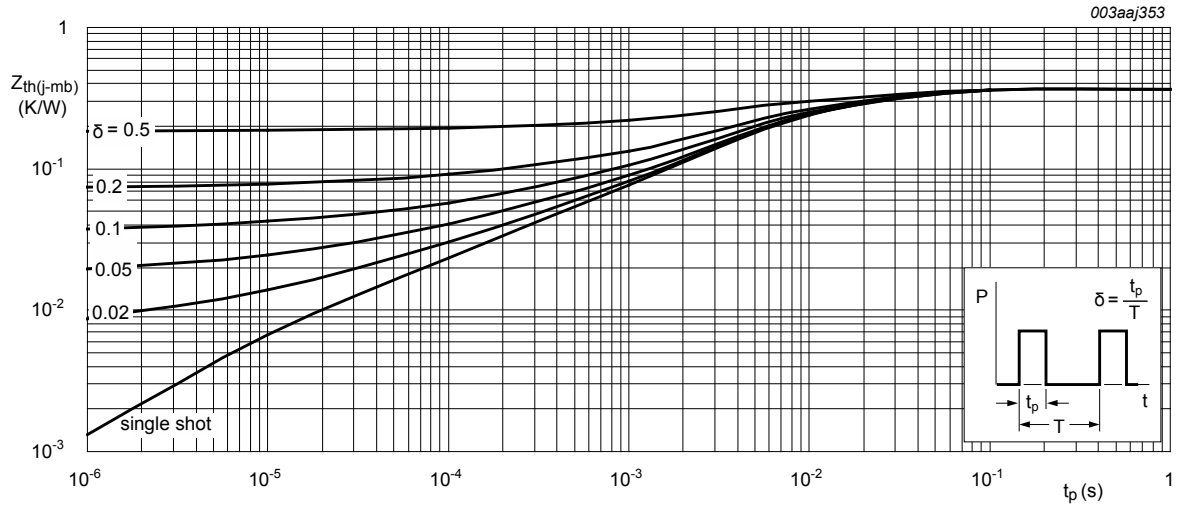


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		27	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; Fig. 10		0.5	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 11; Fig. 10		1.3	1.7	2.15	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; Fig. 10		-	-	2.45	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C		-	0.5	10	µA
		V_{DS} = 30 V; V_{GS} = 0 V; T_j = 100 °C		-	-	200	µA
I_{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 12		-	1.3	1.5	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C; Fig. 12; Fig. 13		-	-	2.1	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; Fig. 12		-	1.7	1.85	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 12; Fig. 13		-	-	2.9	mΩ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_G	internal gate resistance (AC)	f = 1 MHz		0.5	1.1	2.2	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 15 V; V_{GS} = 10 V; Fig. 14; Fig. 15		-	228	-	nC
		I_D = 25 A; V_{DS} = 15 V; V_{GS} = 4.5 V; Fig. 14; Fig. 15		-	108	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	210	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 15 V; V_{GS} = 4.5 V; Fig. 14; Fig. 15		-	31.8	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	21.5	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	10.3	-	nC
Q_{GD}	gate-drain charge			-	33.2	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 15 V; Fig. 14; Fig. 15		-	2.5	-	V
C_{iss}	input capacitance	V_{DS} = 15 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 16		-	14934	-	pF
C_{oss}	output capacitance			-	2741	-	pF
C_{rss}	reverse transfer capacitance			-	1168	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 0.6 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 4.7 Ω; T_j = 25 °C		-	100.6	-	ns
t_r	rise time			-	156.1	-	ns
$t_{d(off)}$	turn-off delay time			-	191.8	-	ns
t_f	fall time			-	99.2	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 17		-	0.78	1.2	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = 100 A/µs; V_{GS} = 0 V; V_{DS} = 15 V		-	62.5	-	ns
Q_r	recovered charge			-	96.8	-	nC

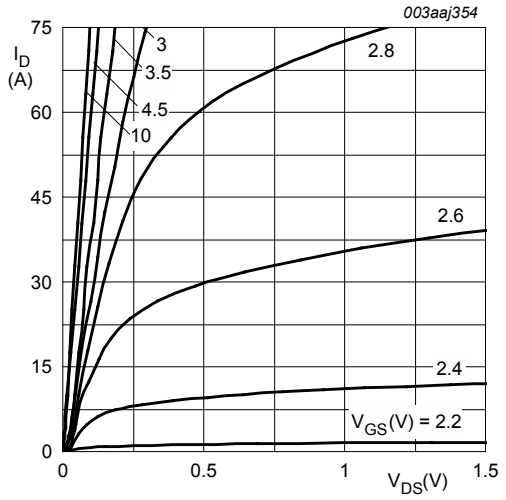


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25°C$

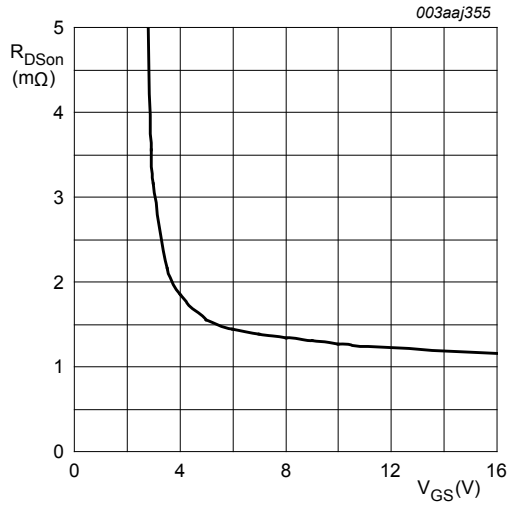


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25°C;\ I_D = 25A$

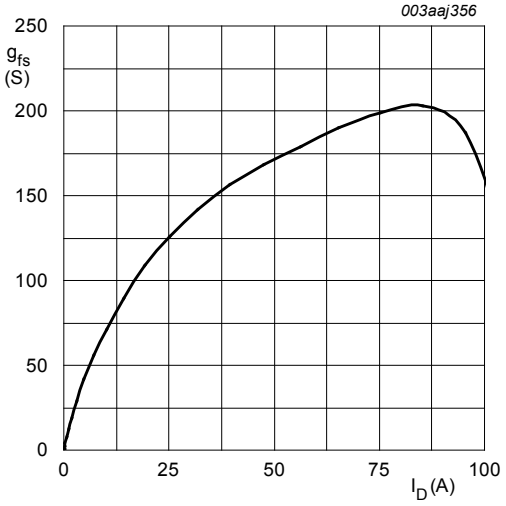


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25°C;\ V_{DS} = 10V$

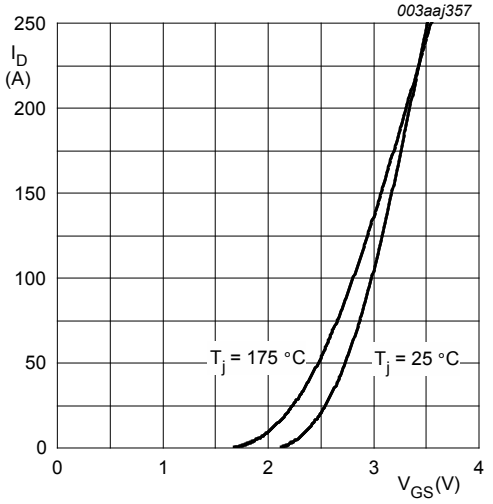


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

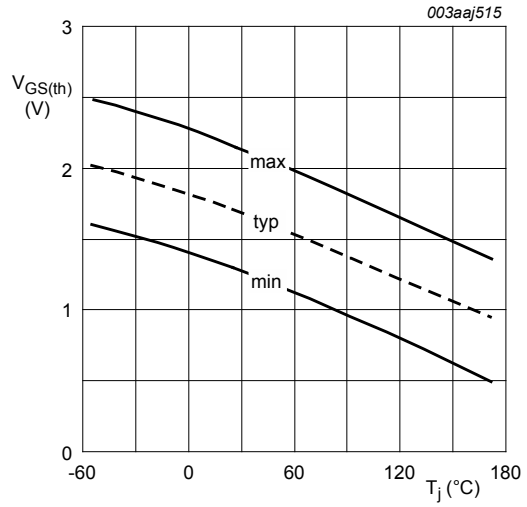


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$V_{DS} = V_{GS}$

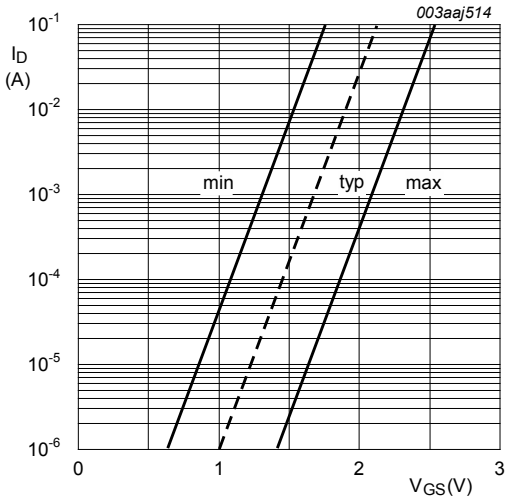


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25°C;\ V_{DS} = 5V$

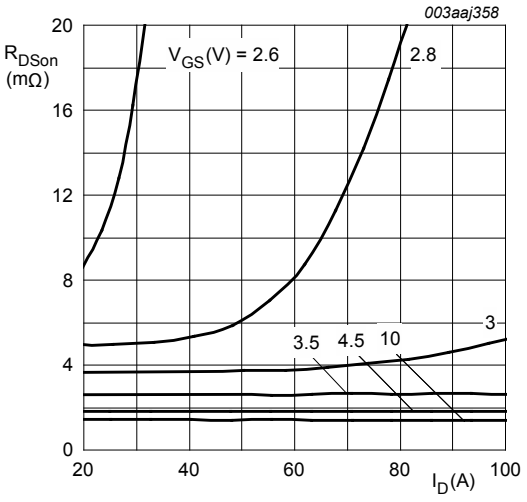


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25°C$

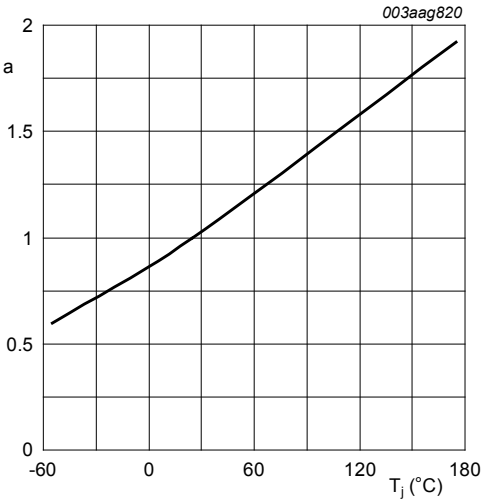


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25\,°C)}}$$

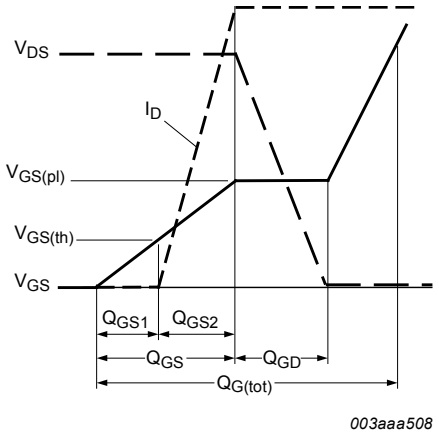


Fig. 14. Gate charge waveform definitions

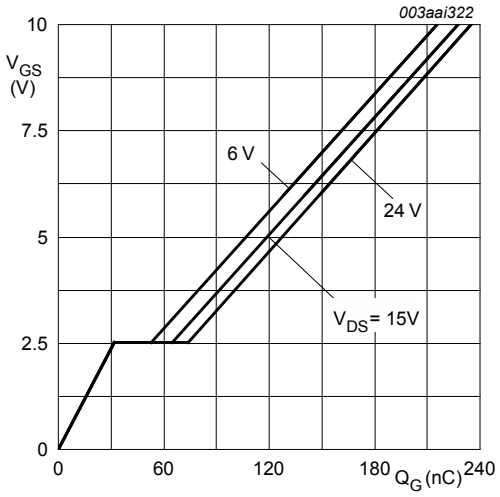


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25°C;\ I_D = 25A$

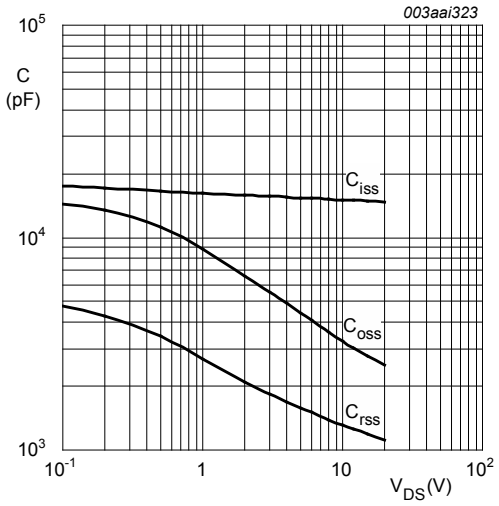


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V;\ f = 1MHz$

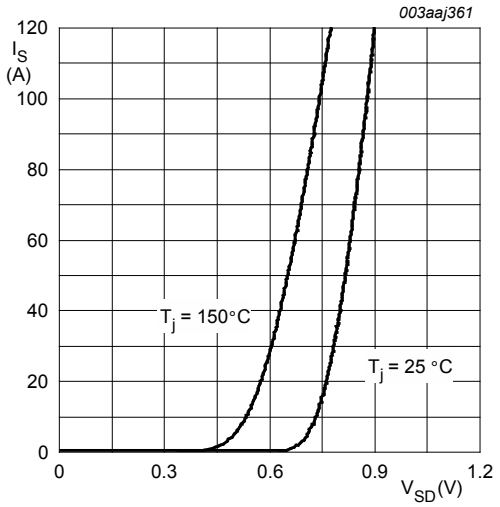
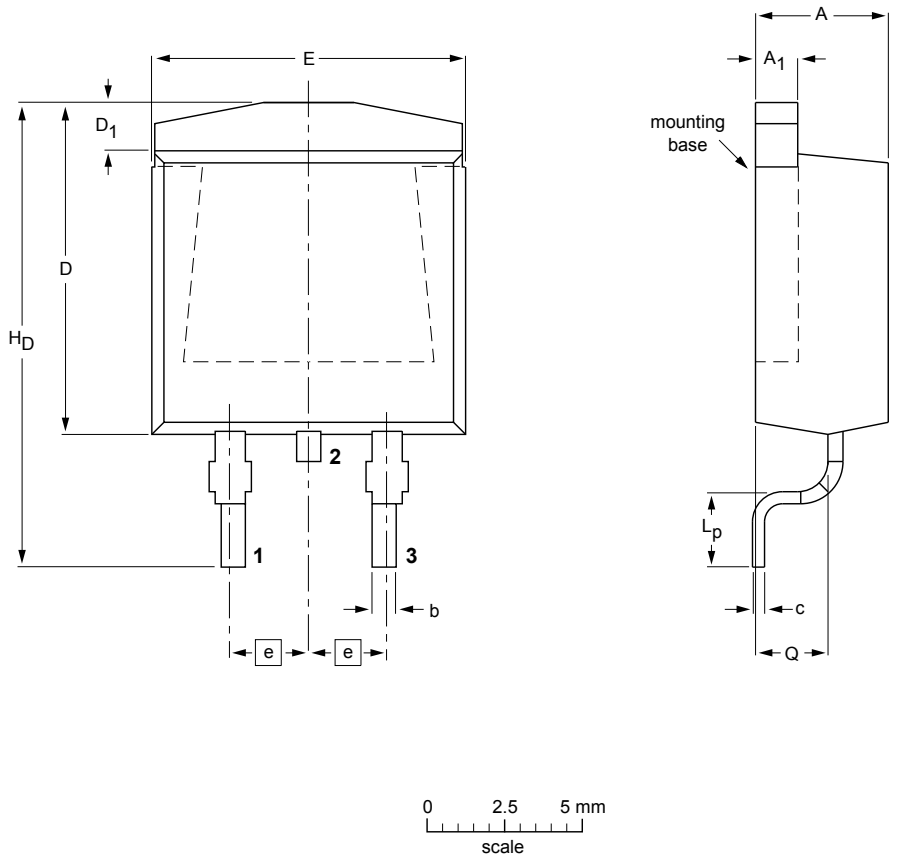


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0V$

8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) **SOT404**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						~~05-02-11~~ 06-03-16

Fig. 18. Package outline D2PAK (SOT404)

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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10. Contents

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Date of release: 12 October 2012