



Features

- Under Voltage Lock-Out Protection (UVLO) with Hysteresis
- Desaturation Detection
- Miller Clamping
- Open Collector Isolated fault feedback
- "Soft" IGBT Turn-off
- Fault Reset by next LED turn-on (low to high) after fault mute period
- Available in 16-pin SOIC package

Applications

- Isolated IGBT/Power MOSFET gate drive

Approvals

- UL 1577 Certified Component
- CSA Certified Component: Certificate 70173160

Description

The IX332B is an advanced 2.5A output current, optically isolated, IGBT gate driver that integrates V_{CE} desaturation detection, UVLO fault status feedback, and active Miller clamping.

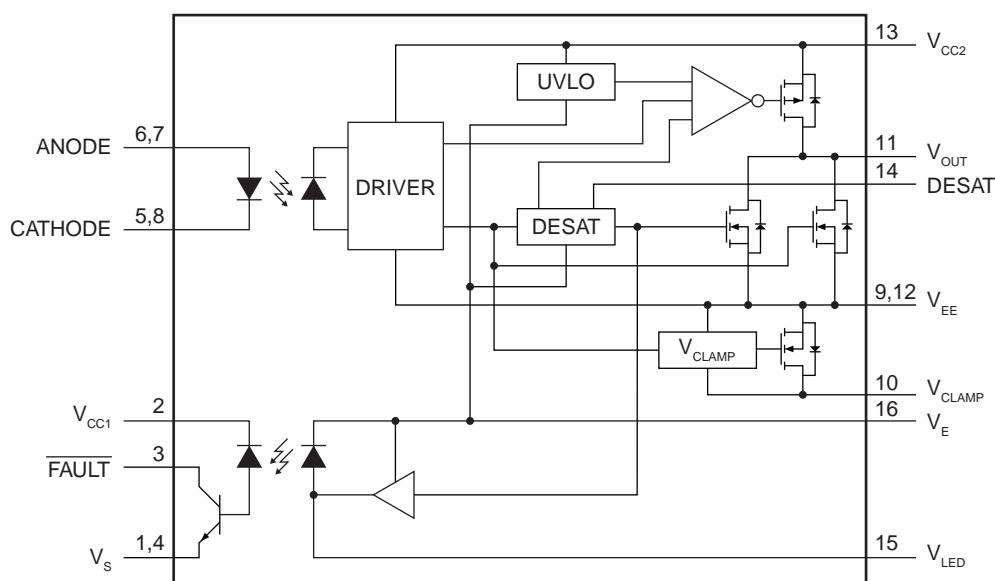
The IX332B is constructed as a power optocoupler with 4250V_{rms} isolation between the control input and power output stages. In addition, an optically isolated, open-collector feedback circuit relays FAULT status to the controller. Both optical isolation circuits employ highly efficient infrared LEDs.

Featuring soft IGBT turn-off, isolated fault feedback, under voltage lock-out with hysteresis, active Miller clamping, and V_{CE} desaturation detection, the IX332B offers engineers design flexibility and maximum circuit protection.

Ordering Information

Part	Description
IX332B	16-Pin SOIC Package (50/Tube)
IX332BTR	16-Pin SOIC Package(1000/Reel)

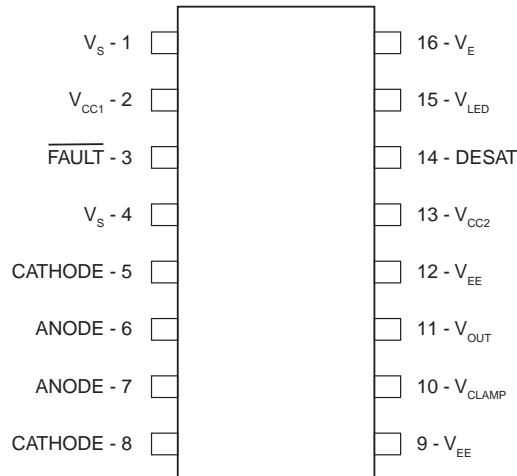
IX332B Block Diagram



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1. Specifications

1.1 Package Pinout



1.2 Pin Description

Pin#	Name	Description
1	V_S	Fault Channel Ground
2	V_{CC1}	Positive Fault Channel supply voltage. (3.3 V to 5.5 V)
3	\overline{FAULT}	Fault output. \overline{FAULT} changes from a high impedance state to a logic low output due to the voltage on the DESAT pin exceeding an internal reference voltage. \overline{FAULT} output is an open collector output.
4	V_S	Fault Channel Ground
5	CATHODE	Cathode
6	ANODE	Anode
7	ANODE	Anode
8	CATHODE	Cathode
9	V_{EE}	Output supply voltage return
10	V_{CLAMP}	Miller clamp
11	V_{OUT}	Gate drive voltage output
12	V_{EE}	Output supply voltage return
13	V_{CC2}	Positive output supply voltage
14	DESAT	Desaturation voltage input. When the voltage on DESAT exceeds an internal reference voltage of 6.5V while the IGBT is on, FAULT output is changed from a high impedance state to a logic low state.
15	V_{LED}	LED anode. This pin must be left unconnected for guaranteed data sheet performance. (For optical coupling testing only)
16	V_E	Common (IGBT emitter) output supply voltage.

1.3 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Note
Storage Temperature	T_S	-	125	°C	-
Operating Temperature	T_A	- 40	105	°C	2
Output IC Junction Temperature	T_J	-	125	°C	2
Average Input Current	$I_{F(AVG)}$	-	20	mA	1
Peak Transient Input Current, (<1 μ s pulse width, 300pps)	$I_{F(TRAN)}$	-	1	A	-
Reverse Input Voltage	V_R	-	5	V	-
“High” Peak Output Current	$I_{OH(PEAK)}$	-	2.5	A	3
“Low” Peak Output Current	$I_{OL(PEAK)}$	-	2.5	A	3
Positive Input Supply Voltage	V_{CC1}	- 0.5	7	V	-
\overline{FAULT} Output Current	I_{FAULT}	-	8	mA	-
\overline{FAULT} Pin Voltage	V_{FAULT}	- 0.5	V_{CC1}	V	-
Total Output Supply Voltage	$(V_{CC2} - V_{EE})$	- 0.5	35	V	-
Negative Output Supply Voltage	$(V_E - V_{EE})$	- 0.5	15	V	-
Positive Output Supply Voltage	$(V_{CC2} - V_E)$	- 0.5	35- $(V_E - V_{EE})$	V	-
Gate Drive Output Voltage	$V_{O(PEAK)}$	- 0.5	V_{CC2}	V	-
Peak Clamping Sinking Current	I_{Clamp}	-	1.7	A	-
Miller Clamping Pin Voltage	V_{Clamp}	- 0.5	V_{CC2}	V	-
DESAT Voltage	V_{DESAT}	V_E	$V_E + 10$	V	-
Input Power Dissipation	P_I	50	-	mW	-
Output Power Dissipation	P_O	-	600	mW	2
Isolation Voltage	V_{ISO}	4250	-	V_{rms}	17,18

1.4 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units	Note
Operating Temperature	T_A	- 40	105	°C	2
Total Output Supply Voltage	$(V_{CC2} - V_{EE})$	15	30	V	-
Negative Output Supply Voltage	$(V_E - V_{EE})$	0	15	V	4
Positive Output Supply Voltage	$(V_{CC2} - V_{EE})$	15	30 $(V_E - V_{EE})$	V	-
Input Current (ON)	$I_{F(ON)}$	8	12	mA	-
Input Voltage (OFF)	$V_{F(OFF)}$	- 3.6	0.8	V	-

1.5 Electrical Specifications (DC)

Unless otherwise noted, all typical values at $T_A = 25^\circ\text{C}$, $V_{CC2} - V_{EE} = 30\text{V}$, $V_E - V_{EE} = 0\text{V}$; all Minimum/Maximum specifications are at Recommended Operating Conditions. Positive Supply Voltage used.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Fig.	Note
FAULT Logic Low Output Voltage	$I_{\text{FAULT}} = 1.1\text{ mA}$, $V_{CC1} = 5.5\text{V}$	V_{FAULTL}	-	0.1	0.4	V	-	-
	$I_{\text{FAULT}} = 1.1\text{ mA}$, $V_{CC1} = 3.3\text{V}$		-	0.1	0.4		-	-
FAULT Logic High Output Current	$V_{CC1} = 5.5\text{V}$	I_{FAULTH}	-	0.037	0.5	μA	-	-
	$V_{CC1} = 3.3\text{V}$		-	0.016	0.3		-	-
High Level Output Current	$V_O = V_{CC2} - 4\text{V}$	I_{OH}	- 0.5	-	-	A	2,6,22	5
	$V_O = V_{CC2} - 15\text{V}$		- 2	-	-			3
Low Level Output Current	$V_O = V_{EE} + 2.5\text{V}$	I_{OL}	0.5	-	-	A	3,7,23	5
	$V_O = V_{EE} + 15\text{V}$		2	-	-			3
Low Level Output Current During Fault Condition	$V_{\text{OUT}} - V_{EE} = 14\text{V}$	I_{OLF}	90	121	230	mA	-	-
High Level Output Voltage	$I_O = 100\text{mA}$	V_{OH}	$V_{CC} - 0.5$	-	-	V	4,25	-
Low Level Output Voltage	$I_O = 100\text{mA}$	V_{OL}	-	0.166	0.5	V	5,26	-
Clamp Pin Threshold Voltage	-	V_{tClamp}	-	3.1	-	V	-	-
Clamp Low Level Sinking Current	$V_O = V_{EE} + 2.5\text{V}$	I_{CL}	0.4	-	-	A	8	-
High Level Supply Current	$I_O = 0\text{mA}$	I_{CC2H}	-	3.8	5	mA	10,11,27,28	-
Low Level Supply Current	$I_O = 0\text{mA}$	I_{CC2L}	-	2.75	5	mA		-
Blanking Capacitor Charging Current	$V_{\text{DESAT}} = 2\text{V}$	I_{CHG}	- 0.13	0.247	- 0.33	mA	12,29	6
Blanking Capacitor Discharge Current	$V_{\text{DESAT}} = 7\text{V}$	I_{DISCHG}	10	29	-	mA	30	-
DESAT Threshold	$V_{CC2} - V_E > V_{\text{UVLO-}}$	V_{DESAT}	6	6.5	7.5	V	13	-
UVLO Threshold	$V_O > 5\text{V}$	$V_{\text{UVLO+}}$	10.5	11.8	12.5	V	-	7
	$V_O < 5\text{V}$	$V_{\text{UVLO-}}$	9.2	10.4	11.1		-	8
UVLO Hysteresis	-	$(V_{\text{UVLO+}}) - (V_{\text{UVLO-}})$	0.4	1.4	-	V	-	-
Threshold Input Current Low to High	$I_O = 0\text{ mA}$, $V_O > 5\text{ V}$	I_{FLH}	-	0.9	4	mA	-	-
Threshold Input Voltage High to Low		V_{FHL}	0.8	-	-	V	-	-
Input Forward Voltage	$I_F = 10\text{ mA}$	V_F	1	1.4	1.75	V	-	-
Temperature Coefficient of Input Forward Voltage	-	$\Delta V_F / \Delta T_A$	-	1.3	-	mV/°C	-	-
Input Reverse Breakdown Voltage	$I_R = 10\mu\text{A}$	B_{VR}	5	-	-	V	-	-
Input Capacitance	$f = 1\text{MHz}$, $V_F = 0\text{ V}$	C_{IN}	-	26	-	pF	-	-

1.6 Switching Specifications (AC)

Unless otherwise noted, all typical values at $T_A = 25^\circ\text{C}$, $V_{CC2} - V_{EE} = 30\text{V}$, $V_E - V_{EE} = 0\text{V}$; all Minimum/Maximum specifications are at Recommended Operating Conditions. Only Positive Supply Voltage used.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Fig.	Note
Propagation Delay Time to High Output Level	$R_g = 10\Omega$, $C_g = 10\text{nF}$, $f = 10\text{kHz}$, Duty Cycle = 50%, $I_F = 10\text{mA}$, $V_{CC2} = 30\text{V}$	t_{PLH}	70	109	220	ns	1,14,15,16,17,31	10
Propagation Delay Time to Low Output Level		t_{PLH}	70	112	220		1,14,15,16,17,31	-
Pulse Width Distortion		PWD	-100	3	100		-	9,12
Propagation Delay Difference Between Any Two Parts or Channels		$(t_{PLH} - t_{PLH})$ PDD	-150	-	150		-	11,12
Rise Time		t_R	-	13	-		-	-
Fall Time		t_F	-	10	-		-	-
DESAT Sense to 90% VO Delay	$C_{DESAT} = 100\text{pF}$, $R_g = 10\Omega$, $C_g = 10\text{nF}$, $V_{CC2} = 30\text{V}$	$t_{DESAT(90\%)}$	-	0.2	0.5	μs	18,32,38	14
DESAT Sense to 10% VO Delay	$C_{DESAT} = 100\text{pF}$, $R_g = 10\Omega$, $C_g = 10\text{nF}$, $V_{CC2} = 30\text{V}$	$t_{DESAT(10\%)}$	-	1.7	3	μs	19,20,21,38	-
DESAT Sense to Low Level FAULT Signal Delay	$C_{DESAT} = 100\text{pF}$, $R_F = 2.1\text{k}\Omega$, $C_F = \text{Open}$, $R_g = 10\Omega$, $C_g = 10\text{nF}$, $V_{CC2} = 30\text{V}$	$t_{DESAT(FAULT)}$	-	0.120	0.5	μs	32,38	13
DESAT Sense to DESAT Low Propagation Delay	$C_{DESAT} = 100\text{pF}$, $R_F = 2.1\text{k}\Omega$, $R_g = 10\Omega$, $C_g = 10\text{nF}$, $V_{CC2} = 30\text{V}$	$t_{DESAT(LOW)}$	-	0.1	-	μs	32,38	14
DESAT Input Mute		$t_{DESAT(MUTE)}$	5	-	-	μs	38	-
RESET to High Level FAULT Signal Delay	$C_{DESAT} = 100\text{pF}$, $R_F = 2.1\text{k}\Omega$, $R_g = 10\Omega$, $C_g = 10\text{nF}$, $V_{CC1} = 5.5\text{V}$, $V_{CC2} = 30\text{V}$	$t_{RESET(FAULT)}$	-	1	2	μs	-	-
	$C_{DESAT} = 100\text{pF}$, $R_F = 2.1\text{k}\Omega$, $R_g = 10\Omega$, $C_g = 10\text{nF}$, $V_{CC1} = 3.3\text{V}$, $V_{CC2} = 30\text{V}$		0.8	1.1	2.5		-	-
Output High Level Common Mode Transient Immunity	$T_A = 25^\circ\text{C}$, $I_F = 10\text{mA}$, $V_{CM} = 1500\text{V}$, $V_{CC2} = 30\text{V}$, $R_F = 2.1\text{k}\Omega$, $C_F = 15\text{pF}$	$ CM_H $	25	-	-	$\text{kV}/\mu\text{s}$	33,34,35,36	15
	$T_A = 25^\circ\text{C}$, $I_F = 10\text{mA}$, $V_{CM} = 1500\text{V}$, $V_{CC2} = 30\text{V}$, $R_F = 2.1\text{k}\Omega$, $C_F = 200\text{pF}$		50	-	-			15,19
Output Low Level Common Mode Transient Immunity	$T_A = 25^\circ\text{C}$, $V_F = 0\text{V}$, $V_{CM} = 1500\text{V}$, $V_{CC2} = 30\text{V}$, $R_F = 2.1\text{k}\Omega$, $C_F = 15\text{pF}$	$ CM_L $	25	-	-	$\text{kV}/\mu\text{s}$	33,34,35,36	16
	$T_A = 25^\circ\text{C}$, $V_F = 0\text{V}$, $V_{CM} = 1500\text{V}$, $V_{CC2} = 30\text{V}$, $R_F = 2.1\text{k}\Omega$, $C_F = 200\text{pF}$		50	-	-			

1.7 Isolation Characteristics

Parameter	Conditions	Symbol	Min	Units	Fig.	Note
Insulation Resistance	$V_{IO} = 500\text{ V}$	R_{IO}	10^9	Ω	-	18
Input-Output Momentary Withstand Voltage	$RH < 50\%$, $t = 1\text{ min}$, $T_A = 25^\circ\text{C}$	V_{ISO}	4250	V_{rms}	-	17,18
Capacitance (Input-Output), Typical	$f = 1\text{ MHz}$	C_{IO}	0.5	pF	-	-

Notes:

- Derate linearly above 70°C free air temperature at a rate of $0.3\text{mA}/^\circ\text{C}$.
- Derate linearly above 25°C free air temperature at a rate of $6.2\text{mW}/^\circ\text{C}$.
- Maximum pulse width = $10\mu\text{s}$. This value is intended to allow for component tolerances for designs with IO peak minimum = 2A . Derate linearly from 3A at $+25^\circ\text{C}$ to 2.5A at $+105^\circ\text{C}$. This compensates for increased I_{OPEAK} due to changes in V_{OL} over temperature.
- This supply is optional. Required only when negative gate drive is implemented.
- Maximum pulse width = $50\mu\text{s}$.
- See the DESAT fault detection blanking time section in the applications notes at the end of this data sheet for further details.
- This is the "increasing" (i.e. turn-on, or "positive going," direction) of $V_{CC2} - V_E$
- This is the "decreasing" (i.e. turn-off, or "negative going," direction) of $V_{CC2} - V_E$
- Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given unit.
- As measured from I_F to V_O .
- The difference between t_{PHL} and t_{PLH} between any two IX332B parts under the same test conditions.
- As measured from ANODE, CATHODE of LED to V_{OUT}
- This is the amount of time from when the DESAT threshold is exceeded, until the FAULT output goes low.
- This is the amount of time the DESAT threshold must be exceeded before V_{OUT} begins to go low, and the FAULT output to go low. This is supply voltage dependent.
- Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM} , to assure that the output will remain in the high state (i.e., $V_O > 15\text{V}$ or $FAULT > 2\text{V}$).
- Common mode transient immunity in the low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM} , to assure that the output will remain in a low state (i.e., $V_O < 1\text{V}$ or $FAULT < 0.8\text{V}$).
- In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage: $5100V_{rms}$ for one second.
- This is a two-terminal measurement: pins 1-8 are shorted together and pins 9-16 are shorted together.
- Split resistors network with a ratio of 1:1 is needed at input LED1. See **Figure 36**.

2. Performance Data

Figure 1.

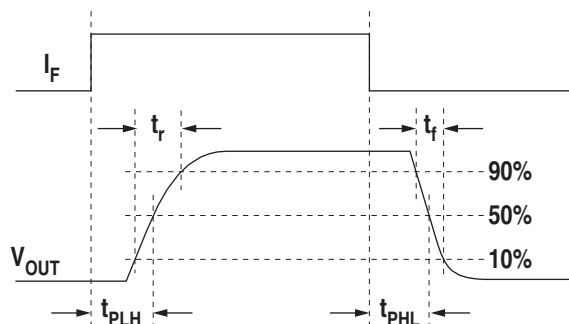


Figure 2.

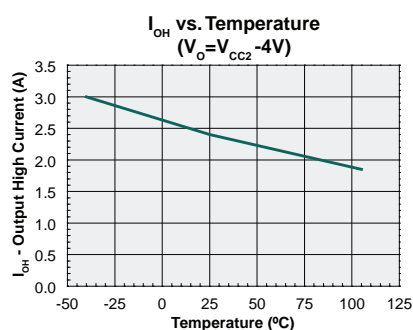


Figure 3.

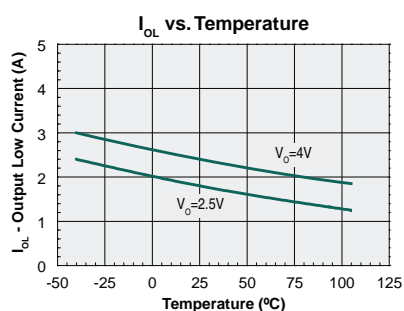


Figure 4.

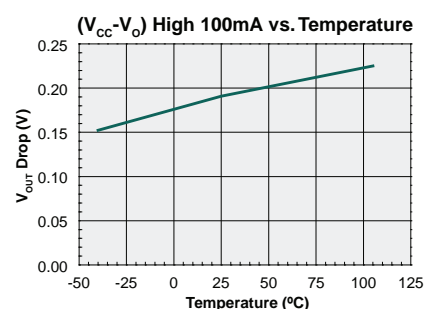


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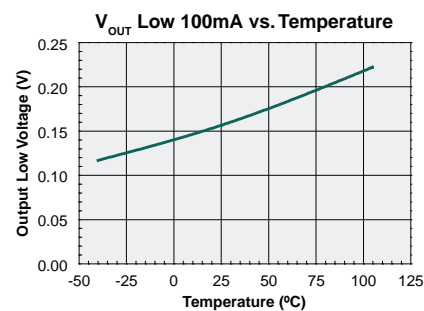


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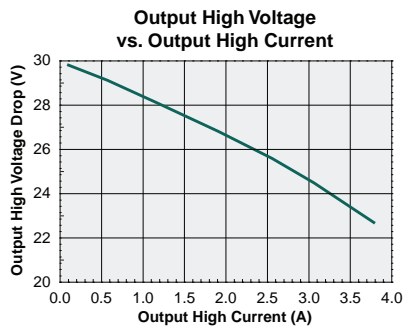


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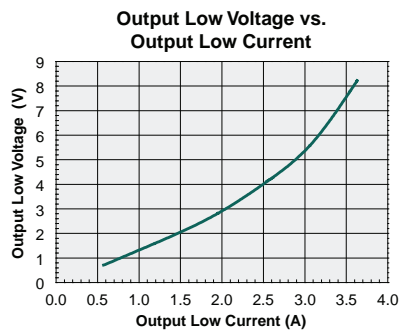


Figure 8.

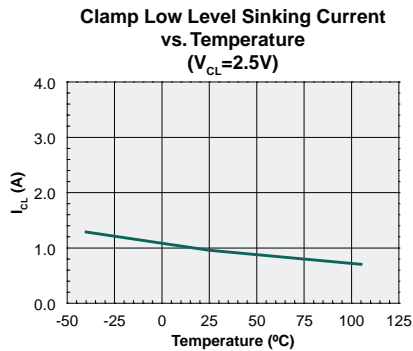


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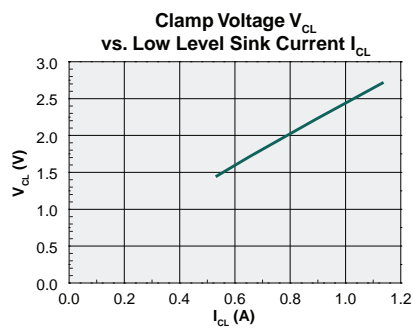


Figure 10.

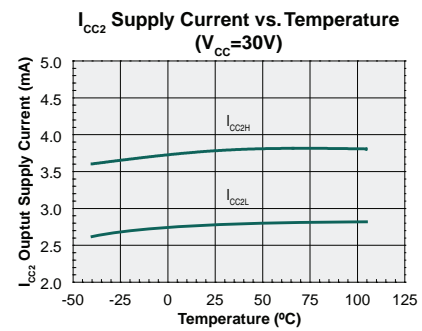


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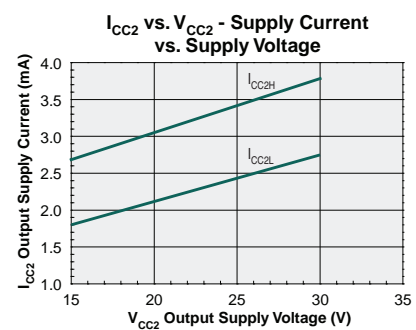


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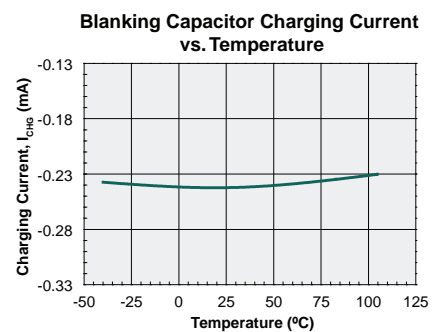


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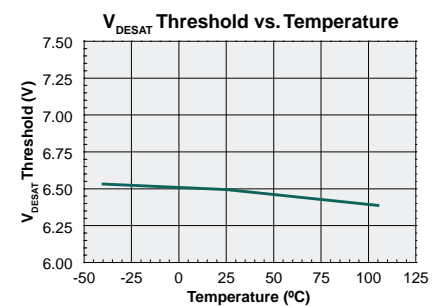


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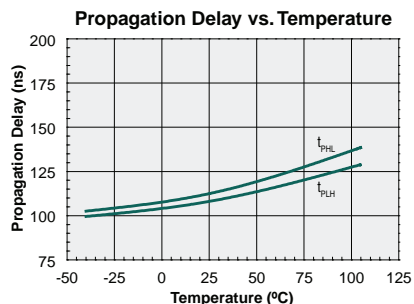


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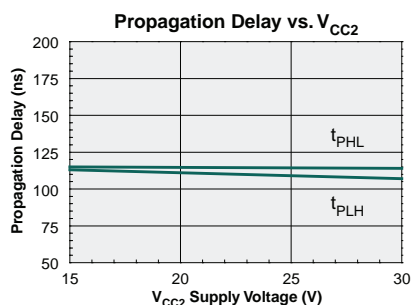


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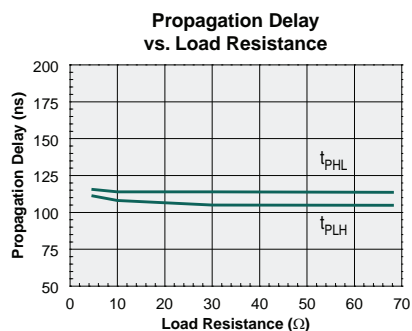


Figure 17.

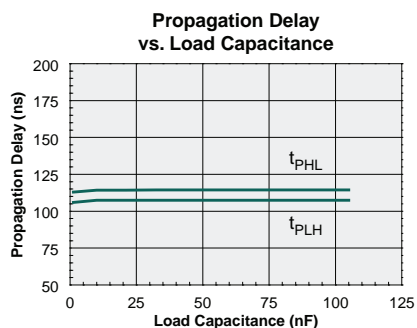


Figure 18.

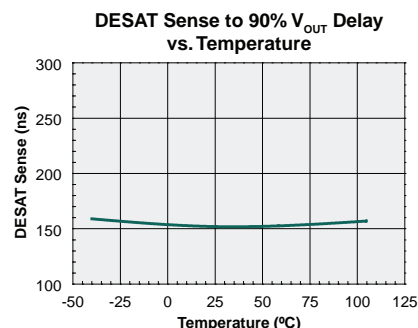


Figure 19.

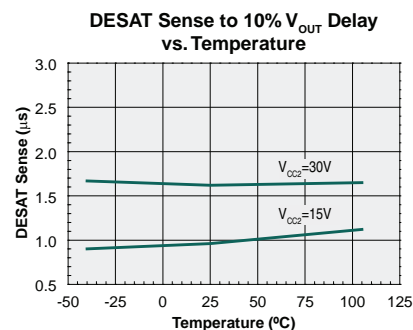


Figure 20.

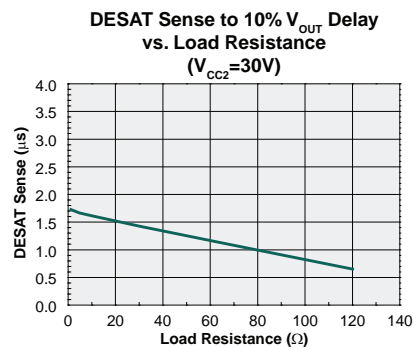


Figure 21.

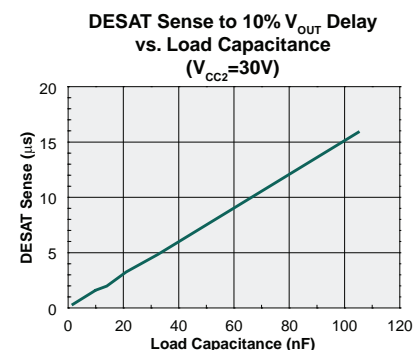


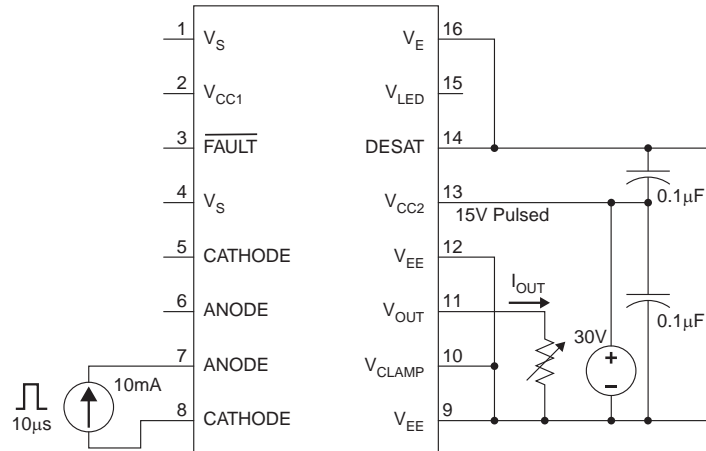
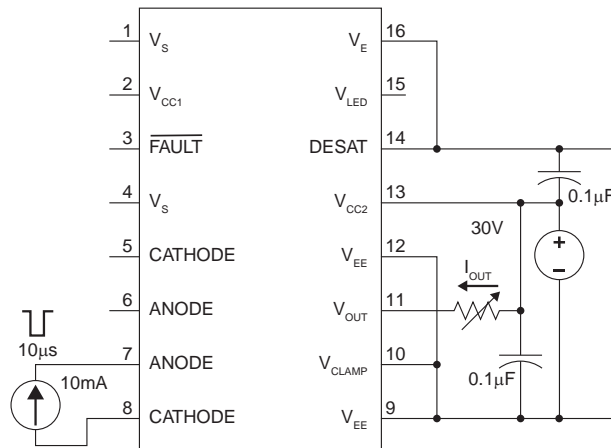
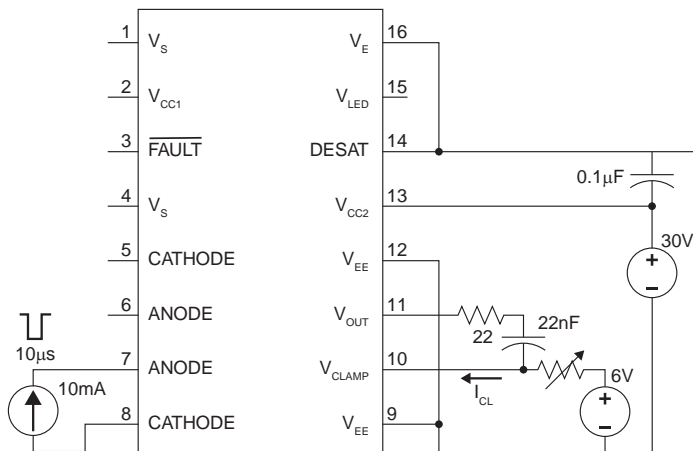
Figure 22. I_{OH} Pulsed & V_{OH} vs. I_{OH} Test Circuit

Figure 23. I_{OL} Pulsed Test Circuit

Figure 24. V_{CL} vs. I_{CL} Test Circuit


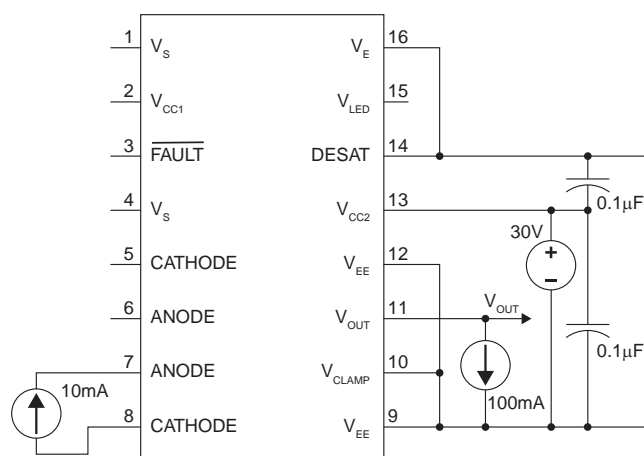
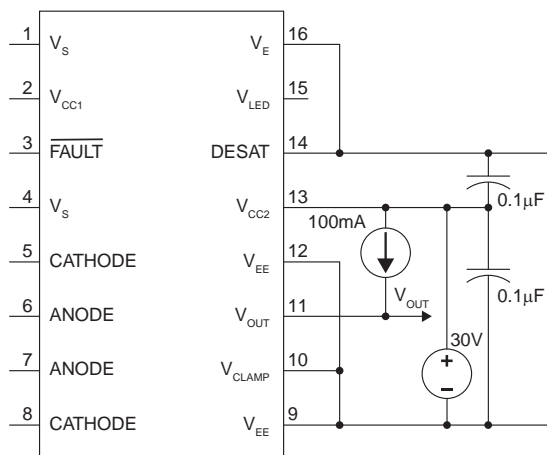
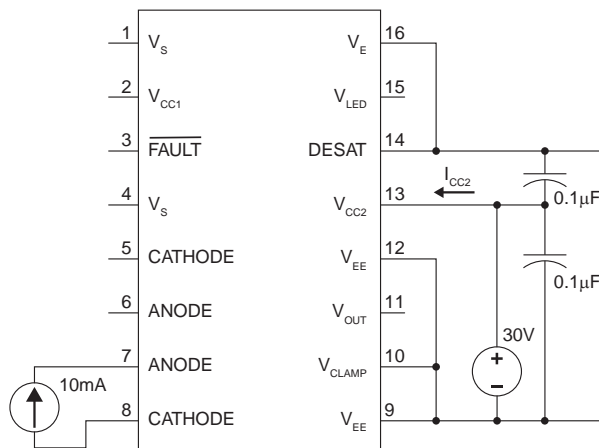
Figure 25. V_{OH} Test Circuit

Figure 26. V_{OL} Test Circuit

Figure 27. I_{CC2H} Test Circuit


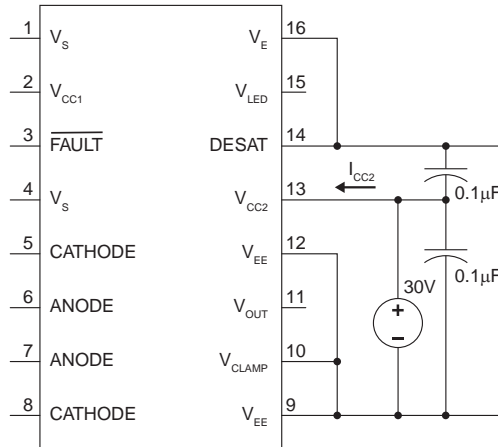
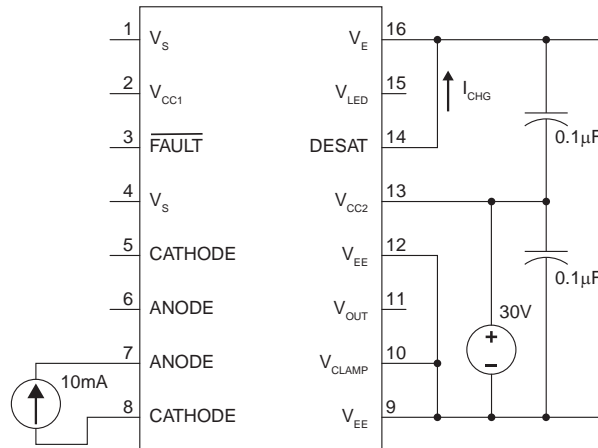
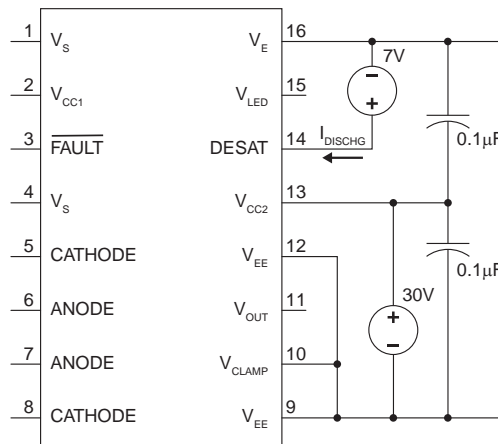
Figure 28. I_{CC2L} Test Circuit

Figure 29. I_{CHG} Pulsed Test Circuit

Figure 30. I_{DSCHG} Test Circuit


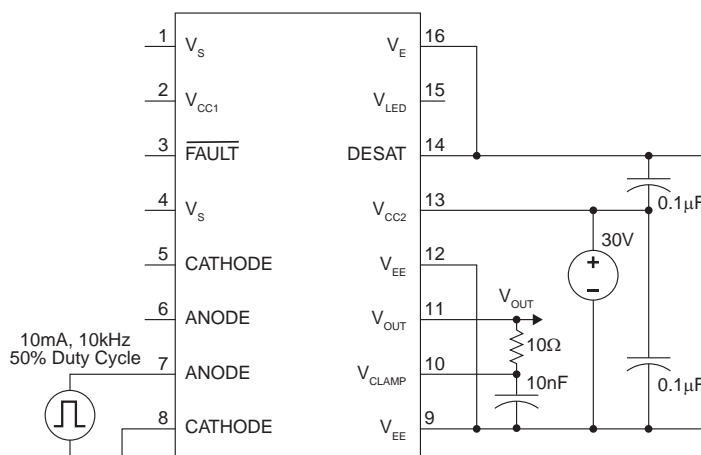
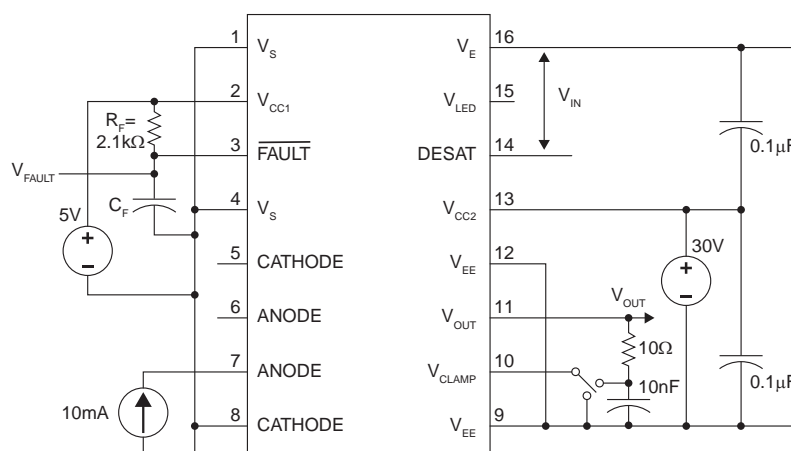
Figure 31. t_{PLH} , t_{PHL} , t_F , t_R Test Circuit

Figure 32. t_{DESAT} Fault Test Circuit


Figure 33. CMR Test Circuit LED2 Off

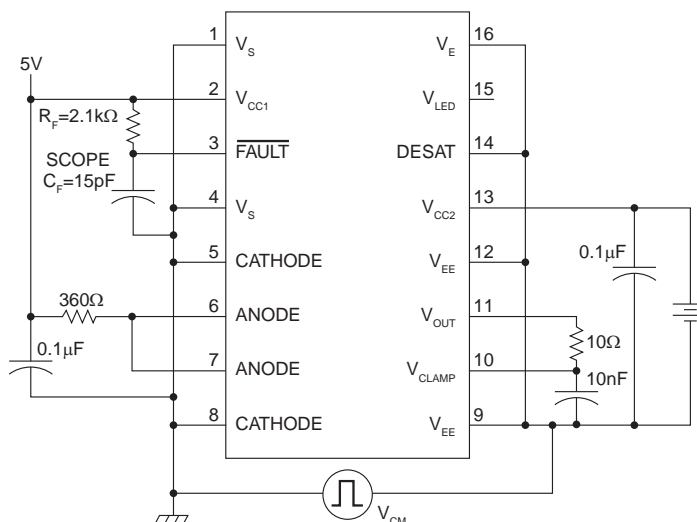


Figure 34. CMR Test Circuit LED2 On

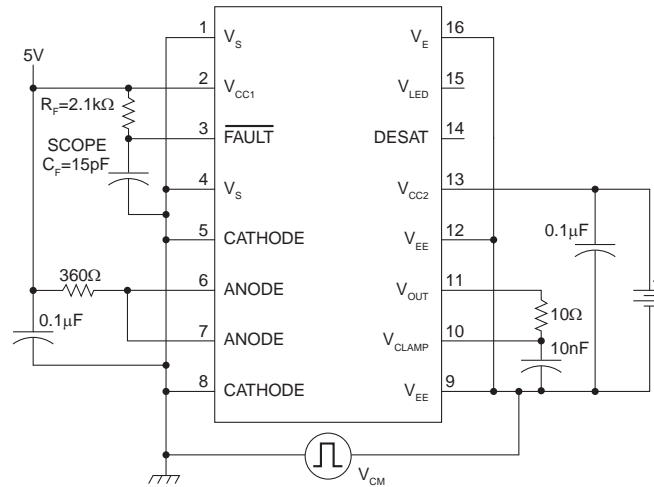


Figure 35. Driver CMR Test Circuit LED1 Off

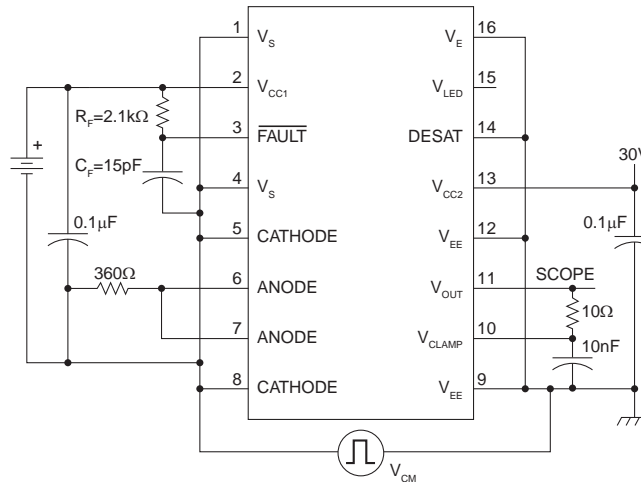
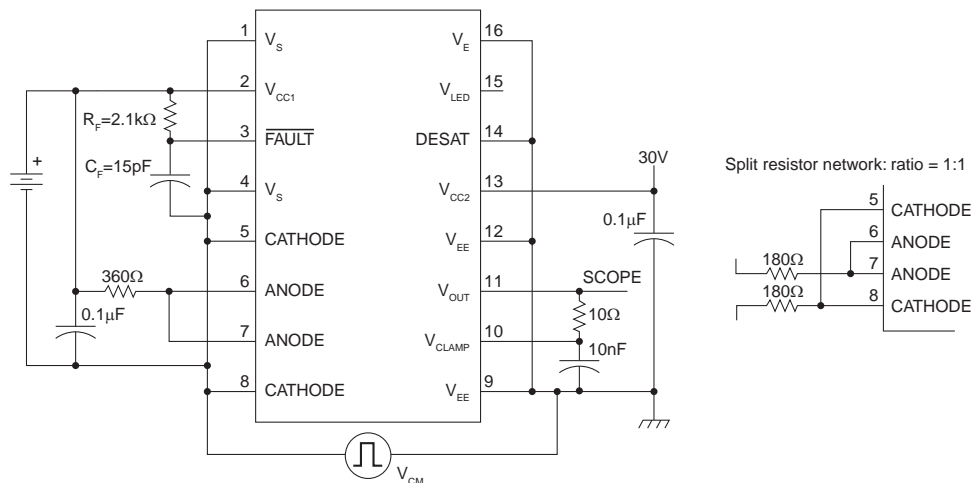


Figure 36. Driver CMR Test Circuit LED1 On



3. Application Information

3.1 Product Overview

The IX332B is a high speed, optically isolated, 2.5A output current gate driver capable of driving power IGBTs and MOSFETs with voltage ratings up to 1200V. It is very well suited for various industrial motor control inverter applications and other power supply systems where isolation and power switch protection is of critical importance.

The driver includes many integrated features such as an active Miller clamp, which simplifies some designs by eliminating the need for negative gate drive and also allows for an inexpensive bootstrap supply for a high side driver. The desaturation detection circuit protects the driven IGBT from short circuits, and provides an isolated optical feedback channel in case a fault condition has occurred. In addition, there is an under voltage lockout (UVLO) that provides protection in case insufficient voltage is present at the gate drive.

This integrated gate driver consists of two isolated channels activated by light emitting diodes which are optically coupled to an integrated driver circuit. This optical circuit arrangement achieves high input to output isolation voltage of 4250Vrms while maintaining high common mode noise immunity. The IX332B is housed in compact 16- Pin SOIC package.

3.2 Normal Operation and Application Circuit

The circuit in **Figure 37** shows the minimum circuit configuration for the IX332B.

Driving the LED turns on the Gate drive voltage V_{OUT} via the internal isolated gate drive circuitry and PMOS transistor. When LED is turned on, V_{OUT} approaches V_{CC2} and provides sufficient gate voltage for the external IGBT device assuming:

$$V_{GEmax} > (V_{CC2} - V_{EE}) > V_{GETH}$$

where V_{GEmax} is the IGBT maximum specified V_{GE} voltage and V_{GETH} is the minimum V_{GE} threshold of the IGBT device. The UVLO function on the IX332B will prevent the IGBT from turning on if there is not sufficient voltage at the gate as described in **Section 3.6**.

To turn on the device, a nominal current of 10mA is driven through the LED by a standard CMOS gate, transistor or microprocessor I/O line. **Figure 37** shows a microprocessor I/O capable of sinking the required

10mA to activate the LED and the output. R_{LED} is the LED limiting resistor where the value is determined by:

$$R_{LED} = \frac{V_{CC1} - V_F}{10mA}$$

where V_F is the maximum LED forward voltage published on the data sheet. For the example circuit in **Figure 37** for a 3.3V system we have:

$$R_{LED} = \frac{3.3V - 1.5V}{10mA} = 180\Omega$$

which is a standard value.

Referring to the figure, D_{DESAT} is a fast recovery diode described in **Section 3.4**. Resistor R_D and capacitor C_D form a time constant for the DESAT blanking interval. Also, R_D limits current to the DESAT pin as protection from excessive current damaging the IC.

Resistor R_G limits gate charge current and controls IGBT rise and fall times. The test circuits use a value of 15Ω . The IGBT gate drive components are discussed in more detail in the applications section. The connection from the IX332B through R_G to the gate of the IGBT should be as low inductance as possible to prevent excessive ringing.

The V_{CLAMP} pin is the Miller clamping circuit that connects to the IGBT gate to safely turn off the IGBT in single supply applications.

The two $0.1\mu F$ capacitors are used for decoupling switching transients and should be placed close to the respective pins in the layout of the PCB.

The \overline{FAULT} pin is an open collector output indicating a DESAT. This pin requires an adequately sized pull-up resistor R_P to V_{CC1} to be functional. Additionally, C_F can be installed as a filter capacitor for potential high voltage transients that can couple through the parasitic capacitance of the IX332B or PCB capacitance.

The timing diagram illustrates the behavior of the LED driver during different fault conditions. The signals shown are I_F (Forward Current), V_{DESAT} (Desaturation Voltage), V_{OUT} (Output Voltage), and $FAULT$ (Fault Flag).

- I_F (Forward Current):** Shows a pulse during normal operation and a low level during fault conditions.
- V_{DESAT} (Desaturation Voltage):** Shows a peak voltage of 6.5V during normal operation and a low level during fault conditions.
- V_{OUT} (Output Voltage):** Shows a ramp-up during normal operation and a ramp-down during fault conditions.
- $FAULT$ (Fault Flag):** Shows a low level during normal operation and a high level during fault conditions.

Key timing parameters and events are labeled:

- $t_{DESAT(LOW)}$: Desaturation time during low current.
- t_{BLANK} : Blank time during fault.
- $t_{DESAT(10\%)}$: Desaturation time at 10% current.
- $t_{DESAT(90\%)}$: Desaturation time at 90% current.
- $t_{DESAT(50\%)}$: Desaturation time at 50% current.
- $t_{DESAT(MUTE)}$: Desaturation time during mute.
- $t_{RESET(FAULT)}$: Reset time during fault.

Annotations include "Reset done during the next LED turn-on" and "50%", "90%", "10%", and "50%" indicating current levels.

The fault output pin is an open collector output and requires a pullup resistor, R_F , to provide a high level signal. In addition, the $\overline{\text{FAULT}}$ output can be OR-ed with additional external protection monitoring circuits.

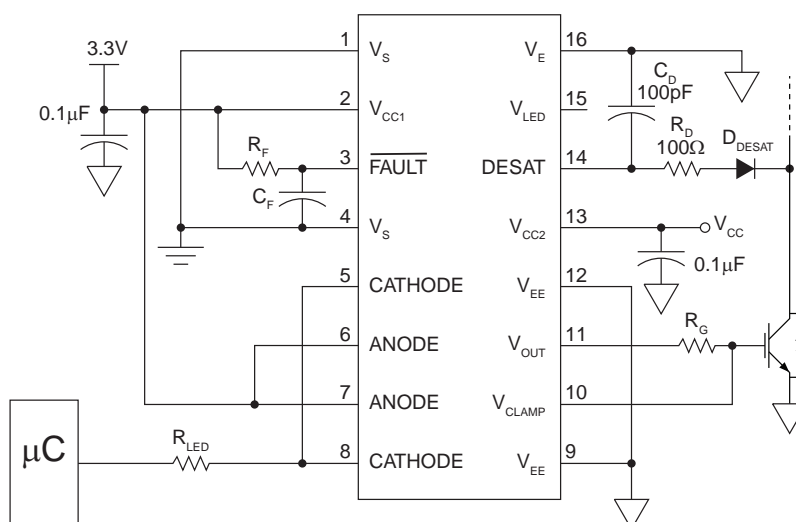
An external capacitor, C_F , on the $\overline{\text{FAULT}}$ pin for high common mode rejection, CMR, is optional and not required because the IX332B will pass this test without the capacitor.

3.4 DESAT Pin Protection & D_{DESAT} Diode Selection

Fast recovery, freewheeling diodes across power IGBTs are exposed to very large instantaneous voltage transients, which can be present on the DESAT pin. In order to limit these currents to levels that will not cause damage to the IC, a resistor, 100Ω to $1k\Omega$, should be placed in series with the diode.

The D_{DESAT} diode should be a fast recovery type with t_{rr} below 75nS and a breakdown voltage rating of 600V to 1200V , depending on the application. The ES1J-600V diode, or equivalent, would be sufficient.

Figure 39. DESAT Pin Protection



3.5 Soft IGBT Turn-Off

This feature ensures safe IGBT shutdown under fault conditions. The gate driver's V_{OUT} turns off the IGBT in a controlled manner that protects the output from developing large voltage spikes due to parasitic lead inductance, which could damage the IGBT.

3.6 Under-Voltage Lockout (UVLO)

In order to ensure proper power stage switching, the IX332B includes an under voltage lock out circuit, UVLO, which prevents the IGBT from turning on when insufficient voltage is present on the gate. The output voltage, V_{OUT} , remains low as long as the supply voltage, $V_{\text{CC}} - V_{\text{EE}}$, is less than $V_{\text{UVLO+}}$ during power up. If the supply voltage falls below $V_{\text{UVLO-}}$, then V_{OUT} goes low.

3.7 Active Miller Clamp Function

The integrated active Miller clamp circuit enables the controlled sinking of current to ground during high dV/dt turn off transitions. An internal NMOS transistor clamp eliminates the need for the negative supply voltage that is commonly required to safely turn off a power IGBT. When turn-off is initiated, the gate voltage is monitored. The voltage clamp circuit is activated when the gate voltage $V_{\text{OL}} = 2.5\text{V}$ (typical) relative to V_{EE} , and while Miller current is approximately 1100mA . During the IGBT turn on cycle, V_{CLAMP} is disabled.

4. Manufacturing Information

4.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. IXYS Integrated Circuits Division classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation.

We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IX332B	MSL 1

4.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

4.3 Soldering Profile

Provided in the table below is the Classification Temperature (T_C) of this product and the maximum dwell time the body temperature of this device may be ($T_C - 5$)°C or greater. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through-hole devices, and any other processes, the guidelines of J-STD-020 must be observed.

Device	Classification Temperature (T_C)	Dwell Time (t_p)	Max Reflow Cycles
IX332B	260°C	30 seconds	3

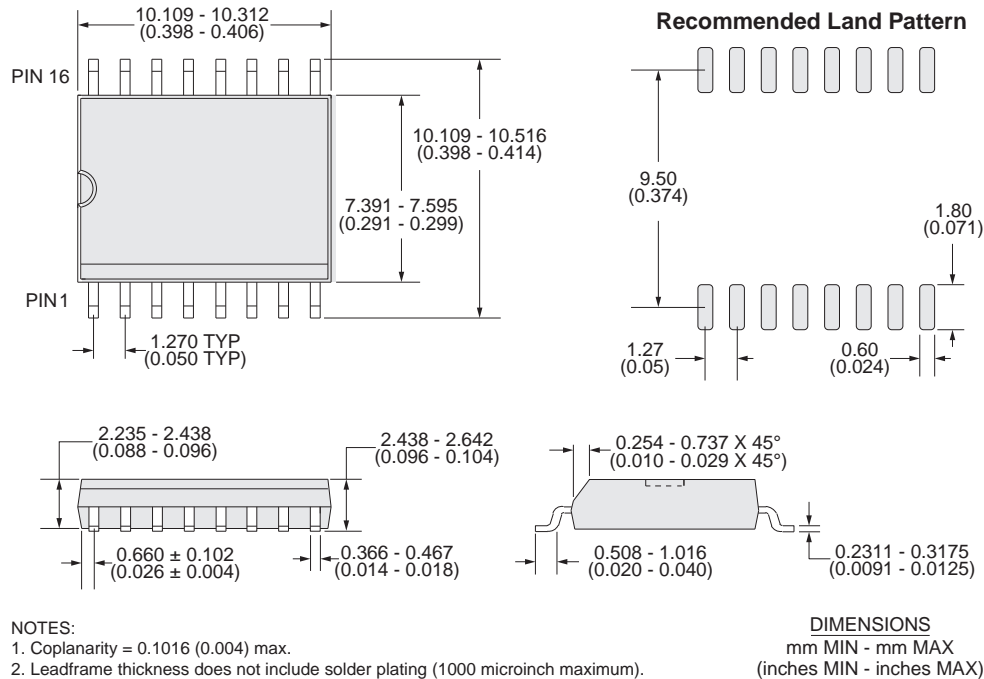
4.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based.

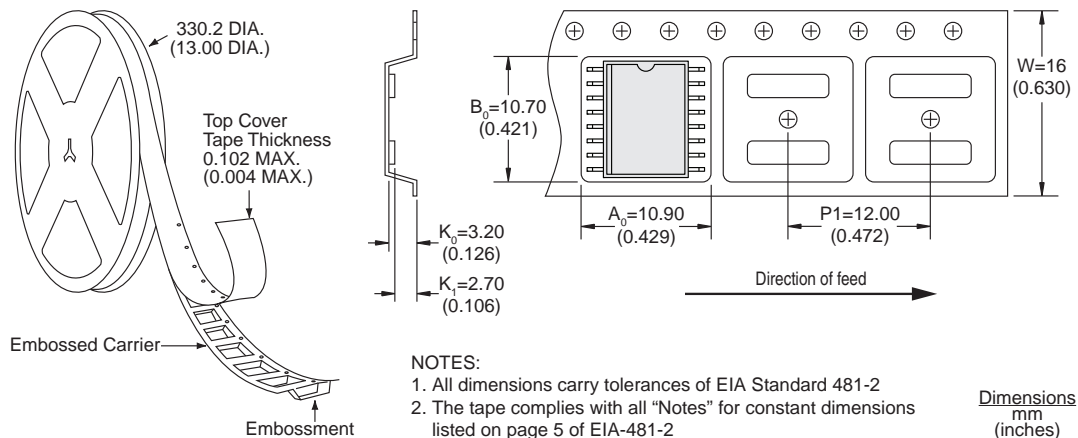


4.5 Package Mechanical Dimensions

4.5.1 IX332B 16-Pin SOIC



4.5.2 IX332BTR Tape & Reel



For additional information please visit our website at: www.ixysic.com

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2/1/2019