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High-Voltage, Overvoltage/Undervoltage, Protection Switch Controller

MAX6399

General Description

The MAX6399 is a small overvoltage and undervoltage protection circuit. The device can monitor a DC-DC output voltage and quickly disconnect the power source from the DC-DC input load when an overvoltage condition occurs. A power-OK output signals when the DC-DC input voltage falls below an adjustable threshold. This controller architecture provides the ability to size the external n-channel MOSFET to meet specific load current requirements.

When the DC-DC monitored output voltage is below the user-adjustable overvoltage threshold, the GATE output of the MAX6399 goes high to enhance the n-channel MOSFET. The MAX6399 offers internal charge-pump circuitry that allows the GATE voltage to be 10V above the input voltage (V_{GS} = 10V) to fully enhance the external n-channel MOSFET, thus minimizing the drainto-source resistance.

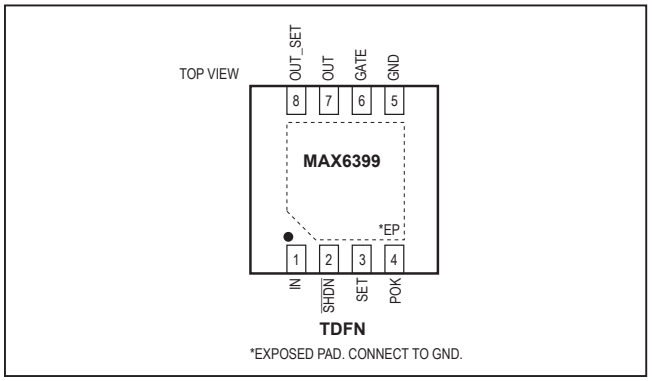
When the monitored output voltage rises above the user-adjusted overvoltage threshold, the GATE output rapidly pulls low to shut off the MOSFET. The MOSFET remains latched off until either the MAX6399 input power or $\overline{SHDN}$ input is cycled. The MAX6399 includes a logic-low shutdown input that disables the GATE. An internal overtemperature detector also disables the gate when the MAX6399 temperature reaches the thermal-shutdown threshold.

The device operates over a wide supply voltage range (5.75V to 72V) and is offered in a small TDFN package, fully specified from -40°C to +125°C.

Applications

- Networking
- Server
- Telecom
- RAID

Pin Configuration



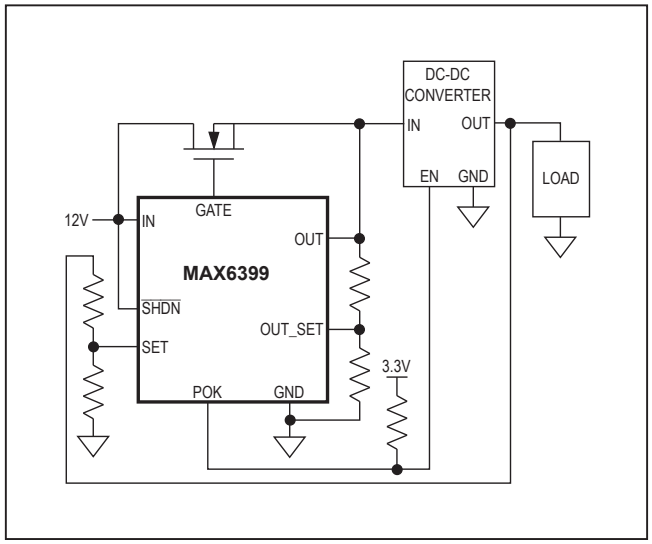
Benefits and Features

- High-Voltage Capability (72V) Allows Direct Monitoring, Ensuring Reliable System Operation in Automotive and Industrial Applications
  - Wide Supply Voltage Range (5.75V to 72V)
  - Specified from -40°C to +125°C
  - Adjustable DC-DC Input Undervoltage-Threshold Power-OK Output
  - Adjustable DC-DC Output Overvoltage Thresholds
- Integrated Protection Features Improve System Reliability
  - Internal Charge Pump Ensures n-Channel MOSFET is Fully Enhanced During Normal Operation (V_{GS} = 10V)
  - Fast GATE Shutoff During Overvoltage with 20mA Sink Capability
  - Latches Off External n-Channel MOSFET During High-Voltage Transients
  - Overtemperature-Shutdown Protection
- Enables Functional Safety at System Level

Ordering Information

PART	PIN-PACKAGE	TOP MARK
MAX6399ATA-T	8 TDFN-8	ANE

Typical Operating Circuit



19-3655; Rev 3; 10/24

Absolute Maximum Ratings

IN, GATE, OUT ..... -0.3V to +80V
$\overline{SHDN}$ ..... -0.3V to (IN + 0.3V)
OUT ..... -0.3V to +80V
GATE to OUT ..... -0.3V to +20V
OUT_SET, SET, POK ..... -0.3V to +12V
Maximum Current (All pins) 50mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin TDFN (derate 18.2mW/°C above +70°C) 1455mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature Range ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN} = 14V; CGATE = 6000pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}		5.75		72.00	V
IN Supply Current	I_{IN}	$\overline{SHDN}$ = high		100	130	µA
		$\overline{SHDN}$ = low		10	22	
IN Undervoltage Lockout		V_{IN} rising, enables GATE	4.68	5	5.50	V
IN Undervoltage Lockout Hysteresis		V_{IN} falling, GATE off		155		mV
SET Threshold Voltage	$V_{TH\ (SET)}$	With respect to GND, SET rising	0.480	0.5	0.517	V
SET Threshold Hysteresis	V_{HYST}			5		% V_{TH}
SET Input Current	I_{SET}		-50		+50	nA
Startup Response Time	t_{START}	$\overline{SHDN}$ rising (Note 2)		100		µs
GATE Rise Time		GATE rising from GND to V_{OUT} + 8V, C_{GATE} = 6000pF, OUT = GND		1		ms
SET to GATE Prop Delay	t_{OV}	SET rising from V_{TH} - 100mV to V_{TH} + 100mV			0.5	µs
GATE Output-Voltage High	V_{OH}	V_{OUT} = V_{IN} = 5V, R_{GATE} to IN = 1MΩ	V_{IN} + 3.6V	V_{IN} + 3.8V	V_{IN} + 4.0V	V
		V_{OUT} = V_{IN}; V_{IN} ≥ 14V, R_{GATE} to IN = 1MΩ	V_{IN} + 15V	V_{IN} + 10V	V_{IN} + 10.7V	
GATE Output-Voltage Low	V_{OL}	GATE sinking 20mA, V_{OUT_SET} = GND			0.3	V
GATE Charge-Pump Current	I_{GATE}	GATE = GND		75		µA
GATE to OUT Clamp Voltage	V_{CLMP}		13.8		18.0	V
$\overline{SHDN}$ Logic-High Input Voltage	V_{IH}		1.4			V
$\overline{SHDN}$ Logic-Low Input Voltage	V_{IL}				0.4	V
$\overline{SHDN}$ Input Pulldown Current		$V_{\overline{SHDN}}$ = 2V, $\overline{SHDN}$ is internally pulled down to GND		1		µA
Thermal-Shutdown Temperature (Note 3)				+150		ºC
Thermal-Shutdown Hysteresis				20		ºC
Power-OK (POK)						
OUT_SET Threshold	$V_{TH\ (OUT\_SET)}$	OUT_SET rising	1.205	1.23	1.258	V

Electrical Characteristics (continued)

(V_{IN} = 14V; CGATE = 6000pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT_SET Hysteresis				5		% V_{TH} (OUT_SET)
OUT_SET to POK Delay		V_{OUT_SET} rising or falling		35		µs
POK Output Voltage Low	V_{OL}	V_{IN} ≥ 1.5V, I_{SINK} = 3.2mA, POK asserted			0.45	V
POK Leakage Current		V_{OUT_SET} = 1.4V			100	nA

Note 1: Specifications to -40°C are guaranteed by design and not production tested.

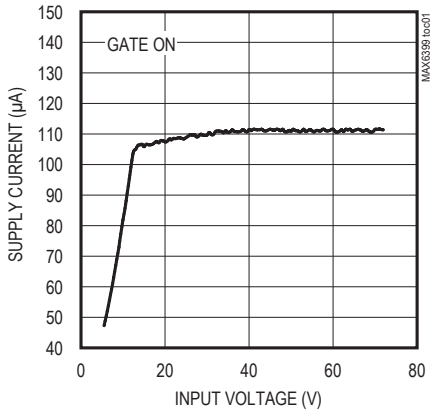
Note 2: The MAX6399 powers up with the external FET in off mode (V_{GATE} = GND). The external FET turns on t_{START} after the device is powered up and all input conditions are valid.

Note 3: For accurate overtemperature shutdown performance, place the device in close thermal contact with the external MOSFET.

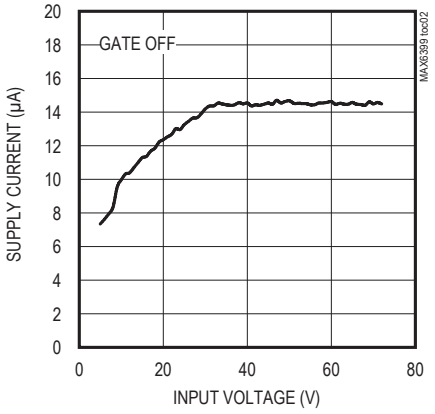
Typical Operating Characteristics

(V_{IN} = 14V, C_{GATE} = 6nF, unless otherwise noted.)

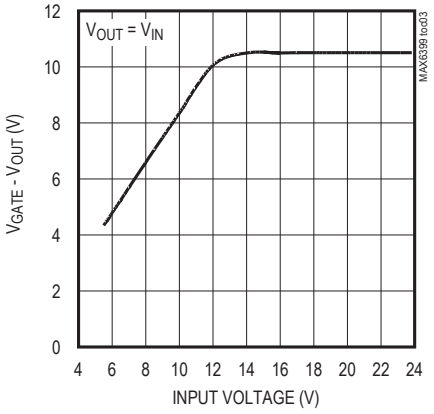
SUPPLY CURRENT vs. INPUT VOLTAGE



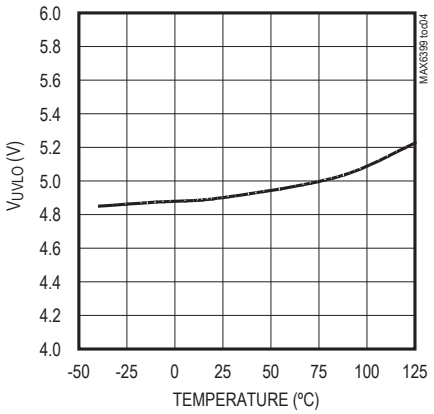
SUPPLY CURRENT vs. INPUT VOLTAGE



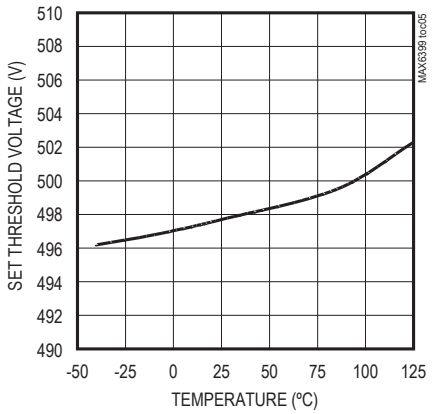
GATE-DRIVE VOLTAGE vs. INPUT VOLTAGE



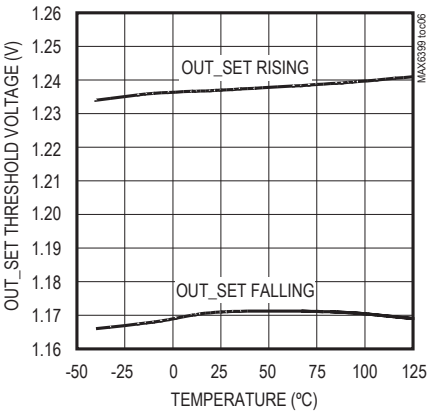
UVLO THRESHOLD vs. TEMPERATURE



SET THRESHOLD vs. TEMPERATURE



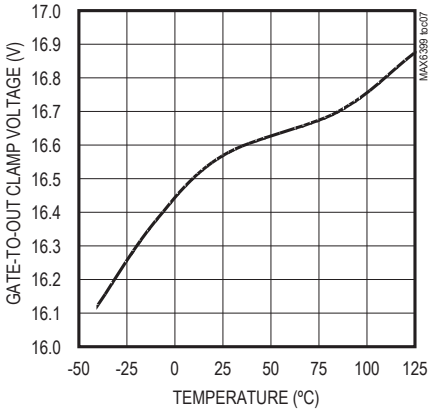
OUT_SET THRESHOLD vs. TEMPERATURE



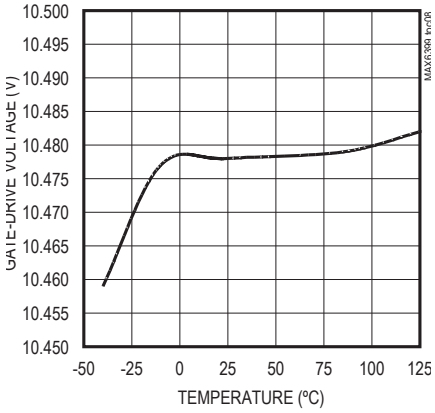
Typical Operating Characteristics (continued)

(V_{IN} = 14V, C_{GATE} = 6nF, unless otherwise noted.)

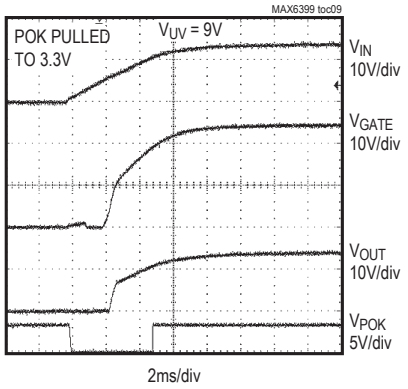
GATE-TO-OUT CLAMP VOLTAGE vs. TEMPERATURE



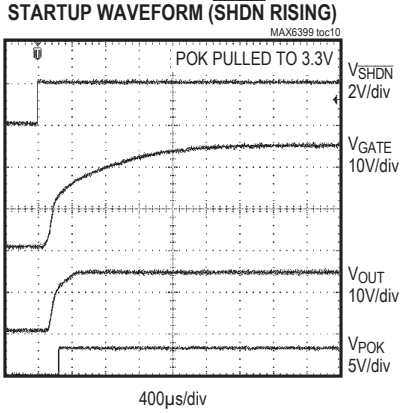
GATE-DRIVE VOLTAGE vs. TEMPERATURE



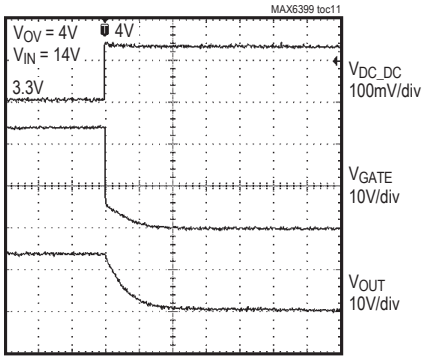
STARTUP WAVEFORM



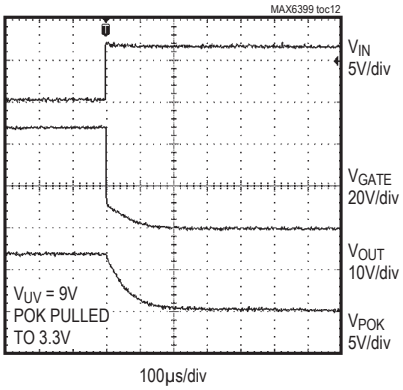
STARTUP WAVEFORM ($\overline{SHDN}$ RISING)



OVERVOLTAGE SWITCH FAULT



UNDERVOLTAGE FAULT



Pin Description

PIN	NAME	FUNCTION
1	IN	Supply Voltage Input. Bypass with a 10µF capacitor (minimum).
2	$\overline{SHDN}$	Shutdown Input. Drive $\overline{SHDN}$ low to force GATE low, turning off the external n-channel MOSFET. $\overline{SHDN}$ is internally pulled down to GND with a 1µA current source. Toggle $\overline{SHDN}$ to unlatch GATE after an overvoltage condition. Connect to IN for normal operation.
3	SET	Overvoltage Threshold Adjustment Input. Use SET to monitor a system output voltage. Connect SET to an external resistor voltage-divider network to adjust the desired overvoltage limit threshold. GATE is quickly turned off when SET rises above its 0.5V (typ) threshold.
4	POK	Power-OK Open-Drain Output. POK asserts low when OUT_SET falls below its 1.23V (typ) threshold.
5	GND	Ground
6	GATE	Gate-Drive Output. Connect GATE to the gate of an external n-channel FET. GATE is a charge pump with a 100µA pullup current to IN + 10V (typ) during normal operation. GATE is quickly turned off during an overvoltage condition. GATE remains latched off until the power is recycled or $\overline{SHDN}$ is toggled. GATE pulls low when $\overline{SHDN}$ is low.
7	OUT	Output Voltage-Sense Input. Connect to the source of the external n-channel MOSFET.
8	OUT_SET	Undervoltage Detector Input. Use OUT_SET to monitor the source of the MOSFET. Connect a resistor-divider from OUT to OUT_SET to adjust the desired undervoltage threshold. POK asserts low when OUT_SET falls below its 1.23V threshold.
—	EP	Exposed Pad. Connect to ground plane.

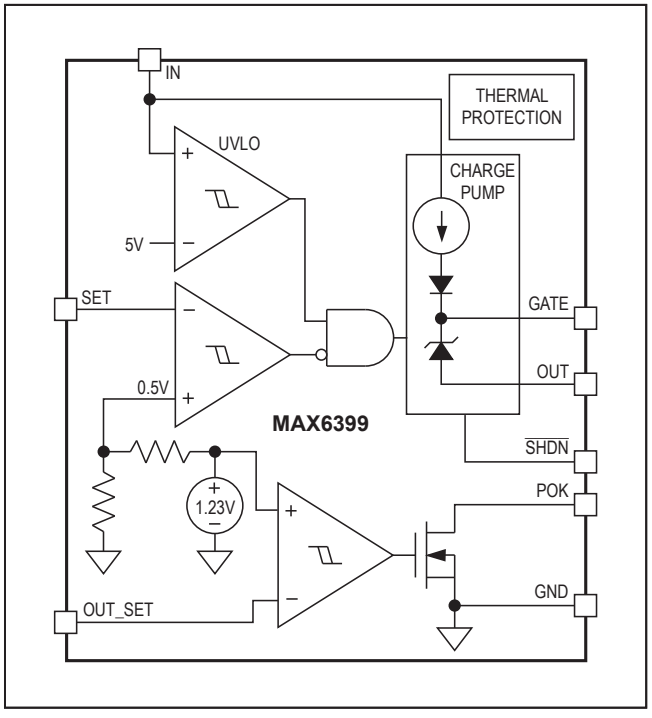


Figure 1. Functional Diagram

Detailed Description

The MAX6399 is an ultra-small, low-current protection circuit utilized in DC-DC converter applications. The MAX6399 monitors the input and output voltages of a DC-DC converter for undervoltage and overvoltage conditions. The MAX6399 controls an external n-channel MOSFET to isolate the load during an overvoltage condition. The device allows system designers to size the external n-channel MOSFET to their load current and board size.

The MAX6399 drives the MOSFET's gate high when the monitored DC-DC output voltage is below the programmable overvoltage threshold, programmed through SET. An internal charge-pump circuit provides a guaranteed 10V gate-to-source drive to ensure low input-to-load voltage drops in normal operating modes. When the monitored DC-DC output voltage rises above the user-adjusted overvoltage threshold, GATE latches low, turning off the MOSFET. The MOSFET remains off until the power is recycled or by toggling $\overline{SHDN}$.

The MAX6399 also monitors for an undervoltage condition at the input of the DC-DC converter through OUT_SET. An active-high, open-drain, power-good output can be used to drive the EN input, notifying the system when the monitored voltage is below the adjusted undervoltage voltage threshold.

The MAX6399 includes internal thermal-shutdown protection, disabling the external MOSFET if the device reaches overtemperature conditions.

Shutdown Control

The MAX6399 active-low $\overline{SHDN}$ input turns off the external MOSFET, disconnecting the load and reducing power consumption. After power is applied and $\overline{SHDN}$ is driven above its logic-high voltage, there is a 100µs delay before GATE begins to enhance. $\overline{SHDN}$ is also utilized to unlatch GATE after an overvoltage condition has been removed.

GATE Voltage

The MAX6399 uses a high-efficiency charge pump to generate the GATE voltage. Upon V_{IN} exceeding the 5V (typ) UVLO threshold, GATE enhances 10V above IN (for $V_{IN} \geq 14V$) with a 100µA pullup current. An overvoltage condition occurs when the voltage at SET pulls above its 0.5V threshold. When the overvoltage fault occurs (SET = 0.5V), GATE latches off, which disconnects the load from the power source (see Figure 2). After the overvoltage fault has disappeared, the fault can be unlatched by toggling $\overline{SHDN}$ or recycling the MAX6399 input.

DC-DC Output Overvoltage Protection

The MAX6399 overvoltage protection features a fast comparator that disconnects the load from the main power line when an overvoltage condition occurs at the output of a DC-DC converter. When an overvoltage condition is sensed, the MAX6399 latches GATE off, disconnecting the power source from the DC-DC input. To unlatch GATE after an overvoltage fault has disappeared, recycle IN or toggle $\overline{SHDN}$.

Setting Output Overvoltage Threshold (SET)

SET provides an accurate means of monitoring a system voltage for an overvoltage fault. Use a resistordivider network to set the desired overvoltage condition (Figure 2). SET has a rising 0.5V threshold.

Begin by selecting the total end-to-end resistance, R_{TOTAL} = R1 + R2. Choose R_{TOTAL} to yield a total current equivalent to a minimum 100 x I_{SET} (SET's input bias current) at the desired overvoltage threshold.

For example, with an overvoltage threshold set to 1.8V:

R_{TOTAL} < 1.8V/(100 x I_{SET}), where I_{SET} is SET's 50nA input bias current.

$$R_{TOTAL} < 360k\Omega$$

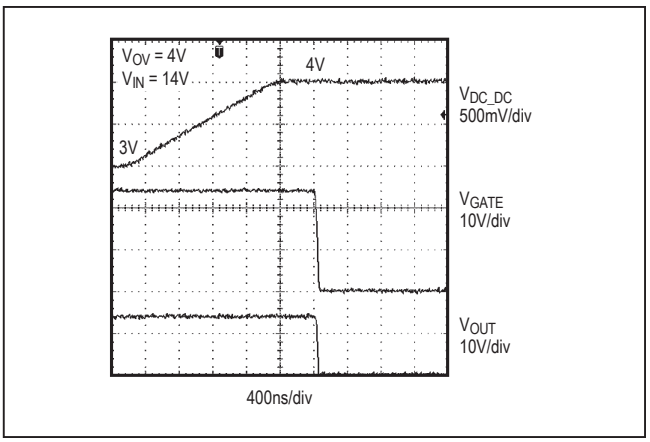


Figure 2. GATE Timing Diagram

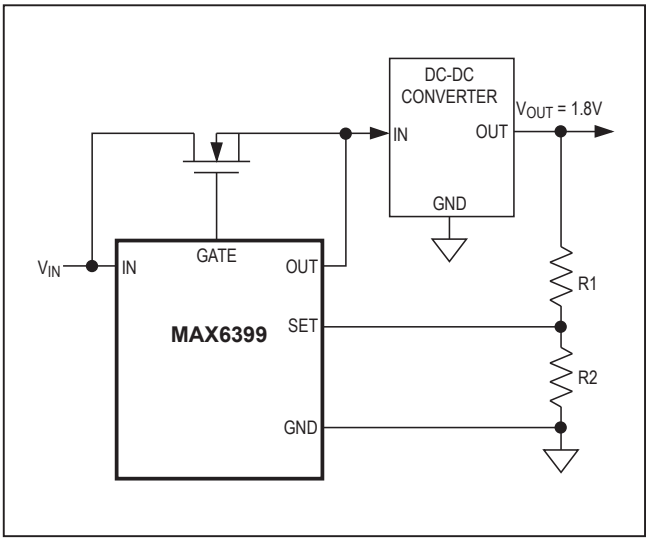


Figure 3. Output Overvoltage Protection Configuration

Use the following formula to calculate R2:

$$R2 = V_{TH} \times \frac{R_{TOTAL}}{V_{OV}}$$

where V_{TH} is the 0.5V SET rising threshold and V_{OV} is the overvoltage condition at the output of a DC-DC converter, R2 = 100kΩ, R_{TOTAL} = R2 + R1, where R1 = 260kΩ. Use a 261kΩ standard resistor.

Using a lower value for total resistance dissipates more power but provides slightly better accuracy.

Monitoring for DC-DC Input Undervoltage Conditions

The MAX6399 can be used to monitor for an undervoltage condition at the input of a DC-DC converter or another system voltage by connecting an external resistor-divider at OUT_SET (Figure 4). Use the following formula to calculate the undervoltage threshold (V_{UV}).

Begin by selecting the total end-to-end resistance, R_{TOTAL} = R1 + R2. Choose R_{TOTAL} to yield a total current equivalent to a minimum 100 x I_{SET} (SET's input bias current) at the desired overvoltage threshold.

For example, with an undervoltage threshold set to 9V:

R_{TOTAL} < 9V/(100 x I_{SET}), where I_{SET} is SET's 50nA input bias current.

$$R_{TOTAL} < 1.8M\Omega$$

Use the following formula to calculate R2:

$$R2 = V_{TH(OUT\_SET)} \times \frac{R_{TOTAL}}{V_{OV}}$$

where $V_{TH(OUT\_SET)}$ is the 1.23V OUT_SET rising threshold and V_{UV} is the undervoltage condition at the input of a DC-DC converter.

R2 = 246kΩ, R_{TOTAL} = R2 + R1, where R1 = 1.554MΩ. Use a 1.54MΩ standard resistor.

Using a lower value for total resistance dissipates more power but provides slightly better accuracy.

Power-OK (POK) Output

POK is an open-drain output that goes low when OUT_SET falls below its 1.23V (typ) threshold voltage. Connect a pullup resistor from POK to a supply voltage. POK asserts high when OUT_SET ramps above 1.23V typical threshold. POK provides a valid output level down to V_{IN} = 1.5V.

Applications Information

Inrush/Slew-Rate Control

Inrush current control can be implemented by placing a capacitor at GATE (Figure 5) to slowly ramp up the GATE, thus limiting the inrush current and controlling GATE's slew rate during initial turn-on. The inrush current can be approximated using the following formula:

$$I_{INRUSH} = \frac{C_{OUT}}{C_{GATE}} \times I_{GATE} + I_{LOAD}$$

where I_{GATE} is GATE's 100µA sourcing current, I_{LOAD} is the load current at the DC-DC output at startup and COUT is the ouput's capacitor. However, most DC-DC converters have soft-start (or peak current limiting) functions that control inrush current.

Input Overvoltage Protection

The MAX6399 also allows overvoltage protection at the input supply (see Figure 6). When the programmed overvoltage threshold is tripped, the internal fast comparator turns off the external MOSFET, latching GATE and OUT low within t_{OV} disconnecting the power source from the load. To unlatch the MAX6399 after an overvoltage fault, recycle IN or toggle $\overline{SHDN}$.

Input Transients Clamping

During hot plug-in/unplug, stray inductance in the power path may cause voltage ringing above the normal input DC value, which may exceed the MAX6399's 80V maximum supply rating. An input transient such as that caused by lightning can also put a severe transient peak voltage on the input rail. The following techniques are recommended to reduce the effect of transients:

- Minimize stray inductance in the power path using wide traces, and minimize loop area including the power traces and the return ground path.
- Add a zener diode or transient voltage suppressor (TVS) rated below the IN absolute maximum rating (Figure 7).
- Add a resistor in series with IN to limit transient current going into the input.

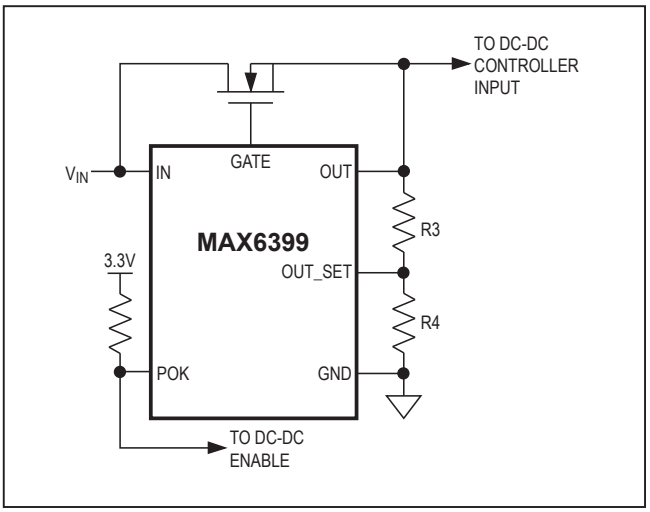


Figure 4. Setting the Undervoltage Threshold

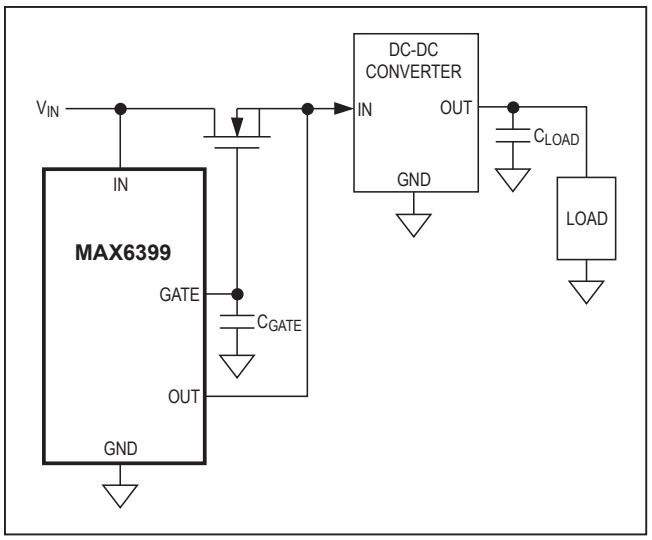


Figure 5. The MAX6399 Controlling GATE Inrush Current

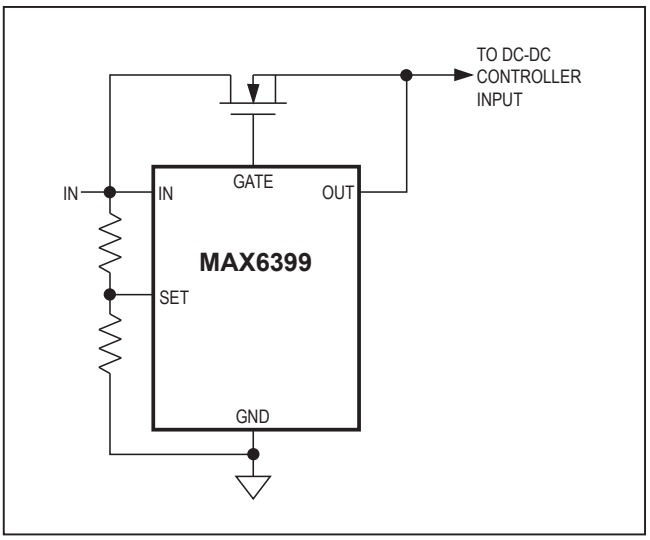


Figure 6. Input Overvoltage Protection Configuration

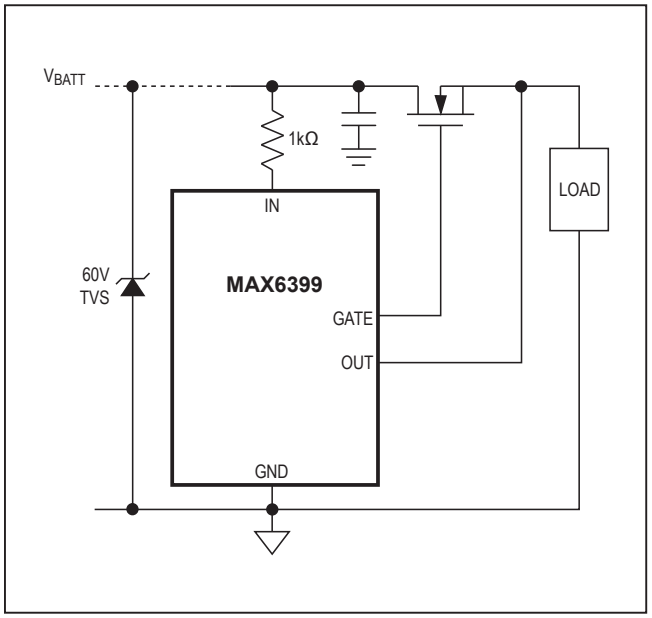


Figure 7. Protecting the MAX6399 Input from High-Voltage Transients

Reverse Voltage Protection

Use a diode or p-channel MOSFET to protect the MAX6399 during a reverse voltage insertion (Figures 8a, 8b). Low p-channel MOSFET on-resistance of 30mΩ or less yields a forward-voltage drop of only a few millivolts (versus hundreds of millivolts for a diode, Figure 8a) thus improving efficiency in battery-operated devices.

Connecting a positive battery voltage to the drain of Q1 (Figure 8b) produces forward bias in its body diode, which clamps the source voltage one diode drop below the drain voltage. When the source voltage exceeds Q1's threshold voltage, Q1 turns on. Once the FET is on, the battery is fully connected to the system and can deliver power to the device and the load.

An incorrectly inserted battery reverse-biases the FET's body diode. The gate remains at the ground potential. The FET remains off and disconnects the reversed battery from the system. The zener diode and resistor combination prevent damage to the p-channel MOSFET during an overvoltage condition.

Thermal Shutdown

The MAX6399 thermal-shutdown feature monitors the PC board temperature of the external MOSFET when the devices sit on the same thermal island. Good thermal contact between the MAX6399 and the external n-channel MOSFET is essential for the thermal-shutdown feature to effectively operate. Place the n-channel MOSFET as close as possible to OUT.

When the MAX6399 junction temperature exceeds T_J = +150°C, the thermal sensor signals the shutdown logic, turning off the GATE output, allowing the device to cool. The thermal sensor turns GATE on after the IC's junction temperature cools by 20°C. For continuous operation, do not exceed the absolute maximum junctiontemperature rating of T_J = +160°C.

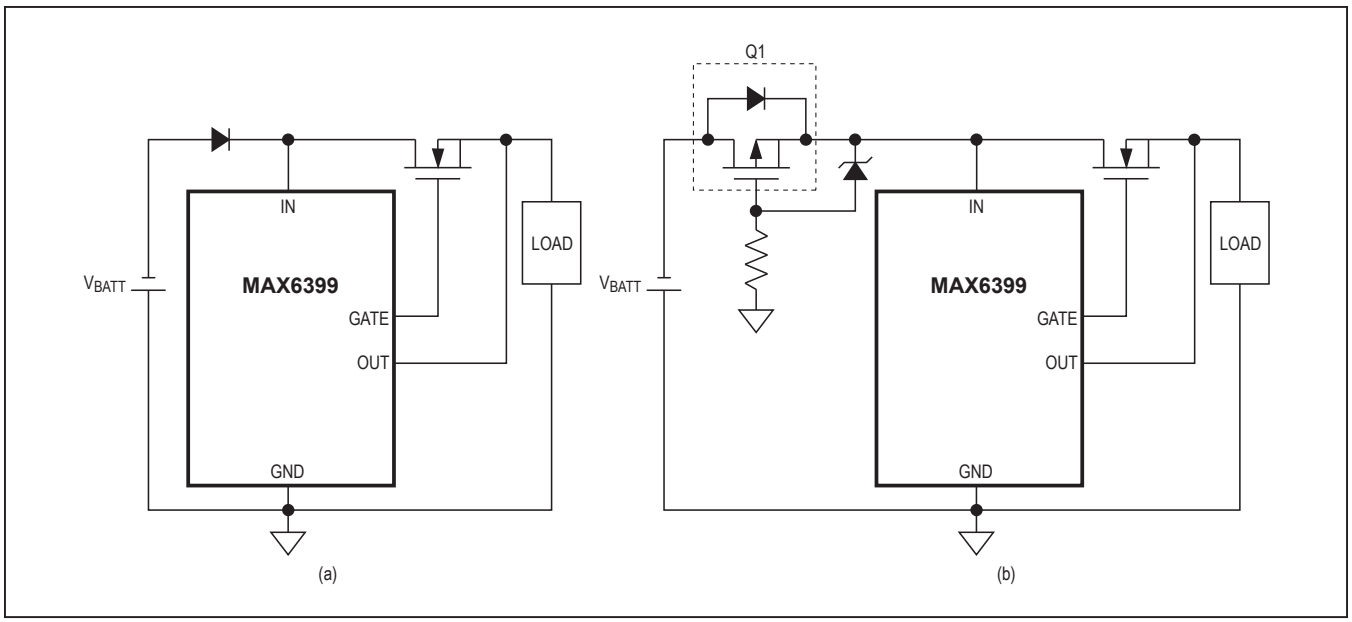


Figure 8. Reverse Voltage Protection Using a Diode or p-Channel MOSFET

MOSFET Selection

Select external MOSFETs according to the application current level. The MOSFETs on-resistance ($R_{DS(ON)}$) should be chosen low enough to have minimum voltage drop at full load to limit the MOSFET power dissipation.

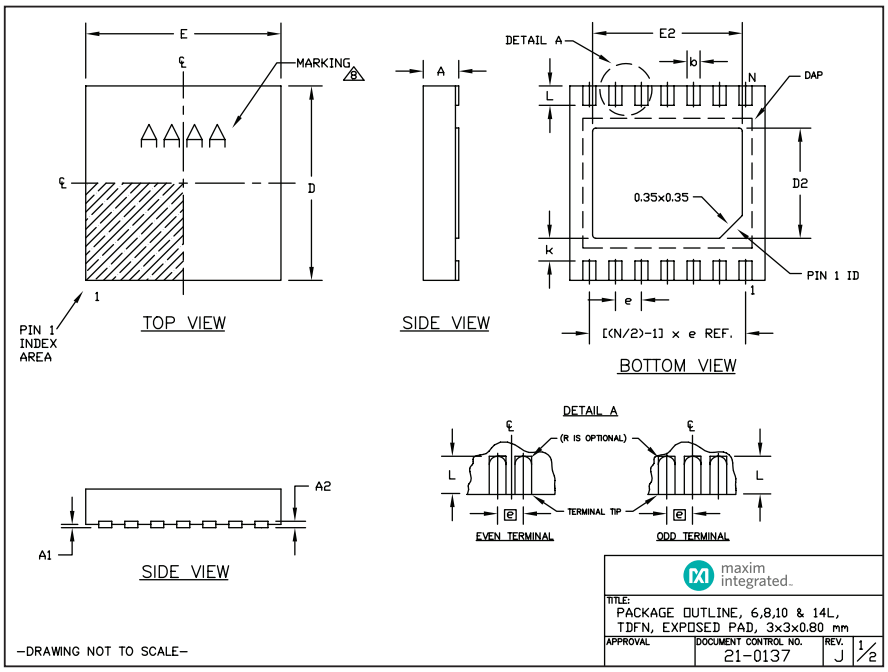
Chip Information

TRANSISTOR COUNT: 590

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.analog.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033MK-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF
T1433-3F	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

maxim integrated.
TITLE:
PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO.
21-0137
REV.
J
2/2

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	4/15	Updated *Benefits and Features* section	1
3	10/24	Updated *Benefits and Features* section	1