0.62Ω R_{ON}, ±15V, +12V, ±5V, +5V/–12V, 4:1 Multiplexer

FEATURES

- Low R_{ON} 0.62Ω
- High continuous current of up to 847mA
- Flat R_{ON} across signal range, 0.003Ω
- THD of −99dB at 1kHz
- 1.8V, 3.3V, and 5V logic compatibility
- 16-lead, 4 mm × 4 mm LFCSP
  - Pin to pin compatible with the ADG1404
- Fully specified at ±15V, +12V, ±5V and +5V /−12V
- Operational with asymmetric power supplies
- V_{SS} to V_{DD} − 2V analog signal range

APPLICATIONS

- Automatic test equipment
- Data acquisition
- Instrumentation
- Avionics
- Audio and video switching
- Communication systems
- Relay replacement

GENERAL DESCRIPTION

The ADG2404 is an analog 4:1 multiplexer. The ADG2404 switches one of four inputs to a common output, D, as determined by the 3-bit binary address line, A0, A1, and EN. For use in multiplexer applications, switches exhibit break-before-make switching action.

Each channel conducts equally well in both directions when on, and each switch has an input signal range that extends from V_{SS} to V_{DD} − 2 V. When switches are disabled, signal levels up to the supplies are blocked.

The digital inputs are compatible with 5V, 3.3V, and 1.8V logic inputs without the requirement for a separate digital logic supply pin.

The on-resistance profile is exceptionally flat over the full-analog input range, which ensures good linearity and low distortion when switching audio signals.

FUNCTIONAL BLOCK DIAGRAM

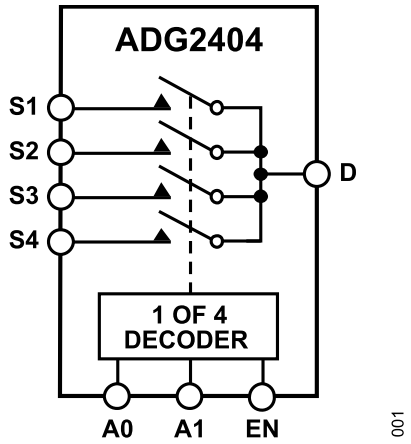

Figure 1. Functional Block Diagram

PRODUCT HIGHLIGHTS

1. Low R_{ON} of 0.62Ω.
2. High continuous current carrying capability, see Table 5.
3. Dual-supply operation. For applications where the analog signal is bipolar, the ADG2404 can be operated from dual supplies up to ±16.5V.
4. Single-supply operation. For applications where the analog signal is unipolar, the ADG2404 can be operated from a single rail power supply up to 16.5V.
5. 1.8V logic-compatible digital inputs: V_{INH} = 1.3V, V_{INL} = 0.8V.
6. No V_L logic power supply required.

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REVISION HISTORY

4/2025—Revision 0: Initial Version

SPECIFICATIONS

OPERATING SUPPLY VOLTAGES

Table 1. Operating Supply Voltages

Supply Voltage	Min	Max	Unit
Dual Supply	±4.5	±16.5	V
Single Supply	+5	+16.5	V

±15V DUAL SUPPLY

V_{DD} = +15V ± 10%, V_{SS} = −15V ± 10%, GND = 0V, unless otherwise noted.

Table 2. ±15V Dual-Supply Specifications

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +13.5V, V_{SS} = −13.5V
Analog Signal Range			V_{DD} − 2 V to V_{SS}	V	
On Resistance, R_{ON}	0.62			Ω typ	Source voltage (V_S) = −13.5V to +10V, source current (I_S) = −10mA, see Figure 37
	0.7	0.87	1.02	Ω max	
	0.65			Ω typ	V_S = −13.5V to +11V, I_S = −100mA
	0.75	0.92	1.07	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.12			Ω typ	V_S = −13.5V to +11V, I_S = −100mA
	0.26	0.29	0.31	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	0.003			Ω typ	V_S = −13.5V to +10V, I_S = −100mA
	0.035	0.035	0.035	Ω max	
	0.04			Ω typ	V_S = −13.5V to +11V, I_S = −100mA
	0.08	0.1	0.1	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5V, V_{SS} = −16.5V
Source Off Leakage, I_S (Off)	±1.7			nA typ	V_S = +10V/−10V, drain voltage (V_D) = −10V/+10V, see Figure 40
	±4	+43.5/−5.5	+248/−5.5	nA max	
Drain Off Leakage, I_D (Off)	±5.1			nA typ	V_S = +10V/−10V, drain voltage (V_D) = −10V/+10V, see Figure 40
	±16	+174/−11	+992/−11	nA max	
Channel On Leakage, I_D (On), I_S (On)	±3.7			nA typ	V_S = V_D = ±10V, see Figure 36
	±13.3	+136/−8.5	+794/−8.5	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			1.3	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL}, or I_{INH}	0.01			μA typ	Input voltage (V_{IN}) = GND voltage (V_{GND}) or V_{DD}
			±0.15	μA max	
Digital Input Capacitance, C_{IN}	4.6			pF typ	
DYNAMIC CHARACTERISTICS					
Transition Time, $t_{TRANSITION}$	319			ns typ	Load resistance (R_L) = 300Ω, load capacitance (C_L) = 35 pF
	378	413	451	ns max	V_S = 10V, see Figure 46
On Time, t_{ON}	310			ns typ	Load resistance (R_L) = 300Ω, load capacitance (C_L) = 35pF
	362	400	437	ns max	V_S = 10V, see Figure 45
Off Time, t_{OFF}	249			ns typ	R_L = 300Ω, C_L = 35pF
	291	292	295	ns max	V_S = 10V, see Figure 45

SPECIFICATIONS

Table 2. ±15V Dual-Supply Specifications (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Break-Before-Make Time Delay, t_D	206			ns typ	R_L = 300Ω, C_L = 35pF
	164	198	232	ns min	V_S = 10V, see Figure 44
Charge Injection, Q_{INJ}	−1.78			nC typ	V_S = 0V, R_S = 0Ω, C_L = 1nF, see Figure 47
Off Isolation	−76			dB typ	R_L = 50Ω, C_L = 5pF, frequency = 100kHz, see Figure 39
Channel-to-Channel Crosstalk	−82			dB typ	R_L = 50Ω, C_L = 5pF, frequency = 100kHz, see Figure 38
Total Harmonic Distortion + Noise, THD + N	0.022			% typ	R_L = 1kΩ, 20V p-p, frequency = 20Hz to 20kHz, see Figure 42
Total Harmonic Distortion, THD	−99			dB typ	R_L = 1kΩ, 20V p-p, frequency = 1kHz
	−73			dB typ	R_L = 1kΩ, 20V p-p, frequency = 20kHz
	−59			dB typ	R_L = 1kΩ, 20V p-p, frequency = 100kHz
−3dB Bandwidth	34			MHz typ	R_L = 50Ω, C_L = 5pF, signal = 0dBm, see Figure 43
Insertion Loss	−0.12			dB typ	R_L = 50Ω, C_L = 5pF, frequency = 1MHz. see Figure 43
Source Off Capacitance, C_S (Off)	76			pF typ	V_S = 0V, frequency = 1MHz
Drain Off Capacitance, C_D (Off)	306			pF typ	V_S = 0V, frequency = 1MHz
Drain On Capacitance, C_D (On), Source On Capacitance C_S (On)	259			pF typ	V_S = 0V, frequency = 1MHz
Match On Capacitance, C_{MATCH}(On)	0.65			pF typ	V_S = 0V, frequency = 1MHz
POWER REQUIREMENTS					V_{DD} = +16.5V, V_{SS} = −16.5V
Power Supply Current, I_{DD}	170			µA typ	Digital inputs = 0V or 5V
	260		260	µA max	
	225			µA typ	Digital inputs = 1.3V
	330		330	µA max	
Negative Supply Current, I_{SS}	85			µA typ	Digital inputs = 0V or 5V
	140		140	µA max	

12V SINGLE SUPPLY

V_{DD} = 12V ± 10%, V_{SS} = 0V, GND = 0V, unless otherwise noted.

Table 3. 12V Single-Supply Specifications

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 10.8V, V_{SS} = 0V
Analog Signal Range			0 V to V_{DD} − 2 V	V	
On Resistance, R_{ON}	0.62			Ω typ	Source voltage (V_S) = 0V to 7.3V, source current (I_S) = −100mA, see Figure 37
	0.7	0.87	1.02	Ω max	
	0.65			Ω typ	V_S = 0V to 8.3V, I_S = −100mA
	0.75	0.92	1.07	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.12			Ω typ	V_S = 0V to 8.3V, I_S = −100mA
	0.26	0.29	0.31	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.003			Ω typ	V_S = 0V to 7.3V, I_S = −100mA
	0.035	0.035	0.035	Ω max	
	0.04			Ω typ	V_S = 0V to 8.3V, I_S = −100mA
	0.08	0.1	0.1	Ω max	

SPECIFICATIONS

Table 3. 12V Single-Supply Specifications (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
LEAKAGE CURRENTS					V_{DD} = 13.2V, V_{SS} = 0V
Source Off Leakage, I_S (Off)	±1.7			nA typ	V_S = 1V/10V, drain voltage (V_D) = 10V/1V, see Figure 40
	±4	+43.5/−5.5	+248/−5.5	nA max	
Drain Off Leakage, I_D (Off)	±5.1			nA typ	V_S = 1V/10V, V_D = 10V/1V, see Figure 40
	±16	+174/−11	+992/−11	nA max	
Channel On Leakage, I_D (On), I_S (On)	±3.7			nA typ	V_S = V_D = 1V/10V, see Figure 36
	±13.3	+136/−8.5	+794/−8.5	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			1.3	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL}, or I_{INH}	0.01			μA typ	Input voltage (V_{IN}) = GND voltage (V_{GND}) or V_{DD}
			±0.15	μA max	
Digital Input Capacitance, C_{IN}	4.6			pF typ	
DYNAMIC CHARACTERISTICS					
Transition Time, $t_{TRANSITON}$	416			ns typ	Load resistance (R_L) = 300Ω, load capacitance (C_L) = 35pF
	496	526	555	ns max	V_S = 8 V, see Figure 46
On Time, t_{ON}	191			ns typ	Load resistance (R_L) = 300Ω, load capacitance (C_L) = 35pF
	222	236	251	ns max	V_S = 8V, see Figure 45
Off Time, t_{OFF}	530			ns typ	R_L = 300Ω, C_L = 35pF
	623	624	627	ns max	V_S = 8V, see Figure 45
Break-Before-Make Time Delay, t_D	78			ns typ	R_L = 300Ω, C_L = 35pF
	58	62	69	ns min	V_S = 10V, see Figure 44
Charge Injection, Q_{INJ}	−1.04			nC typ	V_S = 6V, R_S = 0 Ω, C_L = 1nF, see Figure 47
Off Isolation	−61			dB typ	R_L = 50Ω, C_L = 5pF, frequency = 100kHz, see Figure 39
Channel-to-Channel Crosstalk	−65			dB typ	R_L = 50Ω, C_L = 5pF, frequency = 100kHz, see Figure 38
Total Harmonic Distortion + Noise, THD + N	0.021			% typ	R_L = 1kΩ, 6V p-p, frequency = 20Hz to 20kHz, see Figure 42
Total Harmonic Distortion, THD	−99			dB typ	R_L = 1kΩ, 6V p-p, frequency = 1kHz
	−73			dB typ	R_L = 1kΩ, 6 Vp-p, frequency = 20kHz
	−60			dB typ	R_L = 1kΩ, 6 Vp-p, frequency = 100kHz
−3dB Bandwidth	28			MHz typ	R_L = 50Ω, C_L = 5pF, signal = 0dBm, see Figure 43
Insertion Loss	−0.17			dB typ	R_L = 50Ω, C_L = 5pF, frequency = 1MHz, see Figure 43
Source Off Capacitance, C_S (Off)	99			pF typ	V_S = 6V, frequency = 1MHz
Drain Off Capacitance, C_D (Off)	390			pF typ	V_S = 6V, frequency = 1MHz
Drain On Capacitance, C_D (On), Source On Capacitance,C_S (On)	332			pF typ	V_S = 6V, frequency = 1MHz
Match On Capacitance, C_{MATCH}(On)	0.73			pF typ	V_S = 6V, frequency = 1MHz

SPECIFICATIONS

Table 3. 12V Single-Supply Specifications (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = 13.2V
Power Supply Current, I_{DD}	170			µA typ	Digital inputs = 0V or 5V
	260		260	µA max	
	225			µA typ	Digital inputs = 1.3V
	330		330	µA max	
Negative Supply Current, I_{SS}	85			µA typ	Digital inputs = 0V or 5V
	140		140	µA max	

SPECIFICATIONS

DUAL AND ASYMMETRIC SUPPLY

V_{DD} = +5V ± 10%, V_{SS} = −5V to −12V ± 10%, GND = 0V, unless otherwise noted.

Table 4. Dual and Asymmetric Supply Specifications

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +4.5V, V_{SS} = −13.2V
Analog Signal Range			V_{DD} − 2V to V_{SS}	V	
On Resistance, R_{ON}	0.62			Ω typ	Source voltage (V_S) = V_{SS} to +1V, source current (I_S) = −100mA, see Figure 37
	0.7	0.87	1.02	Ω max	
	0.65			Ω typ	V_S = V_{SS} to +2V, I_S = −100mA
	0.75	0.92	1.07	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.12			Ω typ	V_S = V_{SS} to +2V, I_S = −100mA
	0.26	0.29	0.31	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	0.003			Ω typ	V_S = V_{SS} to +1V, I_S = −100mA
	0.035	0.035	0.035	Ω max	
	0.04			Ω typ	V_S = V_{SS} to +2V, I_S = −100mA
	0.08	0.1	0.1	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5V, V_{SS} = −13.2V
Source Off Leakage, I_S (Off)	±1.7			nA typ	V_S = +1V/−10V, V_D = −10V/ +1V, see Figure 40
	±4	+43.5/−5.5	+248/−5.5	nA max	
Drain Off Leakage, I_D (Off)	±5.1			nA typ	V_S = +1 V/−10V, V_D = −10V/+1V, see Figure 40
	±16	+174/−11	+992/−11	nA max	
Channel On Leakage, I_D (On), I_S (On)	±3.7			nA typ	V_S = V_D = +3V/−10V, see Figure 36
	±13.3	+136/−8.5	+794/−8.5	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			1.3	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL}, or I_{INH}	0.01			μA typ	Input voltage (V_{IN}) = GND voltage (V_{GND}) or V_{DD}
			±0.15	μA max	
Digital Input Capacitance, C_{IN}	4.6			pF typ	
DYNAMIC CHARACTERISTICS					V_{DD} = +5V, V_{SS} = −12V
Transition Time, $t_{TRANSITION}$	277			ns typ	R_L = 300Ω, C_L = 35pF
	336	366	391	ns max	V_S = 1.5V, seeFigure 46
On Time, t_{ON}	262			ns typ	Load resistance (R_L) = 300Ω, load capacitance (C_L) = 35pF
	304	332	355	ns max	V_S = 1.5V, see Figure 45
Off Time, t_{OFF}	295			ns typ	R_L = 300Ω, C_L = 35pF
	343	355	363	ns max	V_S = 1.5V, see Figure 45
Break-Before-Make Time Delay, t_D	122			ns typ	R_L = 300Ω, C_L = 35pF
	73	101	117	ns min	V_S = 1.5V, see Figure 44
Charge Injection, Q_{INJ}	−0.93			nC typ	V_S = −3V, R_S = 0Ω, C_L = 1nF, see Figure 47
Off Isolation	−70			dB typ	R_L = 50Ω, C_L = 5pF, frequency = 100kHz, see Figure 39
Channel-to-Channel Crosstalk	−76			dB typ	R_L = 50Ω, C_L = 5pF, frequency = 100kHz, see Figure 38

SPECIFICATIONS

Table 4. Dual and Asymmetric Supply Specifications (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Total Harmonic Distortion + Noise, THD + N	0.011			% typ	R_L = 1kΩ, 3V p-p, frequency = 20Hz to 20kHz, see Figure 42
Total Harmonic Distortion, THD	−105			dB typ	R_L = 1kΩ, 3V p-p, frequency = 1kHz
	−79			dB typ	R_L = 1kΩ, 3V p-p, frequency = 20kHz
	−65			dB typ	R_L = 1kΩ, 3V p-p, frequency = 100kHz
−3dB Bandwidth	26			MHz typ	R_L = 50Ω, C_L = 5pF, signal = 0dBm, see Figure 43
Insertion Loss	−0.18			dB typ	R_L = 50Ω, C_L = 5pF, frequency = 1MHz see Figure 43
Source Off Capacitance, C_S (Off)	103			pF typ	V_S = 0V, frequency = 1MHz
Drain Off Capacitance, C_D (Off)	408			pF typ	V_S = 0V, frequency = 1MHz
Drain On Capacitance, C_D (On), Source On Capacitance, C_S (On)	347			pF typ	V_S = 0V, frequency = 1MHz
Match On Capacitance, C_{MATCH}(On)	0.70		pF typ		V_S = 0V, frequency = 1MHz
POWER REQUIREMENTS					V_{DD} = +5.5V, V_{SS} = −13.2V
Power Supply Current, I_{DD}	170			µA typ	Digital inputs = 0V or 5V
	260		260	µA max	
	225			µA typ	Digital inputs = 1.3V
	330		330	µA max	
Negative Supply Current, I_{SS}	85			µA typ	Digital inputs = 0V or 5V
	140		140	µA max	

SPECIFICATIONS

CONTINUOUS CURRENT PER CHANNEL, SX OR DX

Table 5. One Channel On, Per Channel Specifications

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT, Sx OR Dx					
V_{DD} = +15V, V_{SS} = −15V					
LFCSP (θ_{JA} = 44°C/W)	847	325	123	mA maximum	$V_S = V_{SS}$ to V_{DD} − 3.5V
V_{DD} = 12V, V_{SS} = 0V					
LFCSP (θ_{JA} = 44°C/W)	847	325	123	mA maximum	$V_S = V_{SS}$ to V_{DD} − 3.5V
V_{DD} = +5V, V_{SS} = −5V					
LFCSP (θ_{JA} = 44°C/W)	847	325	123	mA maximum	$V_S = V_{SS}$ to V_{DD} − 3.5V
V_{DD} = +5V, V_{SS} = −12V					
LFCSP (θ_{JA} = 44°C/W)	847	325	123	mA maximum	$V_S = V_{SS}$ to V_{DD} − 3.5V

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6. Absolute Maximum Ratings

Parameter	Rating
V_{DD} to V_{SS}	35V
V_{DD} to GND	−0.3V to +25V
V_{SS} to GND	+0.3V to −25V
Analog Inputs[1]	V_{SS} − 0.3V to V_{DD} + 0.3V or 30mA, whichever occurs first
Digital Inputs[1]	GND − 0.3V to +6V or 30mA, whichever occurs first
Peak Current, Sx or Dx Pins[2]	2.6A (pulsed at 1ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx[2]	Data[3] + 15%
Temperature	
Operating Range	−40°C to +125°C
Storage Range	−65°C to +150°C
Junction	150°C
Reflow Soldering Peak, Pb-Free	As per JEDEC J-STD-020

[1] Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.

[2] Sx refers to the S1 to S4 pins, and Dx refers to the D1 to D4 pins.

[3] See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure, and θ_{JCB} is the junction to the bottom of the case value.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JCB}	Unit
CP-16-17[1]	44	17.4	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board without thermal vias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADG2404

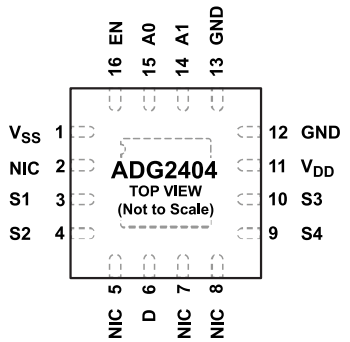
Table 8. ADG2404, 16-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±4000	3A
FICDM	±1250	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED.
2. EXPOSED PAD. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE SUBSTRATE, V_{SS}.

002

Figure 2. Pin Configuration

Table 9. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	V_{SS}	Most Negative Power-Supply Potential. Decouple the V_{SS} pin using a 0.1µF capacitor to GND.
2, 5, 7, 8	NIC	Not Internally Connected.
3	S1	Source Terminal 1. This pin can be an input or output.
4	S2	Source Terminal 2. This pin can be an input or output.
6	D	Drain Terminal. This pin can be an input or output.
9	S4	Source Terminal 4. This pin can be an input or output.
10	S3	Source Terminal 3. This pin can be an input or output.
11	V_{DD}	Most Positive Power-Supply Potential. Decouple the V_{DD} pin using a 0.1µF capacitor to GND.
12, 13	GND	Ground (0V) Reference Supply.
14	A1	Logic Control Input A1.
15	A0	Logic Control Input A0.
16	EN	Active High Digital Input. When this pin is low, the device is disabled, and all switches are off. When this pin is high, the Ax logic inputs determine the on switches.
EP	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

Table 10. ADG2404 Truth Table

EN	A1	A0	S1	S2	S3	S4
0	X[1]	X[1]	Off	Off	Off	Off
1	0	0	On	Off	Off	Off
1	0	1	Off	On	Off	Off
1	1	0	Off	Off	On	Off
1	1	1	Off	Off	Off	On

[1] X = Don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

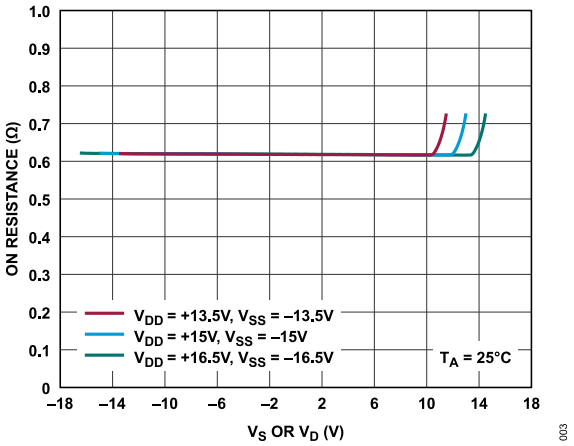


Figure 3. R_{ON} as a Function of V_S, V_D (Dual Supply)

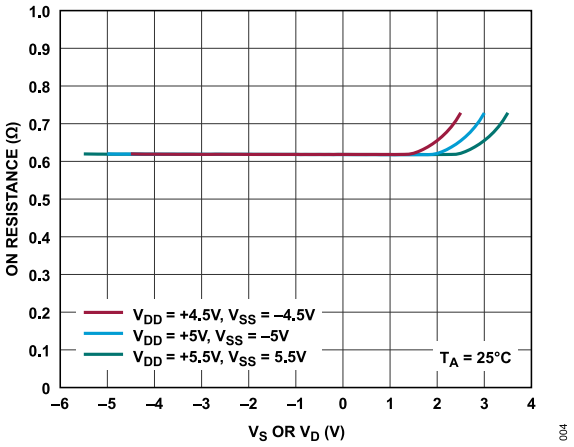


Figure 4. R_{ON} as a Function of V_S, V_D (Dual Supply)

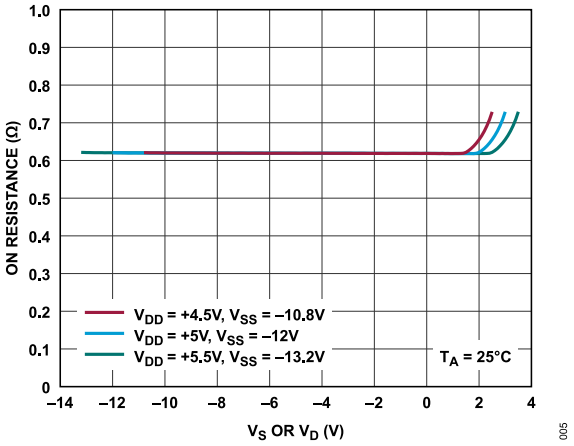


Figure 5. R_{ON} as a Function of V_S, V_D (Dual Supply)

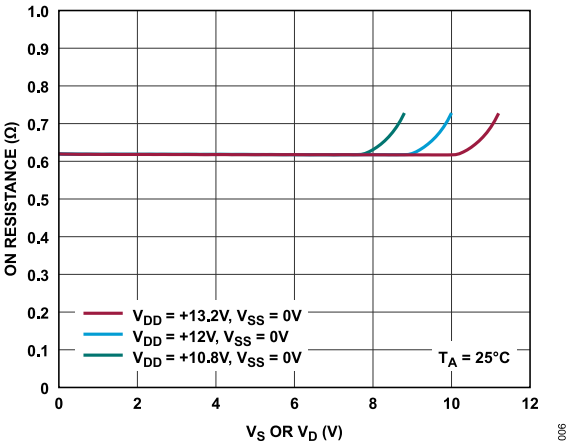


Figure 6. R_{ON} as a Function of V_S, V_D (Single Supply)

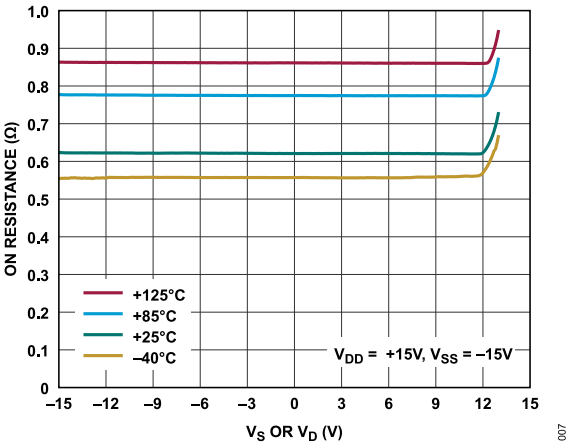


Figure 7. R_{ON} as a Function of V_S (V_D) for Different Temperatures, ±15V Dual Supply

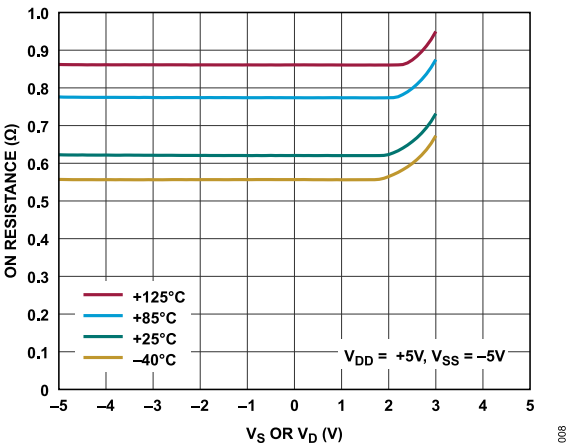


Figure 8. R_{ON} as a Function of V_S (V_D) for Different Temperatures, ±5V Dual Supply

TYPICAL PERFORMANCE CHARACTERISTICS

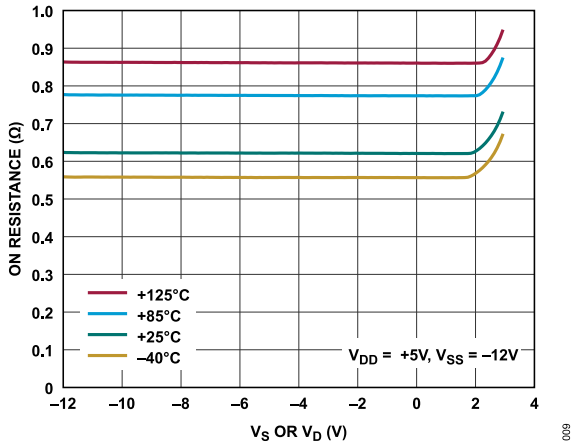


Figure 9. R_{ON} as a Function of V_S (V_D) for Different Temperatures, +5V, −12V Dual Supply

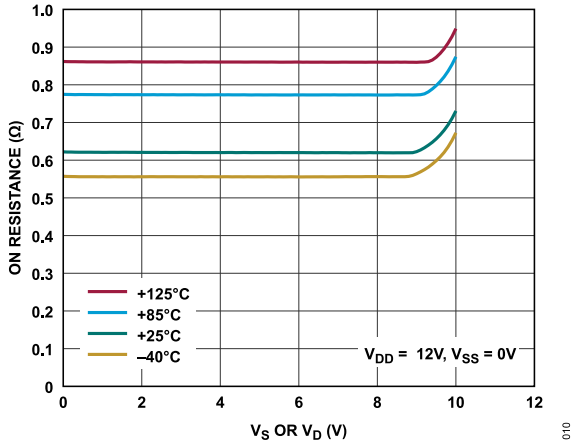


Figure 10. R_{ON} as a Function of V_S (V_D) for Different Temperatures, +12V Single Supply

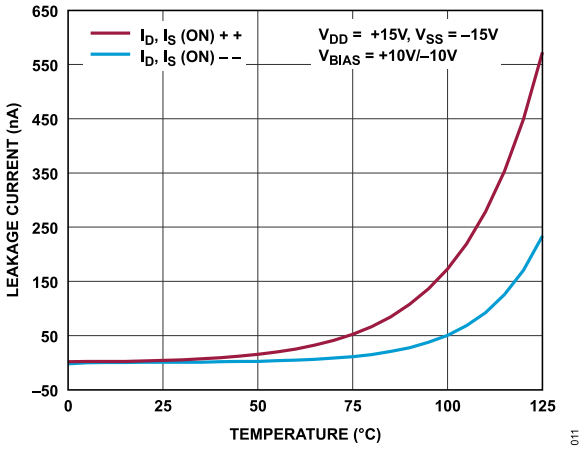


Figure 11. On Leakage Currents vs. Temperature, ±15V Dual Supply

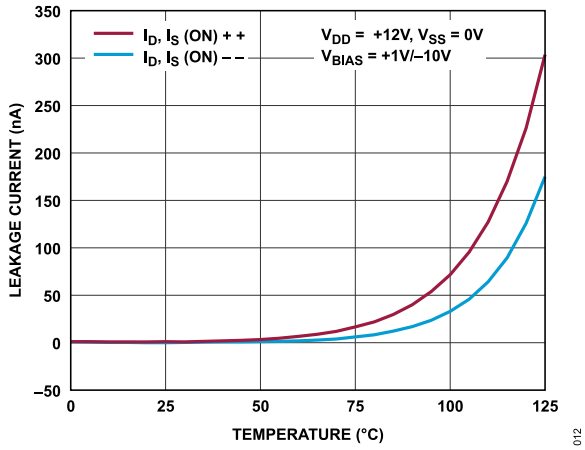


Figure 12. On Leakage Currents vs. Temperature, +12V Single Supply

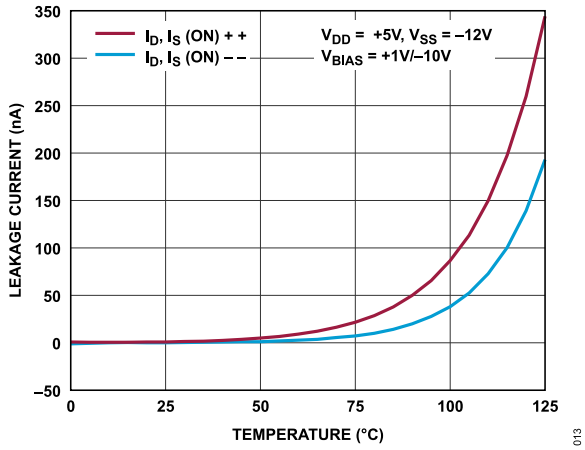


Figure 13. On Leakage Currents vs. Temperature, +5V, −12V Dual Supply

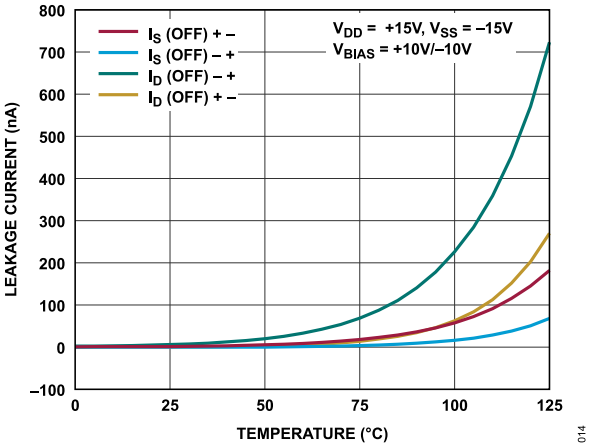


Figure 14. Off Leakage Currents vs. Temperature, ±15V Dual Supply

TYPICAL PERFORMANCE CHARACTERISTICS

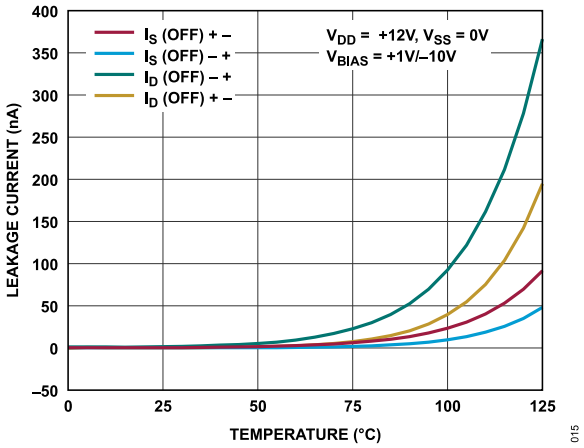


Figure 15. Off Leakage Currents vs. Temperature, +12V Single Supply

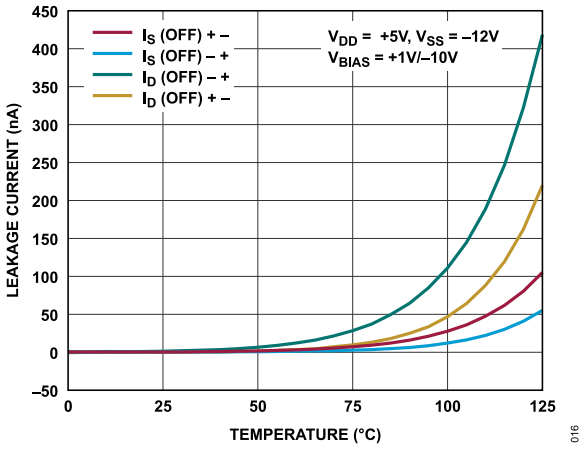


Figure 16. Off Leakage Currents vs. Temperature, +5V, −12V Dual Supply

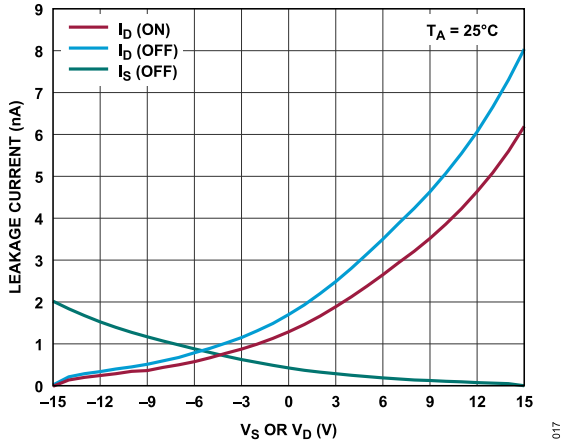


Figure 17. Leakage Currents as a Function of $V_S(V_D)$, 25°C, ±15V Dual Supply

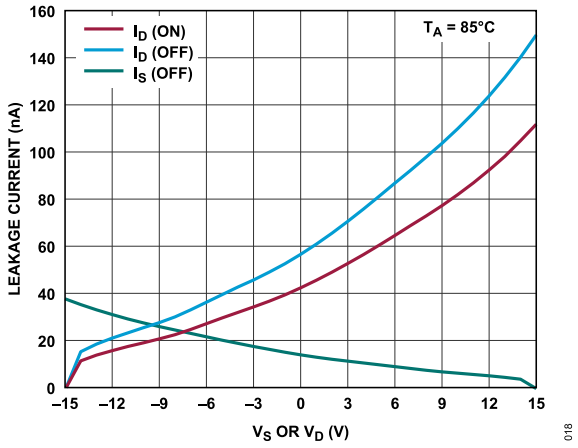


Figure 18. Leakage Currents as a Function of $V_S(V_D)$, 85°C, ±15V Dual Supply

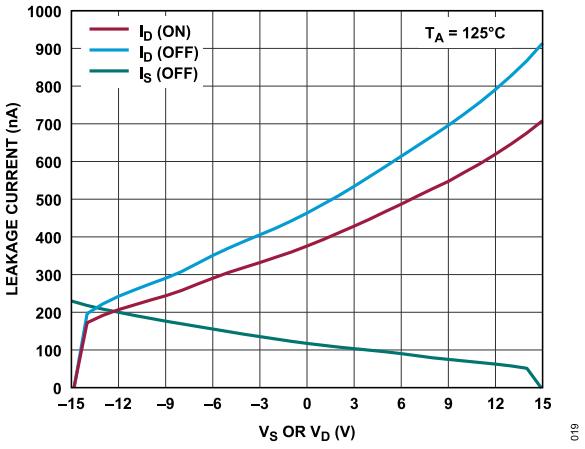


Figure 19. Leakage Currents as a Function of $V_S(V_D)$, 125°C, ±15V Dual Supply

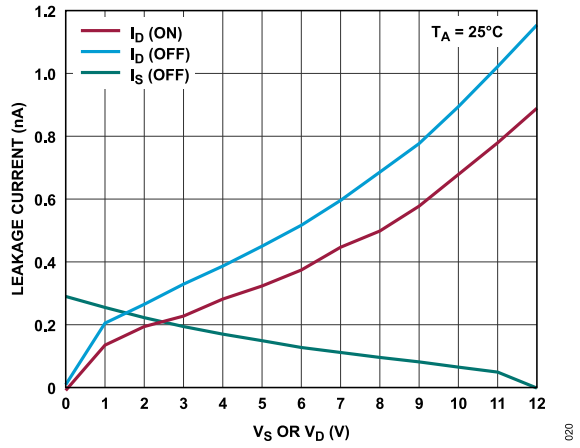


Figure 20. Leakage Currents as a Function of $V_S(V_D)$, 25°C, 12V Single Supply

TYPICAL PERFORMANCE CHARACTERISTICS

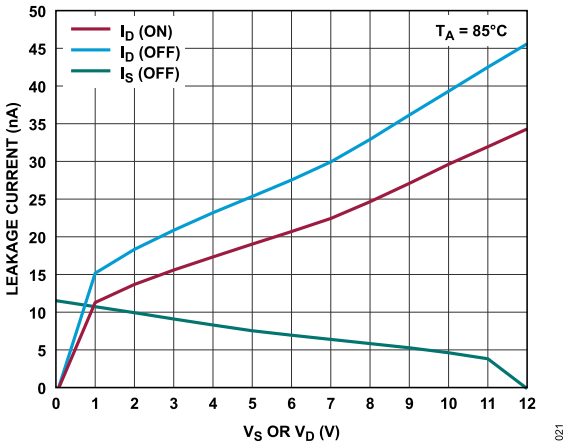


Figure 21. Leakage Currents as a Function of $V_S(V_D)$,85°C, 12V Single Supply

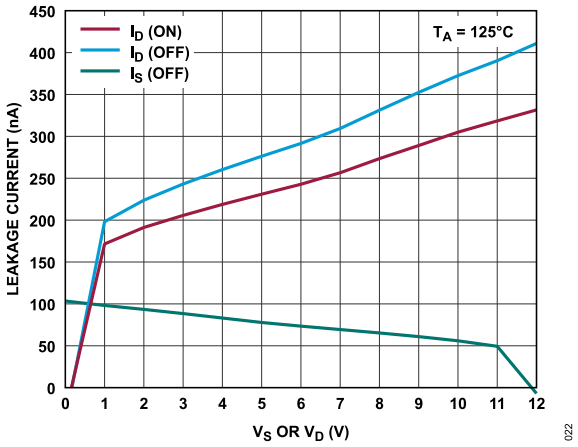


Figure 22. Leakage Currents as a Function of $V_S(V_D)$,125°C, 12V Single Supply

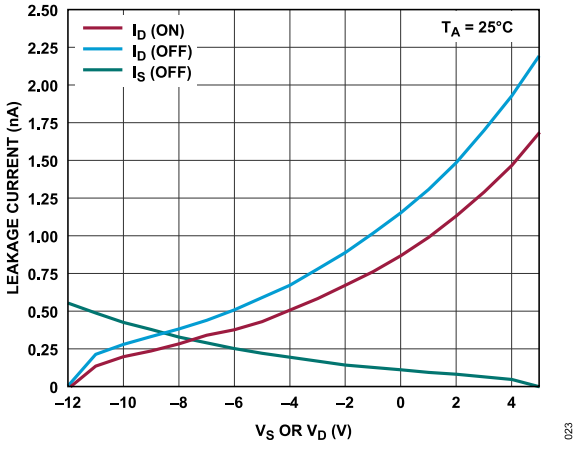


Figure 23. Leakage Currents as a Function of $V_S(V_D)$, 25°C, +5V/−12V Dual Supply

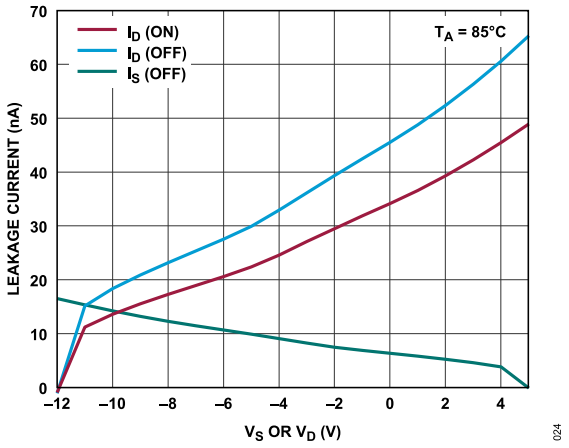


Figure 24. Leakage Currents as a Function of $V_S(V_D)$, 85°C, +5V/−12V Dual Supply

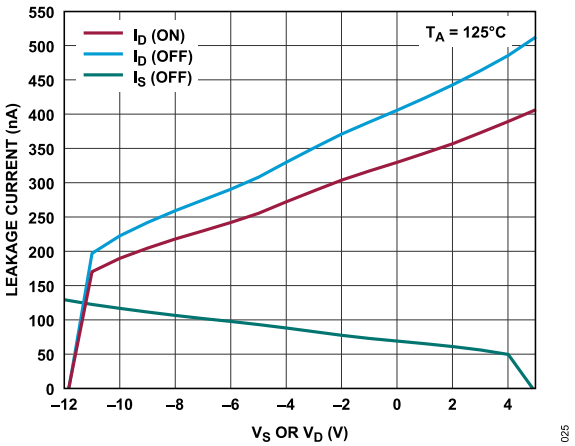


Figure 25. Leakage Currents as a Function of $V_S(V_D)$, 125°C, +5V/−12V Dual Supply

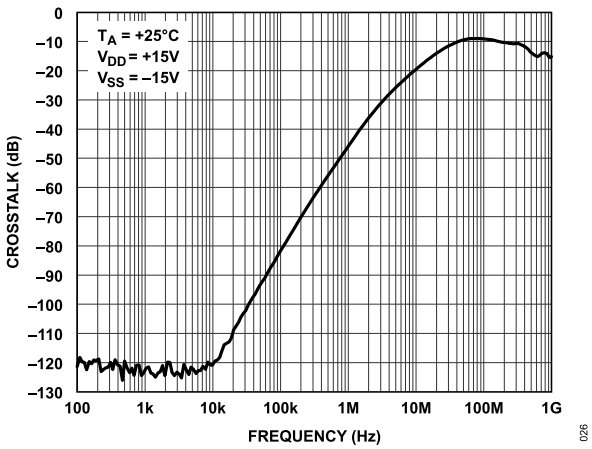


Figure 26. Crosstalk vs. Frequency, ±15V Dual Supply

TYPICAL PERFORMANCE CHARACTERISTICS

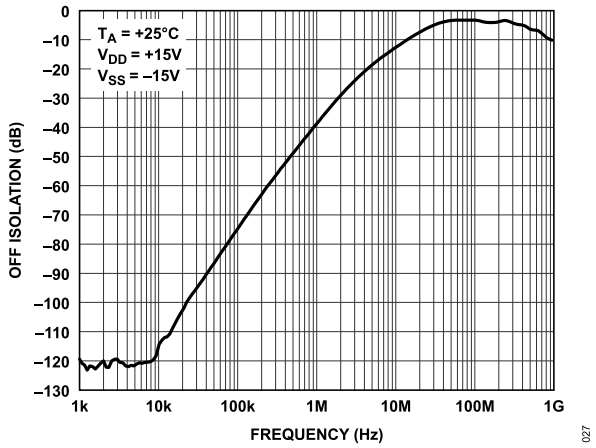


Figure 27. Off Isolation vs. Frequency, ±15V Dual Supply

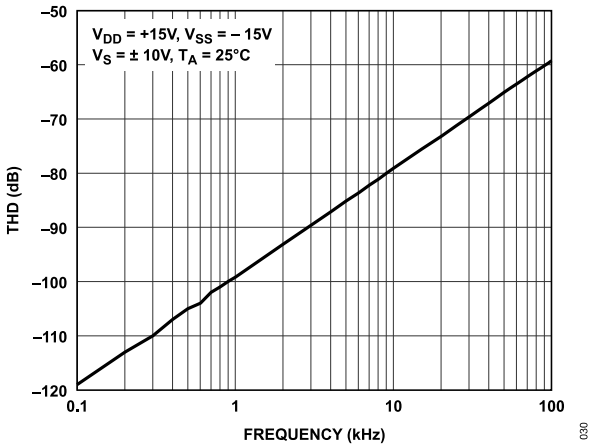


Figure 30. THD vs. Frequency, ±15V Dual Supply

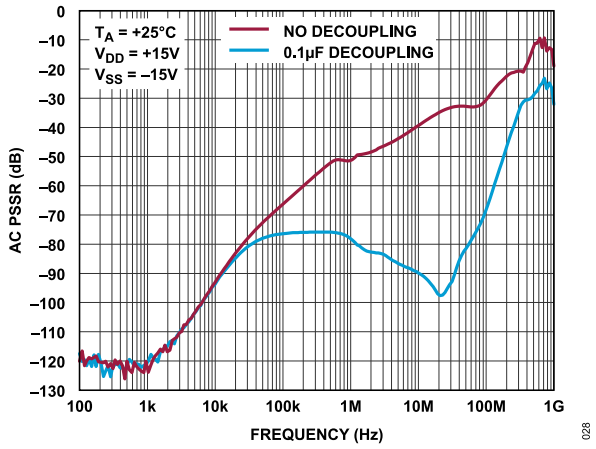


Figure 28. AC PSRR vs. Frequency, ±15V Dual Supply

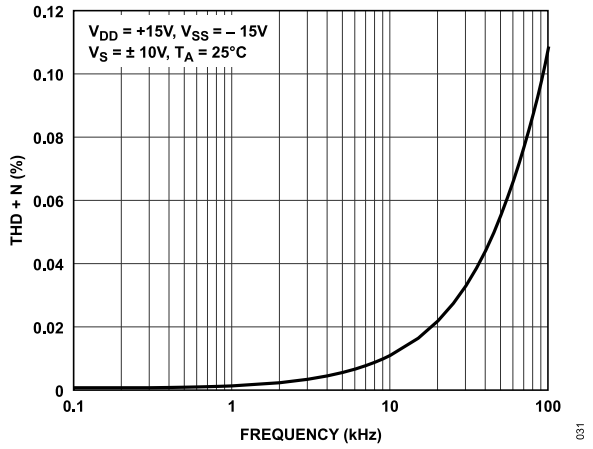


Figure 31. THD + N vs. Frequency, ±15V Dual Supply

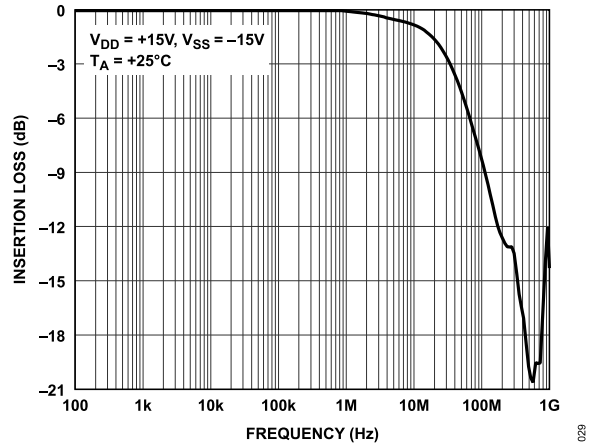


Figure 29. Insertion Loss vs. Frequency, ±15V Dual Supply

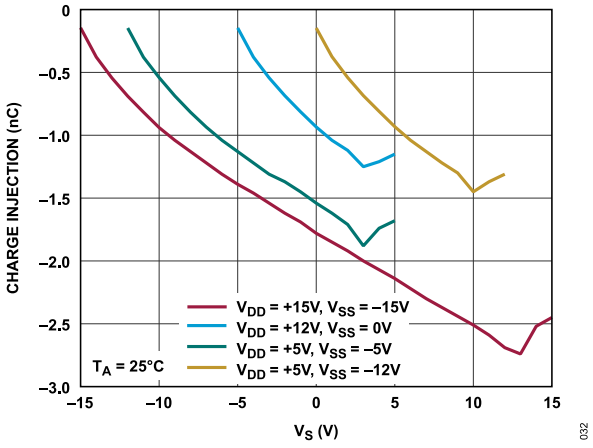


Figure 32. Charge Injection vs. V_S

TYPICAL PERFORMANCE CHARACTERISTICS

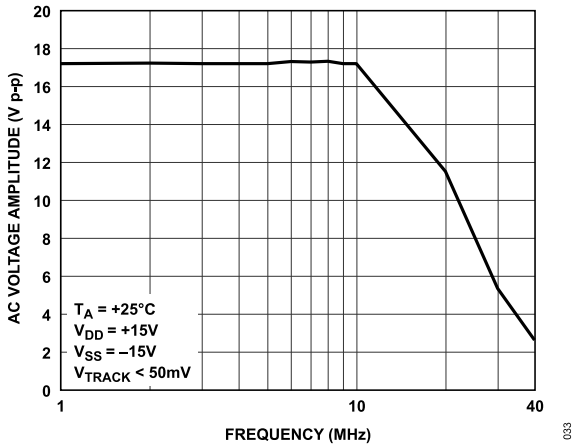


Figure 33. Large AC Signal Voltage vs. Frequency, ±15V Dual Supply

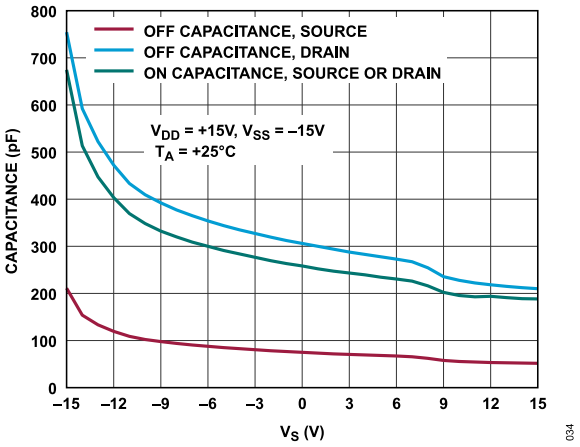


Figure 34. Capacitance vs. V_S, ±15V Dual Supply

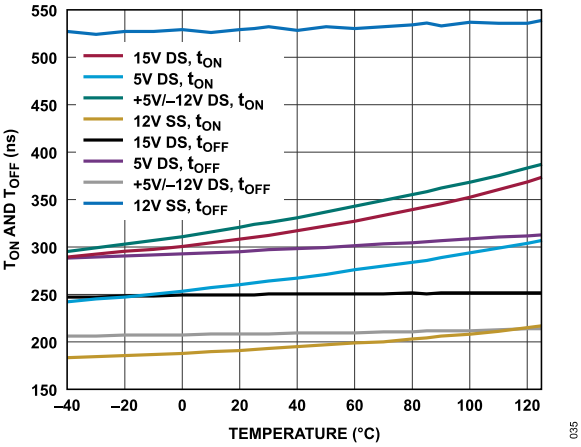


Figure 35. t_{ON}, t_{OFF} Times vs. Temperature

TEST CIRCUITS

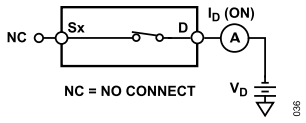


Figure 36. On Leakage

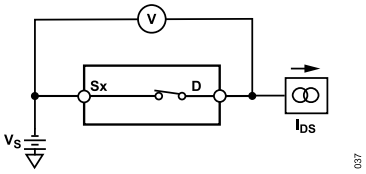


Figure 37. On Resistance

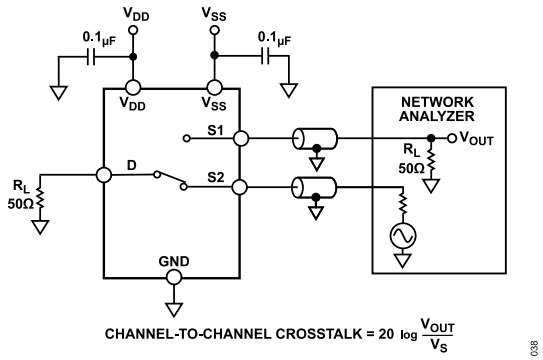


Figure 38. Channel-to-Channel Crosstalk

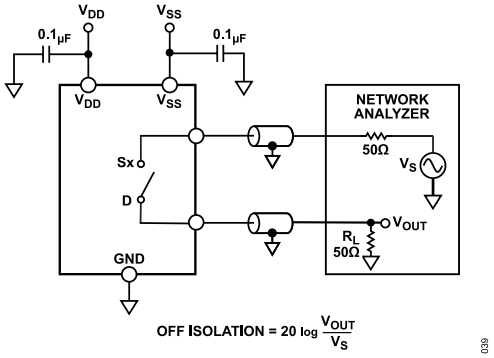


Figure 39. Off Isolation

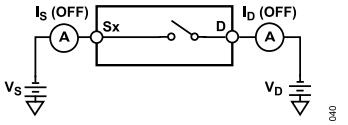


Figure 40. Off Leakage

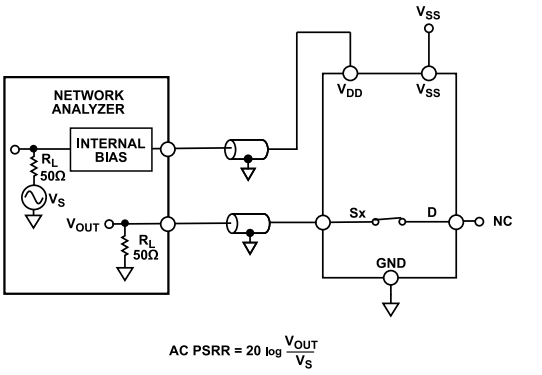


Figure 41. AC PSRR

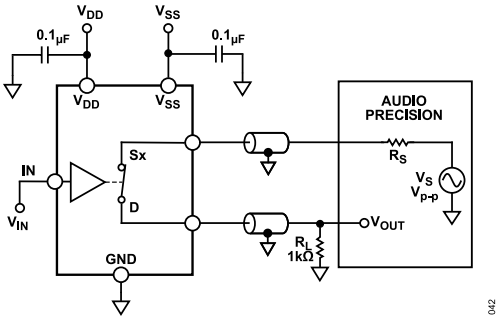


Figure 42. THD + Noise

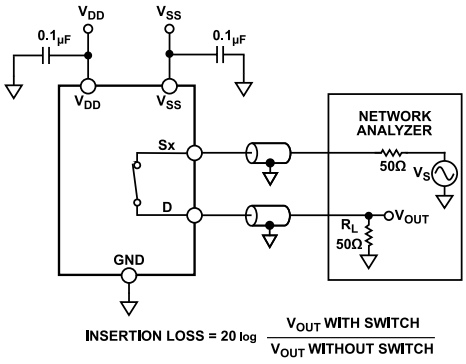


Figure 43. Bandwidth

TEST CIRCUITS

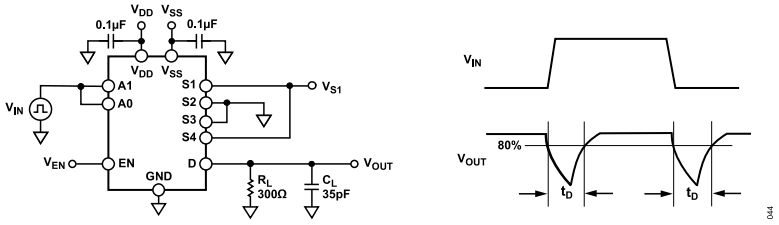


Figure 44. Break-Before-Make Time Delay (t_D)

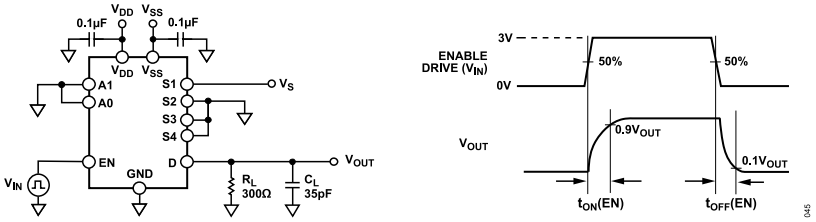


Figure 45. Enable Delay, $t_{ON(EN)}$, $t_{OFF(EN)}$

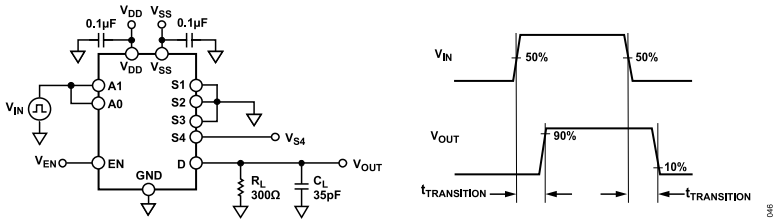


Figure 46. Switching Times

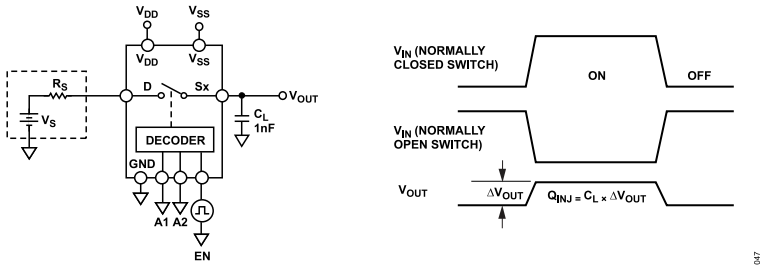


Figure 47. Charge Injection

TERMINOLOGY

I_{DD}

The positive supply current.

I_{SS}

The negative supply current.

V_D and V_S

The analog voltage on Terminal D and Terminal S, respectively.

V_{TRACK}

The difference between V_S and V_D.

R_{ON}

The ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}

The difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$

The difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)

The source leakage current with the switch off.

I_D (Off)

The drain leakage current with the switch off.

I_D (On) and I_S (On)

The channel leakage current with the switch on.

V_{INL}

The maximum input voltage for Logic 0.

V_{INH}

The minimum input voltage for Logic 1.

I_{INL} and I_{INH}

The input current of the digital input when high or when low.

C_S (Off) and C_D (Off)

The off switch source and drain capacitance for the off condition, which is measured with reference to ground.

C_D (On) and C_S (On)

The on switch drain and source capacitance for the on condition, which is measured with reference to ground.

C_{IN}

The digital input capacitance.

$t_{Transition}$

The delay time between the 50% and 90% points of the digital input and switch on condition when switching from one address to another.

t_{ON}

The delay between applying the digital control input and the output switching on.

t_{OFF}

The delay between applying the digital control input and the output switching off.

t_D

The off-time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Channel-to-Channel Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (AC PSRR)

The ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The DC voltage on the device is modulated by a sine wave of 0.62 V p-p.

THEORY OF OPERATIONS

SWITCH ARCHITECTURE

The ADG2404 contains four independent SPST, N-channel diffused metal-oxide semiconductor (NDMOS) switches, which allows for an excellent R_{ON} performance. Using an NDMOS only architecture results in a reduction of signal headroom, meaning signals are limited to V_{DD} – 2 V. To achieve the lowest on resistance, on-resistance flatness, and total harmonic distortion, it is recommended the signal stays less than V_{DD} – 3.5 V.

To guarantee correct operation of the ADG2404, a minimum of 0.1 µF decoupling capacitors are required on both the V_{DD} and V_{SS} supply pins.

The ADG2404 is compatible with single-supply systems that have a V_{DD} of up to 16.5 V, dual-supply systems of up to ±16.5 V, as well as asymmetric power supplies.

1.8 V LOGIC COMPATIBILITY

For ease of use, the ADG2404 does not have a V_L logic reference voltage. The digital inputs are compatible with 1.8 V logic levels over the full-operating supply range. The limits for 1.8 V logic are: V_{INH} = 1.3 V, V_{INL} = 0.8 V. 1.8 V logic-level inputs enable the ADG2404 to be compatible with processors that have lower supply rails, eliminating the need for an external translator.

If full 1.8 V and 1.2 V JEDEC compliance is required, refer to the Analog Devices, Inc., L range part numbers, such as the ADG1412L.

APPLICATIONS INFORMATION

LARGE VOLTAGE, HIGH FREQUENCY SIGNAL TRACKING

Figure 33 shows the voltage range and corresponding frequencies that the ADG2404 can reliably convey. The tracking voltage (V_{TRACK}) in the figure shows the source voltage and the drain voltage difference, which is less than 50mV for a given amplitude and frequency. For large voltage, high frequency signals, the frequency must be kept below 10MHz. If the required frequency is greater than 10MHz, decrease the signal range appropriately to ensure signal integrity.

POWER SUPPLY RECOMMENDATIONS

Analog Devices has a wide range of power management products to meet the requirements of high performance signal chains.

An example of a bipolar solution is shown in Figure 48. The LT3463 (a dual switching regulator), generates a positive and negative supply rail for the ADG2404, an amplifier, and/or a precision converter in a typical signal chain. Also, two optional low-dropout regulators (LDOs), the ADP7142 and the ADP7182 (positive and negative LDOs, respectively) are shown in Figure 48, which can reduce the output ripple of the LT3463 in ultra-low noise sensitive applications.

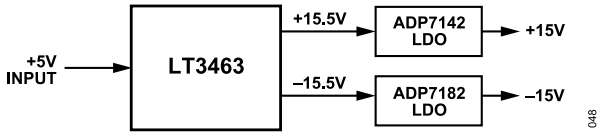


Figure 48. Bipolar Power Solution

Table 11. Recommended Power Management Devices

Product	Description
LT3463	Dual micropower, DC to DC converter with Schottky diodes
ADP7142	40V, 200mA, low noise, CMOS, LDO linear regulator
ADP7182	−28V, −200mA, low noise, LDO linear regulator

DIGITAL AUDIO CHANNEL TO ULTRA-LOW THD

Figure 49 shows an example application for the ADG2404. For precision audio signal chains, THD is a key specification. The THD performance of a switch is related to the on-resistance flatness, and the ADG2404 has exceptionally low on-resistance flatness of approximately 3mΩ. Here, the ADG2404 is set up as a gain selection switch for an audio preamplifier to allow flexibility for the user to select multiple gain ranges. The THD performance of the ADG2404 maximizes the signal fidelity, and the low on-resistance minimizes any gain error in the system.

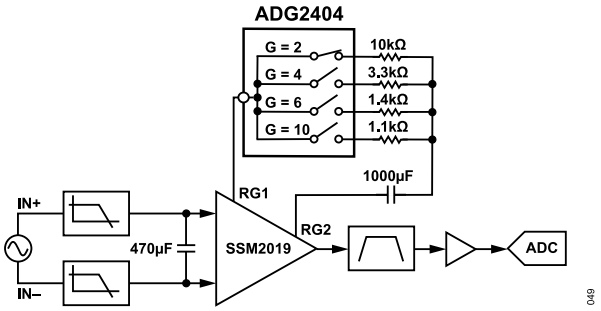


Figure 49. Digital Audio Channel to Ultra-Low THD Application

OUTLINE DIMENSIONS

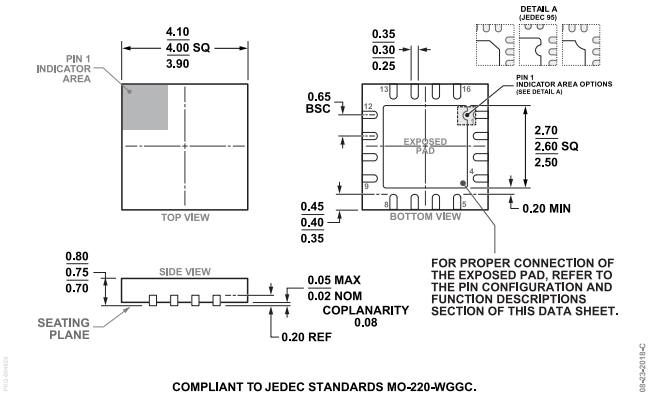


Figure 50. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADG2404BCPZ-REEL7	−40°C to +125°C	16-Lead LFCSP (4mm × 4mm)	Reel, 1500	CP-16-17

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 12. Evaluation Boards

Model[1]	Description
EVAL-ADG2404EBZ	Evaluation Board

[1] Z = RoHS-Compliant Part.