

# OPA177 0.1- $\mu\text{V}/^\circ\text{C}$ Offset Drift, 10- $\mu\text{V}$ Offset, Low-Noise, Bipolar Operational Amplifier

## 1 Features

- Low offset voltage: 25  $\mu\text{V}$  (max)
- Low offset voltage drift: 0.3  $\mu\text{V}/^\circ\text{C}$  (max)
- High open-loop gain: 134 dB (min)
- Low quiescent current: 1.3 mA (typ)
- Low input bias  $\pm 2$  nA (max)
- Wide supply voltage range: 6 V to 36 V
- Replaces industry-standard op amps: OP-07, OP-77, OP-177, AD707, and more
- For improved performance with  $\pm 40$ -V overvoltage protection, see the [OPA206](#)

## 2 Applications

- [Analog input module](#)
- [Data acquisition \(DAQ\)](#)
- [Battery test](#)
- [Lab and field instrumentation](#)
- [Temperature transmitter](#)

## 3 Description

The OPA177 precision bipolar op amp feature very low offset voltage and drift. Laser-trimmed offset, drift and input bias current virtually eliminate the need for costly external trimming. High performance and low cost make these devices an excellent choice for a wide range of precision instrumentation.

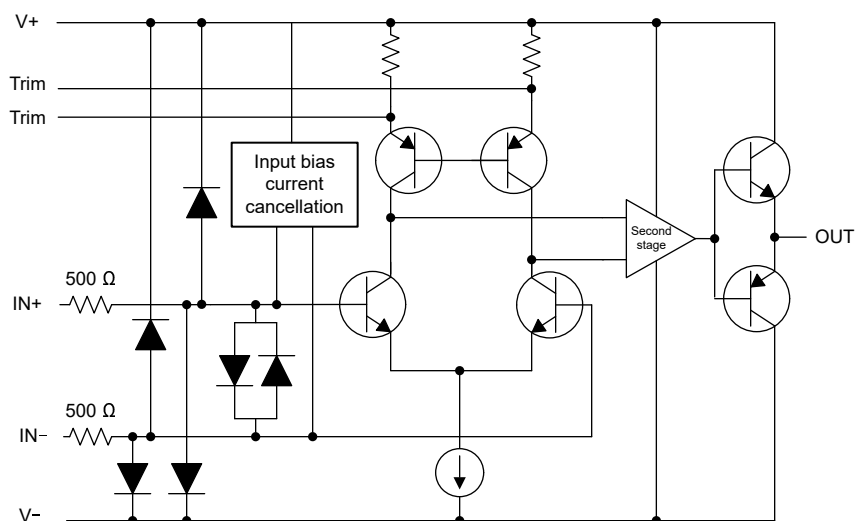
The low quiescent current of the OPA177 dramatically reduces warm-up drift and errors due to thermoelectric effects in input interconnections. The OPA177 provides an effective alternative to chopper-stabilized amplifiers. The low noise of the OPA177 helps maintain maximum signal integrity.

OPA177 performance grade-outs are available. Packaging options include 8-pin plastic DIP and SO-8 surface-mount packages.

### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|-------------|------------------------|-----------------------------|
| OPA177      | D (SOIC, 8)            | 4.9 mm $\times$ 6 mm        |
|             | P (PDIP, 8)            | 9.81 mm $\times$ 9.43 mm    |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length  $\times$  width) is a nominal value and includes pins, where applicable.



## Table of Contents

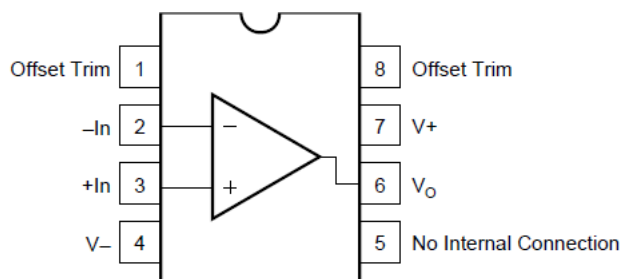
|                                                |          |                                                              |           |
|------------------------------------------------|----------|--------------------------------------------------------------|-----------|
| <b>1 Features</b> .....                        | <b>1</b> | <b>7 Application and Implementation</b> .....                | <b>10</b> |
| <b>2 Applications</b> .....                    | <b>1</b> | 7.1 Application Information.....                             | 10        |
| <b>3 Description</b> .....                     | <b>1</b> | 7.2 Typical Application.....                                 | 11        |
| <b>4 Revision History</b> .....                | <b>2</b> | <b>8 Device and Documentation Support</b> .....              | <b>12</b> |
| <b>5 Pin Configuration and Functions</b> ..... | <b>3</b> | 8.1 Device Support.....                                      | 12        |
| <b>6 Specifications</b> .....                  | <b>4</b> | 8.2 Receiving Notification of Documentation Updates....      | 13        |
| 6.1 Absolute Maximum Ratings.....              | 4        | 8.3 Support Resources.....                                   | 13        |
| 6.2 ESD Ratings.....                           | 4        | 8.4 Trademarks.....                                          | 13        |
| 6.3 Recommended Operating Conditions.....      | 4        | 8.5 Electrostatic Discharge Caution.....                     | 13        |
| 6.4 Thermal Information.....                   | 4        | 8.6 Glossary.....                                            | 13        |
| 6.5 Electrical Characteristics.....            | 5        | <b>9 Mechanical, Packaging, and Orderable Information</b> .. | <b>13</b> |
| 6.6 Typical Characteristics.....               | 7        |                                                              |           |

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision * (September 2000) to Revision A (September 2023)</b>                                                                                                                 | <b>Page</b> |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| • Updated the numbering format for tables, figures, and cross-references throughout the document.....                                                                                          | 1           |
| • Changed data sheet title for clarity.....                                                                                                                                                    | 1           |
| • Added <i>Package Information</i> table, and <i>Typical Application</i> , <i>Device and Documentation Support</i> , and <i>Mechanical, Packaging, and Orderable Information</i> sections..... | 1           |
| • Added additional Features bullets and updated several specifications to align with <i>Electrical Characteristics</i> ..                                                                      | 1           |
| • Changed application bullets to show linked applications.....                                                                                                                                 | 1           |
| • Changed <i>Description</i> text for clarity.....                                                                                                                                             | 1           |
| • Updated front-page diagram.....                                                                                                                                                              | 1           |
| • Added pin functions table.....                                                                                                                                                               | 3           |
| • Changed supply voltage from $\pm 22$ V (44 V) to 40 V in <i>Absolute Maximum Ratings</i> .....                                                                                               | 4           |
| • Moved operating temperature from <i>Absolute Maximum Ratings</i> to <i>Recommended Operating Conditions</i> .....                                                                            | 4           |
| • Deleted lead temperature from <i>Absolute Maximum Ratings</i> .....                                                                                                                          | 4           |
| • Moved junction to ambient thermal information from <i>Absolute Maximum Ratings</i> to <i>Thermal Information</i> .....                                                                       | 4           |
| • Added <i>ESD Ratings</i> and <i>Thermal Information</i> .....                                                                                                                                | 4           |
| • Changed several parameter names for consistency with modern data sheets in <i>Electrical Characteristics</i> .....                                                                           | 5           |
| • Updated the format of <i>Electrical Characteristics</i> .....                                                                                                                                | 5           |
| • Added test conditions to the header of <i>Electrical Characteristics</i> .....                                                                                                               | 5           |
| • Moved test conditions from condition column to the header of <i>Electrical Characteristics</i> .....                                                                                         | 5           |
| • Changed open-loop voltage gain unit from V/mV to dB in <i>Electrical Characteristics</i> .....                                                                                               | 5           |
| • Changed large signal voltage gain to open-loop voltage gain in <i>Electrical Characteristics</i> .....                                                                                       | 5           |
| • Changed Power Supply parameters no load test condition to $I_O = 0$ A in <i>Electrical Characteristics</i> .....                                                                             | 5           |
| • Updated quiescent current maximum over temperature specification value from 25 mA (typo) to $\pm 2.5$ mA.....                                                                                | 5           |
| • Changed supply current to quiescent current in <i>Electrical Characteristics</i> .....                                                                                                       | 5           |
| • Added information about integrated overvoltage protection including OPAx206 to Input Protection.....                                                                                         | 10          |
| • Updated Noise Performance with new products such as the OPAx828, OPAx140, and OPAx210.....                                                                                                   | 10          |
| • Changed operational amplifier recommendations to reflect new product developments.....                                                                                                       | 10          |

## 5 Pin Configuration and Functions



**Figure 5-1. D Package, 8-Pin SOIC  
and P Package, 8-Pin PDIP  
(Top View)**

**Table 5-1. Pin Functions**

| PIN                    |      | TYPE   | DESCRIPTION                                            |
|------------------------|------|--------|--------------------------------------------------------|
| NAME                   | NO.  |        |                                                        |
| +In                    | 3    | Input  | Noninverting input                                     |
| -In                    | 2    | Input  | Inverting input                                        |
| No Internal Connection | 5    | —      | No internal connection (can be left floating)          |
| Offset Trim            | 1, 8 | —      | Input offset voltage trim (leave floating if not used) |
| V+                     | 7    | Power  | Positive (highest) power supply                        |
| V-                     | 4    | Power  | Negative (lowest) power supply                         |
| V <sub>O</sub>         | 6    | Output | Output                                                 |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                              | MIN        | MAX  | UNIT |
|------------------|----------------------------------------------|------------|------|------|
| V <sub>S</sub>   | Supply voltage, V <sub>S</sub> = (V+) – (V–) |            | 40   | V    |
|                  | Input voltage                                | (V–)       | (V+) | V    |
|                  | Differential input voltage                   | –30        | 30   | V    |
| I <sub>SC</sub>  | Output short circuit <sup>(2)</sup>          | Continuous |      |      |
| T <sub>J</sub>   | Junction temperature                         |            | 150  | °C   |
| T <sub>STG</sub> | Storage temperature                          | –65        | 125  | °C   |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Short-circuit to ground, one amplifier per package.

### 6.2 ESD Ratings

|                    |                                                                                           | VALUE | UNIT |
|--------------------|-------------------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup> | ±1000 | V    |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                |                                              |               | MIN | NOM | MAX | UNIT |
|----------------|----------------------------------------------|---------------|-----|-----|-----|------|
| V <sub>S</sub> | Supply voltage, V <sub>S</sub> = (V+) – (V–) | Single supply | 6   | 30  | 36  | V    |
|                |                                              | Dual supply   | ±3  | ±15 | ±18 |      |
| T <sub>A</sub> | Ambient temperature                          |               | –40 |     | 85  | °C   |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                        | OPA177   |          | UNIT |
|-------------------------------|----------------------------------------|----------|----------|------|
|                               |                                        | D (SOIC) | P (PDIP) |      |
|                               |                                        | 8 PINS   | 8 PINS   |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance | 160.0    | 100.0    | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report

## 6.5 Electrical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 30\text{ V}$  ( $\pm 15\text{ V}$ ),  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_L = 2\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted)

| PARAMETER            |                                          | TEST CONDITIONS                                                   |         | MIN  | TYP   | MAX               | UNIT |
|----------------------|------------------------------------------|-------------------------------------------------------------------|---------|------|-------|-------------------|------|
| OFFSET VOLTAGE       |                                          |                                                                   |         |      |       |                   |      |
| VOS                  | Input offset voltage                     | F grade                                                           |         | ±10  | ±25   | μV                |      |
|                      |                                          | G grade                                                           |         | ±20  | ±60   |                   |      |
|                      |                                          | T <sub>A</sub> = −40°C to +85°C                                   | F grade | ±15  | ±40   |                   |      |
|                      |                                          |                                                                   | G grade | ±20  | ±100  |                   |      |
| dV <sub>OS</sub> /dT | Input offset voltage drift               | T <sub>A</sub> = −40°C to +85°C                                   | F grade | ±0.1 | ±0.3  | μV/°C             |      |
|                      |                                          |                                                                   | G grade | ±0.7 | ±1.2  |                   |      |
|                      | Offset adjustment range                  | R <sub>p</sub> = 20 kΩ                                            |         | ±3   |       | mV                |      |
|                      | Long-term drift <sup>(1)</sup>           | F grade                                                           |         | 0.3  |       | μV/mo             |      |
|                      |                                          | G grade                                                           |         | 0.4  |       |                   |      |
| PSRR                 | Power-supply rejection ratio             | V <sub>S</sub> = ±3 V to ±18 V                                    | F grade | 115  | 125   | dB                |      |
|                      |                                          |                                                                   | G grade | 110  | 120   |                   |      |
|                      |                                          | V <sub>S</sub> = ±3 V to ±18 V<br>T <sub>A</sub> = −40°C to +85°C | F grade | 110  | 120   |                   |      |
|                      |                                          |                                                                   | G grade | 106  | 115   |                   |      |
| INPUT BIAS CURRENT   |                                          |                                                                   |         |      |       |                   |      |
| I <sub>B</sub>       | Input bias current                       | F grade                                                           |         | ±0.5 | ±2    | nA                |      |
|                      |                                          | G grade                                                           |         | ±0.5 | ±2.8  |                   |      |
|                      |                                          | T <sub>A</sub> = −40°C to +85°C                                   | F grade | ±0.5 | ±4    |                   |      |
|                      |                                          |                                                                   | G grade | ±0.5 | ±6    |                   |      |
|                      | Input bias current drift <sup>(2)</sup>  | T <sub>A</sub> = −40°C to +85°C                                   | F grade | ±8   | ±40   | pA/°C             |      |
|                      |                                          |                                                                   | G grade | ±15  | ±60   |                   |      |
| I <sub>OS</sub>      | Input offset current                     | F grade                                                           |         | ±0.3 | ±1.5  | nA                |      |
|                      |                                          | G grade                                                           |         | ±0.3 | ±2.8  |                   |      |
|                      |                                          | T <sub>A</sub> = −40°C to +85°C                                   | F grade | ±0.5 | ±2.2  |                   |      |
|                      |                                          |                                                                   | G grade | ±0.5 | ±4.5  |                   |      |
| NOISE                |                                          |                                                                   |         |      |       |                   |      |
|                      | Input bias current drift <sup>(2)</sup>  | F grade                                                           |         | ±1.5 | ±40   | pA/°C             |      |
|                      |                                          | G grade                                                           |         | ±1.5 | ±85   |                   |      |
|                      | Input voltage noise                      | f = 1 Hz to 100 Hz <sup>(3)</sup>                                 |         | 85   | 150   | nV <sub>rms</sub> |      |
|                      | Input current noise                      | f = 1 Hz to 100 Hz                                                |         | 45   |       | pA <sub>rms</sub> |      |
| INPUT VOLTAGE        |                                          |                                                                   |         |      |       |                   |      |
| V <sub>CM</sub>      | Common-mode voltage range <sup>(4)</sup> |                                                                   |         | ±13  | ±14   | V                 |      |
|                      |                                          | T <sub>A</sub> = −40°C to +85°C                                   |         | ±13  | ±13.5 |                   |      |
| CMRR                 | Common-mode rejection ratio              | V <sub>CM</sub> = ±13 V                                           | F grade | 130  | 140   | dB                |      |
|                      |                                          |                                                                   | G grade | 115  | 140   |                   |      |
|                      |                                          | V <sub>CM</sub> = ±13 V<br>T <sub>A</sub> = −40°C to +85°C        | F grade | 120  | 140   |                   |      |
|                      |                                          |                                                                   | G grade | 110  | 140   |                   |      |
| INPUT IMPEDANCE      |                                          |                                                                   |         |      |       |                   |      |
| R <sub>in</sub>      | Input resistance                         | Differential mode <sup>(5)</sup>                                  | F grade | 26   | 45    | MΩ                |      |
|                      |                                          |                                                                   | G grade | 18.5 | 45    |                   |      |
|                      |                                          | Common-mode                                                       |         | 200  |       | GΩ                |      |

## 6.5 Electrical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 30\text{ V}$  ( $\pm 15\text{ V}$ ),  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_L = 2\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted)

| PARAMETER          |                                       | TEST CONDITIONS                                                  |                                 | MIN   | TYP   | MAX | UNIT |
|--------------------|---------------------------------------|------------------------------------------------------------------|---------------------------------|-------|-------|-----|------|
| OPEN-LOOP GAIN     |                                       |                                                                  |                                 |       |       |     |      |
| A <sub>OL</sub>    | Open-loop voltage gain <sup>(6)</sup> | −10 V ≤ V <sub>O</sub> ≤ 10 V                                    | F grade                         | 134   | 141   | dB  |      |
|                    |                                       |                                                                  | G grade                         | 126   | 135   |     |      |
|                    |                                       | −10 V ≤ V <sub>O</sub> ≤ 10 V<br>T <sub>A</sub> = −40°C to +85°C | F grade                         | 126   | 135   |     |      |
|                    |                                       |                                                                  | G grade                         | 120   | 132   |     |      |
| FREQUENCY RESPONSE |                                       |                                                                  |                                 |       |       |     |      |
| BW <sub>CL</sub>   | Closed-loop bandwidth                 | G = 1                                                            |                                 | 0.4   | 0.6   |     | MHz  |
| SR                 | Slew rate                             |                                                                  |                                 | 0.1   | 0.3   |     | V/μs |
| OUTPUT             |                                       |                                                                  |                                 |       |       |     |      |
| V <sub>O</sub>     | Voltage output swing                  | R <sub>L</sub> ≥ 2 kΩ                                            |                                 | ±13.5 | ±14   | V   |      |
|                    |                                       |                                                                  | T <sub>A</sub> = −40°C to +85°C | ±12   | ±13   |     |      |
|                    |                                       | R <sub>L</sub> ≥ 10 kΩ                                           |                                 | ±12.5 | ±13   |     |      |
|                    |                                       | R <sub>L</sub> ≥ 1 kΩ                                            |                                 | ±12   | ±12.5 |     |      |
| I <sub>SC</sub>    | Short-circuit current                 |                                                                  |                                 | ±35   |       |     | mA   |
| R <sub>O</sub>     | Open-loop output resistance           |                                                                  |                                 | 60    |       |     | Ω    |
| POWER SUPPLY       |                                       |                                                                  |                                 |       |       |     |      |
|                    | Power consumption                     | I <sub>O</sub> = 0 A                                             |                                 | 40    | 60    | mW  |      |
|                    |                                       |                                                                  | T <sub>A</sub> = −40°C to +85°C | 60    | 75    |     |      |
| I <sub>Q</sub>     | Quiescent current                     | I <sub>O</sub> = 0 A                                             |                                 | 1.3   | 2     | mA  |      |
|                    |                                       |                                                                  | T <sub>A</sub> = −40°C to +85°C | 2     | 2.5   |     |      |

- (1) Long-term input offset voltage stability refers to the averaged trend line of  $V_{OS}$  vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 operating days are typically less than  $2\text{ }\mu\text{V}$ .
- (2) Specified by characterization.
- (3) Sample tested.
- (4) Specified CMRR test condition.
- (5) Specified by design.
- (6) To maintain high open-loop gain throughout the  $\pm 10\text{-V}$  output range,  $A_{OL}$  is tested at  $-10\text{ V} \leq V_O \leq 0\text{ V}$ ,  $0\text{ V} \leq V_O \leq +10\text{ V}$ , and  $-10\text{ V} \leq V_O \leq +10\text{ V}$ .

## 6.6 Typical Characteristics

at  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$  (unless otherwise noted)

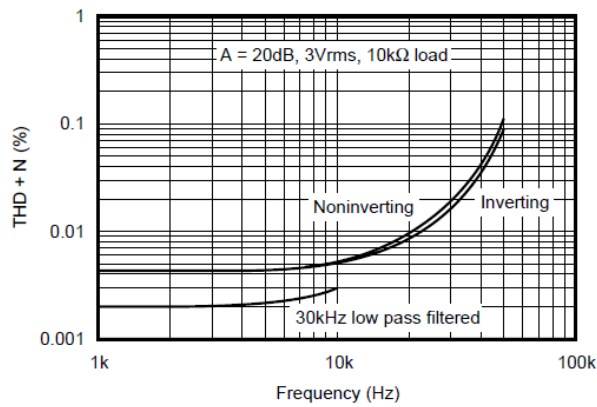


Figure 6-1. Total Harmonic Distortion and Noise vs Frequency

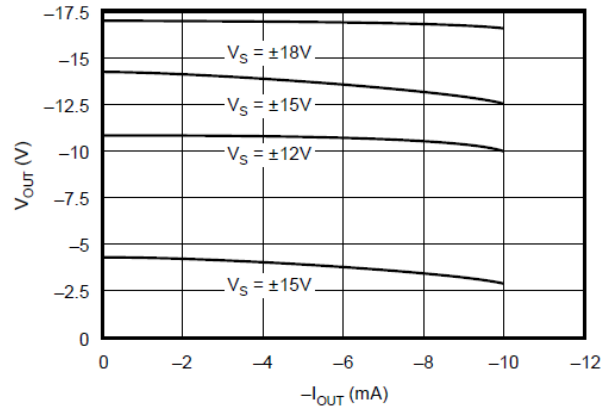


Figure 6-2. Maximum  $V_{OUT}$  vs  $I_{OUT}$  (Negative Swing)

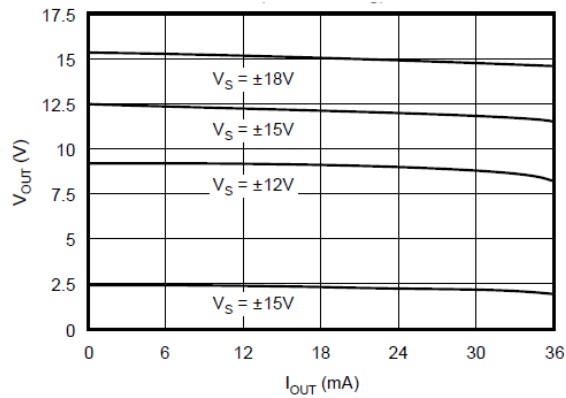


Figure 6-3. Maximum  $V_{OUT}$  vs  $I_{OUT}$  (Positive Swing)

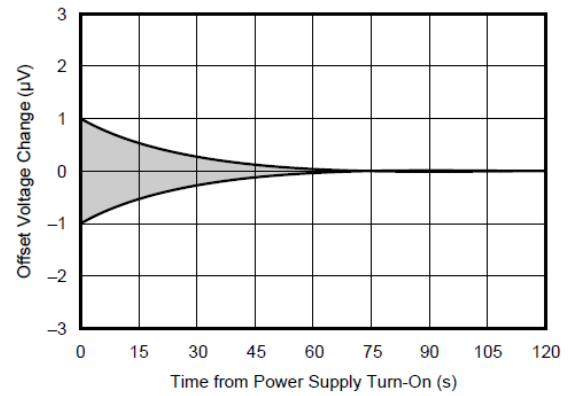


Figure 6-4. Warm-Up Offset Voltage Drift

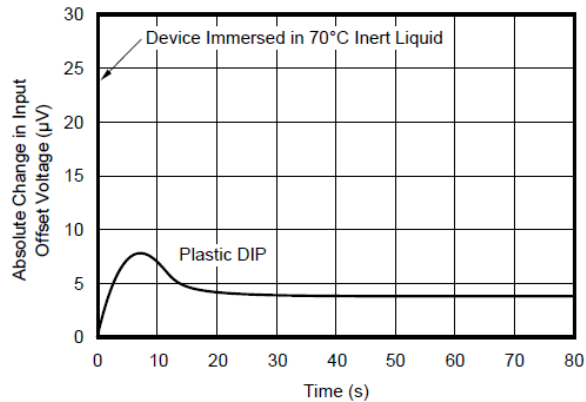


Figure 6-5. Offset Voltage Change Due To Thermal Shock

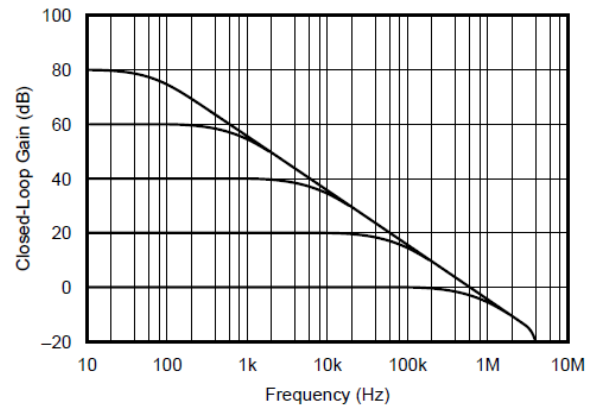


Figure 6-6. Closed-Loop Response vs Frequency

## 6.6 Typical Characteristics (continued)

at  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$  (unless otherwise noted)

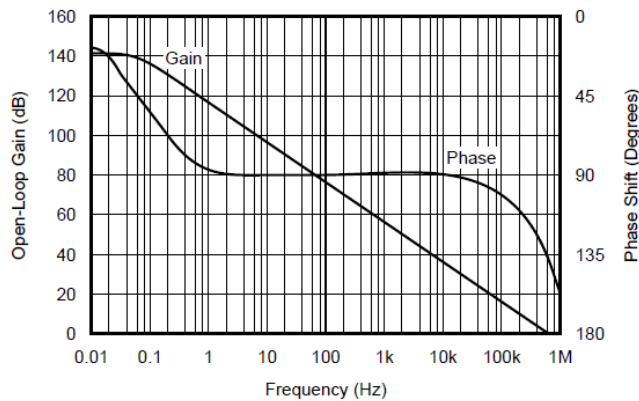


Figure 6-7. Open-Loop Gain/Phase vs Frequency

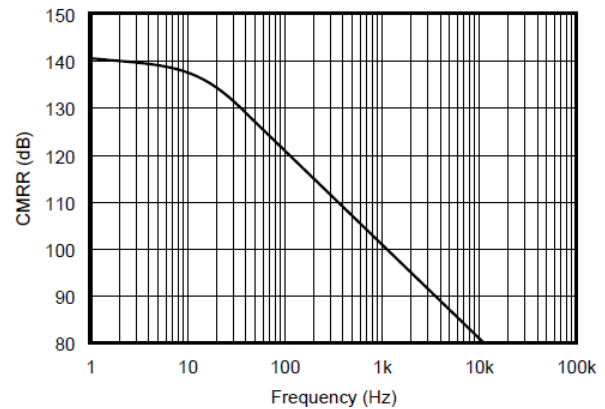


Figure 6-8. CMRR vs Frequency

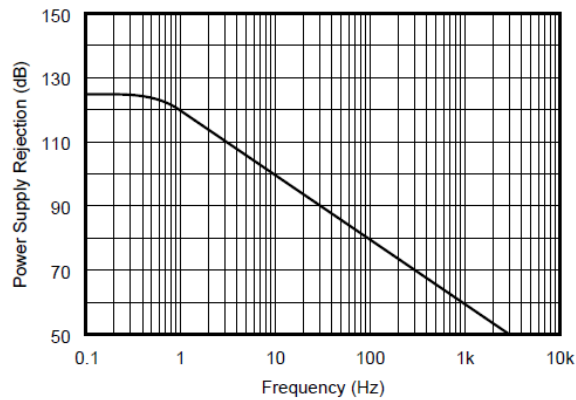


Figure 6-9. Power Supply Rejection vs Frequency

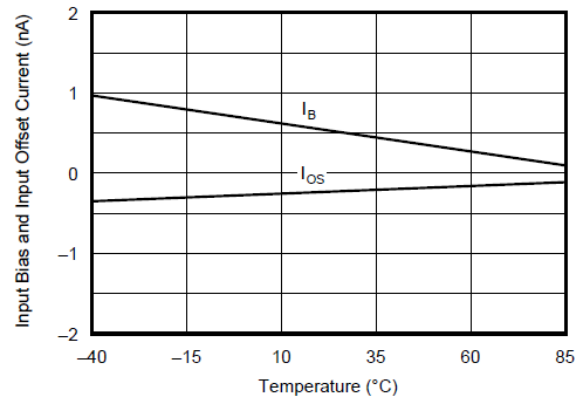


Figure 6-10. Input Bias and Input Offset Current vs Temperature

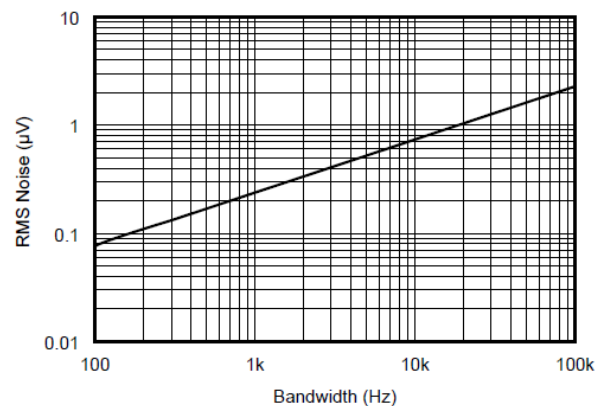


Figure 6-11. Total Noise vs Bandwidth (0.1Hz to Frequency Indicated)

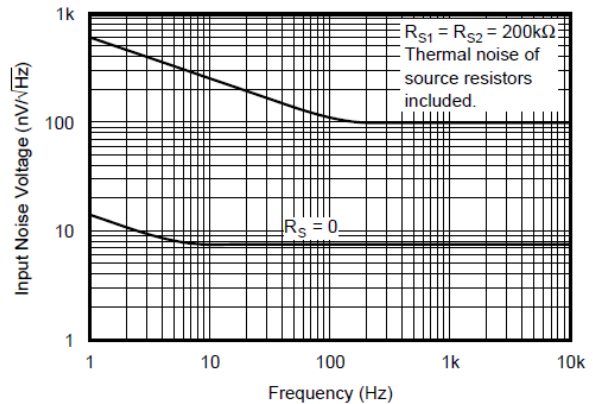


Figure 6-12. Input Noise Voltage Density vs frequency



## 6.6 Typical Characteristics (continued)

at  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$  (unless otherwise noted)

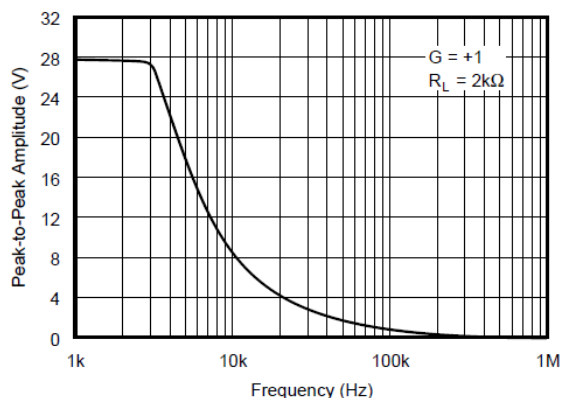


Figure 6-13. Maximum Output Swing vs Frequency

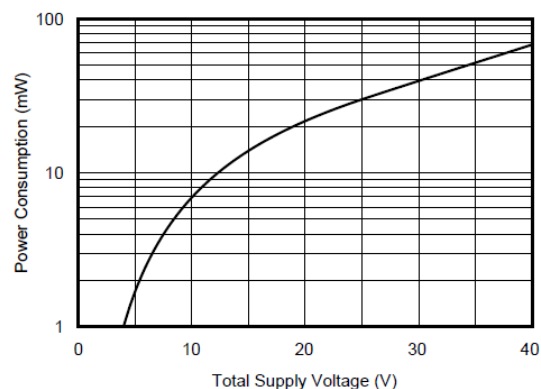


Figure 6-14. Power Consumption vs Power Supply

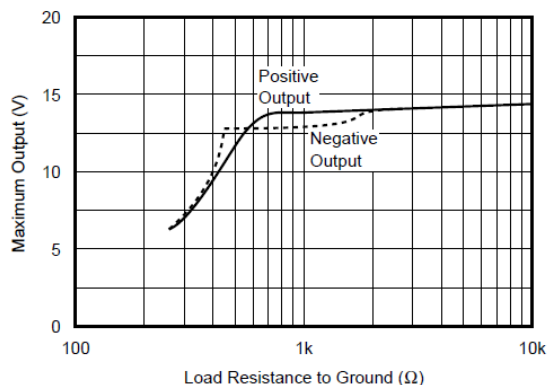


Figure 6-15. Maximum Output Voltage vs Load Resistance

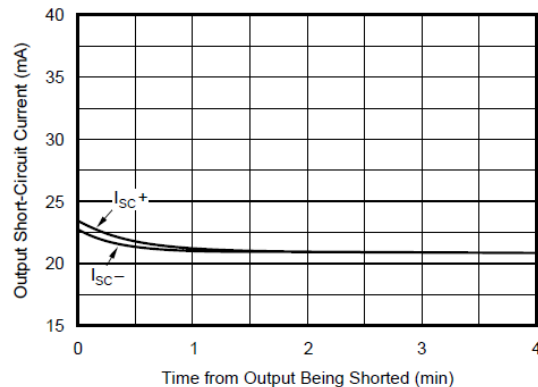


Figure 6-16. Output Short-Circuit Current vs Time

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Application Information

The OPA177 is unity-gain stable, making this device easy to use and free from oscillations in the widest range of circuitry. Applications with noisy or high-impedance power-supply lines can require decoupling capacitors close to the device pins. In most cases, 0.1- $\mu$ F ceramic capacitors are adequate.

The OPA177 has very low offset voltage and drift. To achieve highest performance, optimize circuit layout and mechanical conditions. Offset voltage and drift degrades because of small thermoelectric potentials at the op-amp inputs. Connections of dissimilar metals generate thermal potential that can degrade the ultimate performance of the OPA177. To cancel these thermal potentials, make sure the thermal potentials are equal in both input pins.

1. Keep connections made to the two input pins close together.
2. Locate heat sources as far as possible from the critical input circuitry.
3. Shield the op amp and input circuitry from air currents, such as cooling fans.

#### 7.1.1 Offset Voltage Adjustment

The OPA177 has been laser-trimmed for low offset voltage and drift; therefore, most circuits do not require external adjustment. [Figure 7-1](#) shows the optional connection of an external potentiometer to adjust offset voltage. Do not use this adjustment to compensate for offsets created elsewhere in a system because this adjustment can introduce excessive temperature drift.

#### 7.1.2 Input Protection

The inputs of the OPA177 are protected with 500- $\Omega$  series input resistors and diode clamps as shown in the simplified circuit diagram on the front page. The inputs can withstand  $\pm 30$ -V differential inputs without damage. The protection diodes conduct current when the inputs are overdriven. This conducted current can disturb the slewing behavior of unity-gain follower applications, but does not damage the op amp. Some applications, such as programmable logic controllers (PLCs) require a robust input-protection design. An input-protection circuit can be implemented using four Schottky diodes; however, the temperature and voltage dependent leakage of the diodes can present undesirable nonlinear errors at the input. For applications requiring high precision and robust input protection, the [OPAx206](#) family of op amps are an excellent choice, offering integrated input overvoltage protection that eliminates the need for external clamping circuits.

#### 7.1.3 Noise Performance

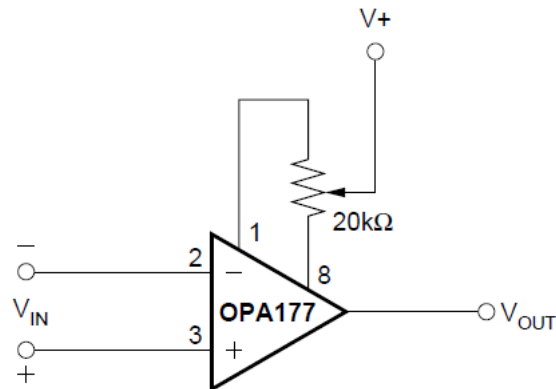
The OPA177 noise performance is optimized for a circuit impedance range of 2 k $\Omega$  to 50 k $\Omega$ . Total noise in an application is a combination of the op-amp input voltage noise and input bias current noise reacting with circuit impedance. For applications with higher source impedance, the [OPAx828](#) and [OPAx140](#) FET-input op amps generally provide lower noise due to the inherently low input current noise. For low-impedance, low-noise applications, the [OPAx210](#) is an excellent choice because of the exceptionally low op-amp input-voltage noise.

### 7.1.4 Input Bias Current Cancellation

The input stage base current of the OPA177 is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

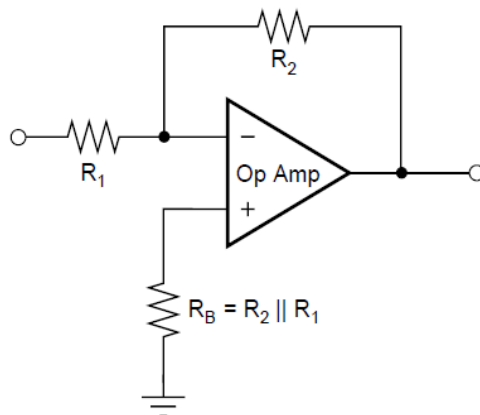
When the bias current is canceled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, there is no need to balance the dc resistance seen at the two input pins (Figure 7-2 and Figure 7-3). A resistor added to balance the input resistances can actually increase offset and noise.

## 7.2 Typical Application



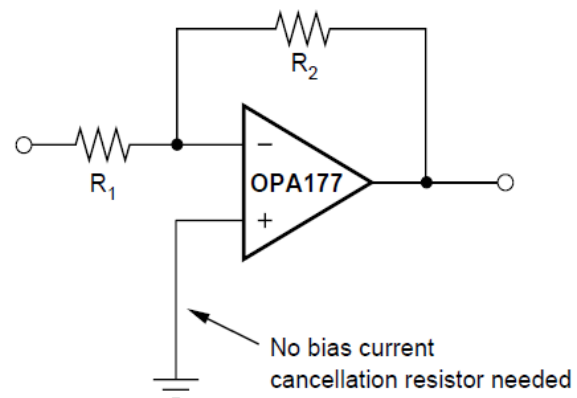
Trim range is approximately  $\pm 3.0$  mV.

**Figure 7-1. Optional Offset Nulling Circuit**



Conventional op amp with external bias current cancellation resistor.

**Figure 7-2. Input Bias Current Cancellation With Conventional Op Amp**



OPA177 with no external bias current cancellation resistor.

**Figure 7-3. Input Bias Current Cancellation With OPA177**

## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 8.1 Device Support

#### 8.1.1 Development Support

##### 8.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

##### 8.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the [Design tools and simulation](#) web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

---

#### Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the [TINA-TI™ software folder](#).

---

##### 8.1.1.3 DIP-Adapter-EVM

Speed up your op amp prototyping and testing with the [DIP-Adapter-EVM](#), which provides a fast, easy and inexpensive way to interface with small, surface-mount devices. Connect any supported op amp using the included Samtec terminal strips or wire them directly to existing circuits. The DIP-Adapter-EVM kit supports the following industry-standard packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT-23-6, SOT-23-5 and SOT-23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6).

##### 8.1.1.4 DIYAMP-EVM

The [DIYAMP-EVM](#) is a unique evaluation module (EVM) that provides real-world amplifier circuits, enabling the user to quickly evaluate design concepts and verify simulations. This EVM is available in three industry-standard packages (SC70, SOT23, and SOIC) and 12 popular amplifier configurations, including amplifiers, filters, stability compensation, and comparator configurations for both single and dual supplies.

##### 8.1.1.5 TI Reference Designs

TI reference designs are analog solutions created by TI's precision analog applications experts. TI reference designs offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI reference designs are available online at <https://www.ti.com/reference-designs>.

##### 8.1.1.6 Filter Design Tool

The [filter design tool](#) is a simple, powerful, and easy-to-use active filter design program. The filter design tool allows the user to create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the [Design tools and simulation](#) web page, the [filter design tool](#) allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

## 8.4 Trademarks

TINA-TI™ and TI E2E™ are trademarks of Texas Instruments.

TINA™ is a trademark of DesignSoft, Inc.

PSpice® is a registered trademark of Cadence Design Systems, Inc.

All trademarks are the property of their respective owners.

## 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">OPA177FP</a>     | Obsolete      | Production           | PDIP (P)   8   | -                     | -           | Call TI                              | Call TI                           | -            | OPA177FP            |
| <a href="#">OPA177GP</a>     | Obsolete      | Production           | PDIP (P)   8   | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | OPA177GP            |
| <a href="#">OPA177GS</a>     | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -            | OPA<br>177GS        |
| OPA177GS.B                   | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | OPA<br>177GS        |
| <a href="#">OPA177GS/2K5</a> | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -            | OPA<br>177GS        |
| OPA177GS/2K5.B               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | OPA<br>177GS        |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

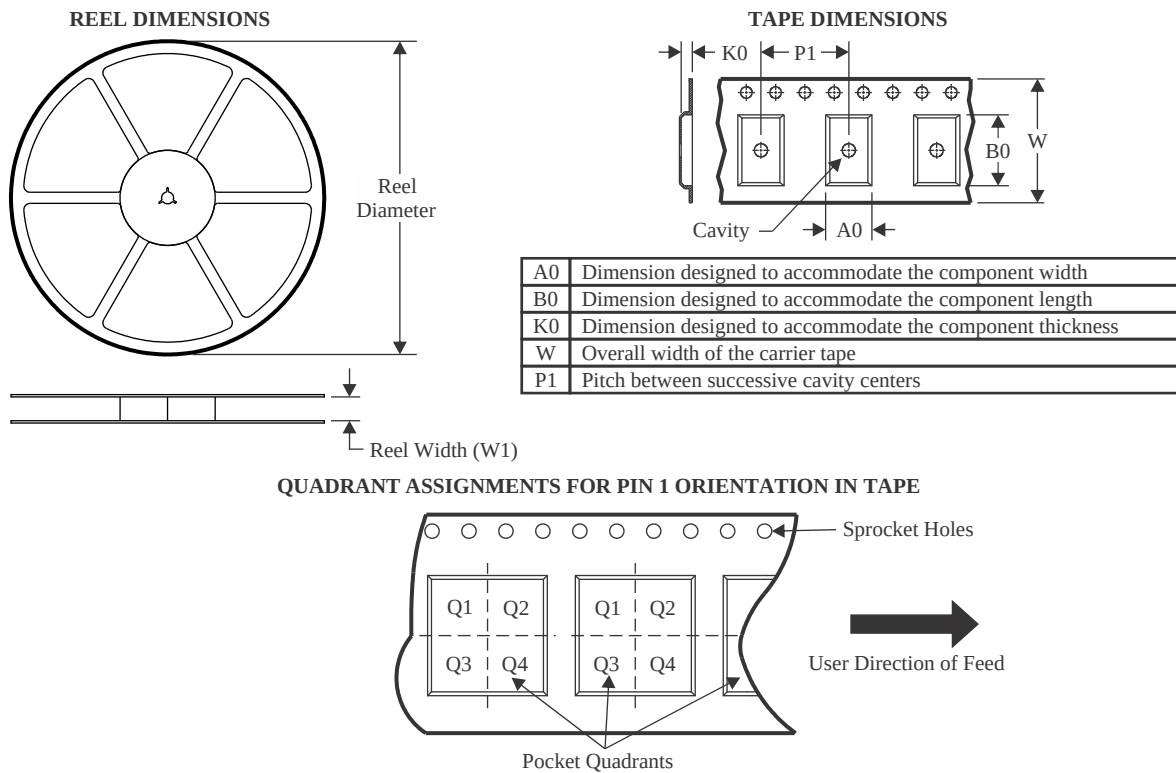
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

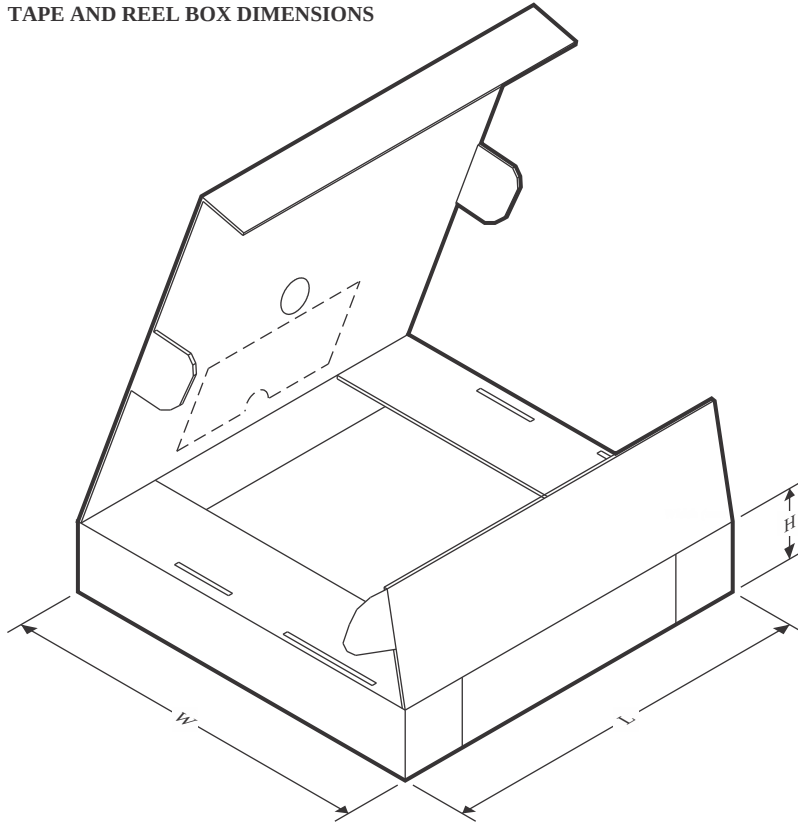


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| OPA177GS/2K5 | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OPA177GS/2K5 | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| OPA177GS/2K5 | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| OPA177GS/2K5 | SOIC         | D               | 8    | 2500 | 356.0       | 356.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device     | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| OPA177GS   | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| OPA177GS.B | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated