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FAIRCHILD

SEMICONDUCTOR®

February 1998
Revised June 2005

74VHC161284
IEEE 1284 Transceiver

General Description

The VHC161284 contains eight bidirectional data buffers and eleven control/status buffers to implement a full IEEE 1284 compliant interface. The device supports the IEEE 1284 standard and is intended to be used in Extended Capabilities Port mode (ECP). The pinout allows for easy connection from the Peripheral (A-side) to the Host (cable side).

Outputs on the cable side can be configured to be either open drain or high drive ($\pm$ 14 mA). The pull-up and pull-down series termination resistance of these outputs on the cable side is optimized to drive an external cable. In addition, all inputs (except HLH) and outputs on the cable side contain internal pull-up resistors connected to the V_{CC} supply to provide proper termination and pull-ups for open drain mode.

Outputs on the Peripheral side are standard LOW-drive CMOS outputs. The DIR input controls data flow on the A_1–A_8/B_1–B_8 transceiver pins.

Features

■ Supports IEEE 1284 Level 1 and Level 2 signaling standards for bidirectional parallel communications between personal computers and printing peripherals

■ Replaces the function of two (2) 74ACT1284 devices

■ All inputs have hysteresis to provide noise margin

■ B and Y output resistance optimized to drive external cable

■ B and Y outputs in high impedance mode during power down

■ Inputs and outputs on cable side have internal pull-up resistors

■ Flow-through pin configuration allows easy interface between the Peripheral and Host

Ordering Code:

Ordering Number	Package Number	Package Description
74VHC161284MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74VHC161284MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

Connection Diagram

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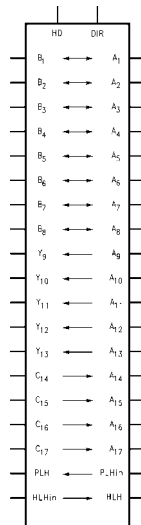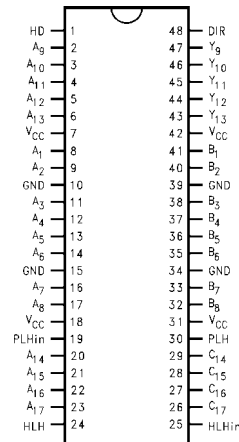
Pin Descriptions

Pin Names	Description
HD	HIGH Drive Enable Input (Active HIGH)
DIR	Direction Control Input
A_1–A_8	Inputs or Outputs
B_1–B_8	Inputs or Outputs
A_9–A_{13}	Inputs
Y_9–Y_{13}	Outputs
A_{14}–A_{17}	Outputs
C_{14}–C_{17}	Inputs
PLH_{IN}	Peripheral Logic HIGH Input
PLH	Peripheral Logic HIGH Output
HLH_{IN}	Host Logic HIGH Input
HLH	Host Logic HIGH Output

Truth Table

Inputs		Outputs
DIR	HD	
L	L	B_1–B_8 Data to A_1–A_8, and A_9–A_{13} Data to Y_9–Y_{13} (Note 1) C_{14}–C_{17} Data to A_{14}–A_{17} PLH Open Drain Mode
L	H	B_1–B_8 Data to A_1–A_8, and A_9–A_{13} Data to Y_9–Y_{13} C_{14}–C_{17} Data to A_{14}–A_{17}
H	L	A_1–A_8 Data to B_1–B_8 (Note 2) A_9–A_{13} Data to Y_9–Y_{13} (Note 1) C_{14}–C_{17} Data to A_{14}–A_{17} PLH Open Drain Mode
H	H	A_1–A_8 Data to B_1–B_8 A_9–A_{13} Data to Y_9–Y_{13} C_{14}–C_{17} Data to A_{14}–A_{17}

Note 1: Y_9–Y_{13} Open Drain Outputs

Note 2: B_1–B_8 Open Drain Outputs

Logic Diagram
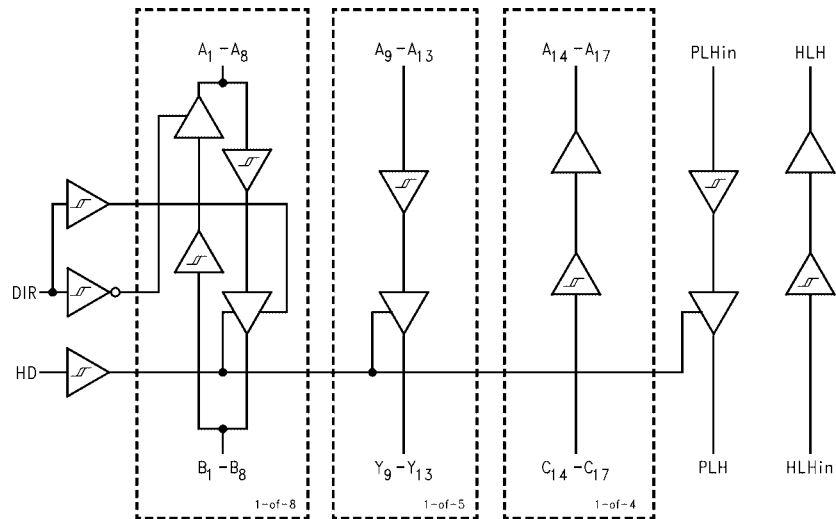
Absolute Maximum Ratings(Note 3)

Supply Voltage

V_{CC} −0.5V to + 7.0V

Input Voltage (V_I) (Note 4)

A_1–A_{13}, PLH_{IN}, DIR, HD	−0.5V to V_{CC} + 0.5V
B_1–B_8, C_{14}–C_{17}, HLH_{IN}	−0.5V to + 5.5V (DC)
B_1–B_8, C_{14}–C_{17}, HLH_{IN}	−2.0V to + 7.0V *
	*40 ns Transient

Output Voltage (V_O)

A_1–A_8, A_{14}–A_{17}, HLH	−0.5V to V_{CC} + 0.5V
B_1–B_8, Y_9–Y_{13}, PLH	−0.5V to + 5.5V (DC)
B_1–B_8, Y_9–Y_{13}, PLH	−2.0V to + 7.0V*
	*40 ns Transient

DC Output Current (I_O)

A_1–A_8, HLH	±25 mA
B_1–B_8, Y_9–Y_{13}	±50 mA
PLH (Output LOW)	84 mA
PLH (Output HIGH)	−50 mA

Input Diode Current (I_{IK}) (Note 4)

DIR, HD, A_9–A_{13},

PLH, HLH, C_{14}–C_{17} −20 mA

Output Diode Current (I_{OK})

A_1–A_8, A_{14}–A_{17}, HLH	±50 mA
B_1–B_8, Y_9–Y_{13}, PLH	−50 mA

DC Continuous V_{CC} or

Ground Current   ±200 mA

Storage Temperature   −65°C to + 150°C

ESD (HBM) Last Passing

Voltage   2000V

Recommended Operating Conditions

Supply Voltage

V_{CC} 4.5V to 5.5V

DC Input Voltage (V_I)   0V to V_{CC}

Open Drain Voltage (V_O)   0V to 5.5V

Operating Temperature (T_A)   −40°C to + 85°C

Note 3: Absolute Maximum continuos ratings are those values beyond which damage to the device may occur. Exposure to these indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 4: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	$T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
V_{IK}	Input Clamp Diode Voltage		3.0	−1.2	V	$I_I = -18$ mA
V_{IH}	Minimum HIGH Level Input Voltage	A_n, PLH_{IN}, DIR, HD	4.5 – 5.5	0.7 V_{CC}	V	
		B_n	4.5 – 5.5	2.0		
		C_n	4.5 – 5.5	2.3		
		HLH_{IN}	4.5 – 5.5	2.6		
V_{IL}	Maximum LOW Level Input Voltage	A_n, PLH_{IN}, DIR, HD	4.5 – 5.5	0.3 V_{CC}	V	
		B_n	4.5 – 5.5	0.8		
		C_n	4.5 – 5.5	0.8		
		HLH_{IN}	4.5 – 5.5	1.6		
ΔVT	Minimum Input Hysteresis	A_n, PLH_{IN}, DIR, HD	4.5 – 5.5	0.4	V	$V_T{}^+ - V_T{}^-$
		B_n	4.5 – 5.5	0.4		$V_T{}^+ - V_T{}^-$
		C_n	5.0	0.8		$V_T{}^+ - V_T{}^-$
		HLH_{IN}	5.0	0.3		$V_T{}^+ - V_T{}^-$
V_{OH}	Minimum HIGH Level Output Voltage	A_n, HLH	4.5	4.4	V	$I_{OH} = -50$ μA
			4.5	3.8		$I_{OH} = -8$ mA
		B_n, Y_n	4.5	3.73		$I_{OH} = -14$ mA
		PLH	4.5	4.45		$I_{OH} = -500$ μA

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC} (V)	$T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
V_{OL}	Maximum LOW Level Output Voltage	A_n, HLH	4.5	0.1	V	$I_{OL} = 50 \ \mu A$
			4.5	0.44		$I_{OL} = 8$ mA
		B_n, Y_n	4.5	0.77		$I_{OL} = 14$ mA
		PLH	4.5	0.7		$I_{OL} = 84$ mA
RD	Maximum Output Impedance	B_1–B_8, Y_9–Y_{13}	5.0	55	Ω	(Note 5)(Note 6)
	Minimum Output Impedance	B_1–B_8, Y_9–Y_{13}	5.0	35	Ω	(Note 5)(Note 6)
RP	Maximum Pull-Up Resistance	B_1–B_8, Y_9–Y_{13}, C_{14}–C_{17}	5.0	1650	Ω	
	Minimum Pull-Up Resistance	B_1–B_8, Y_9–Y_{13}, C_{14}–C_{17}	5.0	1150	Ω	
I_{IH}	Maximum Input Current in HIGH State	A_9–A_{13}, PLH_{IN}, HD, DIR, HLH_{IN}	5.5	1.0	μA	$V_I = 5.5V$
		C_{14}–C_{17}	5.5	100		$V_I = 5.5V$
I_{IL}	Maximum Input Current in LOW State	A_9–A_{13}, PLH_{IN}, HD, DIR, HLH_{IN}	5.5	−1.0	μA	$V_I = 0.0V$
		C_{14}–C_{17}	5.5	−5.0	mA	$V_I = 0.0V$
I_{OZH}	Maximum Output Disable Current (HIGH)	A_1—A_8	5.5	20	μA	$V_O = 5.5V$
		B_1–B_8	5.5	100		$V_O = 5.5V$
I_{OZL}	Maximum Output Disable Current (LOW)	A_1—A_8	5.5	−20	μA	$V_O = 0.0V$
		B_1–B_8	5.5	−5.0	mA	
I_{OFF}	Power Down Output Leakage	B_1–B_8, Y_9–Y_{13}, PLH	0.0	100	μA	$V_O = 5.5V$
I_{OFF}	Power Down Input Leakage	C_{14}–C_{17}, HLH_{IN}	0.0	100	μA	$V_I = 5.5V$
$I_{OFF} - I_{CC}$	Power Down Leakage to V_{CC}		0.0	250	μA	(Note 7)
I_{CC}	Maximum Supply Current		5.5	70	mA	$V_I = V_{CC}$ or GND

Note 5: Output impedance is measured with the output active LOW and active HIGH (HD = HIGH).

Note 6: This parameter is guaranteed but not tested, characterized only.

Note 7: Power-down leakage to V_{CC} is tested by simultaneously forcing all pins on the cable-side (B_1–B_8, Y_9–Y_{13}, PLH, C_{14}–C_{17} and HLH_{IN} to 5.5V and measuring the resulting I_{CC}.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V - 5.5V$ Min	$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V - 5.5V$ Max	Units	Figure Number
t_{PHL}	A_1-A_8 to B_1-B_8	2.0	30.0	ns	Figure 1
t_{PLH}	A_1-A_8 to B_1-B_8	2.0	30.0	ns	Figure 2
t_{PHL}	B_1-B_8 to A_1-A_8	2.0	30.0	ns	Figure 3
t_{PLH}	B_1-B_8 to A_1-A_8	2.0	30.0	ns	Figure 3
t_{PHL}	A_9-A_{13} to Y_9-Y_{13}	2.0	30.0	ns	Figure 1
t_{PLH}	A_9-A_{13} to Y_9-Y_{13}	2.0	30.0	ns	Figure 2
t_{PHL}	$C_{14}-C_{17}$ to $A_{14}-A_{17}$	2.0	30.0	ns	Figure 3
t_{PLH}	$C_{14}-C_{17}$ to $A_{14}-A_{17}$	2.0	30.0	ns	Figure 3
t_{SKEW}	LH-LH or HL-HL		6.0	ns	(Note 9)
t_{PHL}	PLH_{IN} to PLH	2.0	30.0	ns	Figure 1
t_{PLH}	PLH_{IN} to PLH	2.0	30.0	ns	Figure 2
t_{PHL}	HLH_{IN} to HLH	2.0	30.0	ns	Figure 3
t_{PLH}	HLH_{IN} to HLH	2.0	30.0	ns	Figure 3
t_{PHZ}	Output Disable Time	2.0	18.0	ns	Figure 7
t_{PLZ}	DIR to A_1-A_8	2.0	18.0		
t_{PZH}	Output Enable Time	2.0	25.0	ns	Figure 8
t_{PZL}	DIR to A_1-A_8	2.0	25.0		
t_{PHZ}	Output Disable Time	2.0	25.0	ns	Figure 9
t_{PLZ}	DIR to B_1-B_8	2.0	25.0		
t_{pEN}	Output Enable Time HD to B_1-B_8, Y_9-Y_{13}	2.0	28.0	ns	Figure 2
t_{pDis}	Output Disable Time HD to B_1-B_8, Y_9-Y_{13}	2.0	28.0	ns	Figure 2
$t_{pEn}-t_{pDis}$	Output Enable-Output Disable		20.0	ns	
t_{SLEW} t_{PLH} t_{PHL}	Output Slew Rate B_1-B_8, Y_9-Y_{13}	0.05 0.05	0.40 0.40	V/ns	Figure 5 Figure 4
t_r, t_f	t_{RISE} and t_{FALL} B_1-B_8, Y_9-Y_{13} (Note 8)		120 120	ns	Figure 6 (Note 10)

Note 8: Open Drain

Note 9: t_{SKEW} is measured for common edge output transitions and compares the measured propagation delay for a given path type.

(i) A_1-A_8 to B_1-B_8, A_9-Y_{13} to Y_9-Y_{13}

(ii) B_1-B_8 to A_1-A_8

(iii) $C_{14}-C_{17}$ to $A_{14}-A_{17}$

Note 10: This parameter is guaranteed but not tested, characterized only.

Capacitance (Note 11)

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0.0V$ (HD, DIR, A_9—A_{13}, C_{14}—C_{17}, PLH_{IN} and HLH_{IN})
$C_{I/O}$	I/O Pin Capacitance	12	pF	$V_{CC} = 3.3V$

Note 11: Capacitance is measured at frequency = 1 MHz.

AC Loading and Waveforms

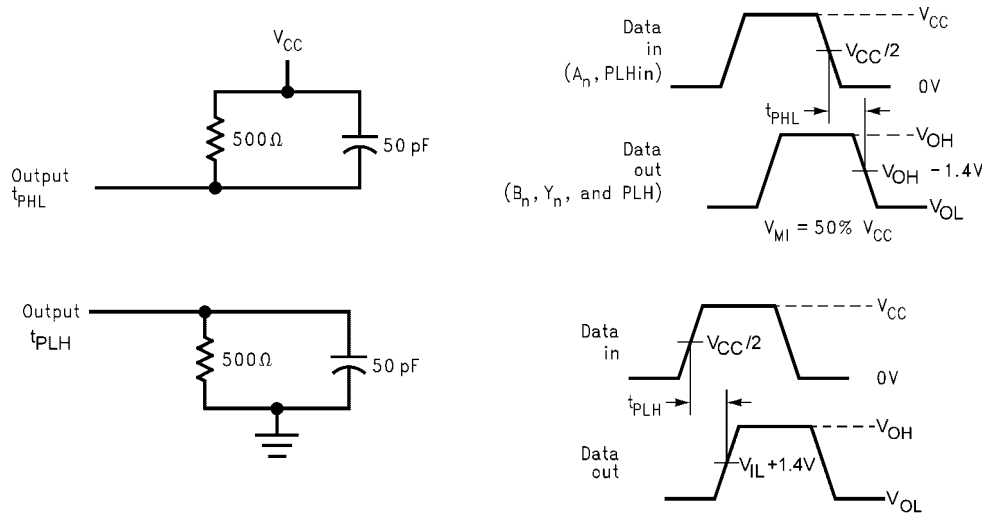Pulse Generator for all pulses: Rate $\leq$ 1.0 MHz; $Z_O \leq 50\Omega$; $t_f \leq 2.5$ ns, $t_r \leq 2.5$ ns.

FIGURE 1. Part A to B and A to Y Propagation Delay Load and Waveforms

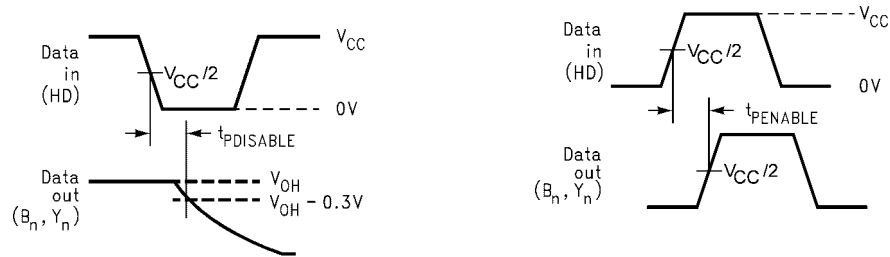

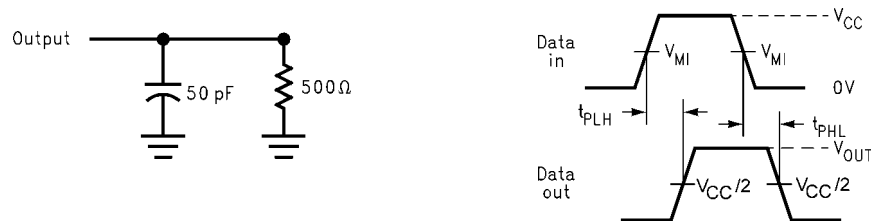**FIGURE 2. Port A to B and a to Y Output Waveforms**

FIGURE 3. Port B to A, C to A and HLHin to HLH Propagation Delay Waveforms
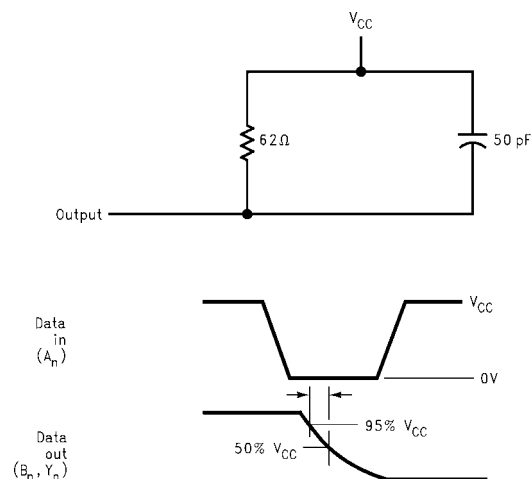
AC Loading and Waveforms (Continued)

V_{CC}

$62\,\Omega$ 50 pF

Output

Data in (A_n)

V_{CC}

0V

Data out (B_n, Y_n)

95% V_{CC}

50% V_{CC}

FIGURE 4. Port A to B and A to Y HL Slew Test Load and Waveforms

Output

$62\,\Omega$ 50 pF

Data in (A_n)

V_{CC}

0V
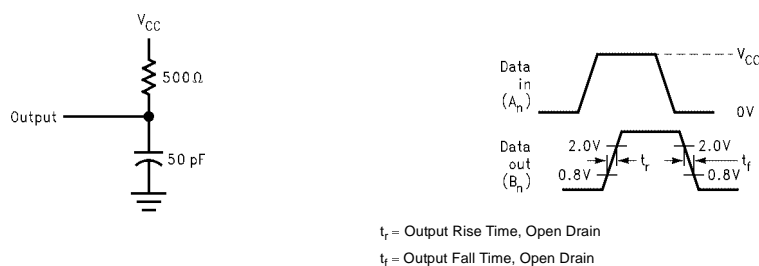
Data out (B_n, Y_n)

0.4V   1.9V (V_{CC} = 4.5V–5.5V)
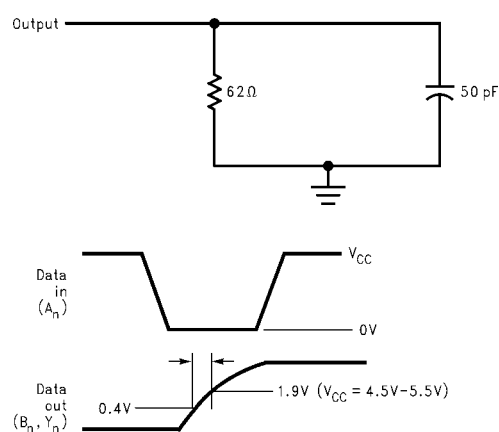
FIGURE 5. Part A to b and A to Y LH Slew Test Load and Waveforms

V_{CC}

$500\,\Omega$

Output

50 pF

Data in (A_n)

V_{CC}

0V

Data out (B_n)

2.0V   2.0V

0.8V t_r t_f 0.8V

t_r = Output Rise Time, Open Drain

t_f = Output Fall Time, Open Drain

FIGURE 6. t_{RISE} and t_{FALL} Test Load and Waveforms for Open Drain Outputs
A_1–A_8 to B_1–B_8, A_9–A_{13} to Y_9–Y_{13}

AC Loading and Waveforms (Continued)

V_CC x2 for t_PLZ
GND for t_PHZ

500Ω

A_1 – A_8

500Ω   50 pF
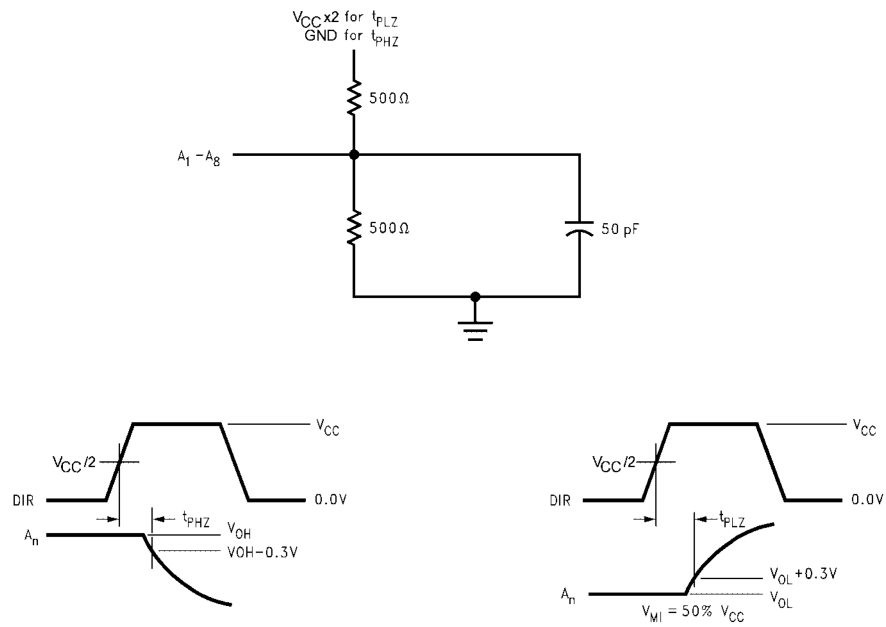
FIGURE 7. t_{PHZ} and t_{PLZ} Test Load and Waveforms, DIR to $A_1–A_8$

V_CC x2 for t_PZL
GND for t_PZH

500Ω

A_1 – A_8

500Ω   50 pF
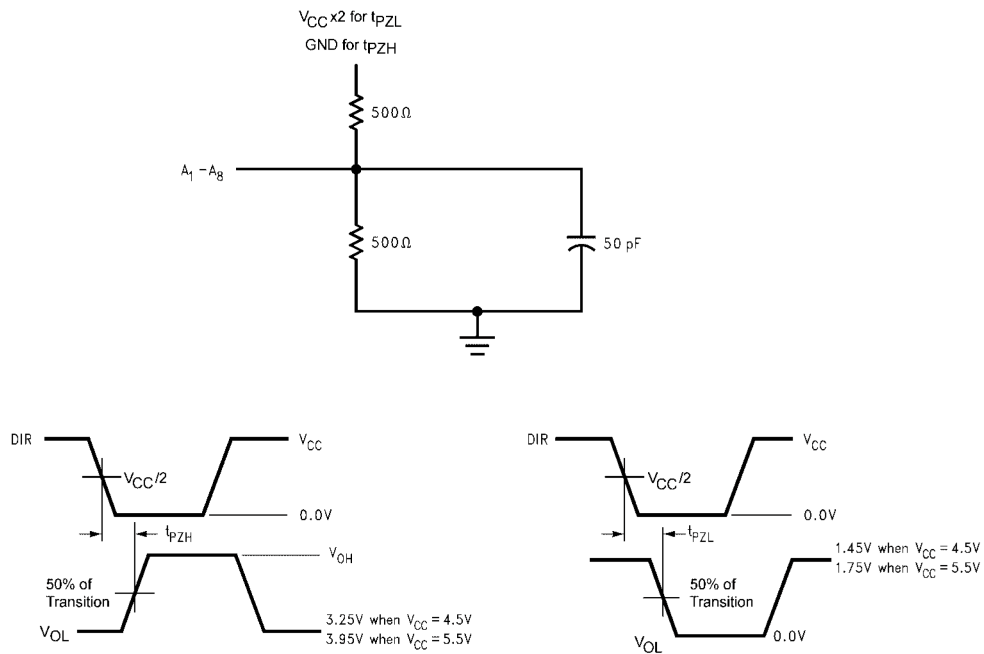
FIGURE 8. t_{PZH} and t_{PZL} Test Load and Waveforms, DIR to $A_1–A_8$

AC Loading and Waveforms (Continued)

FIGURE 9. t_{PHZ} and t_{PLZ} Test Load and Waveforms, DIR to B_1–B_8

74VHC161284

Physical Dimensions inches (millimeters) unless otherwise noted

0.620 − 0.630
[15.75 − 16.00]
− A −

48   25

LEAD #1
IDENT

0.398 − 0.417
[10.10 − 10.60]
⊘ 0.010[0.25] C B Ⓢ A Ⓢ

0.291 − 0.299
[7.40 − 7.59]
− B −

1   24

0.025
[0.635] TYP

0.020±0.003
[0.51 ± 0.08]
TYP

0.008 − 0.012
[0.21 − 0.30] TYP

⊘ 0.0031[0.08] Ⓜ C A Ⓢ B Ⓢ

GAUGE PLANE
0.010
[0.25]

0.005 − 0.009
[0.13 − 0.22]

0.020 − 0.040
[0.51 − 1.01]

DETAIL E TYP

0.096 − 0.108
[2.44 − 2.74]

SEATING PLANE

45° x 0.015 − 0.025
[0.39 − 0.63]

SEE DETAIL E

− D −
− C −

0.025
[0.635] TYP

0.10
[0.25] MIN TYP

0° − 8° TYP

△ 0.004[0.10]

MS48A (REV E)

**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ED, DATE 4/97.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48REVC

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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