

CM1692

Praetorian® L-C LCD and Camera EMI Filter Array with ESD Protection

Features

- Four, Six and Eight Channels of EMI Filtering with Integrated ESD Protection
- Pi-Style EMI Filters in a Capacitor–Inductor–Capacitor (C–L–C) Network
- ± 15 kV ESD Protection on Each Channel (IEC 61000–4–2 Level 4, Contact Discharge)
- Greater than 30 dB Attenuation (Typical) at 1 GHz
- 0.50 mm Thick μ DFN Package with 0.40 mm Lead Pitch:
 - ♦ 4–channel = 8–lead μ DFN
 - ♦ 6–channel = 12–lead μ DFN
 - ♦ 8–channel = 16–lead μ DFN
- Tiny μ DFN Package Size:
 - ♦ 8–lead: 1.70 mm x 1.35 mm
 - ♦ 12–lead: 2.50 mm x 1.35 mm
 - ♦ 16–lead: 3.30 mm x 1.35 mm
- These Devices are Pb–Free and are RoHS Compliant

Applications

- LCD and Camera Data Lines in Mobile Handsets
- Wireless Handsets
- LCD and Camera Modules



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UDFN8
DE SUFFIX
CASE 517BC

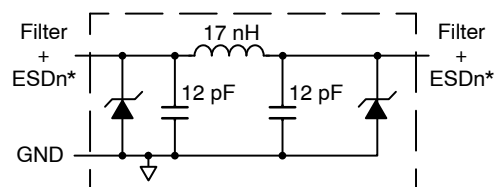


UDFN12
DE SUFFIX
CASE 517BD



UDFN16
DE SUFFIX
CASE 517BE

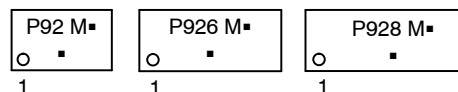
ELECTRICAL SCHEMATIC



1 of 4, 6 or 8 EMI/RFI Filter Channels
with Integrated ESD Protection

* See Package/Pinout Diagrams for expanded pin information.

MARKING DIAGRAM



P92 = CM1692–04DE
P926 = CM1692–06DE
P928 = CM1692–08DE
M = Date Code
■ = Pb–Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
CM1692–04DE	μ DFN–8 (Pb–Free)	3000/Tape & Reel
CM1692–06DE	μ DFN–12 (Pb–Free)	3000/Tape & Reel
CM1692–08DE	μ DFN–16 (Pb–Free)	3000/Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

CM1692

PACKAGE / PINOUT DIAGRAMS

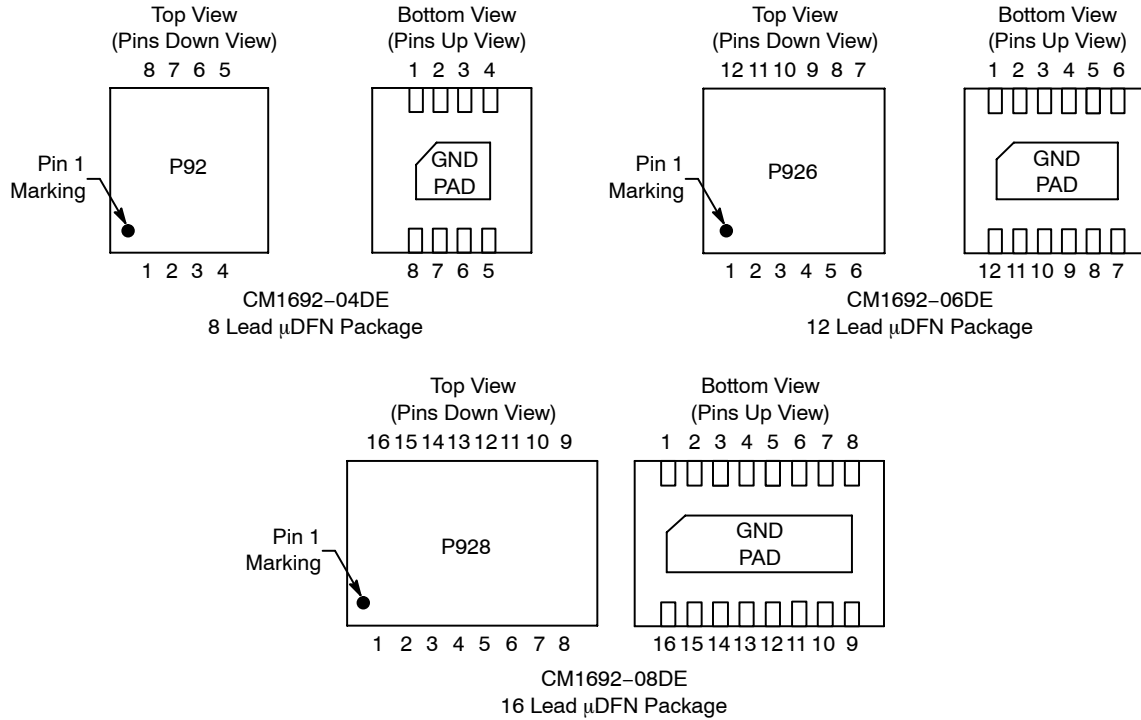


Table 1. PIN DESCRIPTIONS

Device Pin(s)			Name	Description	Device Pin(s)			Name	Description
-04	-06	-08			-04	-06	-08		
1	1	1	FILTER1	Filter + ESD Channel 1	8	12	16	FILTER1	Filter + ESD Channel 1
2	2	2	FILTER2	Filter + ESD Channel 2	7	11	15	FILTER2	Filter + ESD Channel 2
3	3	3	FILTER3	Filter + ESD Channel 3	6	10	14	FILTER3	Filter + ESD Channel 3
4	4	4	FILTER4	Filter + ESD Channel 4	5	9	13	FILTER4	Filter + ESD Channel 4
-	5	5	FILTER5	Filter + ESD Channel 5	-	8	12	FILTER5	Filter + ESD Channel 5
-	6	6	FILTER6	Filter + ESD Channel 6	-	7	11	FILTER6	Filter + ESD Channel 6
-	-	7	FILTER7	Filter + ESD Channel 7	-	-	10	FILTER7	Filter + ESD Channel 7
-	-	8	FILTER8	Filter + ESD Channel 8	-	-	9	FILTER8	Filter + ESD Channel 8
GND PAD			GND	Device Ground	-	-	-	-	

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Storage Temperature Range	-65 to +150	°C
Current per Inductor	30	mA
DC Package Power Rating	500	mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Operating Temperature Range	-40 to +85	°C

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
L	Channel Inductance			17		nH
C _{TOTAL}	Total Channel Capacitance	At 2.5 V DC Reverse Bias, 1 MHz, 30 mV AC	18.8	23.5	28.2	pF
C	Capacitance C1	At 2.5 V DC Reverse Bias, 1 MHz, 30 mV AC		11.8		pF
V _{DIODE}	Stand-off Voltage	I _{DIODE} = 10 μ A		6.0		V
I _{LEAK}	Diode Leakage Current (Reverse Bias)	V _{DIODE} = 3.3 V		0.1	1.0	μ A
V _{SIG}	Signal Clamp Voltage Positive Clamp Negative Clamp	(Note 3) I _{LOAD} = 10 mA I _{LOAD} = -10 mA	5.6 -1.5	6.8 -0.8	9.0 -0.4	V
V _{ESD}	In-system ESD Withstand Voltage Contact Discharge per IEC 61000-4-2 Standard, Level 4	(Notes 2 and 3)	± 15			kV
R _{DYN}	Dynamic Resistance Positive Negative			2.3 0.9		Ω
f _C	Roll-off Frequency at -6 dB Attenuation Z _{SOURCE} = 50 Ω , Z _{LOAD} = 50 Ω			400		MHz

1. T_A = 25°C unless otherwise specified.
2. ESD applied to input and output pins with respect to GND, one at a time.
3. Clamping voltage is measured at the opposite side of the EMI filter to the ESD pin (i.e. if ESD is applied to pin A1 then clamping voltage is measured at pin C1). Unused pins are left open.

PERFORMANCE INFORMATION

Typical Diode Capacitance vs. Input Voltage

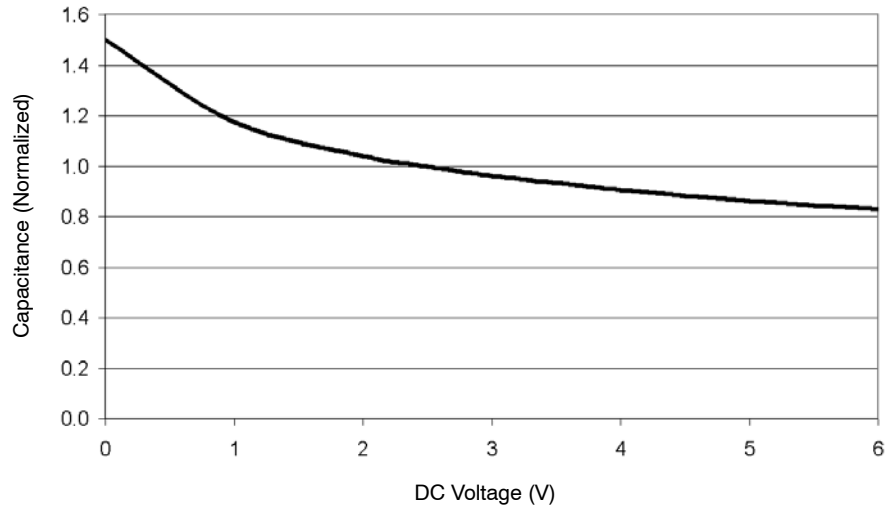


Figure 1. Filter Capacitance vs. Input Voltage
(normalized to capacitance at 2.5 V DC and 25°C)

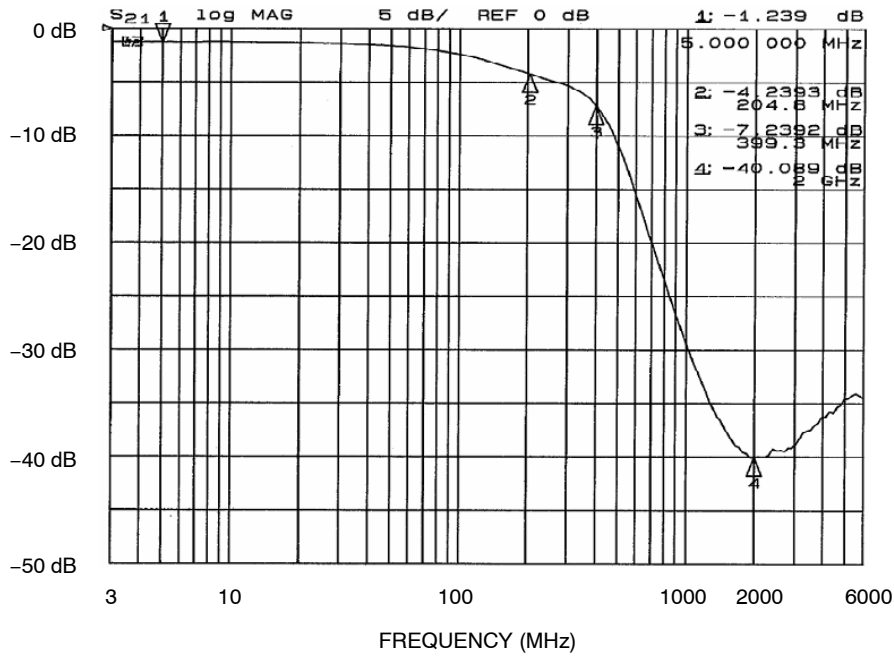


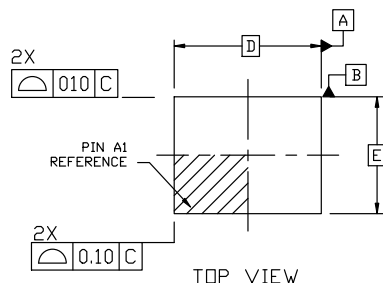
Figure 2. Typical Performance Curve



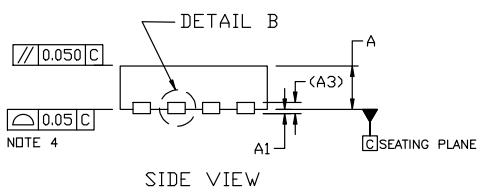
SCALE 4:1

UDFN8, 1.7x1.35, 0.4P
CASE 517BC
ISSUE A

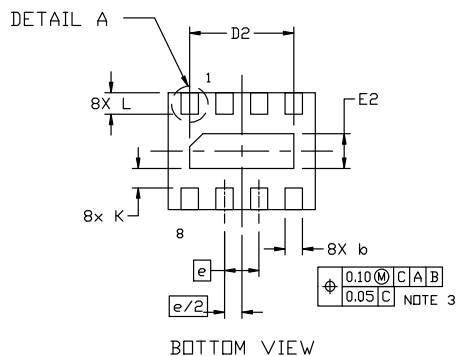
DATE 11 AUG 2022



TOP VIEW



SIDE VIEW



BOTTOM VIEW

GENERIC MARKING DIAGRAMS*

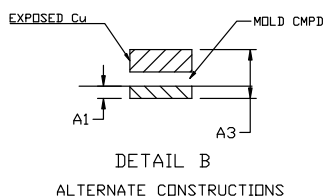
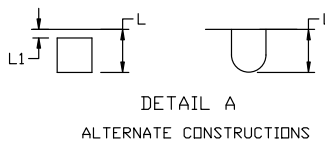
XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

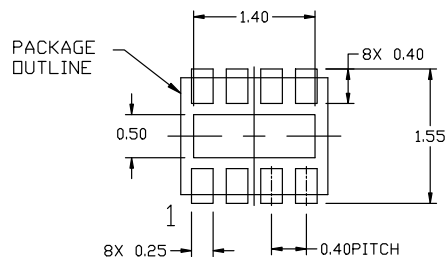
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2004.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.


DETAIL B
ALTERNATE CONSTRUCTIONS

DETAIL A
ALTERNATE CONSTRUCTIONS

DIM	MILLIMETERS	
	MIN.	MAX.
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.70 BSC	
D2	1.10	1.30
E	1.35 BSC	
E2	0.30	0.50
e	0.40 BSC	
K	0.15	---
L	0.20	0.30
L1	---	0.05



RECOMMENDED MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

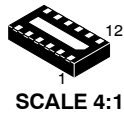
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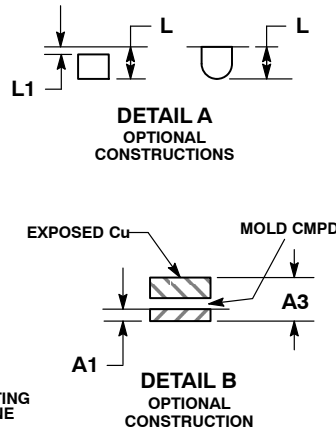
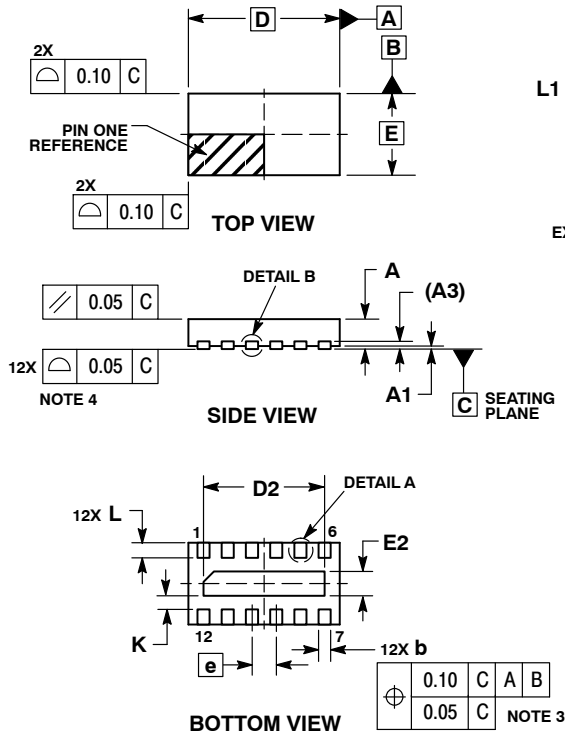
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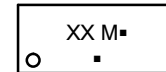

UDFN12, 2.5x1.35, 0.4p
CASE 517BD
ISSUE O

DATE 18 NOV 2009


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.
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MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	2.50	BSC
D2	1.90	2.10
E	1.35	BSC
E2	0.30	0.50
e	0.40	BSC
K	0.15	---
L	0.20	0.30
L1	---	0.05

GENERIC MARKING DIAGRAM*


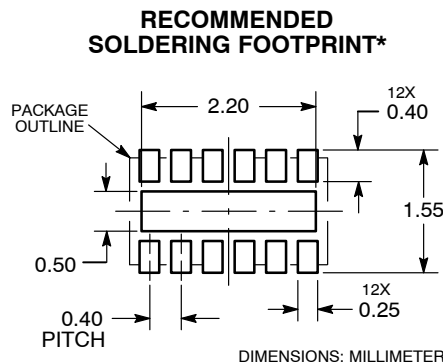
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- XX = Specific Device Code
- M = Month Code
- = Pb-Free Package

(Note: Microdot may be in either location)

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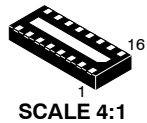
Pb-Free indicator, "G" or microdot "■", may or may not be present.



*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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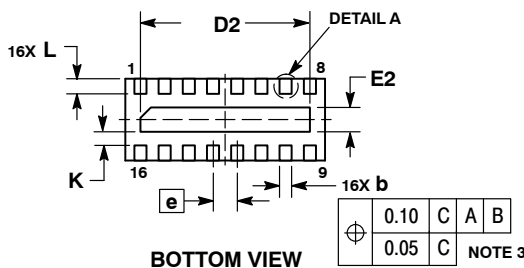
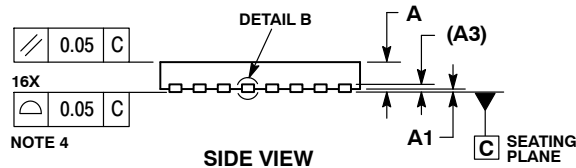
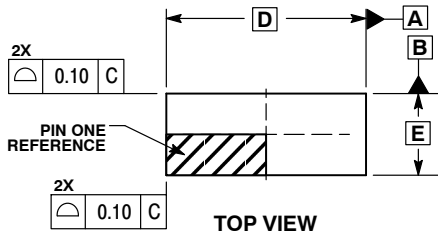
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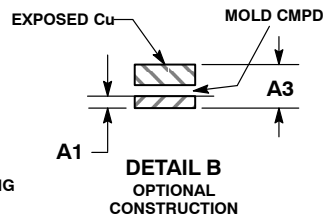
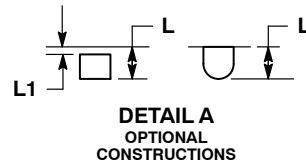
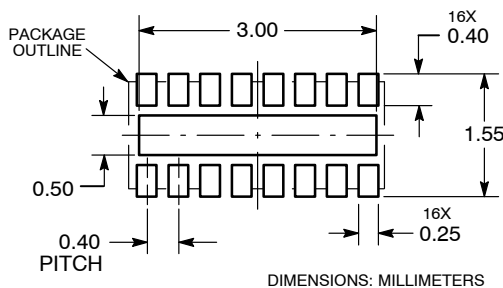
UDFN16, 3.3x1.35, 0.4P

CASE 517BE
ISSUE O

DATE 18 NOV 2009



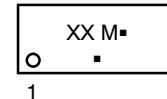
RECOMMENDED SOLDERING FOOTPRINT*



- NOTES:
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A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	3.30	BSC
D2	2.70	2.90
E	1.35	BSC
E2	0.30	0.50
e	0.40	BSC
K	0.15	---
L	0.20	0.30
L1	---	0.05

GENERIC MARKING DIAGRAM*



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