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Kind regards,

Team Nexperia



PH6325L

N-channel 25 V 6.3 mΩ logic level MOSFET in LPAK

Rev. 2 — 22 December 2011

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology

1.2 Features and benefits

- Low thermal resistance
- Low threshold voltage
- Optimized for use in DC-to-DC converters
- Very low switching and conduction losses

1.3 Applications

- DC-to-DC convertors
- Notebook computers
- Switched-mode power supplies
- Voltage regulators

1.4 Quick reference data

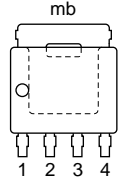
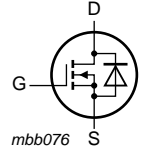
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}$	-	-	25	V
I_D	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1 ; see Figure 3	-	-	78.7	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ see Figure 2	-	-	62.5	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ see Figure 9 ; see Figure 10	-	7.4	9.5	mΩ
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ see Figure 9 ; see Figure 10	-	4.7	6.3	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; V_{DS} = 12\text{ V};$ see Figure 11 ; see Figure 12	-	3.3	-	nC
$Q_{G(tot)}$	total gate charge		-	13.3	-	nC



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>SOT669 (LFAK; Power-SO8)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PH6325L	LFAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

4. Limiting values

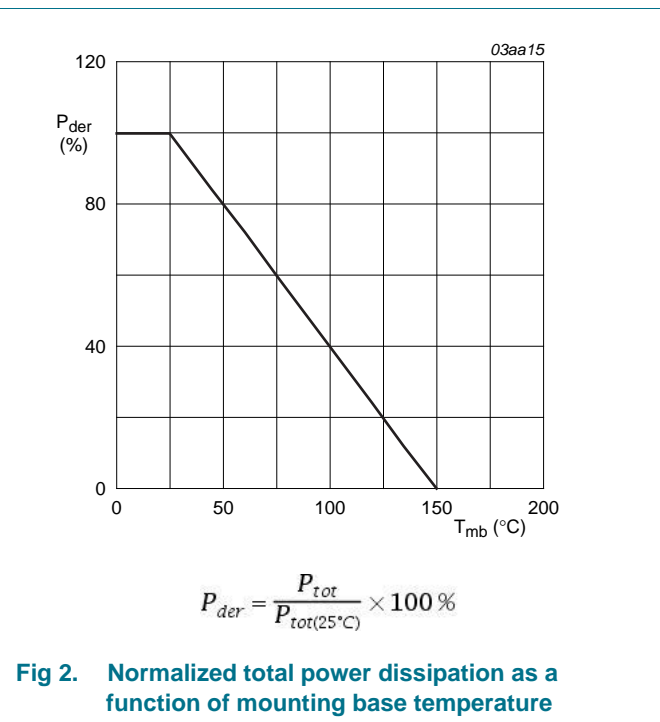
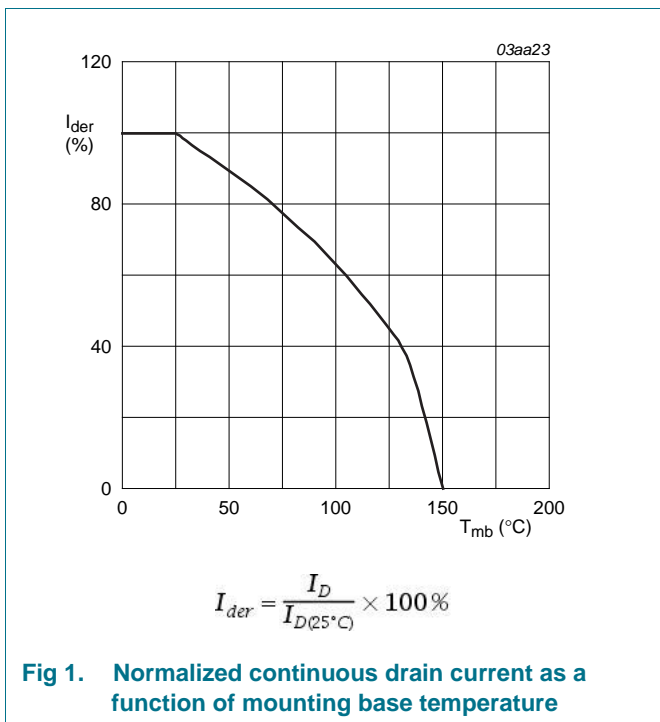
Table 4. Limiting values

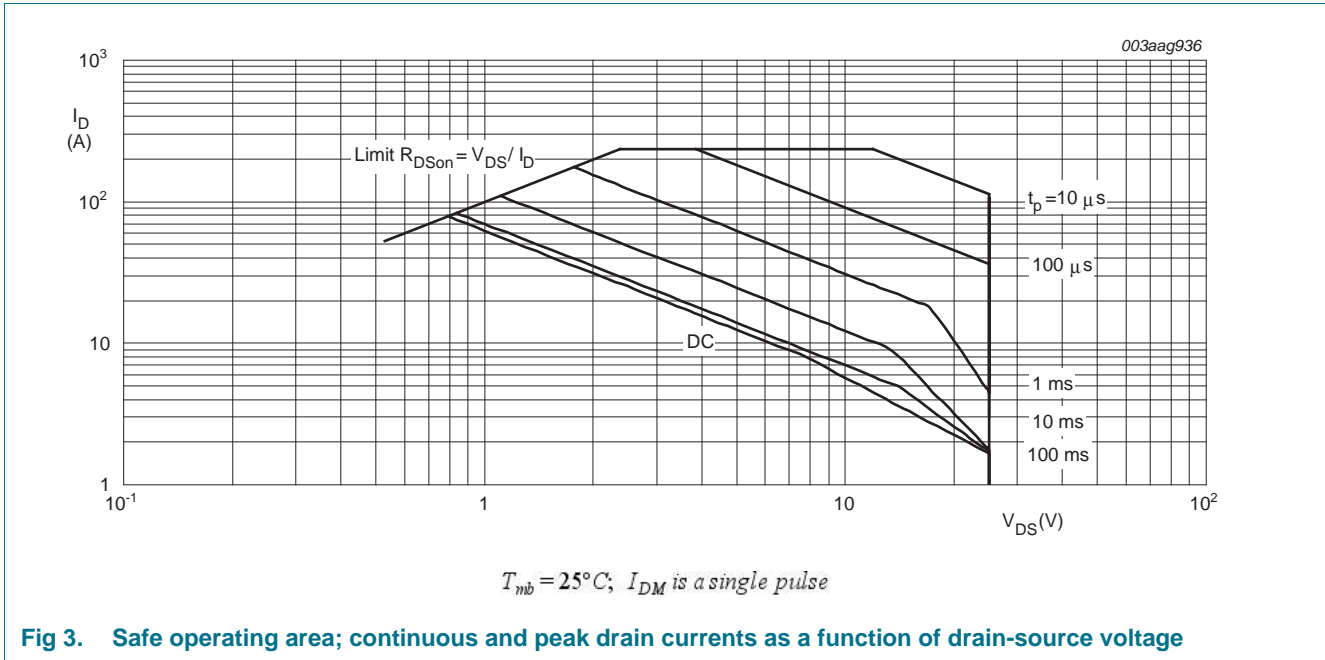
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 150 °C	-	25	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; see Figure 1	-	49.6	A
		V _{GS} = 10 V; T _{mb} = 25 °C; see Figure 1 ; see Figure 3	-	78.7	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; see Figure 3	-	236	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	62.5	W
T _{stg}	storage temperature		-55	150	°C
T _j	junction temperature		-55	150	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	52	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	208	A
Avalanche ruggedness					
E _{DS(AL)R}	repetitive drain-source avalanche energy	t _p = 0.015 ms; unclamped; R _{GS} = 50 Ω; I _D = 3.4 A; [1][2]	-	1.2	mJ
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 34 A; V _{DD} = 25 V; t _p = 0.15 ms; unclamped; R _{GS} = 50 Ω	-	115	mJ

[1] Duty cycle is limited by the maximum junction temperature.

[2] Repetitive avalanche failure is not determined simply by thermal effects. Repetitive avalanche transients should only be applied for short bursts, not every switching cycle.





5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	2	K/W

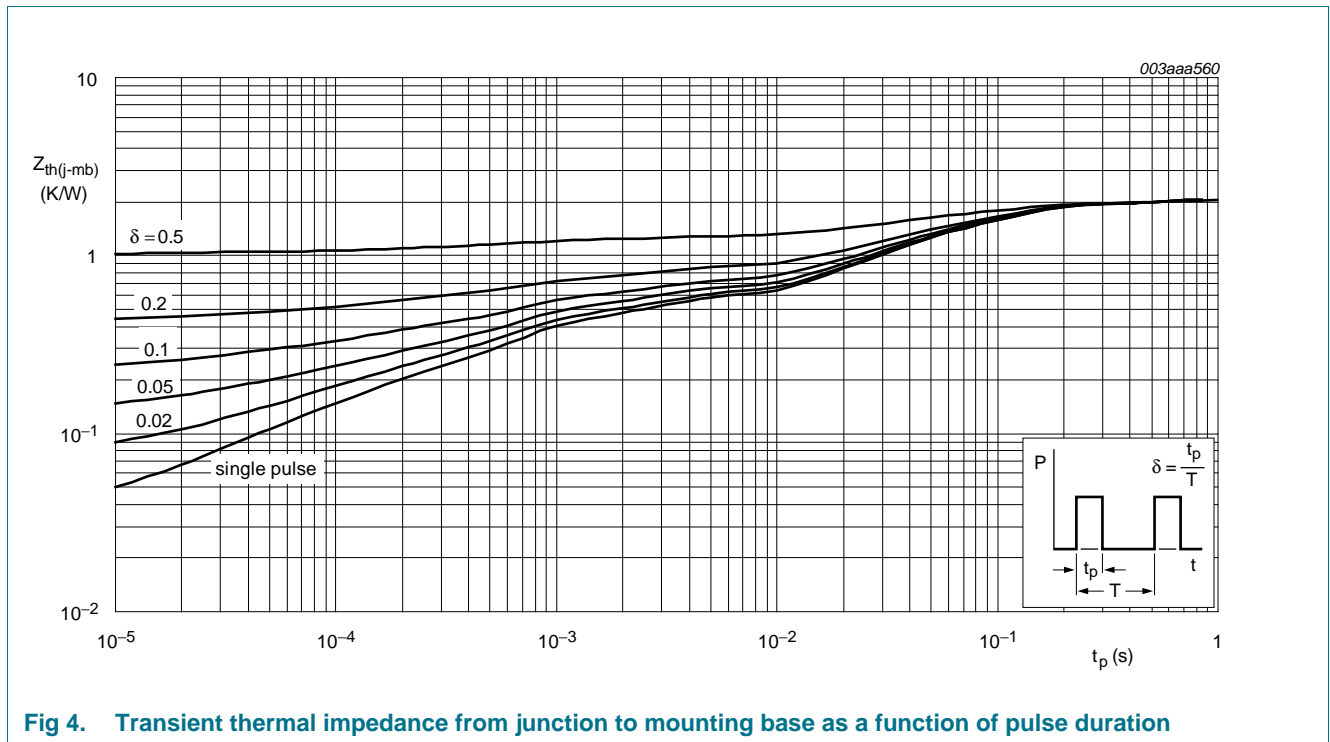


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	25	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = -55 \text{ }^\circ\text{C}$; see Figure 7 ; see Figure 8	-	-	2.2	V
		$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 150 \text{ }^\circ\text{C}$; see Figure 7 ; see Figure 8	0.5	-	-	V
		$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 7 ; see Figure 8	1	1.5	2	V
I_{DSS}	drain leakage current	$V_{DS} = 25 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	0.06	1	μA
		$V_{DS} = 25 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 150 \text{ }^\circ\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = -16 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}$; $I_D = 25 \text{ A}$; $T_j = 150 \text{ }^\circ\text{C}$; see Figure 9 ; see Figure 10	-	7.5	10.1	mΩ
		$V_{GS} = 4.5 \text{ V}$; $I_D = 25 \text{ A}$; $T_j = 150 \text{ }^\circ\text{C}$; see Figure 9 ; see Figure 10	-	11.8	15.2	mΩ
		$V_{GS} = 4.5 \text{ V}$; $I_D = 25 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 9 ; see Figure 10	-	7.4	9.5	mΩ
		$V_{GS} = 10 \text{ V}$; $I_D = 25 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 9 ; see Figure 10	-	4.7	6.3	mΩ
R_G	internal gate resistance	$f = 1 \text{ MHz}$	-	1.8	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}$; $V_{DS} = 12 \text{ V}$; $V_{GS} = 4.5 \text{ V}$; see Figure 11 ; see Figure 12	-	13.3	-	nC
		$I_D = 0 \text{ A}$; $V_{DS} = 0 \text{ V}$; $V_{GS} = 4.5 \text{ V}$	-	11.1	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}$; $V_{DS} = 12 \text{ V}$; $V_{GS} = 4.5 \text{ V}$; see Figure 11 ; see Figure 12	-	4.9	-	nC
Q_{GS1}	pre-threshold gate-source charge		-	2.6	-	nC
Q_{GS2}	post-threshold gate-source charge		-	2.3	-	nC
Q_{GD}	gate-drain charge		-	3.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}$; $V_{DS} = 12 \text{ V}$; see Figure 11 ; see Figure 12	-	2.4	-	V
C_{iss}	input capacitance	$V_{DS} = 0 \text{ V}$; $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ\text{C}$	-	2420	-	pF
		$V_{DS} = 12 \text{ V}$; $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 13 ; see Figure 14	-	1871	-	pF
C_{oss}	output capacitance	$T_j = 25 \text{ }^\circ\text{C}$; see Figure 13 ; see Figure 14	-	517	-	pF
C_{rss}	reverse transfer capacitance		-	179	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12 \text{ V}$; $V_{GS} = 4.5 \text{ V}$; $R_{G(ext)} = 4.7 \text{ } \Omega$; $I_D = 25 \text{ A}$	-	25	-	ns
t_r	rise time		-	25	-	ns
$t_{d(off)}$	turn-off delay time		-	32	-	ns
t_f	fall time		-	12	-	ns

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$;	-	33	-	ns
Q_r	recovered charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$	-	13	-	nC

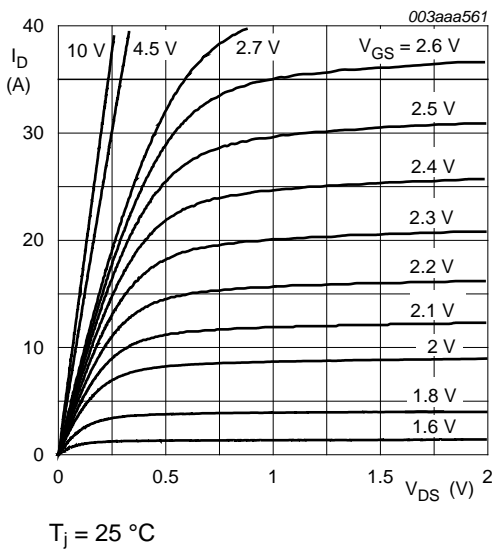


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

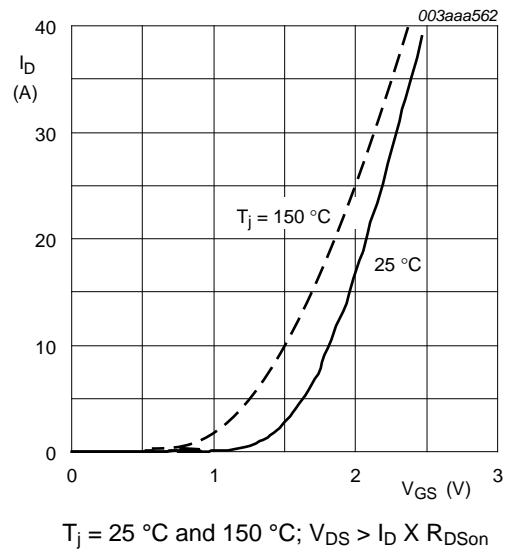


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

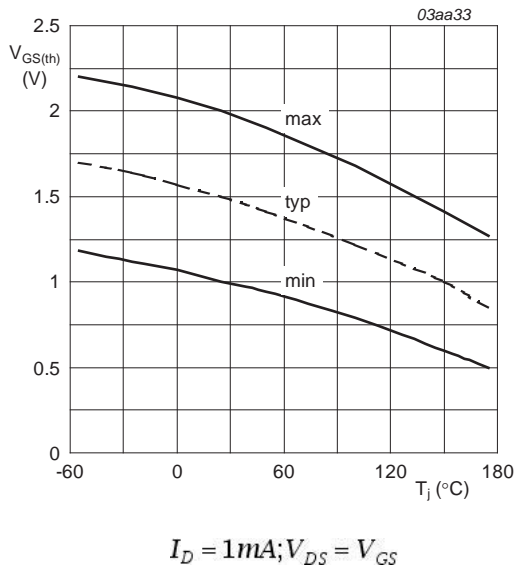


Fig 7. Gate-source threshold voltage as a function of junction temperature

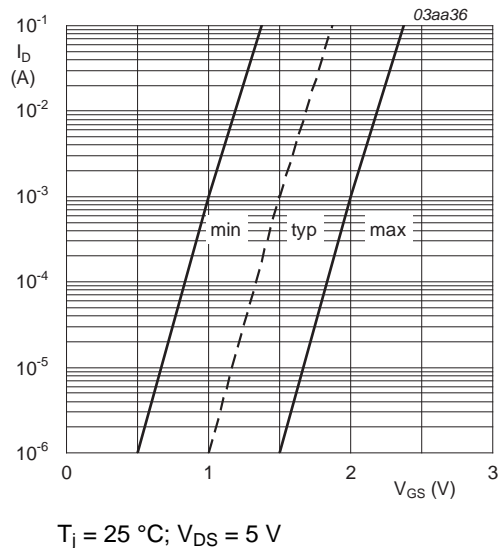
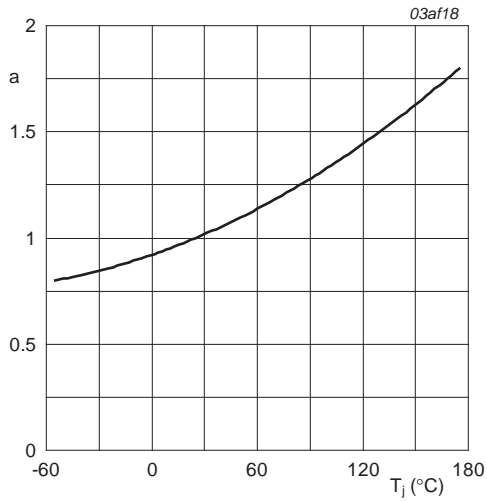
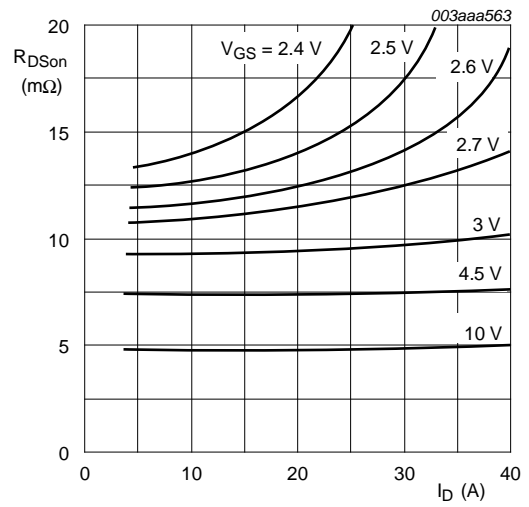


Fig 8. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C

Fig 10. Drain-source on-state resistance as a function of drain current; typical values

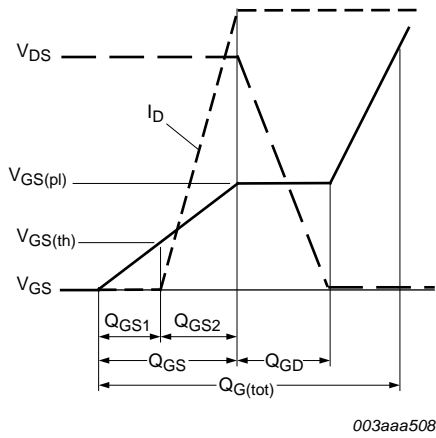
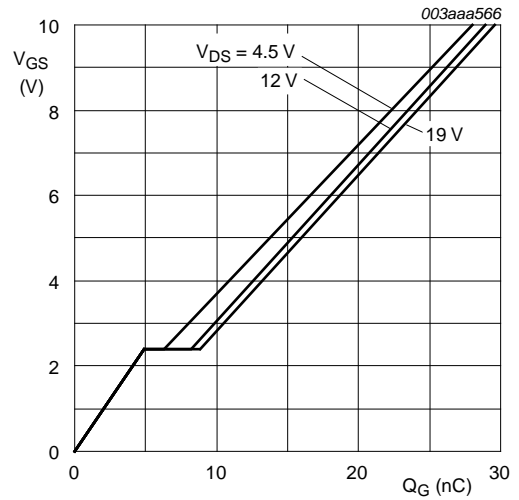


Fig 11. Gate charge waveform definitions



I_D = 25 A; V_{DS} = 4.5 V, 12 V and 19 V

Fig 12. Gate-source voltage as a function of gate charge; typical values

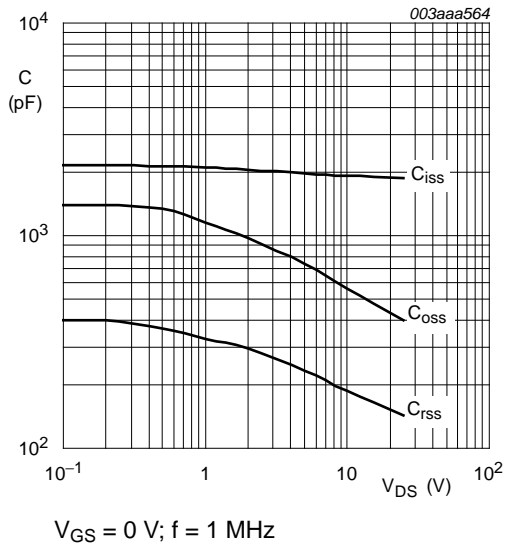


Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

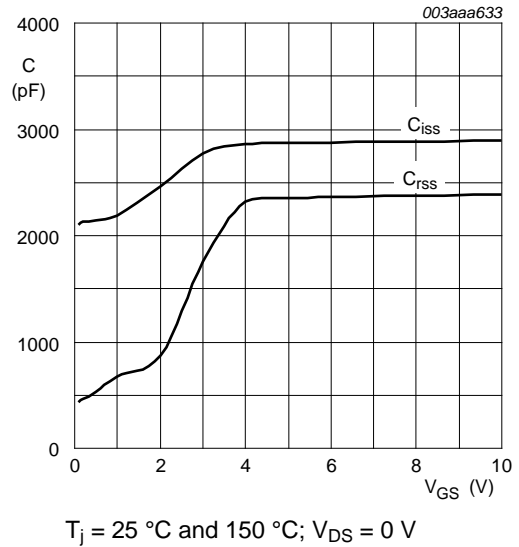


Fig 14. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

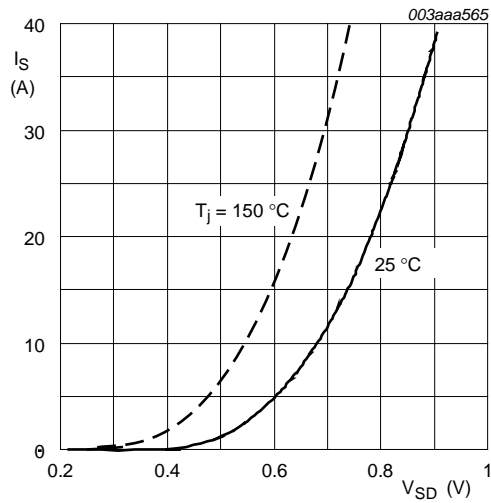


Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK; Power-SO8); 4 leads

SOT669

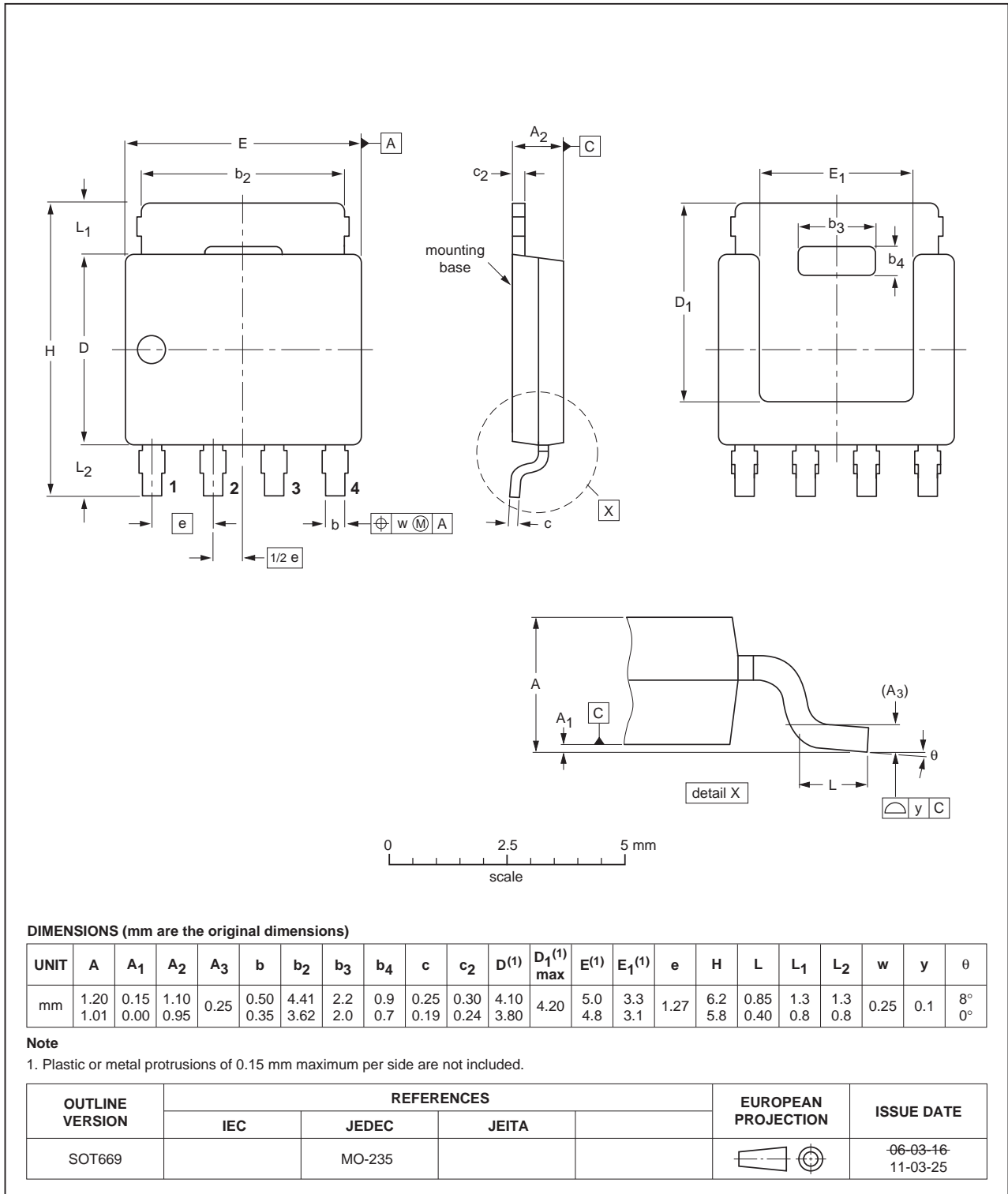


Fig 16. Package outline SOT669 (LPAK; Power-SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH6325L v.2	20111222	Product data sheet	-	PH6325L v.1
Modifications:	<ul style="list-style-type: none">• The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.• Status changed from preliminary to product.			
PH6325L v.1	20040428	Preliminary data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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