DSP Development Kit, Cyclone III Edition

from Intel

The DSP Development Kit, Cyclone® III Edition delivers a complete digital signal processing (DSP) development environment. The kit facilitates the entire design process from design conception through hardware implementation. The DSP Development Kit, Cyclone III Edition includes the Cyclone III development board, the data conversion high-speed mezzanine card (HSMC), Quartus® II development software, MATLAB/Simulink evaluation software, evaluation intellectual property (IP) cores, design examples, power supplies, cables, and documentation. For further DSP-based design productivity, the DSP Builder development tool is available separately.

- Ordering information
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Ordering Information

Table 1 provides the ordering code and pricing information for the DSP Development Kit, Cyclone III Edition.

Table 1. DSP Dev Kit, Cyclone III Edition Ordering Code and Pricing Information

Ordering Code	Price	Ordering Information
DK-DSP-3C120N	Buy Now	In North America, call 1-888-800-0631. For international sales, contact your local distributor.

Notes:
Buyer represents that it is a product developer, software developer or system integrator and acknowledges that this product is an evaluation kit that is not FCC authorized, is made available solely for evaluation and software development, and may not be resold.

Table 2 provides information for finding HSMC-based daughtercards, adapters, and cables.

Table 2. Optional HSMC Interface-Compatible Daughtercards, Adapters, or Cables

Product Name	Type	Vendor	Host Board	Price/Availability
More than 15 different choices	HSMC compatible accessories	Various	Cyclone III FPGA-based boards	As low as

Development Kit Contents

The DSP Development Kit, Cyclone III Edition features:

- Cyclone III Development Board
  - Featured device
    - Cyclone III EP3C120F780 FPGA
  - Display and general user input/output
    - 128 x 64 graphics LCD
    - 2-line x 16-character LCD
    - Buttons, dip-switches, LEDs, 7-segment display, speaker header
  - Memory
    - 256 megabytes (MB) of dual-channel DDR2 SDRAM with error correction code (ECC)
    - 8 MB of synchronous SRAM
    - 64 MB of flash
  - Components and interfaces
    - 10/100/1000 Ethernet (RGMII)

        - USB 2.0 (Type B)
        - Two HSMC connectors
    - Power and data converters
        - LT1963AES8: 2.5 to 1.5-A, low noise, fast transient response LDO regulators
        - LT1963AES8: 1.5-A, low noise, fast transient response LDO regulators
        - LT3481EDD: 36-V, 2-A, 2.8-MHz step-down switching regulator with 50-µA quiescent current
        - LT1761ES5-SD: 100-mA, low noise, LDO micropower regulators in SOT-23
        - LTC3418EUHF: 8-A, 4-MHz, monolithic synchronous step-down regulator
        - LTM4601EV: 12-A DC/DC µModule
        - LT1931AES5: 1.2/2.2-MHz inverting DC/DC converters in ThinSOT
        - LTC2402CMS: 1/2-Channel, 24-bit µPower no latency delta-sigma ADC in MSOP-10
- Data conversion HSMC
    - Dual 14-bit, 150-MSPS A/D converter
    - Dual 14-bit, 250-MSPS D/A converter
    - Audio in/out/mic
- Cyclone III FPGA Development Kit, CD-ROM
    - Design examples for the Cyclone III FPGA development board
    - Complete documentation
        - User guide
        - Reference manual
        - Board schematic and layout
        - Bill of materials (BOM)
        - Product and partner information
- MATLAB/Simulink evaluation software
- Intel® Complete Design Suite (download from Intel Download Center)
    - Quartus II design software
        - Subscription Edition (optional feature, available for purchase)
        - Web Edition (no charge, Windows only)
    - ModelSim®-Intel software
        - Intel Edition (optional feature, available for purchase)
        - Web Edition (no charge, Windows only)
    - MegaCore® IP Library including Nios® II processor —OpenCore Plus evaluation
    - Nios II Embedded Design Suite, Evaluation Edition (free)
    - Video demos of Quartus II software and the Nios II processor
    - System reference designs and labs
        - DSP Builder filtering design
        - Nios II processor reference designs

HSMC Interface

Intel developed the specification for the HSMC, which is based on the Samtec mechanical connector, to define and standardize the interface between optional daughtercards and host boards. This specification outlines both the electrical and mechanical properties of the interface between daughtercard and host. You can also create your own HSMC interface compatible daughtercards.

- Download High Speed Mezzanine Card (HSMC) Specification (PDF)

Figure 1. Cyclone III FPGA Development Board

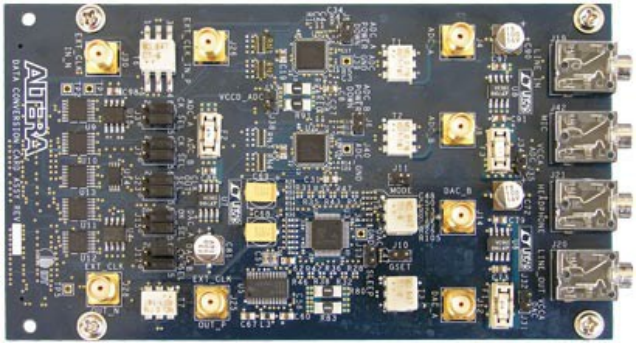

Figure 2. Cyclone III Data Conversion HSMC

Available Documentation

Table 3. Documents Available for the DSP Development Kit, Cyclone III Edition

Document	Description	Version
Kit Installation (via FTP)	**(Updated)** Full installation of all files including reference manual, user guide, quick start guide, demos and tutorials, BOM, layout, PCB, schematics, Board Update Portal example file, Board Test System example file, and others	12.1.0 (1)
Kit Installation (via FTP)	**(Archive)** Full installation of all files including reference manual, user guide, quick start guide, demos and tutorials, BOM, layout, PCB, schematics, Board Update Portal example file, Board Test System example file, and others	12.0.0 (2)
Kit Installation (via FTP)	**(Archive)** Full installation of all files including reference manual, user guide, quick start guide, demos and tutorials, BOM, layout, PCB, schematics, Board Update Portal example file, Board Test System example file, and others	11.1.0 (3)
Kit Installation (via FTP)	**(Archive)** Full installation of all files including reference manual, user guide, quick start guide, demos and tutorials, BOM, layout, PCB, schematics, Board Update Portal example file, Board Test System example file, and others	11.0.0 (4)
Kit Installation (via FTP)	**(Archive)** Full installation of all files including reference manual, user guide, quick start guide, demos and tutorials, BOM, layout,PCB, schematics, Board Update Portal example file, Board Test System example file, and others	7.2.0 (5)

Notes:

1. This kit installation works with Quartus II design software version 12.1.0.
2. This kit installation works with Quartus II design software version 12.0.0.
3. This kit installation works with Quartus II design software version 11.1.0.
4. This kit installation works with Quartus II design software version 11.0.0.
5. This kit installation works with Quartus II design software version 7.2.0

Errata

There are two known errata on this development kit. The problems are with the on-board power monitor circuitry and a reset issue with the embedded USB-Blaster™ circuitry. Both bugs can be fixed by downloading an updated MAX® II CPLD programming file.

To see if your board needs the updated programming file press and hold the CPU_RESET pushbutton. If the Power Display does not show “1337” or higher or it shows nothing at all, then your board should be upgraded to the new programming file. Click here to download a zip file containing the files need to upgrade your board. Follow the instructions in the **max2_upgrade_instructions.txt** text file.

Related Links

- Other Cyclone III FPGA-based development kits
- AN 466: Cyclone III Design Guidelines (PDF)

- Quartus II design software
- Literature for low-cost Cyclone III FPGAs
- Nios II 32-bit embedded processor solutions
- DSP in Cyclone III FPGAs
- Power Management Center for Altera devices