DATA SHEET
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MOSFET - Power, Single N-Channel, DFN5/DFNW5

30 V, 6.0 mΩ, 51 A

NVMFS4C310N

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- AEC−Q101 Qualified and PPAP Capable
- NVMFS4C310NWF − Wettable Flanks Option for Enhanced Optical Inspection
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

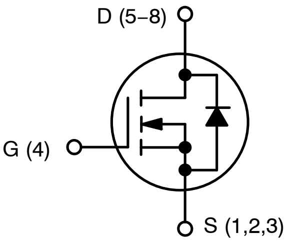
MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2 and 4)	Steady State	T_A = 25°C	I_D	17	A
		T_A = 100°C		12	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2 and 4)		T_A = 25°C	P_D	3.5	W
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3 and 4)		T_C = 25°C	I_D	51	A
		T_C = 100°C		36	
Power Dissipation $R_{\theta JC}$ (Notes 1, 2, 3 and 4)		T_C = 25°C	P_D	32	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 µs		I_{DM}	132	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to +175	°C
Source Current (Body Diode)			I_S	21	A
Single Pulse Drain−to−Source Avalanche Energy (I_L = 25 A_{pk}) (Note 3)			E_{AS}	31	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

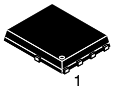
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using 650 mm^2, 2 oz Cu pad.
3. Assumes heat−sink sufficiently large to maintain constant case temperature independent of device power.
4. Continuous DC current rating. Maximum current for pulses as long as one second is higher but dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
30 V	6.0 mΩ @ 10 V	51 A
	9.0 mΩ @ 4.5 V	

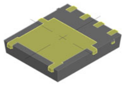


N−CHANNEL MOSFET

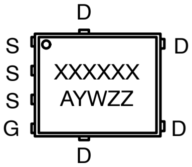
MARKING DIAGRAM



DFN5
CASE 488AA



DFNW5
CASE 507BA



4C10N = Specific Device Code for NVMFS4C310N
4C10WF= Specific Device Code of NVMFS4C310NWF
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceabililty

ORDERING INFORMATION

Device	Package	Shipping[†]
NVMFS4C310NT1G	DFN5 (Pb−Free)	1500 / Tape & Reel
NVMFS4C310NWFT1G	DFNW5 (Pb−Free)	1500 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Drain)	$R_{\theta JC}$	4.7	°C/W
Junction−to−Ambient – Steady State (Note 5)	$R_{\theta JA}$	43	

5. Surface−mounted on FR4 board using 650 mm^2, 2 oz Cu pad.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				14.5		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1.0	µA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 6)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 µA		1.3		2.2	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				4.7		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 30 A		5.0	6.0	mΩ
		V_{GS} = 4.5 V	I_D = 30 A		7.5	9.0	
Forward Transconductance	g_{FS}	V_{DS} = 1.5 V, I_D = 15 A			43		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 15 V			1000		pF
Output Capacitance	C_{OSS}				580		
Reverse Transfer Capacitance	C_{RSS}				160		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V; I_D = 30 A			9.7		nC
Threshold Gate Charge	$Q_{G(TH)}$				1.5		
Gate−to−Source Charge	Q_{GS}				2.8		
Gate−to−Drain Charge	Q_{GD}				4.8		
Gate Plateau Voltage	V_{GP}				3.2		V
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V; I_D = 30 A			18.6		nC
SWITCHING CHARACTERISTICS (Note 7)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω			9.0		ns
Rise Time	t_r				34		
Turn−Off Delay Time	$t_{d(OFF)}$				14		
Fall Time	t_f				7.0		
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω			7.0		ns
Rise Time	t_r				26		
Turn−Off Delay Time	$t_{d(OFF)}$				18		
Fall Time	t_f				4.0		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 10 A	T_J = 25°C		0.80	1.1	V
			T_J = 125°C		0.67		

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN–SOURCE DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 30 A		26.7		ns
Charge Time	t_a			14.1		
Discharge Time	t_b			12.6		
Reverse Recovery Charge	Q_{RR}			13.7		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
7. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

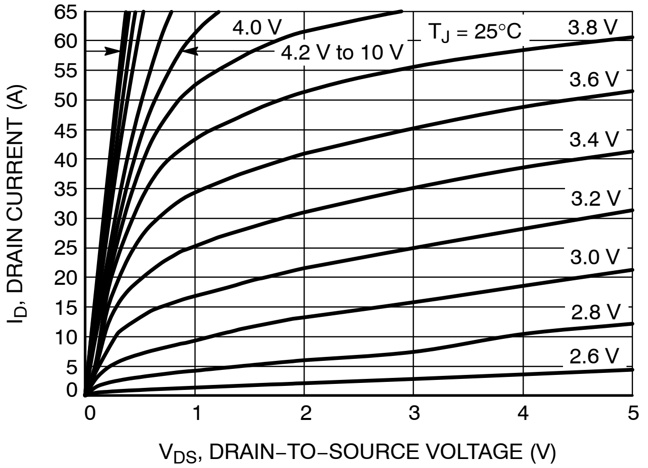


Figure 1. On−Region Characteristics

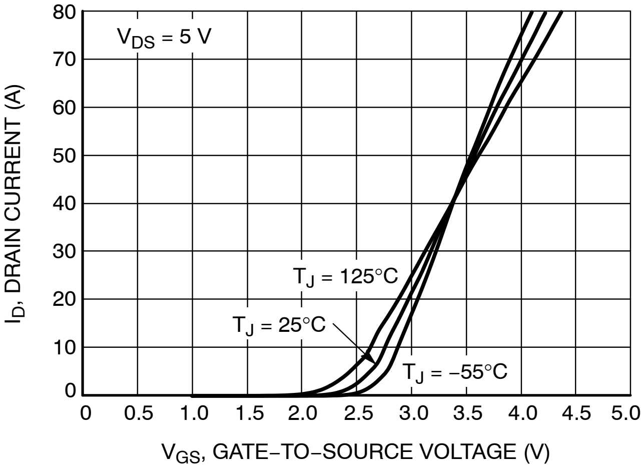


Figure 2. Transfer Characteristics

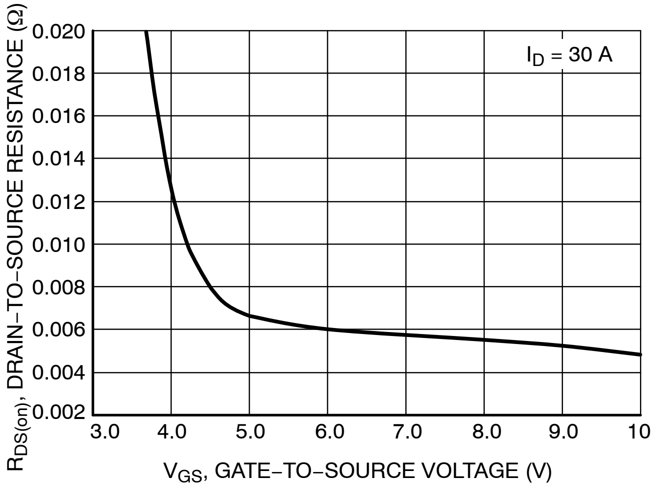


Figure 3. On−Resistance vs. V_{GS}

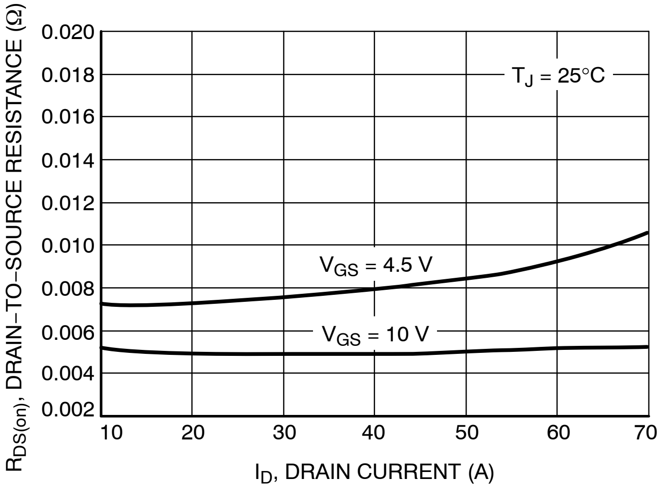


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

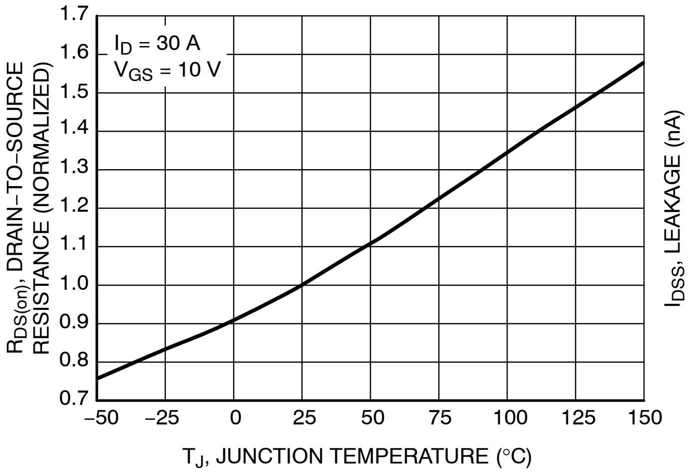


Figure 5. On−Resistance Variation with Temperature

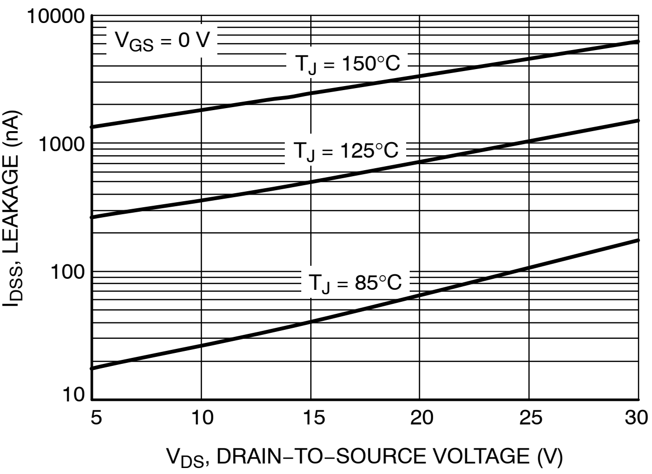


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

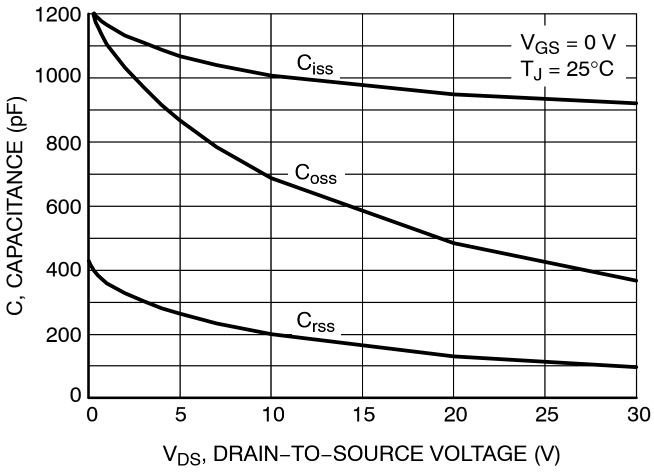


Figure 7. Capacitance Variation

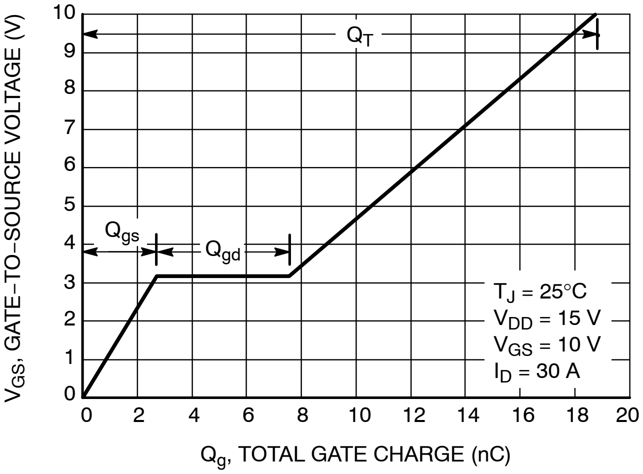


Figure 8. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge

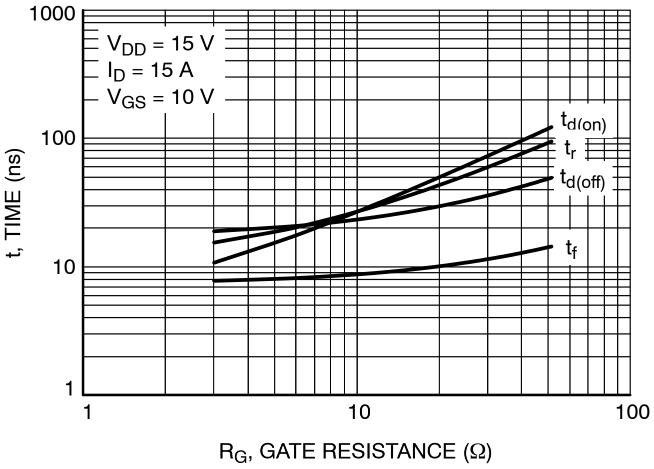


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

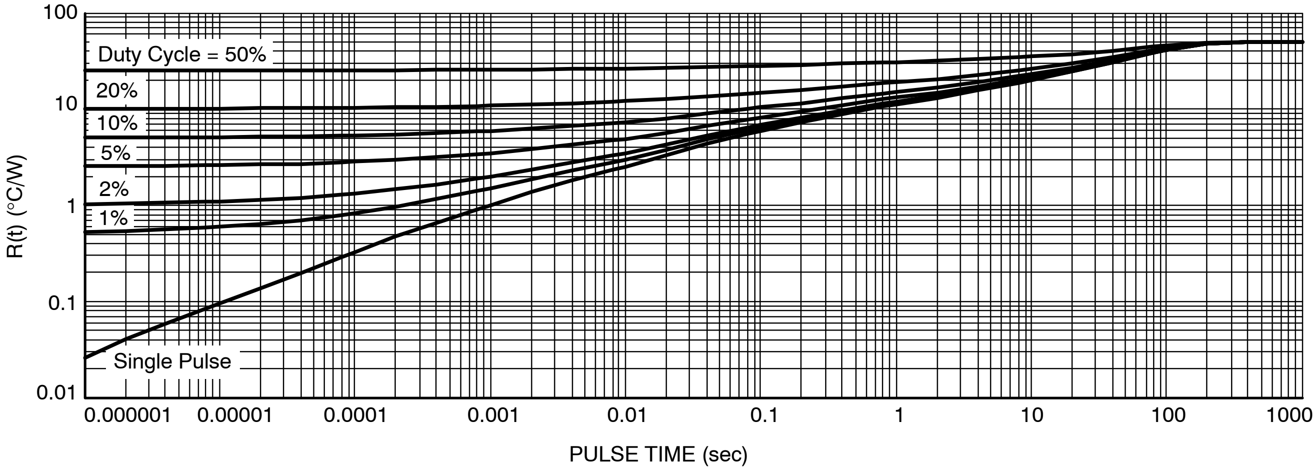
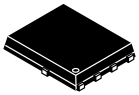


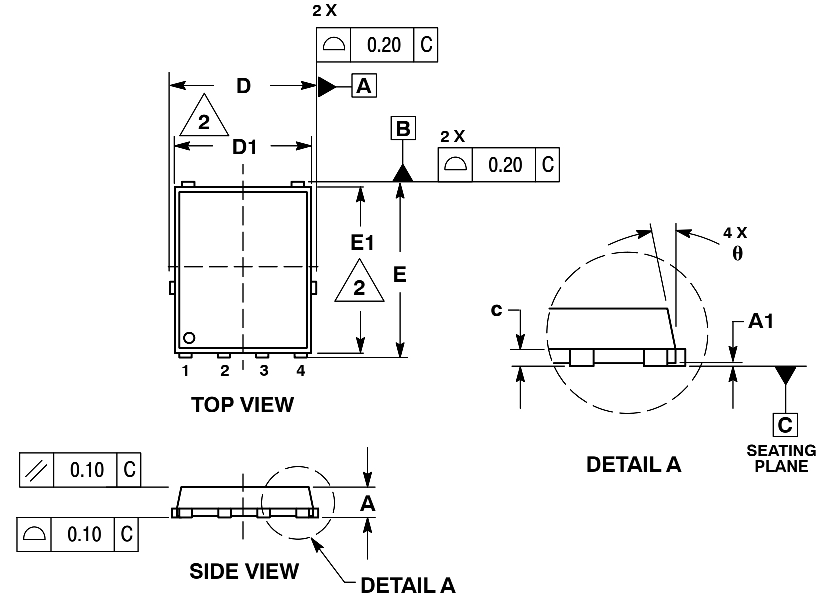
Figure 10. Thermal Response



SCALE 2:1

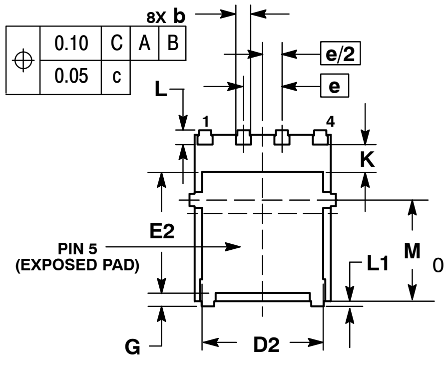
DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018



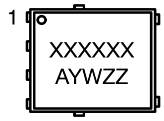
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	---	12 °



BOTTOM VIEW

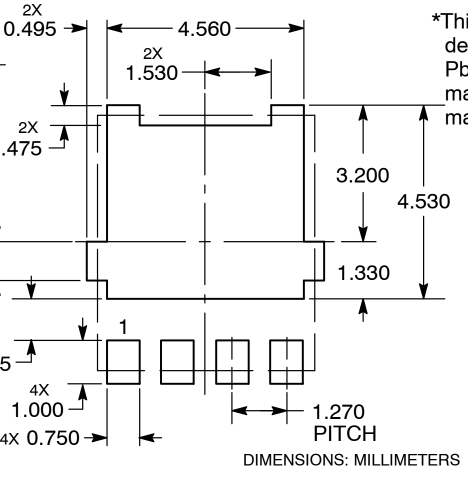
GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

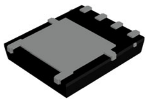
STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

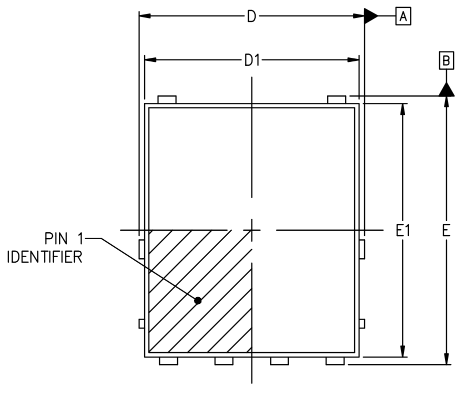
DOCUMENT NUMBER:	**98AON14036D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DFN5 5x6, 1.27P (SO−8FL)**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



DFNW5 4.90x5.90x1.00, 1.27P
CASE 507BA
ISSUE C

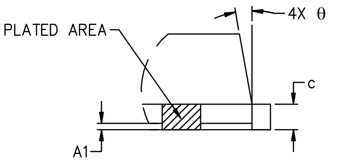
DATE 19 SEP 2024



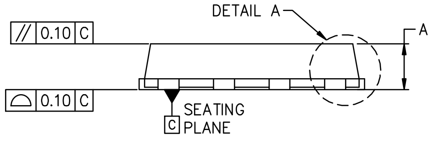
TOP VIEW

NOTES:

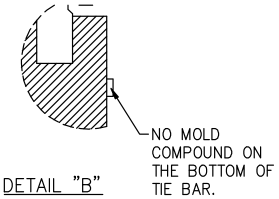
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M−2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.



DETAIL "A"
SCALE 2:1

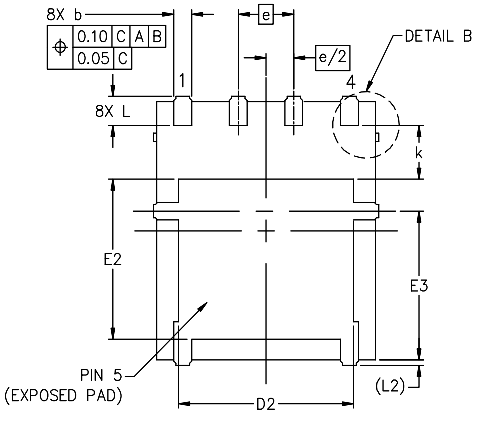


SIDE VIEW

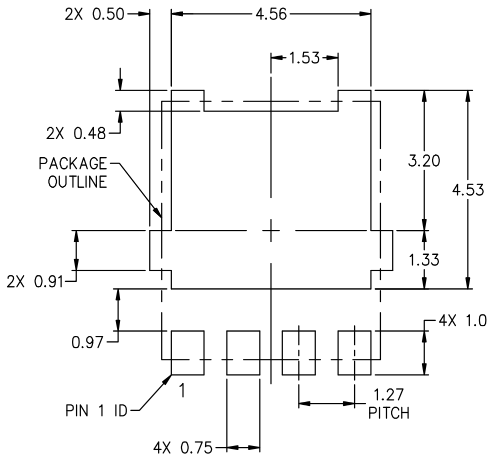


DETAIL "B"
SCALE 2:1

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	−−−	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
θ	0°	6°	12°



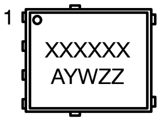
BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



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W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFNW5 4.90x5.90x1.00, 1.27P**	**PAGE 1 OF 1**

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