



PSMN2R2-100SSE

N-channel 100 V, 2.3 mOhm ASFET with enhanced SOA in LFPK88

20 June 2025

Product data sheet

1. General description

N-channel enhancement mode MOSFET in a LFPK88 package qualified to 175 °C. Part of Nexperia's Application Specific MOSFETs (ASFETs) for Hotswap and Soft Start. The PSMN2R2-100SSE delivers very low $R_{DS(on)}$ and enhanced safe operating area performance in a high-reliability copper-clip LFPK88 package.

The PSMN2R2-100SSE complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn-on, low $R_{DS(on)}$ to minimize I^2R losses and deliver optimum efficiency when turned fully ON.

2. Features and benefits

- Fully optimized Safe Operation Area (SOA) for superior linear mode operation
- Enhanced current sharing in parallel applications
- Low $R_{DS(on)}$ for low I^2R conduction losses
- 255 A continuous I_D Max
- Avalanche rated, 100% tested
- Compact and reliable 8x8 LFPK88 package, qualified to 175 °C

3. Applications

- Hotswap
- Load switch
- Soft start
- E-fuse
- Telecom and computing systems based on a 48 V backplane

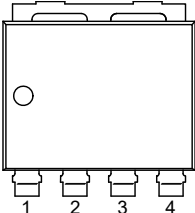
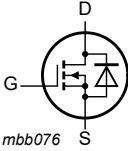
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	255	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	500	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12	-	1.85	2.3	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 50\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 14 ; Fig. 15	2	8	18	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 LFPAK88 (SOT1235)	
2	S	source		
3	S	source		
4	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R2-100SSE	LFPAK88	plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R2-100SSE	X2E2S10S

8. Limiting values

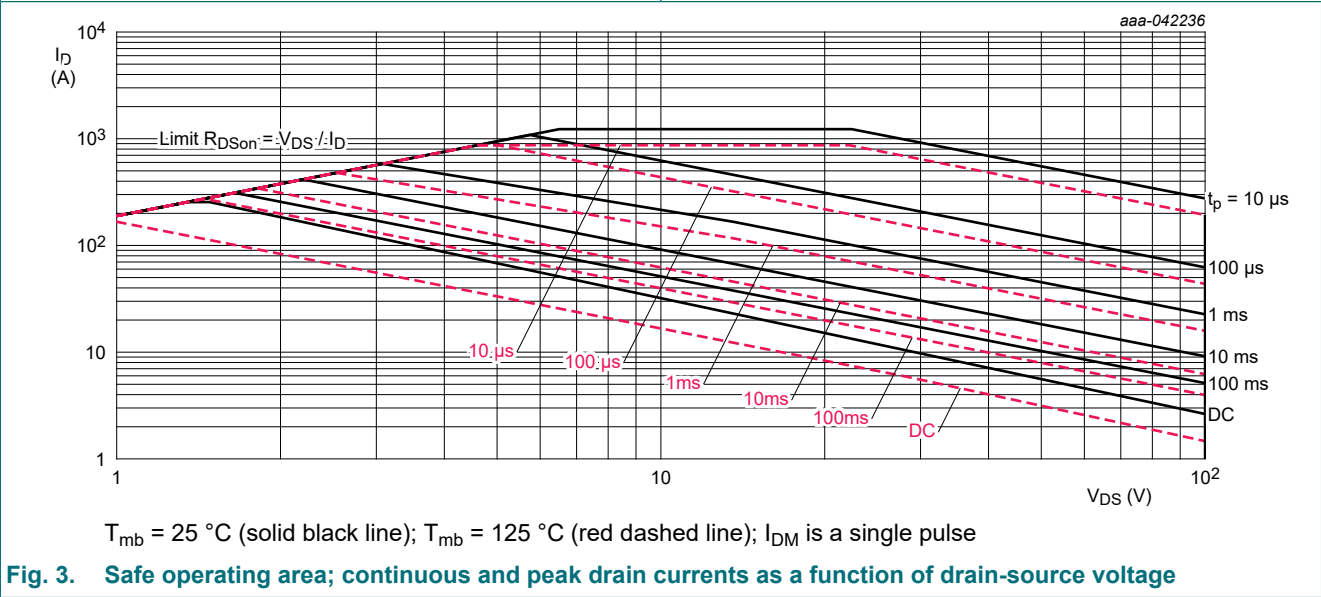
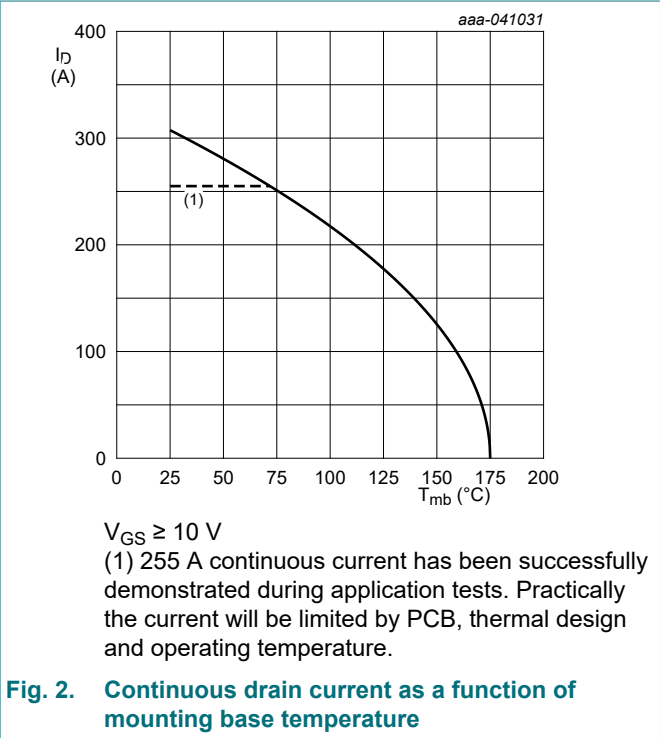
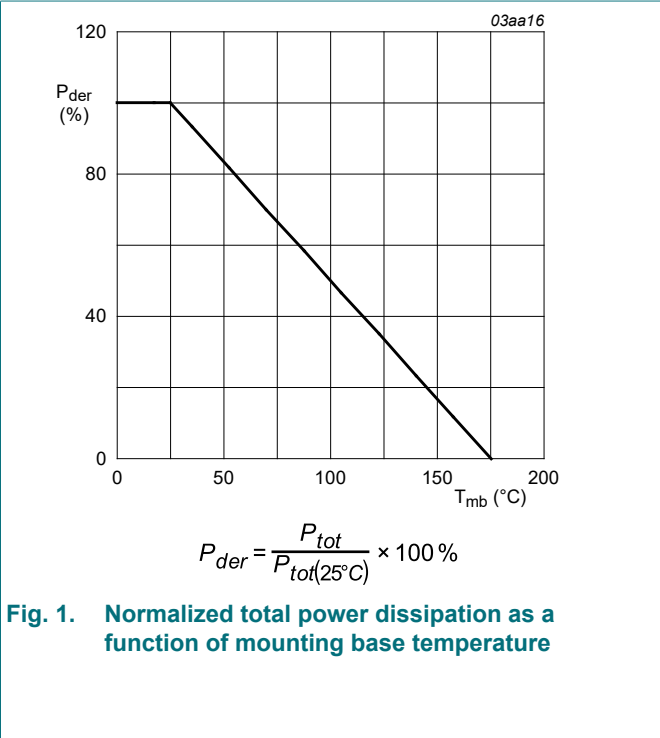
Table 5. Limiting values

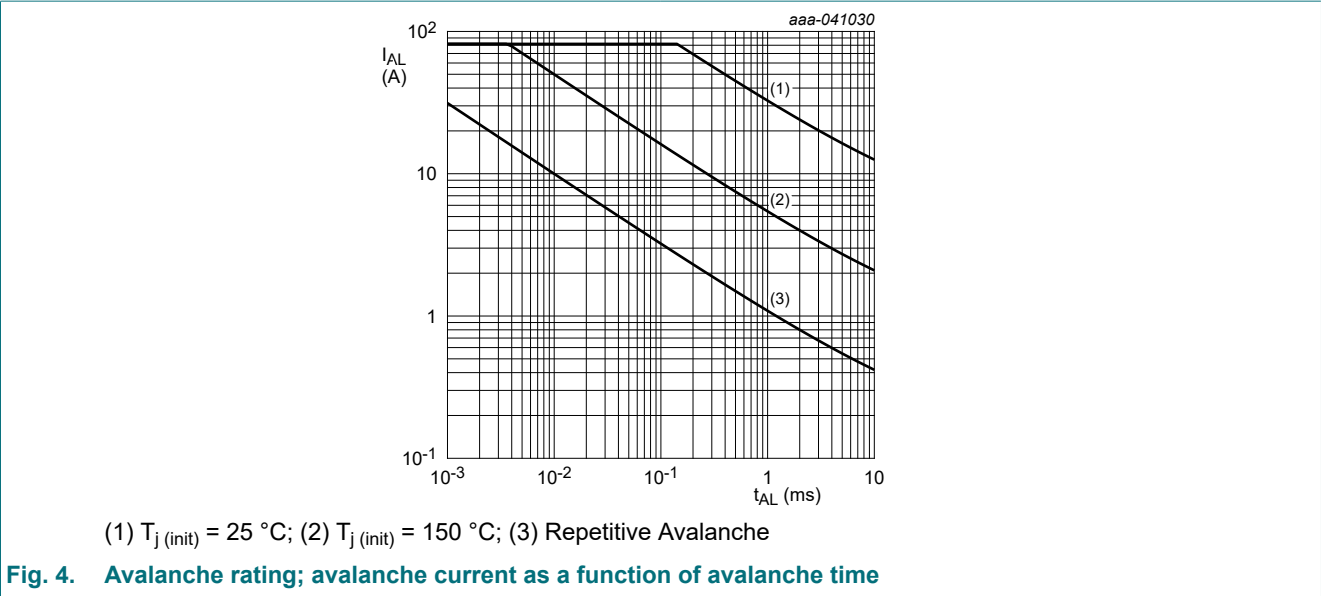
In accordance with the Absolute Maximum Rating System (IEC 60134). *T*_j = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ <i>T</i> _j ≤ 175 °C	-	100	V
V _{DGR}	drain-gate voltage	25 °C ≤ <i>T</i> _j ≤ 175 °C; R _{GS} = 20 kΩ	-	100	V
V _{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	<i>T</i> _{mb} = 25 °C; Fig. 1	-	500	W
I _D	drain current	V _{GS} = 10 V; <i>T</i> _{mb} = 25 °C; Fig. 2	-	255	A
		V _{GS} = 10 V; <i>T</i> _{mb} = 100 °C; Fig. 2	-	217	A
I _{DM}	peak drain current	pulsed; <i>t</i> _p ≤ 10 μs; <i>T</i> _{mb} = 25 °C; Fig. 3	-	1230	A
<i>T</i> _{stg}	storage temperature		-55	175	°C
<i>T</i> _j	junction temperature		-55	175	°C
<i>T</i> _{slid(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	<i>T</i> _{mb} = 25 °C	-	255	A
I _{SM}	peak source current	pulsed; <i>t</i> _p ≤ 10 μs; <i>T</i> _{mb} = 25 °C	-	1230	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 81.7\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ }^\circ\text{C}$; unclamped; $t_p = 142\text{ }\mu\text{s}$; Fig. 4	[1]	-	753	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} = 100\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ }^\circ\text{C}$; $R_{GS} = 50\text{ }\Omega$; Fig. 4	[1]	-	81.7	A

[1] Protected by 100% test

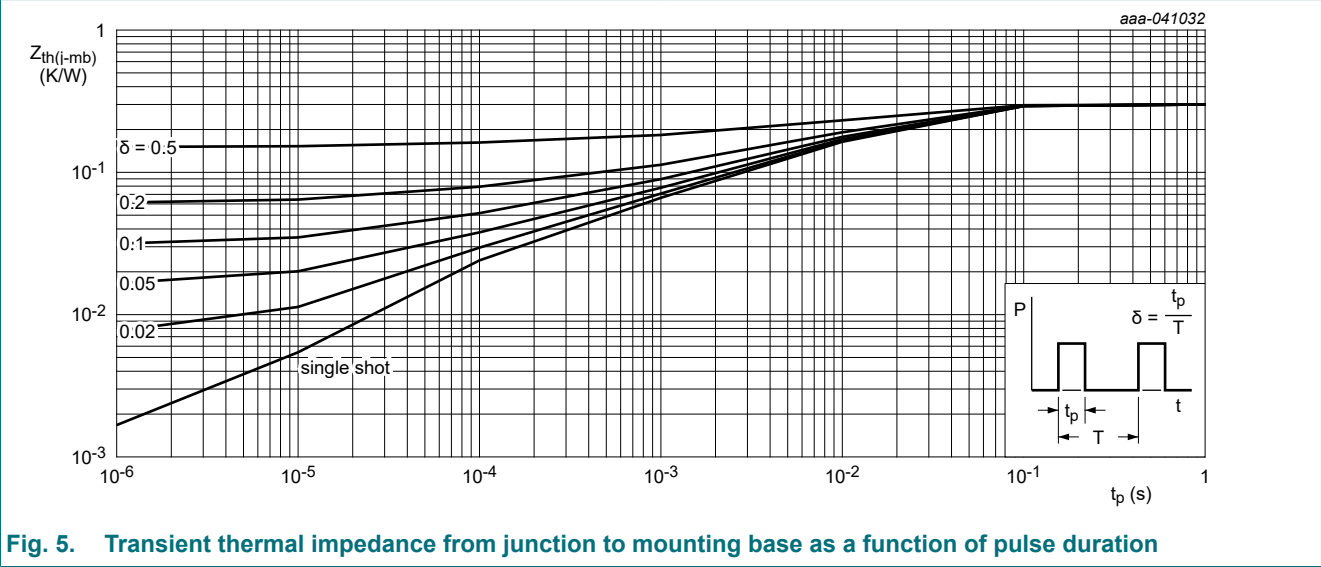


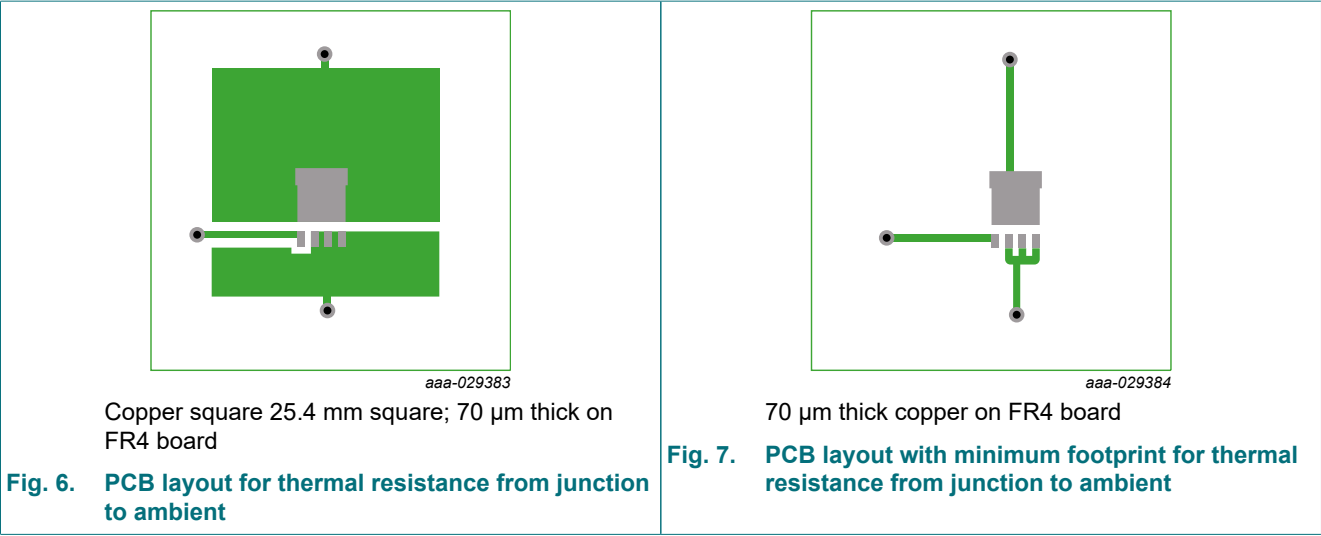


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.23	0.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6		-	35	-	K/W
		Fig. 7		-	70	-	K/W



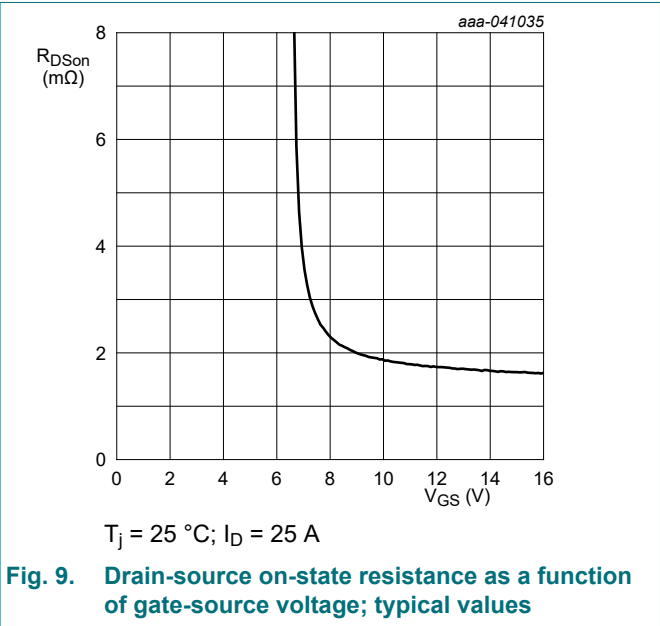
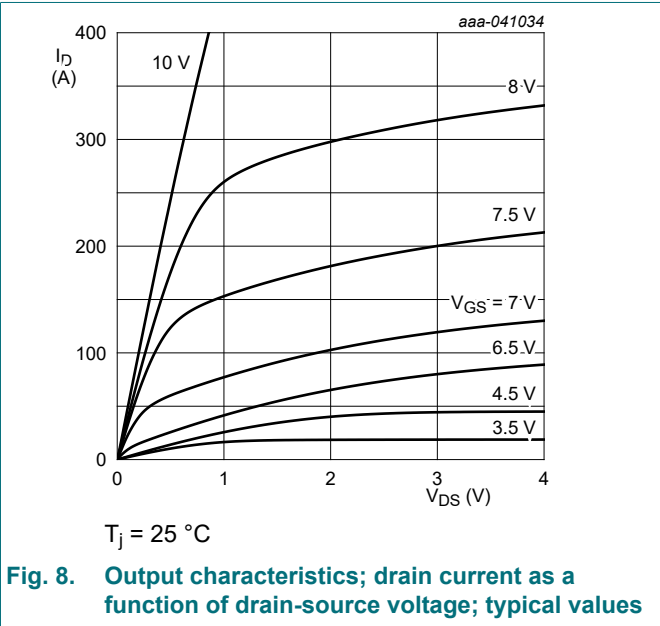


10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	100	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	90	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 25 °C; Fig. 11	1.6	1.85	2.2	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 175 °C	-	1.2	-	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = -55 °C	-	2.1	-	V
ΔV _{GS(th)} /ΔT	gate-source threshold voltage variation with temperature	25 °C ≤ T _j ≤ 150 °C	-	-4.2	-	mV/K
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C	-	0.06	1	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 125 °C	-	20	100	μA
I _{GSS}	gate leakage current	V _{GS} = 16 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -16 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 12	-	1.85	2.3	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C; Fig. 13	-	2.8	3.6	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 13	-	3.9	5.2	mΩ
R _G	gate resistance	f = 1 MHz; T _j = 25 °C	0.68	1.35	2.7	Ω
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 14 ; Fig. 15	140	280	420	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _j = 25 °C	-	274	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 14 ; Fig. 15		52	88	123	nC
Q _{GS(th)}	pre-threshold gate-source charge			-	38	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge			-	50	-	nC
Q _{GD}	gate-drain charge			2	8	18	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 50 V; T _j = 25 °C; Fig. 14 ; Fig. 15		-	3.8	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 16		14904	24840	34776	pF
C _{oss}	output capacitance			1610	2683	4293	pF
C _{rss}	reverse transfer capacitance			5	47	122	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _j = 25 °C		-	57	-	ns
t _r	rise time			-	57	-	ns
t _{d(off)}	turn-off delay time			-	200	-	ns
t _f	fall time			-	89	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	V _{GS} = 0 V; T _j = 25 °C; Fig. 17		-	0.81	1	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; T _j = 25 °C; Fig. 18		-	72	-	ns
Q _r	recovered charge			-	147	-	nC



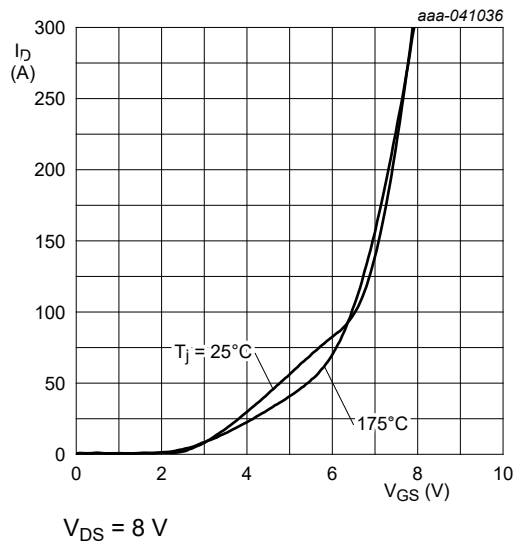


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

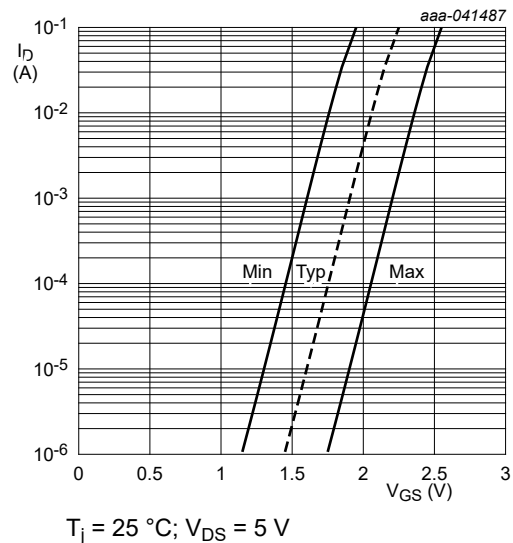


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

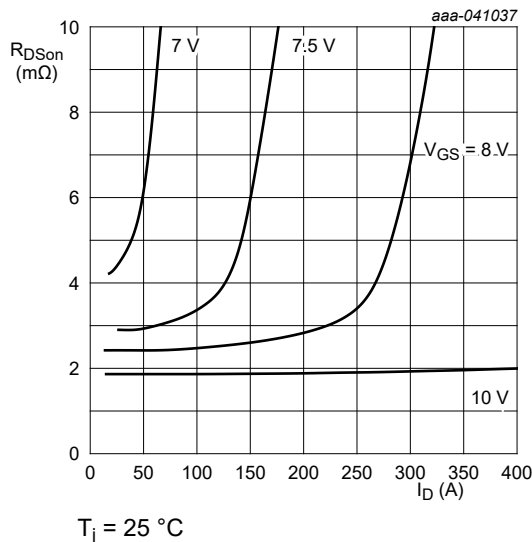


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

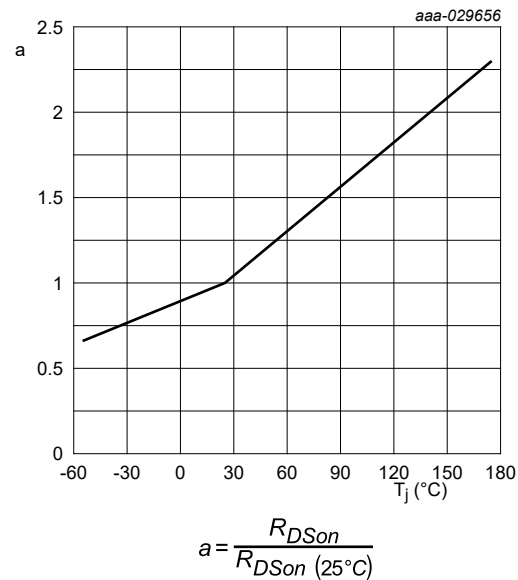


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

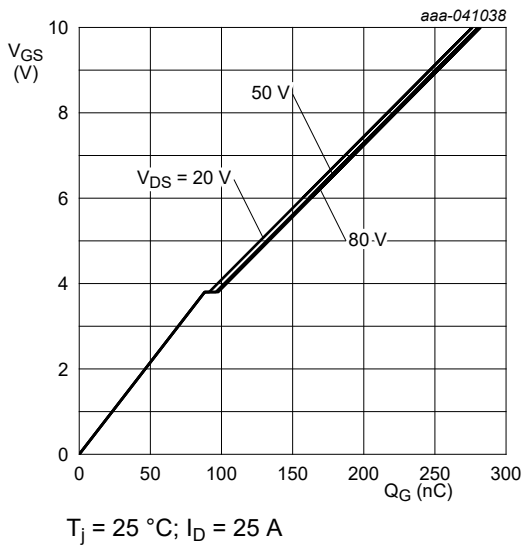


Fig. 14. Gate-source voltage as a function of gate charge; typical values

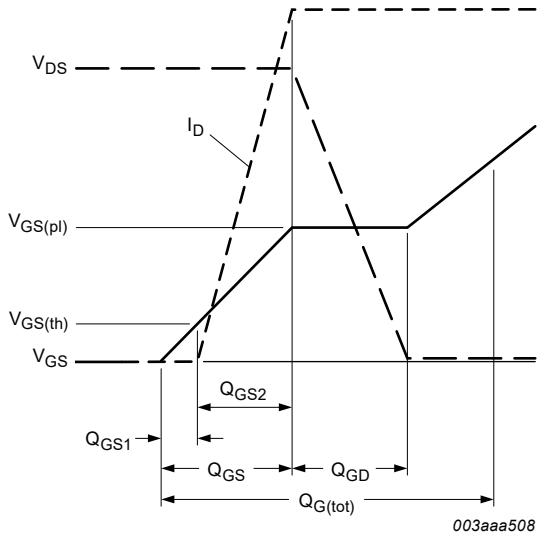


Fig. 15. Gate charge waveform definitions

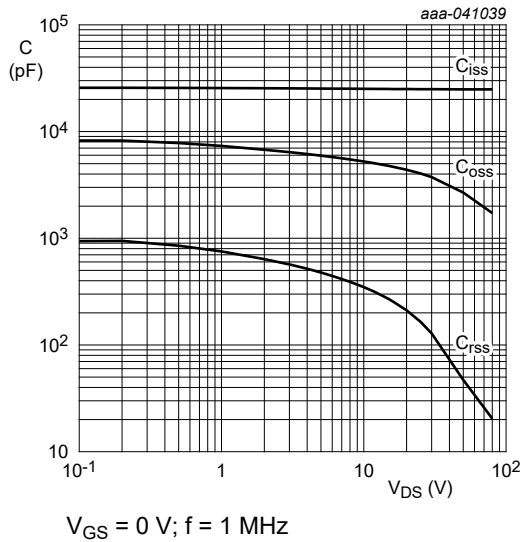


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

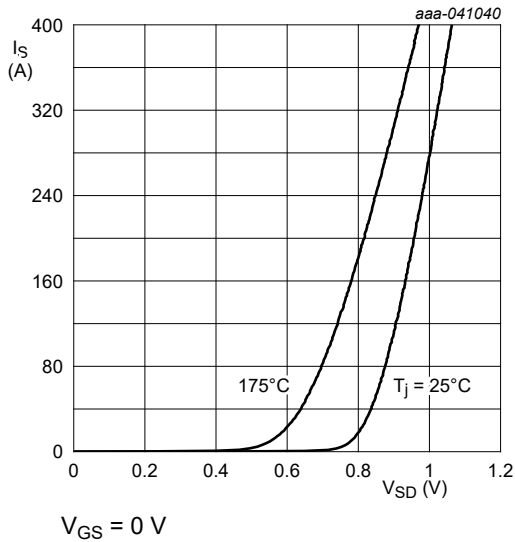


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

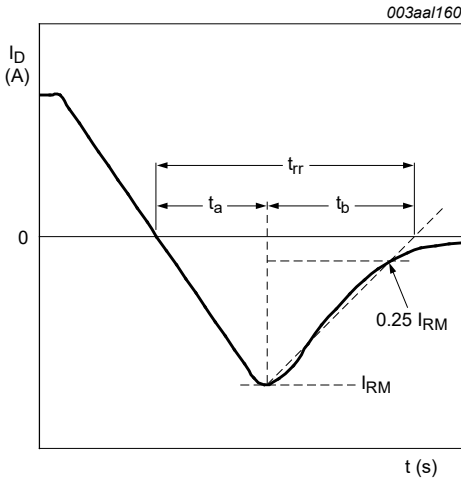


Fig. 18. Reverse recovery timing definition

11. Package outline

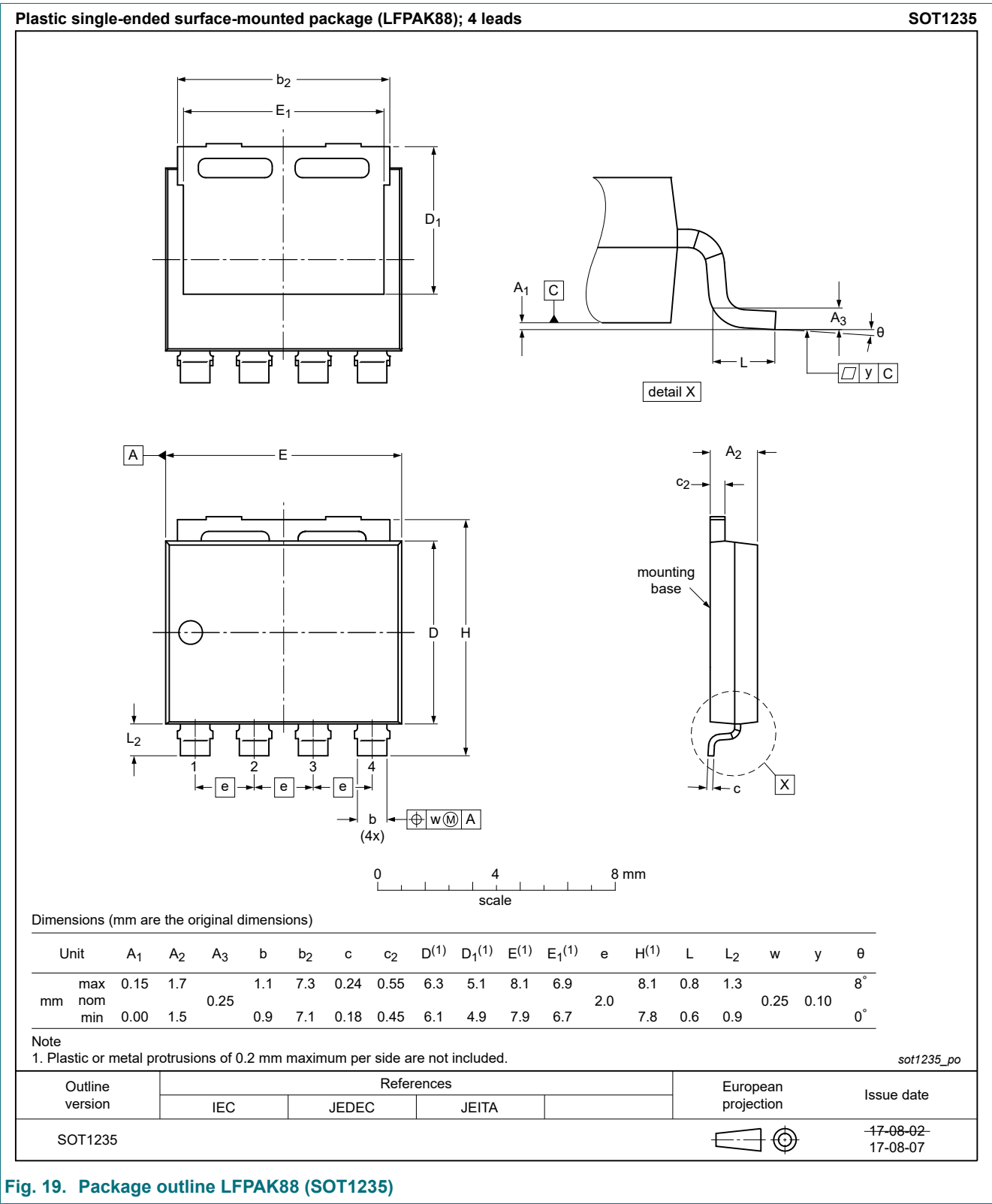


Fig. 19. Package outline LPAK88 (SOT1235)

12. Soldering

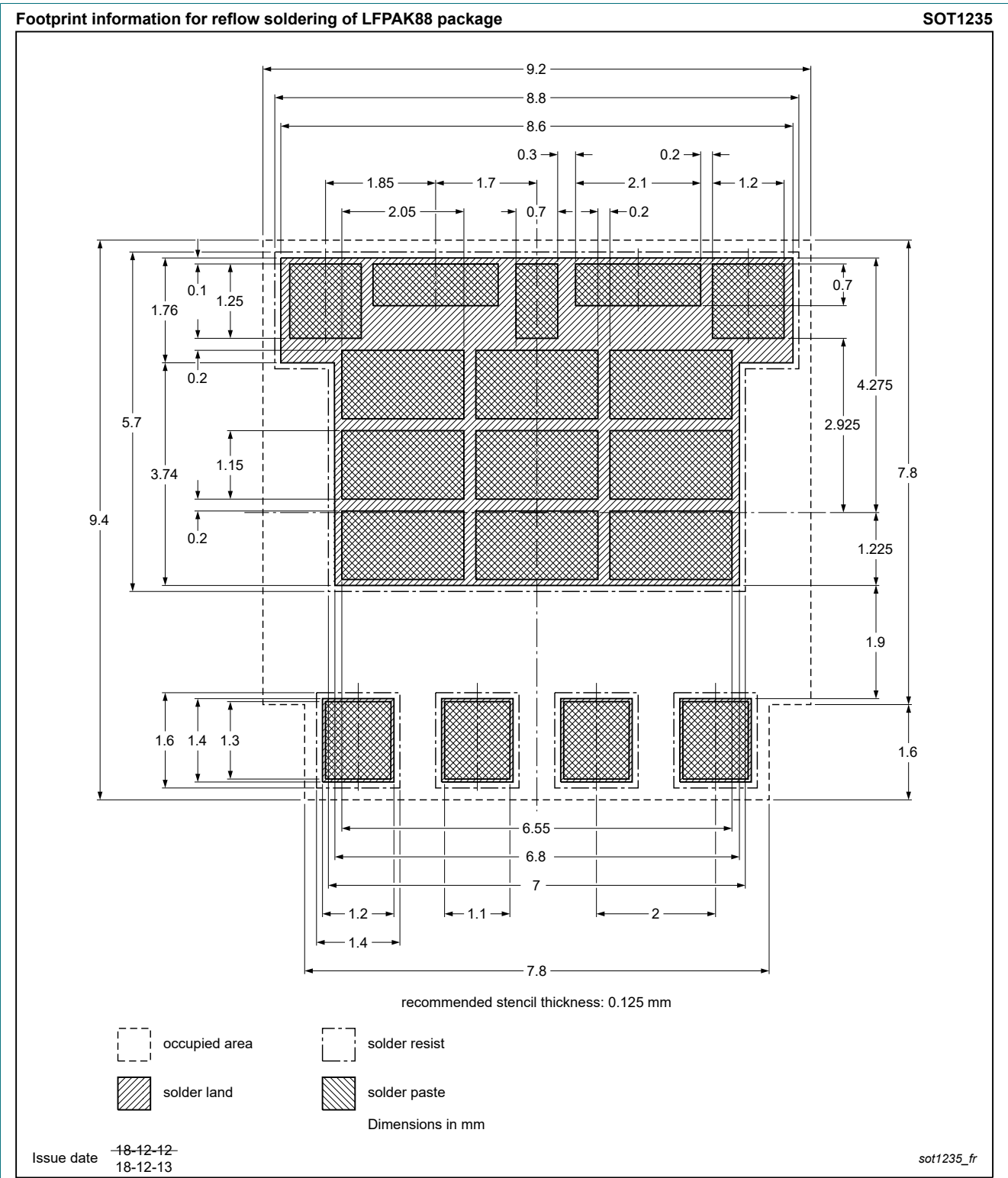


Fig. 20. Reflow soldering footprint for LPAK88 (SOT1235)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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