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January 2003
August, 2024 - Rev. 1

NC7SP74
TinyLogic® ULP D-Type Flip-Flop with Preset and Clear

General Description

The NC7SP74 is a single D-type CMOS Flip-Flop with preset and clear from Fairchild's Ultra Low Power (ULP) Series of TinyLogic®. Ideal for applications where battery life is critical, this product is designed for ultra low power consumption within the V_{CC} operating range of 0.9V to 3.6V.

The internal circuit is composed of a minimum of inverter stages including the output buffer, to enable ultra low static and dynamic power.

The NC7SP74, for lower drive requirements, is uniquely designed for optimized power and speed, and is fabricated with an advanced CMOS technology to achieve best in class speed operation while maintaining extremely low CMOS power dissipation.

The signal level applied to the D input is transferred to the Q output during the positive going transition of the CLK pulse.

Features

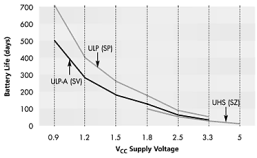
- Space saving US8 surface mount package
- MicroPak™ Pb-Free leadless package
- 0.9V to 3.6V V_{CC} supply operation
- 3.6V overvoltage tolerant I/Os at V_{CC} from 0.9V to 3.6V
- t_{PD}
  - 3.0 ns typ for 3.0V to 3.6V V_{CC}
  - 4.0 ns typ for 2.3V to 2.7V V_{CC}
  - 5.0 ns typ for 1.65V to 1.95V V_{CC}
  - 6.0 ns typ for 1.40V to 1.60V V_{CC}
  - 9.0 ns typ for 1.10V to 1.30V V_{CC}
  - 24.0 ns typ for 0.90V V_{CC}
- Power-off high impedance inputs and outputs
- Static Drive (I_{OH}/I_{OL})
  - ±2.6 mA @ 3.00V V_{CC}
  - ±2.1 mA @ 2.30V V_{CC}
  - ±1.9 mA @ 1.65V V_{CC}
  - ±1.0 mA @ 1.40V V_{CC}
  - ±0.5 mA @ 1.10V V_{CC}
  - ±20 µA @ 0.9V V_{CC}
- Uses patented Quiet Series™ noise/EMI reduction circuitry
- Ultra low dynamic power

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SP74K8X	MAB08A	P74	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
NC7SP74L8X	MAC08A	X9	Pb-Free 8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

Pb-Free package per JEDEC J-STD-020B.

Battery Life vs. V_{CC} Supply Voltage



TinyLogic ULP and ULP-A with up to 50% less power consumption can extend your battery life significantly.
Battery Life = $(V_{battery} * I_{battery} * .9)/(P_{device})/24$hrs/day
Where, $P_{device} = (I_{CC} * V_{CC}) + (C_{PD} + C_L) * V_{CC}^2 * f$
Assumes ideal 3.6V Lithium Ion battery with current rating of 900mAH and derated 90% and device frequency at 10MHz, with C_L = 15 pF load

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Pin Descriptions

Pin Names	Description
D	Data Input
CK	Clock Pulse Input
$\overline{CLR}$	Direct Clear Input
Q, $\overline{Q}$	Flip-Flop Output
$\overline{PR}$	Direct Preset Input

Truth Table

Inputs				Outputs		Function
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q_n	$\overline{Q}_n$	No Change

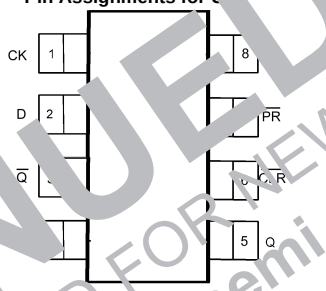
H = HIGH Logic Level
L = LOW Logic Level
Q_n = No change in data
X = Immaterial
Z = High Impedance
↑ = Rising Edge
↓ = Falling edge

Logic Symbol

IEEE/IEC

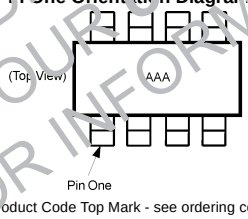
Connection Diagrams

Pin Assignments for U



(Top View)

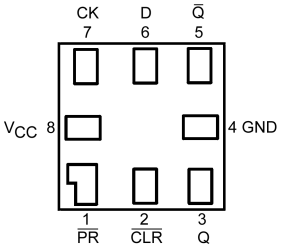
Pin One Orientation Diagram



AAA represents Product Code Top Mark - see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak



(Top Thru View)

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Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_{IN})	−0.5V to +4.6V
DC Output Voltage (V_{OUT})	−0.5V to +7.0V
HIGH or LOW State (Note 2)	−0.5V to V_{CC} +0.5V
V_{CC} = 0V	−0.5V to 4.6V
DC Input Diode Current (I_{IK}) V_{IN} < 0V	±50 mA
DC Output Diode Current (I_{OK})	
V_{OUT} < 0V	−50 mA
V_{OUT} > V_{CC}	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	± 50 mA
DC V_{CC} or Ground Current per	
Supply Pin (I_{CC} or Ground)	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 3)

Power Supply	0.9V to 3.6V
Input Voltage (V_{IN})	0V to 3.6V
Output Voltage (V_{OUT})	
HIGH or LOW State	0V to V_{CC}
V_{CC} = 0V	0V to 3.6V
Output Current in (I_{OH}/I_{OL})	
V_{CC} = 3.0V to 3.6V	±2.6 mA
V_{CC} = 2.3V to 2.7V	±2.[illegible] mA
V_{CC} = 1.65V to 1.95V	±1.5 [illegible]
V_{CC} = 1.40V to 1.60V	±1.0 [illegible]
V_{CC} = 1.10V to 1.30V	[illegible] mA
V_{CC} = 0.9V	±20 µA
Free Air Operating Temperature (T_A)	[illegible]0°C to +85°C
Minimum Input Edge Rate (Δt/ΔV)	
V_{IN} = 0.8V to [illegible]V, V_{CC} = 3.0[illegible]	10 ns/V

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum rating must be observed.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C Min	T_A = +25°C Max	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Units	Conditions
V_{IH}	HIGH Level Input Voltage	0.90	0.65 x V_{CC}		0.65 x V_{CC}		V	
		1.10 ≤ V_{CC} ≤ 1.30	0.65 x V_{CC}		0.65 x V_{CC}			
		1.40 ≤ V_{CC} ≤ 1.60	0.65 x V_{CC}		0.65 x V_{CC}			
		1.65 ≤ V_{CC} ≤ 1.95	0.65 x V_{CC}		0.65 x V_{CC}			
		2.30 ≤ V_{CC} ≤ 2.70	1.6		1.6			
		3.00 ≤ V_{CC} ≤ 3.60	2.1		2.1			
V_{IL}	LOW Level Input Voltage	0.90		0.35 x V_{CC}		0.35 x V_{CC}	V	
		1.10 ≤ V_{CC} ≤ 1.30		0.35 x V_{CC}		0.35 x V_{CC}		
		1.40 ≤ V_{CC} ≤ 1.60		0.35 x V_{CC}		0.35 x V_{CC}		
		1.65 ≤ V_{CC} ≤ 1.95		0.35 x V_{CC}		0.35 x V_{CC}		
		2.30 ≤ V_{CC} ≤ 2.70		0.7		0.7		
		3.00 ≤ V_{CC} ≤ 3.60		0.9		0.9		
V_{OH}	HIGH Level Output Voltage	0.90	V_{CC} - 0.1		V_{CC} - 0.1		V	I_{OH} = −20 µA
		1.10 ≤ V_{CC} ≤ 1.30	V_{CC} - 0.1		V_{CC} - 0.1			
		1.40 ≤ V_{CC} ≤ 1.60	V_{CC} - 0.1		V_{CC} - 0.1			
		1.65 ≤ V_{CC} ≤ 1.95	V_{CC} - 0.1		V_{CC} - 0.1			
		2.30 ≤ V_{CC} ≤ 2.70	V_{CC} - 0.1		V_{CC} - 0.1			
		3.00 ≤ V_{CC} ≤ 3.60	V_{CC} - 0.1		V_{CC} - 0.1			
		1.10 ≤ V_{CC} ≤ 1.30	0.75 x V_{CC}		0.70 x V_{CC}			I_{OH} = −0.5 mA
		1.40 ≤ V_{CC} ≤ 1.60	1.07		0.99			I_{OH} = −1.0 mA
		1.65 ≤ V_{CC} ≤ 1.95	1.24		1.22			I_{OH} = −1.5 mA
		2.30 ≤ V_{CC} ≤ 2.70	1.95		1.87			I_{OH} = −2.1 mA
		3.00 ≤ V_{CC} ≤ 3.60	2.61		2.55			I_{OH} = −2.6 mA

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DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Min	$T_A = +25°C$ Max	$T_A = -40°C$ to $+85°C$ Min	$T_A = -40°C$ to $+85°C$ Max	Units	Conditions
V_{OL}	LOW Level Output Voltage	0.90		0.1		0.1	V	$I_{OL} = 20\ \mu A$
		$1.10 \le V_{CC} \le 1.30$		0.1		0.1		
		$1.40 \le V_{CC} \le 1.60$		0.1		0.1		
		$1.65 \le V_{CC} \le 1.95$		0.1		0.1		
		$2.30 \le V_{CC} \le 2.70$		0.1		0.1		
		$3.00 \le V_{CC} \le 3.60$		0.1		0.1		
		$1.10 \le V_{CC} \le 1.30$		$0.30 \times V_{CC}$		$0.30 \times V_{CC}$		$I_{OL} = [illegible]$ mA
		$1.40 \le V_{CC} \le 1.60$		0.31		0.37		$I_{OL} = 1.0$ [illegible]
		$1.65 \le V_{CC} \le 1.95$		0.31		0.35		[illegible] = 1.5 m[illegible]
		$2.30 \le V_{CC} \le 2.70$		0.31		0.33		I_{OL} [illegible]
		$3.00 \le V_{CC} \le 3.60$		0.31		0.33		I_{OL} [illegible].6 mA
I_{IN}	Input Leakage Current	0.90 to 3.60		±0.1		[illegible]	µA	$0 \le V_I \le 3.6V$
I_{OFF}	Power Off Leakage Current	0		0.5		0.[illegible]		$0 \le (V_I, V_O) \le 3.6V$
I_{CC}	Quiescent Supply Current	0.90 to 3.60		0.9		0.9	µA	$V_I = V_{CC}$ or GND

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AC Electrical Characteristics (10pF, 1MΩ)

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Min	Typ	Max	$T_A = -40°C$ to $+85°C$ Min	Max	Units	Conditions	Figure Number
f_{MAX}	Maximum Clock Frequency	0.90		40.0				MHz	$C_L = 10$ pF, $R_D = 1$ MΩ	Figures 1, 5
		$1.10 \le V_{CC} \le 1.30$	50			50				
		$1.40 \le V_{CC} \le 1.60$	75			75				
		$1.65 \le V_{CC} \le 1.95$	100			100				
		$2.30 \le V_{CC} \le 2.70$	125			125				
		$3.00 \le V_{CC} \le 3.60$	150			150				
t_{PLH} t_{PHL}	Propagation Delay CK to Q, $\overline{Q}$	0.90		24.0				ns	$C_L = 10$ pF, $R_D = 1$ MΩ	Figures 1, 5
		$1.10 \le V_{CC} \le 1.30$	4.0	15.0	22.0	3.5	31.0			
		$1.40 \le V_{CC} \le 1.60$	2.0	9.0	13.0	1.5	14.0			
		$1.65 \le V_{CC} \le 1.95$	1.5	7.0	11.0	1.0	13.0			
		$2.30 \le V_{CC} \le 2.70$	1.0	5.0	8.0	0.8	9.0			
		$3.00 \le V_{CC} \le 3.60$	1.0	4.0	7.0	0.5	8.0			
t_{PLH} t_{PHL}	Propagation Delay $\overline{CLR}$, $\overline{PR}$, to Q, $\overline{Q}$	0.90		6.5				ns	$C_L = 10$ pF, $R_D = 1$ MΩ	Figures 1, 3
		$1.10 \le V_{CC} \le 1.30$	4.0	12.0	23.0	4.0	24.0			
		$1.40 \le V_{CC} \le 1.60$	2.0	9.0	12.0	2.0	[illegible]			
		$1.65 \le V_{CC} \le 1.95$	1.5	7.0	11.0	1.5	13.0			
		$2.30 \le V_{CC} \le 2.70$	1.0	5.0	9.0	1.0	9.0			
		$3.00 \le V_{CC} \le 3.60$	1.0	4.0	8.0	1.0	8.0			
t_S	Setup Time, CK to D	0.90		[illegible]				ns	$C_L = 10$ pF, $R_D = 1$ MΩ	Figures 1, 4
		$1.10 \le V_{CC} \le 1.30$	7.0			7.0				
		$1.40 \le V_{CC} \le 1.60$	3.0			3.0				
		$1.65 \le V_{CC} \le 1.95$	2.0			2.0				
		$2.30 \le V_{CC} \le 2.70$	[illegible]			1.5				
		$3.00 \le V_{CC} \le 3.60$	1.0			1.0				
t_H	Hold Time, CK to D	0.90		1.0				ns	$C_L = 10$ pF, $R_D = 1$ MΩ	Figures 1, 4
		$1.10 \le V_{CC} \le 1.30$	0.5			0.5				
		$1.40 \le V_{CC} \le 1.60$	0.5			0.5				
		$1.65 \le V_{CC} \le 1.95$	0.5			0.5				
		$2.30 \le V_{CC} \le 2.70$	0.5			0.5				
		$3.00 \le V_{CC} \le 3.60$	0.5			0.5				
t_W	[illegible] CK, $\overline{PR}$, $\overline{CL}$	0.90		5.0				ns	$C_L = 10$ pF, $R_D = 1$ MΩ	Figures 1, 5
		$1.10 \le V_{CC} \le 1.30$	5.0			5.0				
		$1.40 \le V_{CC} \le 1.60$	3.0			3.0				
		$1.65 \le V_{CC} \le 1.95$	2.5			2.5				
		$2.30 \le V_{CC} \le 2.70$	2.5			2.5				
		$3.00 \le V_{CC} \le 3.60$	2.0			2.0				
t_{REC}	Recover Time $\overline{CLR}$, $\overline{PR}$ to CK	0.90		12.0				ns	$C_L = 10$ pF, $R_D = 1$ MΩ	Figures 1, 4
		$1.10 \le V_{CC} \le 1.30$	8.5			8.5				
		$1.40 \le V_{CC} \le 1.60$	3.5			3.5				
		$1.65 \le V_{CC} \le 1.95$	3.0			3.0				
		$2.30 \le V_{CC} \le 2.70$	2.5			2.5				
		$3.00 \le V_{CC} \le 3.60$	2.0			2.0				

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AC Electrical Characteristics (15pF, 1MΩ)

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Min	Typ	Max	$T_A = -40°C$ to $+85°C$ Min	Max	Units	Conditions	Figure Number
f_{MAX}	Maximum Clock Frequency	0.90		40.0				MHz	$C_L = 15$ pF, $R_D = 1$ MΩ	Figures 1, 5
		$1.10 \le V_{CC} \le 1.30$	50			150				
		$1.40 \le V_{CC} \le 1.60$	75			200				
		$1.65 \le V_{CC} \le 1.95$	100			250				
		$2.30 \le V_{CC} \le 2.70$	125			175				
		$3.00 \le V_{CC} \le 3.60$	150			200				
t_{PLH} t_{PHL}	Propagation Delay CK to Q, $\overline{Q}$	0.90		27.0				ns	$C_L = 15$ pF, $R_D = 1$ MΩ	Figures 1, 3
		$1.10 \le V_{CC} \le 1.30$	5.0	16.0	23.0	4.5	34.0			
		$1.40 \le V_{CC} \le 1.60$	3.0	10.0	14.0	2.5	16.0			
		$1.65 \le V_{CC} \le 1.95$	2.0	7.0	11.0	2.0	13.0			
		$2.30 \le V_{CC} \le 2.70$	1.5	5.0	8.0	1.0	9.0			
		$3.00 \le V_{CC} \le 3.60$	1.0	4.0	7.0	0.5	[illegible]			
t_{PLH} t_{PHL}	Propagation Delay $\overline{CLR}$, $\overline{PR}$, to Q, $\overline{Q}$	0.90		27.0				ns	$C_L = 15$ pF, $R_D = 1$ MΩ	Figures 1, 3
		$1.10 \le V_{CC} \le 1.30$	5.0	15.0	24.0	5.[illegible]	37.[illegible]			
		$1.40 \le V_{CC} \le 1.60$	3.0	10.0	13.0	3.0	16.0			
		$1.65 \le V_{CC} \le 1.95$	2.0	7.0	[illegible]	[illegible]				
		$2.30 \le V_{CC} \le 2.70$	1.5	5.0	[illegible]	[illegible]	9.0			
		$3.00 \le V_{CC} \le 3.60$	1.0	[illegible].0	7.0	1.0	8.0			
t_S	Setup Time, CK to D	0.90		10.0				ns	$C_L = 15$ pF, $R_D = 1$ MΩ	Figures 1, 4
		$1.10 \le V_{CC} \le 1.30$	7.0			7.0				
		$1.40 \le V_{CC} \le 1.60$	3.0			[illegible]				
		$1.65 \le V_{CC} \le 1.95$	[illegible]			2.0				
		$2.30 \le V_{CC} \le 2.70$	[illegible]			1.5				
		$3.00 \le V_{CC} \le 3.60$	1.0			1.0				
t_H	Hold Time, CK to D	0.90		[illegible].0				ns	$C_L = 15$ pF, $R_D = 1$ MΩ	Figures 1, 4
		$1.10 \le V_{CC} \le 1.30$	0.5			0.5				
		$1.40 \le V_{CC} \le 1.60$	0.5			0.5				
		$1.65 \le V_{CC} \le 1.95$	0.5			0.5				
		$2.30 \le V_{CC} \le 2.70$	0.5			0.5				
		$3.00 \le V_{CC} \le 3.60$	0.5			0.5				
t_W	[illegible] width, CK, $\overline{PR}$, $\overline{CLR}$	0.90		5.0				ns	$C_L = 15$ pF, $R_D = 1$ MΩ	Figures 1, 5
		$1.10 \le V_{CC} \le 1.30$	5.0			5.0				
		$1.40 \le V_{CC} \le 1.60$	3.0			3.0				
		$1.65 \le V_{CC} \le 1.95$	2.5			2.5				
		$2.30 \le V_{CC} \le 2.70$	2.5			2.5				
		$3.00 \le V_{CC} \le 3.60$	2.0			2.0				
t_{REC}	Recover Time $\overline{CLR}$, $\overline{PR}$ to CK	0.90		12.0				ns	$C_L = 15$ pF, $R_D = 1$ MΩ	Figures 1, 4
		$1.10 \le V_{CC} \le 1.30$	8.5			8.5				
		$1.40 \le V_{CC} \le 1.60$	3.5			3.5				
		$1.65 \le V_{CC} \le 1.95$	3.0			3.0				
		$2.30 \le V_{CC} \le 2.70$	2.5			2.5				
		$3.00 \le V_{CC} \le 3.60$	2.0			2.0				

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AC Electrical Characteristics (30pF, 1MΩ)

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Min	Typ	Max	$T_A = -40°C$ to $+85°C$ Min	Max	Units	Conditions	Figure Number
f_{MAX}	Maximum Clock Frequency	0.90		40.0				MHz	$C_L = 30$ pF, $R_D = 1$ MΩ	Figures 1, 5
		$1.10 \le V_{CC} \le 1.30$	50			150				
		$1.40 \le V_{CC} \le 1.60$	75			200				
		$1.65 \le V_{CC} \le 1.95$	100			250				
		$2.30 \le V_{CC} \le 2.70$	125			175				
		$3.00 \le V_{CC} \le 3.60$	150			200				
t_{PLH} t_{PHL}	Propagation Delay CK to Q, $\overline{Q}$	0.90		34.0				ns	$C_L = 30$ pF, $R_D = 1$ MΩ	Figures 1, 5
		$1.10 \le V_{CC} \le 1.30$	6.0	18.0	27.0	5.0	43.0			
		$1.40 \le V_{CC} \le 1.60$	4.0	11.0	17.0	3.0	18.0			
		$1.65 \le V_{CC} \le 1.95$	2.0	8.0	13.0	2.0	15.0			
		$2.30 \le V_{CC} \le 2.70$	1.0	6.0	10.0	1.0	11.0			
		$3.00 \le V_{CC} \le 3.60$	0.8	5.0	8.0	0.5	10.0			
t_{PLH} t_{PHL}	Propagation Delay $\overline{CLR}$, $\overline{PR}$, to Q, $\overline{Q}$	0.90		34.0				ns	$C_L = 30$ pF, $R_D = 1$ MΩ	Figures 1, 3
		$1.10 \le V_{CC} \le 1.30$	6.0	17.0	28.0	5.5	16.0			
		$1.40 \le V_{CC} \le 1.60$	4.0	11.0	16.0	3.[illegible]	[illegible]			
		$1.65 \le V_{CC} \le 1.95$	2.0	8.0	13.0	2.5	15.[illegible]			
		$2.30 \le V_{CC} \le 2.70$	1.0	6.0	[illegible]	[illegible]	11.0			
		$3.00 \le V_{CC} \le 3.60$	0.8	5.0	[illegible]	1.0	10.0			
t_S	Setup Time, CK to D	0.90		[illegible]				ns	$C_L = 30$ pF, $R_D = 1$ MΩ	Figures 1, 4
		$1.10 \le V_{CC} \le 1.30$	7.0			7.0				
		$1.40 \le V_{CC} \le 1.60$	3.[illegible]			3.0				
		$1.65 \le V_{CC} \le 1.[illegible]$	2.0			2.0				
		$2.30 \le V_{CC} \le 2.7[illegible]$	[illegible]			1.5				
		$3.0[illegible] \le V_{CC} \le [illegible]60$	1.0			1.0				
t_H	Hold Time, CK to D	0.90		1.0				ns	$C_L = 30$ pF, $R_D = 1$ MΩ	Figures 1, 4
		$1.[illegible] \le V_{CC} \le 1.[illegible]$	0.5			0.5				
		$1.4[illegible] \le V_{CC} \le [illegible]0$	0.5			0.5				
		$1.65 \le V_{CC} \le 1.95$	0.[illegible]			0.5				
		$[illegible]0 \le V_{CC} \le 2.7[illegible]$	0.5			0.5				
		$3.00 \le V_{CC} \le 3.60$	0.5			0.5				
t_W	[illegible] CK, $\overline{PR}$, $\overline{CL}$	0.90		5.0				ns	$C_L = 30$ pF, $R_D = 1$ MΩ	Figures 1, 5
		$1.[illegible]0 \le V_{CC} \le 1.30$	5.0			4.0				
		$1.[illegible]0 \le V_{CC} \le 1.60$	3.0			3.0				
		$1.65 \le V_{CC} \le 1.95$	2.5			2.0				
		$2.[illegible]0 \le V_{CC} \le 2.70$	2.5			3.0				
		$3.00 \le V_{CC} \le 3.60$	2.0			2.0				
t_{REC}	Recover Time $\overline{CLR}$, $\overline{PR}$ to CK	0.90		12.0				ns	$C_L = 30$ pF, $R_D = 1$ MΩ	Figures 1, 4
		$1.10 \le V_{CC} \le 1.30$	8.5			8.5				
		$1.[illegible]0 \le V_{CC} \le 1.60$	3.5			3.5				
		$1.65 \le V_{CC} \le 1.95$	3.0			3.0				
		$2.30 \le V_{CC} \le 2.70$	2.5			2.5				
		$3.00 \le V_{CC} \le 3.60$	2.0			2.0				

Capacitance

Symbol	Parameter	Typ	Max	Units	Conditions	Figure Number
C_{IN}	Input Capacitance	2.0		pF	$V_{CC} = 0V$	
C_{OUT}	Output Capacitance	4.0		pF	$V_{CC} = 0V$	
C_{PD}	Power Dissipation Capacitance	8.0		pF	$V_I = 0V$ or V_{CC} f = 10 MHz	Figure 2

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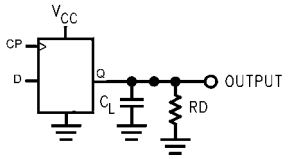
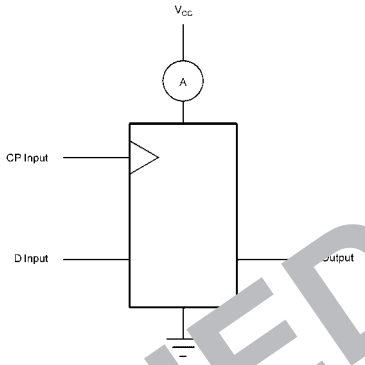
AC Loading and Waveforms



C_L includes load and stray capacitance

Input PRR = 1.0 MHz; t_w = 500 ns

FIGURE 1. AC Test Circuit



CP Input = AC Waveform; t_r = 2.5 ns

CP Input PRR = 10 MHz; Duty Cycle = 50%

D Input PRR = 5 MHz; Duty Cycle = 50%

FIGURE 2. ICC Test Circuit

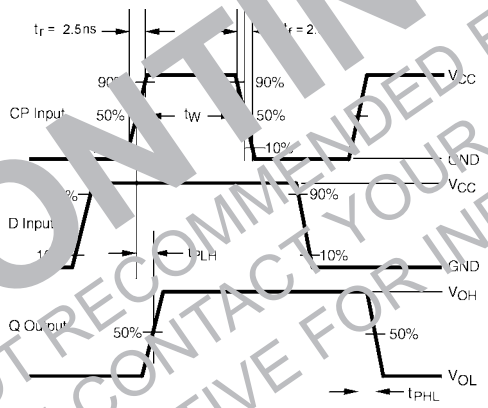


FIGURE 3. AC Waveforms

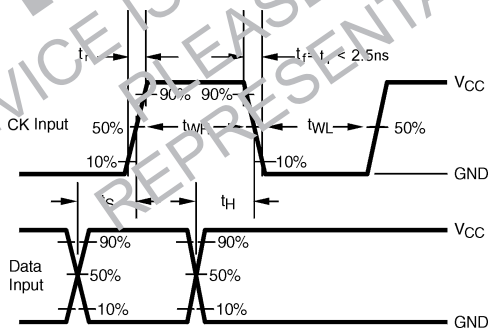


FIGURE 4. AC Waveforms

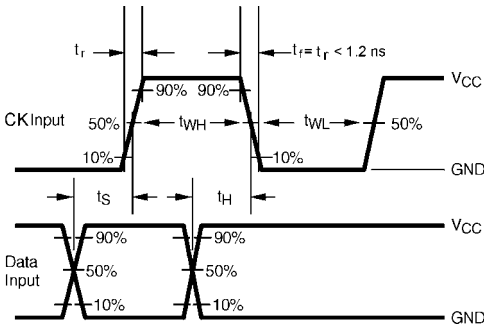


FIGURE 5. AC Waveforms

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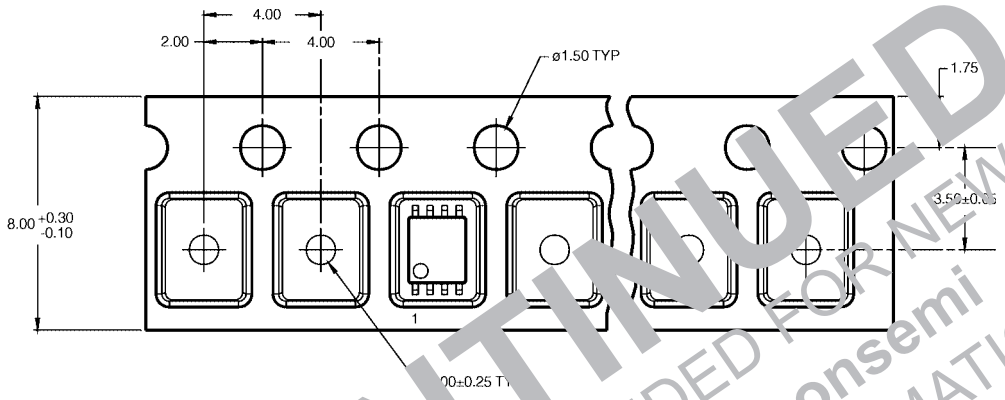
Tape and Reel Specification

TAPE FORMAT for US8

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
K8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

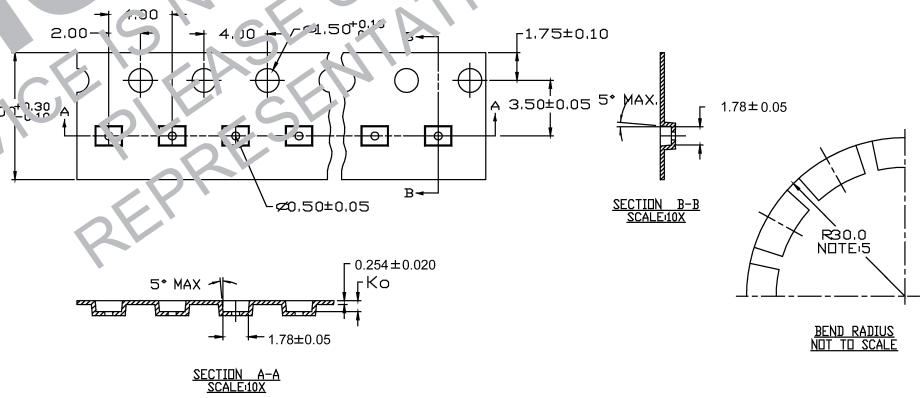
TAPE DIMENSIONS inches (millimeters)



TAPE FORMAT for MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



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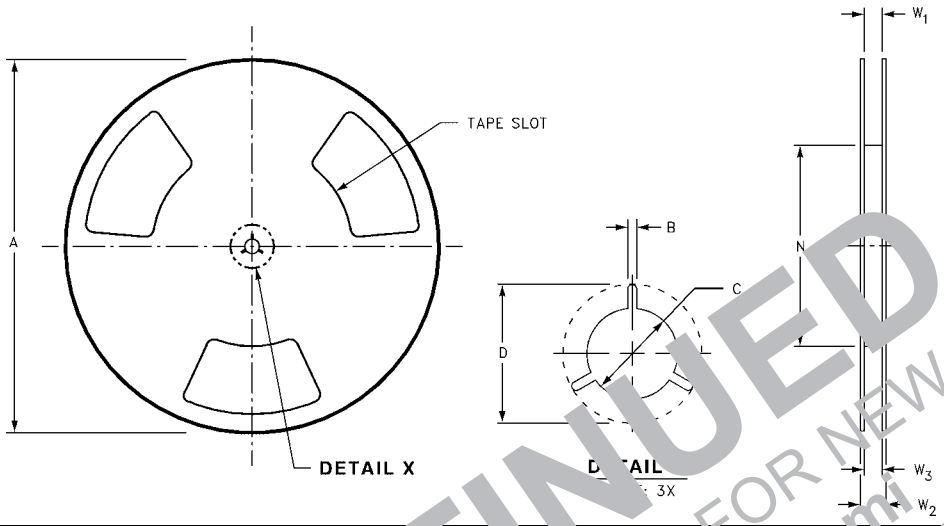
Tape and Reel Specification (Continued)

REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	[illegible]	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 ([illegible].20)	2.165 ([illegible].00)	[illegible]31 + 0.059/–0.000 ([illegible]0 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

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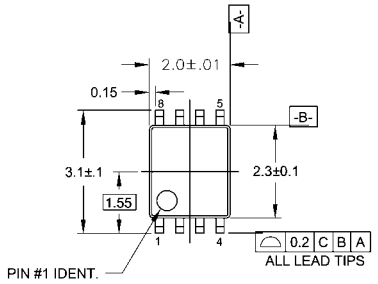
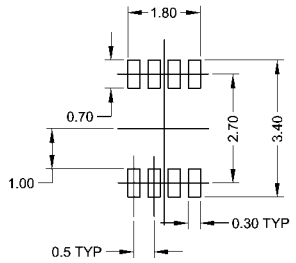
Physical Dimensions inches (millimeters) unless otherwise noted





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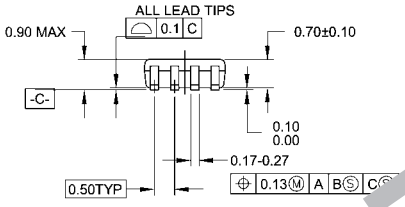

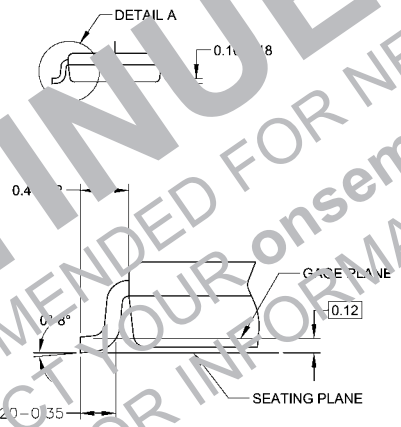

DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, TIE BAR EXTRUSIONS.
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982.

M08AREVC

8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide
Package Number MAB08A

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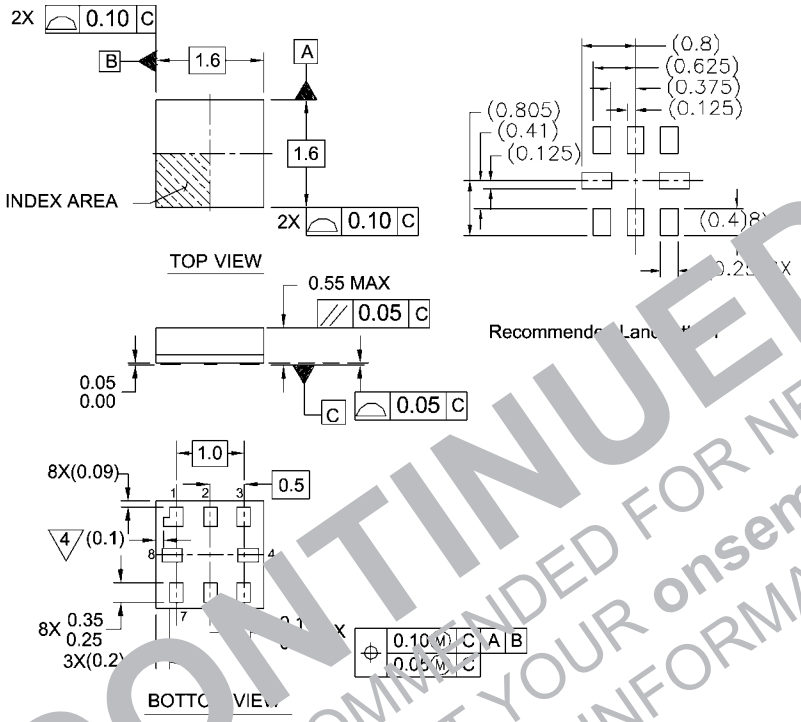
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:
1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONING CONFORMS TO ASME Y14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET.

MAC08AREVC

Pb-Free 8-Lead MicroPak, 1.6 mm Wide
Package Number MAC08A

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