TMUX4827 ±12V Beyond the Supply, 2:1 (SPDT) 2-Channel, Power-Off Protection Switch, with 0.13Ω Ron and 1.8V Compatible Logic

1 Features

- Supply range: 1.8 to 5.5V
- Beyond the supply signal range: -12V to 12V
- High current support: >1A (maximum)
- Ultra-low on-resistance: 0.13Ω
- Low on-resistance flatness: 1.0mΩ
- Low THD+N: 0.001% (-100dB)
- –40°C to +125°C operating temperature
- Powered off protection
- Over temperature protection
- 1.8V logic compatible
- Fail-safe logic
- Break-before-make switching

2 Applications

- Audio input or output switching
- Ultrasonic gas flow transmitters
- Analog input modules
- Industrial module detection

3 Description

The TMUX4827 is a complementary metal-oxide semiconductor (CMOS) multiplexer with 2 selectable 2:1, single-pole, double-throw (SPDT) switch channels. This device works with a single supply (1.8 to 5.5V), but can pass bidirectional analog and digital signals beyond the supply from -12V to 12V.

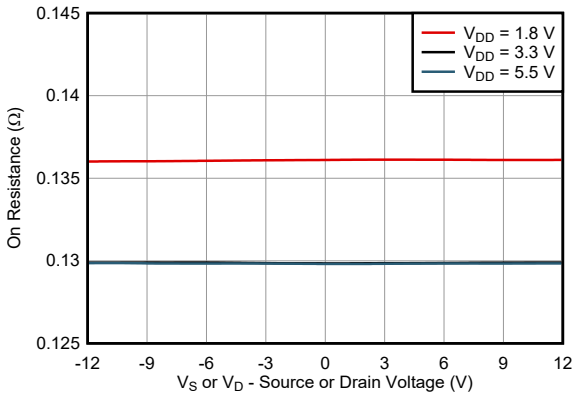
The TMUX4827 also features bidirectional powered off protection up to ±12V, which isolates the switch even when there is no supply voltage present (V_{DD} = 0V). Without this protection feature, any voltage on the switch can back-power the supply rail through an internal ESD diode and cause potential damage to the rest of the system.

With 0.001% THD+N and 1mΩ R_{ON}-flatness, the TMUX4827 is an excellent choice for passing precision analog and audio signals without adding distortion.

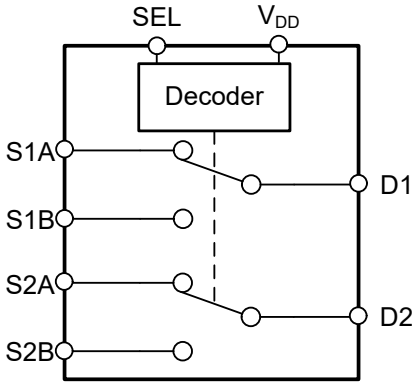
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMUX4827	YBH (DSBGA, 9)	1.6mm × 1.6mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



On-Resistance vs Source or Drain Voltage



TMUX4827 Block Diagram

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4 Pin Configuration and Functions

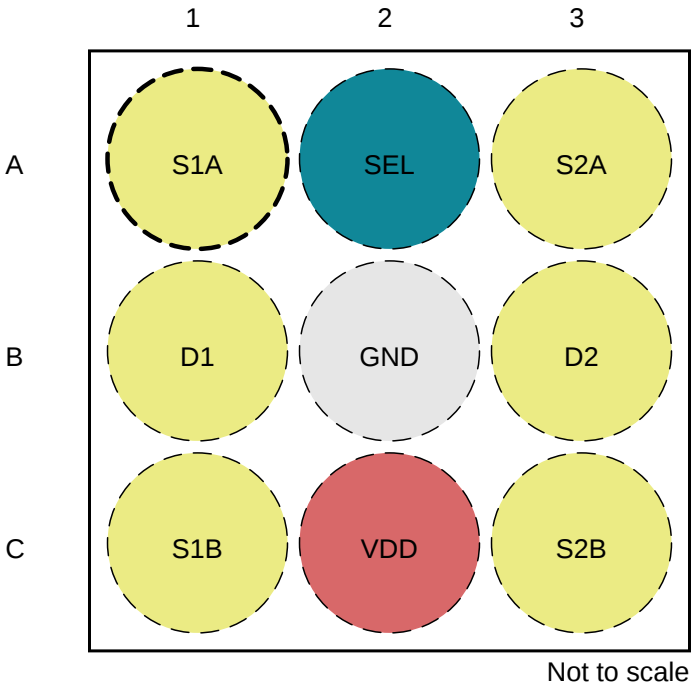


Figure 4-1. YBH Package, 9-Ball DSBGA (Top View, Bump Side Down)

Legend	
Power	Input
Input or Output	Ground

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
A1	S1A	I/O	Source pin 1A. Can be an input or output.
A2	SEL	I	Logic control input. Controls the switch connection as provided in Table 7-1.
A3	S2A	I/O	Source pin 2A. Can be an input or output.
B1	D1	I/O	Drain pin 1. Can be an input or output.
B2	GND	GND	Ground (0V) reference
B3	D2	I/O	Drain pin 2. Can be an input or output.
C1	S1B	I/O	Source pin 1B. Can be an input or output.
C2	VDD	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between VDD and GND. Controls the switch connection as provided in Table 7-1
C3	S2B	I/O	Source pin 2B. Can be an input or output.

(1) I = input, I/O = input or output, GND = ground, P = power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{DD} to GND	Supply voltage	-0.5	6	V
V_{SEL} to GND	Logic control input pin voltage	-0.5	6	V
V_S or V_D to GND	Source or drain voltage (Sx, Dx) to ground	-13	13	V
V_S to V_D or V_S	Source to drain or source (same channel)(4)	-15	15	V
	Source to drain or source (seperate channel)(3)	-24	24	V
I_{SEL}	Logic control input pin current	-30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, Dx)		I_{DC} + 10 %(5)	mA
T_A	Ambient temperature	-55	150	°C
T_{stg}	Storage temperature	-65	150	°C
T_J	Junction temperature		150	°C
P_{tot}	Total power dissipation(6)		750	mW

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Maximum voltage between source and drain pins within the same channel. For example: S1A to D1 or S1A to S1B
(5) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.
(6) For WCSP package: P_{tot} derates linearly above T_A = 70°C by 9.4mW/°C.

5.2 ESD Ratings

				VALUE	UNIT
TMUX4827					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±3000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)		±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC[1]		TMUX4827 (YBH) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive power supply voltage	1.8[1]		5.5	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	-12		12	V
V_{SEL}	Address/Select pin voltage	0		5.5	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)			I_{DC} [2]	A
T_A	Ambient temperature	-40		125	°C

(1) Device operational ±10% of minimum V_{DD} down to 1.6V
(2) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

5.5 Source or Drain Continuous Current

V_{DD} = 3.3V, GND = 0V (unless otherwise noted)

CONTINUOUS CURRENT PER CHANNEL (I_{DC}) [1]				
PACKAGE	25°C	85°C	125°C	UNIT
YBH	1.1	0.87	0.4	A

(1) Refer to Total power dissipation (P_{tot}) limits in A*bsolute Maximum Ratings* table that must be followed with max continuous current specification.

5.6 Source or Drain RMS Current

V_{DD} = 3.3V, GND = 0V (unless otherwise noted)

RMS CURRENT PER CHANNEL (I_{RMS}) [1]				
PACKAGE	25°C	85°C	125°C	UNIT
YBH	1.1	1.1	0.68	A

(1) Refer to Total power dissipation (P_{tot}) limits in A*bsolute Maximum Ratings* table that must be followed with max RMS current specification.

5.7 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)
Typical at V_{DD} = 3.3V T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_{DD} = 2.5V to 5.5V V_S = –12V to +12V I_D = –100mA	25°C		0.13	0.16	Ω
			–40°C to +85°C			0.225	Ω
			–40°C to +125°C			0.250	Ω
R_{ON}	On-resistance	V_{DD} = 1.8V to 2.5V V_S = –12V to +12V I_D = –100mA	25°C		0.19	0.22	Ω
			–40°C to +85°C			0.25	Ω
			–40°C to +125°C			0.3	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_{DD} = 2.5V to 5.5V V_S = –12V to +12V I_D = –100mA	25°C		0.002	0.03	Ω
			–40°C to +85°C			0.03	Ω
			–40°C to +125°C			0.05	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_{DD} = 1.8V to 2.5V V_S = –12V to +12V I_D = –100mA	25°C		0.003	0.035	Ω
			–40°C to +85°C			0.04	Ω
			–40°C to +125°C			0.06	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_{DD} = 2.5V to 5.5V V_S = –12V to +12V I_D = –100mA	25°C		0.001	0.01	Ω
			–40°C to +85°C			0.05	Ω
			–40°C to +125°C			0.07	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_{DD} = 1.8V to 2.5V V_S = –12V to +12V I_D = –100mA	25°C		0.003	0.015	Ω
			–40°C to +85°C			0.07	Ω
			–40°C to +125°C			0.09	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0V, I_S = –100mA	–40°C to +125°C		0.001		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off V_S = ±12V / 0V V_D = 0V / ±12V	25°C		0.02		uA
			–40°C to +85°C	-0.1		0.1	uA
			–40°C to +125°C	-1		1	uA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	Switch state is on V_S = V_D = ±12V	25°C		0.02		uA
			–40°C to +85°C	-0.1		0.1	uA
			–40°C to +125°C	-1		1	uA
$I_{S(POFF)}$	Source powered-off leakage current(1)	V_{DD} = 0V V_S = ±12V / 0V V_D = 0V / ± 12V	25°C		0.02		uA
			–40°C to +85°C	-0.1		0.1	uA
			–40°C to +125°C	-2		2	uA
$I_{D(POFF)}$	Drain powered-off leakage current(1)	V_{DD} = 0V V_S = ±12V / 0V V_D = 0V / ± 12V	25°C		0.02		uA
			–40°C to +85°C	-0.1		0.1	uA
			–40°C to +125°C	-2		2	uA

5.7 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)
Typical at V_{DD} = 3.3V T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.1		5.5	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.6	V
I_{IH}	Input leakage current		–40°C to +125°C		1	80	nA
I_{IL}	Input leakage current		–40°C to +125°C	-10	-1		nA
C_{IN}	Logic input capacitance		–40°C to +125°C		5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0V, 5V, or V_{DD}	25°C		55	125	µA
			–40°C to +85°C			130	µA
			–40°C to +125°C			140	µA

(1) When V_S is at a voltage potential, V_D is 0V, or when V_S is 0V, V_D is at a voltage potential.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.8 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)
Typical at V_{DD} = 3.3V T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_{DD} = 2.5V to 5.5V V_S = 3.3V R_L = 50Ω, C_L = 35pF	25°C		8	185	us
			–40°C to +85°C			220	us
			–40°C to +125°C			220	us
t_{TRAN}	Transition time from control input	V_{DD} = 1.8V to 2.5V V_S = 3.3V R_L = 50Ω, C_L = 35pF	25°C		10	340	us
			–40°C to +85°C			490	us
			–40°C to +125°C			490	us
t_{BBM}	Break-before-make time delay	V_{DD} = 2.5V to 5.5V V_S = 3.3V R_L = 50Ω, C_L = 35pF	25°C	40		300	us
			–40°C to +85°C	40		300	us
			–40°C to +125°C	40		300	us
t_{BBM}	Break-before-make time delay	V_{DD} = 1.8V to 2.5V V_S = 3.3V R_L = 50Ω, C_L = 35pF	25°C	40		420	us
			–40°C to +85°C	40		490	us
			–40°C to +125°C	40		490	us
$t_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1µs R_L = 50Ω, C_L = 35pF	25°C		175		us
Q_{INJ}	Charge injection	V_S = 0V, C_L = 100pF	25°C		5		pC
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 200 mV_{RMS}, V_{BIAS} = 0V, f = 100kHz	25°C		-55		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 200mV_{RMS}, V_{BIAS} = 0V, f = 100kHz	25°C		-100		dB
BW	–3dB Bandwidth	R_L = 50Ω , C_L = 5pF V_S = 200 mV_{RMS}, V_{BIAS} = 0V,	25°C		72		MHz
I_L	Insertion loss	R_L = 50Ω , C_L = 5pF V_S = 200 mV_{RMS}, V_{BIAS} = 0V, f = 1MHz	25°C		-0.01		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62V on V_{DD} R_L = 32Ω , C_L = 5pF, f = 20kHz	25°C		-80		dB
$C_{S(OFF)}$	Source off capacitance	V_S = 0V, f = 1MHz	25°C		70		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0V, f = 1MHz	25°C		40		pF
T_{SD}	Thermal shutdown				160		°C
T_{HYST}	Thermal hysteresis				20		°C

5.8 Switching Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)
Typical at V_{DD} = 3.3V T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 0.5V, V_{BIAS} = 0V R_L = 600Ω f = 20Hz to 20kHz	25°C		0.0006		%
			–40°C to +85°C		0.001		%
			–40°C to +125°C		0.001		%
			25°C		-105		dB
			–40°C to +85°C		-100		dB
			–40°C to +125°C		-100		dB
		V_{PP} = 0.5V, V_{BIAS} = 0V R_L = 32Ω f = 20Hz to 20kHz	25°C		0.0008		%
			–40°C to +85°C		0.001		%
			–40°C to +125°C		0.001		%
			25°C		-102		dB
			–40°C to +85°C		-100		dB
			–40°C to +125°C		-100		dB

5.9 Typical Characteristics

at T_A = 25°C (unless otherwise noted)

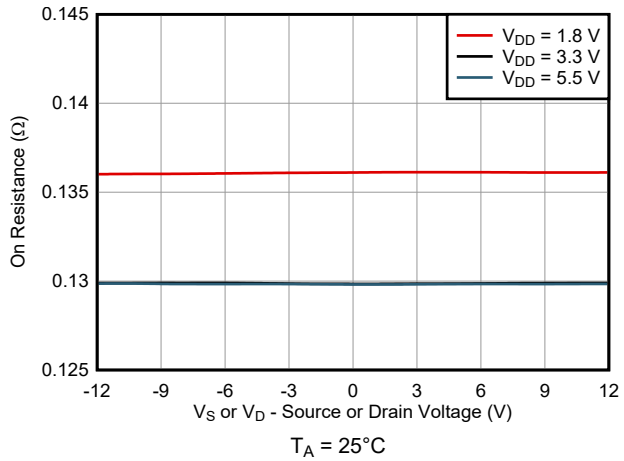


Figure 5-1. On-Resistance vs Source or Drain Voltage

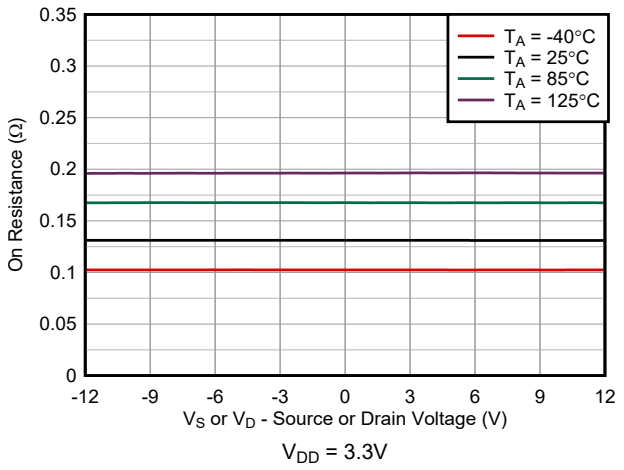


Figure 5-2. On-Resistance vs Temperature

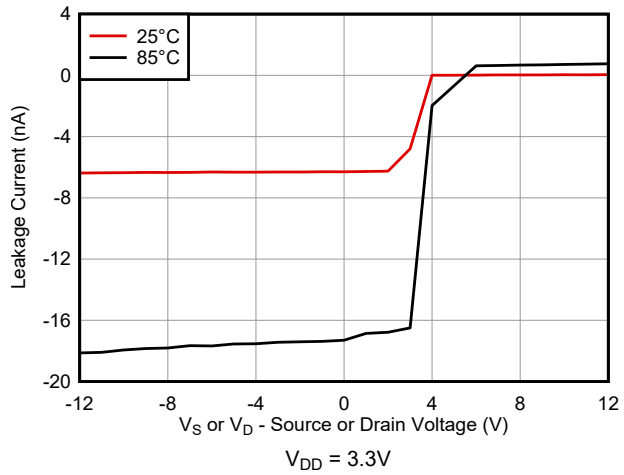


Figure 5-3. On Leakage Current vs Source or Drain Voltage

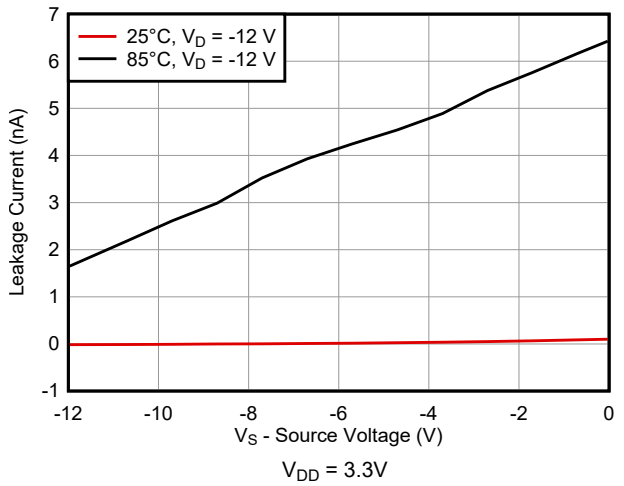


Figure 5-4. ISOFF Leakage vs Source Voltage

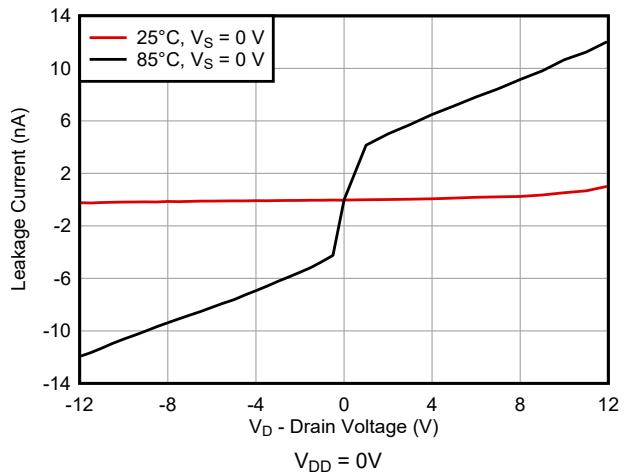


Figure 5-5. IDOFF Leakage vs Drain Voltage

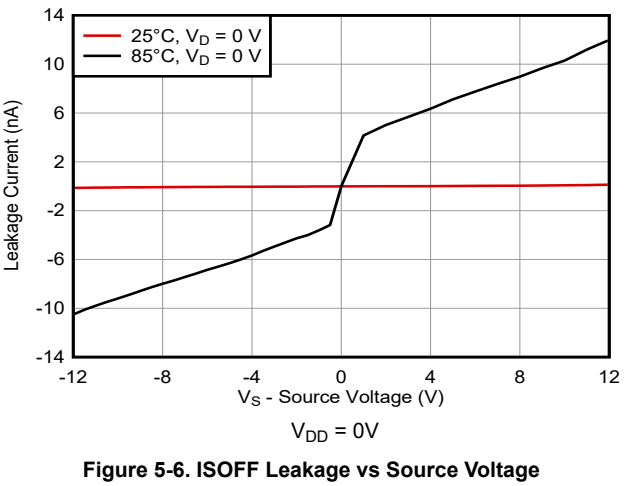
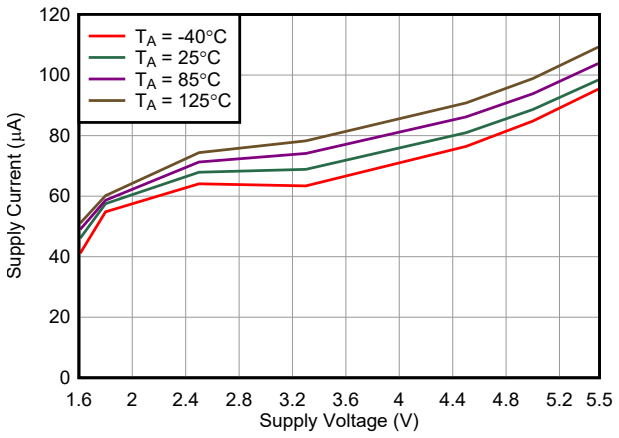


Figure 5-6. ISOFF Leakage vs Source Voltage

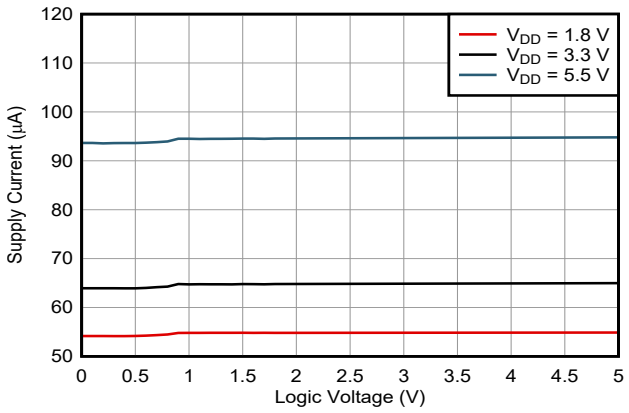
5.9 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



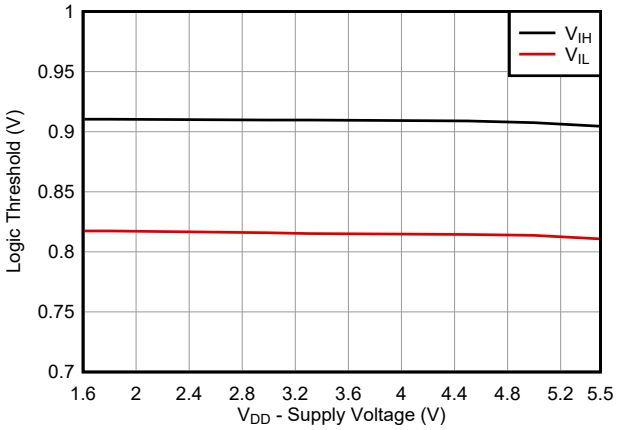
T_A = 25°C

Figure 5-7. Supply Current vs Supply Voltage



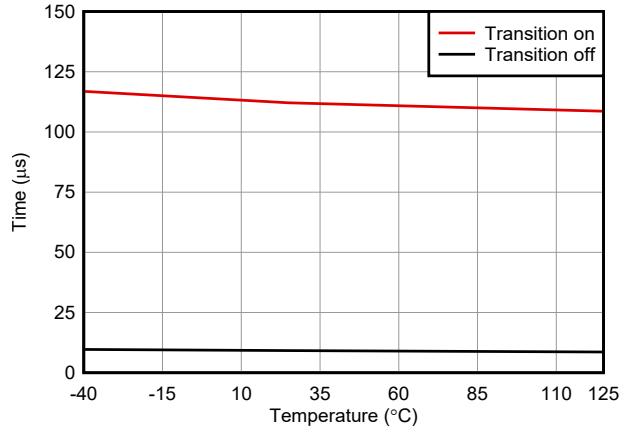
V_{DD} = 3.3V

Figure 5-8. Supply Current vs Logic Voltage



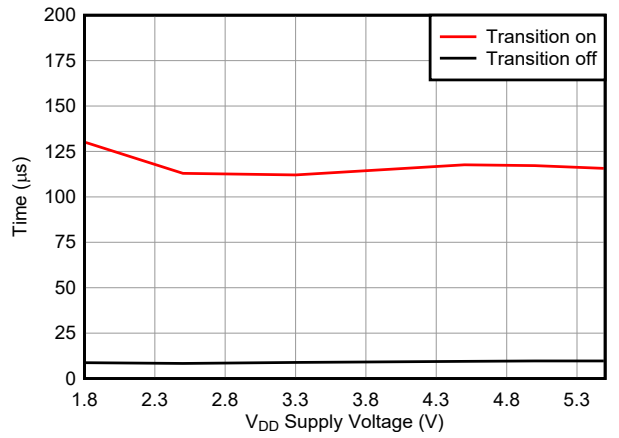
T_A = 25°C

Figure 5-9. Logic Threshold vs Supply Voltage



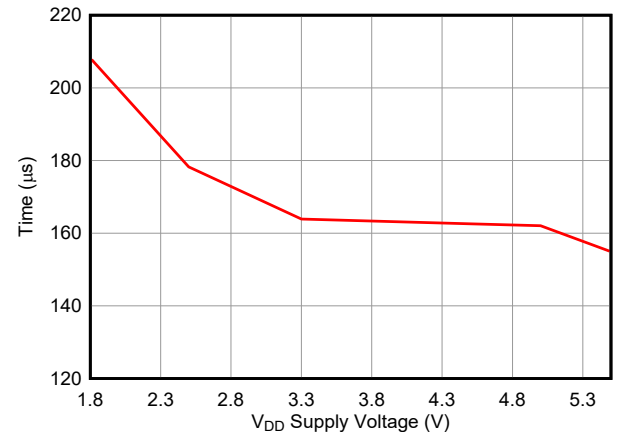
V_{DD} = 3.3V

Figure 5-10. Transition Time vs Temperature



T_A = 25°C

Figure 5-11. Transition Time vs Supply Voltage



T_A = 25°C

Figure 5-12. tBBM vs Supply Voltage

5.9 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

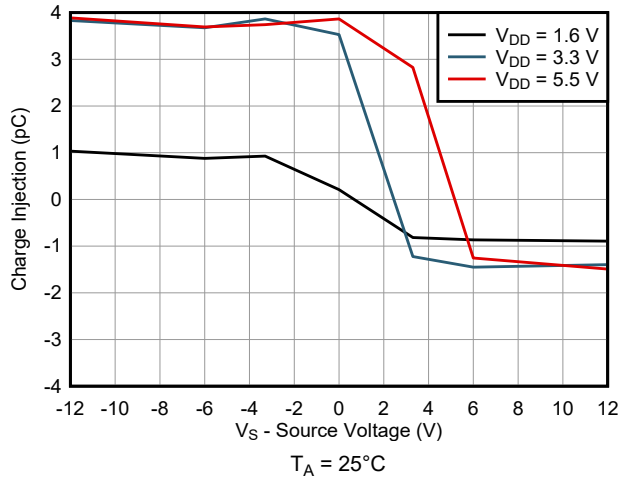


Figure 5-13. Charge Injection vs Source Voltage

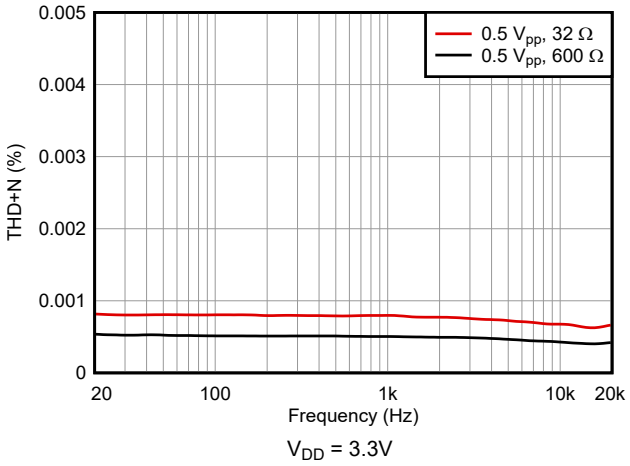


Figure 5-14. THD+N vs Frequency

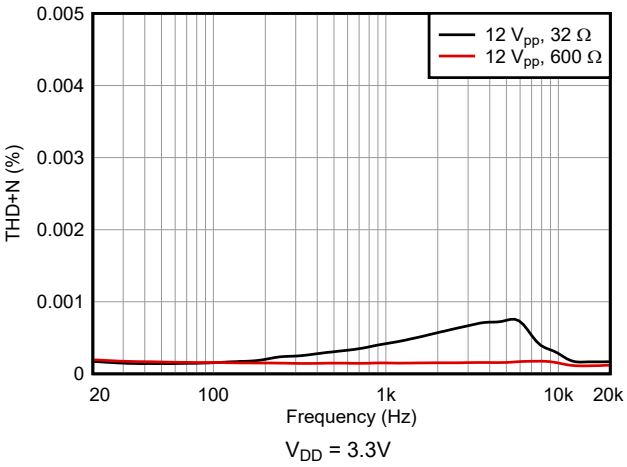


Figure 5-15. THD+N vs Frequency

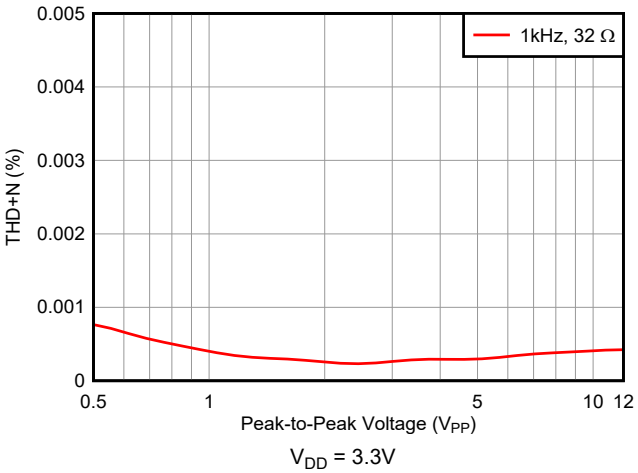


Figure 5-16. THD+N vs Peak-to-Peak Voltage

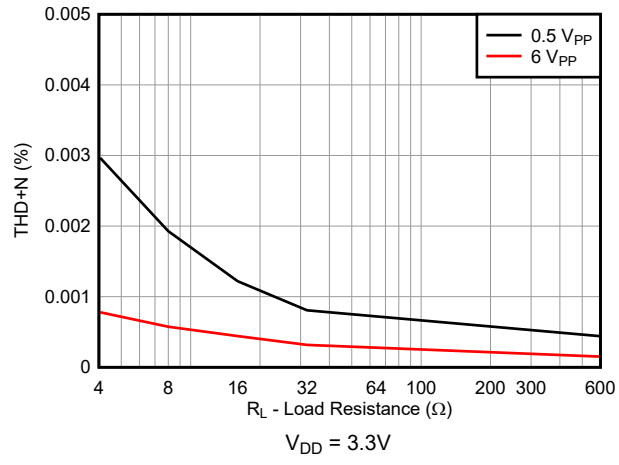


Figure 5-17. THD+N vs Load Impedance

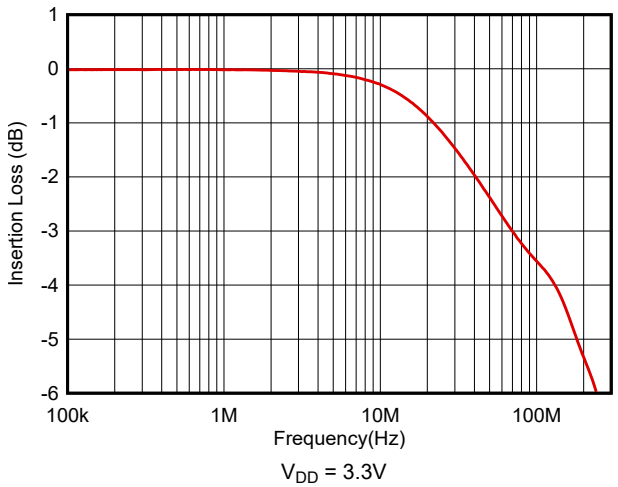
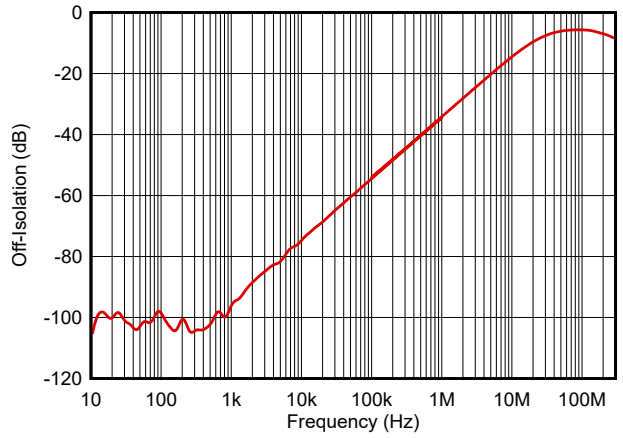


Figure 5-18. Insertion Loss vs Frequency

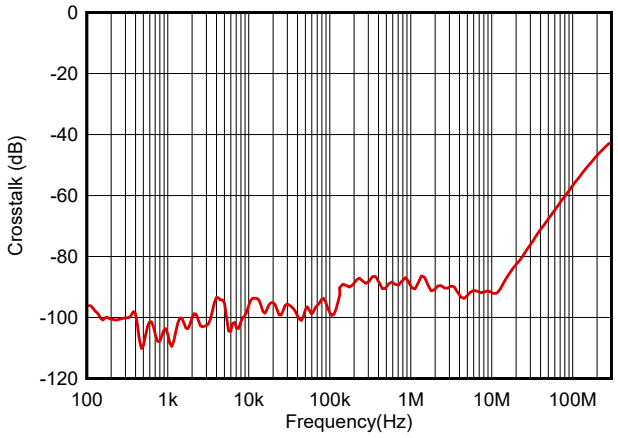
5.9 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



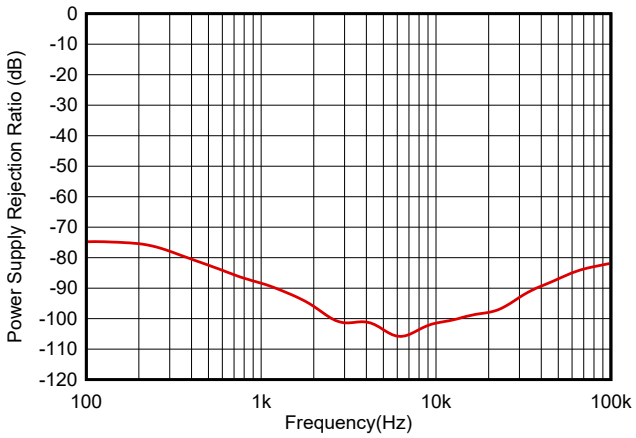
V_{DD} = 3.3V

Figure 5-19. Off Isolation vs Frequency



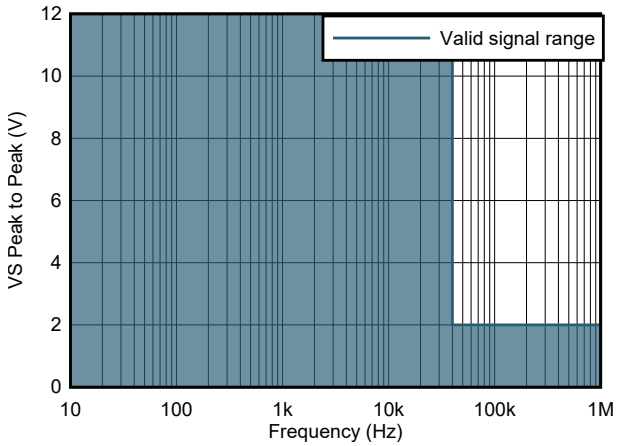
V_{DD} = 3.3V

Figure 5-20. Crosstalk vs Frequency



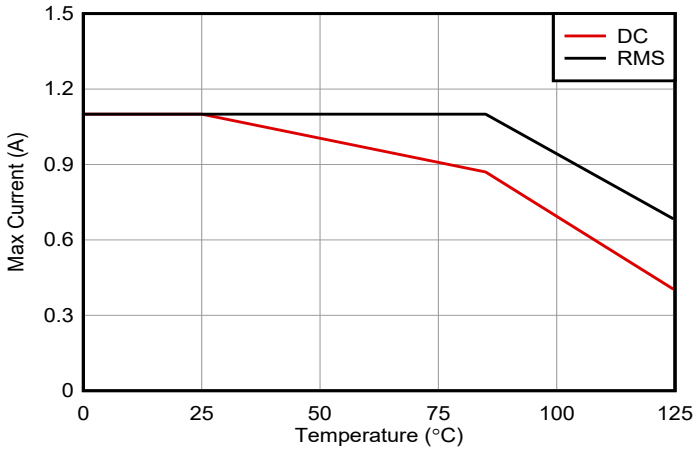
V_{DD} = 3.3V

Figure 5-21. ACPSRR vs Frequency



V_{DD} = 3.3V

Figure 5-22. Maximum Signal Swing



V_{DD} = 3.3V

Figure 5-23. Maximum Continuous Current vs Temperature

6 Parameter Measurement Information

6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. Figure 6-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$.

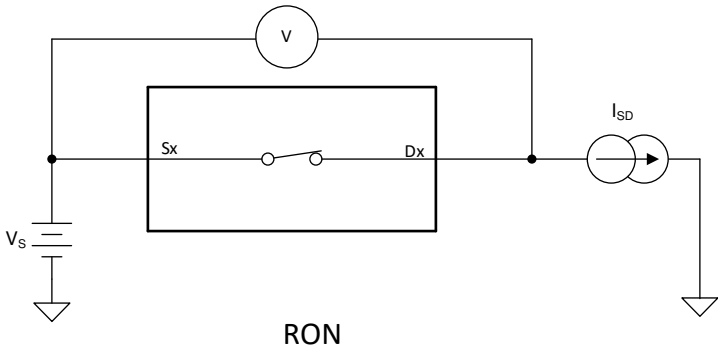


Figure 6-1. On-Resistance Measurement Setup

6.2 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$. Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$. Either the source pin or drain pin is left floating during the measurement. Figure 6-2 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

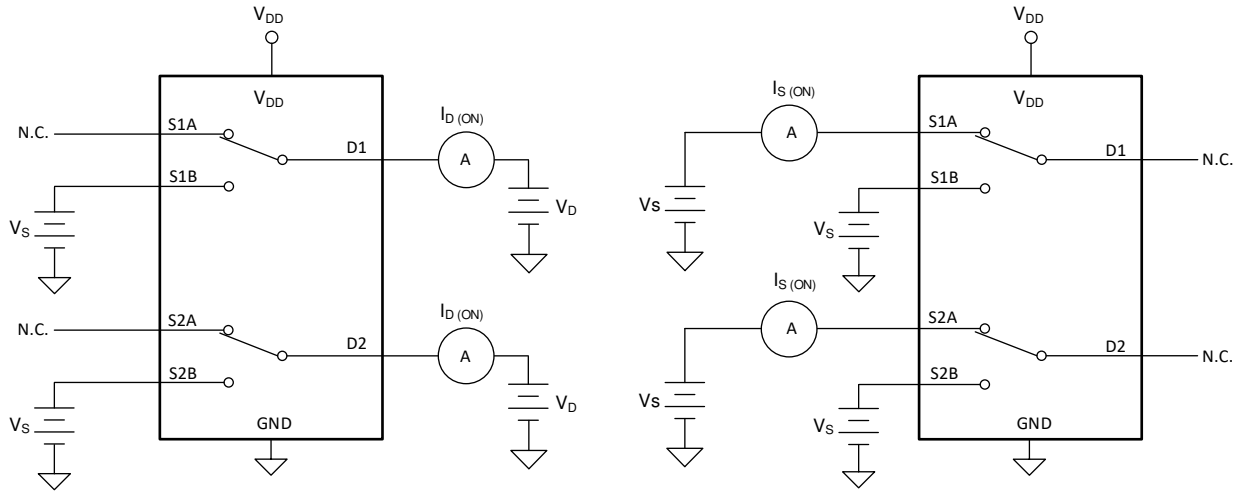


Figure 6-2. On-Leakage Measurement Setup

6.3 Off-Leakage Current

Source and drain off-leakage current is defined as the leakage current flowing into or out of the source or drain pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$ and $I_{D(OFF)}$. Figure 6-3 shows the setup used to measure off-leakage current.

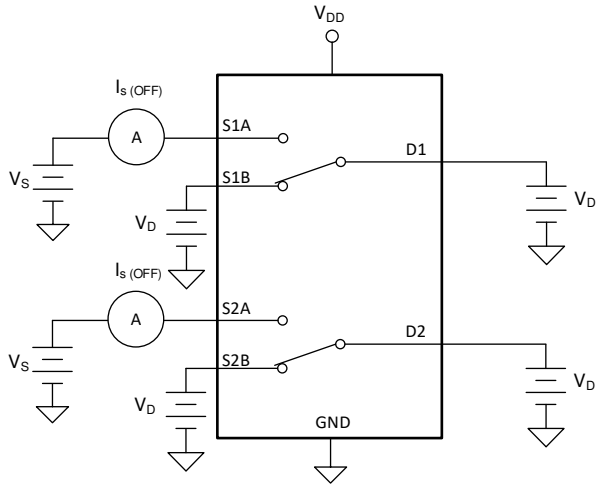


Figure 6-3. Off-Leakage Measurement Setup

6.4 Power-Off Leakage Current

Powered-off source and drain leakage current is defined as the leakage current flowing into or out of the source or drain pin when the device is powered off. This current is denoted by the symbol $I_{PS(OFF)}$ and $I_{PD(OFF)}$. Figure 6-4 shows the setup used to measure off-leakage current.

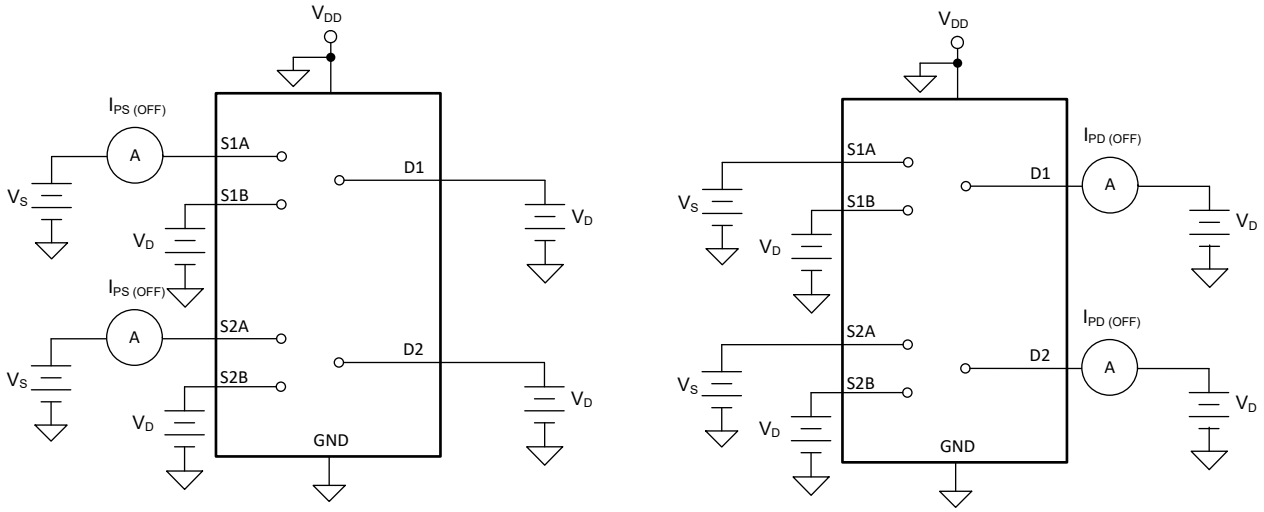


Figure 6-4. Power-Off Leakage Measurement Setup

6.5 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 6-5 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.

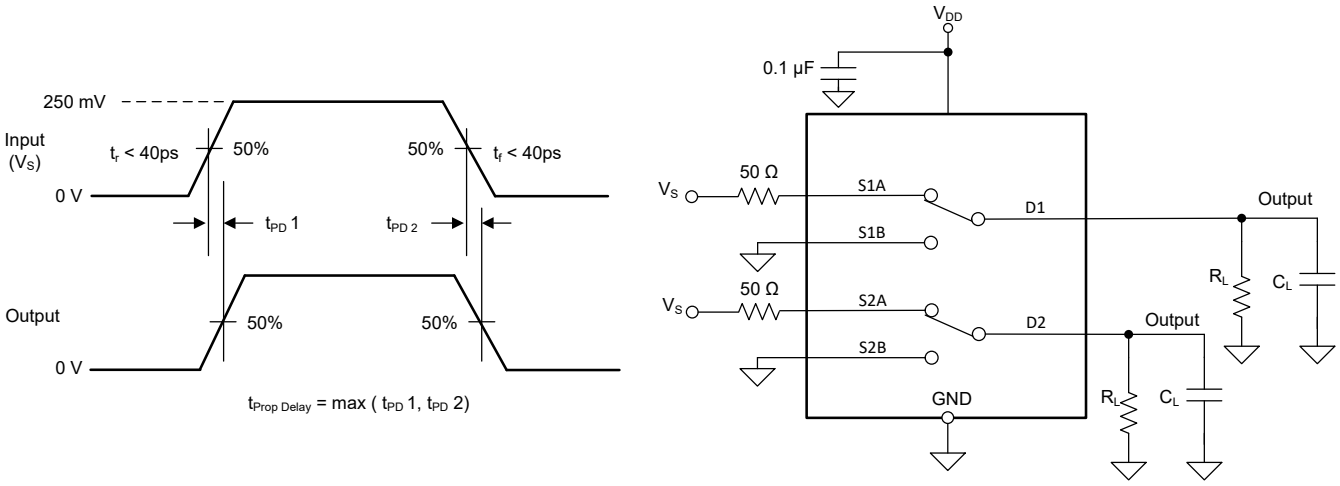


Figure 6-5. Propagation Delay Measurement Setup

6.6 $t_{ON\ (VDD)}$ and $t_{OFF\ (VDD)}$ Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. Figure 6-6 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$

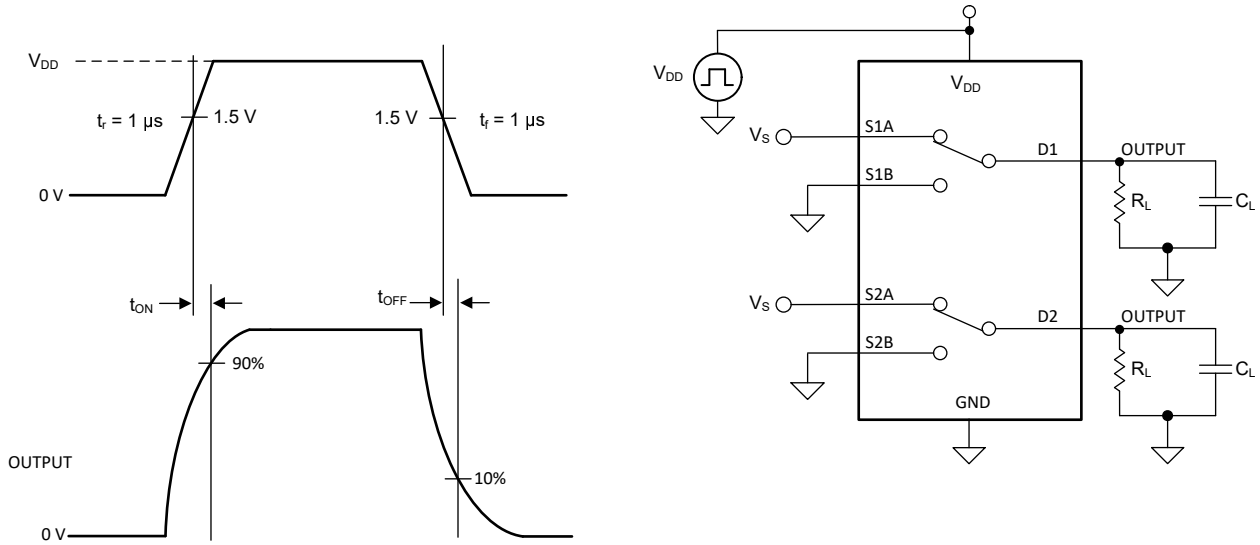


Figure 6-6. $t_{ON\ (VDD)}$ and $t_{OFF\ (VDD)}$ Time Measurement Setup

6.7 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the control signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-7 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

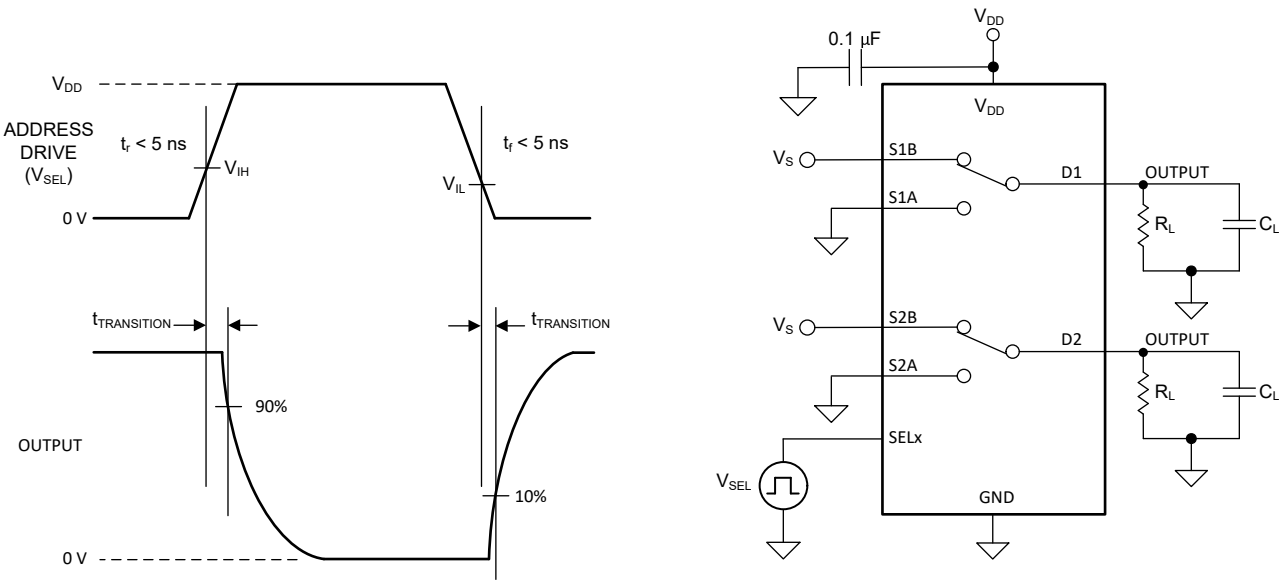


Figure 6-7. Transition-Time Measurement Setup

6.8 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 6-8 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

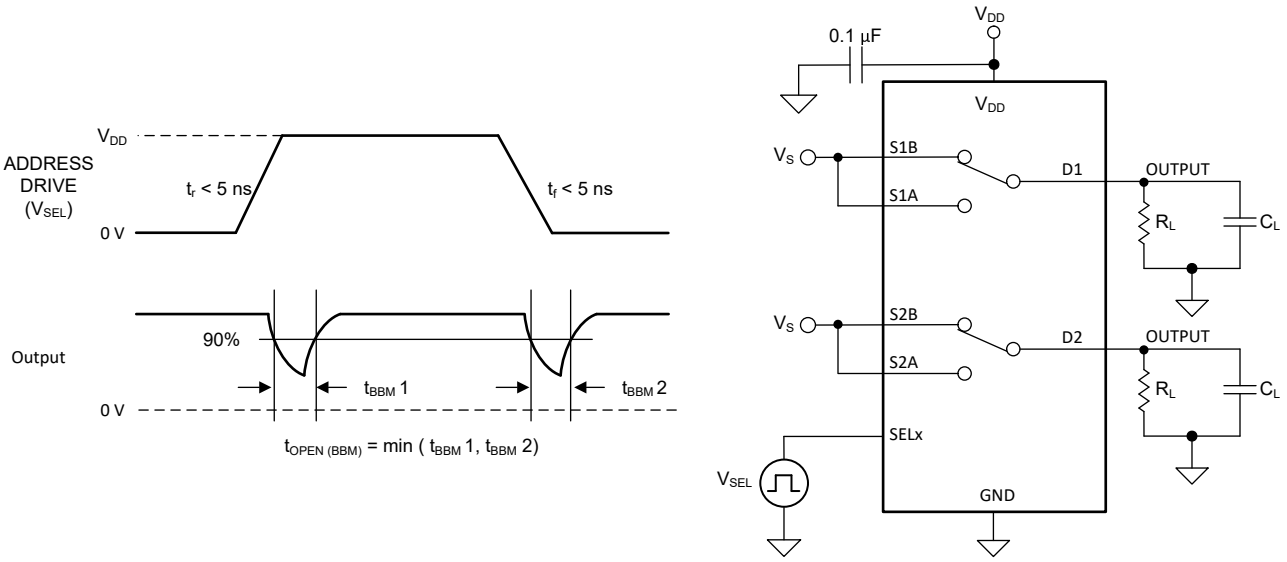


Figure 6-8. Break-Before-Make Delay Measurement Setup

6.9 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD + N.

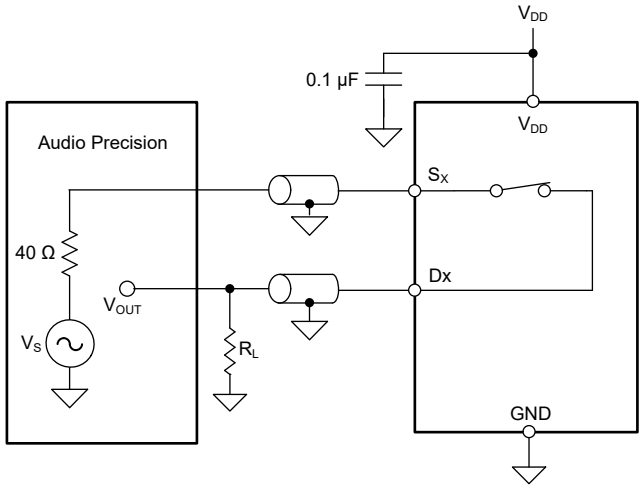


Figure 6-9. THD + N Measurement Setup

6.10 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 100 mV_{PP}. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR.

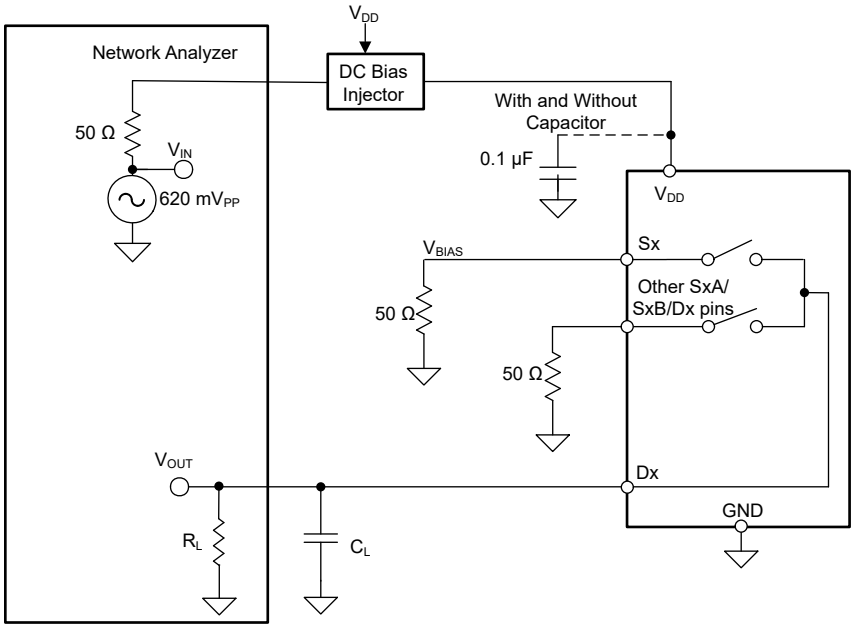


Figure 6-10. AC PSRR Measurement Setup

6.11 Charge Injection

Any mismatch in capacitance results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. Figure 6-11 shows the setup used to measure charge injection from Drain (D) to Source (Sx).

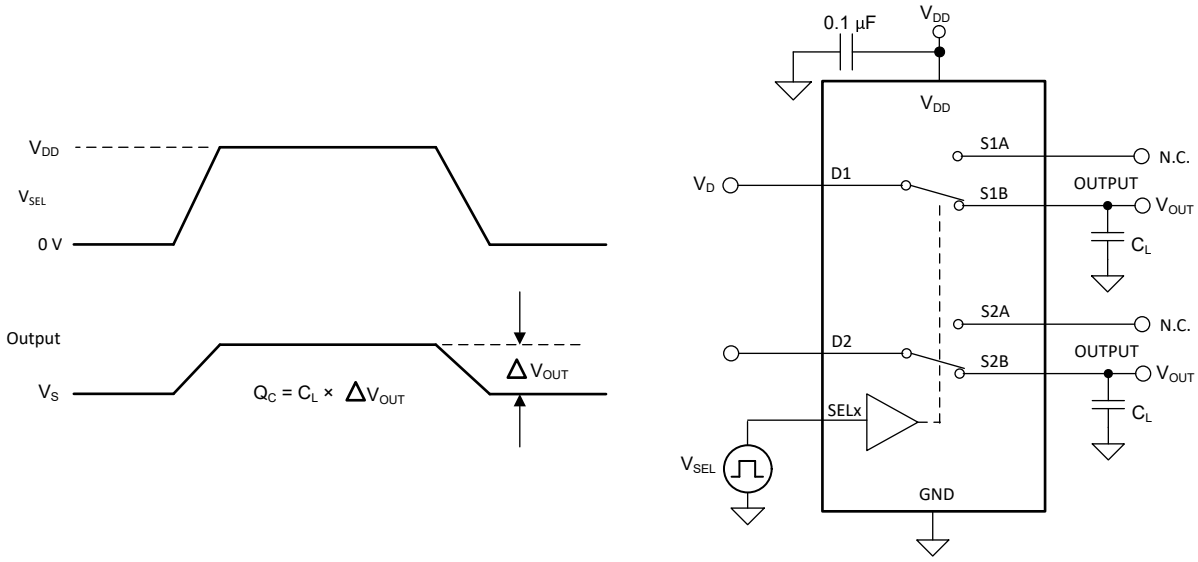


Figure 6-11. Charge Injection Measurement Setup

6.12 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. Figure 6-12 shows the setup used to measure bandwidth.

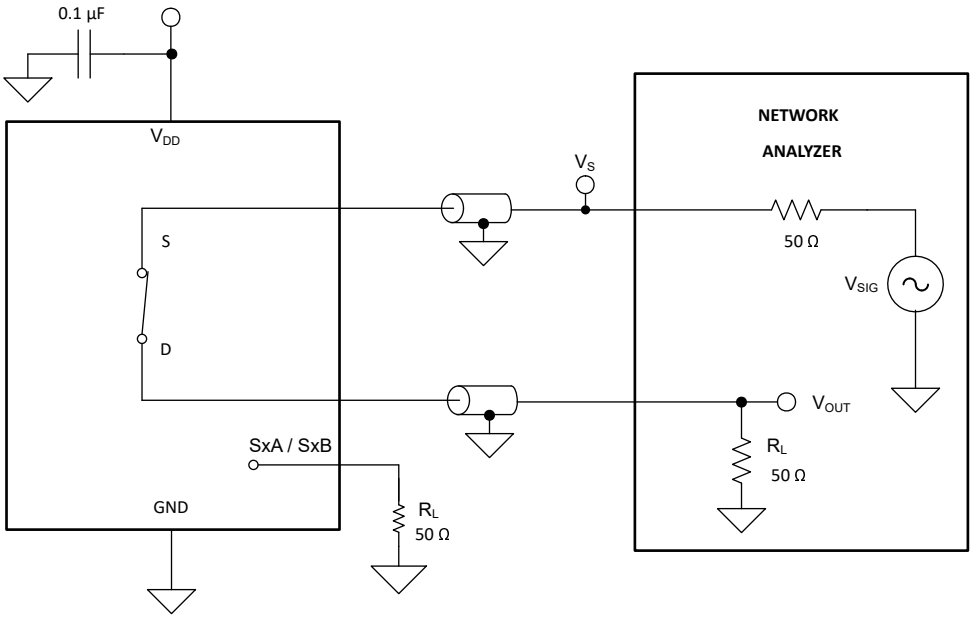


Figure 6-12. Bandwidth Measurement Setup

6.13 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 6-13 shows the setup used to measure, and the equation used to calculate off isolation.

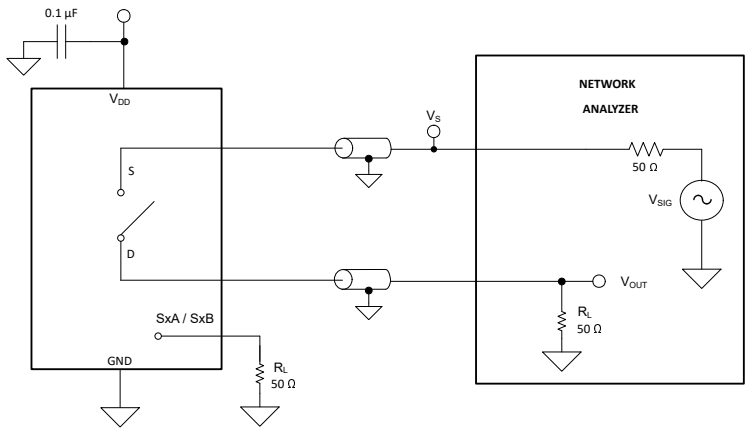


Figure 6-13. Off Isolation Measurement Setup

$$Off\ Isolation\ =\ 20\ \times\ Log\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

6.14 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. Figure 6-14 shows the setup used to measure, and the equation used to calculate crosstalk.

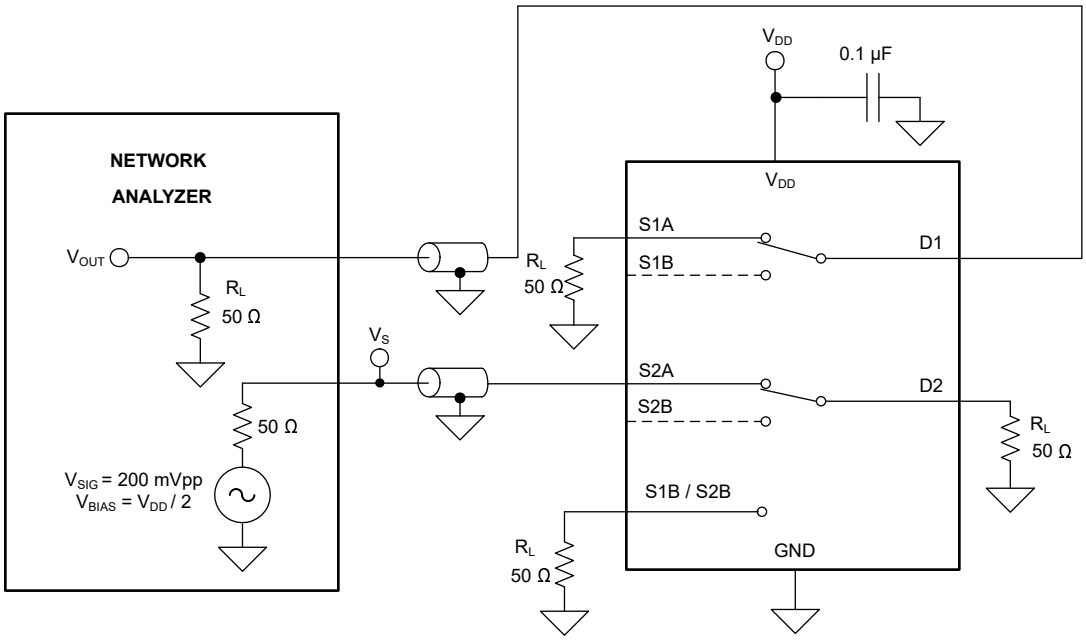


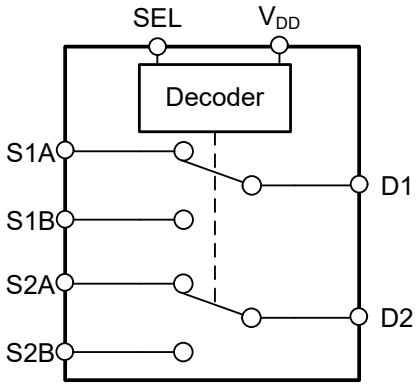
Figure 6-14. Crosstalk Measurement Setup

$$Channel-to-Channel\ Crosstalk\ =\ 20\ \times\ Log\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

7 Detailed Description

7.1 Functional Block Diagram

The TMUX4827 is an 2:1, 2-channel multiplexer or demultiplexer. Each input is turned on or turned off based on the state of the address lines and V_{DD} pin.



7.2 Device Functional Modes

Table 7-1 provides the truth table for the TMUX4827.

Table 7-1. TMUX4827 Truth Table

VDD	SEL	Selected Input Connected To Drain (D) Pin
0	X(1)	All channels are off (Hi-Z). Device is in power-off protection.
1	0	SxA
1	1	SxB

(1) X denotes *do not care*.

7.3 Feature Description

7.3.1 Beyond the Supply

The TMUX4827 supports signal voltages beyond the supply on the source (Sx) and drain (Dx) pins up to ±12V. This feature allows both AC and DC bidirectional signals above Vdd and below ground to pass through the switch without distortion, using a unidirectional supply. The device remains within the performance mentioned in the *Electrical Characteristics*.

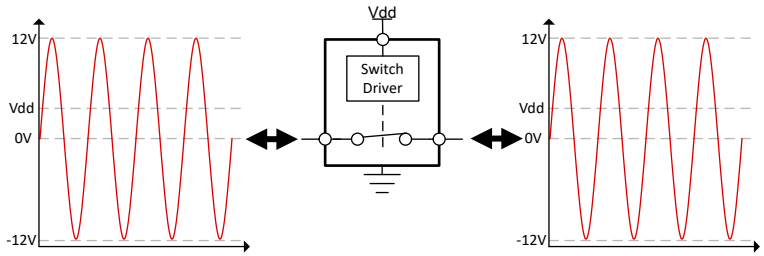


Figure 7-1. Beyond the Supply Signal Support

7.3.2 Bidirectional Operation

The TMUX4827 conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

7.3.3 Over Temperature Protection

Since the TMUX4827 has such a low on-resistance, large continuous currents can be passed through the switch with minimal attenuation. This can cause the device to self heat and may cause damage or instability. To prevent this, the TMUX4827 has integrated over-temperature protection. When the internal temperature reaches 150°C, the switch opens and the device will stop self heating. The over temperature performance is specified within the *Electrical Specifications* table.

7.3.4 Power-Off Protection

The TMUX4827 has powered-off protection up to ±12V on the switch path. This keeps the switch in a high impedance mode and isolates the source (Sx) and drain (Dx) pins when the supply is removed (Vdd = 0V). Powered-off protection minimizes system complexity by removing the need for power supply sequencing on the signal path. The device performance remains within the leakage performance mentioned in the Electrical Specifications. For more information on powered-off protection, refer to *Eliminate Power Sequencing with Powered-off Protection Signal Switches*.

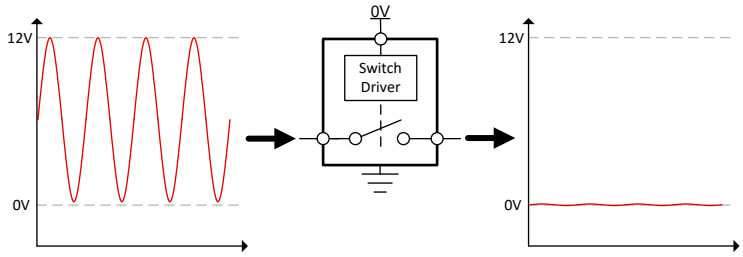


Figure 7-2. Beyond the Supply Signal Support

7.3.5 1.8V Logic Compatible Inputs

The TMUX4827 has 1.8V logic compatible control for all logic control inputs and the supply (V_{DD}). 1.8V logic level inputs allows the TMUX4827 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and bill of material (BOM) cost. For more information on 1.8V logic implementations, refer to Simplifying Design with 1.8V logic Muxes and Switches

7.3.6 Fail-Safe Logic

The TMUX4827 supports Fail-Safe Logic on the control input pin (SEL) allowing for operation up to 5.5V, regardless of the state of the supply pin. This feature allows voltages on the control pin to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the logic input pin of the TMUX4827 to be ramped to 5.5V while V_{DD} = 0V. The logic control input is protected against positive faults of up to 5.5V in powered-off condition, but does not offer protection against negative overvoltage conditions.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

TMUX4827 is part of the *beyond the supply switches and multiplexers* family of devices. This means that this device can switch signals from -12V to 12V with a low voltage supply from 1.8 to 5.5V. Additionally, the TMUX4827 features powered-off protection, which by design keeps the switches open even when there is no supply. This unique feature combination enables the TMUX4827 to be extremely versatile for a wide variety of applications such as boosted outputs and high common mode offsets.

8.2 Typical Applications

8.2.1 Audio Amplifier Switching

Often, there are multiple audio sources in a system giving the user options on which source will connect to the speaker. To enable switching between these sources, a TMUX4827 can be used. The line-in can be biased to a negative voltage, and class-D amplifier output can be higher than the typically used 3V and 5V supplies. So any circuitry connected needs to handle this bipolar voltage. This same scheme can be used in systems where there are multiple speaker outputs and one source as well. Here the switch is used to switch from an internal speaker to an external one. Figure 8-1 shows the block diagram for these applications. Here a TLV320AIC3x is used as an audio codec driving a TPA313x class D audio amplifier. Additionally, if IEC protection is needed on the external connectors (audio jack input or external speaker), then a 2 channel TPD2E007 can be used.

The TMUX4827 can be used to switch up to ±12V with a supply voltage from 1.8V to 5.5V. The supply can also be driven directly with a GPIO, allowing the user to put the device into ultra-low power mode. In this mode, the TMUX4827 operates with powered-off protection, so any high voltage present on the inputs will not propagate to the outputs. This feature allows for the correct power up cycling and increases system robustness. Additionally, the TMUX4827 features excellent THD+N performance, so there is minimal impact to the audio signal quality through the switch. This allows the system designer to save a significant portion of board area without impacting signal integrity.

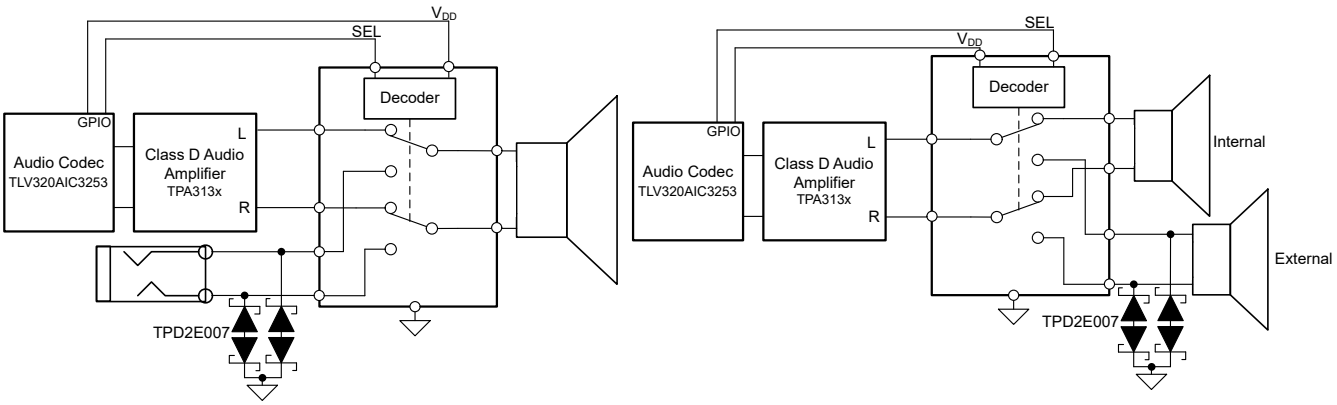


Figure 8-1. Audio Amplifier Switching

8.2.1.1 Design Requirements

Table 8-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	2.5V to 5.5V
MUX I/O signal range (V_S, V_D)	-12V to 12V (Beyond the Supply)
Control logic thresholds (V_{SEL})	1.8V to 5.5V

8.2.1.2 Detailed Design Procedure

The TMUX4827 can support bidirectional signals beyond the supply without any external components except for the supply decoupling capacitors. Figure 7-1 shows how the signal range is above and below the device supply range. Additionally with a very low on-resistance and an ultra flat response, the TMUX4827 has a very low THD+N as well as a reduced impact to DC losses and thermal self-heating. These features make the TMUX4827 designed for audio application.

8.2.1.3 Application Curves

The low on-resistance and ultra flat response enable the TMUX4827 to have an extremely low THD+N. This results in little to no impact in audio fidelity, even in high performance systems. This allows the system designed to save a significant portion of board area without impacting signal integrity.

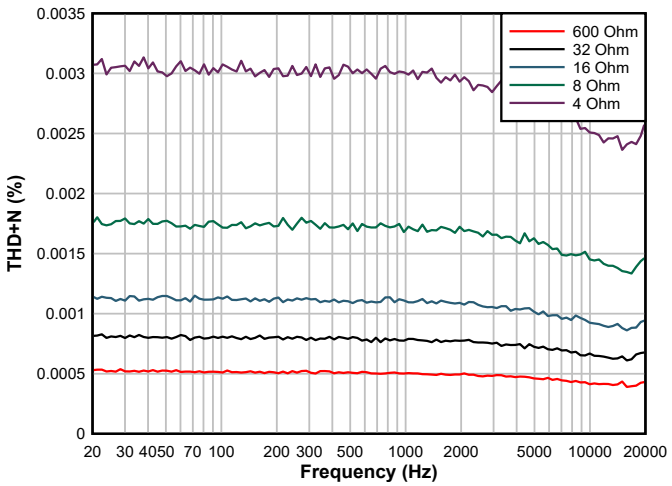


Figure 8-2. THD+N with Different Loading Conditions

Because this device has such a low on-resistance, it can be used in applications with very low output speaker impedance such as 8Ω or 4Ω systems. In these applications, the current through the switch can increase drastically, causing self heating.

8.3 Power Supply Recommendations

The TMUX4827 operates across a wide supply range from 1.8 to 5.5V, while supporting input or output signals from -12V to 12V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF at V_{DD} to ground. Place the bypass capacitors as close to the power supply pin of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes.

For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always confirm that the ground (GND) connection is established before supplies are ramped.

8.4 Layout

8.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 8-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

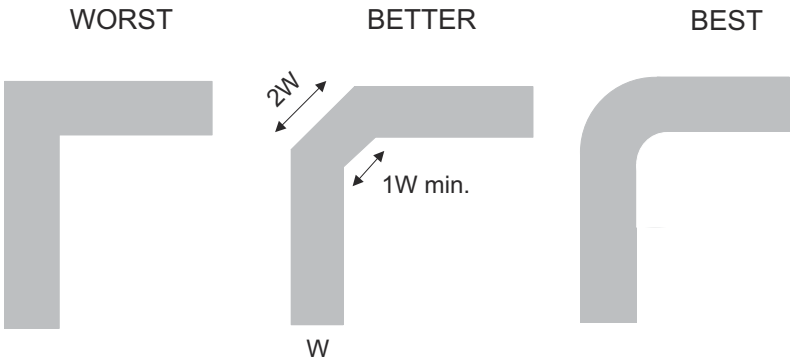


Figure 8-3. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Some key considerations are as follows:

- For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between VDD and GND. TI recommends a 0.1µF and 1µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

8.4.2 Layout Example

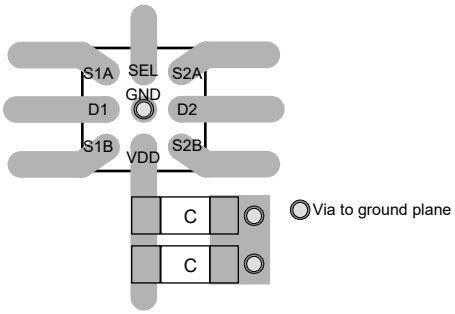


Figure 8-4. TMUX4827 Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches* application brief
- Texas Instruments, *Simplifying Design with 1.8V logic Muxes and Switches* application brief

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2023) to Revision B (July 2024)	Page
• Updated Mechanical Data	32

Changes from Revision * (May 2023) to Revision A (June 2023)	Page
• Changed the status of the data sheet from: *Advanced Information* to: *Production Data*	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Packaging Option Addendum

Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
TMUX4827YBHR	Active	DSBGA	YBH	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	MUX4827

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

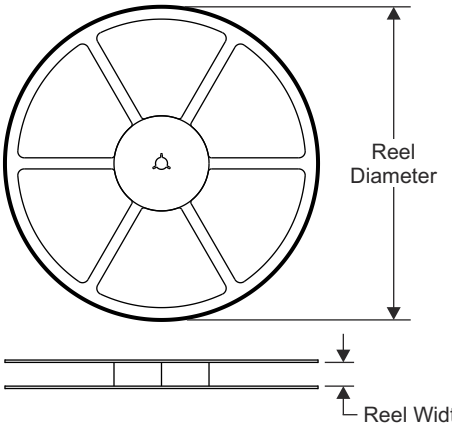
(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

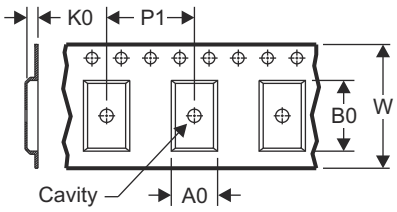
(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

11.2 Tape and Reel Information

REEL DIMENSIONS

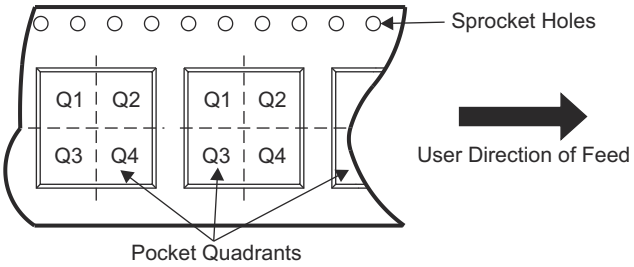


TAPE DIMENSIONS



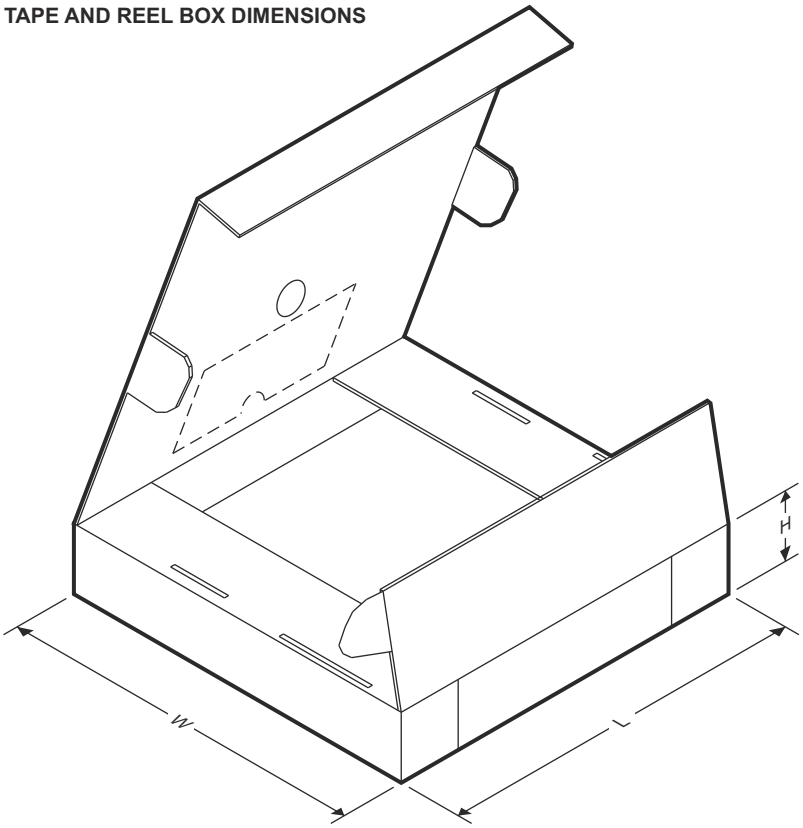
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX4827YBHR	DSBGA	YBH	9	3000	180.0	8.4	1.68	1.72	0.62	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX4827YBHR	DSBGA	YBH	9	3000	182.0	182.0	20.0

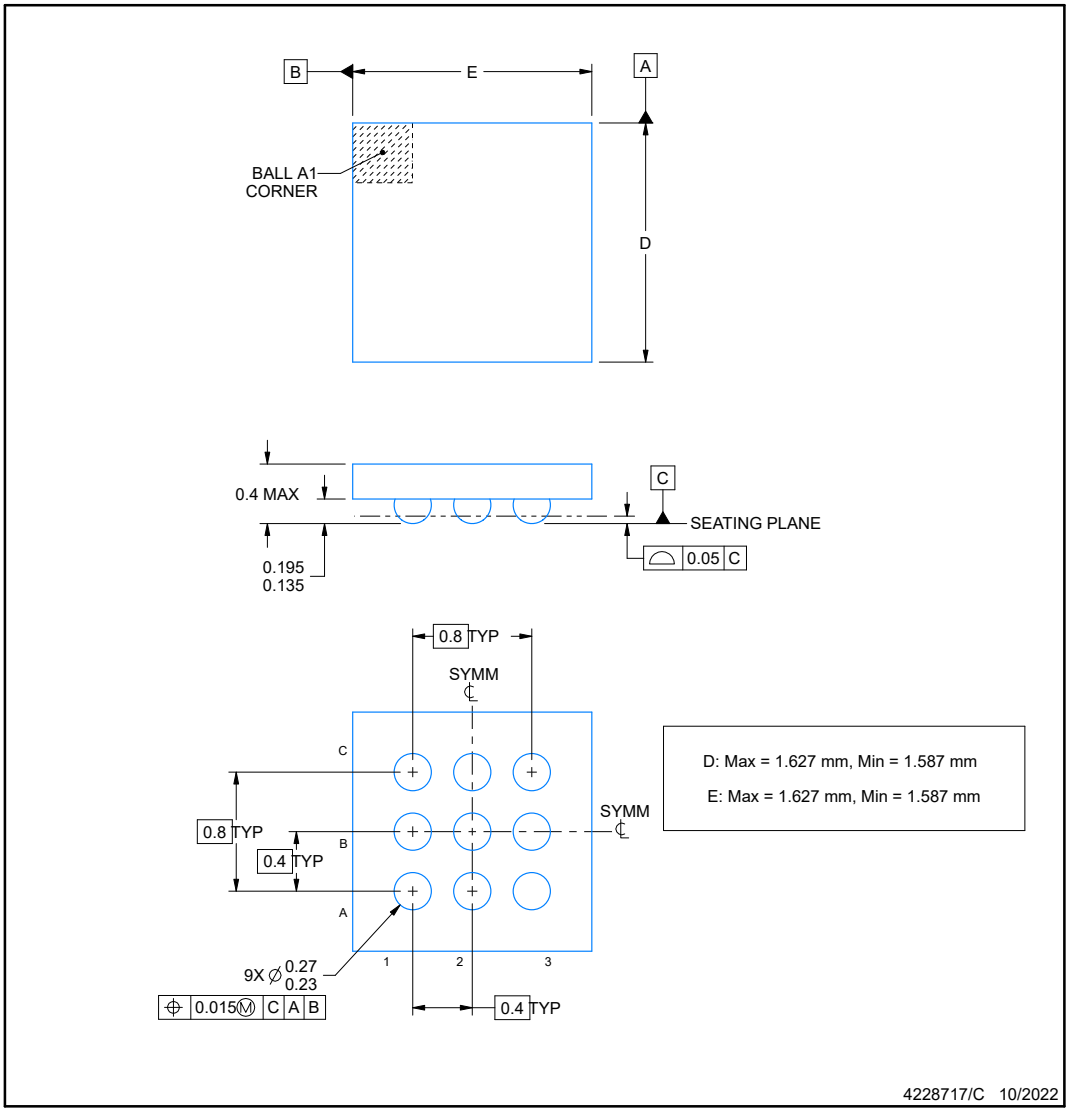
11.3 Mechanical Data

YBH0009-C02

PACKAGE OUTLINE

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

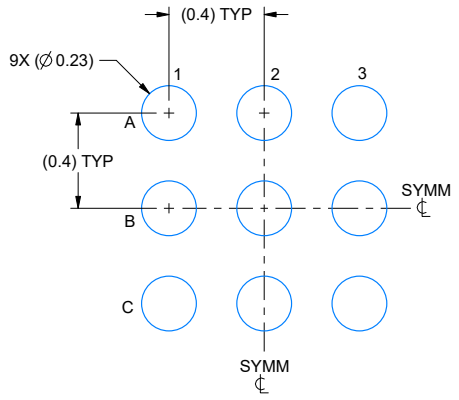
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

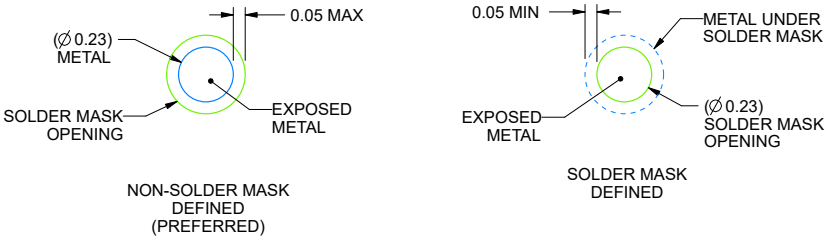
YBH0009-C02

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

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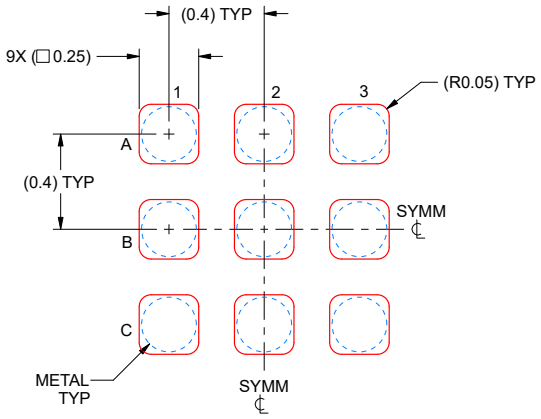
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YBH0009-C02 **DSBGA - 0.4 mm max height**

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX4827YBHR	Active	Production	DSBGA (YBH) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	MUX4827

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

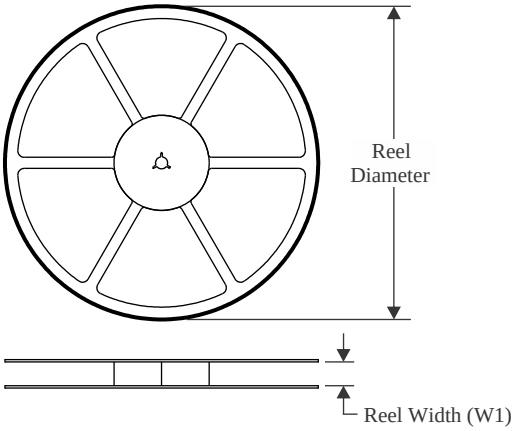
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

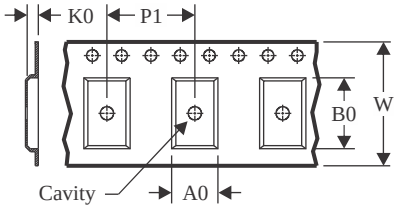
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

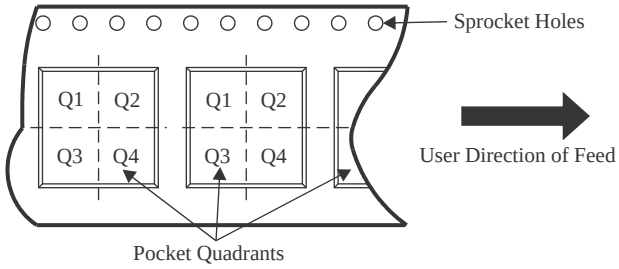


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

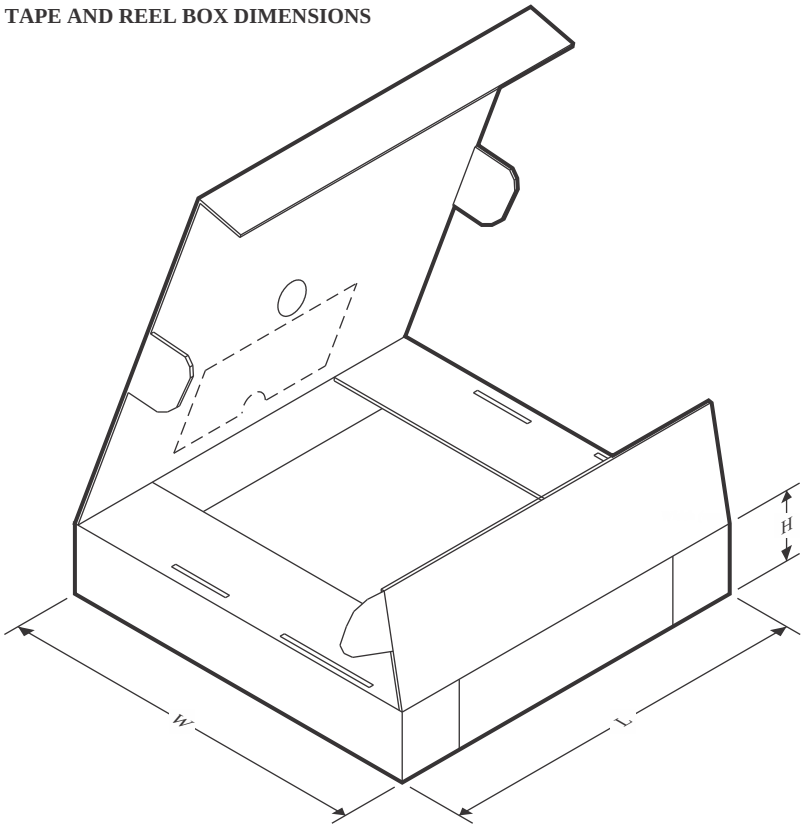
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX4827YBHR	DSBGA	YBH	9	3000	180.0	8.4	1.68	1.72	0.62	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX4827YBHR	DSBGA	YBH	9	3000	182.0	182.0	20.0

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265