NJVMJD340T4G-VF01

High Voltage Power Transistors

DPAK for Surface Mount Applications

Designed for line operated audio output amplifier, switch−mode power supply drivers and other switching applications.

Features

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Electrically Similar to Popular MJE340 and MJE350
- Epoxy Meets UL 94 V−0 @ 0.125 in
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable*
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	300	Vdc
Collector−Base Voltage	V_{CB}	300	Vdc
Emitter−Base Voltage	V_{EB}	3	Vdc
Collector Current − Continuous	I_C	0.5	Adc
Collector Current − Peak	I_{CM}	0.75	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	W W/°C
Total Power Dissipation (Note 1) @ T_A = 25°C Derate above 25°C	P_D	1.56 0.012	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C
ESD − Human Body Model MJD340 (NPN)	HBM	3B	V
ESD − Machine Model MJD340 (NPN)	MM	M4	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

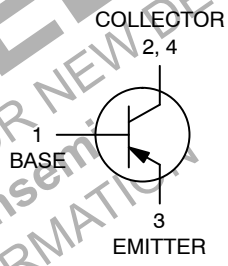
1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

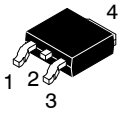
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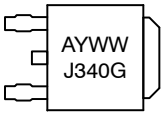
SILICON
POWER TRANSISTORS
0.5 AMPERE
300 VOLTS, 15 WATTS





DPAK
CASE 369C
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
J340 = Device Code
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NJVMJD340T4G−VF01*	DPAK (Pb−Free)	2,500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction−to−Ambient (Note 2)	$R_{\theta JA}$	80	°C/W
Leading Temperature for Soldering Purpose	T_L	260	°C

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 3) (I_C = 1 mA, I_B = 0)	$V_{CEO(sus)}$	300	–	V
Collector Cutoff Current (V_{CB} = 300 V, I_E = 0)	I_{CEO}	–	0.1	mA
Emitter Cutoff Current (V_{BE} = 3 V, I_C = 0)	I_{EBO}	–	0.1	mA
ON CHARACTERISTICS (Note 3)				
DC Current Gain (I_C = 50 mA, V_{CE} = 10 V)	h_{FE}	30	240	–
Collector−Emitter Saturation Voltage (I_C = 100 mA, I_B = 10 mA)	$V_{CE(sat)}$	–	1	V
Base−Emitter On Voltage (I_C = 1 A, V_{CE} = 10 V)	$V_{BE(on)}$	–	1.5	V
DYNAMIC CHARACTERISTICS				
Current Gain − Bandwidth Product (I_C = 50 mA, V_{CE} = 10 V, f = 10 MHz)	f_T	10	–	MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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TYPICAL CHARACTERISTICS

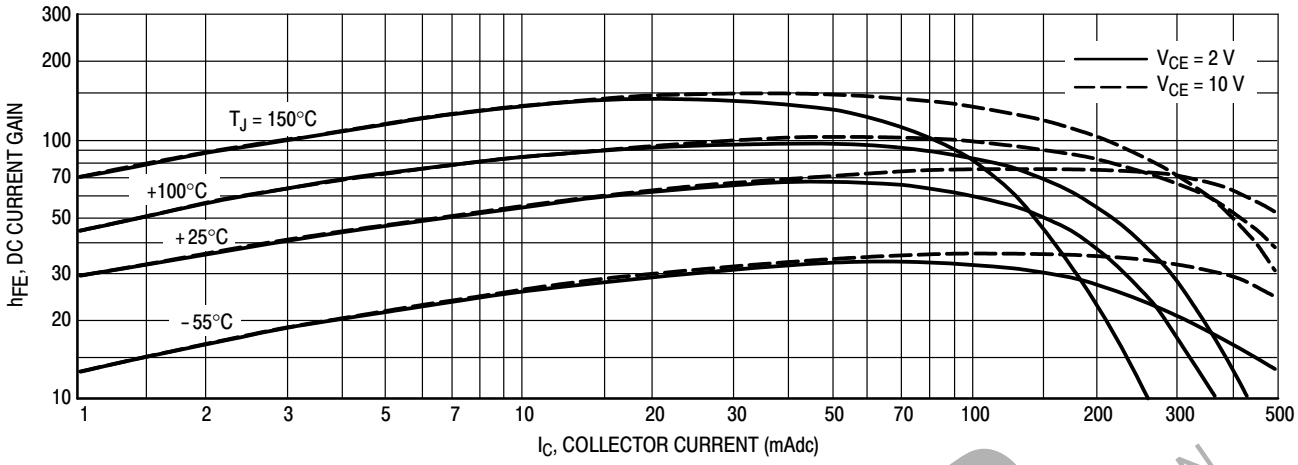


Figure 1. DC Current Gain

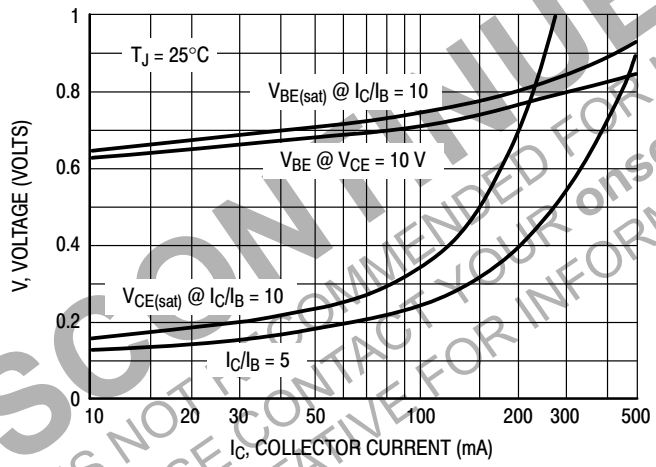


Figure 2. “On” Voltages

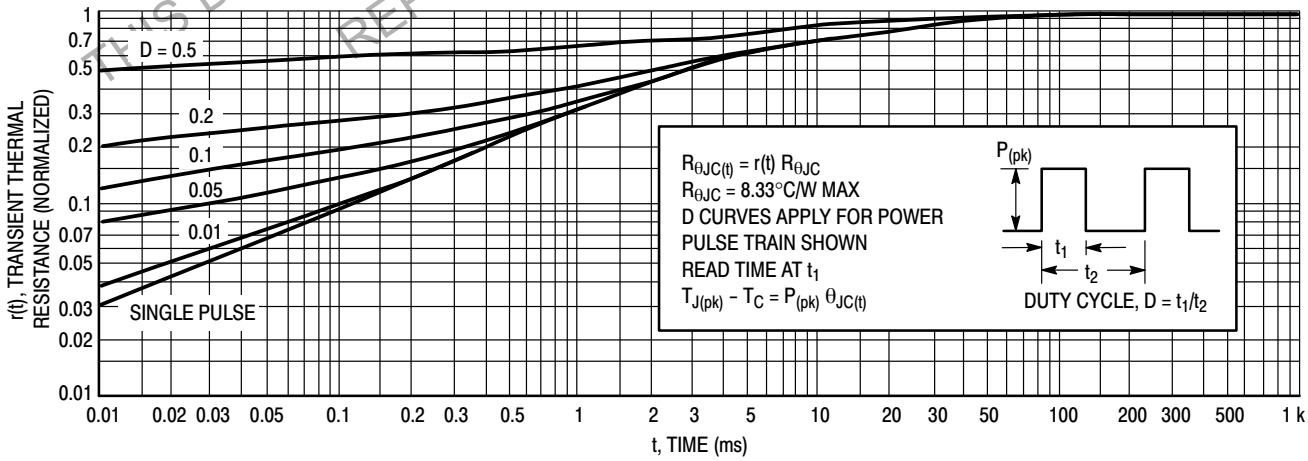


Figure 3. Thermal Response

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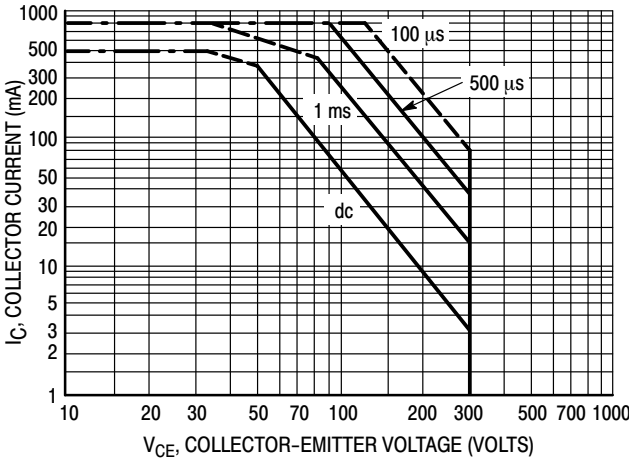


Figure 4. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

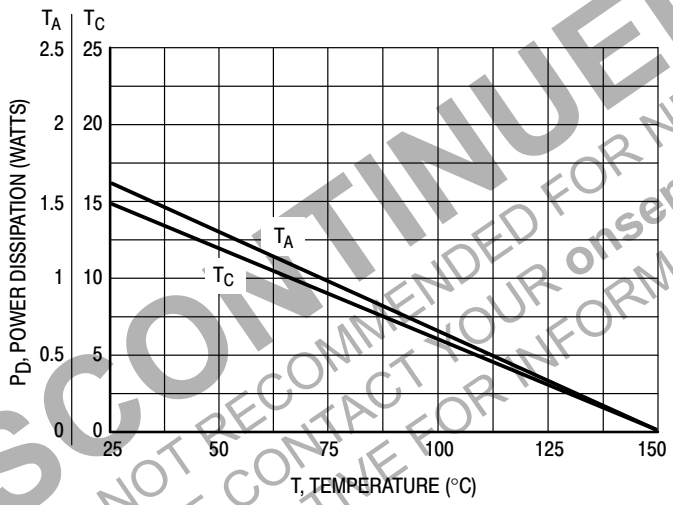


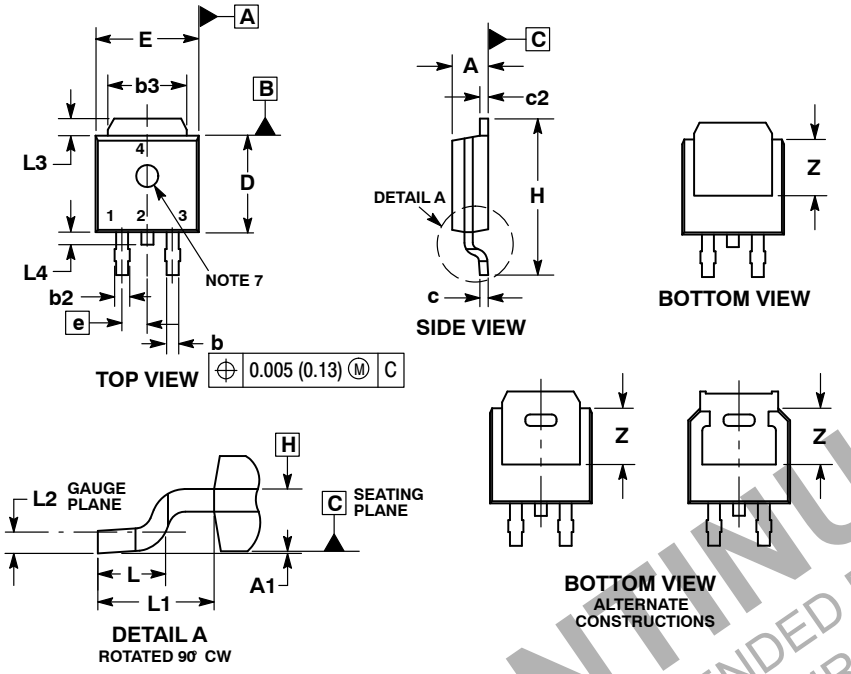
Figure 5. Power Derating

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PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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