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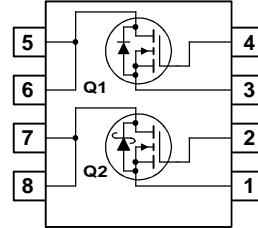
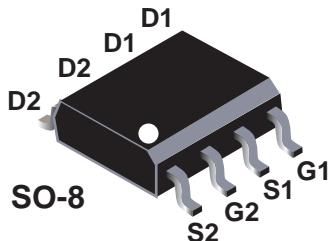
FDS6984AS

Dual Notebook Power Supply N-Channel PowerTrench® SyncFET™ General Description

The FDS6984AS is designed to replace two single SO-8 MOSFETs and Schottky diode in synchronous DC:DC power supplies that provide various peripheral voltages for notebook computers and other battery powered electronic devices. FDS6984AS contains two unique 30V, N-channel, logic level, PowerTrench MOSFETs designed to maximize power conversion efficiency.

The high-side switch (Q1) is designed with specific emphasis on reducing switching losses while the low-side switch (Q2) is optimized to reduce conduction losses. Q2 also includes a patented combination of a MOSFET monolithically integrated with a Schottky diode.

- **Q2:** Optimized to minimize conduction losses
Includes SyncFET Schottky diode
8.5A, 30V $R_{DS(on)}$ max= 20 mΩ @ $V_{GS} = 10V$
 $R_{DS(on)}$ max= 28 mΩ @ $V_{GS} = 4.5V$
- **Q1:** Optimized for low switching losses
Low gate charge (8nC typical)
5.5A, 30V $R_{DS(on)}$ max= 31 mΩ @ $V_{GS} = 10V$
 $R_{DS(on)}$ max= 40 mΩ @ $V_{GS} = 4.5V$
- RoHS Compliant



Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Q2	Q1	Units
V_{DSS}	Drain-Source Voltage	30	30	V
V_{GSS}	Gate-Source Voltage	± 20	± 20	V
I_D	Drain Current - Continuous (Note 1a)	8.5	5.5	A
	- Pulsed	30	20	
P_D	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a)	1.6		
	(Note 1b)	1		
	(Note 1c)	0.9		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6984AS	FDS6984AS	13"	12mm	2500 units

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}$, $I_D = 1 \text{ mA}$ $V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	Q2 Q1	30 30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}$, $V_{GS} = 0 \text{ V}$	Q2 Q1			500 1	μA
		$V_{DS} = 24 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125^\circ\text{C}$	Q2 Q1		2.3 79		mA nA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0 \text{ V}$	All			± 100	nA
On Characteristics (Note 2)							
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 1 \text{ mA}$ $V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	Q2 Q1	1 1	1.7 1.8	3 3	V
$\Delta V_{GS(\text{th})}$ ΔT_J	Gate Threshold Voltage Temperature Coefficient	$I_D = 1 \text{ mA}$, Referenced to 25°C $I_D = 250 \mu\text{A}$, Referenced to 25°C	Q2 Q1		-3 -4		$\text{mV/}^\circ\text{C}$
$R_{DS(\text{on})}$	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 8.5 \text{ A}$ $V_{GS} = 10 \text{ V}$, $I_D = 8.5 \text{ A}$, $T_J = 125^\circ\text{C}$ $V_{GS} = 4.5 \text{ V}$, $I_D = 7 \text{ A}$	Q2		17 24 21	20 32 28	$\text{m}\Omega$
		$V_{GS} = 10 \text{ V}$, $I_D = 5.5 \text{ A}$ $V_{GS} = 10 \text{ V}$, $I_D = 5.5 \text{ A}$, $T_J = 125^\circ\text{C}$ $V_{GS} = 4.5 \text{ V}$, $I_D = 4.6 \text{ A}$	Q1		26 34 32	31 43 40	
$I_{D(\text{on})}$	On-State Drain Current	$V_{GS} = 10 \text{ V}$, $V_{DS} = 5 \text{ V}$	Q2 Q1	30 20			A
g_{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}$, $I_D = 8.5 \text{ A}$ $V_{DS} = 5 \text{ V}$, $I_D = 5.5 \text{ A}$	Q2 Q1		25 18		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	$V_{DS} = 15 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1.0 \text{ MHz}$	Q2 Q1		530 420		pF
C_{oss}	Output Capacitance		Q2 Q1		170 120		pF
C_{rss}	Reverse Transfer Capacitance		Q2 Q1		60 50		pF
R_G	Gate Resistance	$V_{GS} = 15 \text{ mV}$, $f = 1.0 \text{ MHz}$	Q2 Q1		3.1 2.2		Ω

Electrical Characteristics (continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

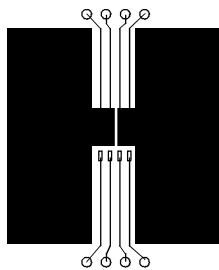
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time		Q2	8	16		ns
			Q1	9	18		
t_r	Turn-On Rise Time	$V_{DD} = 15\text{ V}$, $I_D = 1\text{ A}$,	Q2	5	10		ns
		$V_{GS} = 10\text{ V}$, $R_{GEN} = 6\Omega$	Q1	6	12		
$t_{d(off)}$	Turn-Off Delay Time		Q2	23	37		ns
			Q1	22	35		
t_f	Turn-Off Fall Time		Q2	4	8		ns
			Q1	2	4		
$t_{d(on)}$	Turn-On Delay Time		Q2	9	18		ns
			Q1	10	19		
t_r	Turn-On Rise Time	$V_{DD} = 15\text{ V}$, $I_D = 1\text{ A}$,	Q2	7	14		ns
		$V_{GS} = 4.5\text{ V}$, $R_{GEN} = 6\Omega$	Q1	11	20		
$t_{d(off)}$	Turn-Off Delay Time		Q2	13	24		ns
			Q1	13	24		
t_f	Turn-Off Fall Time		Q2	4	8		ns
			Q1	3	6		
$Q_{g(TOT)}$	Total Gate Charge, $V_{GS} = 10\text{ V}$		Q2	10	14		nC
			Q1	8	11		
Q_g	Total Gate Charge, $V_{GS} = 5\text{ V}$	$Q2: V_{DS} = 15\text{ V}$, $I_D = 8.5\text{ A}$	Q2	5	8		nC
			Q1	4	6		
Q_{gs}	Gate-Source Charge	$Q1: V_{DS} = 15\text{ V}$, $I_D = 5.5\text{ A}$	Q2	1.5			nC
			Q1	1.3			
Q_{gd}	Gate-Drain Charge		Q2	1.9			nC
			Q1	1.5			

Drain-Source Diode Characteristics and Maximum Ratings

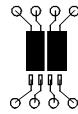
I_S	Maximum Continuous Drain-Source Diode Forward Current	Q2			3.0	A	
		Q1			1.3		
t_{rr}	Reverse Recovery Time	$I_F = 10\text{ A}$, $dI_F/dt = 300\text{ A}/\mu\text{s}$	Q2		13	ns	
Q_{rr}	Reverse Recovery Charge				6	nC	
t_{rr}	Reverse Recovery Time	$I_F = 5.5\text{ A}$, $dI_F/dt = 100\text{ A}/\mu\text{s}$	Q1		17	ns	
Q_{rr}	Reverse Recovery Charge				6	nC	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2.3\text{ A}$ $V_{GS} = 0\text{ V}$, $I_S = 1.3\text{ A}$	Q2		0.6	0.7	V
			Q1		0.8	1.2	

Notes:

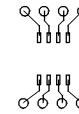
1. $R_{IJ(A)}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{IJ(A)}$ is guaranteed by design while $R_{OC(A)}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5in² pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in² pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. See "SyncFET Schottky body diode characteristics" below.
3. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

Typical Characteristics: Q2

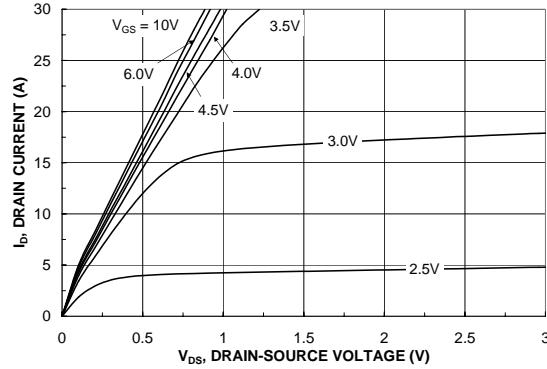


Figure 1. On-Region Characteristics.

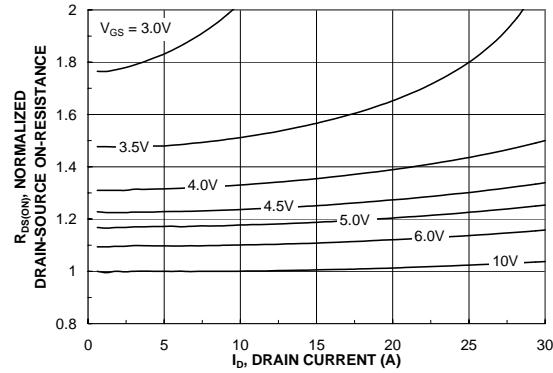


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

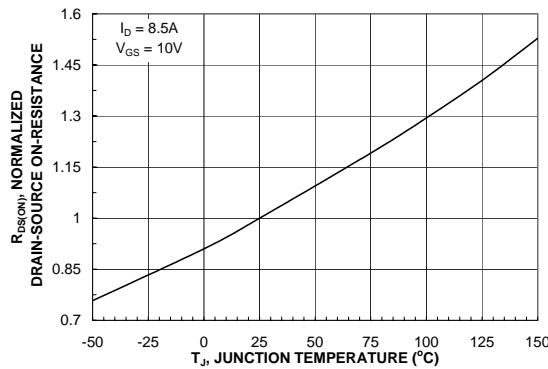


Figure 3. On-Resistance Variation with Temperature.

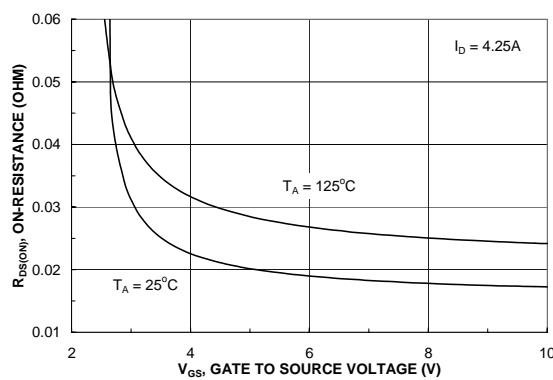


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

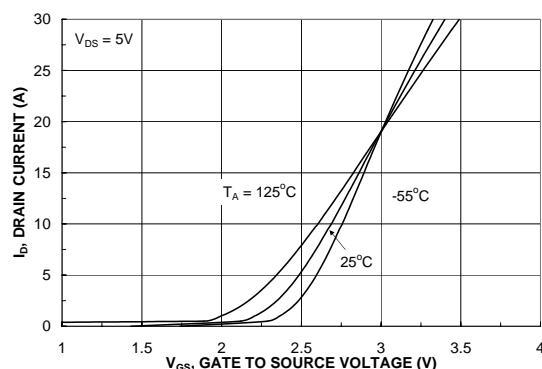


Figure 5. Transfer Characteristics.

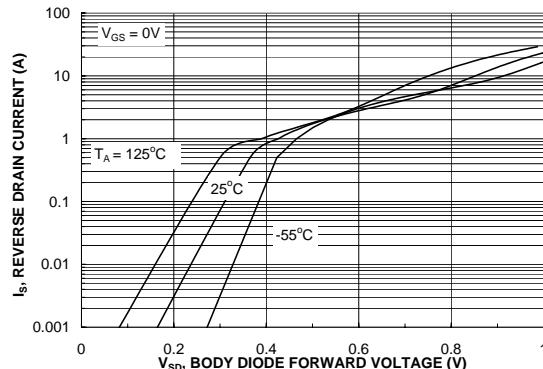


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2

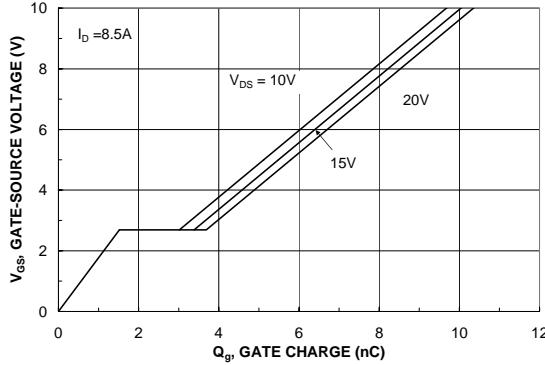


Figure 7. Gate Charge Characteristics.

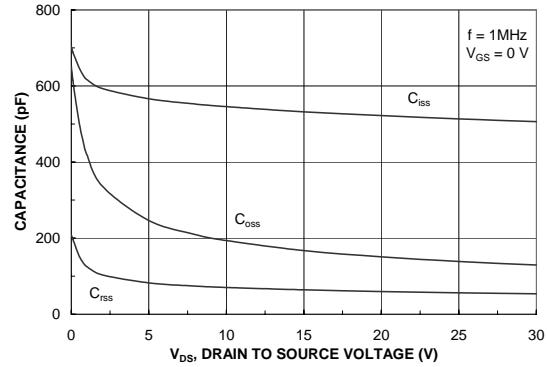


Figure 8. Capacitance Characteristics.

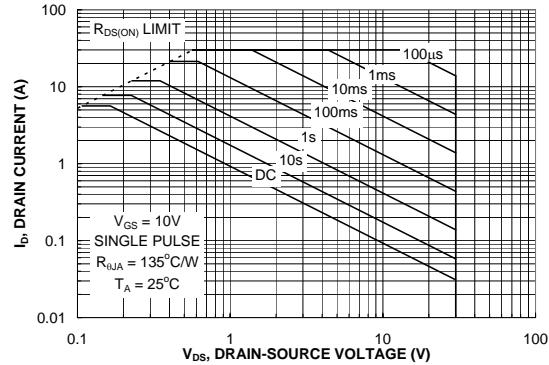


Figure 9. Maximum Safe Operating Area.

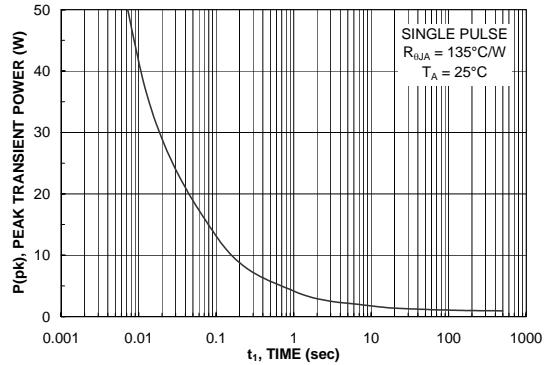


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics Q1

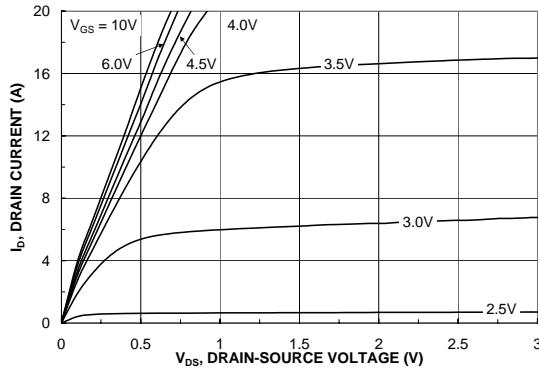


Figure 11. On-Region Characteristics.

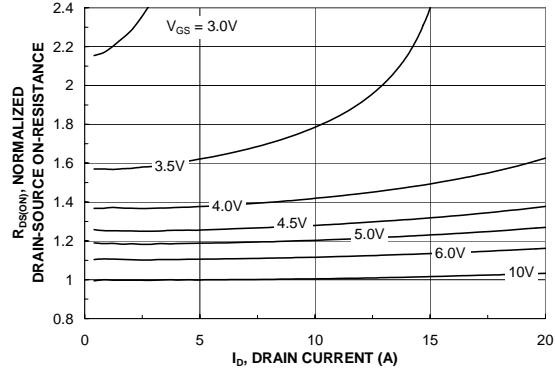


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

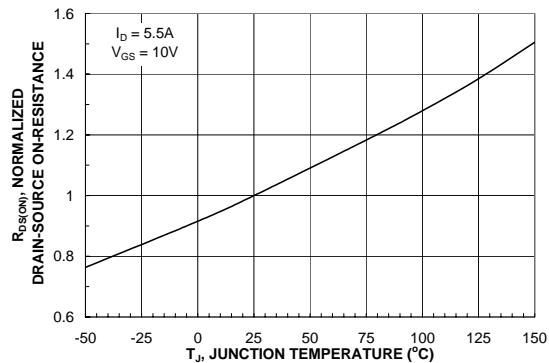


Figure 13. On-Resistance Variation with Temperature.

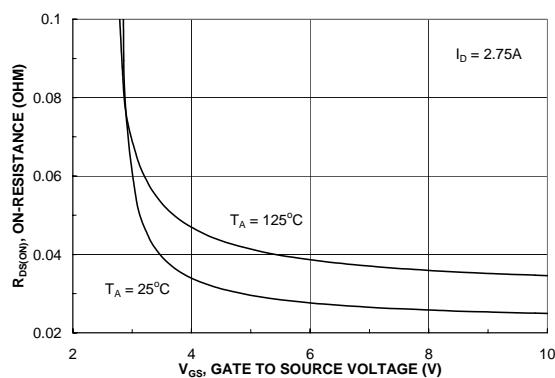


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

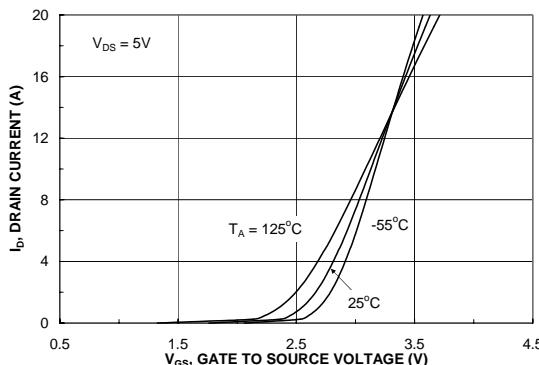


Figure 15. Transfer Characteristics.

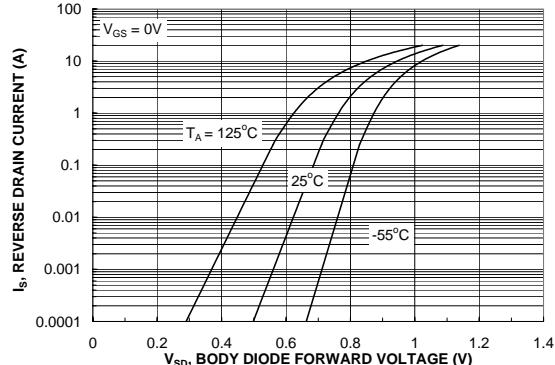


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics Q1

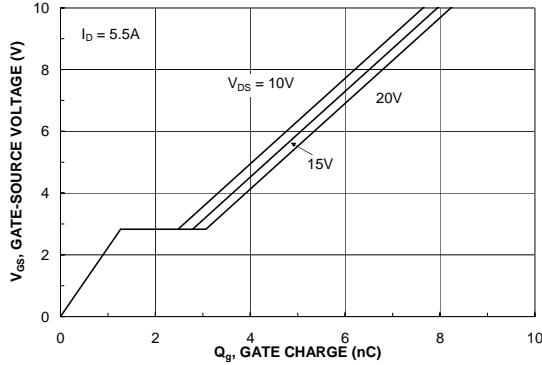


Figure 17. Gate Charge Characteristics.

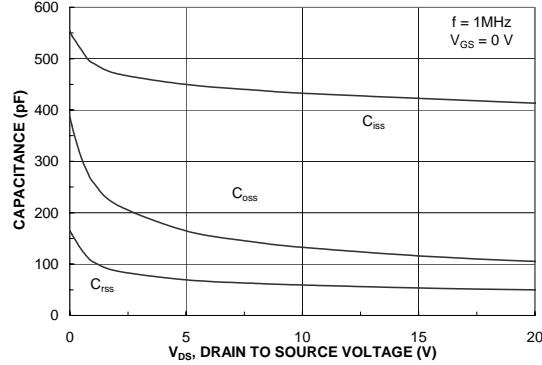


Figure 18. Capacitance Characteristics.

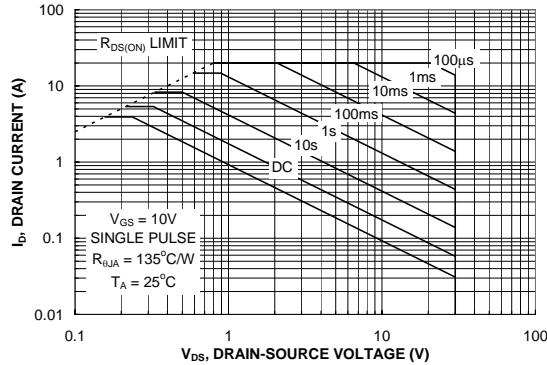


Figure 19. Maximum Safe Operating Area.

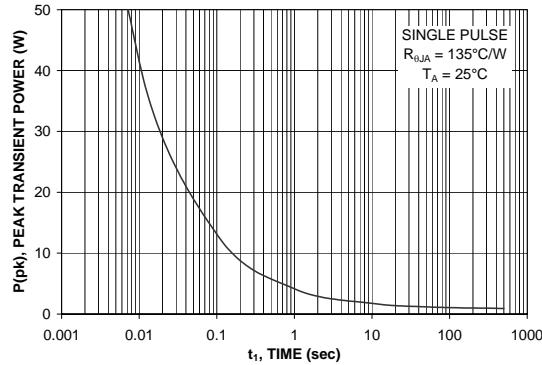


Figure 20. Single Pulse Maximum Power Dissipation.

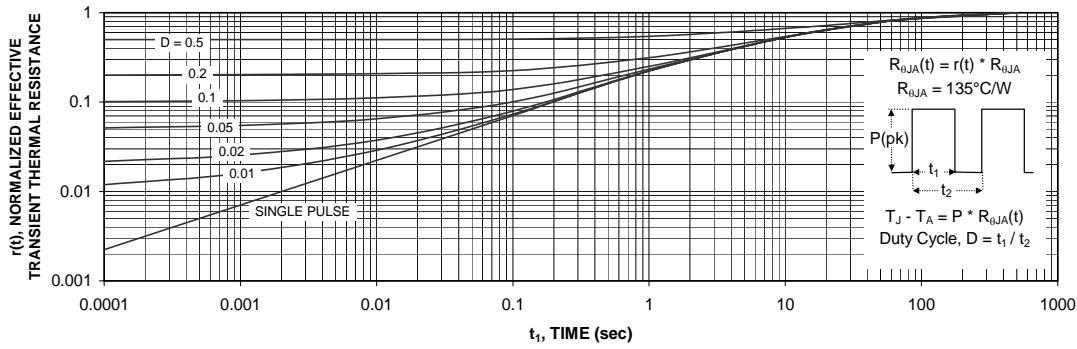


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

Typical Characteristics (continued)

SyncFET Schottky Body Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 22 shows the reverse recovery characteristic of the FDS6984AS.

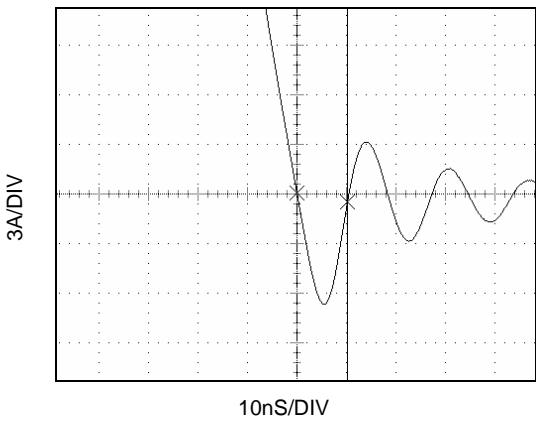


Figure 22. FDS6984AS SyncFET body diode reverse recovery characteristic.

For comparison purposes, Figure 23 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDS6984A).

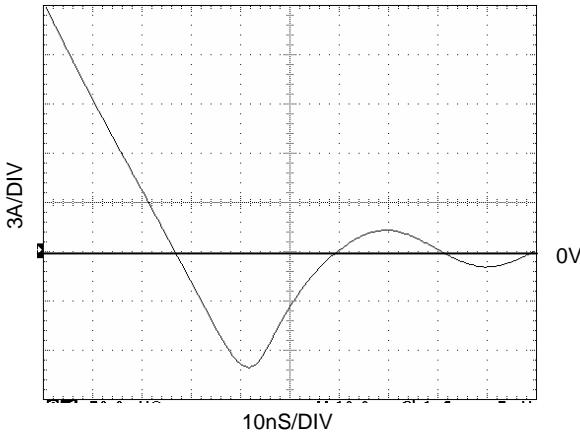


Figure 23. Non-SyncFET (FDS6984A) body diode reverse recovery characteristic.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

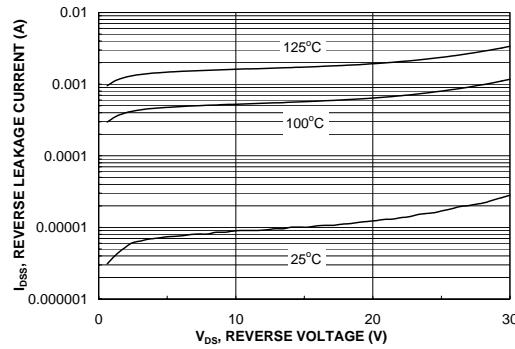


Figure 24. SyncFET body diode reverse leakage versus drain-source voltage and temperature.



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