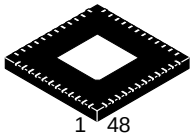
Bluetooth® 5.2 Radio System-on-Chip (SoC) for Automotive

NCV-RSL10



QFNW48
CASE 512AD

Introduction

A member of the RSL10 product family, NCV−RSL10 brings the industry's lowest power Bluetooth Low Energy technology to the automotive industry. NCV−RSL10 helps enable advanced new functionality including keyless entry using a fob or smartphone, active safety and diagnostic alerts, and enhanced infotainment controls while maximizing energy efficiency.

The Bluetooth 5.2 certified radio SoC supports 2 Mbps data rates, twice the speed possible with previous Bluetooth generations. Specially designed and qualified for the unique needs of automotive, NCV−RSL10 features built−in data encryption, wettable flank−plated packaging, and a higher operating temperature range.

Key Features

- Automotive Ready
  - AEC−Q100 Grade 2, ETSI, FCC Qualified
  - Operating Temperature Range (−40°C to +105°C)
- Advanced Wireless Functionality
  - Bluetooth 5.2 certified with LE 2−Mbit PHY (High Speed), as well as backwards compatibility and support for earlier Bluetooth Low Energy specifications
  - Transmitting Power: −17 dBm to +6 dBm
  - Rx Sensitivity (Bluetooth Low Energy Mode, 1 Mbps): −94 dBm
- Enhanced Security
  - Built−in AES128 encryption accelerator
- Industry's Lowest Power Consumption
  - Tx peak (PHY) @ 0 dBm: 4.3 mA (3.3 V Supply)
  - Rx peak (PHY): 2.7 mA (3.3 V Supply)
  - Deep Sleep, I/O Wake−up (3.3 V Supply): 25 nA
  - Deep Sleep, Active External 32 kHz oscillator (3.3 V Supply): 40 nA
- Reliable Assembly
  - Wettable flank−plated QFNW48, 7x7 mm package
- Highly−Integrated System−on−Chip (SoC)
  - 384 kB of Flash Memory
  - Flexible Dual−Core architecture (Arm(R) Cortex−M3 processor, 32−bit DSP)

Other Specifications

- Data Rate: 62.5 to 2000 kpbs
- Flexible Supply Voltage Range (1.1−3.3 V)
- Supports Firmware Over−The−Air (FOTA) updates

MARKING DIAGRAM



(QFNW48)

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCV−RSL10−101Q48−AVG	QFNW48 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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FEATURES

- **Arm Cortex−M3 Processor:** A 32−bit core for real−time applications, specifically developed to enable high−performance low−cost platforms for a broad range of low−power applications.
- **LPDSP32:** A 32−bit Dual Harvard DSP core that efficiently supports custom crypto graphic algorithms or other signal processing that require significant number crunching.
- **Radio Frequency Front−End:** Based on a 2.4 GHz RF transceiver, the RFFE implements the physical layer of the Bluetooth Low Energy technology standard and other proprietary or custom protocols.
- **Protocol Baseband Hardware:** Bluetooth 5.2 certified and includes support for a 2 Mbps RF link and custom protocol options. The RSL10 baseband stack is supplemented by support structures that enable implementation of **onsemi** and customer designed custom protocols.
- **Highly−Integrated SoC:** The dual−core architecture is complemented by high−efficiency power management units, oscillators, flash and RAM memories, a DMA controller, along with a full complement of peripherals and interfaces.
- **Deep Sleep Mode:** RSL10 can be put into a Deep Sleep Mode when no operations are required. Various Deep Sleep Mode configurations are available, including:
  - “IO wake−up” configuration. The power consumption in deep sleep mode is 25 nA (3.3 V VBAT).
  - Embedded 32 kHz oscillator running with interrupts from timer or external pin. The total current drain is 40 nA (3.3 V VBAT).
  - As above with 8 kB RAM data retention. The total current drain is 150 nA (3.3 V VBAT).
  - The DC−DC converter can be used in either buck mode or LDO mode during Sleep Mode, depending on VBAT voltage.
- **Standby Mode:** Can be used to reduce the average power consumption for off−duty cycle operation, ranging typically from a few ms to a few hundreds of ms. The typical chip power consumption is 30 μA in Standby Mode.
- **Multi−Protocol Support:** Using the flexibility provided by LPDSP32, the Arm Cortex−M3 processor, and the RF front−end; proprietary protocols and other custom protocols are supported.
- **Flexible Supply Voltage:** RSL10 integrates high−efficiency power regulators and has a VBAT range of 1.1 to 3.3 V.
- **Highly Configurable Interfaces:** I^2C, UART, two SPI interfaces, PCM interface, multiple GPIOs.
- **Flexible Clocking Scheme:** RSL10 must be clocked from the XTAL/PLL of the radio front−end at 48 MHz when transmitting or receiving RF traffic. When RSL10 is not transmitting/receiving RF traffic, it can run off the 48 MHz XTAL, the internal RC oscillators, the 32 kHz oscillator, or an external clock. A low frequency RTC clock at 32 kHz can also be used in Deep Sleep Mode. It can be sourced from either the internal XTAL, the RC oscillator, or a digital input pad.
- **Diverse Memory Architecture:** 76 kB of SRAM program memory (4 kB of which is PROM containing the chip boot−up program, and is thus unavailable to the user) and 88 kB of SRAM data memory are available. A total of 384 kB of flash is available to store the Bluetooth stack and other applications. The Arm Cortex−M3 processor can execute from SRAM and/or flash.
- **Security:** AES128 encryption hardware block for custom secure algorithms and code protection with authenticated debug port access (JTAG ‘lock’)
- **RoHS Compliant device**

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RSL10 INTERNAL BLOCK DIAGRAM

The block diagram of the RSL10 chip is shown in Figure 1.

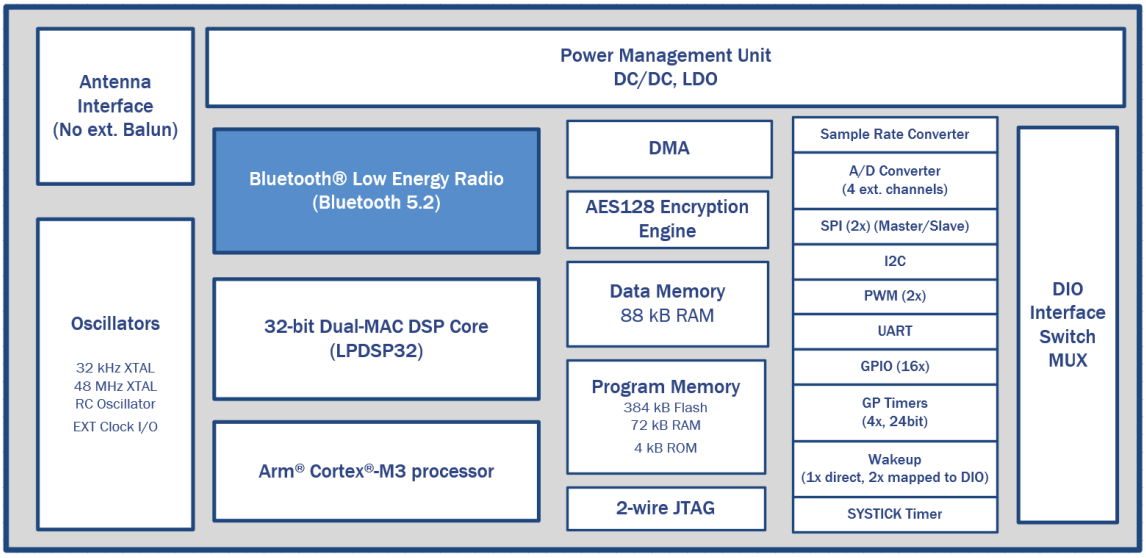


Figure 1. RSL10 Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
VBAT	Power supply voltage		3.63	V
VDDO	I/O supply voltage		3.63	V
VSSRF	RF front−end ground	−0.3		V
VSSA	Analog ground	−0.3		V
VSSD	Digital core and I/O ground	−0.3		V
Vin	Voltage at any input pin	VSSD−0.3	VDDC + 0.3 (Note 1)	V
T storage	Storage temperature range (Note 2)	−40	150	°C
Caution: ESD Classification Class C3 per AEC−Q100−011 Rev−C1. The QFN package meets 250 V CDM level				

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Up to a maximum of 3.63 V.
2. Applies after soldering to PCB.

Table 2. RECOMMENDED OPERATING CONDITIONS

Description	Symbol	Conditions	Min	Typ	Max	Units
Supply voltage operating range	VBAT	Input supply voltage on VBAT pin (Note 4)	1.18	1.25	3.3	V
Functional temperature range	T functional		−40		105 (Note 3)	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. For functional operation at greater than 85°C, the following trimming parameters must be used:
   − VDDMRET_VTRIM = 0x3
   − VDDTRET_VTRIM = 0x3
   − VDDCRET_VTRIM = 0x3
4. In order to be able to use a VBAT Min of 1.1 V, the following reduced operating conditions should be observed:
   − Maximum Tx power 0 dBm.
   − SYSCLK ≤ 24 MHz.
   − Functional temperature range limited to 0−50 °C
   The following trimming parameters should be used:
   − VCC = 1.10 V
   − VDDC = 0.92 V
   − VDDM = 1.05 V, will be limited by VCC at end of battery life
   − VDDRF = 1.05 V, will be limited by VCC at end of battery life. VDDPA should be disabled
   RSL10 should enter in end−of−battery−life operating mode if VCC falls below 1.03 V. VCC will remain above 1.03 V if VBAT ≥ 1.10 V under the restricted operating conditions described above.

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Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C for VBAT = VDDO = 3 V in DC−DC (buck) mode.

Description	Symbol	Conditions	Min	Typ	Max	Units
OVERALL						
Current consumption RX, V_{BAT} = 3 V	I_{VBAT}			0.9		mA
Current consumption TX, V_{BAT} = 3 V	I_{VBAT}			0.9		mA
Deep sleep current, example 1, V_{BAT} = 3 V	Ids1	Wake up from wake up pin or DIO wake up.		25		nA
Deep sleep current, example 2, V_{BAT} = 3 V	Ids2	Embedded 32 kHz oscillator running with interrupts from timer or external pin.		40		nA
Deep sleep current, example 3, V_{BAT} = 3 V	Ids3	As Ids2 but with 8 kB RAM data retention.		100		nA
Standby Mode current, V_{BAT} = 3 V	Istb	Digital blocks and memories are not clocked and are powered at a reduced voltage.		17		μA
EEMBC ULPMark BENCHMARK, CORE PROFILE						
ULPMark CP 3.0 V		Arm Cortex−M3 processor running from RAM, VBAT= 3.0 V, IAR C/C++ Compiler for ARM 8.20.1.14183		1090		ULP Mark
ULPMark CP 2.1 V		Arm Cortex−M3 processor running from RAM, VBAT= 2.1 V, IAR C/C++ Compiler for ARM 8.20.1.14183		1260		ULP Mark
EEMBC CoreMark BENCHMARK for the Arm Cortex−M3 Processor and the LPDSP32 DSP						
Arm Cortex−M3 processor running from RAM		At 48 MHz SYSCLK. Using the IAR 8.10.1 C compiler, certified		159		Core Mark
LPDSP32 running from RAM		At 48 MHz SYSCLK Using the 2020.03 release of the Synopsys LPDSP32 C compiler		174		Core Mark
Arm Cortex−M3 processor and LPDSP32 running from RAM, VBAT = 3 V		At 48 MHz SYSCLK		284		Core Mark/ mA
Arm Cortex−M3 processor running CoreMark from RAM, VBAT = 3 V		At 48 MHz SYSCLK (processor consumption only)		12.3		μA/MHz
Arm Cortex−M3 processor running CoreMark from Flash, VBAT = 3 V		At 48 MHz SYSCLK (processor consumption only)		14.6		μA/MHz
LPDSP32 running CoreMark from RAM, VBAT = 3 V		At 48 MHz SYSCLK (processor consumption only)		8.2		μA/MHz
INTERNALLY GENERATED VDDC: Digital Block Supply Voltage						
Supply voltage: operating range	VDDC		0.92	1.15	1.32 (Note 5)	V
Supply voltage: trimming range	$VDDC_{RANGE}$		0.75		1.38	V
Supply voltage: trimming step	$VDDC_{STEP}$			10		mV
INTERNALLY GENERATED VDDM: Memories Supply Voltage						
Supply voltage: operating range	VDDM		1.05	1.15	1.32 (Note 6)	V
Supply voltage: trimming range	$VDDM_{RANGE}$		0.75		1.38	V
Supply voltage: trimming step	$VDDM_{STEP}$			10		mV
INTERNALLY GENERATED VDDRF: Radio Front end supply voltage						
Supply voltage: operating range	VDDRF		1.00	1.10	1.32 (Notes 7 and 8)	V
Supply voltage: trimming range	$VDDRF_{RANGE}$		0.75		1.38	V

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Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C for VBAT = VDDO = 3 V in DC−DC (buck) mode.

Description	Symbol	Conditions	Min	Typ	Max	Units
INTERNALLY GENERATED VDDRF: Radio Front end supply voltage						
Supply voltage: trimming step	$VDDRF_{STEP}$			10		mV
INTERNALLY GENERATED VDDPA: Optional Radio Power Amplifier Supply Voltage						
Supply voltage: operating range	VDDPA		1.05	1.3	1.68	V
Supply voltage: trimming range	$VDDPA_{RANGE}$		1.05		1.68	V
Supply voltage: trimming step	$VDDPA_{STEP}$			10		mV
Supply voltage: trimming step	$DCDC_{STEP}$			10		mV
VDDO PAD SUPPLY VOLTAGE: Digital Level High Voltage						
Digital I/O supply	VDDO		1.1		3.3	V
INDUCTIVE BUCK DC−DC CONVERTER						
VBAT range when the DC−DC converter is active (Note 9)	$DCDC_{IN_RANGE}$		1.4		3.3	V
VBAT range when the LDO is active	LDO_{IN_RANGE}		1.1		3.3	V
Output voltage: trimming range	$DCDC_{OUT_RANGE}$		1.1	1.2	1.32	V
Supply voltage: trimming step	$DCDC_{STEP}$			10		mV
POWER−ON RESET						
POR voltage	$VBAT_{POR}$		0.4	0.8	1.0	V
RADIO FRONT−END: General Specifications						
RF input impedance	Z_{in}	Single ended		50		Ω
Input reflection coefficient	S_{11}	All channels			−8	dB
Data rate FSK / MSK / GFSK	R_{FSK}	OQPSK as MSK	62.5	1000	3000	kbps
Data rate 4−FSK					4000	kbps
On−air data rate	bps	GFSK	250		2000	kbps
RADIO FRONT−END: Crystal and Clock Specifications						
Xtal frequency	F_{XTAL}	Fundamental		48		MHz
Equiv. series Res.	ESR_{XTAL}	RSL10 has internal load capacitors, additional external capacitors are not required	20		80	Ω
Differential equivalent load capacitance	CL_{XTAL}	Internal load capacitors (NO EXTERNAL LOAD CAPACITORS REQUIRED)	6	8	10	pF
Settling time				0.5	1.5	ms
RADIO FRONT−END: Synthesizer Specifications						
Frequency range	F_{RF}	Supported carrier frequencies	2360		2500	MHz
RX frequency step		RX Mode frequency synthesizer resolution			100	Hz
TX frequency step		TX Mode frequency synthesizer resolution			600	Hz
PLL Settling time, RX	t_{PLL_RX}	RX Mode		15	25	μs
PLL Settling time, TX	t_{PLL_TX}	TX mode, BLE modulation		5	10	μs
RADIO FRONT−END: Receive Mode Specifications						
Current consumption at 1 Mbps, V_{BAT} = 3 V, DC−DC	$IBAT_{RFRX}$	VDDRF = 1.1 V, 100% duty cycle		3.0		mA
Current consumption at 2 Mbps, V_{BAT} = 3 V, DC−DC	$IBAT_{RFRX}$	VDDRF = 1.1 V, 100% duty cycle		3.4		mA
RX Sensitivity, 0.25 Mbps		0.1% BER (Notes 10, 11)		−97		dBm

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Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C for VBAT = VDDO = 3 V in DC−DC (buck) mode.

Description	Symbol	Conditions	Min	Typ	Max	Units
RADIO FRONT−END: Receive Mode Specifications						
RX Sensitivity, 0.5 Mbps		0.1% BER (Notes 10, 11)		−96		dBm
RX Sensitivity, 1 Mbps, BLE		0.1% BER (Notes 10, 11) Single−ended on chip antenna match to 50 Ω		−94		dBm
RX Sensitivity, 2 Mbps, BLE		0.1% BER (Notes 10, 11)		−92		dBm
RSSI effective range		Without AGC		60		dB
RSSI step size				2.4		dB
RX AGC range				48		dB
RX AGC step size		Programmable		6		dB
Max usable signal level		0.1% BER		−10		dBm
RADIO FRONT−END: Transmit Mode Specifications						
Tx peak power consumption at VBAT = 3 V (Note 12)	$IBAT_{RFTX}$	Tx power 0 dBm, VDDRF = 1.07 V, VDDPA: off, DC−DC mode		4.6		mA
		Tx power 3 dBm, VDDRF = 1.1 V, VDDPA = 1.26 V, DC−DC mode		8.6		mA
		Tx power 6 dBm, VDDRF = 1.1 V, VDDPA = 1.60 V, DC−DC mode		12		mA
Transmit power range		BLE	−17		+6 (Note 15)	dBm
Transmit power step size		Full band.		1		dB
Transmit power accuracy		Tx power 3 dBm. Full band. Relative to the typical value.	−1.5		+1	dB
		Tx power 0 dBm. Full band. Relative to the typical value.	−1.5		1.5	dB
Power in 2nd harmonic		0 dBm mode. 50 Ω for “Typ” value. (Note 14)		−31	−18	dBm
Power in 3rd harmonic		0 dBm mode. 50 Ω for “Typ” value. (Note 14)		−40	−31	dBm
Power in 4th harmonic		0 dBm mode. 50 Ω for “Typ” value. (Note 14)		−49	−42	dBm
ADC						
Resolution	ADC_{RES}		8	12	14	bits
Input voltage range	ADC_{RANGE}		0		2	V
INL	ADC_{INL}		−2		+2	mV
DNL	ADC_{DNL}		−1		+1	mV
Channel sampling frequency	ADC_{CH_SF}	For the 8 channels sequentially, SLOWCLK = 1 MHz	0.0195		6.25	kHz
32 kHz ON−CHIP RC OSCILLATOR						
Untrimmed Frequency	$Freq_{UNTR}$		20	32	50	kHz
Trimming steps	Steps			1.5		%
3 MHz ON−CHIP RC OSCILLATOR						
Untrimmed Frequency	$Freq_{UNTR}$		2	3	5	MHz
Trimming steps	Steps			1.5		%
Hi Speed mode	Fhi			10		MHz
32 kHz ON−CHIP CRYSTAL OSCILLATOR (Note 16)						
Output Frequency	$Freq_{32k}$	Depends on xtal parameters		32768		Hz
Startup time				1	3	s
Internal load trimming range		Steps of 0.4 pF	0		25.2	pF

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Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C for VBAT = VDDO = 3 V in DC−DC (buck) mode.

Description	Symbol	Conditions	Min	Typ	Max	Units
32 kHz ON−CHIP CRYSTAL OSCILLATOR (Note 16)						
Load Capacitance		No external load capacitors required. Maximum external parasitic capacity allowed (package, routing, etc.)			3.5	pF
ESR					100	kΩ
Duty Cycle			40	50	60	%
DC INPUT CHARACTERISTICS OF THE DIGITAL PADS − With VDDO = 2.97 V – 3.3 V, nominal: 3.0 V Logic						
Voltage level for high input	V_{IH}		2		VDDO+0.3	V
Voltage level for low input	V_{IL}		VSSD−0.3		0.8	V
DC OUTPUT CHARACTERISTICS OF THE DIGITAL PADS						
Voltage level for high input	V_{OH}	I_{OH} = 2 mA to 12 mA	VDDO−0.4			V
Voltage level for low input	V_{OL}	I_{OH} = 2 mA to 12 mA			0.4	V
DIO DRIVE STRENGTH						
DIO drive strength	IDIO		2	12	12	mA
FLASH SPECIFICATIONS						
Endurance of the 384 kB of flash			40,000			write/erase cycles
Endurance for sections NVR1, NVR2, and NVR3 (6 kB in total)			1000			write/erase cycles
Retention			25			years

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. The maximum VDDC voltage cannot exceed the VBAT input voltage or the VCC output from the buck converter.
6. The maximum VDDM voltage cannot exceed the VBAT input voltage or the VCC output from the buck converter.
7. The maximum VDDRF voltage cannot exceed the VBAT input voltage or the VCC output from the buck converter.
8. The VDDRF calibrated targets are:
   − 1.10 V (TX power > 0 dBm, with optimal RX sensitivity)
   − 1.07 V (TX power = 0 dBm)
   − 1.20 V (TX power = 2 dBm)
   The VDDPA calibrated targets are:
   − 1.30 V
   − 1.26 V (TX power = 3 dBm, assumes VDDRF = 1.10 V)
   − 1.60 V (TX power = 6 dBm, assumes VDDRF = 1.10 V)
9. The LDO can be used to regulate down from VBAT and generate VCC. For VBAT values higher than 1.5 V, the LDO is less efficient and it is possible to save power by activating the DC−DC converter to generate VCC.
10. Signal generated by RF tester.
11. 0.5 to 1.0 dB degradation in the RX sensitivity is present on the QFN package. This is attributed to the presence of the metal slug of the QFN package which is in close proximity to on−chip inductors.
12. All values are based on evaluation board performance at the antenna connector, including the harmonic filter loss
13. At +6 dBm Tx power, an antenna gain of +2.2 dBi or less must be used to ensure out−of−band regulatory emissions compliance
14. The values shown here are without RF filter. Harmonics need to be filtered with an external filter (See “RF Filter” on Table 6).
15. For optimal performance, charge pump frequency of 125 kHz should be avoided when VDDPA supply is enabled.
16. These specifications have been validated with the Epson Toyocom MC – 306 crystal

Table 4. VDDM Target Trimming Voltage as a Function of VDDO Voltage

VDDM Voltage (V)	DIO_PAD_CFG DRIVE	Maximum VDDO Voltage (V)
1.05	1	2.7
1.05	0	3.2
1.10	0	3.3

NOTE: These are trimming targets at room/ATE temperature 25∼30°C.

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Table 5. VDDC Target Trimming Voltage as a Function of SYSCLK Frequency

VDDC Voltage (V)	Maximum SYSCLK Frequency (MHz)	Restriction
0.92	≤ 24	The ADC will be functional in low frequency mode and between 0 and 85°C only.
1.00	≤ 24	Fully functional
1.05	48	Fully functional

NOTE: These are trimming targets at room/ATE temperature 25～30°C.

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Table 6. RECOMMENDED EXTERNAL COMPONENTS:

Components	Function	Recommended typical value	Tolerance
Cap (VBAT−VSSA)	VBAT decoupling	4.7 μF + 100 pF (Note 17)	±20%
Cap (VDDO−VSSD)	VDDO decoupling	1 μF	±20%
Cap (VDDRF−VSSRF)	VDDRF decoupling	2.2 μF	±20%
Cap (VCC−VSSA)	VCC decoupling	Low ESR 2.2 μF (Note 18) or 4.7 μF	±20%
Cap (VDDA−VSSA)	VDDA decoupling	1 μF	±20%
Cap (CAP0−CAP1)	Pump capacitor for the charge pump	1 μF	±20%
Inductor (DC−DC)	DC−DC converter inductance	Low ESR 2.2 μH (See Table 7 below)	±20%
Xtal_32 kHz	Xtal for 32 kHz oscillator	− MC – 306, Epson − CM8V−T1A, Micro Crystal Switzerland WMRAG32K76CS1C00R0, Murata	
Xtal_48 MHz	Xtal for 48 MHz oscillator	8Q−48.000MEEV−T, TXC Corporation, Taiwan XRCTD48M000NXQ2ER0, Murata	
RF filter (Note 19)	External harmonic filter	1.5 pF / 3 nH / 1.5 pF / 1.8 nH	±20%

NOTE: All capacitors used must have good RF performance.
17. The recommended decoupling capacitance uses 2 capacitors with the values specified.
18. Example: AMK105BJ225_P, Taiyo Yuden.
19. For improved harmonic performance in environments where RSL10 is operating in close proximity to smartphones or base stations, FBAR filters such as the Broadcom ACPFP−7924 can be applied instead of the suggested discrete harmonic filter.

Table 7. RECOMMENDED DC−DC CONVERTER INDUCTANCE TABLE

Manufacturer	Part Number	Case Size	Comments
Taiyo Yuden	CKP2012N_2R2	0805 SMD with T_{max} = 1.0 mm	A degradation of 1 dB in the RX sensitivity is expected in DC−DC mode (Vbat = 3.3 V) versus LDO mode operation.
Taiyo Yuden	CBMF1608T2R2M	0603 SMD with T_{max} = 1.0 mm	A degradation of <1 dB in RX sensitivity is expected in DC−DC mode (Vbat = 3.3 V) versus LDO mode operation. Also, the current drawn from the battery will be 4−10% higher than when the CKP2012N_2R2 is used depending on operation mode and settings.

NOTE: Values have been measured on the QFN version of the RSL10 development board.

PCB Design Guidelines

1. Decoupling capacitors should be placed as close to the related pins as possible.
2. Differential output signals should be routed as symmetrically as possible.
3. Analog input signals should be shielded as well as possible.
4. Pay close attention to the parasitic coupling capacitors.
5. Special care should be made for PCB design in order to obtain good RF performance.
6. Multi−layer PCB should be used with a keep−out area on the inner layers directly below the antenna matching circuitry in order to reduce the stray capacitances that influence RF performance.
7. All the supply voltages should be decoupled as close as possible to their respective pin with high performance RF capacitors. These supplies should be routed separately from each other and if possible on different layers with short lines on the PCB from the chip’s pin to the supply source.
8. Digital signals shouldn’t be routed close to the crystal or the power supply lines.
9. Proper DC−DC component placement and layout is critical to RX sensitivity performance in DC−DC mode.

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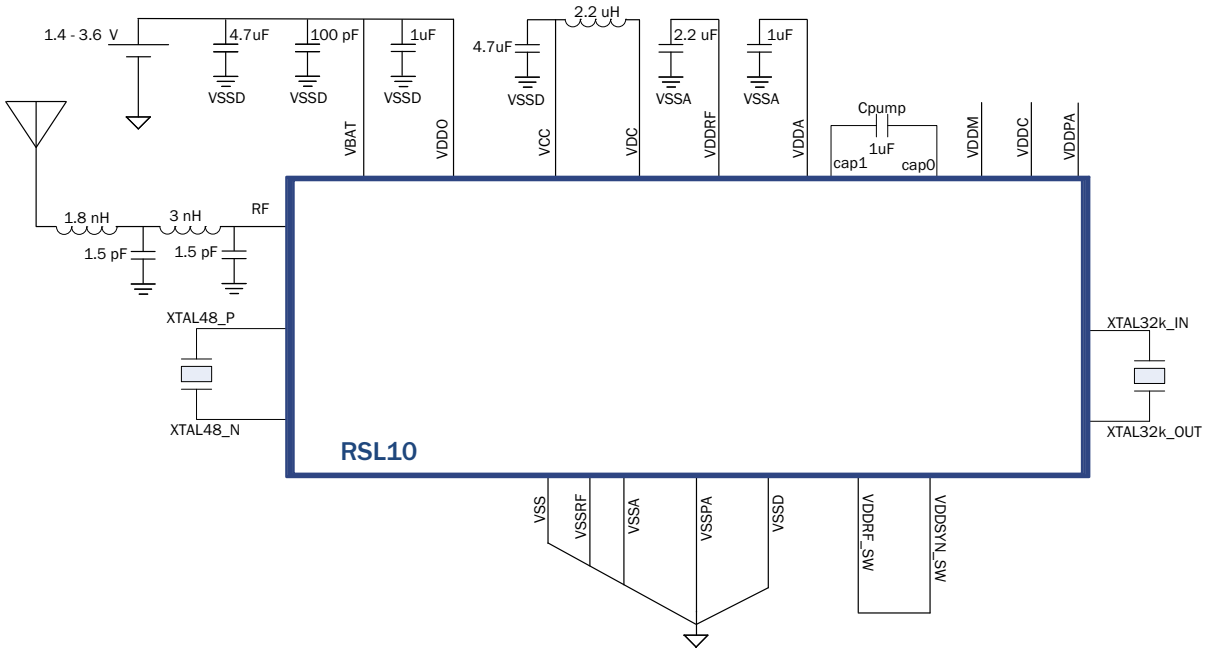
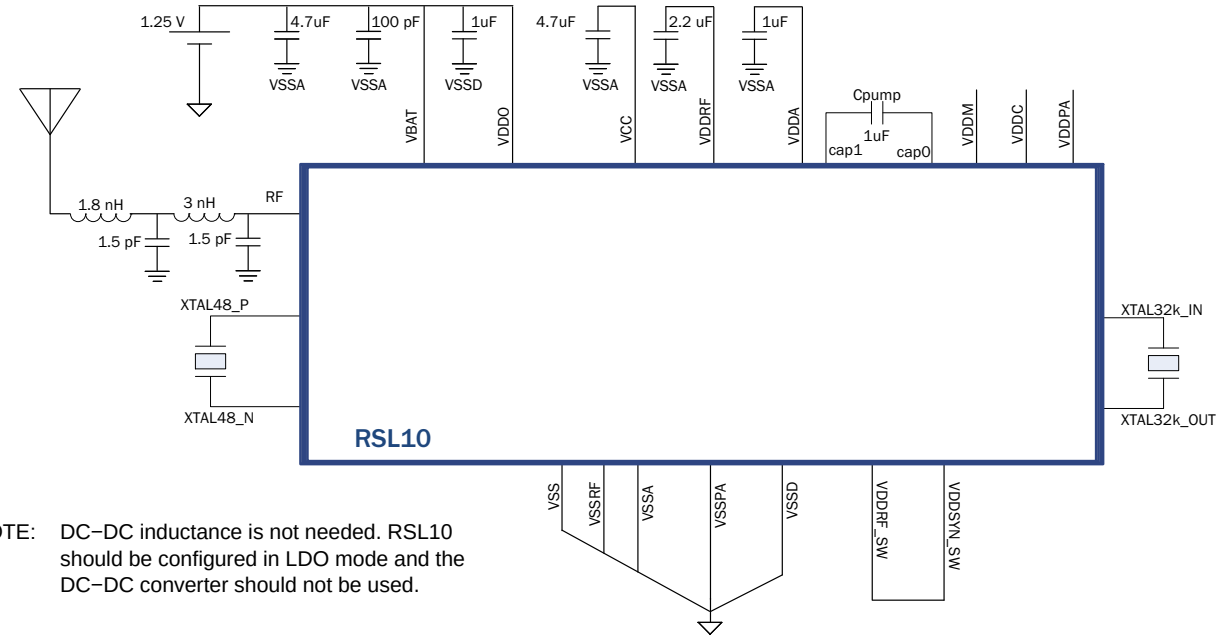


Figure 2. RSL10 Application Diagram in Buck Mode



NOTE: DC−DC inductance is not needed. RSL10 should be configured in LDO mode and the DC−DC converter should not be used.

Figure 3. RSL10 Application Diagram in LDO Mode

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Table 8. CHIP INTERFACE SPECIFICATIONS

Pad Name	Description	Power Domain	I/O	A/D	Pull	Pad #, QFN48
VBAT	Battery input voltage	VBAT	I	P		9
VDC	DC−DC output voltage to external LC filter		O	A		10
VCC	DC−DC filtered output		I	P/A		12
XTAL32_IN	Xtal input pin for 32 kHz xtal		I/O	A		14
XTAL32_OUT	Xtal output pin for 32 kHz xtal		I/O	A		13
VSSA	Analog ground		I/O	P		8
RES	RESERVED		I	D	D	11
VDDA	Charge pump output for analog and flash supplies	VDDA	I/O	P/A		5
VDDRF	LDO's output for radio voltage supply		I/O	P/A		48
CAP0	Pump capacitor connection		O	A		7
CAP1	Pump capacitor connection		O	A		6
AOUT	Analog test pin		O	A		4
VDDRF_SW	Supply pin for the RF	VDDRF_SW		P/A		47
VDDSYN_SW	Supply pin for the radio synthesizer			P/A		45
VSSRF	RF analog ground		I/O	P		46
XTAL48_N	Negative input for the 48 MHz xtal block		I/O	A		43
XTAL48_P	Positive input for the 48 MHz xtal block		I/O	A		44
VDDPA	Radio power amplifier voltage supply	VDDPA	I/O	P/A		2
VSSPA	Radio power amplifier ground		I/O	P		3
RF	RF signal input/output (Antenna)	RF	I/O	A		1
VPP	Flash high voltage access	VPP	I/O	A		17

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Table 8. CHIP INTERFACE SPECIFICATIONS

Pad Name	Description	Power Domain	I/O	A/D	Pull	Pad #, QFN48
NRESET	Reset pin	VDDO	I	D	U1	16
WAKEUP	Wake−up pin for power modes		I	A		15
VDDC	LDO output for Core logic voltage supply		I/O	P		19
VDDM	LDO output for memories voltage supply		I/O	P		21
VDDO	Digital I/O voltage supply		I	P		36
VSSD	Digital ground pad for I/O		I/O	P		28, 35
VSS (*)	Substrate connection for the RF part		I/O	P		42
EXTCLK	External clock input		I	D	U	31
DIO[0]	Digital input output / ADC 0 / Wakeup 0 / STANDBYCLK input		I/O	A/D	U/D	18
DIO[1]	Digital input output / ADC 1 / Wakeup 1 / STANDBYCLK input		I/O	A/D	U/D	20
DIO[2]	Digital input output / ADC 2 / Wakeup 2 / STANDBYCLK input		I/O	A/D	U/D	23
DIO[3]	Digital input output / ADC 3 / Wakeup 3 / STANDBYCLK input		I/O	A/D	U/D	25
DIO[4]	Digital input output 4		I/O	D	U/D	24
DIO[5]	Digital input output 5		I/O	D	U/D	27
DIO[6]	Digital input output 6		I/O	D	U/D	29
DIO[7]	Digital input output 7		I/O	D	U/D	30
DIO[8]	Digital input output 8		I/O	D	U/D	26
DIO[9]	Digital input output 9		I/O	D	U/D	22
DIO[10]	Digital input output 10		I/O	D	U/D	32
DIO[11]	Digital input output 11		I/O	D	U/D	38
DIO[12]	Digital input output 12		I/O	D	U/D	37
DIO[13]	Digital input output / CM3−JTAG Test Reset		I/O	D	U/D	39
DIO[14]	Digital input output / CM3−JTAG Test Data In		I/O	D	U/D	41
DIO[15]	Digital input output / CM3−JTAG Test Data Out		I/O	D	U/D	40
JTCK	CM3−JTAG Test Clock		I/O	D	U	33
JTMS	CM3−JTAG Test Mode State		I/O	D	U	34

*VSS should be connected to VSSRF at the PCB level.

NOTE: It is recommended that the QFN package metal slug be left open/floating for optimal Rx sensitivity performance

Legend:
Type: A = analog; D = digital; I = input; O = output; P = power
Pull: U = pull up; D = pull down
Pull up: selectable between 10 kΩ and 250 kΩ
Pull down: 250 kΩ
Pull resistor tolerance of ±15%
All digital pads have a Schmitt trigger input.
All DIO pads have a programmable I^2C low pass filter.

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ARCHITECTURE OVERVIEW

The architecture of the RSL10 chip is shown in Figure 4.

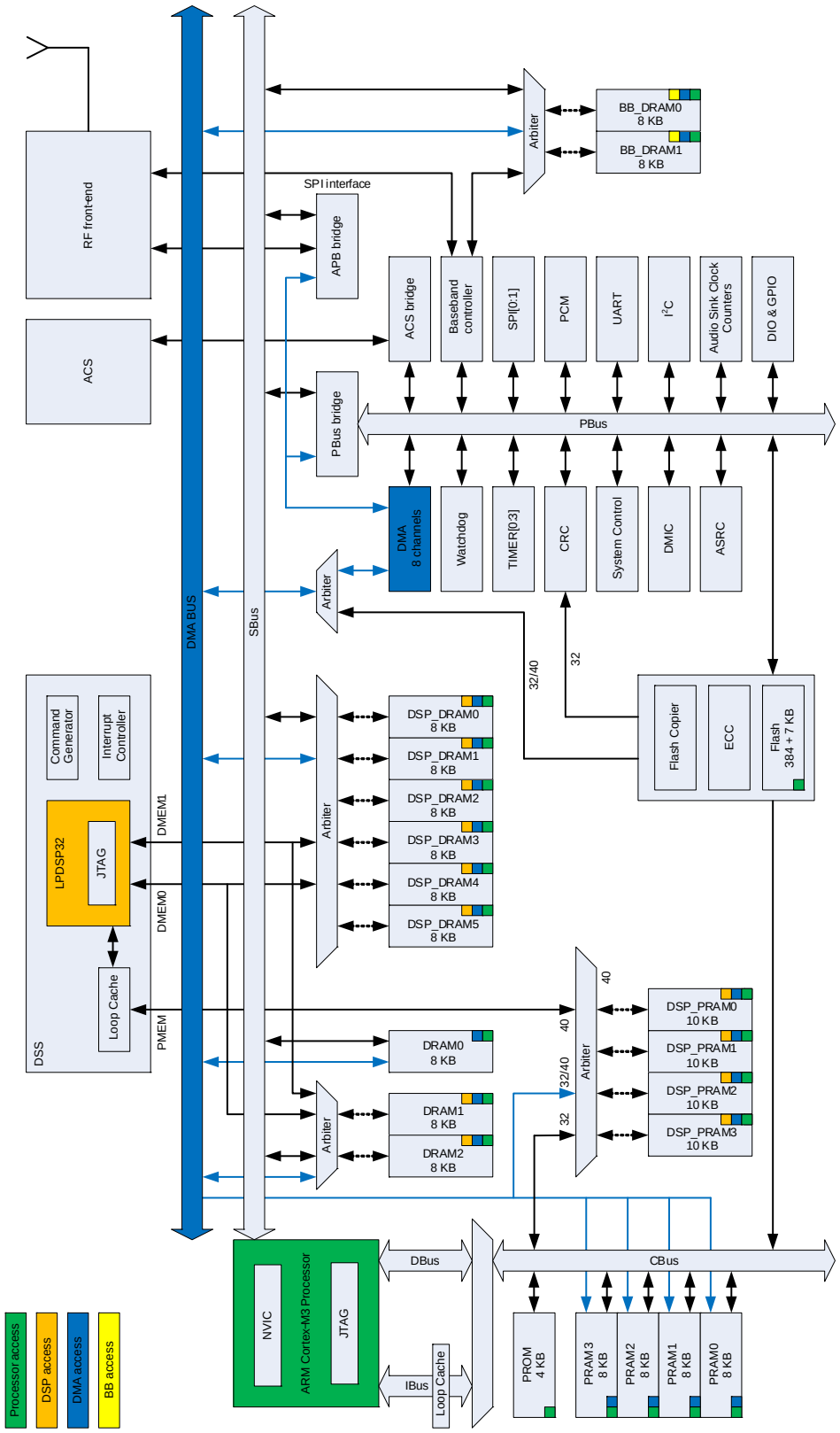


Figure 4. RSL10 Architecture

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Power Management Unit

The RSL10 power management unit allows for operation across wide temperature and voltages ranges at low power consumption and monitors the battery voltage to ensure reliable operation. If the battery voltage dips below the POWER−ON RESET (POR) voltage, a POR is asserted to the system. This also prevents possible damage to RSL10 when the battery is inserted or removed.

RSL10 allows the use of either the DC−DC converter for a better efficiency when the battery voltage is higher than 1.4 V or the internal LDO when VBAT is lower than 1.4 V. The output of the DC−DC converter or the LDO regulator is used to supply other voltage regulator blocks of RSL10. These blocks are:

- A programmable voltage regulator to supply the digital cores (VDDC)
- A programmable voltage regulator to supply the memories (VDDM)
- A charge pump supplying the analog blocks and the flash memory (VDDA)
- A programmable voltage regulator to supply the radio front−end (VDDRF)
- A programmable voltage regulator to supply the power amplifier of the radio (VDDPA): This regulator is used only for the +6 dBm output power case or if we want to transmit at +3 dBm output power with a battery level less than 1.4 V. The VDDPA regulator can be disabled if RSL10 doesn't have to transmit at high power, and VDDRF only should be used.

Clock and Clocking Options

RSL10's system clock (SYSCLK) can come from various sources:

- A 48 MHz crystal oscillator, used in normal operation mode
- An internal trimmable RC oscillator that supplies a 3 MHz – 12 MHz clock used at system startup
- A Real Time Clock, used in stand−by mode, generated from one of:
  - A 32 kHz RC oscillator
  - A 32 kHz crystal oscillator
  - An external input on one of DIO0 to DIO3
- A JTAG clock, used in debug mode, coming from the JTCK pad
- An external clock source, coming from the EXTCLK pad

Every clock generated in the system can be disabled when they are not needed. Also, every clock has an associated configurable prescaler to minimize the power dissipated on the clock tree.

A clock detector unit can be used to monitor the system clock and/or the RTC clock in sleep and standby modes. In the event the clock frequency goes below a certain threshold, the RSL10 IC will be reset. The clock detector threshold is nominally 2 kHz. This block and the reset it triggers is enabled by default, but both can be disabled.

Radio Front−End

RSL10 2.4 GHz radio front−end implements the physical layer for the Bluetooth Low Energy technology standard and other standard, proprietary, and custom protocols. It operates in the worldwide deployable 2.4 GHz ISM band (2.4000 to 2.4835 GHz) and supports:

- Bluetooth 5.2 certified with LE 2M PHY support

The 2.4 GHz radio front−end is based on a low−IF architecture and comprises the following building blocks:

- High performance single−ended RF port
- On−chip matching network with 50 ohm RF input
- High gain, low power LNA (low noise amplifier), and mixer
- PA (Power Amplifier) with +3 dBm output power for Bluetooth applications, and up to +6 dBm with dedicated PA voltage supply
- ADC converter
- RSSI (Received Signal Strength Indication) with 60 dB nominal range with 2.4 dB steps (not considering AGC)
- Fully integrated ultra−low power frequency synthesis with fast settling time, with direct digital modulation in transmission (pulse shape programmable)
- 48 MHz XTAL reference (finely trimmable)
- Fully−integrated FSK−based modem with programmable pulse shape, data rate, and modulation index
- Digital baseband (DBB) with Link layer functionalities, including automatic packet handling with preamble & sync, CRC, and separate Rx and Tx 128−bytes FIFOs
- Serial and parallel digital interfaces

The 2.4 GHz radio front−end contains a full transceiver with the following features:

- Manchester encoding
- Data whitening

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The 2.4 GHz radio front−end contains also a highly−flexible digital baseband−in terms of modulations, configurability and programmability – in order to support Bluetooth Low Energy technology, and DSSS, and proprietary protocols. It allows for programmable data rates from 62.5 kbps up to 2 Mbps, FSK with programmable pulse shape and modulation index.

The 2.4 GHz radio front−end also include Manchester encoding and Data whitening. Its packet handling includes:

- Automatic preamble and sync word insertion
- Automatic packet length handler
- Basic address check
- Automatic CRC calculation and verification with a programmable CRC polynomial
- Multi−frame support
- 2x128 byte FIFOs

Baseband Controller and Software Stack

The RSL10 Bluetooth baseband controller is connected to the radio front−end. It configures the physical layer of the RSL10 for use as a Bluetooth Low Energy technology device. It provides access and support for the Direct−Test Mode (DTM) layer for RF testing, and it implements portions of the link layer and other controller level components from the Bluetooth stack. It is dedicated to low level bitwise operations and data packet processing.

RSL10 is Bluetooth 5.2 certified and includes LE 2 Mbps support and all optional features from earlier versions of Bluetooth Low Energy technology.

Also, the coexistence between Bluetooth and a custom protocol is supported.

The software stack, including the profiles and the application, handles the protocol functions and is executed on the Arm Cortex−M3 processor. The Bluetooth IP implementation is split among software and hardware as shown in Figure 5.

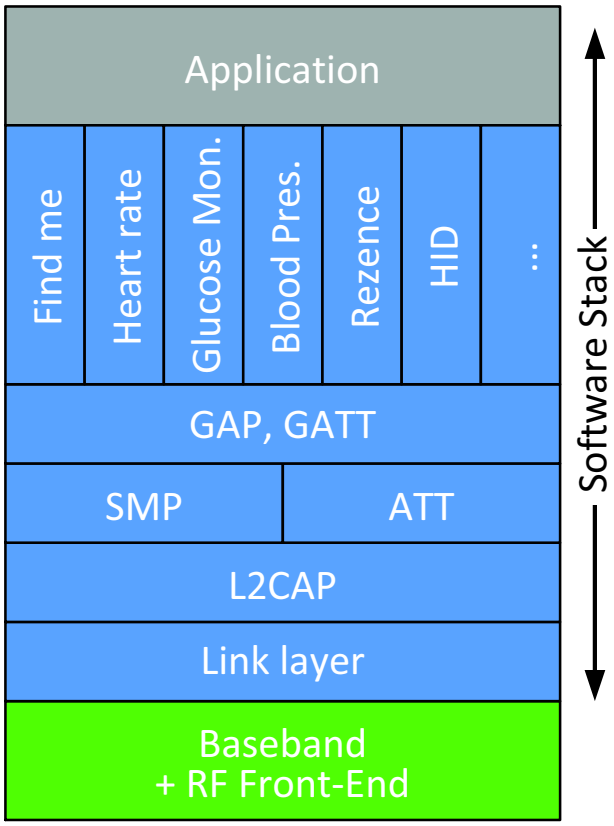


Figure 5. Bluetooth Protocol Implementation

The following is a sample of the Bluetooth Low Energy profiles supported by RSL10. For more information and a complete list of the profiles offered, please download the RSL10 SDK.

- Find Me
- Proximity
- HID over GATT (HOG)
- Alert Notification
- Phone Alert Status
- Location and Navigation
- Rezence (custom protocol defined by AirFuel™ Alliance to support wireless battery charging)

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Arm Cortex−M3 Processor Subsystem

The Arm Cortex−M3 processor subsystem includes the Arm Cortex−M3 processor, which is the master processor of the RSL10 chip. It also contains the Bluetooth baseband controller, and all interfaces and other peripherals.

Arm Cortex−M3 Processor

The Arm Cortex−M3 processor is a state−of−the−art 32−bit core with embedded multiplier and ALU for handling typical control functions. Software development is done in C.

It features a low gate count, low interrupt latency, and low−cost debug functionality. It is primarily intended for deeply embedded applications that require low power consumption with fast interrupt response. The processor implements the Arm architecture v7−M. For power management, the processor can be placed under firmware control, into a Standby mode, in which the processor clock is disabled. The Nested Vectored Interrupt Controller (NVIC) will continue to run to enable exiting Standby mode on an interrupt.

LPDSP32

LPDSP32 is a C−programmable, 32−bit DSP developed by **onsemi**. LPDSP32 is a high efficiency, dual Harvard DSP that supports both single (32−bit) and double precision (64−bit) arithmetic.

LPDSP32's dual MAC unit, load store architecture is specifically optimized to support audio processing tasks. The advanced architecture also provides:

- Two 72−bit ALUs capable of doing single and double precision arithmetic and logical operations
- Two 32−bit integer/fractional multipliers
- Four 64−bit accumulators with 8−bit overflow (extension bits)

Communications to the Arm Cortex−M3 processor are completed via interrupts and shared memories. Software development is done in C, and the development tools are provided upon request from Synopsys.

Interfaces

RSL10 includes:

- Two independent SPI interfaces that can be configured in master and slave mode
- A fully configurable PCM interface
- A standard general purpose I^2C interface
- A standard general purpose UART interface
- Two PWM (Pulse Width Modulation) drivers that can generate a single bit output signal at a given frequency
- SWJ−DP interface for the Arm Cortex−M3 processor
- JTAG interface for the Arm Cortex−M3 processor, internal Flash memory, and the LPDSP32

RSL10 includes 16 DIO pads (Digital Input/Output) that all can be assigned to any of the interfaces above, or used as general purpose DIOs.

Peripherals

RSL10 includes:

- Four general purpose timers
- A DMA (Direct Memory Access) controller to transfer data between peripherals and memories without any core intervention
- A flash copier to initialize SRAM memories and that can be used with the CRC blocks to validate flash memory contents
- An Analog to Digital converter (ADC), accessed by the Arm Cortex−M3 processor. The ADC can read 4 external values (DIO[0]−DIO[3]), AOUT, VDDC, VBAT/2 and the ADC offset value.
- Two standard Cyclic Redundancy Code (CRC) blocks to ensure data integrity of the user application code and data
- A Watchdog timer to detect and recover from RSL10 malfunctions.
- Four autonomous 32−bit Activity Counters. These counters help analyze how long the system has been running and how much the Arm Cortex−M3 processor, LPDSP32, and the flash memory have been used by the application. This is useful information to estimate and optimize the power consumption of the application.
- An IP protection system to ensure that the flash content cannot be copied by a third party. It can be used to prevent any core or memory of the RSL10 from being accessed externally after the RSL10 has booted.
- Program memory loop caches for each processor to reduce the RSL10 power consumption. This reduces the number of flash and RAM memory accesses by caching the program words that are read in these loops.

RSL10 Memory Structure

Table 9 lists the memory structures attached to RSL10, and the size and width of each memory structure.

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Table 9. RSL10 MEMORY STRUCTURES

Memory type	Data Width	Memory Size	Accessed by
Program memory (ROM)	32	4 kB	Arm Cortex−M3 processor
Program memory (RAM)	32	4 instances of 8 kB	Arm Cortex−M3 processor
Program memory (RAM)	40	4 instances of 10 kB	LPDSP32 / Arm Cortex−M3 processor
Data memory (RAM)	32	1 instances of 8 kB	Arm Cortex−M3 processor
Data memory (RAM)	32	2 instances of 8 kB	Arm Cortex−M3 processor / LPDSP32
Data memory (RAM)	32	6 instances of 8 kB	LPDSP32 / Arm Cortex−M3 processor
Data memory (RAM)	32	2 instances of 8 kB	Baseband / Arm Cortex−M3 processor
Flash	32	384 kB	Arm Cortex−M3 processor / Flash copier

Chip Identification

System identification is used to identify different system components. For the RSL10 chip, the key identifier components and values are as follows:

- Chip Family: 0x09
- Chip Version: 0x01
- Chip Major Revision: 0x01

Electrostatic Discharge (ESD) Sensitive Device

CAUTION: ESD sensitive device. Permanent damage may occur on devices subjected to high−energy electrostatic discharges. Proper ESD precautions in handling, packaging and testing are recommended to avoid performance degradation or loss of functionality.

Solder Information

The RSL10 QFN package is constructed with all RoHS compliant material and should be reflowed accordingly.

This device is Moisture Sensitive Class MSL1 and must be stored and handled accordingly. Re−flow according to IPC/JEDEC standard J−STD−020C, Joint Industry Standard: Re−flow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices. Hand soldering is not recommended for this part.

For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Development Tools

RSL10 is supported by a full suite of comprehensive tools including:

- An easy−to−use development board
- Software Development Kit (SDK) including an Oxygen Eclipse−based development environment, Bluetooth protocol stacks, sample code, libraries, and documentation

Export Control Classification Number (ECCN)

The ECCN designation for RSL10 is 5A991.g

Company or Product Inquiries

For more information about **onsemi** products or services visit our Web site at http://onsemi.com.

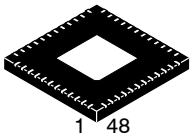
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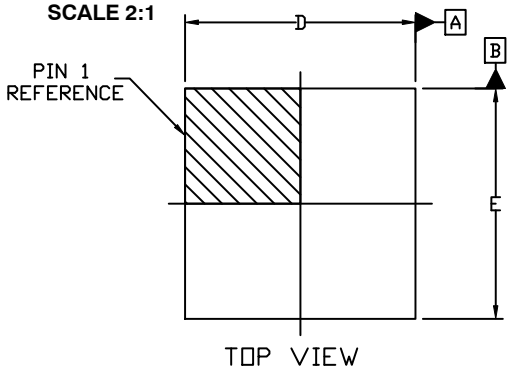
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QFNW48 7x7, 0.5P
CASE 512AD
ISSUE B

DATE 18 JAN 2019



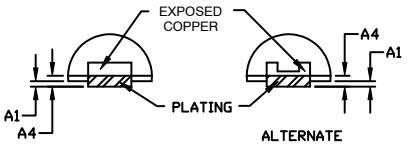
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TOP VIEW

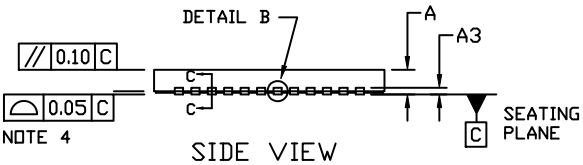
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

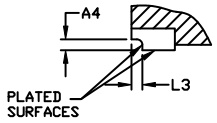


DETAIL B

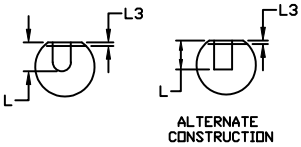
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	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	---	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.20	0.25	0.30
D	6.90	7.00	7.10
D2	3.00	3.10	3.20
E	6.90	7.00	7.10
E2	3.00	3.10	3.20
e	0.50 BSC		
K	1.55 REF		
L	0.30	0.40	0.50
L3	0.05 REF		



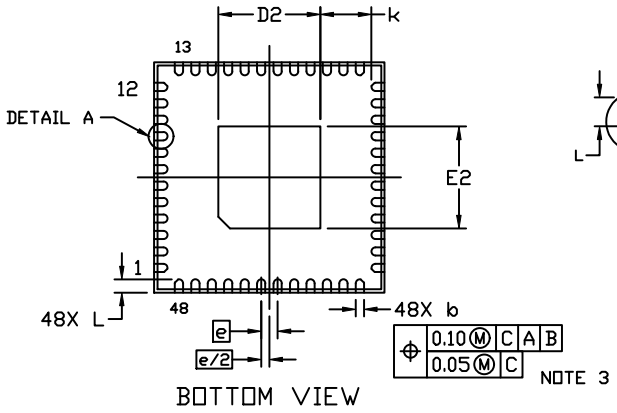
SIDE VIEW



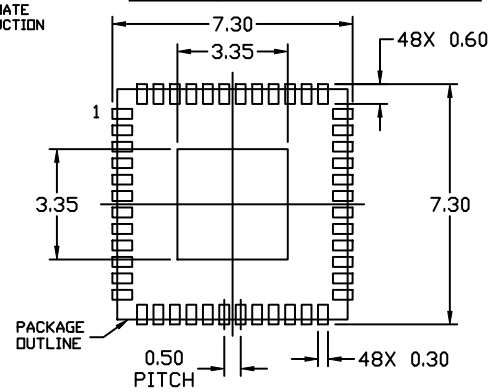
SECTION C-C



DETAIL A

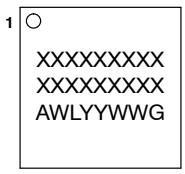


BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC
MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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