TLC6C5912-Q1 Power Logic 12-Channel Shift Register LED Driver

1 Features

- Qualified for Automotive Applications
- Wide V_{CC} Range from 3 V to 5.5 V
- Output Maximum Rating of 40 V
- Twelve Power DMOS Transistor Outputs of 50-mA Continuous Current With V_{CC} = 5 V
- Thermal Shutdown Protection
- Enhanced Cascading for Multiple Stages
- All Registers Cleared With Single Input
- Low Power Consumption
- Slow Switching Time (t_r and t_f), Which Helps Significantly With Reducing EMI
- 20-Pin TSSOP-PW Package
- 20-Pin DW Package

2 Applications

- Instrumentation Clusters
- Tell-Tale Lamps
- LED Illumination and Controls

3 Description

The TLC6C5912-Q1 is a monolithic, medium-voltage, low-current power 12-bit shift register designed for use in systems that require relatively moderate load power, such as LEDs.

This device contains a 12-bit serial-in, parallel-out shift register that feeds a 12-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift register clear ($\overline{CLR}$) is high. A low on $\overline{CLR}$ clears all registers in the device. Holding the output enable ($\overline{G}$) high holds all data in the output buffers low, and all drain outputs are off. Holding $\overline{G}$ low makes data from the storage register transparent to the output buffers.

When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink-current capability. The serial output (SER OUT) clocks out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This provides improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference. The device contains a built-in thermal shutdown protection.

Outputs are low-side, open-drain DMOS transistors with output ratings of 40 V and 50-mA continuous sink-current capabilities when V_{CC} = 5 V. The current limit decreases as the junction temperature increases for additional device protection. The device also provides up to 2000 V of ESD protection when tested using the human-body model and 200 V when tested using the machine model.

The TLC6C5912-Q1 characterization is for operation over the operating ambient temperature range of −40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC6C5912-Q1	SOIC (20)	12.80 mm × 7.50 mm
	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic

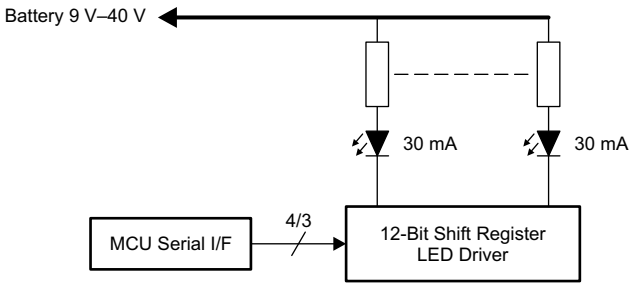


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2015) to Revision C — **Page**

- Changed $r_{DS(on)}$ test condition from 50 mA to 20 mA ... 5
- Added the *Receiving Notification of Documentation Updates* section ... 16

Changes from Revision A (January 2013) to Revision B — **Page**

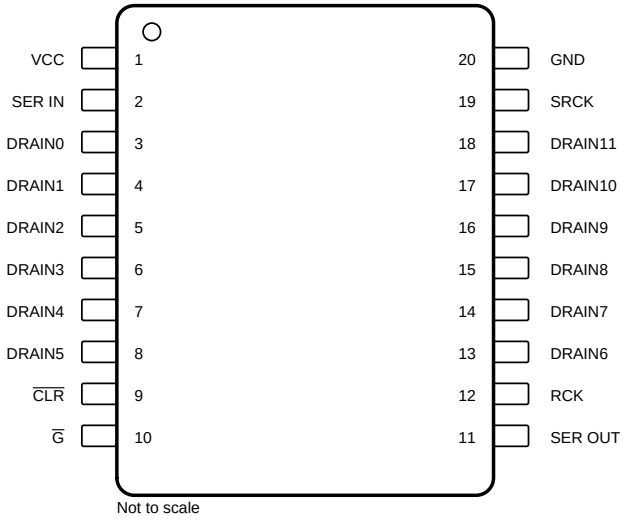
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (December 2012) to Revision A — **Page**

- Changed the device status from PRODUCT PREVIEW to PRODUCTION DATA ... 1

5 Pin Configuration and Functions

PW Package
20-Pin TSSOP
Top View



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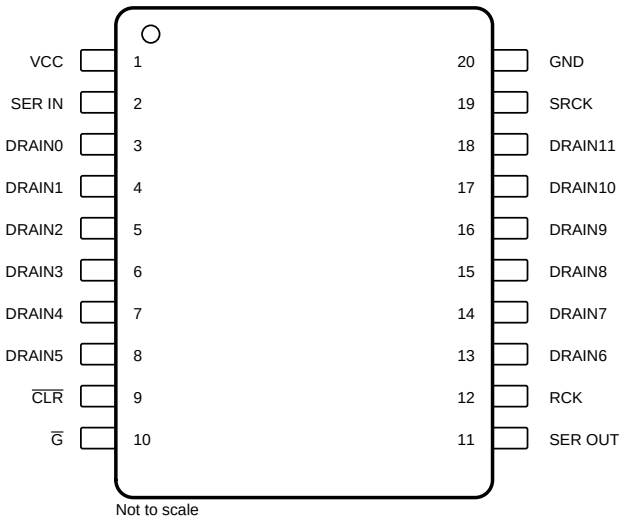
DW Package
20-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{CLR}$	9	I	**Shift register clear, active-low:** $\overline{CLR}$ is the signal used to clear all the registers. The storage register transfers data to the output buffer when shift register clear $\overline{CLR}$ is high. Driving $\overline{CLR}$ is low clears all the registers in the device.
DRAIN0	3	O	**Open-drain output:** DRAIN0 to DRAIN11 are the LED current-sink channels. These pins connect to the LED cathodes, and they can survive up to 40-V LED supply voltage. This is quite helpful during automotive load-dump conditions.
DRAIN1	4	O	
DRAIN2	5	O	
DRAIN3	6	O	
DRAIN4	7	O	
DRAIN5	8	O	
DRAIN6	13	O	
DRAIN7	14	O	
DRAIN8	15	O	
DRAIN9	16	O	
DRAIN10	17	O	
DRAIN11	18	O	
$\overline{G}$	10	I	**Output enable, active-low:** $\overline{G}$ is the LED channel enable and disable input pin. Having $\overline{G}$ low enables all drain channels according to the output-latch register content. When high, all channels are off.
GND	20	—	**Power ground:** GND is the ground reference pin for the device. This pin must connect to the ground plane on the PCB.
RCK	12	I	**Register clock:** RCK is the storage register clock. The data in each shift register stage transfers to the storage register at the rising edge of RCK. Data in the storage register appears at the output whenever the output enable $\overline{G}$ input signal is high.
SER IN	2	I	**Serial-data input:** SER IN is the serial data input. Data on SER IN loads into the internal register on each rising edge of SRCK.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SER OUT	11	O	**Serial-data output:** SER OUT is the serial data output of the 12−bit serial shift register. The purpose of this pin is to cascade several devices on the serial bus. By connecting the SER OUT pin to the SER IN input of the next device on the serial bus to cascade, the data transfers to the next device on the falling edge of SRCK. This can improve the cascade application reliability, as it can avoid the issue that the second device receives SRCK and data input at the same rising edge of SRCK.
SRCK	19	I	**Shift-register clock:** SRCK is the serial clock input. On each rising SRCK edge, data transfers from SER IN to the internal serial shift registers.
V_{CC}	1	I	**Power supply:** V_{CC} is the power supply pin voltage for the device. TI recommends adding a 0.1 μF ceramic capacitor close to the pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Logic supply voltage		8	V
V_I	Logic input-voltage	–0.3	8	V
V_{DS}	Power DMOS drain-to-source voltage		42	V
	Continuous total dissipation	See *Thermal Information*		
	Operating ambient temperature (Top)		125	°C
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	165	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	5.5	V
V_{IH}	High-level input voltage	2.4		V
V_{IL}	Low-level input voltage		0.7	V
t_{su}	Setup time, SER IN high before SRCK↑	15		ns
t_h	Hold time, SER IN high after SRCK↑	15		ns
t_w	Pulse duration	40		ns
T_C	Operating case temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TLC6C5912-Q1		UNIT
		20 PINS		
		PW (TSSOP)	DW (SOIC)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.8	81.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.1	45.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.3	49.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.7	17.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.8	48.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	DRAIN0 to DRAIN11, drain-to-source voltage					40	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = –20 μA	V_{CC} = 5 V	4.9	4.99		V
		I_{OH} = –4 mA		4.5	4.69		
V_{OL}	Low-level output voltage, SER OUT	I_{OH} = 20 μA	V_{CC} = 5 V		0.001	0.01	V
		I_{OH} = 4 mA			0.25	0.4	
I_{IH}	High-level input current	V_{CC} = 5 V, V_I = V_{CC}			0.2		μA
I_{IL}	Low-level input current	V_{CC} = 5 V, V_I = 0			–0.2		μA
I_{CC}	Logic supply current	V_{CC} = 5 V, No clock signal	All outputs off		0.1	1	μA
			All outputs on		130	170	
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5 MHz, C_L = 30 pF, all outputs on			300		μA
I_{DSX}	Off-state drain current	V_{DS} = 30 V, V_{CC} = 5 V				0.1	μA
		V_{DS} = 30 V, T_C = 125°C, V_{CC} = 5 V			0.15	0.3	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 20 mA, V_{CC} = 5 V, T_A = 25°C, single channel ON		6	7.4	8.6	Ω
		I_D = 20 mA, V_{CC} = 5 V, T_A = 25°C, all channels ON		6.7	8.9	9.6	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 25°C, single channel ON		7.9	9.3	11.2	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 25°C, all channels ON		8.7	10.6	12.3	
		I_D = 20 mA, V_{CC} = 5 V, T_A = 125°C, single channel ON		9.1	11.2	12.9	
		I_D = 20 mA, V_{CC} = 5 V, T_A = 125°C, all channels ON		10.3	13	14.5	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 125°C, single channel ON		11.6	13.7	16.4	
		I_D = 20 mA, V_{CC} = 3.3 V, T_A = 125°C, all channels ON		12.8	15.6	18.2	
$T_{SHUTDOWN}$	Thermal shutdown trip point			150	175	200	°C
T_{HYS}	Hysteresis				15		°C

6.6 Switching Characteristics

V_{CC} = 5 V, T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	C_L = 30 pF, I_D = 48 mA		210		ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$			75		ns
t_r	Rise time, drain output			250		ns
t_f	Fall time, drain output			200		ns
t_{pd}	Propagation delay time, SRCK↓ to SEROUT	C_L = 30 pF, I_D = 48 mA		35		ns
T_{or}	SEROUT rise time (10% to 90%)	C_L = 30 pF		20		ns
T_{of}	SEROUT fall time (90% to 10%)	C_L = 30 pF		20		ns

Switching Characteristics (continued)

V_{CC} = 5 V, T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SRCK)}$	Serial clock frequency	C_L = 30 pF, I_D = 20 mA			10	MHz
T_{SRCK_WH}	SRCK pulse duration, high		30			ns
T_{SRCK_WL}	SRCK pulse duration, low		30			ns

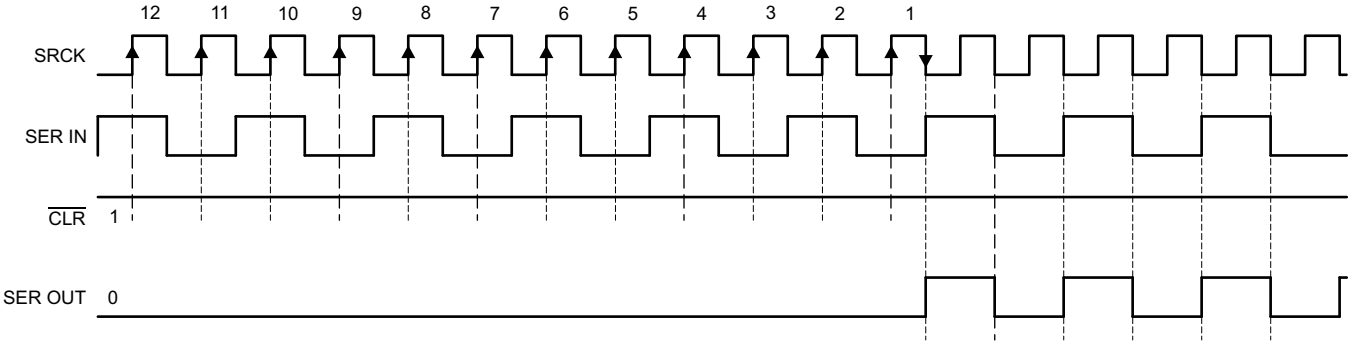


Figure 1. SER IN to SER OUT Waveform

Figure 1 shows the SER IN to SER OUT waveform. The output signal appears on the falling edge of the shift register clock (SRCK) because there is a phase inverter at SER OUT (see Figure 2). As a result, it takes seven and a half periods of SRCK for data to transfer from SER IN to SER OUT.

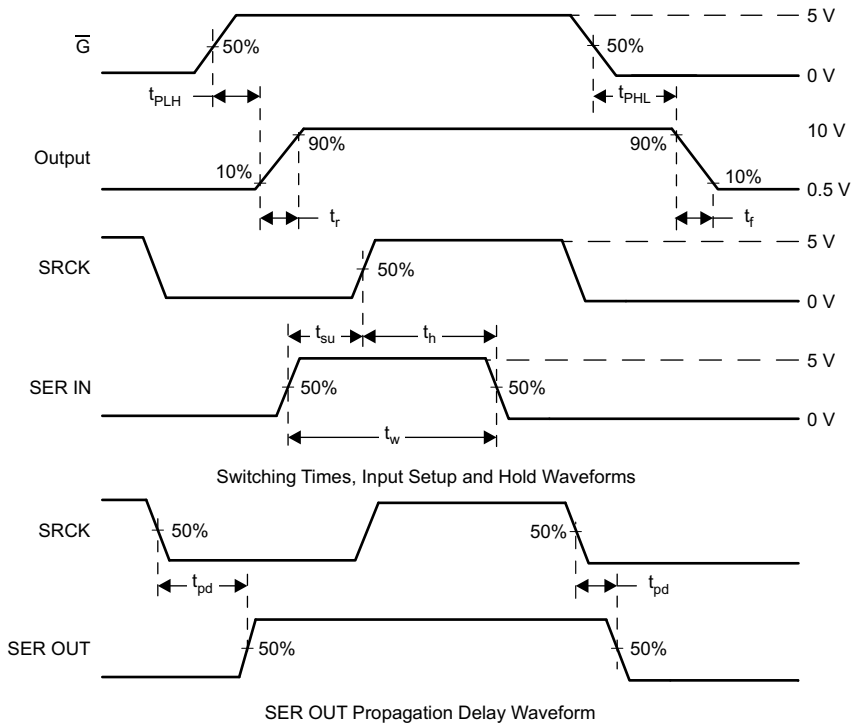


Figure 2. Switching Times and Voltage Waveforms

Figure 2 shows the switching times and voltage waveforms. Tests for all these parameters took place using the test circuit shown in Figure 12.

6.7 Typical Characteristics

Conditions for Figure 5 and Figure 6: Single channel on; conditions for Figure 7, Figure 8, and Figure 9: All channels on.

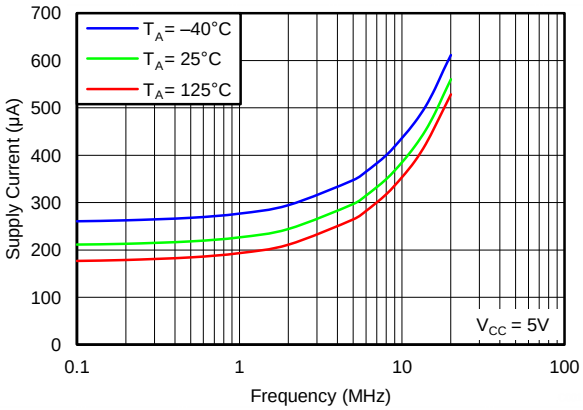


Figure 3. Supply Current vs Frequency

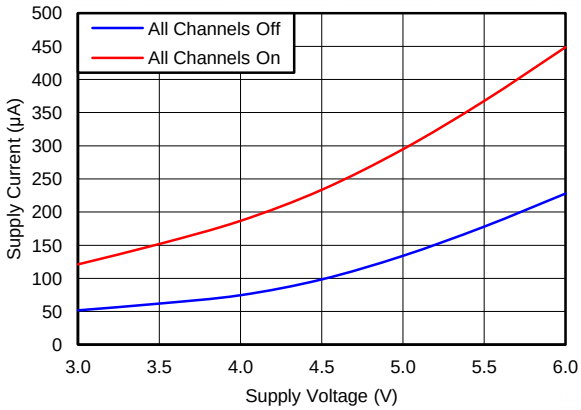


Figure 4. Supply Current vs Supply Voltage

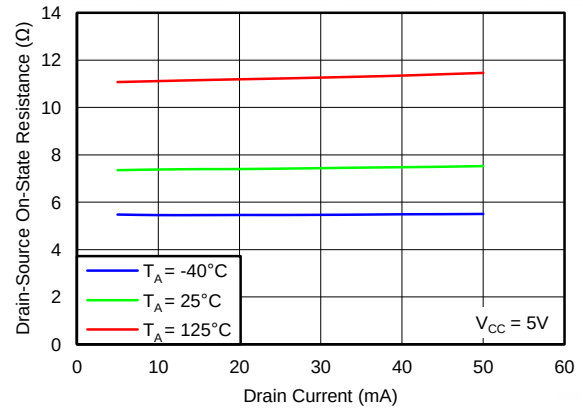


Figure 5. Drain-to-Source On-State Resistance vs Drain Current

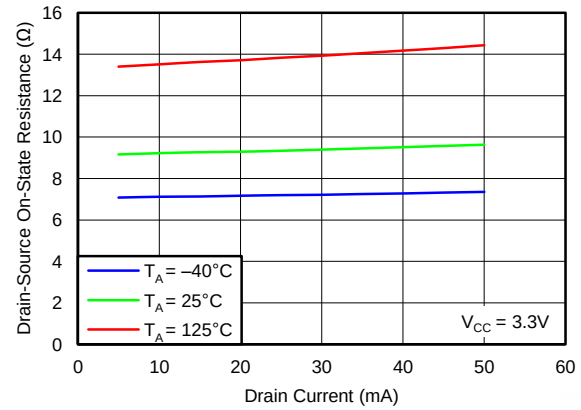


Figure 6. Drain-to-Source On-State Resistance vs Drain Current

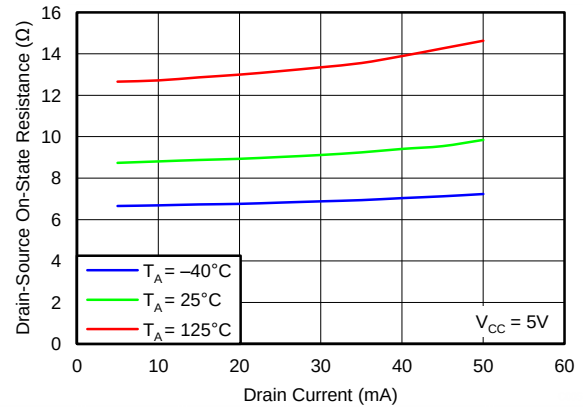


Figure 7. Drain-to-Source On-State Resistance vs Drain Current

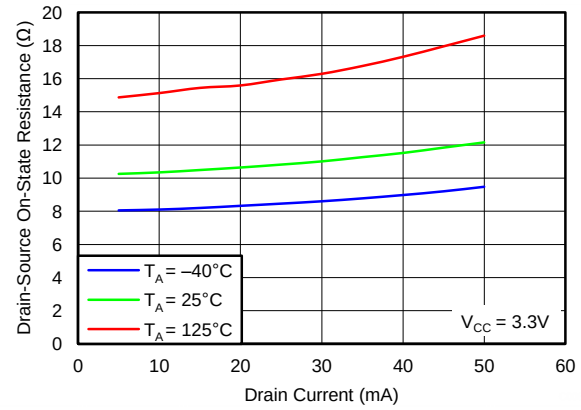


Figure 8. Drain-to-Source On-State Resistance vs Drain Current

Typical Characteristics (continued)

Conditions for Figure 5 and Figure 6: Single channel on; conditions for Figure 7, Figure 8, and Figure 9: All channels on.

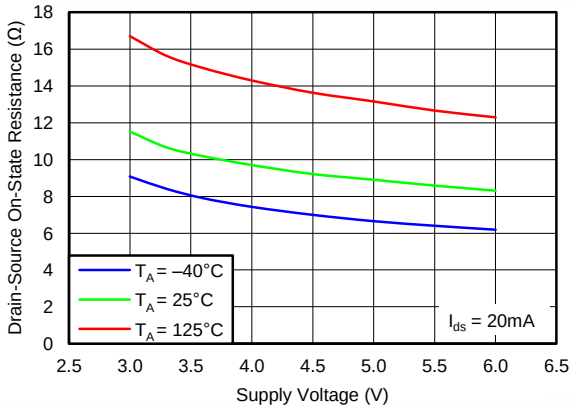


Figure 9. Drain-to-Source On-State Resistance vs Drain Current

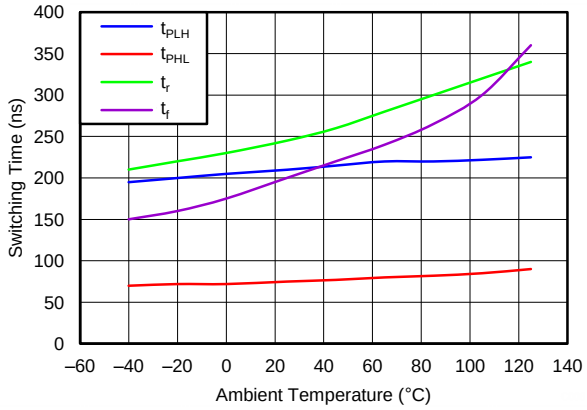
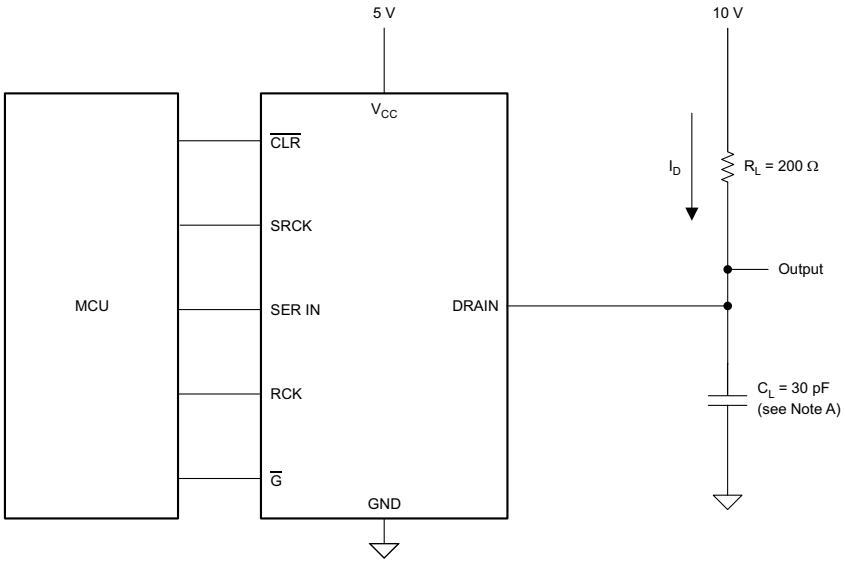


Figure 10. Switching Time vs Ambient Temperature

7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

Figure 11. Resistive-Load Test Circuit

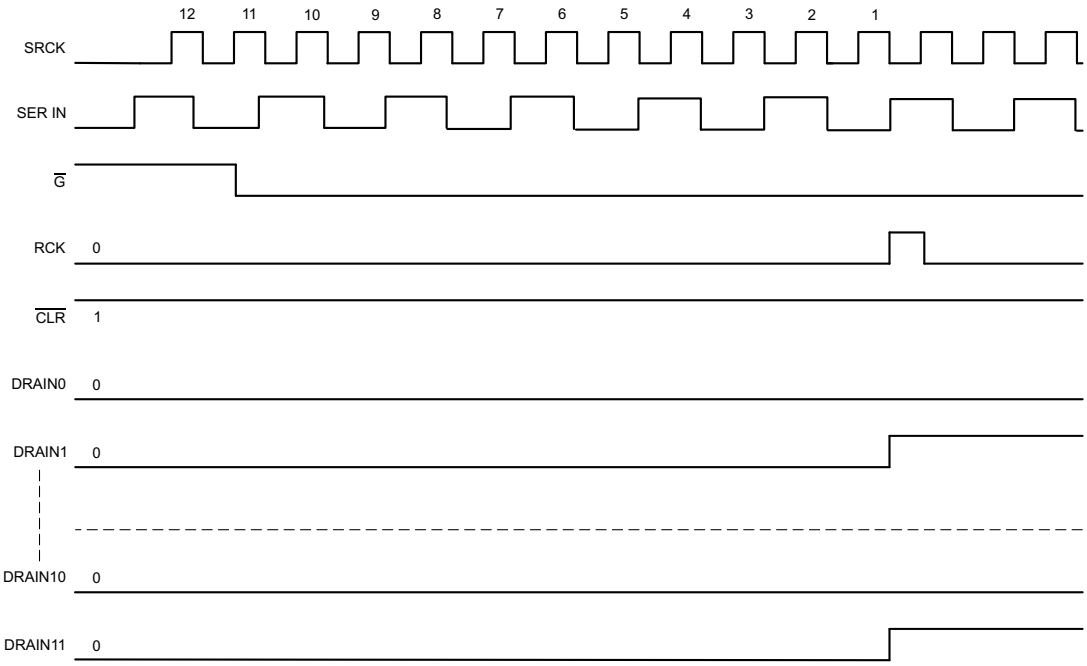


Figure 12. Voltage Waveforms

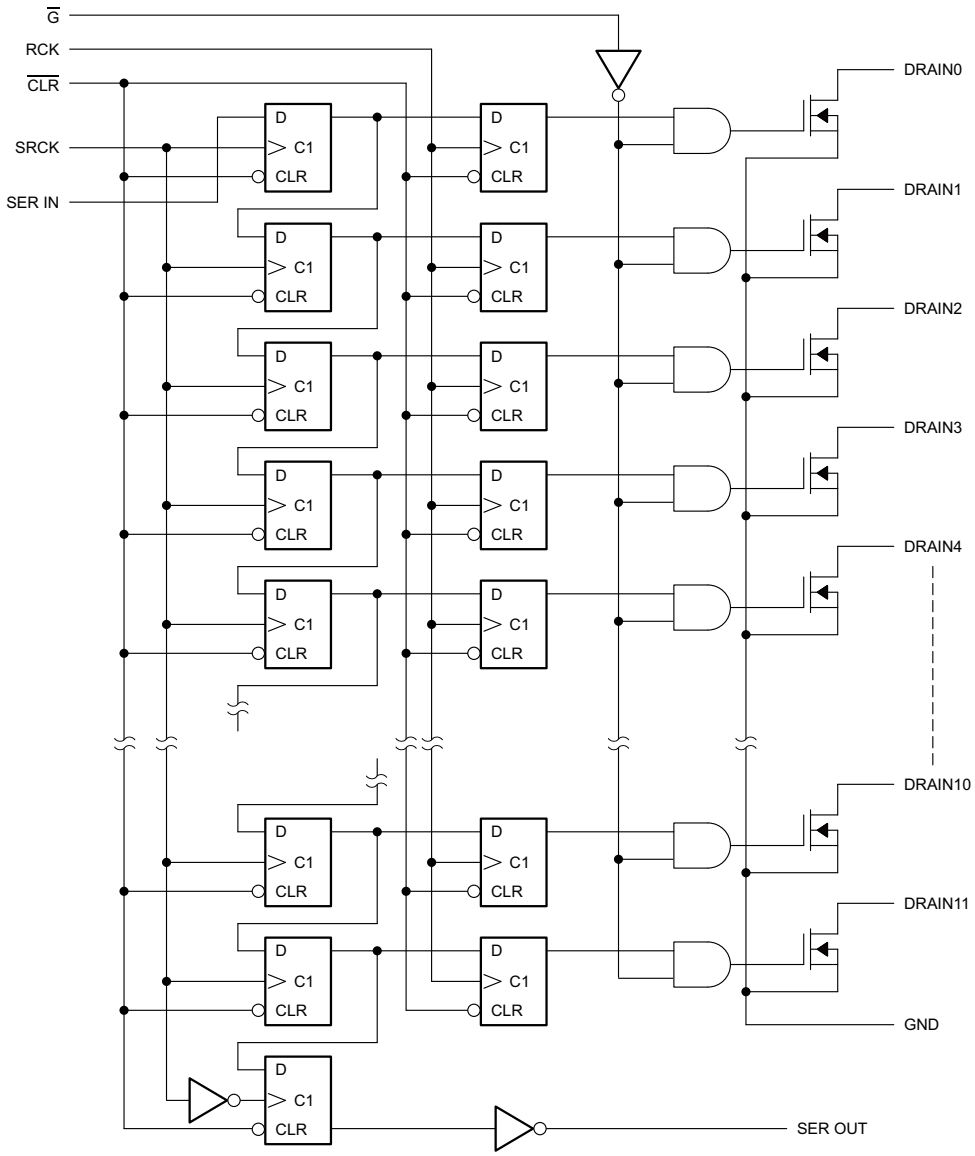
Figure 11 and Figure 12 show the resistive-load test circuit and voltage waveforms. One can see from Figure 12 that with $\overline{G}$ held low and $\overline{CLR}$ held high, the status of each drain changes on the rising edge of the register clock, indicating the transfer of data to the output buffers at that time.

8 Detailed Description

8.1 Overview

The TLC6C5912-Q1 device is a monolithic, medium-voltage, low current 12-bit shift register designed to drive relatively moderate load power such LEDs. The device contains a 12-bit serial-in, parallel-out shift register that feeds a 12-bit D-type storage register. Thermal shutdown protection is also built-into the device.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 175°C (typical). The thermal shutdown forces the device to have an open state when the junction temperature exceeds the thermal trip threshold. Once the junction temperature decreases to less than 160°C (typical), the device begins to operate again.

Feature Description (continued)

8.3.2 Serial-In Interface

The TLC6C598 device contains an 8-bit serial-in, parallel out shift register that feeds an 8-bit D-type storage register. Data transfer through both the shift and storage registers on the rising edge of the shift register clock (SRCK) and the register clock (RCK), respectively. The storage transfers data to the output buffer when shift register clear (CLR) is high.

8.3.3 Clear Register

A logic low on $\overline{CLR}$ clears all registers in the device. TI suggests clearing the device during power up or initialization.

8.3.4 Cascade Through SER OUT

By connecting the SER OUT pin to the SER IN input of the next device on the serial bus to cascade, the data transfers to the next device on the falling edge of SRCK. This can improve the cascade application reliability, as it can avoid that the second device receives SRCK and data input at the same rising edge of SRCK.

8.3.5 Output Control

Holding the output enable (G) high holds all data in the output buffers low, and all drain outputs are off. Holding G low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs are capable of sink-current. This pin also be used for global PWM dimming.

8.4 Device Functional Modes

8.4.1 Operation With V_{CC} < 3 V

This device works normally during 3 V ≤ V_{CC} ≤ 5.5 V, when operation voltage is lower than 3 V. The behavior of device cannot be ensured, including communication interface and current capability.

8.4.2 Operation With 5.5 V ≤ V_{CC} ≤ 8 V

The device works normally during this voltage range, but reliability issues may occurs while the device works for a long time in this voltage range.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLC6C5912-Q1 device is a serial-in, parallel-out, power logic 8-bit shift register with low-side open-drain DMOS output rating of 40 V and 50-mA continuous sink-current capabilities when V_{CC}= 5 V. The device is designed to drive resistive loads and is particularly well-suited as an interface between a microcontroller and LEDs or lamps. The device also provides up to 2000 V of ESD protection when tested using the human body model and 200 V when using the machine model.

9.2 Typical Application

Figure 13 shows a typical cascade application circuit with two TLC6C5912-Q1 chips configured to cascade topology. The MCU generates all the input signals.

Typical Application (continued)

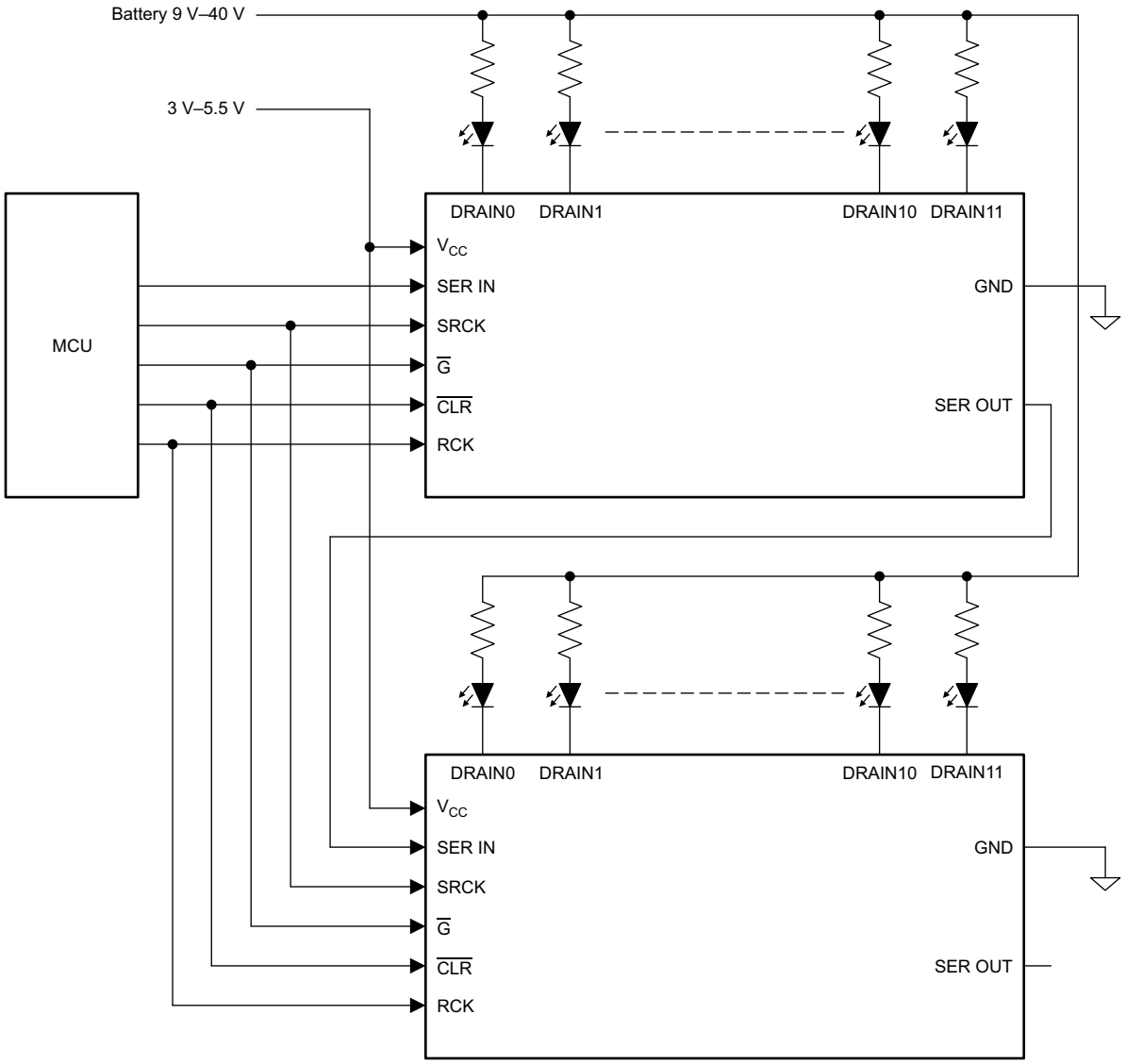


Figure 13. Typical Application Circuit

9.2.1 Design Requirements

Table 1 lists the parameters for this design example.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Vbattery	9 to 40 V
V_{CC}_1	3.3 V
I(D0), I(D1), I(D2), I(D3) , I(D4), I(D5), I(D6), I(D7), I(D8), I(D9), I(D10), I(D11)	30 mA
V_{CC}_2	5 V
I(D12), I(D13), I(D14), I(D15) , I(D16), I(D17), I(D18), I(D19), I(D20), I(D21), I(D122), I(D23)	50 mA

9.2.2 Detailed Design Procedure

To begin the design process, the designer must decide on a few parameters:

- Vsupply: LED supply voltage
- VDx: LED forward voltage
- I: LED current

After determining the parameters, calculate the resistor in series with LED using Equation 1.

$$Rx = (Vsupply – VDx) / I \quad (1)$$

9.2.3 Application Curve

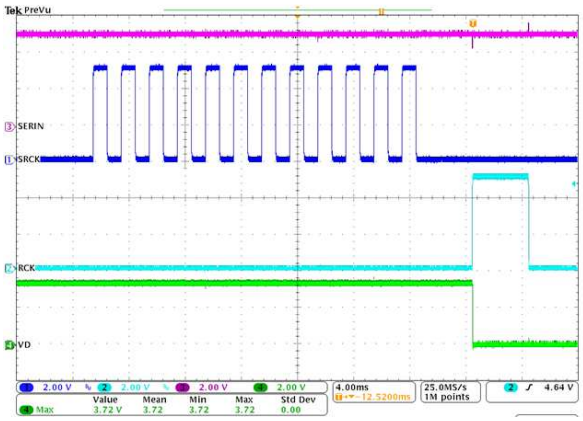


Figure 14. TLC6C5912-Q1 Application Waveform

10 Power Supply Recommendations

The TLC6C5912-Q1 device is designed to operate from an input voltage supply range from 3 V to 5.5 V. This input supply should be well regulated. TI recommends placing the ceramic bypass capacitors near the V_{CC} pin.

11 Layout

11.1 Layout Guidelines

There are no special layout requirement for the digital signal pins. The only requirement is placing the ceramic bypass capacitors near the corresponding pin.

Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the cooper on the PCB. Maximizing the copper coverage is extremely important when the design does not include heat sinks attached to the PCB on the other side of the package.

- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should be either plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

11.2 Layout Example

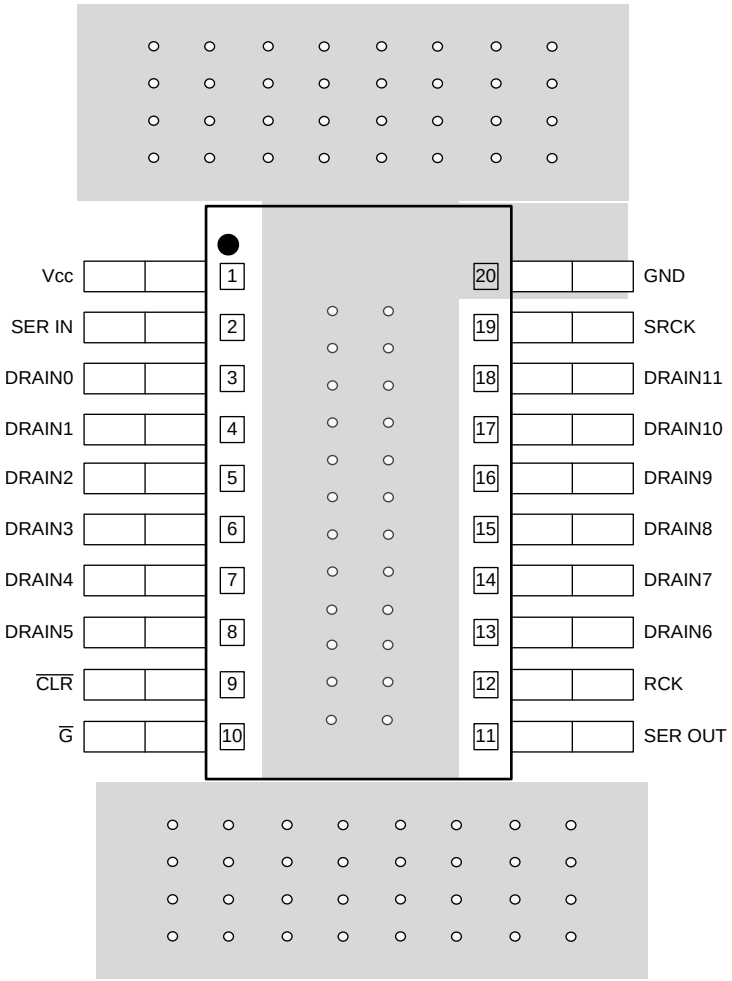


Figure 15. Layout Recommendation

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC6C5912GQPWRQ1	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	6C5912G
TLC6C5912GQPWRQ1.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	6C5912G
TLC6C5912QDWRQ1	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TLC6C5912
TLC6C5912QDWRQ1.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TLC6C5912
TLC6C5912QPWRQ1	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	6C5912
TLC6C5912QPWRQ1.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	6C5912

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLC6C5912-Q1 :

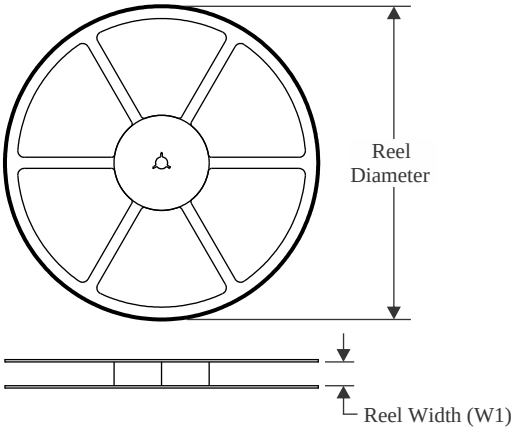
- Catalog : TLC6C5912

NOTE: Qualified Version Definitions:

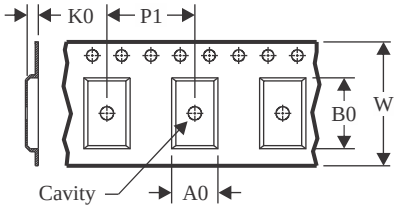
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

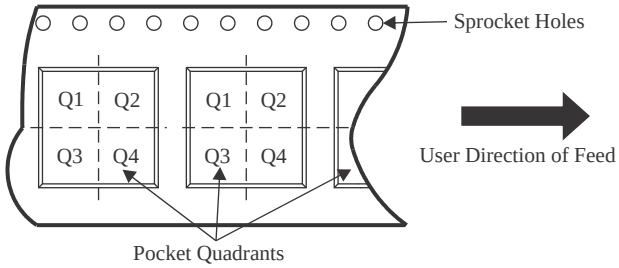


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

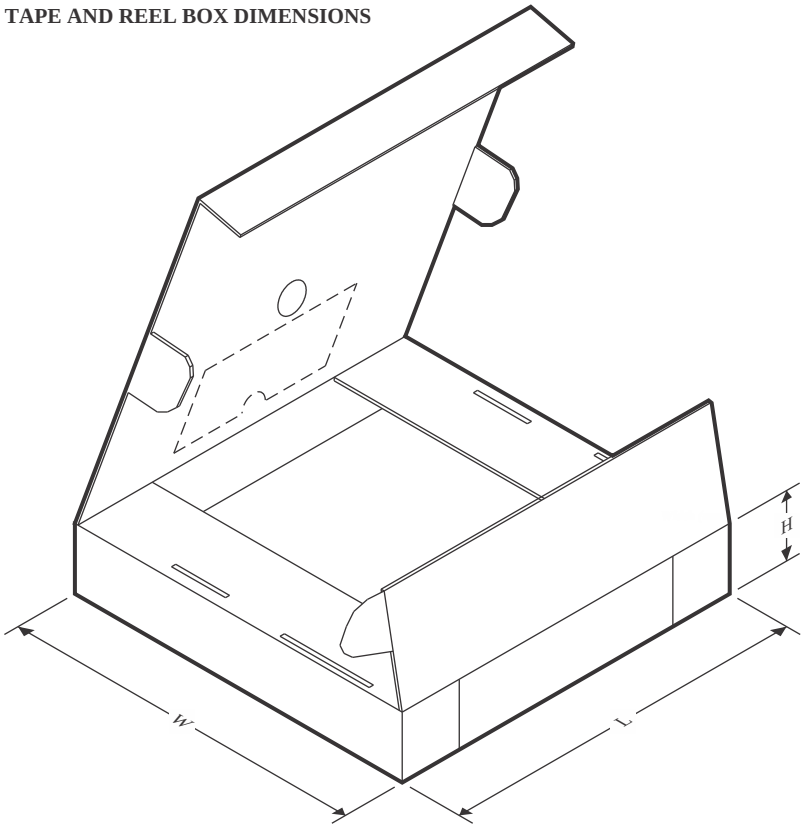
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

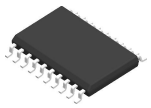
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC6C5912GQPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLC6C5912QDWRQ1	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLC6C5912QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC6C5912GQPWRQ1	TSSOP	PW	20	2000	350.0	350.0	43.0
TLC6C5912QDWRQ1	SOIC	DW	20	2000	367.0	367.0	45.0
TLC6C5912QPWRQ1	TSSOP	PW	20	2000	350.0	350.0	43.0

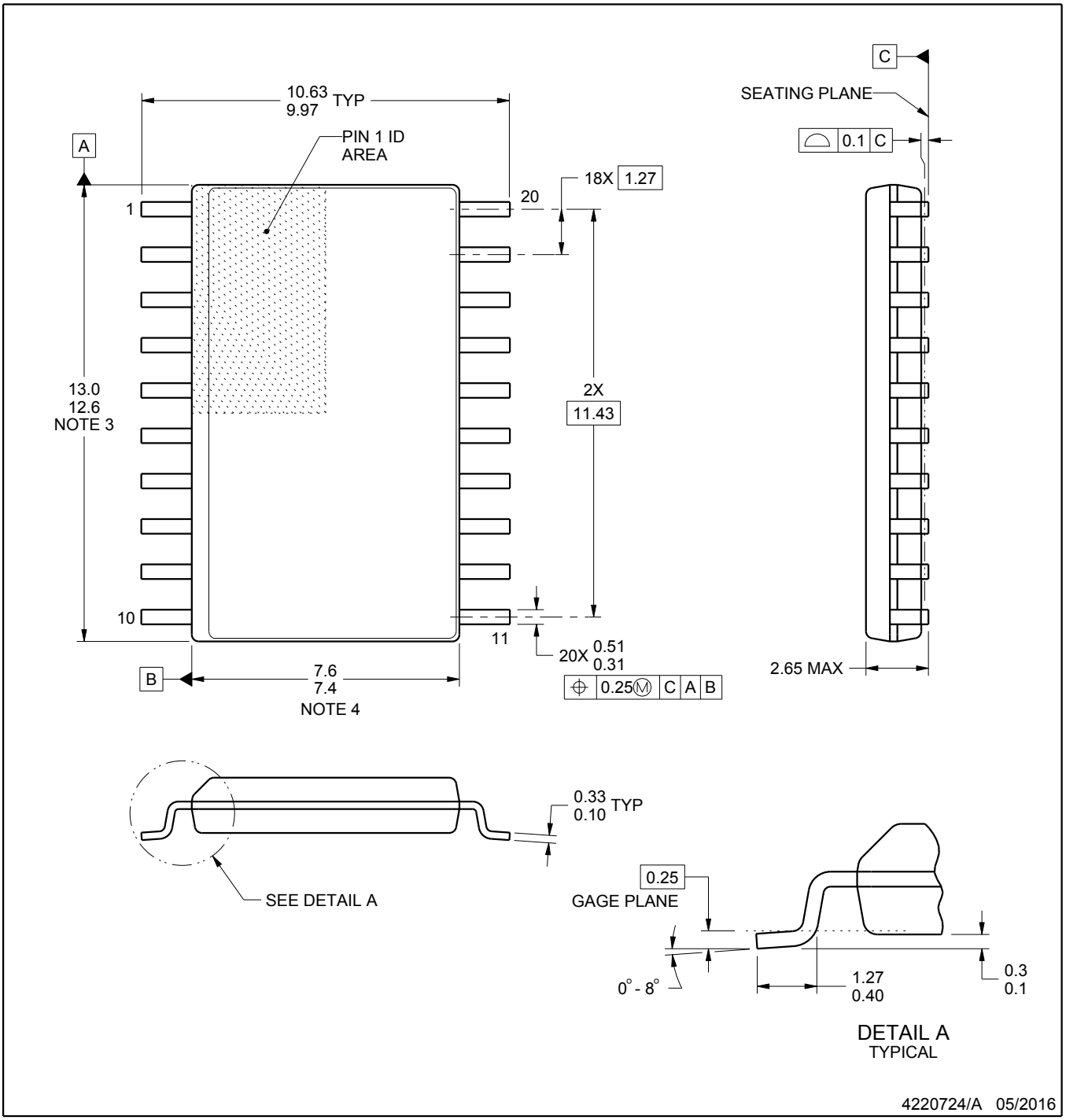


PACKAGE OUTLINE

DW0020A

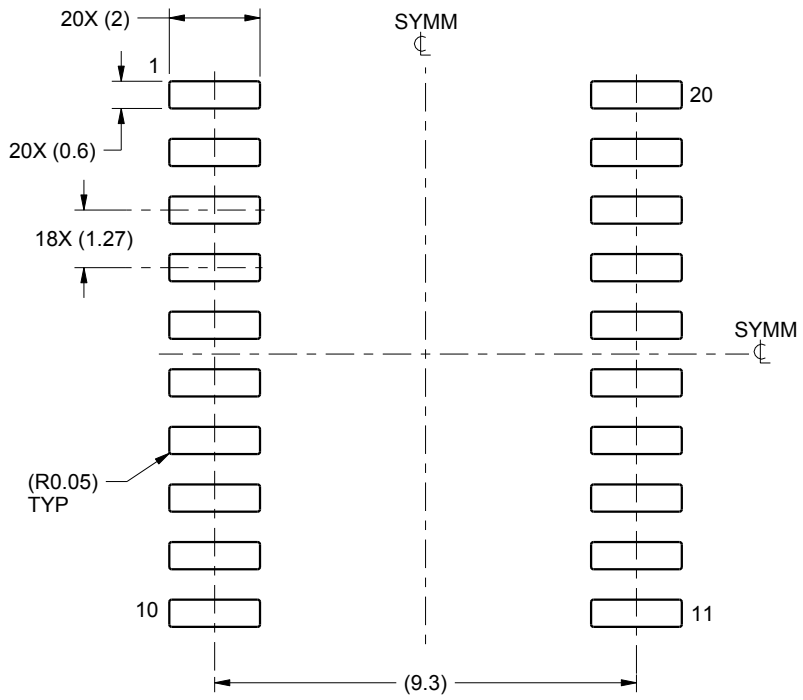
SOIC - 2.65 mm max height

SOIC

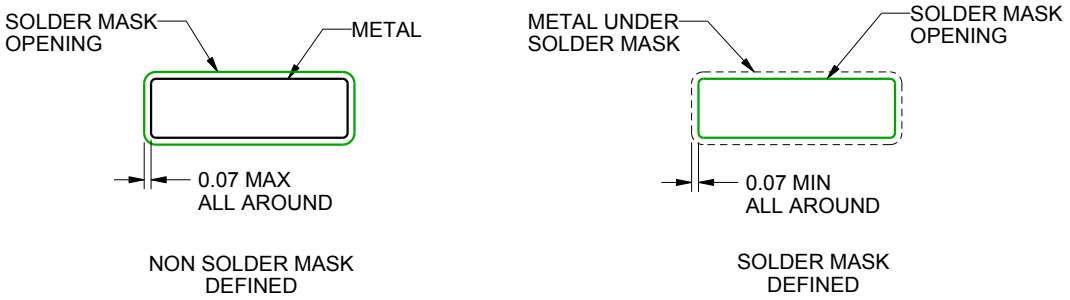


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

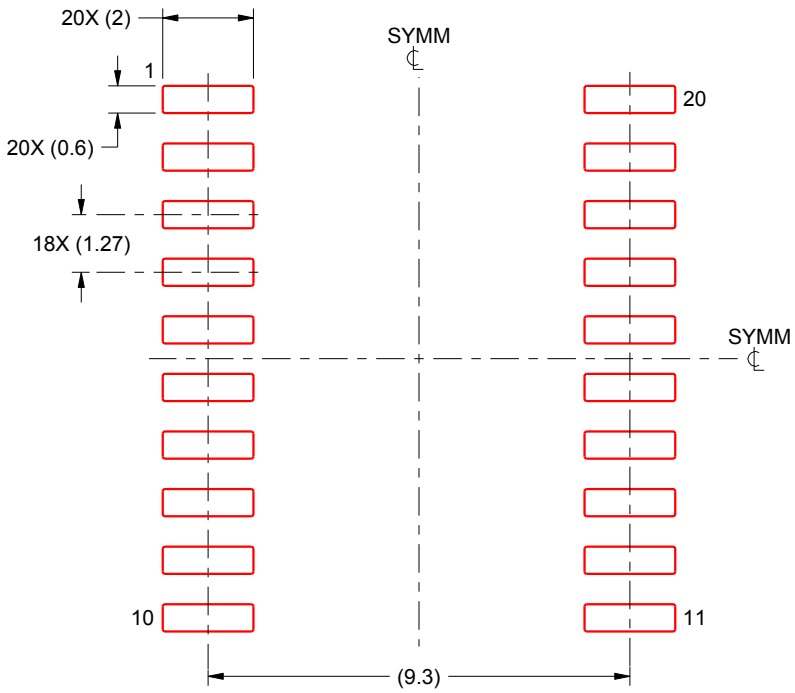


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

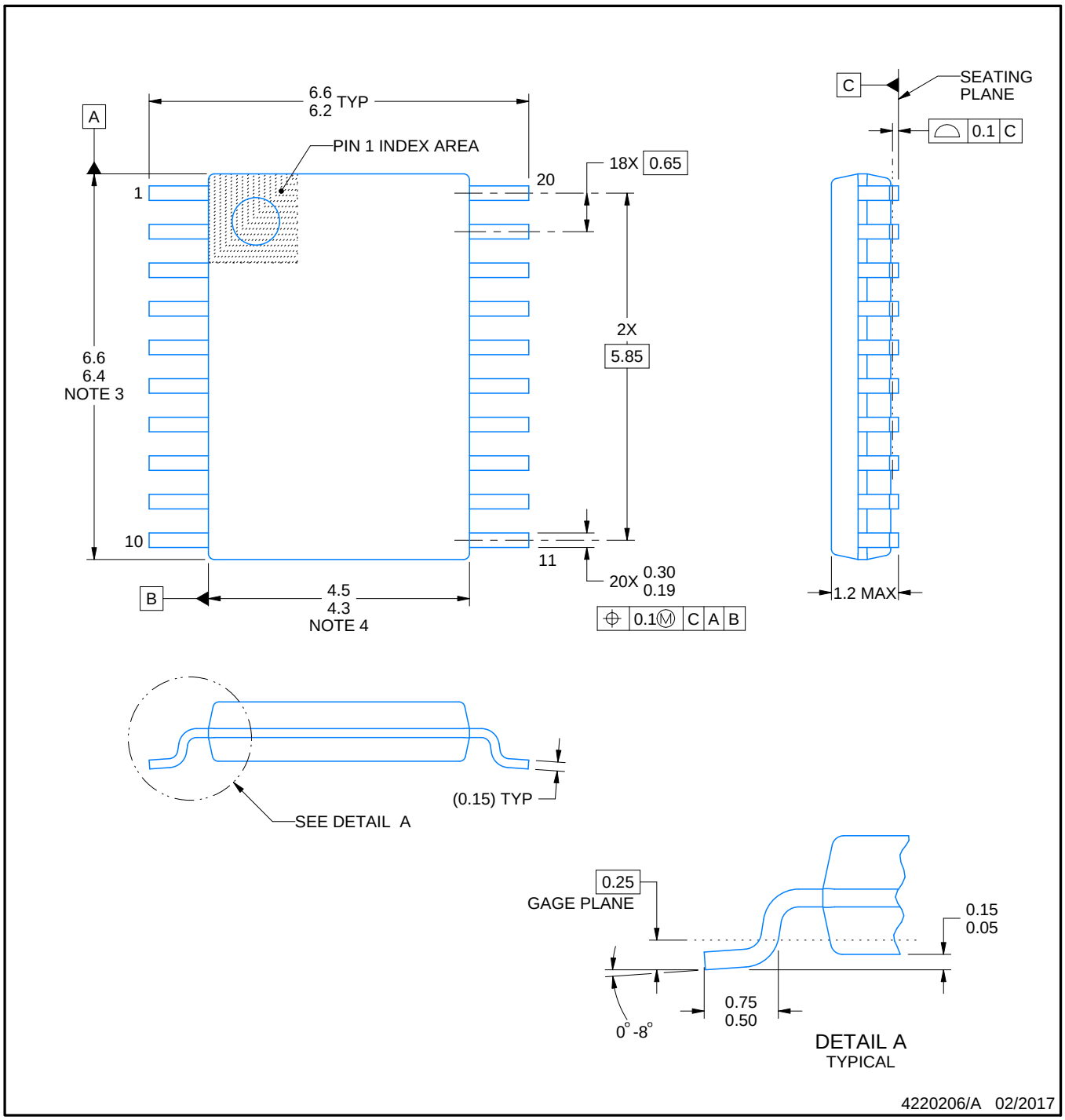
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

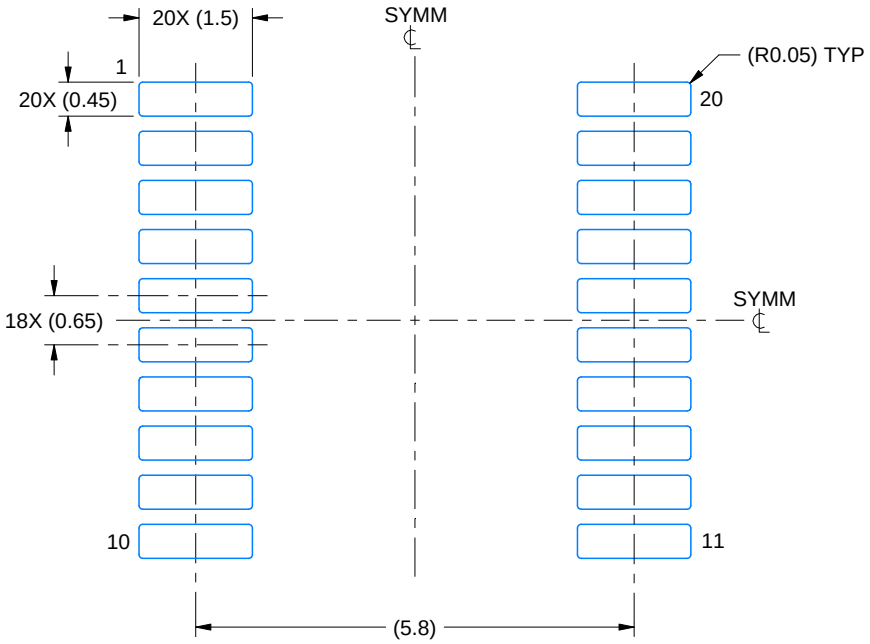
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



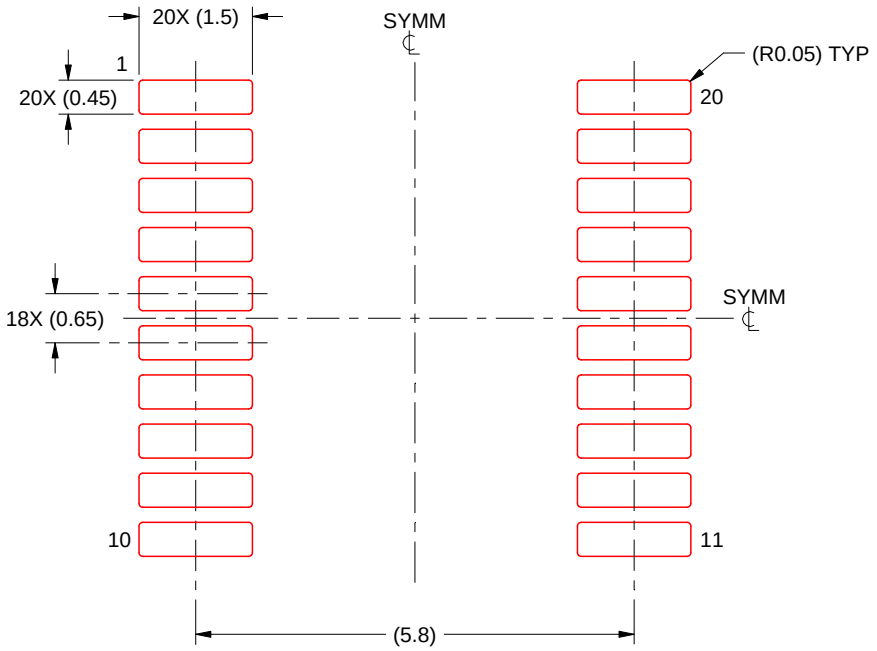
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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